Three-Level Buck Quasi-Square-Wave dc-dc Converter

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***Abstract*—The challenges for future more electric aviation requires the investigation of new topologies and technologies able to switch at high frequencies. The proposal of this paper is to apply quasi-square-wave (QSW) technique to a three-level buck converter. On QSW, the demagnetization of the power inductor is allowed to reach zero or even negative values of current, and thus zero voltage switching (ZVS) is achieved. By soft-switching, the converter can be optimized to efficiency increase or weight/volume reduction. The limits and conditions for a three-level buck converter are defined in the paper. Experimental validation is obtained via a 50 kW-rated prototype, where two continuous conduction mode (CCM) and two QSW scenarios are compared.**

***Index Terms*—Three-level buck, QSW, Soft-switching, ZVS, dc-dc conversion.**

I. Introduction

Environmental awareness has become one of the main drivers of greener technologies development. The aerospace sector alone contributes with 2.4% of the global CO_2 levels and it is expected to increase in future [1]. To countermeasure it, commercial aerospace has been shifting towards more electric aircraft, as installed electric loads yield the replacement of the heavier heritage hydraulic/pneumatic systems [2]. Future electrical aircraft distribution will have availability to much higher voltages due to the use of electric propulsion, with voltages being higher than 1kV [1]. Projects such as the Clean Aviation's Hybrid Electric Regional Aircraft Distribution Technologies (HECATE), for instance, envision the propulsion bus operating at voltage levels between 800V to 1500V [3], imposing serious challenges on its kW-level dc-dc power conversion.

Although the use of silicon carbide (SiC) devices has greatly matured over the last years [4], current commercial availability of SiC power modules narrows down for devices above 1.7kV breakdown voltage, turning two-level topologies impracticable for high-voltage propulsion systems reaching up to 3kV [1], [5]. An option to overcome the voltage constraining the power devices is the use of multi-level topologies [6]–[11]. Among the dc-dc multi-level converters, a vastly used topology is the three-level buck (Fig. 1) [7], [8]. With simple control and modulation schemes, the topology can be optimized to operate ZVS and reach high power density [8]. If compared to a traditional two-level buck converter, the three-level buck at the same switching frequency has smaller passive components and voltage stress over the semiconductors, which set an advantage in power density and specific power.

At such power levels, the cooling system can become dominant over the converter's overall weight. In order to improve efficiency and thus reduce weight and size, soft-switching becomes a must on the power stage. If not by the addition of extra hardware, soft-switching on traditional non-isolated dc-dc converters can be achieved by means of control/modulation. In triangular conduction mode (TCM) zero voltage switching (ZVS) is achieved by allowing the power inductor current to reach negative [12]–[14]. Since TCM is operated at fixed switching frequency, the converter's efficiency is severely hindered a low power operation by the elevated RMS current flowing through the inductor [14].

In quasi-square-wave (QSW) operation, the recirculating current issue from TCM is fixed by operating with variable switching frequency [14]–[16]. As the load becomes lighter, the switching frequency is increased to maintain the minimum negative current required for ZVS operation [14]. Although the necessity of operating at higher switching frequencies, the ZVS ensured throughout the operation range allows a flatter efficiency on the converter [14]. Therefore, by applying a QSW ZVS technique to the converter its switching frequency can be pushed higher resulting on even greater achievements in weight and volume reduction. Nonetheless, RMS current in QSW mode is yet larger than in CCM and adequate trade-off

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is required for an optimal design.

This paper presents the analysis, design and test of a three-level buck converter operating in QSW mode [17]. Chapter II will discuss the conditions and limits of QSW operation while Chapter III will present experimental results for validation. Finally, Chapter IV contains the conclusions over the three-level buck operating at QSW. Fig. 1 shows the three-level buck converter topology.

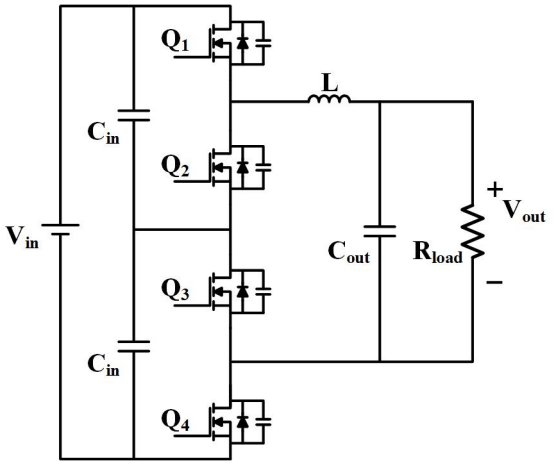

Fig. 1. Three-level buck converter.

II. Three-Level QSW Buck Operation Principle

There are two different methods of applying pulse width modulation (PWM) to the three-level buck which are characterized by the phase-shift between carriers of each pair of switches. In the first method, by having 0° phase-shift, the main switches (Q_1/Q_4) and the complementary switches (Q_2/Q_3) are synchronized and produce the same effect of a two-level buck over the inductor. In the second method the carriers are phase-shifted by 180°, thus the voltage over the inductor acquires half-cycle symmetry, meaning that the equivalent frequency over the passive elements are double the switching frequency. Such feature yields the passives to be smaller without increasing the actual switching frequency over the semiconductors [8]. The input switching voltage V_x, as illustrated in Fig. 2, depending on the duty cycle D will then swing between either 0V and V_{in}/2 for $D > 0.5$ or V_{in}/2 and V_{in} for $D < 0.5$.

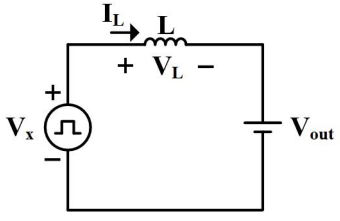

Fig. 2. Three-level buck equivalent circuit.

The main waveforms of the three-level buck operating with 180° phase-shift are presented in Fig. 3. From the half-period symmetry the volt-second balance over the inductor L can be defined as:

$$\langle V_L \rangle_{\frac{T_{sw}}{2}} = \begin{cases} (1-D)\left(\frac{V_{in}}{2} - V_{out}\right) + \left(\frac{2D-1}{2}\right)(V_{in} - V_{out}) = 0, \mathrm{D} > 0.5, \\ D\left(\frac{V_{in}}{2} - V_{out}\right) + \left(\frac{1-2D}{2}\right)(0 - V_{out}) = 0, \mathrm{D} < 0.5. \end{cases} \quad (1)$$

where T_{sw} is the switching period.

From (1), the three-level buck static gain can be defined as:

$$\frac{V_{out}}{V_{in}} = D. \quad (2)$$

As discussed in [15], the semiconductors' turn-on losses in bidirectional buck-boost converter are virtually reduced to zero by employing QSW technique. The maximum L current to guarantee QSW ZVS operation is defined as i_{ZVS} in Fig. 3. For a two-level converter operating in buck mode, i_{ZVS} can assume its maximum possible value of 0A [15] if:

$$V_{in} \geq 2V_{out}. \quad (3)$$

The importance of the condition in (3) is that it establishes the minimum QSW RMS current possible and, therefore, the lowest conductions losses on the mode [15]. Due to its 180° phase-shifted operation, the three-level buck will present two different regions of operation (shown in Fig. 3): $D > 0.5$ and $D < 0.5$. The zoomed waveforms in Fig. 3 present the ZVS operation of Q_1/Q_4 in detail for the two regions while Fig. 4 illustrates the equivalent circuits of the three-level buck at those instants.

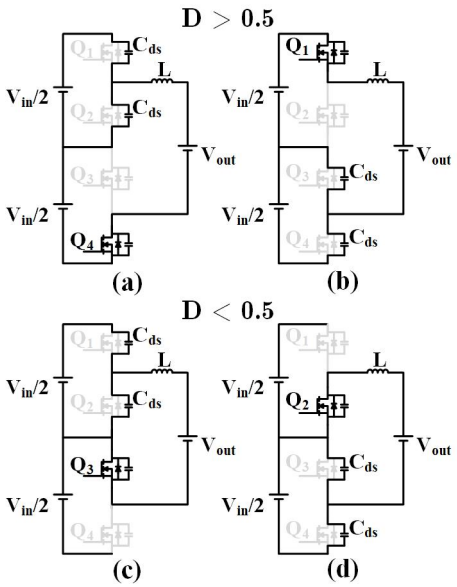

Fig. 4. Three-level buck equivalent circuit with $D > 0.5$ prior to (a) Q_1 turn-on, (b) Q_4 turn-on and $D < 0.5$ prior to (c) Q_1 turn-on and (d) Q_4 turn-on.

From Fig. 4 equivalent circuits, (3) can be adapted for a three-level as:

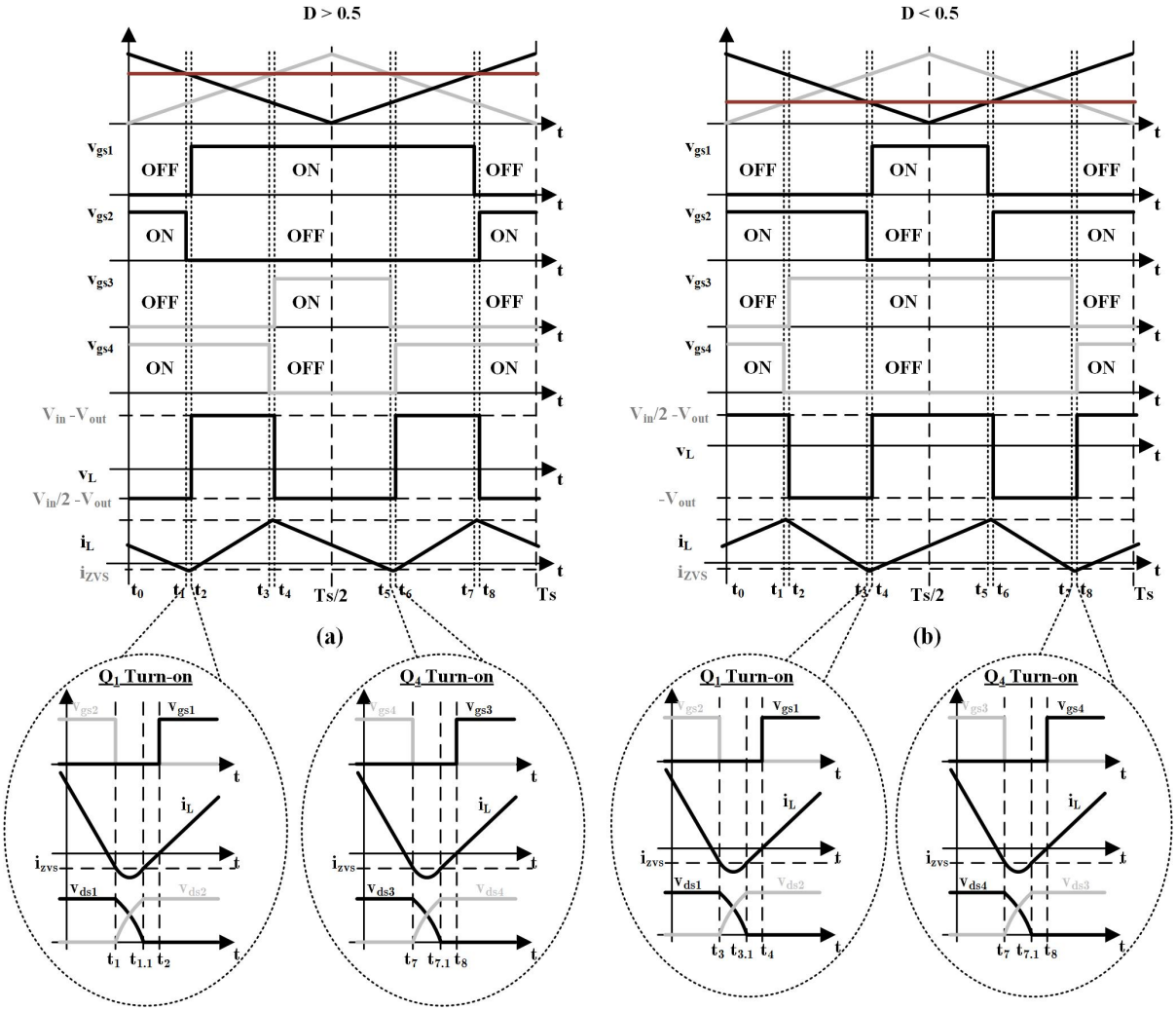

Fig. 3. Three-level buck QSW main waveforms for (a) D $>$ 0.5 and (b) D $<$ 0.5.

$$V_{in} \geq \begin{cases} 4V_{out}, & D < 0.5, \\ \frac{4}{3}V_{out}, & D > 0.5. \end{cases} \quad (4)$$

Nonetheless, conditions in (4) are not part of the design but a requirement in the project, therefore they cannot be guaranteed. In that sense, i_{ZVS} value (as introduced in Fig. 3) becomes a key point of analysis.

In order to understand the impact of i_{ZVS} on extending ZVS range, Fig. 5 presents the three-level buck state plane under two different scenarios. As can be seen in Fig. 5 (a), different output voltage (i.e., V_1, V_2 and V_3, where $V_1 > V_2 > V_3$) will incur in different A_r resonance vector length for i_{ZVS} equal to zero. While V_3 reaches zero voltage during the resonance and V_2 is the limit case, with V_1 the vector length A_{r1} is not large enough to ensure ZVS operation. In Fig. 5 (b), i_{ZVS} is set to a value smaller than zero in order to include output voltages larger than V_2 in the QSW ZVS operation. By allowing the inductor L current to reach negative values, the initial conditions of the resonance are changed, thus increasing A_r vector length.

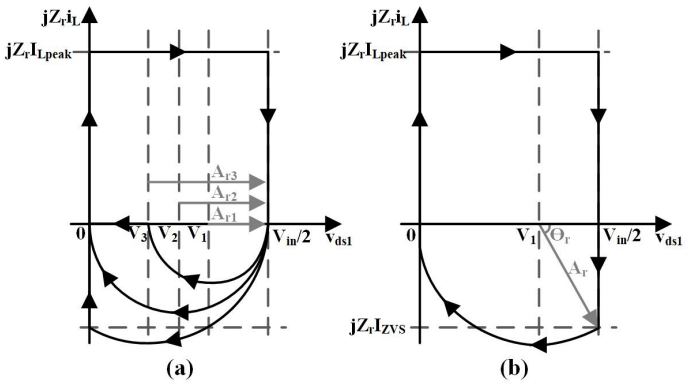

Fig. 5. Three-level buck state plane representation of a (a) switching cycle with three different output voltages and (b) switching cycle deploying negative current to achieve ZVS for larger output voltages.

From Fig. 5 (b), the vector lenght A_r can be generically defined as:

$$A_r = \sqrt{\left(\frac{V_{in}}{2} - V_{out}\right)^2 + (Z_r I_{ZVS})^2}. \quad (5)$$

Where Z_r is:

$$Z_r = \sqrt{\frac{L}{2C_{ds}}}. \quad (6)$$

As V_{out} is the sole energy source during the resonance and, therefore, the center of it (see Fig 5), the minimum value of A_r to reach ZVS is V_{out}. Thus, I_{ZVS} for the minimal RMS current can be calculated as:

$$|I_{ZVS}| \geq \frac{\sqrt{(V_{out})^2 - \left(\frac{V_{in}}{2} - V_{out}\right)^2}}{Z_r}. \quad (7)$$

III. Experimental Results

In order to experimentally validate the analysis presented, a three-level buck prototype was developed. The prototype is designed for 50 kW, but tested up to 20 kW. The main test parameters are displayed in Table I. In addition, the same prototype with different inductors will be also put under continuous conduction mode (CCM) conditions so both modes can be compared and conclusions draw on advantages and disadvantages for this applications. Table II presents the prototype main components list.

TABLE I
Experimental Test Parameters.

Parameter	Symbol	Value
Input Voltage	V_{in}	800 V
Output Voltage	V_{out}	540 V
Max Output Power	P_{out}	20 kW
Duty Cycle	D	0.675
QSW Switching Frequency	f_{sw}	7 kHz - 45 kHz
CCM Switching Frequency	f_{sw}	25 kHz & 45 kHz
Max ZVS Current	i_{ZVS}	0 A

TABLE II
Prototype Components List.

Component	Symbol	Part Number
Power Modules	Q_1, Q_2, Q_3, Q_4	BSM180D12P3C007
Gate-Drivers	-	2ASC-12A2HP
Input Capacitors	C_{in}	C4AQIEW5850A3AJ
Output Capacitors	C_{out}	C4AQIEW5850A3AJ
Inductor A*	L	Custom, 142 μH, 45 mΩ
Inductor B**	L	Custom, 5.7 μH, 0.7 mΩ
DSP	-	TMS320F28379D

*Two in series for CCM, two in parallel for low frequency QSW.
**Two in series for high frequency QSW.

Fig. 6 shows the prototype with the components listed in Table II. The power modules are not visible in the picture once they are placed underneath the PCB in order to simplify their connection to the liquid-cooled coldplate.

Four different sets of experimental results were measured from the prototype in Fig. 6: two in CCM and two in QSW. Initially, with two Inductor A in series, CCM results for 25 kHz and 45 kHz were measured for a range of load from 500 W to 20 kW. These two are intended to set the comparison with QSW. Fig. 7 presents the three-level buck main waveforms for two of the four cases commented above at 20 kW.

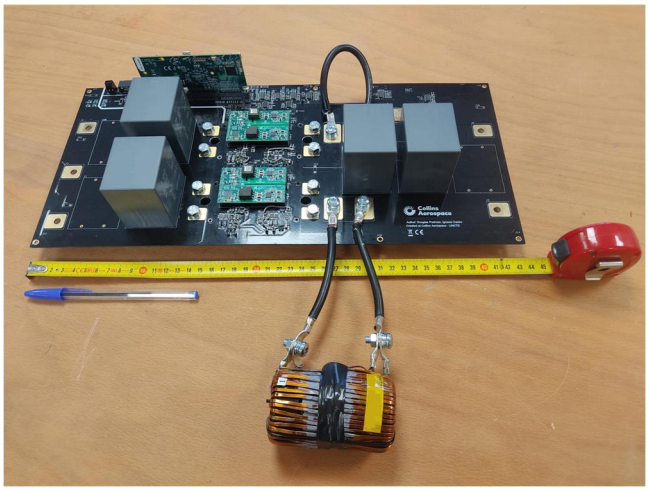

Fig. 6. 50 kW-rated three-level buck prototype at QSW configuration.

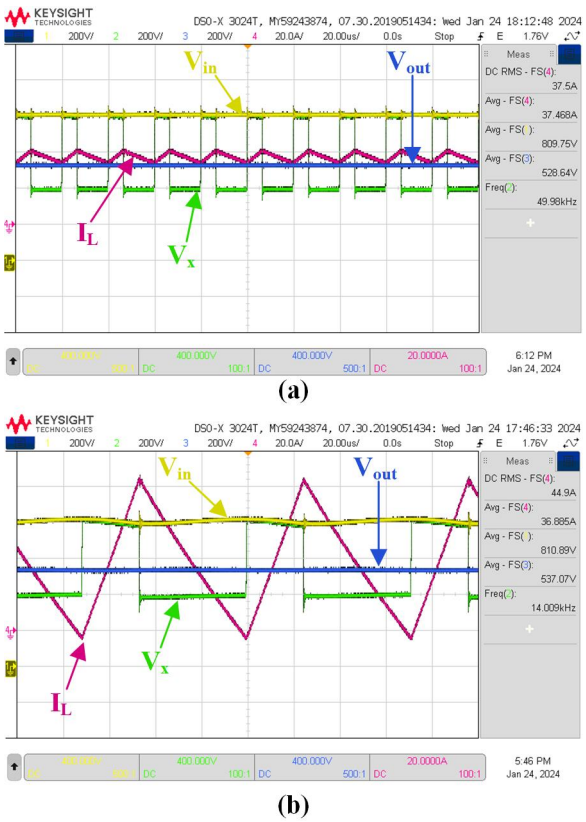

Fig. 7. Inductor current (I_L), input (V_{in}), output (V_{out}) and, switching node (V_x) voltages at 20 kW for (a) 25 kHz CCM and (b) 7 kHz QSW.

Fig. 8 presents the detailed waveforms of Q_3 and Q_4 for the 25 kHz CCM at 20 kW as initially displayed in Fig. 7 (a).

By reconfiguring the two Inductor A parts in parallel (as

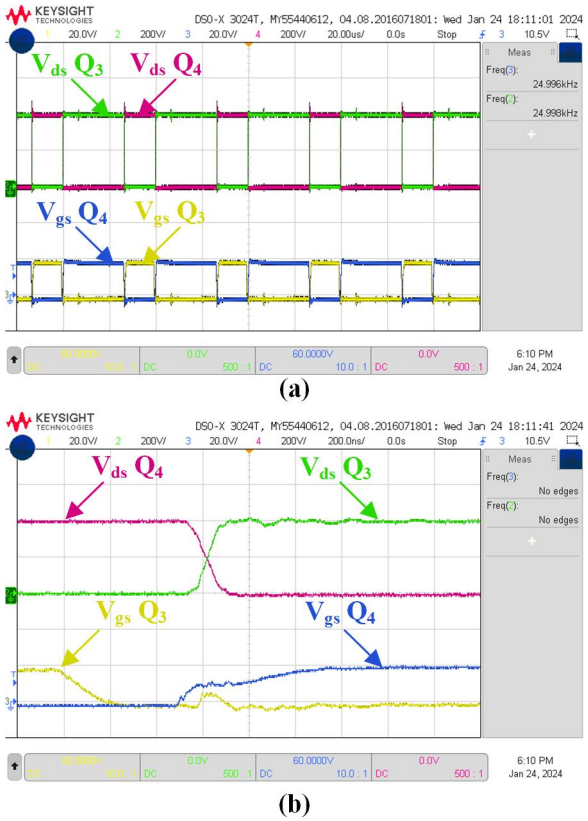

Fig. 8. (a) 25 kHz CCM experimental waveforms of Q_3 and Q_4 drain-source (V_{ds}) and gate-source (V_{gs}) voltages at 20 kW, and (b) zoom at Q_4 turn-on.

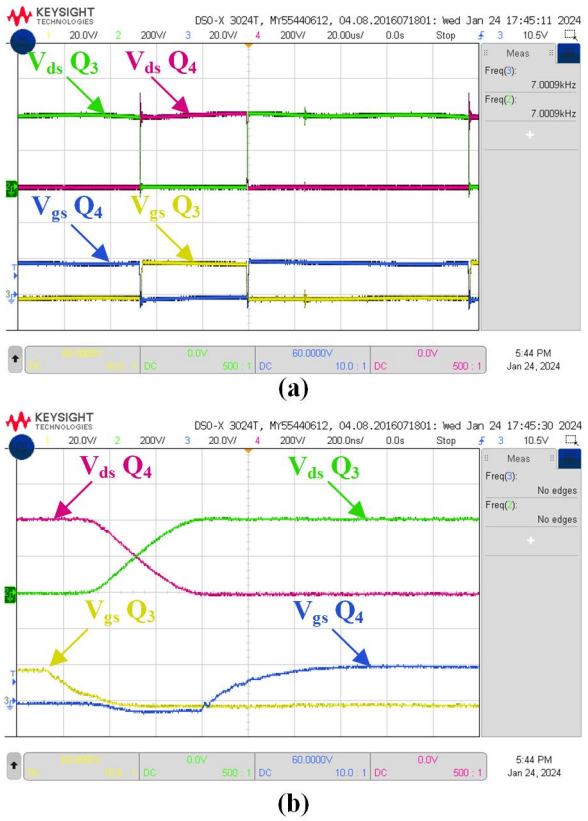

Fig. 9. (a) 7 kHz QSW experimental waveforms of Q_3 and Q_4 drain-source (V_{ds}) and gate-source (V_{gs}) voltages at 20 kW, and (b) zoom at Q_4 ZVS turn-on.

illustrated in Fig. 6), the results for QSW under the same load range are acquired. Up to 3 kW, however, the converter is locked onto the maximum switching frequency of 45 kHz. For loads above 3 kW the switching frequency is adjusted accordingly so that ZVS is reached with 0 A i_{ZVS}. At the maximum load of 20 kW the converter operates at 7 kHz as shown in Fig. 9.

Although the equivalent inductance is reduced to 71 μH, the value is still high for QSW at the intended power level, leading to the undesired low frequency operation. Optionally, two Inductor B parts (see Table II) are placed in series so QSW experimental results at 17.5 kW and 20 kW can be obtained at 45 kHz and 39 kHz, respectively.

A compilation of the efficiency over different loads and operation modes, as previously described, is presented in Fig. 10. As can be seen CCM presents the expected trend of efficiency reduction, despite the lower RMS current, due to switching losses. When comparing the low frequency QSW results, efficiency is kept above 45 kHz CCM through the whole load range, while in comparison to 25 kHz CCM few points are seen lower. These points are majorly explained by the gains of ZVS being diminished by the increase of the RMS current (as can be noticed from measurements in Figs. 7). Most importantly, the efficiency of QSW at full power is higher than CCM at the same point. Especially comparing the higher frequency cases, which are of interest for passive components reduction, 45 kHz CCM shows 97.4% efficiency versus 97.8% of the 7 kHz QSW and 98.3% of the 39 kHz QSW (although the latest efficiency is boosted by Inductor B's lower dc resistance).

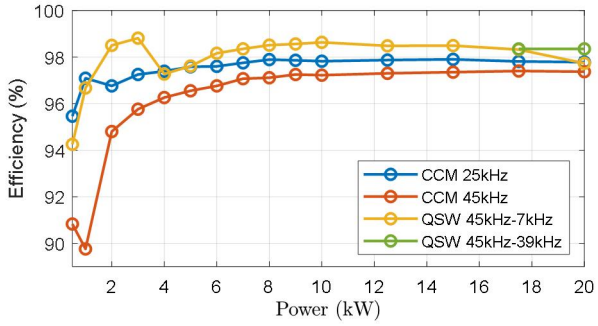

Fig. 10. Efficiency measurements for CCM and QSW operation.

For the cases where Inductor A was used the specific weight for both CCM and QSW was 13.05 kW/kg. However, in QSW, further development on the magnetics can yield lower weight as the switching frequency is increased without penalizing the

losses, thus allowing the specific weight of the converter to reach higher figures.

IV. Conclusion

This paper presented the concept, analysis and validation of the QSW technique applied to a three-level buck converter. QSW, in comparison to TCM, yields system's RMS current reduction and therefore higher efficiency. When it comes to CCM, the comparison is not as straightforward as to TCM, and further analysis is required to define the optimal operation point where QSW can improve the converter overall efficiency or reduce passive components without penalizing the cooling system size.

Acknowledgment

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