Modular DCX Blocks with Autonomous Synchronization for Power Distribution Subsystem of Satellites

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***Abstract*—This paper proposes the utilization of power electronics building blocks to standardize the power distribution subsystems in space applications. The main objective is to offer a viable strategy to expedite development with enhanced reliability, proposing an electronic-transformer-based (DCX) module. The DCX is an open-loop isolated converter that presents high efficiency and fast dynamics and enables series and parallel connections to accommodate various voltage and power requirements. The resonant full-bridge converter is studied as the DCX solution for the proposed system. Given its necessity of synchronized switching between modules, a concept of Modular Distributed Synchronization System (MDSS) is introduced. The MDDS is designed to ensure the synchronization of the switches of the modules and thus equal power sharing among connected modules, integrating redundancy and self-sustained operation, providing the flexibility needed for the DC-DC conversion. The present paper outlines the conceptual framework of the proposed system and presents a prototype for a modular Full Bridge (FB) DCX, integrated with a MDDS. The results are centered on the validating of the DCX module feasibility and in the MDSS performance in normal operation and its recovery from operational failures.**

Keywords— DCX, space power applications, building-blocks, resonant converters.

I. INTRODUCTION

The continuous launch of new space missions, with a wide variety of electronic loads, leads to a permanent development of power converters to ensure efficiency in the bus voltage adaptation (secondary power subsystem). This approach requires the investment of time and financial resources in its development. For these reasons, the standardization through modular circuits, based on Power Electronics Building Blocks (PEBBs) [1], offers a viable alternative to accelerate new developments aligned with the "New Space" paradigm [2] [3]. Besides, the utilization of modular circuits has the potential to increase system reliability and to reduce the total cost as it becomes more extensively implemented.

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A simplified diagram of a space applications distribution system is depicted in Fig. 1, where the main DC-DC conversions are shown [3]. The Power Control and Distribution Unit (PCDU) manages the main bus, charging and discharging the batteries via a Battery Charge and Battery Discharge Regulators (BCR and BDR respectively). The PCDU also controls the input power delivered by the Solar Array via a Solar Array Regulator (SAR).

The voltage level of the primary bus in a regulated power supply architecture is determined by the power demands [4]. Consequently, for a power requirement below 1.5 kW, the bus operates at 28 V. When power demands are between 1.5 kW and 8 kW, the bus voltage is set to 50 V. For power demands exceeding 8 kW, the bus voltage is either 100 V or 120 V.

Through DC-DC conversion, a variety of secondary buses are derived from the primary bus, where the point-of-load (PoL) converters and loads are connected. While the primary bus has standard values, the voltage value in the secondary buses is not uniform. There is a wide range of voltage and power levels (as Fig. 1 suggests) demanded from these secondary buses, being dependent on the load, mission requirements, etc. This implies poor circuits standardization, which often leads to the power converters being redesigned.

In order to standardize the design of the DC-DC conversion between the primary and secondary buses, maintaining the flexibility and reliability of the system, this work proposes the usage of a modular solution based in the concept of electronic transformer (DCX) [5][6][7]. In complement to the power converter, this work proposes a modular synchronization circuit, that works independently from the power circuit and also avoids the need for a central control. This helps to fulfill redundancy and safety requirements.

The main concept to be adopted will be discussed in section II, with a brief explanation of the DCX concept in subsection A. A review of the full-bridge converter design as a DCX (FB-DCX) will be presented in section II, subsection B. Section III will address a Modular Distributed Synchronization System (MDSS), responsible for generating the reference to synchronize the modules switching, and so its resonances, which is essential for the even voltage and power

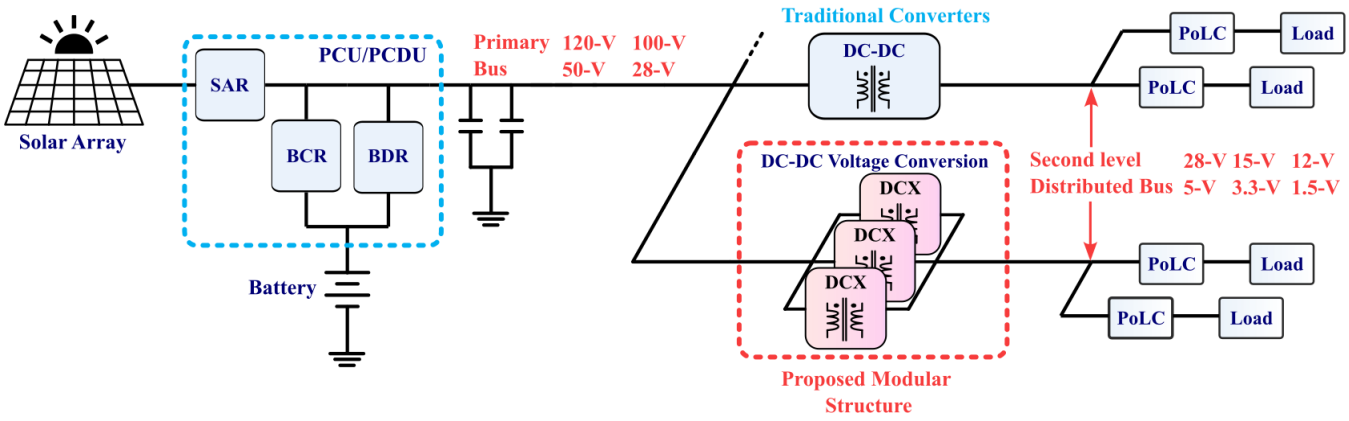

Fig. 1. Representation of a power supply system for a spacecraft.

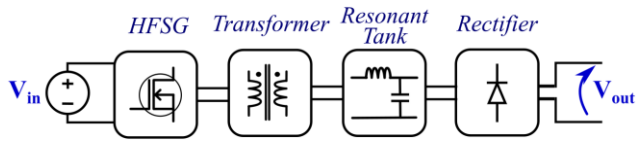

Fig.2 Resonant DCX basic representation.

distribution in a modular FB-DCX system. The prototypes and the experimental results will be discussed in section IV, covering the power stage and the MDDS performance. Finally, the conclusions will be elaborated in section V.

II. The Proposed DCX Concept

A. *The modular DCX and the voltage adequacy*

The DCX is an open-loop isolated converter with fast dynamics (between input and output) and high efficiency. As a mean of improving its performance, it's common the adoption of resonant topologies that provide soft switching.

DCX converters have been used as a PEBB in power conversion architectures for several applications, mostly in second stages. Some examples are the utilization of DCX in data centers [8][9] or microgrids with wide range of applications, from medium to low voltage conversions [10][11].

The basic structure of a resonant DCX is depicted in Fig.2. The input voltage is converted by an inverter into a squared wave which is applied to the primary side of a transformer. The transformer is connected to a resonant tank, which can be arranged on the primary or secondary sides and is designed to resonate at a given frequency (f_r). The resonant current passes through a rectifier and charges an output capacitor, which could be part of the resonant tank.

To meet the different voltage and power requirements, the DC-DC conversion will be achieved through series and parallel connections of several modules. Series connection (at input or output) would enlarge the voltage capability, while parallel connection is crucial for meeting redundancy standards and to adequate the total power [12].

Considering a modular DCX design with a voltage gain of 2:1, Fig. 3.a depicts a single DCX block performing a voltage conversion of 0.5. Figure3.b shows an Input Series Output Parallel (ISOP) arrangement with the same DCX block, resulting in an overall voltage conversion of 0.125.

Figure 3.c depicts a different situation: a 4:1 voltage gain (i.e. two DCX blocks in ISOP configuration), where the

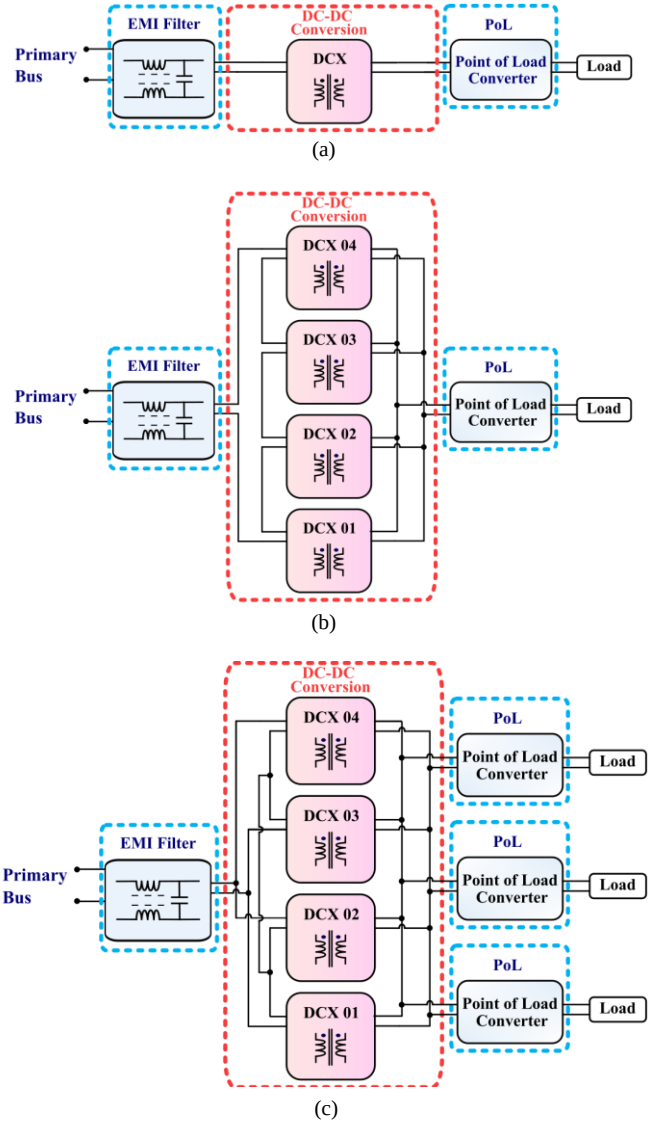

Fig.3 DCX module connection to acquire different voltage conversions: (a) 2:1 as single module, (b) 8:1 with ISOP connection, and (c) 4:1 with matrix connection.

amount of power required by the loads is larger than the power capacity of two ISOP modules. Therefore, the power requirement can be met by adding another structure of two DCX modules (in ISOP) in parallel to the first one. This could be theoretically expanded to meet any power requirement without affecting the overall voltage gain.

B. *Full-bridge converter as a DCX*

Different converters could be designed based on the main resonant DCX representation depicted in Fig. 2. The common circuit structures designed for each block are a half-bridge (HB) or a full-bridge (FB) to compose the inverter, a transformer featuring one or two secondary windings, and a resonant tank placed in series (e.g., LLC converter) or in parallel with the load. Additionally, the rectification can be diode-based or synchronous. Each structure chosen has a different impact not only on the DCX performance, but also on the circuits and conditions required to be suitable for operating in a power supply system for space applications.

According to the "Space Product Assurance. Failure modes, effects (and criticality) analysis" found in [14], it is assumed that only one element can fail at any given time. While a failure may impact the operation of the module in which it occurs, it should be designed not to propagate to other modules or affect the system integrity. As a practical example, assuming a failure in just one switch, a FB could promptly isolate the affected module by ceasing the conduction of the remaining switches, diminishing the necessity for supplementary protective switches if compared to a HB [13].

The resonant FB depicted in Fig. 4 is the chosen topology for this DCX implementation. The resonant elements of the FB-DCX are the leakage inductances (L_{k1} y L_{k2}) and the output (resonant) capacitor (C_r). In Fig.4, the FB-DCX resonant elements are highlighted in red, and its main waveforms are depicted in Fig. 5.

This converter presents a natural power sharing, not only in ISOP, but in Input Parallel Output Parallel (IPOP) connections, requiring only the synchronization of the switching signals [13]. This complements the chosen converter strength of permitting parallel module interconnections if compared to an LLC resonant converter.

C. *FB-DCX design*

The equivalent circuit for a single resonant branch is displayed in Fig 6 and is valid just during the diode conduction. In a practical analysis, the intrinsic impedances such as copper tracks inductance, could be significative and should be considered into the equivalent circuit values.

The input source in Fig 6 represents the value of the voltage applied in the primary windings times the voltage ratio of the transformer. In the beginning of each half period, the value of the secondary winding voltage is higher than the value of the resonant capacitors voltage (V_{Cr}). This voltage difference could be seen between V_1 and V_{Cr} in Fig. 5 (red and black waveforms, respectively), and this starts a resonance process with zero current in I_1.

Both resonant currents are reflected in the primary winding current (I_p) and are added to the magnetizing current (I_{Lm}). As depicted by I_1 and I_2 in Fig 5, when the current goes back to zero value, the diode blocks the conduction of negative charges. While there is no resonant current in the circuit, the energy stored in the magnetizing inductance will promote Zero Voltage Switching (ZVS) in the primary switches, discharging the primary MOSFETs intrinsic capacitance. As there is no resonant current in the secondary, there is no positive current in Cr, so it is linearly discharged by the output current (I_O).

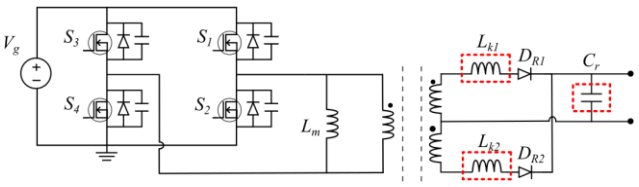

Fig.4 Electrical diagram of the full-bridge DCX.

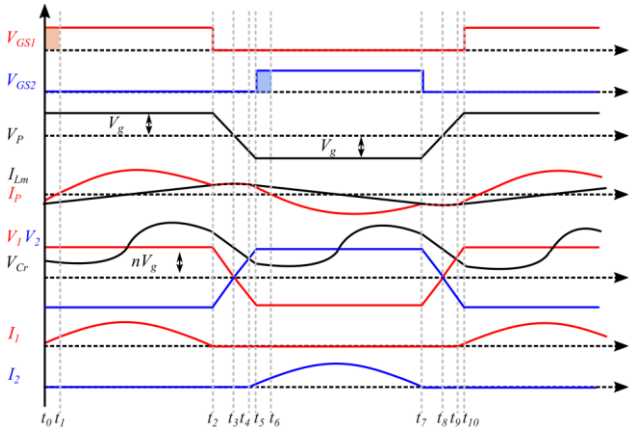

Fig.5 Main converter waveforms of the FB DCX.

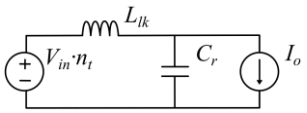

Fig.6 Equivalent circuit of the resonant FB-DCX.

When connected in parallel, the FB-DCX circuits have their resonant capacitors connected in parallel. Assuming that the variation between the circuit elements is controlled, i.e. relatively low, and ensuring synchrony between the bridge switching on the primary side, an equitable distribution of power is guaranteed without major problems. This way, the general design of the power modules can be carried out without additional considerations.

The resonance time (t_{res}) is designed to be smaller than the change of operational state in the primary, allowing smaller currents in the switching in the primary side and zero current switching (ZCS) in the rectifiers. The equations (2) and (3) define the resonant current and the resonant voltage respectively.

$$I_{lk}(t) = \left(\frac{n_s}{n_p}V_{in} - V_{Cr}(0)\right)\sqrt{\frac{C_r}{L_{lk}}} \cdot \sin(\omega_0 t) + I_o \cdot (1 - \cos(\omega_0 t)), \quad (1)$$

$$V_{Cr}(t) = V_{Cr}(0)(\cos(\omega_0 t)) + \frac{n_s}{n_p}V_{in}(1 - \cos(\omega_0 t)) - I_o\sqrt{\frac{L_{lk}}{C_r}} \cdot \sin(\omega_0 t), \quad (2)$$

where np and ns are the primary and secondary turn numbers respectively, ω_0 is the resonant angular frequency defined by (4), and $V_{Cr}(0)$ is the starting C_r voltage, defined by (5).

$$\omega_0 = \left(\sqrt{C_r \cdot L_{lk}}\right)^{-1} = 2\pi \cdot f_r, \quad (3)$$

$$V_{Cr}(0) = V_{Cr}(t_{res}) - \frac{I_o}{C_r}\left(\frac{T_{sw}}{2} - t_{res}\right). \quad (4)$$

The considered output voltage (V_{out}) is the average value of the resonant capacitor's voltage (V_{Cr}), and based in Fig 6, it's easy to see that V_{Cr} average value is the same as the reflected voltage in the secondary winding. Therefore, V_{out} is defined in (1) in function of V_{in} and the transformers turn ratio.

$$V_{out} = \overline{V_{Cr}} = \frac{1}{T_{sw}} \int_0^{T_{sw}} V_{Cr}(t)\, dt = V_{in} \cdot \frac{n_s}{n_p}. \qquad (5)$$

where T_{sw} is the switching period.

The design of a FB-DCX is already discussed in the literature, and more details can be found in [5] [9].

III. Modular Distributed Synchronization System

As mentioned previously, the desired FB-DCX operation only requires modules with synchronous switching to equally share the processed power. This feature requires that all modules interconnected are in synchrony to a leader signal, labelled in this work as Global Clock Signal (GCS).

In order to generate the GCS, it must be considered that the local ground (GND of each DCX) will be at different voltage levels when connected in series (see figure 3); therefore, isolation between the GCS and MOSFET drivers is necessary.

This work also proposes the entire system being independent of a central control, adding the capacity to generate the reference signal from any DCX module. This will increase the robustness of the entire system linearly to the number of connected modules. Notably, the use of FPGAs or Microcontrollers suitable for space applications can be of little interest to generate the control signals, as it may significantly increase the overall price of the electronic design.

To address these three aspects, voltage isolation, modular autonomy and avoiding the use of microcontrollers (or FPGAs), the present work proposes a Modular Distributed Synchronization System (MDSS).

The simplified diagram of Fig. 7 shows the proposed system operation with "n" DCX modules, where each DCX carries its own MDSS module. The "DCX 01" is represented with more details, with the main local signals (in red) in addition to the global signals (in blue). Labels "leader" and "follower" are added to facilitate system understanding. Nevertheless, there is no order of priority for choosing the "leader" module, which occurs naturally within the system.

All MDSS modules are designed to have the same voltage reference as the GCS, while the power circuit communicates with the global signal via an isolator. The output of the isolators reproduces the GCS, and connects to a phase locked loop, that provides a reference signal for the FB MOSFET drivers.

A. *MDDS Circuit*

The main circuit of an MDSS unit can be subdivided into three circuits (see the MDSS Module 01 in Fig. 7) representing its main internal functions: Signal Generation, Signal Amplifier and Enabling Circuit.

The output of the Signal Generation is the Local Clock Signal (LCS), which is continuously generated in each MDSS module. The LCS is received by the Amplifier Circuit and sent to the GCS bus when receiving a positive signal from the Enabler. The Enabling Circuit is continuously comparing

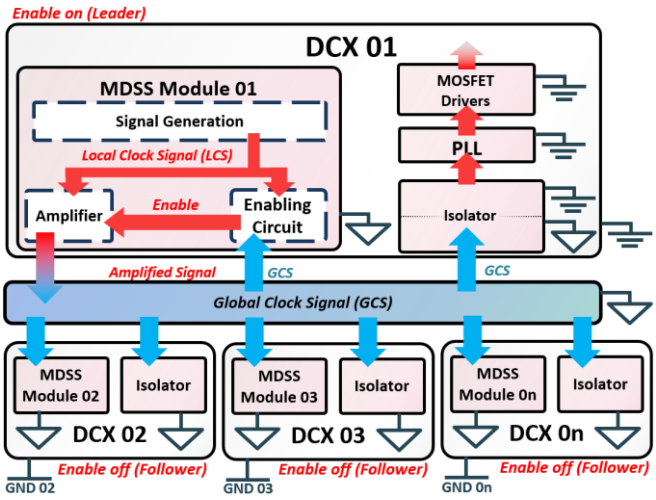

Fig.7 Diagram of the DCX modules with integrated MDDS, with module 01 presented in more detail.

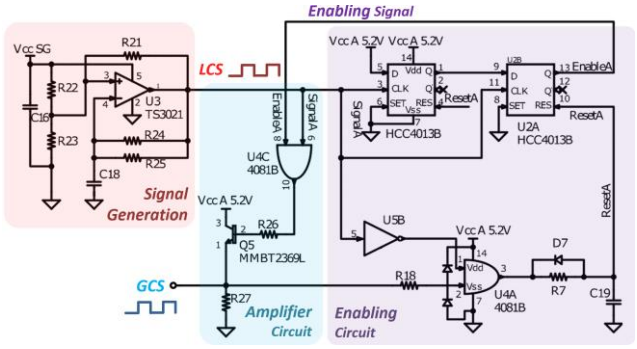

Fig.8 MDSS main circuit.

GCS with LCS and is the key circuit for structuring the system and providing an arbitrage operation between the modules.

The circuit inside of the MDSS module is depicted in Fig. 8 and is designed with discrete components that already have space qualified equivalents, such as comparators, transistors, logic gates, capacitors and resistors. As these components are standard for this kind of application, this design offers independence from specific suppliers.

The LCS is generated via an astable oscillator, made with a comparator (U3) and the charge and discharge of a capacitor (C18). The amplifier circuit is made through an NPN transistor (Q5) controlled by the output of a logic gate (U4C), that execute the AND operation between the LCS and the "Enabling signal"

The "Enabling Circuit" is an edge accumulator made by two Toggle Flip Flop structures (U2) in series, that generates a positive enable signal after just two edges of the LCS.

The output of the "AND" gate in the enabling circuit (U4A) is a reset signal for the edge accumulator, that is positive when there is a GCS that is different from the LCS. Finally, this reset signal passes through a low pass filter (R7 and C19) to avoid any delays present in the circuit.

B. *MDSS operation*

For the description of the MDSS operation, it will be taken the MDSS Module 01 from Fig. 7 as the main example.

In the startup, when there is no global clock signal, the Enabling Circuit will count two edges from the LCS and, in the absence of a GCS (and so a reset signal), the enable signal changes from '0' to '1'. In this moment, this module assumes the leader role in the system, and injects its LCS to the GCS.

Considering that all the LCS generated inside the modules are very similar, with minimal differences in frequency and duty cycle, the beforementioned startup process could occur with more than one module at the same time. Considering that all the MDSS modules are trying to assume the role of leaders, there will be more than one LCS injected into the GCS. As there is a constant comparison between the GCS and LCS performed by the enabling circuits, one by one the modules will identify that there is a difference between its own LCS and the GCS. Therefore, one by one of the amplifiers will be disable until just one leader will remain. This disabling process will generate an arbitrage operation independent from a central control and the number of modules, covering one of the premises initially proposed.

IV. The Prototype And Experimental Results

To validate the system concept, the FB-DCX module was implemented, with the MDSS module integrated in the same board. The PCB design was made to facilitate a "plug-and-play" connection in ISOP configuration, via connectors positioned on the lateral edges. In Fig. 7 four modules are presented in ISOP connection (in the same configuration as Fig.3.b).

Each module is designed for an input voltage of 25 V, voltage gain of 0.5 and a power of 100 W. Therefore, the ISOP arrangement of Fig. 5 could convert from 100 V to 12.5 V. Further details on each module are presented in Table I

TABLE I. Prototype Parameters

Parameter	**Symbol**	**Value** [a]
Prototype total power capacity	P_o	100 W
Switching frequency	f_s	500 kHz
Resonance frequency	f_r	1 MHz
DCX Input voltage	V_{in}	25 V
Primary MOSFETs	S_1, S_2, S_3, S_4	IPD053N08N3G
Secondary side rectifiers	D_{r1}, D_{r2}	NRVBB60H100CT
Duty cycle	D	50% (43%)
Dead time	t_d/T_s	7.6% (7%)
Transformer magnetizing inductance	L_m	9,8 µH
Transformer primary side turn number	N_p	4
Transformer secondary side turn number	N_s	2
Considered transformer leakage inductance	L_{kA}	25 nH
Resonant (output) capacitor	C_r	1 µF

Figure 10 presents the main waveforms of a FB-DCX module, focusing on the resonant current and voltage signals (pink and yellow waveforms respectively), with the output current (green waveform) and the presence of the GCS in the top (blue waveform). The current measurements are taken at the primary winding to minimize the impact of the current probe (and the current measurement loop) in the resonant circuit as the inductances involved are on the order of 25 nH.

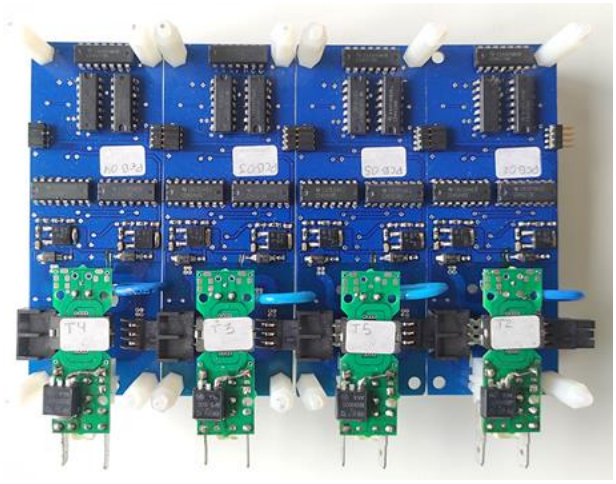

Fig. 9 FB DCX prototype in ISOP arrangement.

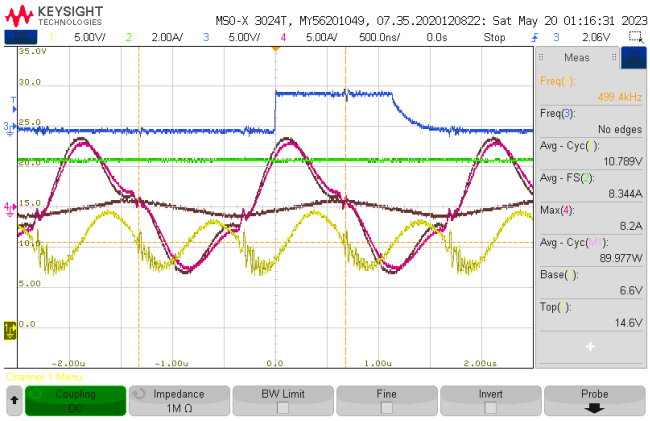

Fig. 10 Results for a single DCX module. Yellow: DCX output voltage; Green: Input Voltage; Blue: reference signal; Pink: current in the primary winding.

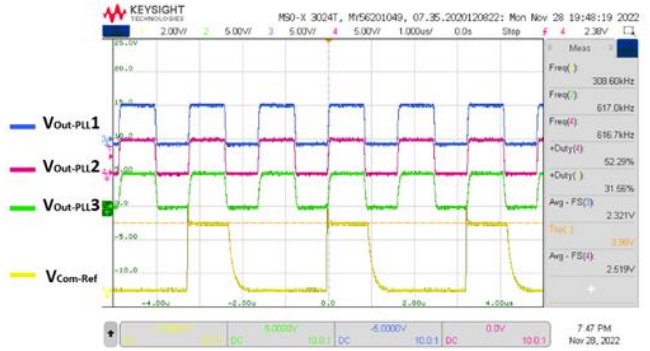

Fig. 11 Results for the MDDS in normal operation, with the GCS and the output signal of three different modules PLL circuit. Yellow trace: GCS; Green trace: output of PLL 01; Pink trace: output of PLL 02, Blue trace: output of PLL 03.

Following the validation test focused on the power circuit of a DCX module, the synchronization system was analyzed through two additional tests. These tests were conducted at the maximum frequency for which the SMSD was designed. Fig. 11 shows again the GCS, now with a yellow trace, and the output signal of three PLL circuits of different DCX modules.

It can be seen that there is a fine synchronization between all the output signals of the PLL circuits and the GCS.

With the purpose of understanding which module is the leader during normal operation, four synchronization modules were placed to share a GCS. Fig. 12 shows the measurement before the resistor in the base of the transistors that form the open-emitter output of each MDSS module (in the output of the “AND” gate, see Fig. 8). The leader role seamlessly alternates between different modules in normal operation, and temporarily permits (for a few clock cycles) multiple modules to operate as leaders. This alternation is a result of local clock signals eventually synchronizing with the GCS, so the enabling circuit is not able to detect the difference between the local and global signal. This forces the state of "Enabling signal" to change to '1' during the moment of synchronization. After a few clock cycles, a slight difference between the LCS frequencies implies a phase difference; the first module that detects this difference changes the value of its "Enabling signal" from '1' to '0', leaving the leader role.

Fig. 13 shows a leader role change situation in more detail, with just two modules placed to share a GCS. The green trace is the GCS and both blue signals are the outputs of two different modules. After some clock cycles both modules assume the role of leader. At the end of three synchronized cycles, it is generated a delay between the signals that is enough for one of the modules to detect it and reset its edge accumulator, changing its "Enabling signal" from '1' to '0'.

This phenomenon is not a problem, as they generate almost identical signals on the bus and they use outputs in open-emitter, the quality of the SSG signal is not compromised. Furthermore, it is a demonstration of the agility of the system in detecting and replacing the reference signals, what emphasizes the inherent redundancy in all DCX modules.

To simulate a fault in the synchronization system, a case with an induced disconnection of the leader MDSS module is presented by Fig.14. The voltage probe configuration is similar to the previous test (Fig. 13) with the addition of a third MDSS module, represented by the signal in pink. This third module has been modified to act as the leader until it is disconnected from the reference by a bipolar transistor (controlled by an external trigger). It can be seen that the GCS follows the pink reference until it is disconnected. After this disconnection, the GCS presents a longer off time that is shorter than two cycles. This delay represents the time required for one of the remaining MDSS modules to detect the lack of reference and assume the role of leader.

V. Conclusions And Future Works

A modular converter based on an electronic transformer with a full-bridge structure has been presented. This modular converter is designed to perform DC-DC power conversion on secondary buses of power supply systems in space applications. The proposed solution is based on the modular concept by channeling the connection possibilities between inputs and outputs of the designed modules.

This work also proposed a Modular Distributed Synchronization System, which provides autonomy to the modules and redundancy in the reference signal generation.

The developed prototypes demonstrate the validity of the proposed DCX circuits. Furthermore, synchronization tests show that the distributed system works effectively, allowing agile and seamless changes of roles between leader and follower modules. This is crucial to guarantee an equitable distribution of power and ensure system redundancy.

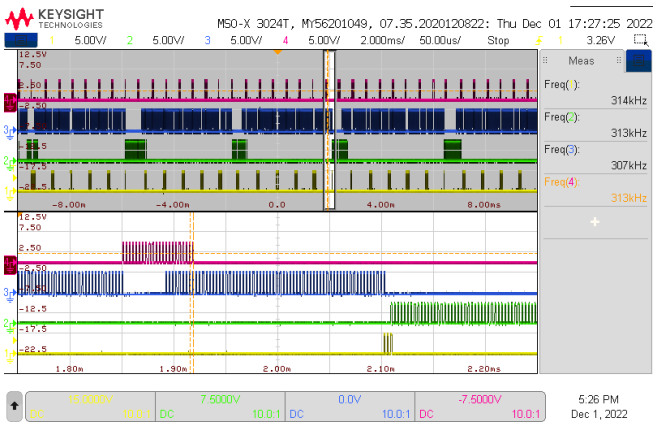

Fig. 12 Fig. 12 Normal (non-faulty) operation of four modules. The four traces represent the output of the AND gate in charge of governing the open collector output. 20 ms duration (upper part) with a detail of 500 µs (lower part).

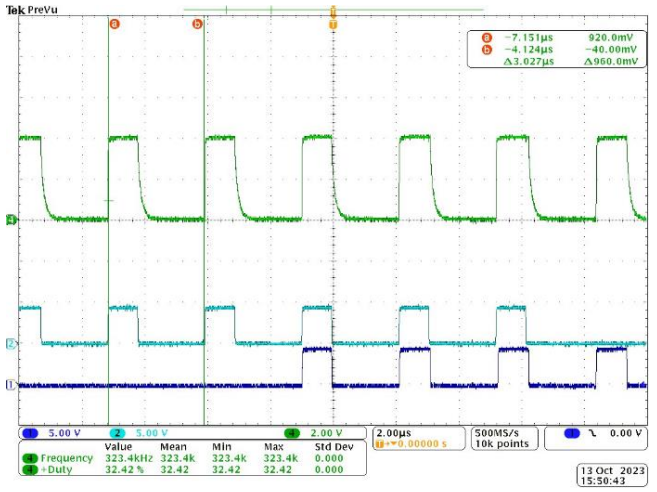

Fig. 13 Behavior of the DSSS under normal conditions, with the occurrence of natural change of master signals. Green - GCS; Dark blue - signal at the base of the amplifying transistor of PCB 01; Light blue - signal at the base of the amplifying transistor of PCB 02.

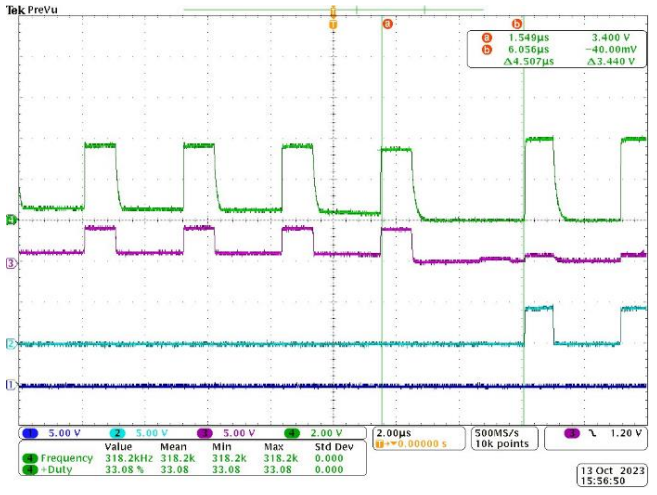

Fig. 14 Intentional disconnection of the master signal. Green - GCS; Dark blue - Signal at the base of the amplifier transistor of PCB 01; Light blue - Signal at the base of the amplifier transistor of PCB 02; Pink/magenta - Signal at the base of the amplifier transistor of PCB 03.

REFERENCES

[1] Y. Chen, P. Wang, Y. Elasser and M. Chen, "LEGO-MIMO Architecture: A Universal Multi-Input Multi-Output (MIMO) Power Converter with Linear Extendable Group Operated (LEGO) Power Bricks," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 5156-5163, doi: 10.1109/ECCE.2019.8912965.

[2] A. Golkar and A. Salado, "Definition of New Space-Expert Survey Results and Key Technology Trends," IEEE Journal on Miniaturization for Air and Space Systems, vol. 2, no. 1, pp. 2–9, 2021, doi: 10.1109/JMASS.2020.3045851.

[3] ESA, "Development of an End to End Line of Standard DC/DC Converters." [Online]. Available: https://rosa.ro/development-of-an-end-to-end-line-of-standard-dc-dc-converters/

[4] M. Patel, Spacecraft Power Systems, Boca Raton (FL) 2005.

[5] W. Qin, G. Lan, and X. Wu, "A family of ZVSZCS resonant DCX with DC resonant capacitor," 2015 IEEE 2nd International Future Energy Electronics Conference, IFEEC 2015, no. c, pp. 6–11, 2015, doi: 10.1109/IFEEC.2015.7361431.

[6] Y. Ren, M. Xu, C. S. Leu, and F. C. Lee, "A Family of High Power Density Unregulated Bus Converters," PESC Record - IEEE Annual Power Electronics Specialists Conference, vol. 1, no. 5, pp. 527–532, 2004, doi: 10.1109/pesc.2004.1355802.

[7] F. Flores-Bahamonde, H. Renaudineau, A. M. Llor, A. Chub, and S. Kouro, "The DC Transformer Power Electronic Building Block: Powering Next-Generation Converter Design," IEEE Industrial Electronics Magazine, vol. 17, pp. 21–35, 2022, doi: 10.1109/MIE.2022.3147168.

[8] Y. Cai, M. H. Ahmed, Q. Li and F. C. Lee, "Optimal Design of Megahertz LLC Converter for 48-V Bus Converter Application," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 495-505, March 2020, doi: 10.1109/JESTPE.2019.2939469

[9] M. H. Ahmed, M. A. de Rooij and J. Wang, "High-Power Density, 900-W LLC Converters for Servers Using GaN FETs: Toward Greater Efficiency and Power Density in 48 V to 6\/12 V Converters," in IEEE Power Electronics Magazine, vol. 6, no. 1, pp. 40-47, March 2019, doi: 10.1109/MPEL.2018.2886106.

[10] J. Huang and X. Zhang, "Three-Step Switching Frequency Selection Criteria for Symmetrical CLLC-Type DC Transformer in Hybrid AC/DC Microgrid," in IEEE Transactions on Power Electronics, vol. 34, no. 10, pp. 9379-9385, Oct. 2019, doi: 10.1109/TPEL.2019.2904045

[11] Q. Zhu, L. Wang, L. Zhang and A. Q. Huang, "A 10 kV DC transformer (DCX) based on current fed SRC and 15 kV SiC MOSFETs," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 2018, pp. 149-155, doi: 10.1109/APEC.2018.8341001.

[12] P. Czyz, T. Guillod, F. Krismer, J. Huber, and J. W. Kolar, "Design and Experimental Analysis of 166 kW Medium-Voltage Medium-Frequency Air-Core Transformer for 1:1-DCX Applications," IEEE J Emerg Sel Top Power Electron, vol. 10, no. 4, pp. 3541–3560, Aug. 2022, doi: 10.1109/JESTPE.2021.3060506.

[13] A. López, T. H. Oliveira, M. Arias, P. F. Miaja, J. A. Villarejo and A. Fernández, "Modular Fault Tolerant DC/DC Transformer Enabled by Natural Power Sharing," in IEEE Open Journal of Power Electronics, vol. 5, pp. 902-919, 2024, doi: 10.1109/OJPEL.2024.3414141.

[14] E.-E. ECSS Secretariat, "Failure modes, effects (and criticality) analysis (FMEA/FMECA)," Requirements & Standard division, no. March. 2009.