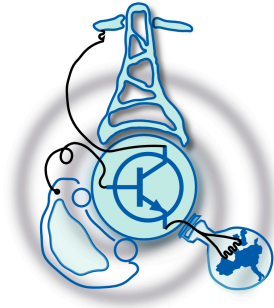# Design of High-Voltage High-Current Power Stack
by
Touseef Ali

Submitted to the Department of Electrical Engineering, Electronics,
Computers and Systems
in partial fulfillment of the requirements for the degree of
Erasmus Mundus Joint Masters Degree in Sustainable Transportation
and Electrical Power Systems
at the
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Abstract

This research-based thesis presents the 1.2 kV/ 1.4 kA IGBT power module-based power stack with a DC-link voltage of 1.5 kV, featuring the medium voltage power conversion with a simple three-level neutral-point clamped (3L-NPC) converter. The project is intended to design the 750 kVA/ 1.5 MVA high-voltage high-current power stack. The design of the power stack assembly comprises medium-voltage/high-current IGBT power modules, gate driver units with dual-channel IGBT driver cores that are fully equipped with isolated DC/DC converters along with short-circuit protection, DC-link capacitors, and air-cooled heat sink. The 750 kVA single-phase and three-phase 3L-NPC converter is simulated in MATLAB/Simscape software to analyze the power losses and efficiency and the same approach is adopted for the design of 1.5 MVA power stack design. The initial 750 kVA single-leg power stack prototype is designed using a 3L-NPC converter and is tested with an RL load at low power at the laboratory due to the availability of the load and safety precautions. The hardware setup is tested under two experiments with a total average circulated power of 1.045 kW with a modulation index of 0.8 and a power factor of 0.96 in one experiment with an efficiency of 96.7%. In another experiment, the average power of 2.09 kW is injected with a modulation index of 0.9, and a power factor of 0.97 and 97.84% efficiency is obtained and the results are validated with the simulation results.

Thesis Supervisor: Juan M. Guerrero Muñoz
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Chapter 1

Introduction

1.1   General overview

Power stack is a groundbreaking technology in the field of power electronics in the electrical energy sector. Modern power electronics is evolving to efficient and reliable power conversion which requires the development of advanced power stacks capable of managing and controlling high voltage and high currents in large-scale electrical power systems. The power stack is a cutting-edge technology that has revolutionized the back-to-back (B2B) marketplace. It will be a game changer for businesses with its innovative design and advanced features that offer a comprehensive solution to their power needs. The power stack is a compact and versatile assembly of semiconductor devices, i.e., SiC MOSFETs, IGBTs, etc., along with gate drivers, DC-link capacitors with bus bars, and cooling systems and are designed to convert, control, and condition electrical power efficiently within various applications [1]. Power stack technology implementation provides reliable power supply, scalability, environmental sustainability, energy independence, high power density, compact and lightweight, flexible configuration and integration, and cost savings. The power stack assembly can be made by connecting SiC MOSFET or IGBT power modules in series or parallel depending upon the application and output power requirement [2]. Currently, power stacks are used in marine and off-shore applications, wind turbines, solar inverters, oil, gas, and mining, compressors, high voltage air conditioning systems, and grid,

industrial, and motor drive applications. Fig. 1-1 shows the medium voltage and high-power IGBT and SiC-based power stack, designed by the SEMIKRON Danfoss company [3].
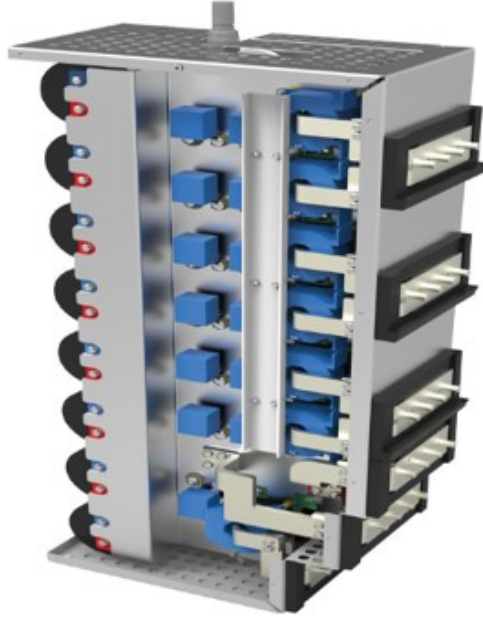
Figure 1-1: IGBT and SiC-based power stack from SEMIKRON Danfoss [3]

To overcome, the medium voltage and high-power demand in the electrical energy and industrial sector, different power electronic topologies have been used for designing the power stacks based on the application. For the medium voltage power stacks design series connected 2-level and multilevel converter topologies have been used. Earlier, the two-level voltage source converters were used to design the power stacks but high dv/dt due to synchronous commutation of series devices, static and dynamic voltage sharing of series devices, high switching frequency harmonic content in the inverter output voltage are the main issues concerned with this topology. To prevail over, these issues with the two-level converters, the multilevel converters are used for the designing of the medium voltage (MV) power stacks as an alternate solution to reduce the harmonic content in the output voltage and current waveforms of the converter at a given switching frequency [4]. The classification of the multilevel converter based on the voltage sources required is shown in Fig. 1-2. Among the different multilevel converter topologies, three-level neutral point clamped (3L-NPC)

is widely used because it provides reduced harmonic content, better usage of switches, reduced dv/dt compared to two-level and is considered as the basic building block for multilevel converters in medium voltage and high power stack design. Several power stack types are available in the market including single power stacks having one power module, series or parallel power stacks, and hybrid power stacks (series and parallel combination of power modules) [5]. In this research-based thesis project, to design the high-voltage high-current power stack, a 3L-NPC converter is used because of its promising performance in medium voltage and high power stack design.
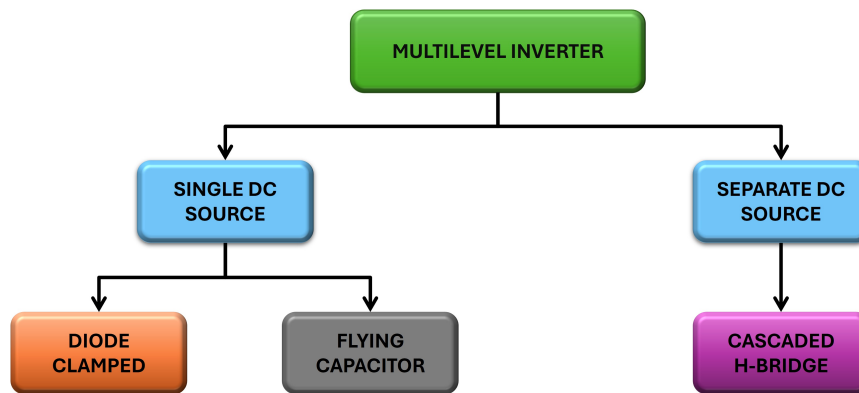
Figure 1-2: Classification of MLI topologies

1.2 Motivation of the project

The increasing demand for high-efficiency, reliable power conversion systems in renewable energy, industrial, and drive applications has highlighted the limitations of conventional converter topologies. The innovations in the power stack technology and their design by using a single source and common DC-link multilevel converters offer promising solutions by utilizing the full DC-link voltage and semiconductor devices effectively. So, the researchers and companies have raised their heads toward the three-level converter topologies and the 3L-NPC converter shows significant and satisfactory results for the design of medium voltage and high power density power stacks. Elinsa Grupo Amper company is one of them and is interested in this emerging technology. This research-based master thesis internship is funded by Elinsa Grupo

Amper company to design and develop a high-voltage high-current power stack for industrial applications.

1.3 Scope of the work

This research-based thesis project focuses on designing a 1.5 MVA power stack using a single-phase 3L-NPC converter topology for industrial applications. So, the initial prototype of 750 kVA is designed for testing purposes using the available power electronic components. Moreover, the prototype is designed and tested on low power in the laboratory considering the availability of the load and safety precautions, and the 3L-NPC converter provided a highly efficient power stack at that testing level. It is intended to be further tested at the company at the rated power of the power stack.

1.4 Research objectives

This research-based thesis project is broken down into the following sub-objectives;

- The state of the art in the three-level converter topologies to select a topology that is efficient for designing high-voltage high-current power stacks.

- DC-link capacitor sizing for the 750 kVA and 1.5 MVA power stack prototype design.

- Power electronic components selection for the particular power range design, based on the voltage and current ratings.

- Design of the heat sink to satisfy the thermal requirements of the power stack for the initial design of 750 kVA.

- The prototype design of the 750 kVA for the initial testing of the power stack.

1.5 Research methodology

The following research steps are adopted to complete this project.

- State-of-the-art three-level converter topologies and PWM techniques for the 3L-NPC converter topology.

- The availability of power stacks and the availability of maximum rating IGBT modules in the market and the converter topologies that companies are using for power stack design.

- A single-phase 3L-NPC and 3L-NPP converter is simulated using MATLAB/Simscape and comparative analysis is performed based on power losses, efficiency, and cost-effectiveness.

- The three-phase three-level NPC converter simulation is done using the MAT-LAB/Simscape platform.

- DC-link capacitor sizing and analysis are done based on different load conditions.

- The selection of hardware components for a prototype designed for initial testing of a 750 kVA power stack using the 3L-NPC converter topology.

1.6   Thesis structure

The thesis structure of the design of a high-voltage high-current power stack is as follows;

- Chapter 1, portrays the general overview of the power stack technology, its background study, motivation, scope, objectives, and methodology to design the project.

- Chapter 2, states the state-of-art in three-level converter topologies and literature review on PWM techniques based on the dc-link capacitor balancing, and mitigation of low-frequency oscillation at the neutral point (NP) is studied.

- Chapter 3, reveals the comparative analysis of the single-phase 3L-NPC and 3L-NPP converter based on power losses, efficiency, and cost-effectiveness.

- Chapter 4, registers the simulation of a three-phase three-level NPC converter using MATLAB/Simscape, and its power loss and efficiency analysis section is also included in this part of the thesis.

- Chapter 5, is about the hardware design and selection of the power electronic components.

- Chapter 6, starts with testing of the IGBT power module, prototype design of the 750 kVA power stack. This prototype is tested under low-power conditions because of the availability of the load and safety precautions.

- Chapter 7, concludes the research-based thesis project and suggests possible future recommendations.

Chapter 2

State-of-art in three-level converters

This chapter discusses the state-of-art in three-level common DC-link converter topologies to select the efficient three-level converter topology to design the high-voltage high-current power stack in the beginning part of the chapter. The middle part explains the PWM techniques for the 3L-NPC converter and the last part ends the chapter with a summary of the literature review.

2.1 Common DC-link topologies

In this section, the common DC-link three-level converter topologies are discussed.

2.1.1 Three-level neutral-point clamped (3L-NPC) converter

This type of converter commonly known as a diode-clamped converter is one of the widely adopted topologies of the multilevel converter for various industrial, automotive, and drive applications due to its simple implementation, effective operation, and performance [6]. The basic structure of the single-phase three-level NPC converter is shown in Fig. 2-1. It is not recommended to go for the higher number of levels with this basic structure of the NPC converter because of its increasing number of

clamping diodes, and control limitations [7]. This topology gives promising results due to its simplicity in control and structure but because of several limitations that led to advanced research related to this topology to mitigate those limitations. A state-of-art cost and higher levels of this topology are some of the main limitations as they are directly related. This topology is widely used in three-level applications because of promising results and better efficiency.
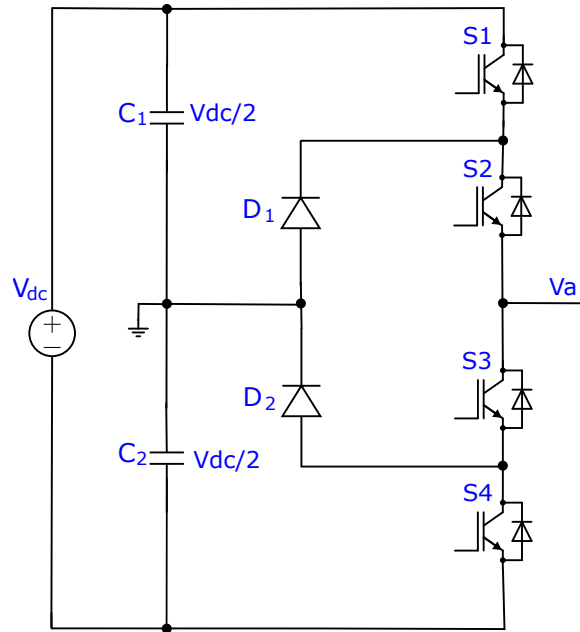
Figure 2-1: Single-phase 3L-NPC converter

Advantages

- The 3L-NPC can be easily implemented because of the simple structure and modulation techniques that reduce control complexity and associated costs.

- Because of the clamping diodes, the reverse blocking voltage of each power switch in a 3L-NPC topology is regarded as half of the DC-link voltage equalized.

- This provides a better dynamic response that improves the power quality and at the same time precisely controls the output voltage and current.

- 3L-NPC converter has lower switching losses because of the equal voltage stress

on each switching device that enhances the overall efficiency of the converter design.

- 3L-NPC converter has high efficiency due to this reason it is used in applications where power conversion is a critical factor.

Disadvantages

- Because the inner and outer semiconductor switches in a 3L-NPC converter operate under different conditions, then there is an unequal distribution of losses in the converter.

- It has higher conduction losses which requires a robust cooling system.

- Higher voltage levels are not appropriate for 3L-NPC because of the increasing number of clamping diodes and their cost.

2.1.2 Three-level active neutral-point clamped (ANPC) converter

If the derivative of the 3L-NPC converter is taken, the resulting configuration is the 3L-ANPC [8]. This 3L-ANPC addresses the issue of unequal power loss sharing across the semiconductor devices by employing two different modulation techniques known as carrier-based and space vector modulation techniques. Fig. 2-2, reflects the basic single-phase three-level ANPC structure which is comprised of two active switches (IGBTs) that replace the clamping diodes as in the case of 3L-NPC and because of that reason this topology is the advanced version of 3L-NPC converter. In a 3L-ANPC converter, the flow of the current in a zero-state direction can be controlled due to these active power devices. According to the previously listed PWM techniques, the majority of switching losses in the 3L-ANPC converter occur in the outer switches of each single-phase leg when carrier-based (CB-PWM) is used. However, by using space vector modulation, those switching losses can be transferred to the inner semiconductor switches. To obtain a better loss balance among switches,

the literature reveals the combination of both CB-PWM and SV-PWM methods or the modification of the inverter structure, but using one of these patterns does not employ the power loss balance over an entire switching period [9]. Other than the power loss balancing techniques of 3L-ANPC, to increase the power density corresponding to the basic structure, the hybrid structures are proposed and to reduce losses several switching patterns are exploited [10, 11].
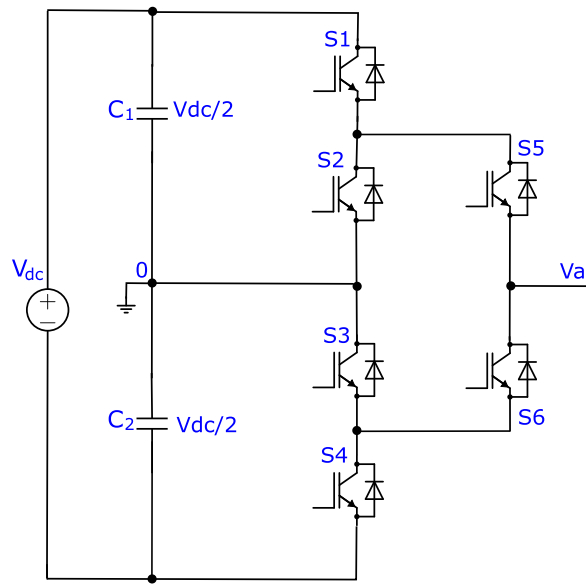
Figure 2-2: Single-phase 3L-ANPC converter

Advantages

- Maintaining a balanced loss distribution throughout power devices can significantly improve the 3L-ANPC output power rating and switching frequency.

- The two active switches in 3L-ANPC provide the controlled path for the neutral point current in place of the clamping diodes in 3L-NPC [12].

- Due to the carefully regulated power loss distribution among the semiconductor devices, 3L-ANPC thermal performance is uniform.

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Disadvantages

- Six active switches for single-phase, three-level operation is the primary draw-back of the 3L-ANPC. This feature raises overall conduction and switching power losses, which lowers converter efficiency.

- Reliability is also the main concern of this topology because of the active switches with the gate drivers [13].

2.1.3 Three-level stacked neutral-point clamped (3L-SNPC) converter

The 3L-NPC converter has an unequal power loss distribution problem, so to overcome this issue the evaluated version of the 3L-NPC converter is addressed as the three-level stacked neutral point converter as shown in Fig. 2-3. The voltage stress on the semiconductor devices is Vdc/2 because of the utilization of two clamping diodes as in 3L-NPC [14]. With the use of two back-to-back switches, the additional neutral point path can be achieved along with the opportunity to implement new PWM techniques. With these different sinusoidal PWM techniques, the apparent switching frequency of the 3L-SNPC can be doubled resulting the lower switching losses on the outer power devices of the topology. This topology gives better performance results under lower or high modulation index conditions by providing parallel conversion and more degrees of freedom.

Advantages

- The apparent switching frequency of the 3L-SNPC is doubled.

- Because back-to-back switches create an extra path for the neutral point, the power loss balancing problem is better and more balanced. [15].

- The load current is passed through two parallel paths in some switching states.

Disadvantages
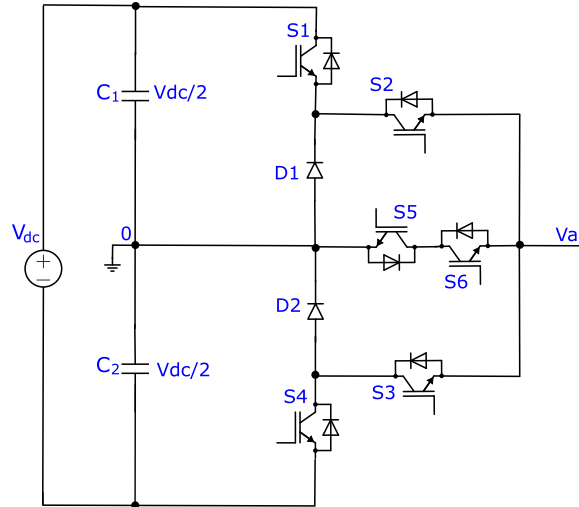
Figure 2-3: Single-phase 3L-SNPC converter

- Because at least four IGBTs must be operating at a switching frequency, the output power is lost. Additionally, because switching losses are directly correlated with switching frequency, efficiency is decreased.

- Higher conduction losses are the result of the load current flowing through at least two power devices during any switching condition.

2.1.4 Three-level active stacked neutral point clamped (3L-ASNPC) converter

The improvement in power density and efficiency can be achieved by reducing almost half of the average switching frequency of the semiconductor devices with the replacement of two diodes with two active switches in 3L-SNPC to get the active stacked neutral point clamped topology shown in Fig. 2-4. In 3L-ANPC or 3L-SNPC the apparent switching frequency is doubled but there is some problem with the switching of some devices in a half cycle of the switching period while some switch the entire period this limits the output power and maximizes the average switching frequency and this drawback is mitigated by the 3L-ASNPC converter and has more degrees of freedom to achieve the zero-state and with different PWM techniques can be controlled [16].
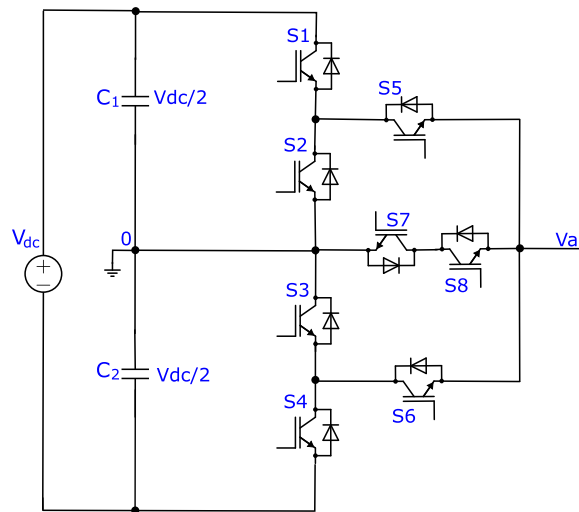
Figure 2-4: Single-phase 3L-ASNPC converter

Advantages

- The average switching frequency for all the power devices is reduced resulting in double the apparent switching frequency of the output voltage.

- The analysis of the switching states and sequences is done at one switching period for each polarity of the reference voltage because of the above advantage.

- It allows the better balancing of the total losses in switches for both low and high modulation indexes [17].

Disadvantages

- 3L-ASNPC has a complex control system and high cost because it requires more active switches.

- To balance the neutral point voltage advanced control algorithms are needed because the control strategies are more sophisticated because of additional active components.

- It reduces the overall efficiency of the converter because the current flow passes through many semiconductor devices so the conduction and switching power losses increase.

- Advance thermal solutions are required due to a higher number of active components.

2.1.5   Companies using 3L-NPC and 3L-ANPC topologies

The following table 2.1 expresses the names of the companies that are using 3L-NPC and 3L-ANPC for different applications and also shows the product series, voltage, and current rating of the products.

Company name	Product series	Topology	V/I/P rating	Application
Toshiba	T300MVi	NPC	6600 V/391 A	Drive
ABB	ACS6000	NPC	3-3.3 kV	Drive
ABB	ACS2000	ANPC	6 kV/800 kW	Drive
Schneider Electric	Altivar 1260	NPC	4.16 kV	Drive

Table 2.1: Companies using 3L-topologies

2.1.6   Three-level T-type converter (3L-T^{2}C)

The 3L-T-type converter, shown in Fig. 2-5, mitigates the potential problem of uneven power loss distribution in conventional 3L-NPC. Because this topology, in contrast to 3L-NPC and 3L-ANPC converters, does not benefit from voltage stress, it is not recommended for use in high-voltage applications [18]. The conventional two-level converters have a higher number of harmonics but compared to two-level converters, three-level T-type converters have easy control implementation, reduced number of components, and low conduction power losses making them flexible and cost-efficient solutions for the 3L-operation resulting in better waveform quality [19]. Using this design in hybrid applications allows for a greater variety of voltage levels and is more adaptable as in [20, 21].

Advantages

- The capacitor heating and losses are reduced due to reduced currents through the DC-link capacitors.
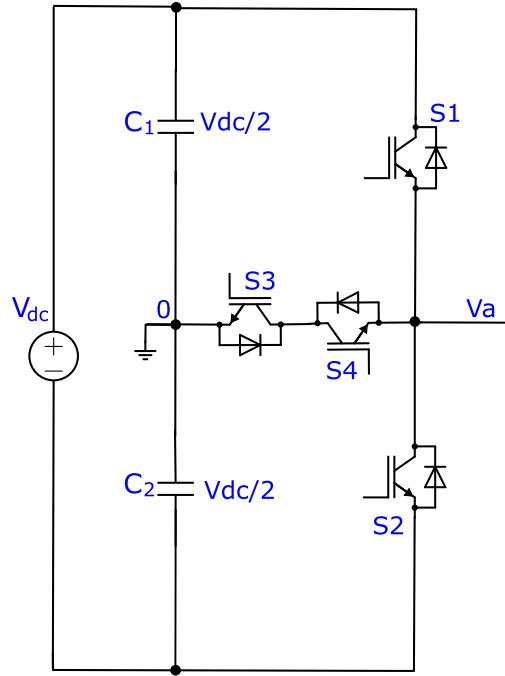
Figure 2-5: Single-phase 3L-T^2 converter

- To further reduce the losses, this topology can use the discontinuous PWM schemes without impacting the voltage deviation of the capacitor compared to the conventional topology [22].

- This topology has low conduction losses because two anti-series switches are at the neutral point path.

- It has a simple structure, easy control implementation, and reduces the unbalanced power loss distribution issue of power switches.

Disadvantages

- Usage of passive DC-link capacitors and voltage balancing schemes to balance of voltage levels among split DC-link capacitors increase switching losses by 10-15%.

- Active capacitor balancing schemes are used for better performance which requires more sensors for the operation.

- Inverter output voltage gets distorted if the capacitor voltages are not equal which results in degradation of output current.

- The DC-Link capacitors of the three-level inverter carry the load current, which heats them and creates problems under high-temperature operations of the inverter.

- To further reduce the switching losses, the discontinuous pulse-width modulation technique cannot be used since capacitor balancing and inverter PWM schemes are coupled.

- The half of the semiconductor components per leg has full DC-link reverse blocking voltage.

2.1.7 Companies using 3L-T-type converter topology (3L-T²C)

The following Table 2.2, expresses the names of the companies that are using 3L-T-type converter topology for different applications and also shows the product series, voltage, and current rating of the products.

Company name	Topology	Voltage rating	Current rating	Applications
Vinco-tech (149)	3L-T^2	650/1200 V	25-1800 A	Drives, solar inverters UPS
Fuji Electric (152)	3L-T^2	600/900/1200 V	50-600 A	Drivers, power conditioners UPS
Semikron (153)	3L-T^2	650/1200 V	50-600 A	Wind turbine converters solar inverters UPS
Infineon (154)	3L-T^2	650/1200 V	15-600 A	High-speed drives
Vinco-tech (151)	FC	1200 V	200 A	Drivers solar inverters UPS

Table 2.2: Companies using 3L-topologies

2.1.8 Three-level flying capacitor converters (3L-FC)

The flying capacitors are used without a clamped neutral point, and therefore the three-level flying capacitor design is not affected by the DC-link voltage balancing problem. To generate the voltage levels, DC sources are replaced with flying capacitors (FCs) and a higher number of voltage levels can be generated with this topology as shown in Fig. 2-6. The two most popular FC topologies, 3L-FC and 4L-FC, are regarded as mature converters for a variety of industrial applications, such as solar inverters and electric drives. The operation range of these types of converters is up to 0.86 modulation index with zero common mode voltage (Z-CMV). Different control algorithms and PWM techniques are used to deal with the elimination of common mode voltage, with the reduction of leakage current, low-frequency fluctuations, and bias voltage of FC because of the actual hardware asymmetry as in [23].

Advantages

- The 3L-FC converter offers improved adaptability, fault-tolerant performance, and equitable power loss distribution across the power switches.

- Because it remains operational if other topologies operating in hybrid settings
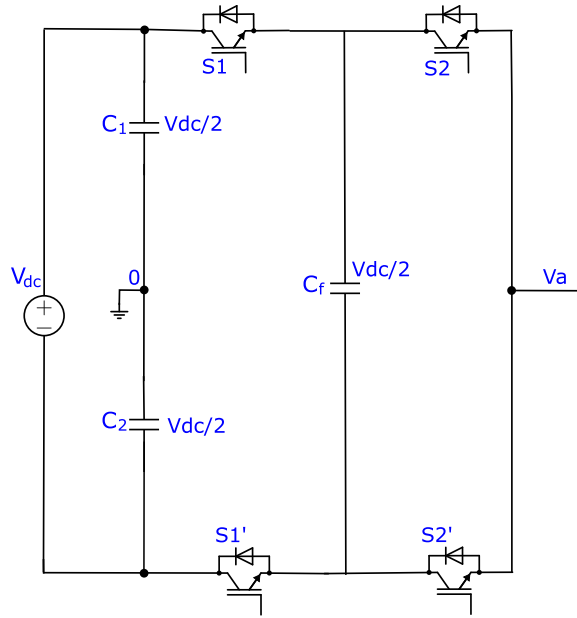
Figure 2-6: Single-phase three-level FC converter

fail, it has a high level of reliability among conversion systems.

- This topology pertains to smooth operation without bringing up the issue of DC-link balancing.

Disadvantages

- The low-frequency fluctuation, leakage current, and bias voltage of FC are the main issues with this topology.

- The pre-charging of the flying capacitors, voltage control of the FCs, and implementation of a huge count of capacitors are the major challenges with this topology [24, 25].

2.1.9 Three-level neutral-point piloted converters (3L-NPP)

There are two possible setups in which this design can be used. One power switch is located at the top and one at the bottom of the output leg of a single-phase, three-level NPP converter in the first type of implementation. On the other hand, the second configuration type uses a single-phase 3L-NPP converter with two semiconductor switches placed in series at the top and bottom of the output leg, as shown

in Fig. 2-7 and Fig. 2-8. The 3L-NPP converter, also called a T-type converter, is a single-phase device that comprises four IGBT transistors and four anti-parallel diodes with one semiconductor switch on each leg [26]. It is not suitable for medium voltage applications since it contains a single semiconductor switch on both the top and bottom legs of the converter. Small solar systems and other low-to-medium power applications are common uses for single-switch topologies. [27]. The 3L-NPP converter design with two switches at each leg provides greater advantages than the single switch per leg topology since there are two semiconductor switches connected in series at the top and bottom of the leg. Furthermore, compared to the one switch per leg of the 3L-NPP topology, the switching losses are halved. This allows for higher voltage levels to be used. The two switches that are connected anti-series
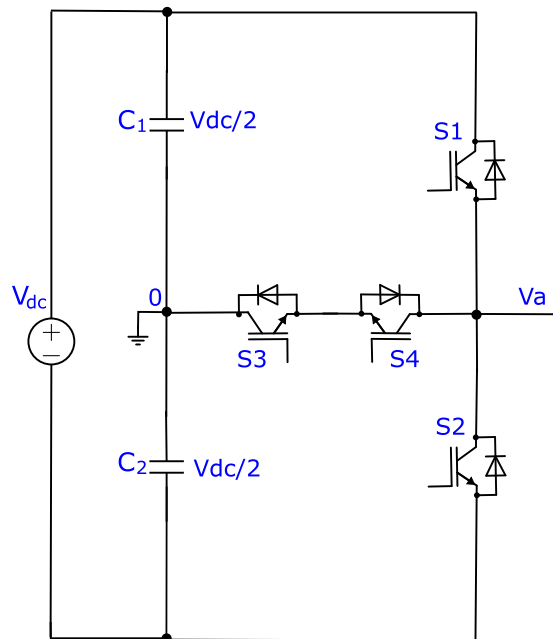
Figure 2-7: Single-phase 3L-NPP converter with one switch/leg

made the bidirectional switch and sometimes could be used in a soft-switching mode that depends upon the converter operation.

Advantages

- Because the 3L-NPP topology has greater output voltage levels, it performs better in terms of THD at higher modulation depths.

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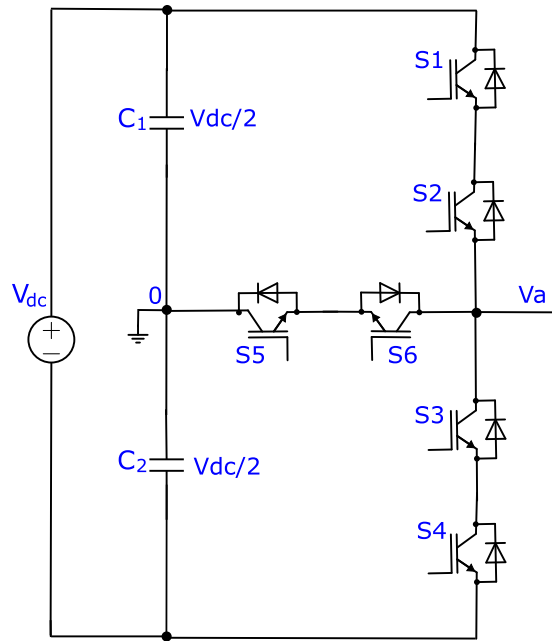
Figure 2-8: Single-phase 3L-NPP converter with 2 switches/leg

- This topology shows low voltage variation (dv/dt) and current ripple.

- A significant advantage of this topology is half the switching losses with two switches per leg.

Disadvantages

- The implementation cost is higher because of the number of semiconductor switches.

- This topology has higher conduction losses.

2.1.10   Three-level F-type converter (3L-FTC)

The 3L-FTC contains four semiconductor switches per single phase among these four IGBTs, the one semiconductor switch has to block the whole DC-link voltage in the reverse blocking mode of operation whereas half of the DC-link voltage is blocked by the rest of the three power switches that results in the reduction of voltage stress on the semiconductor switches [28]. This topology is modifying the 3L-T-type converter as shown in Fig. 2-9. The lower voltage stress of the three power

switches of this converter has cost and loss implications. Furthermore, according to the same topological characteristic, the F-type inverter performed more efficiently than its diode-free T-type equivalent.
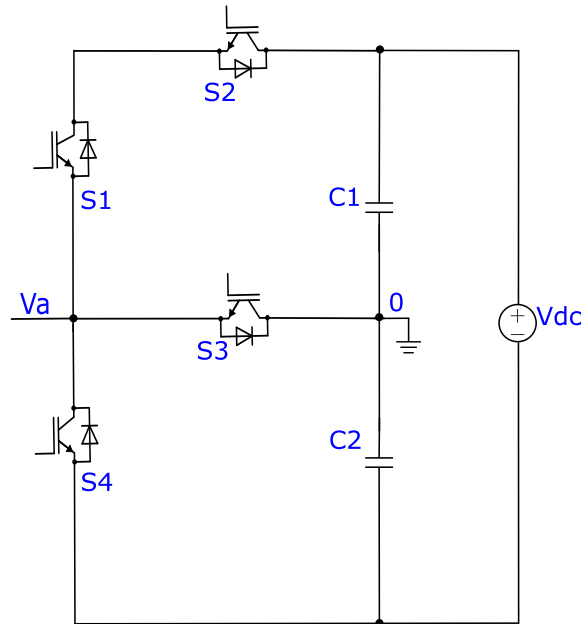
Figure 2-9: Single-phase 3L-FTC

Advantages

- The voltage stress on the semiconductor devices is low.

- It has lower conduction losses.

- The implementation cost is low compared to 3L-NPC and 3L-T-type converters.

- This converter has high efficiency compared to a T-type converter.

Disadvantages

- This topology is only used for low-to-medium voltage applications.

- One of the semiconductor switches has to sustain the whole DC-link voltage.

2.1.11 Single-phase three-level triple boost CG converter

Using a new configuration based on a three-level switching capacitor with common grounding, the input voltage can be boosted up to three times without involving any DC-DC boost converter stage. The parallel combination of two switched capacitors is selected to get the input PV voltage and generate the three levels of the voltage at the output. The configuration with common grounding is recommended to mitigate the leakage current by bypassing the stray capacitance resulting in the EMI reduction [29]. The configuration has six semiconductor switches including one bidirectional switch made by the combination of two anti-series switches S7 (S7p+s7n), two diodes (D1, D2), one uni-directional switch with diode in series (S6+D3), two switched capacitors and the dc-link which is the main element for the generation of negative boosted voltage for the negative cycle of grid voltage as in Fig. 2-10.
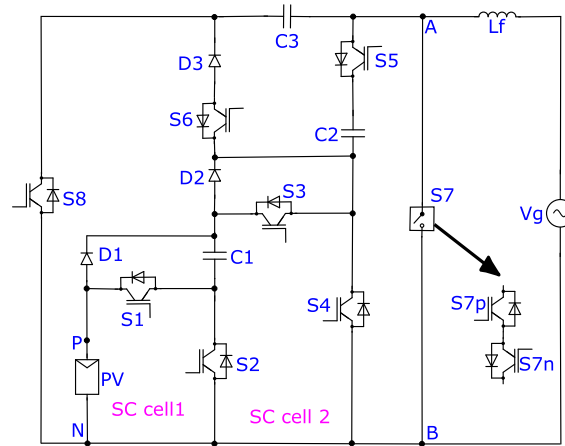
Figure 2-10: Single-phase 3L triple boost CG Inverter

Advantages

- With just one step, input DC voltage can be increased up to three times without needing an additional boost conversion stage.

- By using the common ground technique the EMI effect can be reduced by eliminating the leakage current.

- Because of the EMC problems, no EMI filter is required as EMC issues are mitigated.

- To generate the negative voltage at the output H-bridge is not required.

- All three capacitors—two SCs and one virtual DC-link—adopt the suggested PWM technique and are self-balancing.

- The ability to manage the reactive power flow between PV and the grid is a feature of the suggested topology.

Disadvantages

- It is an expensive design because more capacitors and semiconductor switches are required.

- The efficiency is not good because the total losses are high as several semiconductor switches are used.

2.1.12 Comparison of widely used three-level topologies

Among the discussed topologies, the 3L-NPC is considered the basic topology that is widely used in industrial, automotive, drives, grid, and low/medium voltage and high-power applications. Along with this topology, some of the topologies are revealed by changing the configuration of the 3L-NPC topology which are 3L-ANPC, 3L-SNPC, 3L-ASNPC, etc., The following Table 2.3, expresses the comparative analysis among the widely used 3L-topologies.

2.1.13 Commercial development of power modules

When the high-power electrical components are a combination of several devices or contain only a single device in a functional or isolated unit they are known as power modules. In this part of the report, the IGBTs and SiC MOSFET power modules their voltage and current ratings, and some of the major names of the companies are tabulated in Table 2.4. These are some of the main power modules of the related company that they are manufacturing. The Semikron Danfoss, designing the 1.5 MVA power stack which is under development by using 3L-NPC topology [30]. The power

S.no.	3L-Topologies	3L-NPC	3L-T-type	3L-FC	3L-F-type
1	Power switches per phase	2(n-1)	2(n-1)	2(n-1)	2(n-1)
2	Clamping diodes per phase	(n-1)(n-2)	0	0	0
3	DC bus capacitors	(n-1)	(n-1)	(n-1)	(n-1)
4	Balancing capacitors per phase	0	0	(n-1)(n-2)	0
5	Voltage unbalance problem	Yes(average)	No (Low)	Yes(High)	No (Low)
6	Voltage stress on power switches	Equally stressed (Vdc/2)	50% of switches are stressed to Vdc and 50% are stressed to Vdc/2	Equally stressed	One switch is stressed to Vdc, and the other three are stressed to Vdc/2
7	Modularity	Low	Low	High	Low

Table 2.3: Comparison of 3L-Topologies

stack by the Guasch components and power electronics by using Half-bridge topology is in the range of 230-500 kVA [31]. The power stacks were designed by using the H-bridge topology by the collaboration of Mersen (responsible for cooling, connection, protection, filtering, and assembling), Microchip (responsible for powering), and Agile switch (responsible for controlling (digital programmable drivers)) [32].

S.no.	Company name	Power modules	Voltage rating	Current rating	Product series
1	Semikron Danfoss	IGBT modules SiC MOSFET modules	1700V 1200V	1000A 485A	SKM1000GB17E4 SKM500MB120SC
2	Infineon	IGBT modules SiC MOSFET modules	3300V 2000V	2400A 400A	FZ2400R33HE4 FF3MR20KM1HP
3	ON Semi-conductors	IGBT modules	1200V	800A	NXH800H120L7QDSG
4	Mitsubishi electric company	IGBT modules SiC MOSFET modules	1200V 1200V	1400A 1200A	CM1400HA-24S FMF1200DXZ-24B
5	ST Micro-electronics	SiC MOSFET	750V	300A	SCTHS300N75G3AG
6	Fuji Electric	IGBT modules SiC MOSFET modules	1200-1700V 1700V	600-900A 400A	4MBI900VB-120R1-50 2CSI400DAHE170-50

Table 2.4: Available commercial power modules

2.2 PWM Techniques for 3L-NPC converter

Pulse width modulation is a powerful technique for controlling analog circuits with the digital outputs of a microcontroller and directly influences the overall efficiency of the system [33]. The basis for considering PWM techniques in a 3L-NPC converter are Low switching frequency voltage oscillations at neutral point, THD rate, total power loss percentage, and implementation complexity in a physical system. In this part widely used PWM techniques for 3L-NPC converter are discussed.

2.2.1 Space vector modulation (SVM) technique for 3L-NPC converter

There is a trade-off between the complexity and control demand of the converters. As complexity increases, control demand and objectives are crucial to consider when designing the converter. Converters with a common DC-link have issues related to DC-link voltage balancing, as in the case of the 3L-NPC, where the control of DC-link balance plays a vital role in avoiding undesirable impacts on the power devices [34].

This technique provides better results and is widely used for 3L-NPC converters. This technique contains the voltage vectors, including small, medium, and large voltage vectors that constitute the 19 voltage vectors for the commutation states, having 27 switching states for the 3L-NPC converter. The hexagon of the space vector has six sectors, and each sector has four regions as shown in Fig. 2-11 [35], in one of the four regions the reference voltage vector resides. SVM works by generating a reference vector (V_{ref}) from three nearby vectors that are formed with related states and switching times. For the implementation of the SV-PWM technique, the following key points must be noted for the calculation of the switching interval in SV-PWM.

- Sector identification.

- Identification of the region where the nearest three voltage vectors are lying.

- After the selection of the sector, the dwell time must be determined for that sector based on the reference vector.

- The switching sequence should be selected accordingly.

- For each of the switches, the switching time must be calculated.

The transformation of the switching state is dependent on the reference vector location in a particular sector. For the 3L-NPC converter, seven-segment synchronization is used to trigger the switches based on commutation pulse selection. The reference vector (V_{ref}) location varies in different sectors and regions depending upon the nearest three vectors as shown in Fig. 2-12 [35], for the sector-I.

Advantages

- DC-link capacitor voltages are balanced using the SV-PWM technique.

- Good for industrial utilization because of the digital performance dynamics in power electronic converters.

- This technique provides a low percentage of overall losses.

- The THD rate obtained using this technique is low.
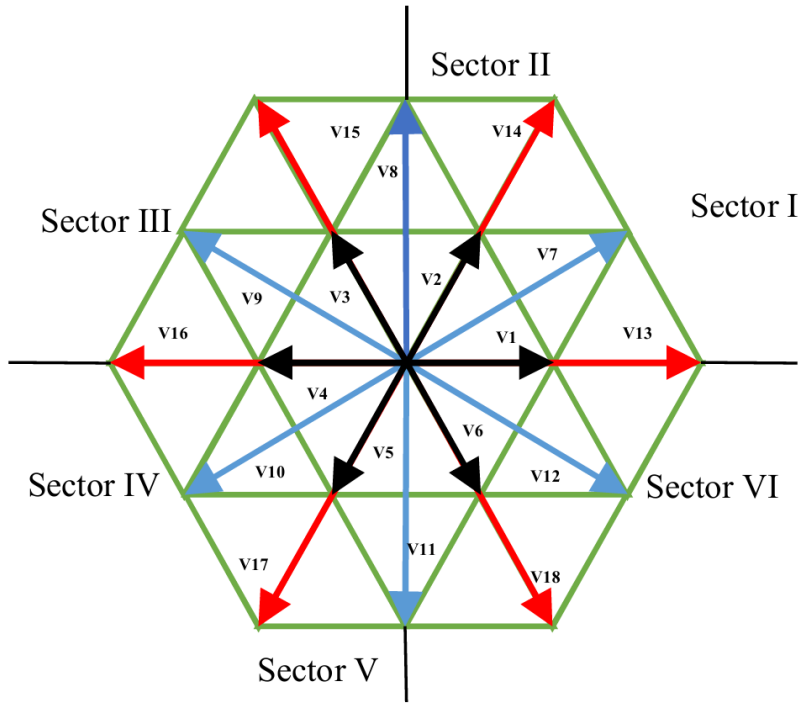
Figure 2-11: SV-PWM hexagon for 3L-NPC converter [35]
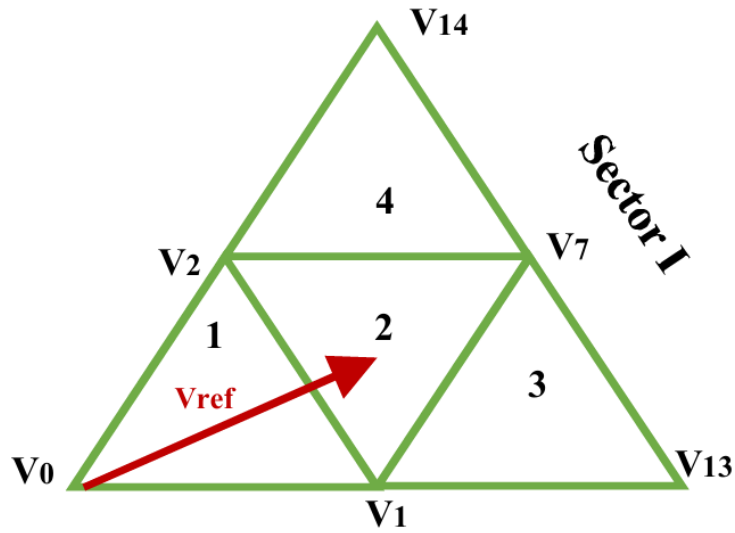
Figure 2-12: Reference voltage vector location in sector-I [35]

Disadvantages

- The complexity of the implementation is high.

- The extensive computation is required by this technique for the sector selection and switching time computation.

- It is complex to design the modulation strategies in this PWM technique.

2.2.2 Single carrier-based PWM technique for 3L-NPC converter (SCB-PWM)

Generally, the pulse width modulation techniques for the 3L-NPC converter are classified into two main groups i.e. space vector PWM and carrier-based PWM techniques. The carrier-based PWM technique is widely preferred among both methods because of its simple structure and easy implementation. In the CB-PWM technique, the sinusoidal/non-sinusoidal modulation signal is compared with two triangular carrier signals and is mostly used in traditional CB-PWM techniques for the three-level NPC converters [36]. The three-phase sinusoidal reference signals are given as;

$$
\begin{aligned}
V_a^* &= m_a \cos(\omega_s t) \\
V_b^* &= m_b \cos\left(\omega_s t - \frac{2}{3}\pi\right) \\
V_c^* &= m_c \cos\left(\omega_s t + \frac{2}{3}\pi\right)
\end{aligned}
\tag{2.1}
$$

where mx is called the modulation index where (x = a,b,c), ω_s is called the angular frequency, and $\omega_s t$ is called the phase angle. The suggested modulation technique uses the effective three-phase sinusoidal reference signal and the maximum and minimum of the three reference signals to modify the sinusoidal modulating signal. This method generates the gating pulses for the three-level converter using a single triangular carrier signal. For the suggested modulation technique, the modified modulation reference signal equation takes the following general form:

$$
\begin{aligned}
V_{km}^* &= V_{kP}^* + V_{kN}^* \\
V_{km}^* &= \left[V_k^* - \frac{\min(V_k^*)}{2}\right] + \left[\frac{V_k^* + \max(V_k^*)}{2} + 1\right]
\end{aligned}
\tag{2.2}
$$

Where V_{km}^*, V_{kP}^*, and V_{kN}^* represent the modulated modified reference signals, the positive and the negative reference signals respectively. The V_k^* represents the sinusoidal reference signals where (k = a,b,c). The block diagram of the proposed technique is depicted in Fig. 2-13 [36], and their reference modulation signals are shown in Fig. 2-14 [37] at the top, modified modulated signals at the middle, and gate pulses are shown at the bottom.
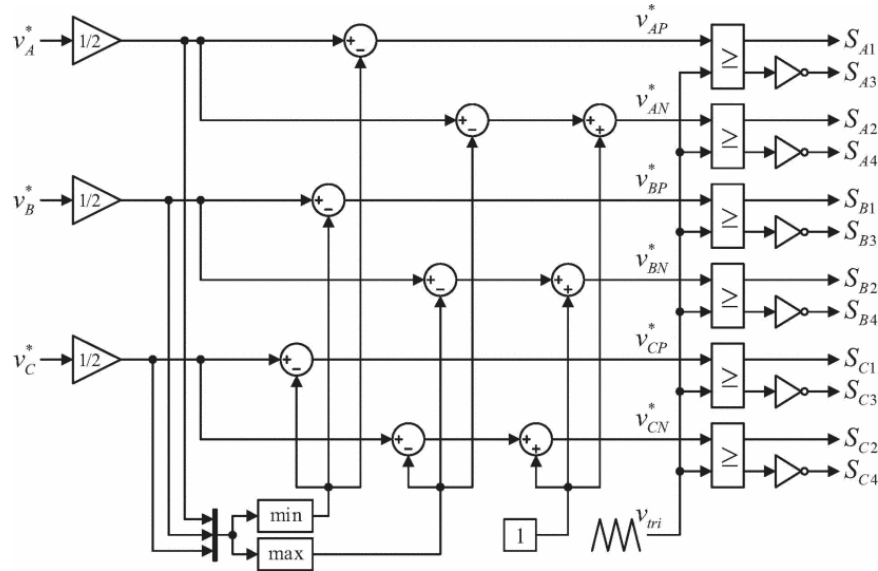
Figure 2-13: Single CB-PWM technique block diagram [36]

Advantages

- The single triangular carrier signal with a simple structure and easy implementation is used.

- The common-mode voltage control system eliminates the leakage current.

- The active and reactive power flow into the utility grid has an independent control system.

- This technique maintains the constant dc-link voltage.

Disadvantages

- It involves particular and altered modulation switching signals with analog circuits, which raises the implementation costs and complexity of the system.
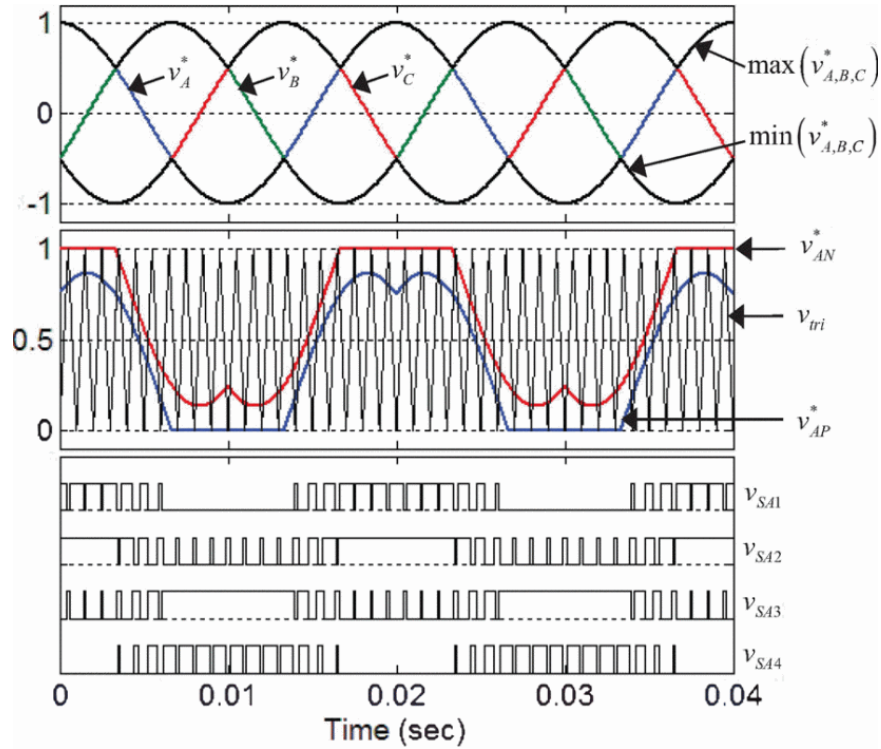
Figure 2-14: Gate pulse generation for 3L-NPC converter using single CB-PWM technique [36]

2.2.3 Carrier-based SPWM technique with two carrier triangular waves and zero-sequence voltage injection (CB-SPWM-ZVS)

The space vector modulation (SVM) technique can be classified as a carrier-based modulation technique. This is because, like traditional sinusoidal PWM (SPWM), it involves applying voltage vectors sequentially within a sampling period that aligns closely with the triangular carrier wave period. After determining the vectors used in a PWM cycle and calculating their duty cycles, SVM algorithms typically generate the converter output states by comparing these duty-cycle values to a double-slope triangular carrier. However, when examining the output phase voltages produced by SVM, they do not display a sinusoidal waveform [38]. This is because of the addition of a zero-sequence component to the fundamental frequencies. Although this zero-sequence component may not be evident when analyzing the line-to-line output

46

voltage, it contributes to achieving higher fundamental output voltage amplitudes when operating in linear mode. Alternatively, by incorporating an appropriate zero-sequence signal into the three-phase modulation signals, the same output patterns seen with space vector modulation (SVM) can be replicated using sinusoidal PWM (SPWM) [39].

The three-level NPC converter contains 27 switching states in the $\alpha\beta$ frame of reference. A two-layer hexagon centered at the plane origin indicates the space-voltage vectors in the $\alpha\beta$ frame as shown in Fig. 2-15 [40]. The switching states can be denoted as 1, 0, and -1 which correspond to the voltage levels of $\frac{V_{dc}}{2}$, 0, and $-\frac{V_{dc}}{2}$ respectively. The DC-link capacitors voltage balancing task can be achieved by the proper selection of the short vectors, i.e., 0-1-1/100, 00-1/110, -10-1/010, -1-10/001, 0-10/101 that supports the redundant switching states and the same line-to-line ac voltages are generated. However, the currents flowing into the neutral point (NP) with opposite directions are provided. Vector 0-1-1, for example, applies current i_a to the NP ($i_0 = i_a$), whereas vector 100 applies the same current to the NP but in the opposite direction ($i_0 = -i_a$). To obtain the "high" short vectors, which are 100, 110, 010, 011, 001, and 101, respectively, one level is added to each of the three integer values that constitute the "low" short vectors, which are $0-1-1$, $00-1$, $-10-1$, -100, -110, and $0-10$.

Correlation between nearest-three vectors (NTV-SVM) and CB-PWM with zero sequence voltage injection

The link between nearest-three space vector modulation (NTV-SVM) and carrier-based PWM (CB-PWM) with zero-sequence voltage injection is thoroughly examined by analyzing sector-1. With a few small adjustments, this analysis can be expanded to include the other sectors. A complete list of all feasible switching sequences for the sector-1 NTV method is shown in Table 2.5. The nearest-three vectors (NTVs) are determined for each sampling period, and the appropriate short vector or vectors are selected based on voltage-balancing parameters. Next, the optimal switching sequences are determined to minimize the switching frequency. To further reduce

switching events i.e. switching frequency, these sequences are reversed to avoid any switching during the transitions between sequences. The sequences that are referred to as "increasing sequences" have vector indices that rise steadily throughout the sequence, whereas the indices of the subsequent sequences, known as "decreasing sequences," decrease as in Table. 2.5. The NTV technique stands out due to its ability to lower switching frequencies when compared to other SVM strategies.

In the case of a three-level NPC converter using a CB-PWM technique, two carrier waveforms are symmetrically shifted about the zero axis. The high-frequency carrier signal waveforms and the sinusoidal modulating waveform are compared to obtain the switching signal patterns as in Fig. 2-16 [41]. In the context of the SVM approach, one phase not switching is equal to keeping the appropriate modulation reference signal clamped to one, zero, or minus one (1, 0, -1) for the duration of the PWM cycle. The clamping of phase a to one is required to retain the matching modulation signal (the higher DC-link rail). For the sake of clamping the AC-side voltages to a specific voltage level, a zero-sequence signal can be added to the sinusoidal-modulation reference signal waveform. For instance, Fig. 2-16, illustrates how the sinusoidal modulation reference signals are supplemented with a zero-sequence signal (v_{OFF}), which causes the modulation signals to be clamped at one for a portion of the time. As a result, throughout the relevant time frame, neither phase changes. If only a zero sequence component is added to the sinusoidal waveforms, the line-to-line voltages remain sinusoidal. The injection of the zero-sequence signal, however, has a significant effect on the NP current. Therefore, the voltage-balancing tasks can be assisted by a suitable injected signal. The most widely adopted common CB-PWM approach for the three-level NPC converter is the traditional SPWM technique with the subsequent zero-sequence signal, (v_{OFF}) and can be calculated as;

$$V_{\mathrm{OFF}} = -\left(\frac{V_{\max} + V_{\min}}{2}\right) \tag{2.3}$$
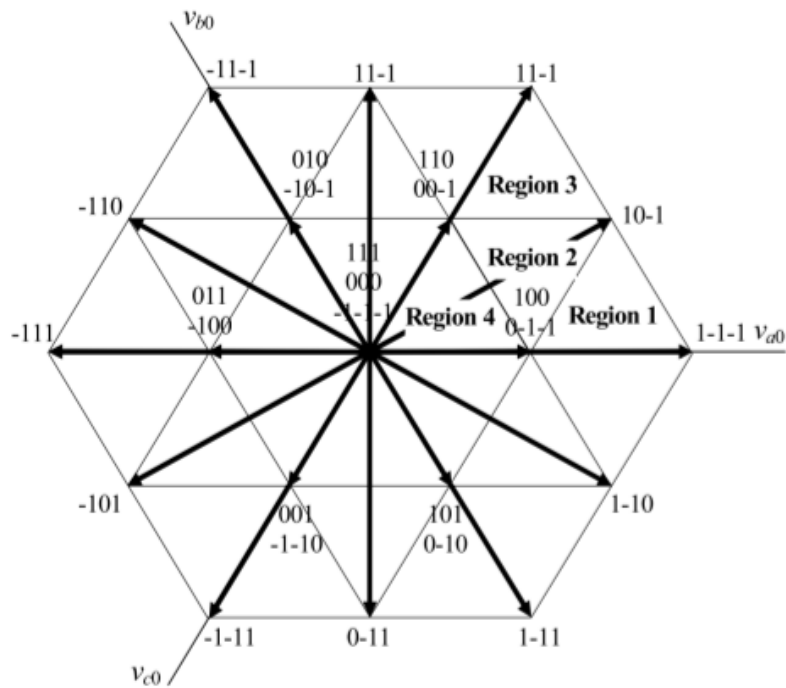
Figure 2-15: SV diagram for 3L-NPC converter [40]

Advantages

- DC-link voltage is balanced without implementing an additional control strategy.

- This technique reduces the switching frequency and as a result switching losses are reduced.

- At the neutral point the low-frequency oscillations are significantly reduced.

- As the technique requires less computational time and its feature of digital implementation makes it more attractive for an effective implementation.

- The implementation of this technique provides bandwidth extension capability of the linear modulation.

Disadvantages

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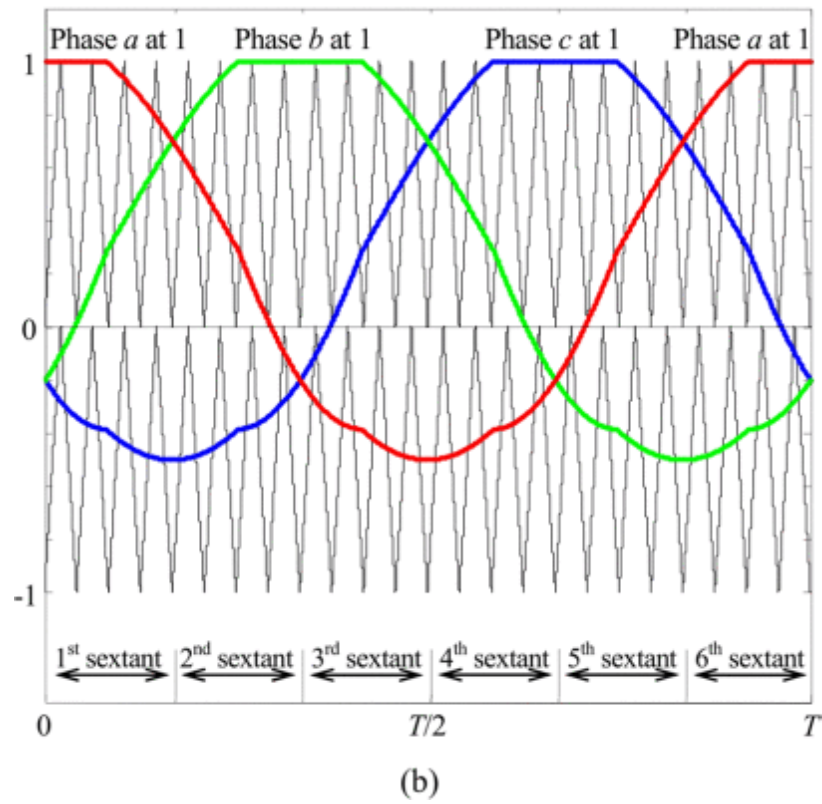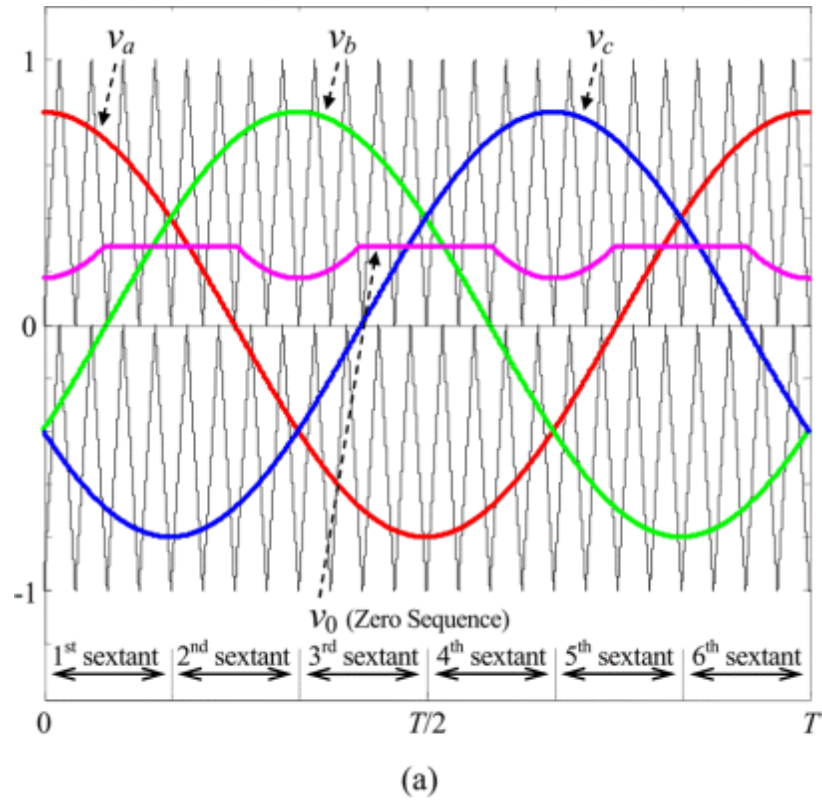
Figure 2-16: Modulation signals. a, Sinusoidal reference signal. b, Injection of positive zero-sequence voltage signal [41]

- At low modulation indices, the CB-PWM technique with zero-sequence voltage component injection fails to eliminate the low-frequency voltage fluctuations at the neutral point (NP).

2.2.4   Discontinuous PWM technique with zero-sequence signal injection (DPWM-ZSS)

The fundamental voltage produced by a three-phase inverter on the load or pumped into the grid can be controlled in several ways. Among the techniques being used at the moment are discontinuous techniques (DPWM), space-vector modulation (SVM), third harmonic injection (THIPWM), and sine-wave PWM (SPWM) [42]. Adopting a PWM approach or modulation method often aims to enhance system performance, including conversion efficiency, harmonic content (THD) or dynamic response, and switching losses. A zero-sequence signal (ZSS) injection is a common feature of many different kinds of algorithms. This PWM technique enables the modulation index (MI) of the power converter to have a larger linear range. In addition, the line voltages cancel out the inherent harmonics. Switching events can be decreased due to the rejection of certain harmonics, which also improves the switching losses in the inverter power components [43]. Generally speaking, it is feasible because these systems only impact switching for two-thirds of the signal cycle. The method utilized to obtain the ZSS signal distinguishes the various PWM modulation approaches examined. The resulting zero-sequence signal has three times the fundamental frequency, is discontinuous, and is periodic. Different waveforms show the sinusoidal reference wave with the injection of the zero sequence signal versus the produced DPWM signal. Carrier-based PWM modulators, or CB-PWMs, have been employed in each case. A variety of discontinuous PWM algorithms are described in the literature, including DPWM0, DPWM1, DPWM2, DPWM3, DPWM-Max, DPWM-Min, and others. Some of the techniques are shown in Fig. 2-17, and Fig. 2-18 [44]. Among the several DPWM modulation algorithms discussed, the most widely used ones are symmetric, meaning they result in equal power losses in upper and lower electronic

devices of power converters.
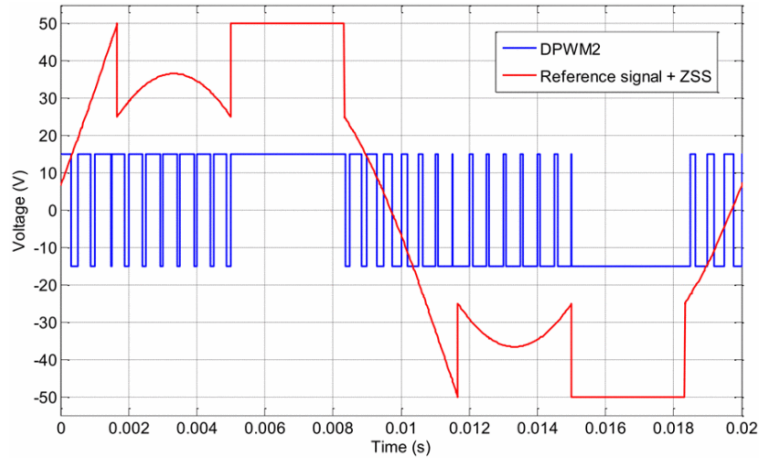
Figure 2-17: DPWM2 modulation method in comparison to zero sequence signal injection (ZSS) reference wave [44]
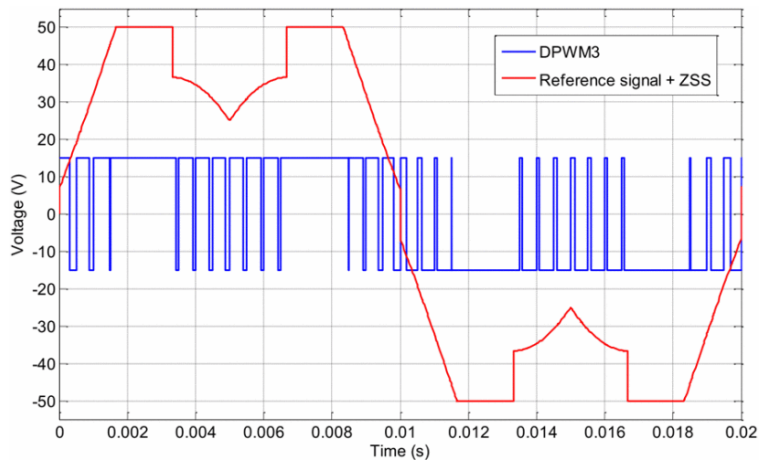
Figure 2-18: Zero sequence signal injection (ZSS) vs reference wave using the DPWM3 modulation approach [44]

Advantages

- DPWM increases the linear range of the modulation index.

- Using the DPWM technique, the switching events can be reduced, and the built-in harmonics in the line voltages are canceled.

- The switching losses are low and because of the low losses the conversion efficiency is increased.

- DPWM improves dynamic response and THD content.

- This increases the reliability of the system and maintains the constant dc-link voltage.

- The control of the active and reactive power flow into the utility grid is independent.

Disadvantages

- Unsymmetrical DPWM techniques cannot be used for voltage unbalance and power loss balance.

2.2.5 Hybrid PWM technique (H-PWM)

In this modulation technique, a zero sequence derived from space-vector modulation (SVM) patterns modifies the initial modulation signals, which are supplied by a controller in the manner described below:

$$
\begin{aligned}
\nu'_a &= \nu_a - \nu_0 \\
\nu'_b &= \nu_b - \nu_0 \\
\nu'_c &= \nu_c - \nu_0 \\
\text{where } \nu_0 &= \frac{\max(\nu_a, \nu_b, \nu_c) + \min(\nu_a, \nu_b, \nu_c)}{2}
\end{aligned}
\tag{2.4}
$$

The goal of doing this is to give the linear operation mode its greatest range. From these signals, two modified modulation signals are obtained for each phase, which need to achieve;

$$
\begin{aligned}
\nu'_a &= \nu_{ap} + \nu_{an} \\
\nu'_b &= \nu_{bp} + \nu_{bn} \\
\nu'_c &= \nu_{cp} + \nu_{cn}
\end{aligned}
\tag{2.5}
$$

where $\nu_{ip} \geq 0$, and $\nu_{in} \geq 0$ with $i = \{a, b, c\}$. The signals with the subscript 'p" will only cross the upper carrier $\nu_{p\text{carrier}} \in [0, 1]$, while the signals with the subscript n" will only cross the lower one $\nu_{n\text{carrier}} \in [-1, 0]$. The output current of the converter

is injected into this location when one of its phase legs is clamped to the NP. The expression for the NP current i_0 is as follows;

$$i_0 = s_{a0}i_a + s_{b0}i_b + s_{c0}i_c \tag{2.6}$$

in which the control functions $s_{i0} = \{0, 1\}$ for $i = \{a, b, c\}$. When the relevant output phase is linked to the NP, they take on the value "1"; otherwise, they have a value of "0".

To ensure voltage balance, the NP current locally averaged value needs to be zero. The switching period (Ts) is the definition of the window-width value of the averaging operator. The following is an expression for the locally averaged NP current:

$$\bar{i}_0 = \left|\nu_{an}^{+1} - \nu_{ap}\right| \cdot \bar{i}_a + \left|\nu_{bn}^{+1} - \nu_{bp}\right| \cdot \bar{i}_b + \left|\nu_{cn}^{+1} - \nu_{cp}\right| \cdot \bar{i}_c \tag{2.7}$$

In this expression, the variables $\left|\nu_{in}^{+1} - \nu_{ip}\right|$ for $i = \{a, b, c\}$ are the duty cycles of the NP connection (d_{i0}), where $\nu_{in}^{+1} = \nu_{in} + 1$. A solution that achieves $\bar{i}_0 = 0$ is as follows:

$$\nu_{ip} = \frac{\nu_i - \min(\nu_a, \nu_b, \nu_c)}{2} \tag{2.8}$$

$$\nu_{in} = \frac{\nu_i - \max(\nu_a, \nu_b, \nu_c)}{2} \tag{2.9}$$

for $i = \{a, b, c\}$. To control the voltage balance of the capacitors, however, $\bar{i}_0 = 0$ must be generated sometimes.

Modulation signals for DSPWM and SPWM are displayed in Fig. 2-19 [45].

To attain a similar range as achieved in the case of DSPWM in the linear operation mode, a converter designer should know that the SPWM signals include the zero sequence derived from SVM patterns. In this example, one of the DSPWM modulation signals aligns with the SPWM signal within the intervals $0 \leq \omega t \leq \frac{\pi}{3}$, $\frac{2\pi}{3} \leq \omega t \leq \frac{4\pi}{3}$, and $\frac{5\pi}{3} \leq \omega t \leq 2\pi$. During these intervals, the other DSPWM modulation signal is held at zero. As a result, the switching pattern of switches obtained are similar to those which were produced by SPWM. Therefore, the switching patterns differ only
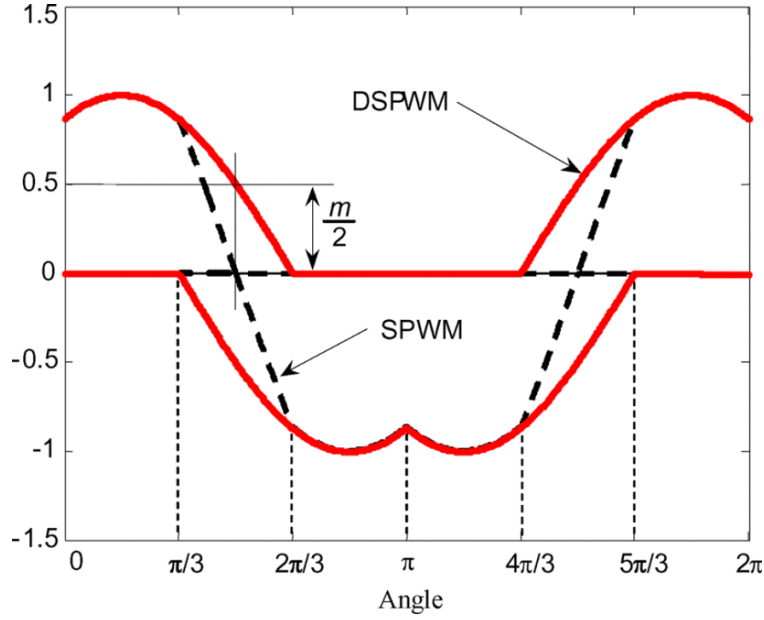
Figure 2-19: Modulation signals for the DSPWM and SPWM techniques [45]

during the intervals $\frac{\pi}{3} \leq \omega t \leq \frac{2\pi}{3}$ and $\frac{4\pi}{3} \leq \omega t \leq \frac{5\pi}{3}$. The basis of HPWM is the transient clamping of a single modulation signal during non-common periods. This moves DSPWM in the direction of SPWM. By further restricting the modulation signals to zero, the switching frequency of transistors can be reduced. Their switching losses consequently drop. The shared variable D that has values in the range [0, 1] defines the precise combination. When the value of this parameter D is set to digital outputs i.e. either zero or unity, the HPWM transforms into DSPWM or SPWM, respectively. Fig. 2-19 [45], demonstrates that the absolute value of the DSPWM modulation signals is precisely half the modulation index (m = amplitude of the modulation signals) when the SPWM modulation signal passes zero. The variable x used for this is calculated as in equation 2.10.

$$x = D \cdot \frac{m}{2} \tag{2.10}$$

A sample with D = 0.5 of each modulation strategy clamped for the non-common intervals, is shown in Fig. 2-20. The following requirements are applied to do this:

55
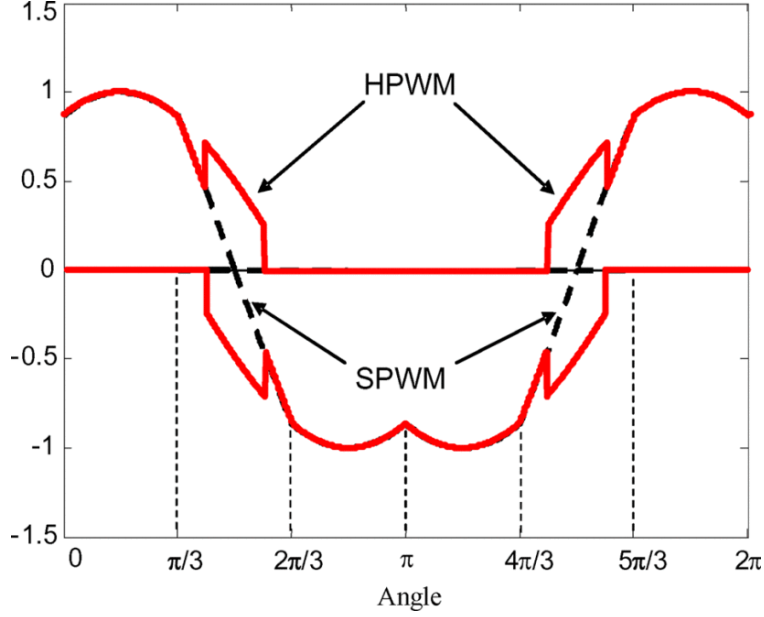
Figure 2-20: Modulation signals for the HPWM [45]

$$\nu_{i,\text{off}} = \begin{cases} \nu_{ip} & \text{if } \nu_{ip} \leq x \\ 0 & \text{otherwise} \end{cases} \tag{2.11}$$

$$\nu_{i,\text{off}} = \begin{cases} -\nu_{in} & \text{if } -\nu_{in} \leq x \\ 0 & \text{otherwise} \end{cases} \tag{2.12}$$

The variable $\nu_{i,\text{off}}$ for $i = \{a, b, c\}$ is the offset that needs to be applied to phase i, DSPWM signals to prolong zero clamping. If a modulation signal (e.g., ν_{in}) is modified, It should have the opposite sign relative to the other signal. (ν_{ip}) to prevent low-frequency distortion of the output voltages. The relationships listed below are used to meet this principle:

$$\nu_{ip\_HPWM} = \nu_{ip} - \nu_{i\_off}$$
$$\nu_{in\_HPWM} = \nu_{in} + \nu_{i\_off} \tag{2.13}$$

In Fig. 2-20, during $\frac{\pi}{3} \leq \omega t \leq \frac{2\pi}{3}$ and $\frac{4\pi}{3} \leq \omega t \leq \frac{5\pi}{3}$, At some intervals, the HPWM modulation signals line up with the DSPWM waveforms, and at other times, with the SPWM waveforms.

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Advantages

- HPWM reduces the switching frequency, reducing the switching losses.

- HPWM attenuates the neutral point low-frequency voltage oscillations.

Disadvantages

- This reduces the max: voltage applied to the capacitors.

- This decreases the efficiency of the converter.

2.2.6 Carrier-based double signal (partial dipolar) in conjunction with zero-sequence signal (CB-DSPWM-ZSS)

Modulation modes in carrier-based modulation systems can be classified as dipolar, partly dipolar, or uni-polar depending on how many switching states are made in a single fundamental cycle [46]. The partial dipolar mode of modulation, which offers the best capacity to regulate NP imbalance among the three modes, is typically used for conventional motor control applications. The suggested modulation method falls under the partial dipolar mode group. By injecting a zero sequence voltage ν_0 to the reference voltage ν_i^* in this approach, the inverter linear range of operations increases and the adjusted modulation signal becomes;

$$v_i' = v_i^* + v_o \quad \text{for } i \in \{a, b, c\} \tag{2.14}$$

where ν_0 is represented as;

$$v_o = -\frac{\max(v_a^*, v_b^*, v_c^*) + \min(v_a^*, v_b^*, v_c^*)}{2} \tag{2.15}$$

This modified signal is now used to generate two auxiliary modulating signals per phase (v_{ip}) and (v_{in}) that control the upper arm switch-pair S1, S2 and lower arm switch-pair S3, S4, respectively. The auxiliary signals must satisfy this equation (2.18)

to avoid noise for all phase angles.

$$v_i' = v_{ip} + v_{in} \qquad (2.16)$$

where

$$v_{ip} = \frac{v_i - \min(v_a, v_b, v_c)}{2} \qquad (2.17)$$

$$v_{in} = \frac{v_i - \max(v_a, v_b, v_c)}{2} \qquad (2.18)$$

for $v_{ip} \in [0,1]$ and $v_{in} \in [-1,0]$ The average neutral point current calculation can be done using the above auxiliary modulating signals, in which the duty factor for the neutral point connection is the difference between these two modulating signals, and their value is used to generate the average NP current. At steady-state the average NP current is zero for balanced load conditions. But if an imbalance is found, the duty factor is adjusted by varying the zero sequence current component, which results in a non-zero average neutral current flowing in the intended direction to offset voltage imbalances. The theoretical maximum modulation index of this scheme is 1.1547, which is the same as that of the third harmonic injected PWM (THIPWM) scheme [47].

Advantages

- This PWM technique eliminates the voltage unbalances at the neutral point for full PF range and high modulation indices and also controls the DC-link voltage unbalance.

- It mitigates the low-frequency voltage oscillations at the neutral point.

- Using this technique, the linear range of operation of the converter can be increased.

- This PWM technique is simple and can be easily implemented.

Disadvantages

- Uni-polar and dipolar-based double signal PWM techniques do not provide proper NP voltage unbalance control capability and are used for normal motor control applications.

2.2.7 A simple zero-sequence voltage injection method for carrier-based pulse width modulation (simple CB-PWM-ZVS)

In CB-PWM systems, offset signals were added to double reference signals in [48] and [49] to deliver double-modulation signals that balanced and removed the DC-link capacitor voltage ripples. The duration required to balance the DC-link capacitance voltages remained constant and unaffected by the load power factor, as the double-modulation signals generated a steady NP current. However, to generate the offset signals, the reference voltage vector angle needs to be known instantaneously, which necessitates the calculation of inverse trigonometric functions. The CB-PWM method described in [50] modified the switching sequence of one phase per PWM cycle to reduce the common-mode voltage in three-level NPC inverters. It also employed double-modulation signals to prevent voltage ripples in the DC-link capacitor. However, this approach led to increased phase-to-phase voltage distortions and higher switching power losses, as noted in [51].

In this technique, the three sinusoidal reference voltages used are;

$$
\begin{aligned}
v_{a,\text{ref}} &= m \cdot \cos(2\pi f_s t) \\
v_{b,\text{ref}} &= m \cdot \cos(2\pi f_s t - \frac{2\pi}{3}) \\
v_{c,\text{ref}} &= m \cdot \cos(2\pi f_s t + \frac{2\pi}{3})
\end{aligned}
\tag{2.19}
$$

where f_s is the fundamental frequency and m is the modulation index of the reference voltages. In this technique, the calculation of the zero-sequence component does not

require the three-phase currents and can be given as [52];

$$v_{zs} = \begin{cases} v_{zs,\text{max}} = 1 - \max(v_{a,\text{ref}}, v_{b,\text{ref}}, v_{c,\text{ref}}), & \text{if } V_{c1} \geq V_{c2} \\ v_{zs,\text{min}} = -1 - \min(v_{a,\text{ref}}, v_{b,\text{ref}}, v_{c,\text{ref}}), & \text{if } V_{c1} < V_{c2} \end{cases} \qquad (2.20)$$

Note: As this technique is implemented so further detailed discussion about this technique can be explained in the three-phase 3L-NPC converter simulation chapter.
Advantages

- The suggested approach uses a set PWM frequency for switching, and it does not take into account the comparison between V_{c1} and V_{c2} while figuring out how many switching transitions there are in every switching phase.

- When the suggested CBPWM is applied, its switching loss is decreased by $1/3$ since there are $1/3$ fewer switching transitions than with the normal SPWM.

- The simple structure, requires less computation time and is easy to implement.

- At the neutral-point lower-frequency oscillations are reduced using this PWM technique.

- The linear range of the modulation index increases.

- To control the DC-link voltage unbalance there is no need to implement the additional control circuitry.

- The line-to-line voltage with the lowest THD was obtained by the CBPWM in terms of computation time and memory usage.

Disadvantages

- The only disadvantage of this PWM technique is it requires voltage sensors for the DC-link voltage to measure and compare them to provide the offset voltage to maintain the balance of the DC-link voltage of capacitors.

2.2.8 Phase opposition disposition (POD-PWM) technique

This PWM technique comes under the classification of multi-carrier pulse width modulation techniques [53]. In this technique, the required number of carrier signals depends upon the number of output voltage levels denoted by "n". Since there are three output voltage levels in this instance, the following equation can be satisfied using two carrier signals.;

$$N = n - 1 \tag{2.21}$$

where "N" represents the number of carrier signals used for a particular level of output voltage.

Note: This technique is used for the analysis of single-phase 3L-NPC converter and is explained in detail in chapter no. 3.

Advantages

- POD PWM can significantly reduce the total harmonic distortion (THD) in the output voltage and current compared to traditional two-level PWM techniques. This leads to better power quality and less stress on the load and power network.

- In a 3L-NPC converter, maintaining the balance of the neutral point voltage is crucial. POD PWM helps in better distribution of the switching states, which aids in maintaining the neutral point voltage balance.

- By appropriately timing the switching events, POD PWM can reduce the number of switching transitions required per cycle, leading to lower switching losses and improved efficiency of the converter.

- POD PWM generates symmetrical switching patterns, which can help in reducing the common-mode voltage generated by the converter. This can result in lower electromagnetic interference (EMI) and better performance in sensitive applications.

Disadvantages

- In some operating conditions, especially under low modulation indices, POD PWM may still cause drift in the neutral point voltage, necessitating additional balancing strategies or circuits.

- While POD PWM helps in maintaining neutral point voltage balance, it still requires careful design and additional control mechanisms to ensure that the neutral point voltage does not drift over time, especially under unbalanced load conditions.

Table 2.6 shows the comparative analysis of the widely used PWM techniques for 3L-NPC converters based on DC-link voltage balance, low-frequency voltage oscillation at the neutral point, switching frequency, computational time, system reliability, THD rate, etc.

2.3 Summary of the literature review

In this chapter, the state-of-art three-level converter topologies are studied at the beginning for the selection of the 3L-converter topology, and then among those topologies 3L-NPC and 3L-NPP converter topologies are selected for analysis based on power losses, efficiency, and cost-effectiveness which will be explained in detail in the next chapter i.e., chapter 03. This selection is made based on the DC-link voltage unbalance, elimination of fluctuations in low-frequency voltage oscillations at the neutral point, uneven distribution of losses, number of components, structure complexity, implementation in hardware, and modularity. The 3L-NPC converter topology is selected and PWM techniques for the 3-phase converter system are studied from the literature. It is concluded that based on the DC-link voltage unbalance, mitigation of the low-frequency voltage level oscillations at the NP, switching frequency reduction, operating range of linear modulation, computational time, reliability of the system, unbalance loss distribution, and implementation complexity a simple zero-sequence voltage injection method for carrier-based PWM of three-phase three-level NPC converter is selected. It must be noted that the single-phase 3L-NPC converter

phase opposition disposition (POD-PWM) technique is selected in comparison with the standard sinusoidal PWM technique and for 3L-NPP topology simple sinusoidal PWM technique is selected and for the three-phase 3L-NPC converter, a simple zero-sequence voltage injection method for carrier-based pulse width modulation is used to analyze as mentioned above.

Region	Short Vectors	Sequences of vectors (Increasing and Decreasing Sequences)	Switching Steps	No Switching phases
1	0-1-1 100	(0-1-1/1-1-1/10-1 10-1/1-1-1/0-1-1) (1-1-1/10-1/100 100/10-1/1-1-1)	2//2 2//2	c clamped to -1 a clamped to 1
2	(0-1-1/00-1 0-1-1/110 100/00-1 100/110	(0-1-1/00-1/10-1 10-1/00-1/0-1-1) (0-1-1/10-1/110 110/10-1/0-1-1) (00-1/10-1/100 100/10-1/00-1) (10-1/100/110 110/100/10-1)	2//2 4//4 2//2 2//2	c clamped to -1 None b clamped to 0 a clamped to 1
3	00-1 110	(00-1/10-1/11-1 11-1/10-1/00-1) (10-1/11-1/110 110/11-1/10-1)	2//2 2//2	c clamped to -1 a clamped to 1
4	0-1-1/00-1 0-1-1/110 100/00-1 100/110	(0-1-1/00-1/000 000/00-1/0-1-1) (0-1-1/000/110 110/000/0-1-1) (00-1/000/100 100/000/00-1) (000/100/110 110/100/000)	2//2 4//4 2//2 2//2	a clamped to 0 None b clamped to 0 c clamped to 0

Table 2.5: Sector-I: Vector sequences

y

PWM Techniques	SVM	Single CB-PWM	CB-S PWM ZVS	D-PWM ZSS	H-PWM	CB DS-PWM ZVS	Simple CB-PWM ZVS
DC-link Voltage Balance	Yes	Yes	Yes	Yes	No	Yes	Yes
Mitigation of low-frequency voltage oscillations at NP	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Low Switching frequency	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Extension of linear modulation range	No	No	Yes	Yes	No	Yes	Yes
Low computational processing time	No	Yes	Yes	No	No	No	Yes
Increases reliability of system	Yes	No	Yes	Yes	No	No	Yes
Implementation complexity	Yes	No	No	No	Yes	No	No
Low-THD rate	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table 2.6: Comparison of widely used PWM techniques for 3-phase 3L-NPC converter

Chapter 3

Comparative analysis of 3L-NPC and 3L-NPP converter

This chapter explains the comparative analysis between the two single-phase three-level converter topologies, i.e., single-phase 3L-NPC and single-phase 3L-NPP converter based on their power losses, efficiency, and cost-effectiveness. In the first part of the chapter, the explanation of the three-level NPC converter is given related to the working principle of the topology, implementation of the PWM technique, and analytical calculation of the power losses and efficiency, then those results are compared with the simulation results, and is same procedure is done for the 3L-NPP converter in the second part of the converter, and then in the last part of the chapter comparison is done between both the converters. It must be remembered that this entire analysis is done during the steady-state operation of the converter and devices.

3.1 3L-NPC converter

The 3L-NPC converter topology is one of the basic and widely used multilevel converter topologies in industrial motor drive, renewable energy systems, transportation, power quality and grid support, uninterruptible power systems (UPS), HVDC transmission systems, aerospace and defense, smart-grid systems, and energy storage systems, etc., This topology is widely used compared to the two-level inverter because

of the improved efficiency, better total harmonic distortion results, higher voltage operation, enhanced reliability, lower switching losses, smoother voltage transition, and better dynamic response. Fig. 3-1, shows the basic circuit diagram of the 3L-NPC converter including power devices, clamping diodes, and DC-link capacitors. The number of electronic components required to design a single-phase 3L-NPC converter can be calculated using table 3.1 [54].
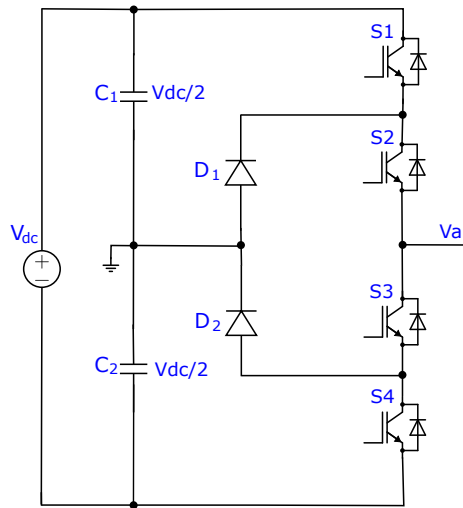
Figure 3-1: Single-phase leg of 3L-NPC converter

Semiconductor switches per phase	Flying capacitors	Flying diodes	DC capacitors
2 (n-1)	0	(n-1) (n-2)	(n-1)

Table 3.1: Calculation of power electronic components for 3L-NPC converter [54]

In the design of a single-phase 3L-NPC converter, four IGBT power devices with anti-parallel diodes, two clamping diodes, and two DC-link capacitors are required. In the circuit diagram of 3L-NPC, it can be seen that the upper part of the single leg has two IGBTs that are connected in series and their mid-point is connected to the clamping diodes and the mid-point of two series connected clamping diodes has a connection with the series connected DC-link capacitors at their mid-point.

3.1.1 Working principle of single-phase 3L-NPC converter

Referring to the circuit diagram of the 3L-NPC converter in Fig. 3-1, it is observed that each power device in this structure can sustain the voltage stress of $\left(\frac{V_{dc}}{2}\right)$ i.e., half of the DC-link voltage. It is important to remember that in a 3L-NPC converter, the switches S1 and S3, S2 and S4 are complementary. The working principle of the 3L-NPC topology can be explained based on the direction of the voltage and current. The analysis here considers the four cases based on the flow of current and output voltage (as the flow of current from source to load i.e., load side current is considered positive and vice versa. Based on this analysis switching states of the converter can be generated.

Case# 01

In this case the output current i.e., $I_L > 0$, and also the output voltage i.e., $V_o \geq 0$, including two possible switching operations. In one operation mode, the switches of the upper leg of converter S1 and S2 are at the on state and conduct the current from the source to the load and generate the output voltage of $\left(+\frac{V_{dc}}{2}\right)$. But when the output voltage is 0, switch S1 is turned off but S2 is turned on continuously to operate with upper clamping diode D1 as in Fig. 3-2. In this case, the switch S2 is turned-on always. So, when $V_o = 0$ then switch S1 and clamping diode D1 are commutated which is due to the effect of the switching action of power switch S1. This is also called the small commutation loop because it involves the commutation process with S1, D1, and C1. So both the modes of operation are considered based on the switching of S1. It can be found that due to the commutation loop switch S1 is going to have some off-voltage spike stress because of the stray inductance of the commutation loop.

Case# 02

In this case the output current i.e., $I_L > 0$ and also the output voltage i.e., $V_o \leq 0$, including two operations when $V_o = 0$ and when $V_o = -\frac{V_{dc}}{2}$. When the $V_o = 0$ power
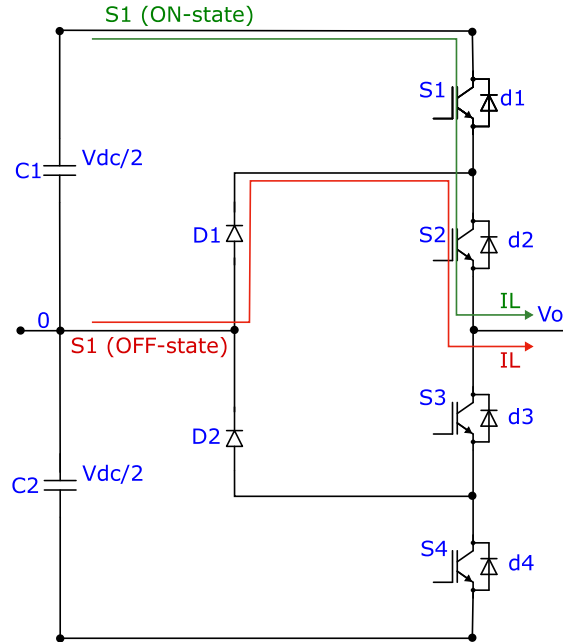
Figure 3-2: 3L-NPC converter operation case# 01

device S2 and clamping diode D1 are turned on and conduct the current towards the load. When switch S2 is turned off then the output voltage is $\left(-\frac{V_{dc}}{2}\right)$ and the current starts conducting through the d3, and d4 anti-parallel diodes of switches S3 and S4 respectively, and generates that voltage level. Here S2, D1, and d3 are commutated because of the switching of the switch S2. This is also known as the large commutation loop because it involves the commutation process with S2, D1, d3, d4, and C2. Fig. 3-3, represents the case. 02 which is based on the switching of S2. Remember that due to the commutation loop switch, S2 is going to have some off-voltage spike stress because of the stray inductance of the commutation loop.

Case# 03

In this case the output current i.e., $I_L < 0$, and also the output voltage i.e., $V_o \leq 0$. In this case, the switch S3 is going to be turned on always in this state. During this case operation when the output voltage is $\left(-\frac{V_{dc}}{2}\right)$ the current passing through the S3 and S4 towards the dc-link from the load. But when switch S4 is turned off then switch S3 and the clamping diode D2 start conducting the current from load to the

70
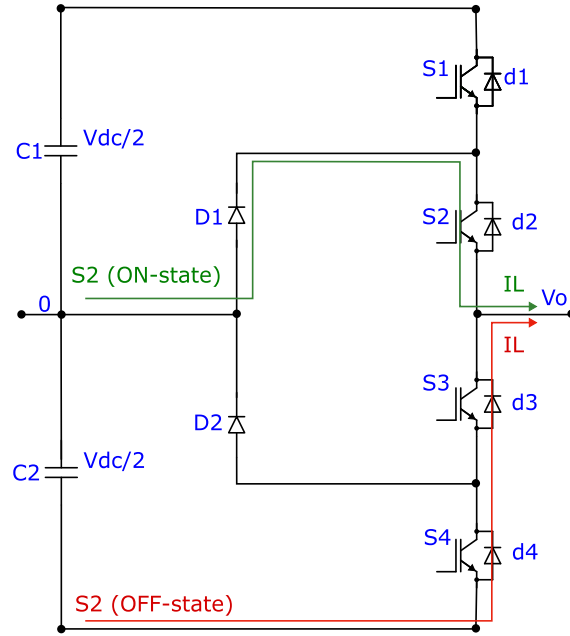
Figure 3-3: 3L-NPC converter operation case# 02

dc-link mid-point and generate $V_o = 0$ and at this stage, both S3 and D2 reverse the current as shown in Fig. 3-4 which is based on the switching states of the power device S4. This is to be known as the small commutation loop because it involves the commutation process with S4, D2, and C2. It must be noted that due to the commutation loop switch, S4 has some off-voltage spike stress because of the stray inductance of the commutation loop.

Case# 04

In this case the output current i.e., $I_L < 0$, and also the output voltage i.e., $V_o \geq 0$. This case is based on the switching transition of the semiconductor device S3 when it is on then the output voltage is zero and current is flowing from the load to the dc-link through S3 and D3. But when the switch S3 is turned off then the current flows through the anti-parallel diodes d1 and d2 and they reverse the current and generate the output voltage of $\left(+\frac{V_{dc}}{2}\right)$ as in Fig. 3-5. This is also called the large commutation loop because it involves the commutation process with S3, D2, d1, d2, and C1. Remember that due to the commutation loop switch, S3 is going to have some off-voltage spike stress because of the stray inductance of the commutation loop.

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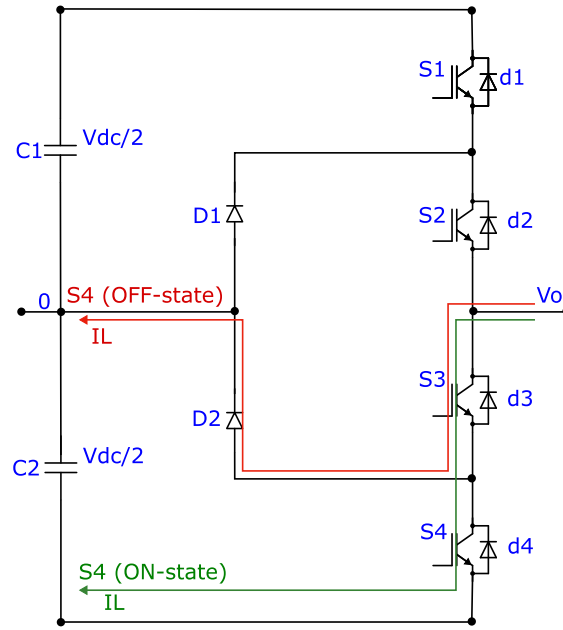
Figure 3-4: 3L-NPC converter operation case# 03
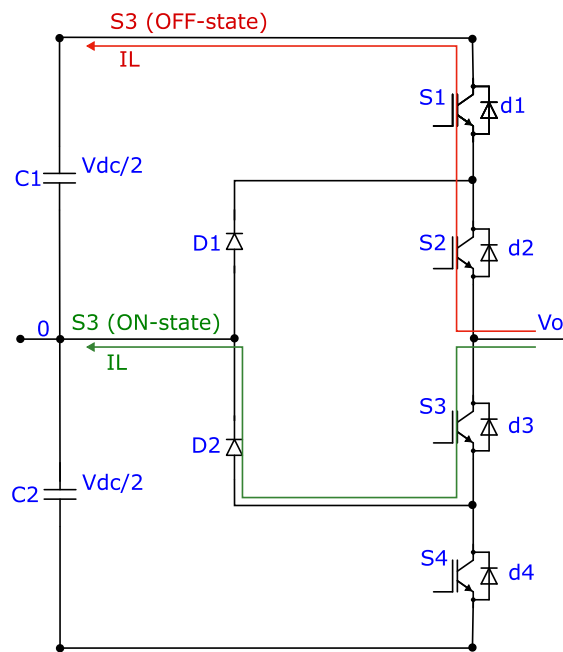
Figure 3-5: 3L-NPC converter operation case# 04

3.1.2 DC-link capacitor sizing for 3L converter

DC-link capacitor sizing is a critical aspect of the power electronic converter design because when the load or input power variations occur then DC-link capacitors ensure the maintained and stabilized voltage across the DC bus. After all, this voltage across the DC bus is affected by the variation of the input power or load. This design is important in power electronic converters because it mitigates the voltage fluctuations which are crucial for the reliable operation of the power electronic devices. Also, it is important here to note for the reliable operation of the power electronic converter that the high-frequency voltage ripples that are caused by the semiconductor switching devices are filtered by the DC-link capacitor. It is worth mentioning here that to reduce the voltage ripple to keep the semiconductor device operation reliable and prevent them from potential damage done by DC-link. This results in the reduction of EMI effects, and improves the overall performance and efficiency of the system. For the sizing of the DC-link capacitor, it is assumed that the converter is operating ideally. This means that the DC-link losses and all the power losses i.e., conduction and switching power losses of the converter are neglected. The DC-link capacitor value can be obtained using equation 3.1 [55].

$$C = \frac{P_L}{(2\pi f) \cdot V_c \cdot \Delta V_{C1}} \tag{3.1}$$

where $V_c = V_{C1_{max}} + V_{C1_{min}}$ in which $V_{C1,max}$ and $V_{C1,min}$ are the maximum and minimum amplitude of the voltage across the capacitor respectively. Also $\Delta V_{C1} = V_{C1_{max}} - V_{C1_{min}}$ is called the voltage ripple across the individual capacitor and can be obtained by differentiating the maximum and minimum value of the voltage across the capacitor. In equation 3.1, the term P_L is called the system power, and f is called the frequency of the output sinusoidal current also it is clear that the voltage ripple across the DC-link capacitor is inversely proportional to the capacitor sizing this shows that higher the capacitor value lower the voltage ripple across the capacitor and vice versa. Table 3.2 represents the calculated value for the DC-link capacitor for the rated power of the 3L-NPC converter and also using the DC-link voltage. In this design of the

	Parameter	Value
DC link Voltage	Vc	1500 V
Output Power	PL	1.5 MVA
Voltage Ripple	Δ Vc	5% of Vc
Frequency of output sinusoidal current	f	50 Hz
DC-link Capacitance	C	85 mF

Table 3.2: 3L-NPC converter design parameters

three-level NPC converter and also for the three-level NPP converter which is going to be explained in the second part of this chapter, the capacitor ripple selected for high-power application is 5% because from the literature it is recommended that for medium DC-link voltage and high-power applications, the voltage ripple should be kept below 8.5% [56]. The value in Table 3.2 for the DC-link capacitance is the equivalent DC-link capacitance value. The value of the DC-link capacitor is 85 mF which is for the design of 1.5 MVA rated power and it must be remembered that based on the available IGBT power modules the design is done for 750 kVA of rated power and for that the DC-link capacitor value that is calculated using equation 3.1 is 42.5 mF. Fig. 3-6, depicts the voltage ripple across the individual DC-link capacitors at a rated output power of 750 kVA, with a modulation index of 1, a power factor of 0.85, and with a calculated capacitance value of 85 mF. The minimum and maximum voltage across individual capacitors lies between 720 V and 780 V respectively.

Analysis of the voltage ripple across DC-link capacitors for 3L-NPC converter

Table 3.3 represents the analysis of the voltage ripple across the individual DC-link capacitors based on the different power factor values and then it is concluded that the voltage ripple across the DC-link capacitors varies w.r.to the load at the output because varying the power factor of the load at the constant input and output apparent power, the current drawn from the AC side has a high reactive component at lower power factor values leads higher peaks in the current waveform results the higher current ripple that causes the voltage ripple to increase at the DC-link capacitors. Table 3.2 shows the parameters for which this analysis is done.
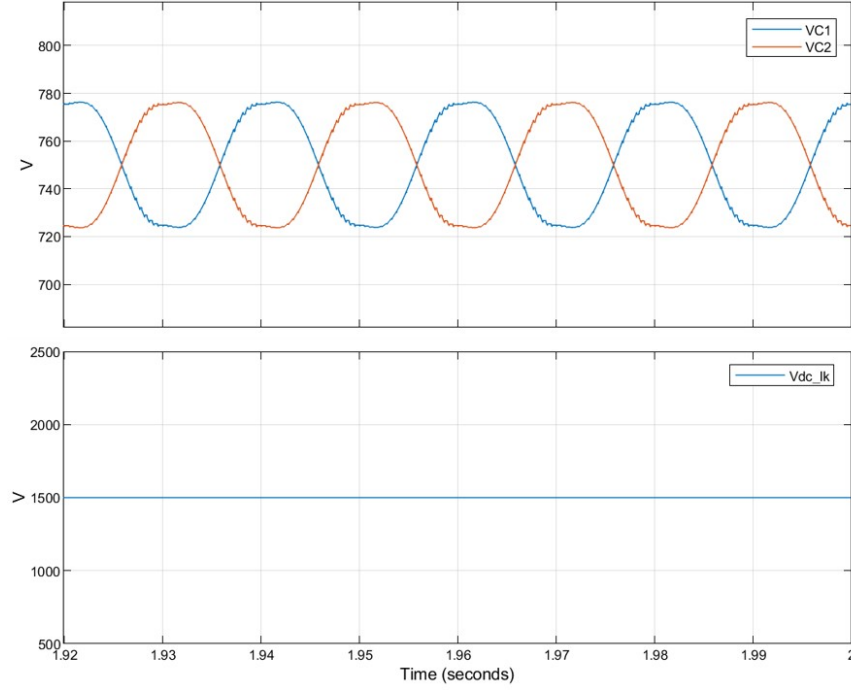
Figure 3-6: Voltage ripple across DC-link capacitors

Type of load	Pf	$\Delta V_{\text{dc-link}}$	ΔV_{c1}	ΔV_{c2}
L	Pf=0	1.086%	10.6%	10.65%
RL	Pf=0.5	1.46%	11.97%	11.98%
RL	Pf=0.85	0.945%	14.4%	14.42%
RL	Pf=0.9	1.28%	15.7%	15.8%
R	Pf=1	1.09%	21%	20.96%

Table 3.3: DC-link capacitor voltage ripple analysis on different Pf

Table 3.4, shows the design of a 3L-NPC on a half-load condition to reduce the rated power from 1.5 MVA to 750 kVA and then the same analysis of the voltage ripple across the DC-link capacitors is done as shown in Table 3.5 and the conclusion could be made that by varying the power factor the voltage ripple across the DC-link capacitor changes and that is consistent with what is analyzed in Table 3.3 of above design analysis.

3.1.3 Phase opposition disposition (POD-PWM) technique

Carrier-based pulse width modulation (CB-PWM) techniques frequently drive MLI topologies. CB-PWM categories into phase-shifted and level-shifted PWM tech-

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	Parameter	Value
DC link Voltage	Vc	1500 V
Output Power	PL	750 kVA
Voltage Ripple	Δ Vc	5% of Vc
Frequency of output sinusoidal current	f	50 Hz
DC-link Capacitance	C	85 mF

Table 3.4: 3L-NPC converter design parameters

Type of load	Pf	$\Delta V_{dc\text{-}link}$	ΔV_{c1}	ΔV_{c2}
L	Pf=0	0.546%	5.25%	5.26%
RL	Pf=0.5	0.51%	5.8%	5.8%
RL	Pf=0.85	0.47%	7.07%	7.09%
RL	Pf=0.9	0.46%	7.3%	7.3%
R	Pf=1	0.429%	10%	10%

Table 3.5: DC-link capacitor voltage ripple analysis on different Pf

niques. The three categories of level-shifted PWM are phase disposition (PD), phase opposition disposition (POD), and alternate phase opposition disposition (APOD) as in Fig. 3-7. Comparing the phase-shifted PWM technique with the level-shifted
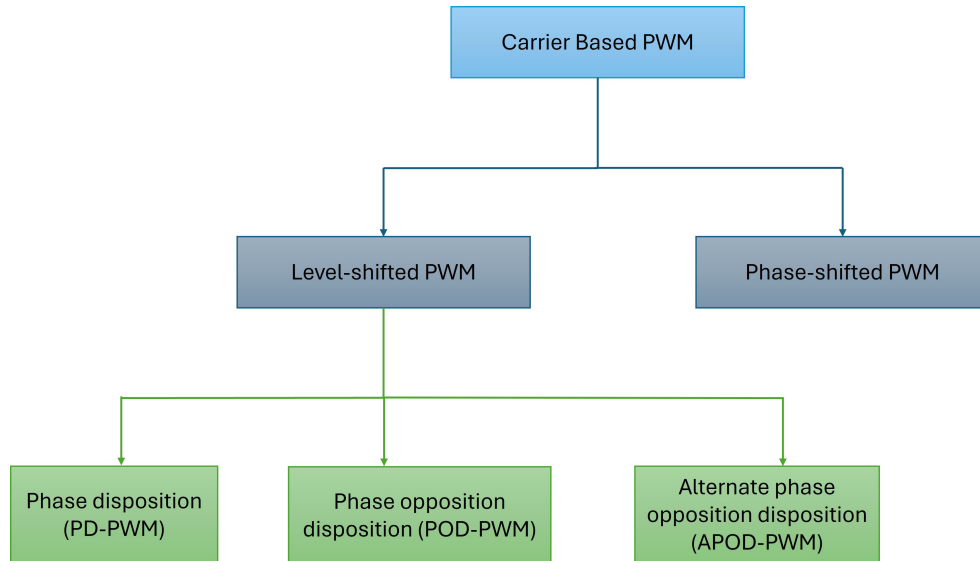
Figure 3-7: Classification of CB-PWM

PWM technique in terms of THD the phase-shifted exhibits more than the level-shifted PWM technique [57]. It is also important to note that the POD-PWM and APOD-PWM techniques for 3-level converters are similar.

In the proposed phase opposition disposition (POD-PWM) technique, two carrier signals $C_1(t)$ and $C_2(t)$ have the same amplitude and frequency. Still, they are phase-shifted by 180 degrees to each other as shown in the following equation 3.2.

$$C_1(t) = A_c \cdot \text{tri}\,(f_c \cdot t),$$
$$C_2(t) = -A_c \cdot \text{tri}\,(f_c \cdot t)$$

(3.2)

where A_c is the amplitude of the carrier signals, f_c is the frequency of the carrier signals, and tri represents the triangular waveform. The reference signal $V_{\text{ref}}(t)$ is a sinusoidal signal that is compared with the carrier signals to generate the commands for the desired output voltage and is shown in equation 3.3.

$$V_{\text{ref}}(t) = A_m \cdot \sin(\omega t)$$

(3.3)

Where: A_m is the amplitude of the reference signal, $\omega = 2\pi f_m$ is the angular frequency of the reference signal, and f_m is the frequency of the reference signal. By using this approach, when both carrier signals are smaller than the reference sinusoidal signal then the output voltage is switched to $\left(+\frac{V_{\text{dc}}}{2}\right)$, whereas when the reference signal is greater than the lower carrier waveform signal then the output voltage level is switched to zero, and it is $\left(-\frac{V_{\text{dc}}}{2}\right)$ when the reference signal is lower than both carriers signals [58]. In this way, the switching signals are generated and the switching states of the single-phase 3-level NPC converter are shown in Table 3.6. and Fig. 3-8, shows this POD-PWM technique that is implemented in MATLAB/Simulink environment to generate the switching signals, and Fig. 3-9, represents the switching signal waveforms using the proposed POD-PWM technique for a single-phase 3L-NPC converter. In the 3L-NPC converter, the neutral point balancing is the main issue to make it stable and balanced the duty cycles of the switches must be carefully selected. The modulation index of the 3L-NPC converter is the ratio of the reference signal (modulating) amplitude with the carrier signal amplitude and is defined as

$$m_a = \frac{A_m}{A_c}$$

(3.4)

Switching States	S1	S2	S3	S4	V_{out}
Positive Level	1	1	0	0	$+\frac{V_{\text{dc}}}{2}$
Neutral Level	0	1	1	0	0
Negative Level	0	0	1	1	$-\frac{V_{\text{dc}}}{2}$

Table 3.6: Switching states and corresponding output voltage for a single-phase 3-Level NPC converter.
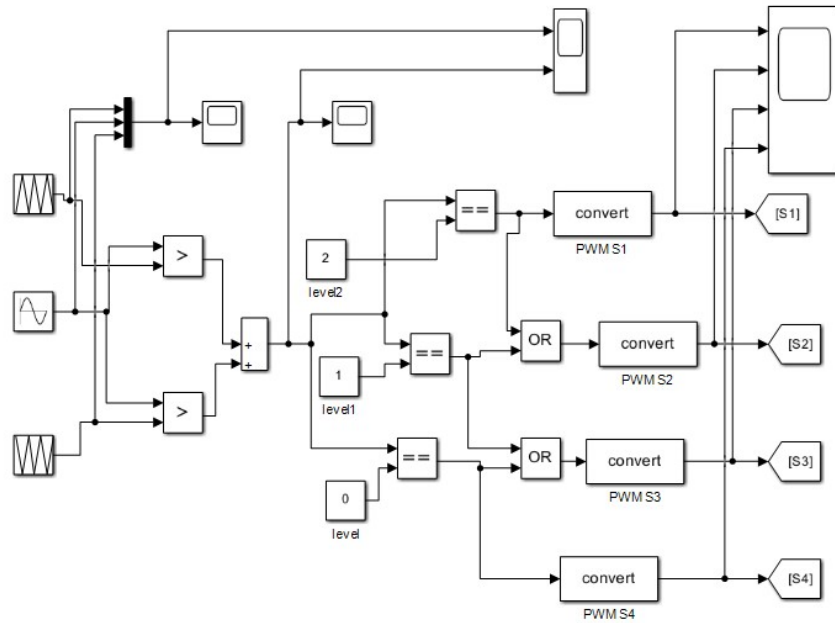
Figure 3-8: Simulink implementation of POD-PWM technique

where A_{m} is the peak amplitude of the reference signal and A_{c} is the peak amplitude of the carrier signal. In terms of the voltage modulation index can also be explained as,

$$m_a = \frac{V_{\text{ref}}}{V_{\text{car}}} \tag{3.5}$$

where V_{ref} is the peak voltage of the reference signal and V_{car} is the peak voltage of the carrier signal.
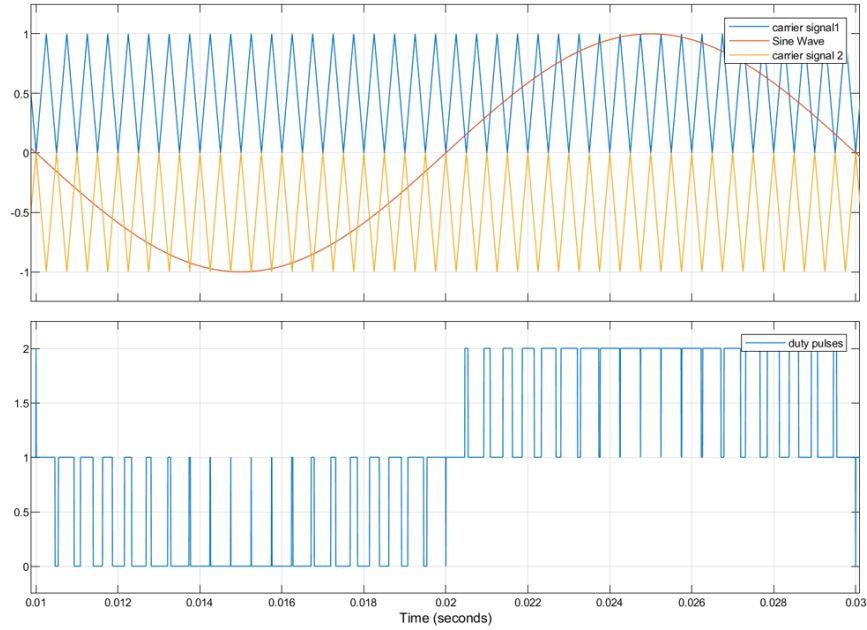
Figure 3-9: Switching signal waveform of single-phase 3L-NPC converter using POD-PWM

3.2 3L-NPP converter

The single-phase 3L-NPP converter topology is shown in Fig. 3-10, including two switches at the top branch S1 and S2 connected in series, and similar is the case for the bottom branch two switches S3 and S4 are connected in series. This topology does not count the clamping diodes and includes two more switches at the neutral point path connecting at the mid-point of the DC-link capacitors and they are connected anti-series to make the bi-directional switch. J. Holtz 1977 [59] had presented this topology and then A. Nabae presented this as the second type of 3L-NPC inverter [60]. The number of electronic components required for the design of the single-phase 3L-NPP converter can be calculated using the expressions in Table 3.7

Semiconductor switches per phase	Flying capacitors	Flying diodes	DC capacitors
2 (n-1)	0	0	(n-1)

Table 3.7: Calculation of power electronic components for 3L-NPC converter

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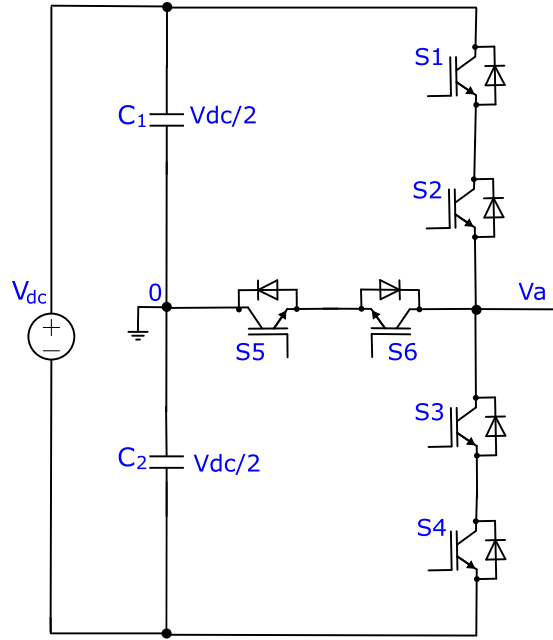
Figure 3-10: Single-phase 3L-NPP converter

3.2.1 Working principle of single-phase 3L-NPP converter

To explain the working principle of the 3L-NPP converter, the direction of the flow of the current is considered, and based on this consideration the operation is explained by the following two cases. It must be noted that the flow of current from the source i.e., from the DC-link to the load is considered positive and vice versa.

Case#1 $I_L > 0$

In this case when the output voltage is $\left(+\frac{V_{dc}}{2}\right)$, and the direction of current is assumed from the source to the load i.e., +ve then switching signals are sent to the S1, S2, and S5. But the current only flows through S1 and S2, there is no current flow through switch S5. In this case, switch S5 is getting the switching signal not for the conduction of the current but only to prepare for turning it on, and in this way switch S5 faces the soft switching that is shown by the green color to the BJT of switch S5 as in Fig. 3-11, and only occurs when the output voltage level changes between $\left(+\frac{V_{dc}}{2}\right)$ and 0. In this mode of operation when switches S1 and S2 are switched off, then the current only flows from switch S5 and anti-parallel diode d6 of switch S6 and this
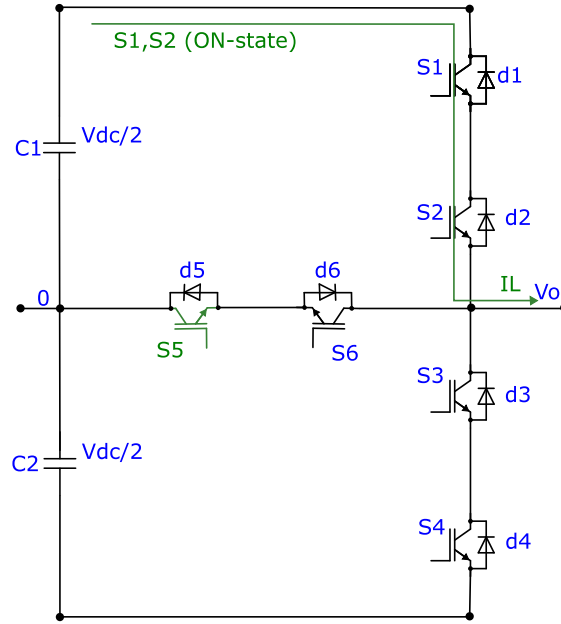
Figure 3-11: Positive voltage mode operation in case# 01

mode generates the output voltage of zero as in Fig. 3-12. So, in this mode, the bi-directional switch starts leading the current toward the load, and do not forget that the whole commutation takes place at the anti-parallel diode d6 of switch S6. There is no switching loss occurring at S5 at this moment of operation. When the
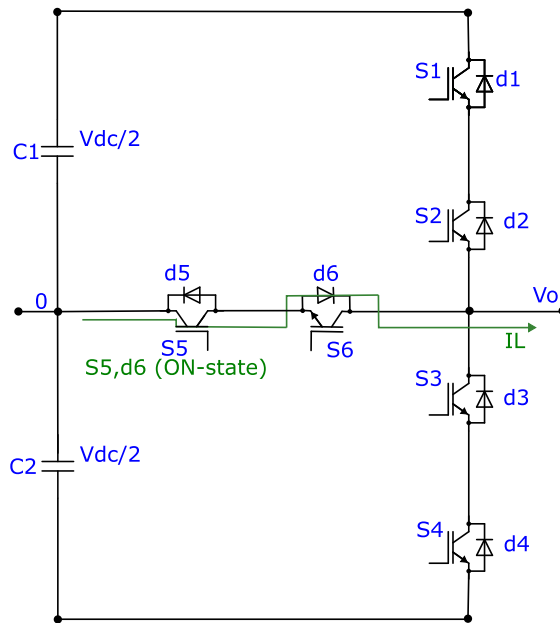
Figure 3-12: Zero-voltage mode of operation in case# 01

output voltage is $\left(-\frac{V_{dc}}{2}\right)$, this means that now the current is flowing from the anti-parallel diodes d3 and d4, and all the switches are turned off during this mode of operation as in Fig. 3-13. It should be noted that during this phase of operation, soft switching does not exist. It is worth mentioning here that during this operation the blocking voltage of each switch is $\left(\frac{V_{dc}}{2}\right)$ but the switching voltage is reduced to $\left(-\frac{V_{dc}}{4}\right)$ as shown in Table 3.8, and the soft switching only occurred when the output voltage was $\left(+\frac{V_{dc}}{2}\right)$ as shown in Table 3.9.
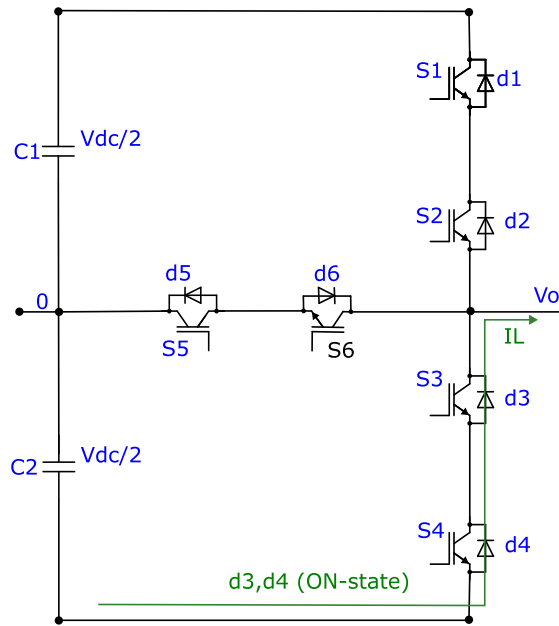
Figure 3-13: Negative voltage operation mode in case# 01

Case# 02 $I_L < 0$

In this mode, it is assumed that when the direction of the current is from the load to the source i.e., DC-link, it is assumed negative. When the output voltage in this mode of operation is $\left(+\frac{V_{dc}}{2}\right)$ then no switching signals are received by the power switches and they remain turned off and the current flows through the top branch anti-parallel diodes i.e., d1 and d2 of switches S1 and S2 as in Fig. 3-14. When the output voltage is $\left(-\frac{V_{dc}}{2}\right)$, then the switches S3 and S4 are turned on by providing the switching signals. In this mode, the switch S6 is going to see the soft switching because the switching signal is also sent to this switch as well, and no current flows through this
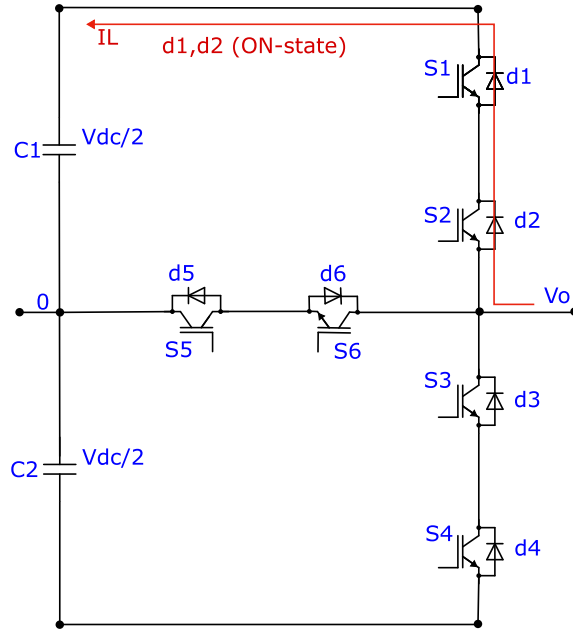
Figure 3-14: Positive voltage operation mode in case# 02

switch. The switch S6 provided the signal only to get ready to conduct in the next switching phase as in Fig. 3-15, and this is only possible when the output voltage changes between the level $\left(-\frac{V_{dc}}{2}\right)$ and 0. When the zero-voltage occurs at the output
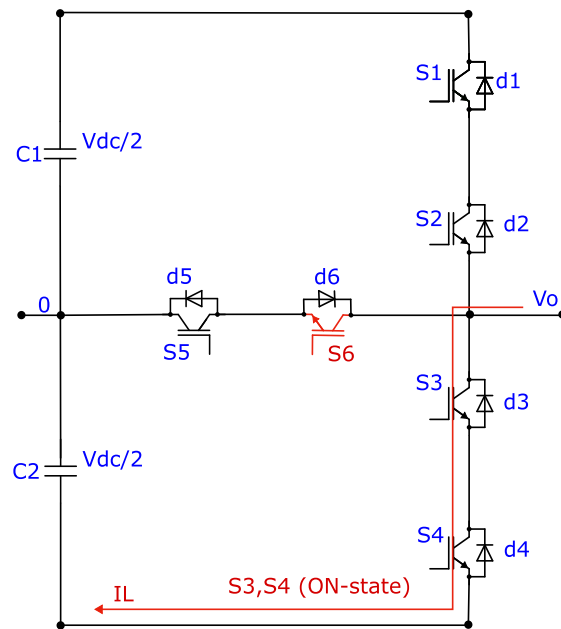
Figure 3-15: Negative voltage mode of operation in case# 02

side then the current is going to flow from switch S6 and anti-parallel diode d5. In this case, the whole commutation occurs at the d5. The switching losses of switch S6 do not exist because of the soft switching and this switch was triggered before this mode of operation as in Fig. 3-16. It must be noted that during this operation the
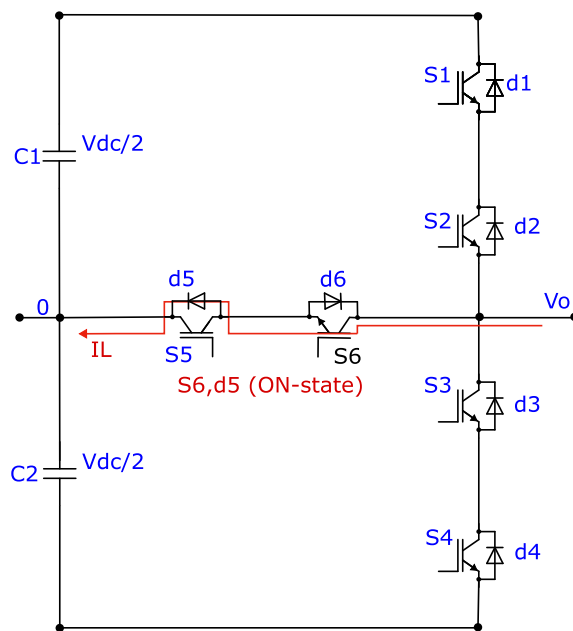
Figure 3-16: Zero-voltage mode operation in case# 02

blocking voltage of each switch is $\left(\frac{V_{dc}}{2}\right)$ but the switching voltage is reduced to $\left(\frac{V_{dc}}{4}\right)$ as shown in Table 3.8 and the soft switching only occurred when the output voltage was $\left(+\frac{V_{dc}}{2}\right)$ and their cases are shown in Table 3.9.

Semiconductor switch	Blocking voltage	Switching voltage
S1	Vdc/2	Vdc/4
S2	Vdc/2	Vdc/4
S3	Vdc/2	Vdc/4
S4	Vdc/2	Vdc/4
S5	Vdc/2	Vdc/2
S6	Vdc/2	Vdc/2

Table 3.8: Blocking and switching voltage of switches in 3L-NPP converter

It is concluded that the bi-directional switch is made at the neutral point to use in soft switching for some of the cases of operation and it depends upon the operating

Operation modes of 3L-NPP	Current direction	Soft switched switches
$\frac{V_{DC}}{2} \leftrightarrow 0$	$I_L > 0$	S5
$\frac{-V_{DC}}{2} \leftrightarrow 0$	$I_L > 0$	does not exist
$\frac{V_{DC}}{2} \leftrightarrow 0$	$I_L < 0$	does not exist
$\frac{-V_{DC}}{2} \leftrightarrow 0$	$I_L < 0$	S6

Table 3.9: Soft switching cases in 3L-NPP converter

mode of the 3L-NPP converter that leads to the switching states of the converter and can be seen in Table 3.10.

V_{out} level		+Vdc/2	0	-Vdc/2
Switching sequence		S1, S2, S5	S5, S6	S3, S4, S6
Current orientation	$I_L > 0$	S1, S2	S5, d6	d3, d4
	$I_L < 0$	d1, d2	d5, S6	S3, S4

Table 3.10: Switching states of single-phase 3L-NPP converter

3.2.2 DC-link capacitor sizing

For the DC-link capacitor sizing for the 3L-NPP converter, the same procedure of the calculation of the DC-link capacitor is utilized as it was done in section 3.1.2 and the same values are used as well. Fig. 3-17, depicts the voltage ripple across the individual DC-link capacitors at a rated output power of 750 kVA, with a modulation index of 1, a power factor of 0.85, and a calculated capacitance value of 85 mF. The minimum and maximum voltage across individual capacitors lies between 720 V and 780 V respectively.

Analysis of the voltage ripple across DC-link capacitor for 3L-NPP converter

Table 3.11 represents the analysis of the voltage ripple across the individual DC-link capacitors based on the different power factor values and then it is concluded that the voltage ripple across the DC-link capacitors varies w.r.to the load at the output because varying the power factor of the load at the constant input and output apparent power, the current drawn from the AC side has a high reactive component
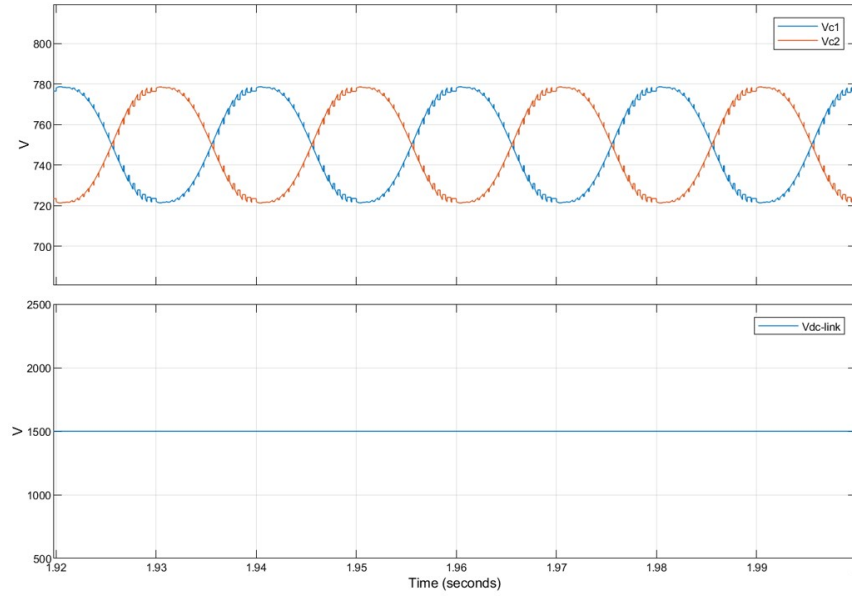
Figure 3-17: Voltage ripple across DC-link capacitors

at lower power factor values leads higher peaks in the current waveform results in the higher current ripple that causes the voltage ripple to increase at the DC-link capacitors. Table 3.2 shows the parameters for which this analysis is done. From

Type of load	pf	$\Delta V_{dc\text{-}link}$	ΔV_{c1}	ΔV_{c2}
L	Pf=0	2.67%	18.1%	18%
RL	Pf=0.5	2.22%	16.9%	16.87%
RL	Pf=0.85	1.78%	16.59%	16.58%
RL	Pf=0.9	1.65%	16.2%	16.29%
R	Pf=1	1.35%	19.9%	19.9%

Table 3.11: DC-link capacitor voltage ripple analysis on different Pf

Table 3.11, it can be seen that as the power factor increases from 0 to 1, at every step the voltage ripple across the equivalent DC-link decreases which is consistent that at higher power factor the voltage ripple decreases but across the individual capacitors it is also consistent except for the one case where the active power at the input and output side changes because that reason it has some variation when the power factor is changed from 0.9 to 1 and the ripple across the individual DC-link capacitors increase but it should be noted that the input and output apparent power is same. Table 3.12, shows another analysis for Table 3.4, design parameters that are

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considered for the 3L-NPP topology as well.

Type of load	Pf	$\Delta V_{dc\text{-link}}$	ΔV_{c1}	ΔV_{c2}
L	Pf=0	1.29%	8.79%	8.81%
RL	Pf=0.5	1.16%	8.6%	8.6%
RL	Pf=0.85	0.83%	8.1%	8.1%
RL	Pf=0.9	0.78%	7.8%	7.8%
R	Pf=1	0.68%	10.1%	10.1%

Table 3.12: Voltage variation for different load types and power factors

3.2.3 Sinusoidal (SPWM) technique

The sinusoidal pulse width modulation technique is one of the well-known PWM techniques in power electronic converters. In this PWM technique, the reference voltage waveform is compared with the triangular carrier waveform to generate the gate signals of the converter. Fig. 3-18 shows the PWM1 for the top leg series-connected two switches, and PWM2 for the bottom leg series-connected two switches with a duty ratio of 0.5. and Fig. 3-19, shows the implementation of the technique in MATLAB/Simulink software.
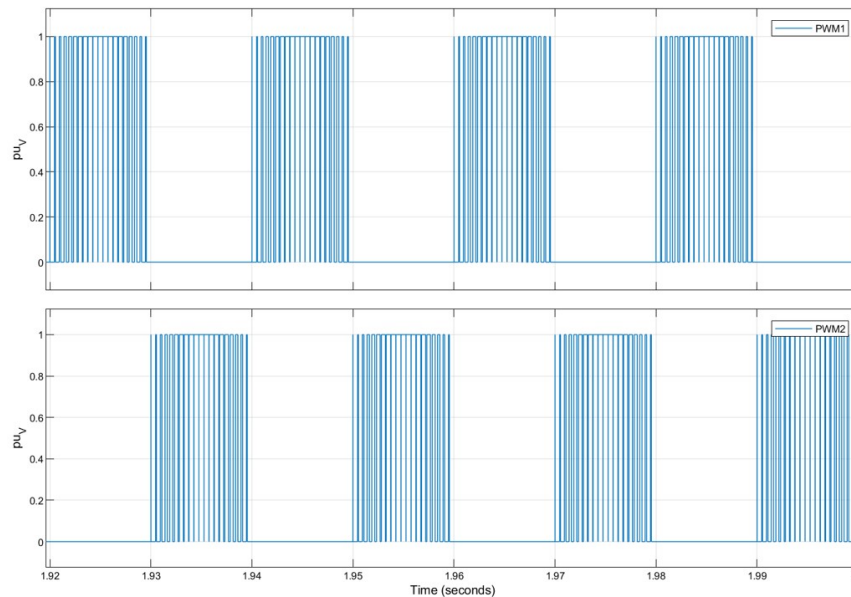
Figure 3-18: PWM signals for switches S1-S4
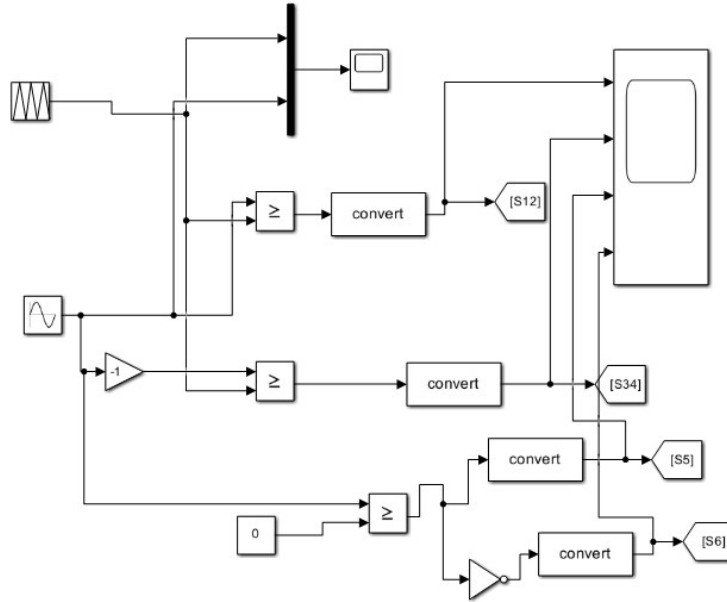
Figure 3-19: SPWM technique implementation in MATLAB/Simulink

3.3 Comparison between 3L-NPC and 3L-NPP converter

The comparative analysis of the 3L-NPC converter and 3L-NPP converter is done based on the average power losses and efficiency to decide which converter is going to be more beneficial for this particular design of a high-voltage high-current power stack.

3.3.1 Power loss analysis of 3L-NPC converter

The power losses in a converter are categorized into switching losses and conduction losses of the semiconductors that are used for the design of the converter.

Switching losses

The energy lost during the transition i.e., turn-on and turn-off transitions of power IGBTs and the switching frequency are the main reasons for switching loss occurrence. The switching frequency, DC bus voltage, collector current, and gate resistance are the related sources of these power losses. Fig. 3-20 [61], shows that the voltage and

current crossing are the points where switching losses take place. The switching losses of the IGBTs are calculated by using equation 3.6.

$$P_{\text{sw}} = (E_{\text{on}} + E_{\text{off}}) \cdot f_{\text{sw}} \tag{3.6}$$

where E_{on} is the energy lost of the IGBT when it is turning on i.e., start conducting, and E_{off} is the energy lost when it is turned off and f_{sw} is called the switching frequency. The reverse recovery effect is the cause of the diode switching losses and can be
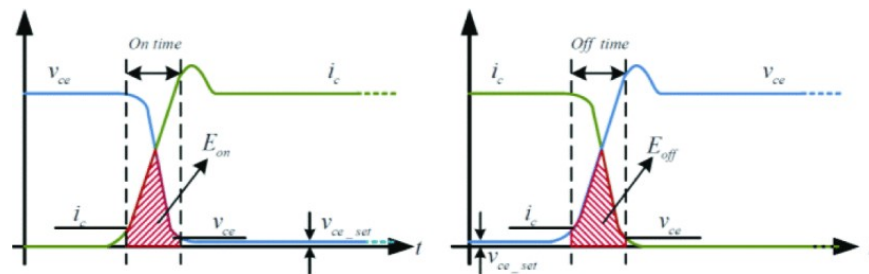
Figure 3-20: Turn-on and turn-off switching losses [61]

calculated using equation 3.7. These power switching losses depend upon the DC bus voltage, switching frequency, and current through the diode.

$$P_{\text{sw}} = E_{\text{rr}} \cdot f_{\text{sw}} \tag{3.7}$$

where E_{rr} is called the reverse recovery energy of the diode. The E_{on}, E_{off}, and E_{rr} can be directly obtained from the datasheet of the corresponding components.

Conduction losses

The conduction losses in the IGBT are associated with the forward voltage drop i.e., V_{CE}, and the collector current through the IGBT. It is produced when the power device starts conducting the current. The formula used to calculate the average power losses through the IGBTs and the diodes is represented by equation 3.8.

$$P_{CON} = (V_d \cdot I_{ak}) + (R_{on} \cdot I^2_{RMS}) \tag{3.8}$$

where V_d = Forward voltage drop at zero current across IGBTs and diodes, I_{ak} = average current through IGBTs and diodes, R_{on} = on-state resistance of IGBTs and diodes, I_{RMS} = root mean square value of current through IGBTs and diodes. The forward voltage drop and the on-state resistance of the power devices can be obtained from the datasheet directly but the average current through the IGBT and the anti-parallel diodes must be analytically calculated. The power loss analysis is done by two methods i.e., the analytical method and the simulation method. To, calculate the average I_a and RMS current of switches S1 and S4 can be calculated using equation 3.9 [62, 63].

$$I_{aS1} = I_{aS4} = \frac{\sqrt{2} \cdot m \cdot I_{rms}}{4 \cdot \pi} \left[\sin(\theta) + (\pi - \theta) \cdot \cos(\theta)\right]$$

$$I_{RMSS1} = I_{RMSS4} = I_{rms} \sqrt{\frac{m}{3 \cdot \pi}} \left[\cos\theta + 1\right]$$

$$(3.9)$$

Both the IGBTs have the same current formula this is due to because both switches get the switching signals once in the whole period, conduct half the period, and remain off during the other half of the period. The average (I_a) and RMS currents through the power switch S2 and S3 can be calculated using equation 3.10 [62, 63].

$$I_{aS2} = I_{aS3} = -\frac{\sqrt{2} \cdot I_{rms}}{4 \cdot \pi} \left[m \cdot (\sin(\theta) - \theta \cdot \cos(\theta) - 4\right]$$

$$I_{RMSS2} = I_{RMSS3} = \frac{\sqrt{2}I_{rms}}{2} \sqrt{1 + \frac{2m}{3\pi} \left(2\cos\theta - \cos^2\theta - 1\right)}$$

$$(3.10)$$

Similarly, the average I_a and RMS currents through the anti-parallel diodes of these four IGBT switches can be found using equation 3.11 [62, 63].

$$I_{ad1,ad2} = I_{ad3,ad4} = \frac{m \cdot I_{rms}}{4 \cdot \pi} \left[(\sin(\theta) - \theta \cdot \cos(\theta)\right]$$

$$I_{RMSd1,d2} = I_{RMSd3,d4} = I_{rms} \sqrt{\frac{m}{3 \cdot \pi}} \left[1 - \cos\theta\right]$$

$$(3.11)$$

Also, the average I_a and RMS current through the clamping diodes in the 3L-NPC converter can be determined by using equation 3.12 [62,63].

$$I_{aD1} = I_{aD2} = \frac{\sqrt{2} \times I_{rms}}{2\pi} \left[m \cdot (\theta - \frac{\pi}{2}) \cdot \cos\theta - m \cdot \sin\theta + 2 \right]$$

$$I_{RMSD1} = I_{RMSD2} = \frac{\sqrt{2} \times I_{rms}}{2} \sqrt{1 - \frac{4m}{3\pi}(\cos^2\theta + 1)} \tag{3.12}$$

In equations from (3.9) to (3.12), m is the modulation index, I_{RMS} is the output RMS current that can be calculated using $S = V_{\mathrm{rms}} \times I_{\mathrm{rms}}$, and θ is the power factor angle. Table 3.13, shows all the design parameters that are used to calculate the currents analytically, and also these parameters are used in MATLAB/Simscape library to compare the analytical values of currents through power IGBTs and their anti-parallel diodes with the simulated results as Simscape library provides more physical values as compared to Simulink and same models of the power IGBTs are used.

Parameter	Values
DC-link voltage ($V_{\text{dc-link}}$)	1500 Vdc
Rated power (S)	750 kVA
DC-link capacitance (C)	85 mF
Switching (carrier) frequency (f_{sw})	2 kHz
Load frequency (f)	50 Hz
Load impedance (Z)	375 mΩ
Power factor (Pf)	0.85
Modulation index (m)	1

Table 3.13: Design parameters

Table 3.14, represents the IGBT parameters, anti-parallel diode of the IGBT inserted inside the IGBT module taken from [64] and also clamping diode parameters used for the simulation and analytical loss calculation purpose taken from [65]. These parameters are used for simulation and analytical loss calculation. It must be noted that for the power loss analysis and simulation, all the parameters are taken at a high-temperature operation of the devices to ensure that the design is robust, reliable, and safe under the worst operating conditions. Using the data from Table 3.14, the analytically calculated average I_{avg} and RMS I_{RMS} currents of the IGBTs, anti-parallel diodes of IGBTs, and clamping diodes using equations from 3.9-3.12 and calculated

Parameter	Value
Forward voltage drop of IGBT at $T_{vj} = 125°C$	2.05 V
On-state resistance of IGBT R_{on}	$1\,m\Omega$
Forward voltage drop of anti-parallel diode at $T_{vj} = 125°C$	1.85 V
On-state resistance of anti-parallel diode R_{on}	$0.446\,m\Omega$
Turn-on energy loss per pulse of IGBT E_{on} at $T_{vj} = 125°C$	80 mJ
Turn-off energy loss per pulse of IGBT E_{off} at $T_{vj} = 125°C$	280 mJ
Reverse recovery energy loss per pulse of the anti-parallel diode at $T_{vj} = 125°C$	110 mJ
Forward voltage drop of clamping diode at $T_{vj} = 125°C$	2.08 V
On-state resistance of clamping diode R_{on}	$0.5\,m\Omega$
Reverse recovery energy loss per pulse of clamping diode at $T_{vj} = 125°C$	104 mJ

Table 3.14: IGBT and anti-parallel diode parameters

values are shown in Table 3.15 and also depicts the average and RMS values of currents that are taken from the simulation results whose waveforms can be shown below as well. It must be noted that during this analysis DC-link is not considered because DC-link capacitors have very low parasitic series resistance value which does not impact a lot on the overall losses of the converter so it is neglected during this analysis. The average power losses per pulse for the IGBTs, anti-parallel diodes of the

Calculation method	IGBT S1, S4	IGBT S2, S3	Anti-parallel diodes d1-d4	Clamping diodes D1, D2
Analytical method	$I_{avg} = 433.9$ A $I_{rms} = 852.3$ A	$I_{avg} = 627.9$ A $I_{rms} = 995.9$ A	$I_{avg} = 6.205$ A $I_{rms} = 69.02$ A	$I_{avg} = 194.8$ A $I_{rms} = 518.6$ A
Simulation method	$I_{avg} = 431.3$ A $I_{rms} = 859.5$ A	$I_{avg} = 621.1$ A $I_{rms} = 998.9$ A	$I_{avg} = 7.37$ A $I_{rms} = 63.55$ A	$I_{avg} = 184.8$ A $I_{rms} = 522.2$ A

Table 3.15: Analytical and simulated current values of devices

IGBTs, and also for the clamping diodes are analytically calculated using equations 3.6 and 3.7 for switching losses of IGBTs and diodes both clamping and anti-parallel respectively. Equation 3.8 is used to find the average conduction losses of the IGBTs, anti-parallel diodes, and clamping diodes. The average power losses both switching and conduction are calculated analytically using the data in Table 3.13, 3.14, and 3.15 respectively, and are expressed in Table 3.16. It must be noted that the values in Table 3.16 are multiplied by 2 or by 4 this is because of the number of devices used

in the analysis and having the same losses.

Power losses	IGBT S1, S4	IGBT S2, S3	d1, d2, d3, d4	D1, D2
Conduction losses	1.616×2 kW	2.285×2 kW	0.0133×4 kW	0.539×2 kW
Switching losses	0.72×2 kW	0.72×2 kW	0.22×4 kW	0.208×2 kW

Table 3.16: Analytical calculation of average power losses of devices

Table 3.17, shows the simulation results of the average power losses including only the conduction losses that are calculated by using the product of voltage times current $P = V \times I$ through each of the IGBT, anti-parallel diodes of each of the IGBT, and clamping diode. The switching losses are not considered in the simulation of the single-phase 3L-NPC converter. Remember that the simulation of the 3L-NPC converter is done in MATLAB/Simscape platform to analyze the results close to real values because in this simulation real models of the devices are used and average values of conduction power losses are taken over a one-cycle of load frequency using mean value from signal statistics. The design parameters for the simulation are used in Table 3.13.

Power losses	IGBT S1, S4	IGBT S2, S3	d1, d2, d3, d4	D1, D2
Conduction losses	1.642×2 kW	2.292×2 kW	0.01908×4 kW	0.53×2 kW

Table 3.17: Simulation results of average power losses of devices

Fig. 3-21, shows the simulation block diagram of a single-phase 3L-NPC converter in a MATLAB/Simscape environment. Fig. 3-22, and 3-23, show the current, voltage, and conduction power loss waveform of the BJT of the S1 and S2 switches used in the simulation of the 3L-NPC converter in the Simscape environment, and the waveform for the S3 and S4 switches are also analyzed in the same way.

Fig. 3-24 and 3-25, show the current, voltage, and power loss waveform of the anti-parallel diode of the IGBT S1, and S2 respectively. In the waveforms, the blocking voltage across the anti-parallel diode can be seen as negative this is because the
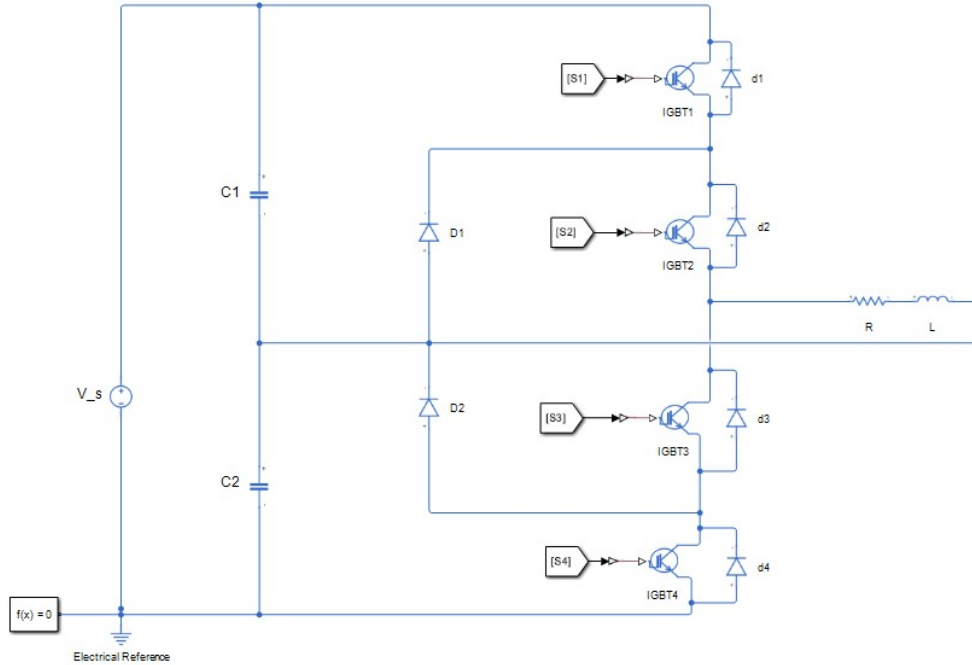
Figure 3-21: Single-phase 3L-NPC converter Simscape simulation diagram
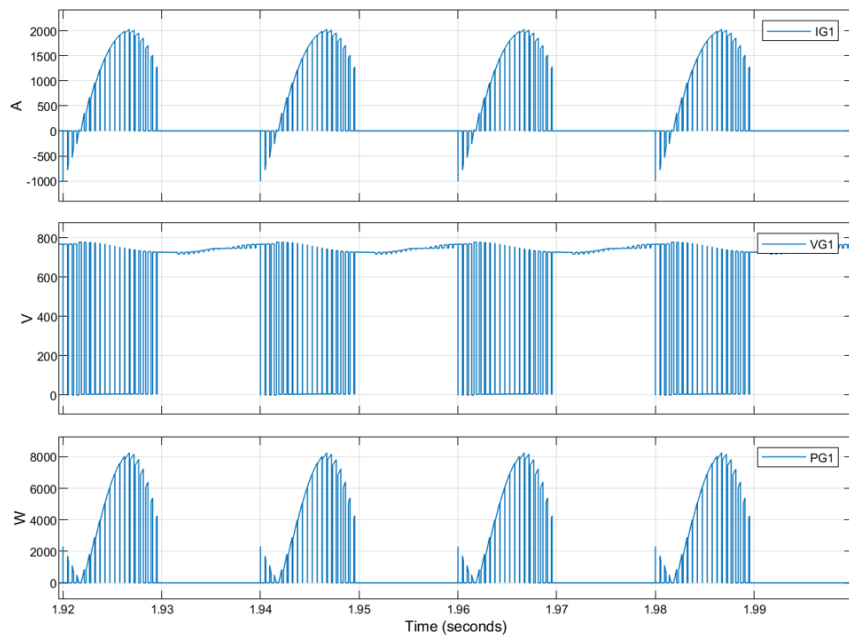
Figure 3-22: V/I/P waveform results of IGBT1

anti-parallel diode conducts when the current flows from the load to the DC-link, it can be seen as positive by changing the connections of the voltage sensor across the anti-parallel diode. This power loss here is the product of the forward voltage drop
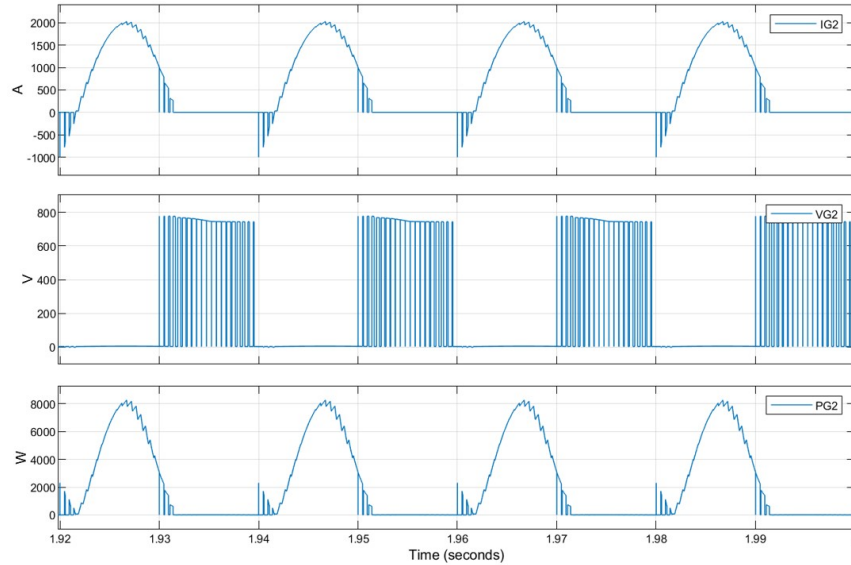
Figure 3-23: V/I/P waveform results of IGBT2

across the anti-parallel diode and the current flowing through it, the forward voltage drop across the anti-parallel is positive and the current is also flowing in the opposite direction but the sensor is connected in a way to show the current as positive then the product of both these forward voltage drop and current is seen as positive as in given figures. The same procedure can be applied for the anti-parallel diode d3 and d4 and it must be noted that d3 has the same power losses as d2 and d4 has the same as d1.   Fig. 3-26, shows the current, voltage, and power loss waveforms of the clamping diode (D1). Remember that the same procedure can be applied for the second clamping diode and both have the same power losses.

Fig. 3-27, shows the output waveforms of the current, voltage, and power (denoted by P in waveforms). The output voltage has three levels $\left(+\frac{V_{dc}}{2}\right)$, 0, and $\left(-\frac{V_{dc}}{2}\right)$, and can be seen from the waveform. The output current is sinusoidal because of the RL load and the inductor smooths the output current waveform.

3.3.2   Power loss analysis of 3L-NPP converter

For the power loss analysis of a single-phase 3L-NPC converter, the data of the devices that were used in the previous subsection of power loss analysis of the 3L-
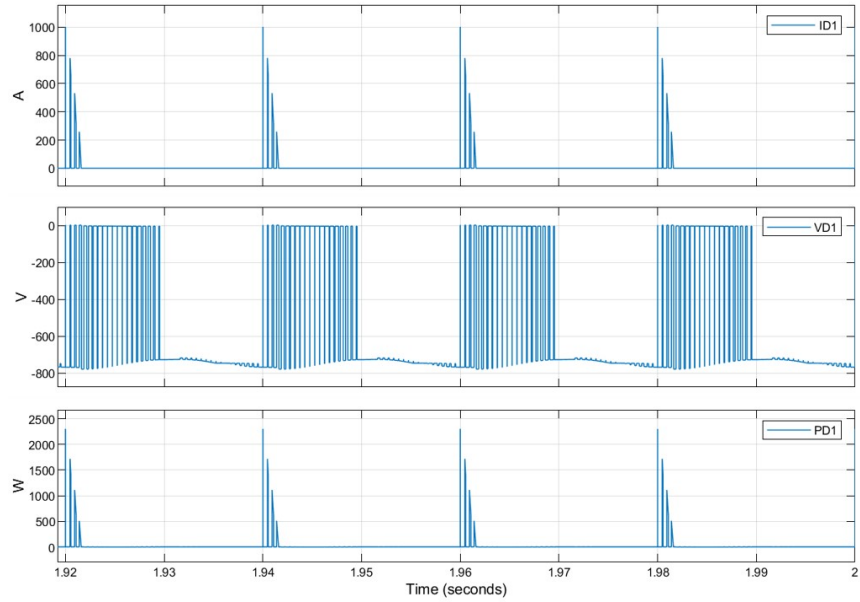
Figure 3-24: V/I/P waveform results of anti-parallel diode d1
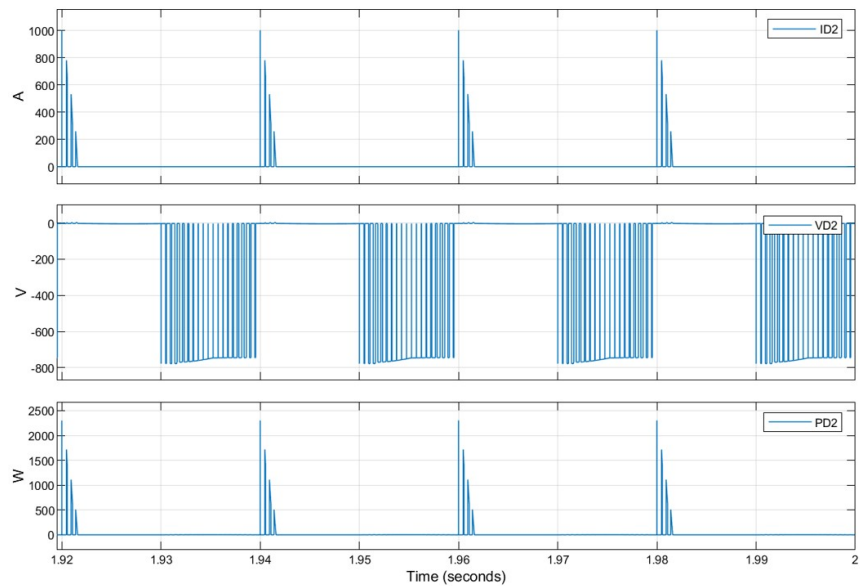
Figure 3-25: V/I/P waveform results of anti-parallel diode d2

NPC converter is the same. For the switching and conduction losses equations 3.6, 3.7, and 3.8 are going to be used respectively. The assumptions used for the analysis of the 3L-NPC converter are the same as for the analysis of the 3L-NPP converter as well. The DC-link capacitor losses are neglected and switching losses in the simulation are also neglected as were done in the analysis of the 3L-NPC converter. Although the
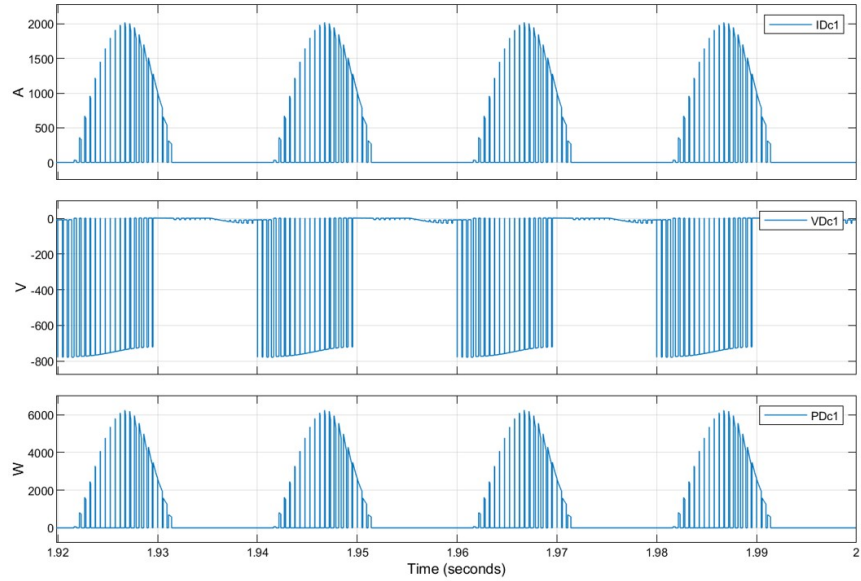
Figure 3-26: V/I/P waveform results of clamping diode Dc1
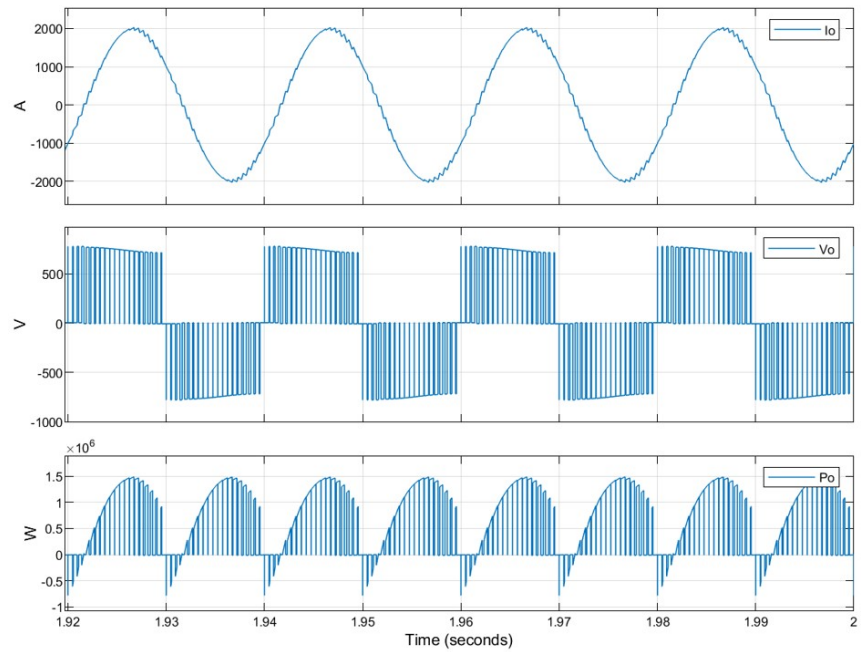
Figure 3-27: Output current, voltage, and power waveform

average I_a and RMS currents of the devices that are going to be calculated by using the given formulas as the topology and switching technique are different, the expressions for calculation are also going to be different. The average I_a and RMS current of the

switches S1, S2, S3, and S4 can be calculated by using equation 3.13 [62, 63].

$$I_{aS1,aS2} = I_{aS3,aS4} = \frac{\sqrt{2} \cdot m \cdot I_{rms}}{4 \cdot \pi} \left[(\pi - \theta) \cdot \cos(\theta) + sin(\theta) \right]$$

$$I_{\text{RMS S1, S2}} = I_{\text{RMS S3, S4}} = \sqrt{2} \cdot I_{\text{RMS}} \cdot \sqrt{\frac{m}{6 \cdot \pi}} \cdot [\cos(\theta) + 1] \tag{3.13}$$

Equation 3.14, will be used to calculate the average I_a and RMS currents through the anti-parallel diodes of IGBT S1-S4 [62, 63].

$$I_{ad1,ad2} = I_{ad3,ad4} = \frac{\sqrt{2} \cdot m \cdot I_{rms}}{4 \cdot \pi} \left[(\sin(\theta) - \theta \cdot \cos(\theta) \right]$$

$$I_{RMSd1,d2} = I_{RMSd3,d4} = \sqrt{2} \cdot I_{RMS} \cdot \sqrt{\frac{m}{6 \cdot \pi}} (1 - cos(\theta)) \tag{3.14}$$

Equation 3.15, will be used to calculate the average I_a and RMS currents through the anti-series IGBTs i.e., S5 and S6, and also through their anti-parallel diodes i.e., d5 and d6 [62, 63].

$$I_{aS5,ad5} = I_{aS6,ad6} = \frac{\sqrt{2} \cdot I_{\text{rms}}}{4\pi} \left[(2\theta - \pi) \cdot m \cdot \cos\theta - 2 \cdot m \cdot \sin\theta + 4 \right]$$

$$I_{\text{RMSS5,d5}} = I_{\text{RMSS6,d6}} = \frac{\sqrt{2} \cdot I_{\text{rms}}}{2} \sqrt{1 - \frac{4m}{3\pi} (\cos^2\theta + 1)} \tag{3.15}$$

The design parameters in Table 3.13 and the parameters of the IGBTs and their anti-parallel diodes are taken from Table 3.14 and then average and RMS currents are calculated analytically. The MATLAB/Simscape platform is used to simulate the single-phase 3L-NPP converter as in Fig. 3-28. The average values of current are taken over the one-cycle of load frequency using the mean value from the signal statistics and the same is done for the RMS values from the simulation.

 The average power losses per switch of the IGBTs and their anti-parallel diodes are calculated analytically and are shown in Table 3.19. The switching losses are calculated using equations 3.6 and 3.7, and the average conduction losses are calculated using equation 3.8. It is again reminded here that in the table some values are mul-

Calculation method	IGBTs S1, S2 S3, S4	Anti-parallel diodes d1-d4	Anti-series IGBTs S5, S6	Anti-parallel diodes d5, d6 of anti-series IGBTs S5 , S6
Analytical method	$I_{avg} = 433.9$ A $I_{rms} = 852.3$ A	$I_{avg} = 8.8$ A $I_{rms} = 69$ A	$I_{avg} = 194$ A $I_{rms} = 518.7$ A	$I_{avg} = 194$ A $I_{rms} = 518.7$ A
Simulation method	$I_{avg} = 441.1$ A $I_{rms} = 891.5$ A	$I_{avg} = 15.1$ A $I_{rms} = 102.8$ A	$I_{avg} = 165.4$ A $I_{rms} = 488.1$ A	$I_{avg} = 165.4$ A $I_{rms} = 488.1$ A

Table 3.18: Analytical and simulated current values of devices
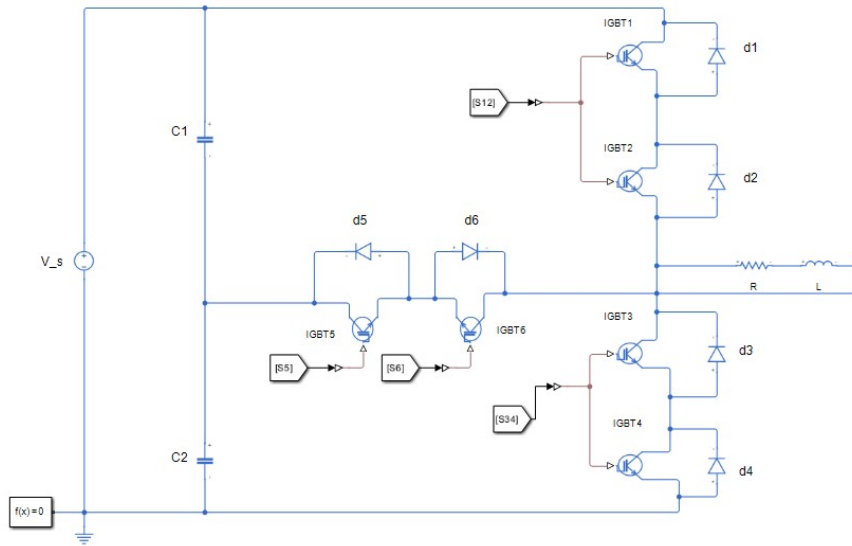
Figure 3-28: Single-phase 3L-NPP converter simulation diagram

tiplied by two or some by four this shows the number of devices used in the design.

Power losses	IGBT S1, S2 S3, S4	IGBT S5, S6	Anti-parallel diodes d1, d2 d3, d4	Anti-parallel diodes d5, d6 of anti-series IGBTs S5, S6
Conduction losses	1.6159×4 kW	0.6667×2 kW	0.0184×4 kW	0.479×2 kW
Switching losses	0.72×4 kW	0.72×2 kW	0.22×4 kW	0.22×2 kW

Table 3.19: Analytical calculation of average power losses of devices

Table 3.20, represents the average conduction power losses depicted from the simulation of a single-phase 3L-NPP converter that is performed in the MATLAB/Simscape environment. It is also assumed here that switching losses are not considered during

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the simulation analysis and average conduction power losses are taken over a one-cycle load frequency using mean values from the signal statistics. The design parameters were used from Table 3.13 for the simulation of a single-phase 3L-NPP converter.

Power losses	IGBT S1, S2 S3, S4	IGBT S5, S6	Anti-parallel diodes d1, d2 d3, d4	Anti-parallel diodes d5, d6 of anti-series IGBTs S5, S6
Conduction losses	1.789×4 kW	0.9905×2 kW	0.03785×4 kW	0.441×2 kW

Table 3.20: Simulation results of average power losses of devices

The waveform results of the simulation of a single-phase 3L-NPP converter are shown in the below figures. It must be noted that the same method of calculation is used for the average conduction power losses for the switches and their anti-parallel diodes as it was done in the case of a single-phase 3L-NPC converter. Fig. 3-29 and 3-30, show the current, voltage, and average conduction power losses of the switches S1 and S3 respectively because switches S1 and S2 are connected in series so the voltage drop they share between each other, and the same is for switches S3 and S4 and the same method can be applied for the results of S2 and S4 switches. It is clear from Fig. 3-29 and 3-30 that the blocking voltage across each switch is $\left(\frac{V_{\mathrm{dc}}}{2}\right)$ but the switching voltage is $\left(\frac{V_{\mathrm{dc}}}{4}\right)$.

Fig. 3-31 and 3-32, show the current, voltage, and instantaneous power loss across the anti-parallel diodes of switches S1 and S3 i.e., d1 and d3, and are shown in figures with symbols D1 and D3 respectively.

It can be seen here as well the blocking voltage across the anti-parallel diodes is $\left(\frac{V_{\mathrm{dc}}}{2}\right)$ but the switching voltage is $\left(\frac{V_{\mathrm{dc}}}{4}\right)$. Fig. 3-33 and 3-34, show the results of the current, voltage, and instantaneous power losses of the anti-series IGBTs which make the bi-directional switch and the anti-parallel diodes i.e., d5 and d6 (represented by D5 and D6 in Fig. 3-34) of a bi-directional switch. It must be remembered that these switches face soft switching when the commutation occurs from $\left(\frac{V_{\mathrm{dc}}}{2}\right)$ to 0 and from $\left(-\frac{V_{\mathrm{dc}}}{2}\right)$ to 0 during the operation of the converter.

Fig. 3-35, shows the input current (I_{in}), input dc-link voltage (V_{in}), the input power
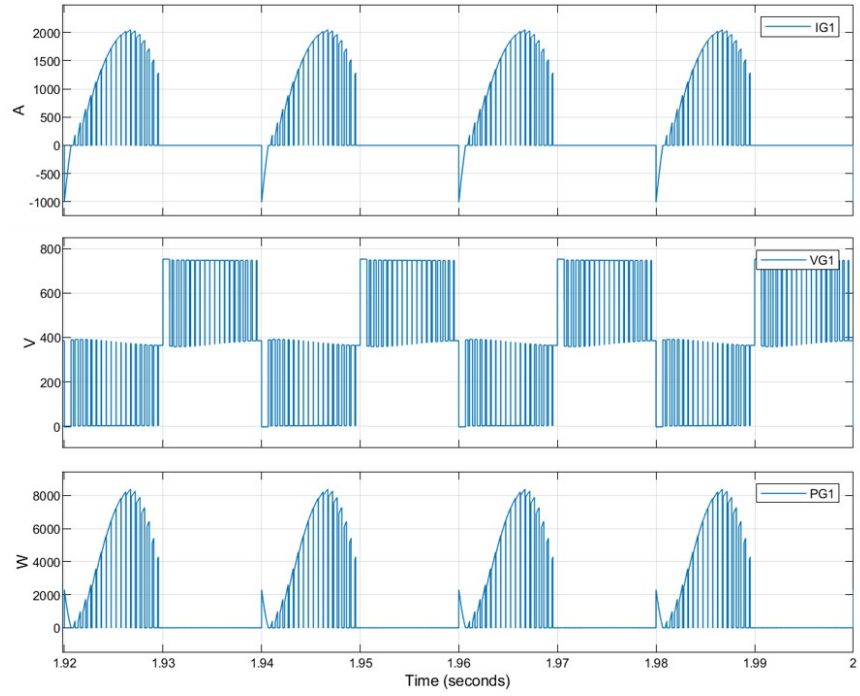
Figure 3-29: V/I/P waveform results of IGBT S1
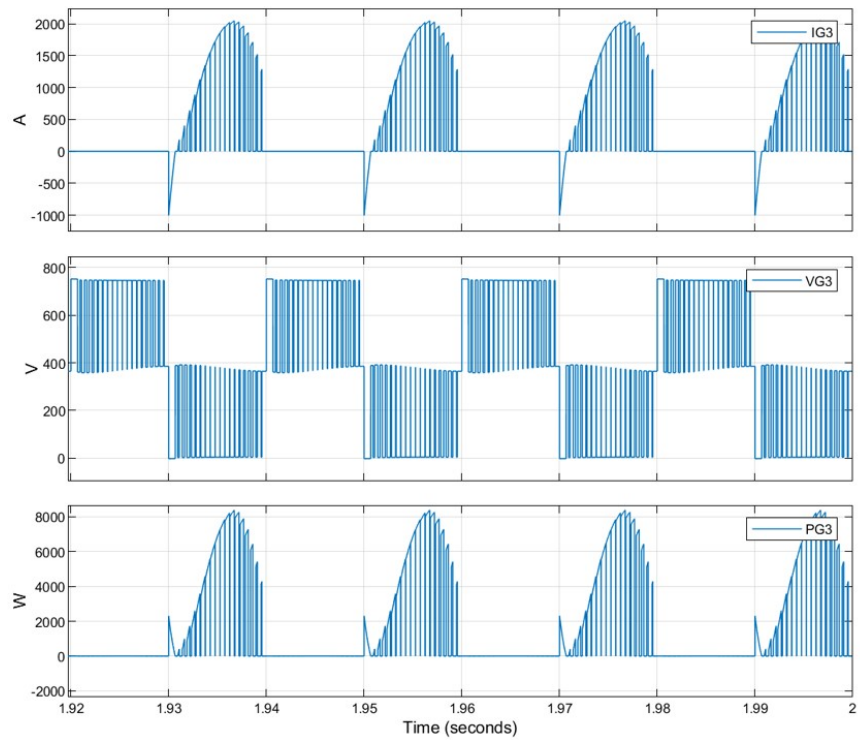
Figure 3-30: V/I/P waveform results of IGBT S3

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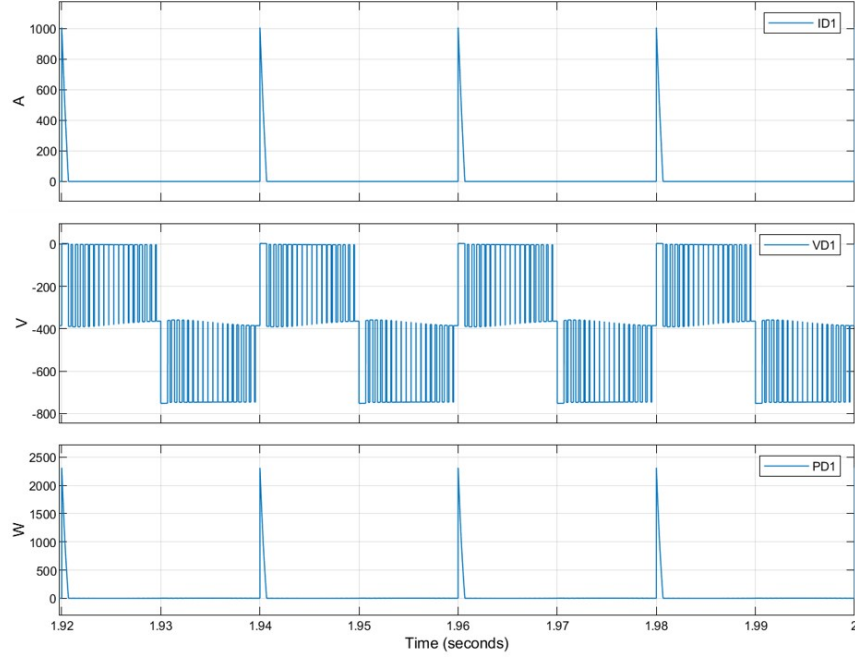
Figure 3-31: V/I/P waveform results of anti-parallel diode d1

(P_in), and output current (I_o) that is sinusoidal in this case because of the inductor in the RL-load at the output side, three levels of the output voltage (V_o), and output power (P_o).

3.4 Efficiency calculation of 3L-NPC and 3L-NPP converter

The efficiency of the converter is defined as the measurement of how effectively the converter converts the input power into a useful output power. It is an indication of how much input energy is utilized to do the useful work w.r.to lost energy (heat dissipation) and can be calculated using equation 3.16.

$$\eta = \frac{P_\text{out}}{P_\text{in}} \times 100\%$$
(3.16)

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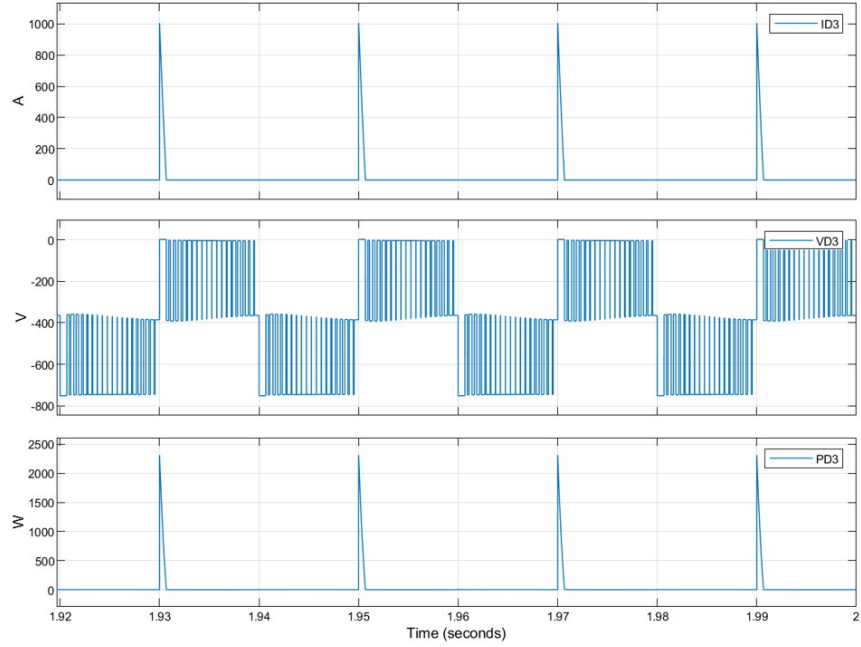
Figure 3-32: V/I/P waveform results of anti-parallel diode d3
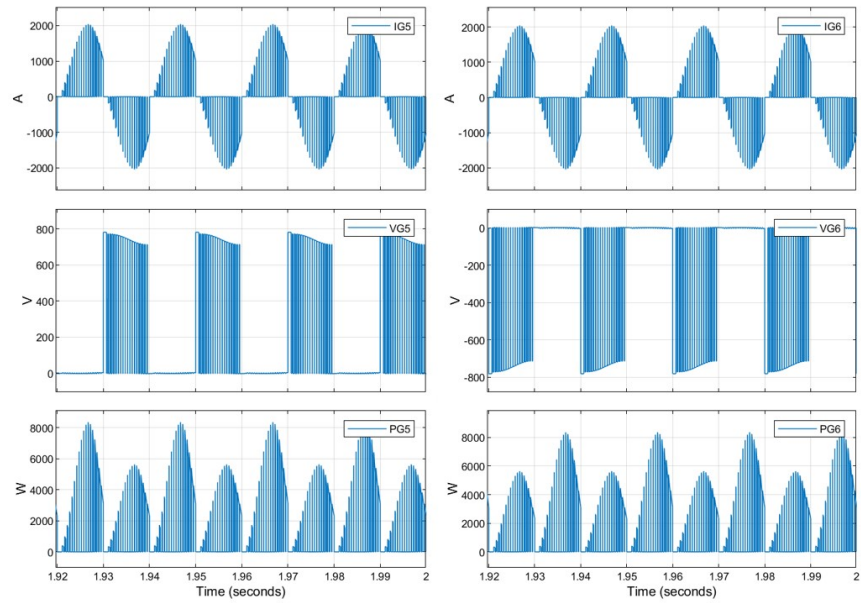
Figure 3-33: V/I/P waveform results of bi-directional switch

The input power can be expressed in terms of output power and the power losses so the efficiency in another form can be calculated using equations 3.17 and 3.18.

$$\eta = \frac{P_{\text{in}} - P_{\text{loss}}}{P_{\text{in}}} \times 100\% \tag{3.17}$$
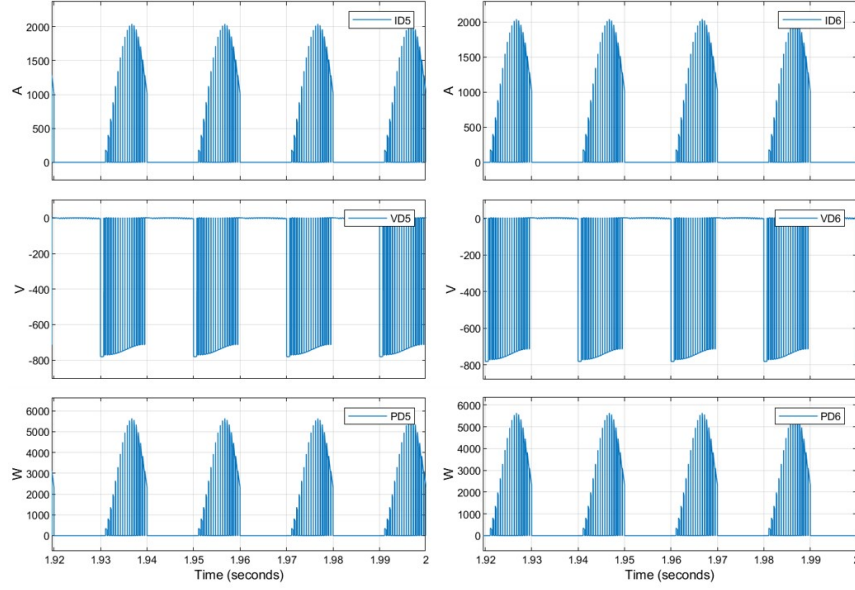
Figure 3-34: V/I/P waveform results of anti-parallel diodes of bi-directional switch
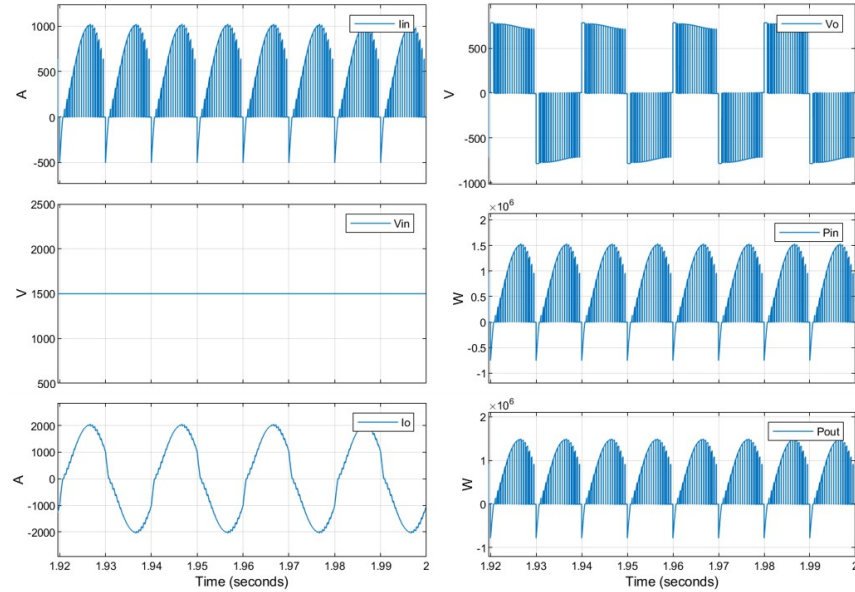
Figure 3-35: Input and output V/I/P parameters

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \times 100\% \tag{3.18}$$

The efficiency for the single-phase 3L-NPC is calculated using any of the above equations from equations 3.16 to 3.18, with both the methods i.e., using the analytical method and also using the simulation method, and the calculated efficiency is shown in Table 3.21 and 3.22 respectively. In the simulation method, the average input and

output powers are taken over a one-cycle load frequency using the mean value from signal statistics and then the efficiency calculation formula is used from equations 3.16 to 3.18.

Input Power (kW)	Total Power Losses (conduction) + (switching) (kW)	Output Power(kW)	Efficiency ($\eta\%$)
750	13.11	736.9	98.25

Table 3.21: Efficiency calculation by analytical method for 3L-NPC converter

Input Power (kW)	Total Power Losses (conduction) (kW)	Output Power(kW)	Efficiency ($\eta\%$)
749.6	9	737.5	98.38

Table 3.22: Efficiency calculation by simulation method for 3L-NPC converter

In the same way, the efficiency of the single-phase 3L-NPP converter is calculated using both analytical and simulation methods, and the results are depicted in Tables 3.23 and 3.24.

Input Power (kW)	Total Power Losses (conduction) + (switching) (kW)	Output Power(kW)	Efficiency ($\eta\%$)
750	14.5	735.5	98.07

Table 3.23: Efficiency calculation by analytical method for 3L-NPP converter

Input Power (kW)	Total Power Losses (conduction) (kW)	Output Power(kW)	Efficiency ($\eta\%$)
750	10.2	737	98.26

Table 3.24: Efficiency calculation by simulation method for 3L-NPP converter

Table 3.2 shows that the single-phase 3L-NPC converter is more beneficial for this high-voltage high-current power stack design because of the high efficiency and low cost compared with the single-phase 3L-NPP converter. So, the 3L-NPC converter is considered for further design of the power stack.

	NPC	NPP
No. of switches	4	6
Voltage stress switches	equal	equal
Efficiency	high	low
Cost	low	high
Switching	hard	hard and soft

Table 3.25: Comparison between 3L-NPC and 3L-NPP converters

Chapter 4

Simulation of three-phase three-level NPC converter

This chapter discusses the introduction of the three-phase three-level NPC converter as the final selection for designing a high-voltage high-current power stack in the very first part, in the second part of the chapter, the discussion about the DC-link capacitor sizing is further enhanced for the three-phase three-level NPC converter, and the final selection is suggested. The third part explains the choice of the PWM technique based on the neutral point (NP) voltage balance and the elimination of the low-frequency oscillations at the neutral point. In the fourth part of this chapter, load estimation for a three-phase three-level NPC converter is done and the last part of the chapter, includes the power loss analysis and simulation results of a three-phase three-level NPC converter, and FFT analysis is discussed.

4.1   Three-phase three-level NPC converter

This converter can be designed by combining (n-1) DC-link capacitors, 3×2(n-1) power switches i.e., IGBTs with anti-parallel diodes installed inside in this case, and $3 \times \{$(n-1)(n-2)$\}$ clamping diodes to produce n-levels of output voltage i.e., three-level in this design. The 3 is multiplied by the number of semiconductor switches and clamping diodes because of the three-phase system. Fig. 4-1, represents the structure

of the three-phase three-level NPC converter. Because of the symmetry that exists in the design of this converter, the working principle explained for the single-phase 3L-NPC converter in the previous chapter section 3.1.1 can be presented in the same way for the rest of the two legs of the three-phase 3L-NPC converter. It remains the same for the switching states of the converter as well as in a three-phase system, the phase voltages are 120° phase shifted from each other so it is also consistent with the switching states and working principle as well. Table 3.6, shows the switching states for the single-phase 3L-NPC converter and the corresponding voltage levels and it is also true in the case of a three-phase 3L-NPC converter except that they are 120° phase shifted. It must be noted that turning on the upper or lower three adjacent modules of a leg will cause the short-circuit of the upper or lower DC-link capacitor while turning on all 4 modules would cause the whole DC-link to be short-circuited.
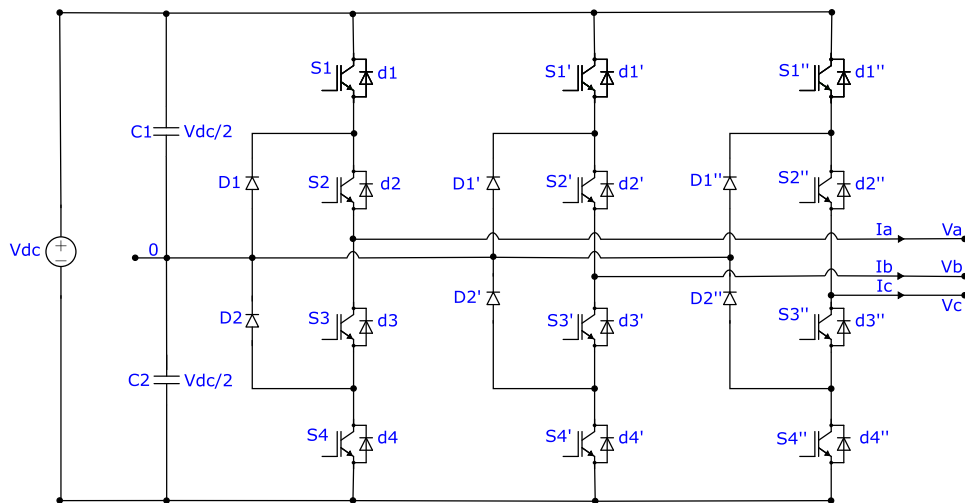
Figure 4-1: Structure of three-phase three-level NPC Converter

From Fig. 4-1, it can be seen that S1, S2, S3, S4, and their corresponding anti-parallel diodes d1, d2, d3, d4, and the clamping diodes D1 and D2 represent the components for the phase (a) whose output phase voltage and phase current are expressed as Va and Ia respectively. In the same way, a single apostrophe (') and a double apostrophe (") are used on the switches, anti-parallel diodes, and clamping diodes of phase (a) to represent phase (b) and phase (c) whose output phase voltages and currents are demonstrated as Vb and Ib for phase (b), and Vc and Ic for phase (c) respectively.

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The voltages Va0, Vb0, and Vc0 are called instantaneous pole voltages and are taken w.r.to the mid-point of the DC-link i.e., 0 as in Fig. 4-1. These pole voltages are shown below.

- $V_{a0} = 0, \pm \frac{V_{dc}}{2}$

- $V_{b0} = 0, \pm \frac{V_{dc}}{2}$

- $V_{c0} = 0, \pm \frac{V_{dc}}{2}$

It is important to understand that when the middle two switches (i.e., (S2) and (S3) for phase (a)) and the corresponding middle switches for the other two phases are turned on, then all the pole voltages at the output side appear to be zero. But for $\left(+\frac{V_{dc}}{2}\right)$ or $\left(-\frac{V_{dc}}{2}\right)$ the two transistors or the two anti-parallel diodes in the top part of the leg or to the bottom part of the leg have to be turned on. The line-to-line voltage can be given as V{ab} = V{a0} - V{b0}. This line-to-line voltage has five possible values i.e., $\pm V_{dc}, \pm \frac{V_{dc}}{2}$, and 0. The phase voltages V_a, V_b, and V_c can be found by using the following equation 4.1.

$$Va = Vm \sin(\omega t)$$
$$Vb = Vm \sin(\omega t + 120°) \qquad (4.1)$$
$$Vc = Vm \sin(\omega t + 240°)$$

where V_m is the maximum amplitude of the output voltage, ω is called angular frequency. Similarly, the phase currents I_a, I_b, and I_c can be calculated by dividing the corresponding phase voltages by the impedance (Z) of the load.

$$I_a = \frac{Vm \sin(\omega t)}{Z}$$
$$I_b = \frac{Vm \sin(\omega t + 120°)}{Z} \qquad (4.2)$$
$$I_c = \frac{Vm \sin(\omega t + 240°)}{Z}$$

4.2 DC-link capacitor sizing

The voltage ripple requirement, capacitor current ripple, and capacitance rating of the DC-link capacitors determine DC-link capacitors for the inverter. The voltage rating of the selected capacitor must be greater than the DC-link operation voltage to avoid and mitigate the voltage oscillations, and effects caused by the input grid voltage fluctuations or by the transitory regenerative operation of the inverter. The capacitor current ripple is accountable for the capacitor power losses that are not considered in this part of the design and are dependent on the series resistance of the capacitor. This series resistance (ESR) varies w.r.to frequency of capacitor current in the case of electrolytic capacitors. The DC-link capacitor value is calculated by considering the maximum allowable voltage ripple ($\frac{\Delta V_{C,\max}}{2}$)which is capacitor current harmonic dependent. Assuming all voltage harmonics are in phase, the needed capacitance is calculated by equation 4.3 [66].

$$C \geq \frac{1}{\frac{\Delta V_{C,\max}}{2}} \sum_h \frac{I_h}{2\pi f_h} \tag{4.3}$$

This equation 4.3, states that the inverter switching (PWM) action produces high-frequency (HF) capacitor current harmonics, which have a negligible impact on the capacitor voltage ripple. Conversely, low-frequency (LF) harmonics, which are found at multiples of the inverter fundamental frequency, might result in low-frequency capacitor voltage fluctuations, which can increase the necessary capacitance. Increased capacitance may be necessary for various uses, such as voltage support during input power outages. If the calculation is limited to the fundamental frequency component then equation 4.3 in normalized form of capacitor voltage ripple can be written as in equation 4.4.

$$\frac{\text{Norm}\,(\Delta V_C)}{2} = \frac{fC}{I_o} \left(\frac{\Delta V_C}{2}\right) \tag{4.4}$$

Where $\frac{\text{Norm}(\Delta V_C)}{2}$ is the normalized capacitor voltage ripple, f is the fundamental frequency, and I_o is the output sinusoidal current and C is the capacitance of the DC-link capacitors. This formula can also be used to calculate the value of capacitance

required to maintain the required maximum voltage ripple across the capacitor.

Analysis of the voltage ripple across DC-link capacitor

The analysis of the voltage ripple across the individual DC-link capacitors and the whole DC-link capacitor is done by varying the calculated values of the capacitance and the power factor to get the suitable value of capacitance for this design. The analysis is carried out using the same value of the DC-link capacitance that was calculated for the single-phase 3L-NPC converter in the previous chapter i.e., 85 mF. The analysis is carried out for a rated power of 1.5 MVA and also for 750 kVA for the design of a three-phase 3L-NPC converter. The analysis is carried out considering the different values of the DC-link capacitor i.e., 85 mF, 42.5 mF, 21.25 mF, 12 mF, 10.625 mF, 5.3125 mF, 2.6525 mF by varying the power factor i.e., 0, 0.5, 0.85, 0.9, and 1 corresponding to each value of DC-link capacitance. In each analysis of both designs, it was observed that by varying the values of the DC-link capacitance with varying power factor the voltage ripple across the individual capacitors of the DC bus, and the voltage ripple across the whole DC bus varies at each analysis. The analysis of the voltage ripple across the DC-link and DC-link capacitors is done by using the controlled current source that is controlled by the PI controller and the gains of the PI controller are calculated considering the DC-link capacitance as a plant to maintain the dc-bus voltage to 1500 V as in Fig. 4-2, implementation is done using the MATLAB/Simscape environment and this implementation is done to simplify the rectifier design. It must be remembered that using the same procedure the analysis for a single-phase 3L-NPC was done in the section on analysis of voltage ripple across DC-link capacitors in the previous chapter.

It must be remembered that the circuit of the 3-phase 3L-NPC converter in Fig. 4-1, is used inside the subsystem block. It is concluded from the analysis of the voltage ripple across DC-link and DC-link capacitors that a 12 mF capacitor value is suitable for the final design of the 3-phase 3L-NPC converter for the design of a high-voltage high-current power stack and the analysis is shown in Table 4.1 for the design of 750 kVA rated power of 3-phase 3L-NPC converter. The parameters for this design are
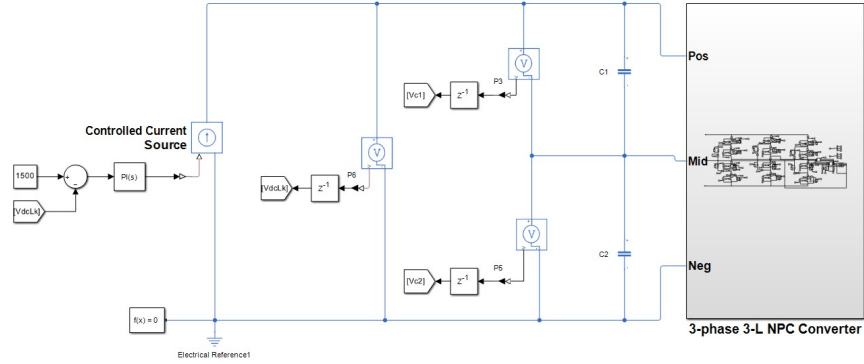
Figure 4-2: Voltage ripple analysis circuit across the DC-link capacitors

shown in Table 3.4 except for the value of DC-link capacitance that is changed from 85 mF to 12 mF.

Type of load	Pf	$\Delta V_{\text{dc-link}}$	ΔV_{c1}	ΔV_{c2}
L	Pf=0	0.28%	13.38%	13.4%
RL	Pf=0.5	0.26%	5.4%	5.4%
RL	Pf=0.85	0.26%	0.57%	0.57%
RL	Pf=0.9	0.25%	0.53%	0.52%
R	Pf=1	0.29%	1.96%	1.96%

Table 4.1: DC-link capacitor voltage ripple analysis on different Pf

From Table 4.1, it can be concluded that at a DC-link capacitance of 12 mF, due to the variation of the active power, the voltage ripple across the capacitors varies and it is always less than the selected maximum affordable voltage ripple considered for the design except when the load is purely inductive in nature or half-inductive and half resistive. The voltage ripple across the DC-link and DC-link capacitors at a power factor of 0.85 that is considered for the design is shown in Fig. 4-3, in which VdcLk shows the voltage ripple across DC-link, Vc1, and Vc2 show the voltage ripple across capacitor C1 and capacitor C2 respectively. The analysis shown in Table 4.1, is done for the 1.5 MVA power rating for the design of a 3-phase 3L-NPC converter but the voltage ripple waveform across dc-link and dc-link capacitors is shown in Fig. 4-4 at capacitance of 12 mF and power factor of 0.85 and data in Table 3.2 is used. It is observed that the voltage ripple across the dc-link is 0.46%, and across the capacitors C1 and C2 is 1.12%.

Figure 4-3: Voltage ripple across DC-bus and DC-bus capacitors

Figure 4-4: Voltage ripple across DC-bus and DC-bus capacitors

4.3 PWM technique for 3-phase 3L-NPC converter

A simple zero-sequence voltage injection method for carrier-based pulse width modulation is selected for the three-phase three-level NPC converter because this method

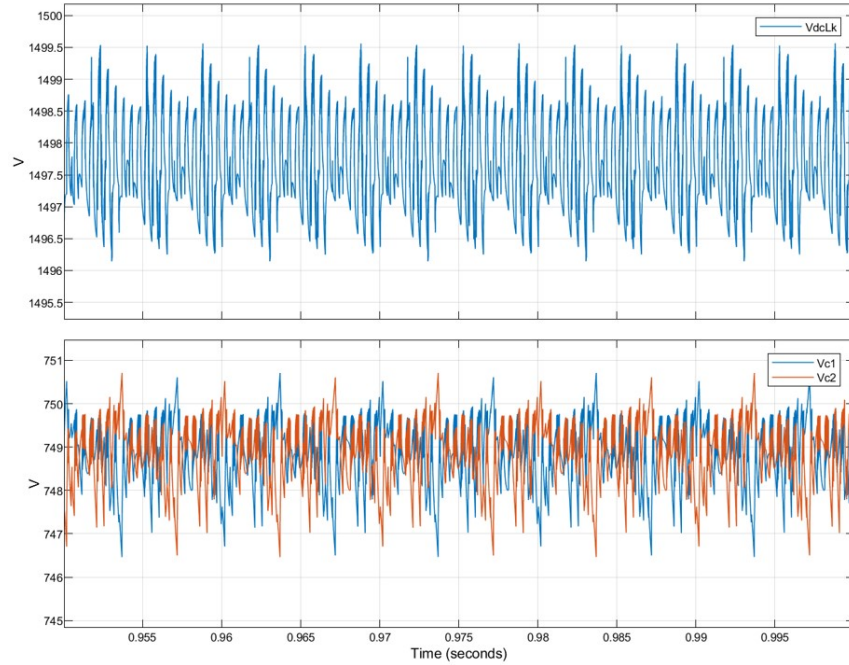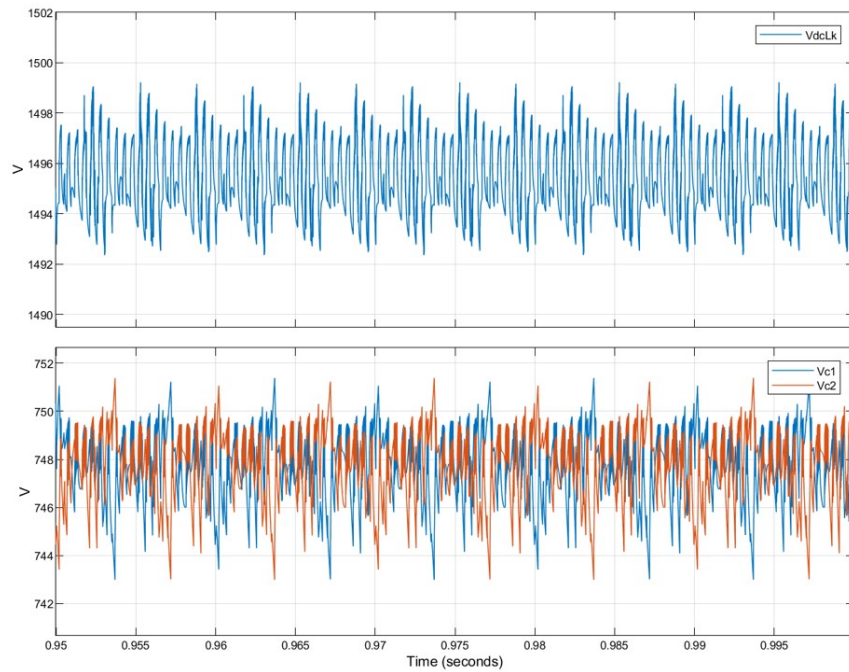mitigates low-frequency voltage oscillations at the neutral point (NP), eliminates the problem of voltage unbalances at the DC-link, reduces the switching losses approximately 1/3 since there are 1/3 fewer transitions than with the normal SPWM. This technique requires low computation time and is easy to implement. This technique is explained briefly in section 2.2.7. In this technique, the three sinusoidal reference voltages used are;

$$v_{a,\text{ref}} = m \cdot \cos(2\pi f_s t)$$
$$v_{b,\text{ref}} = m \cdot \cos(2\pi f_s t - \frac{2\pi}{3})$$
$$v_{c,\text{ref}} = m \cdot \cos(2\pi f_s t + \frac{2\pi}{3})$$

(4.5)

where f_s is the fundamental frequency and m is the modulation index of the reference voltages. In this technique, the calculation of the zero-sequence component does not require the three-phase currents and can be given as [52];

$$v_{zs} = \begin{cases} v_{zs,\text{max}} = 1 - \max(v_{a,\text{ref}}, v_{b,\text{ref}}, v_{c,\text{ref}}), & \text{if } V_{c1} \geq V_{c2} \\ v_{zs,\text{min}} = -1 - \min(v_{a,\text{ref}}, v_{b,\text{ref}}, v_{c,\text{ref}}), & \text{if } V_{c1} < V_{c2} \end{cases}$$

(4.6)

where $\min[va_{\text{ref}}, vb_{\text{ref}}, vc_{\text{ref}}]$ and $\max[va_{\text{ref}}, vb_{\text{ref}}, vc_{\text{ref}}]$ refer to the minimum and maximum values of the reference phase voltages signals denoted in equation 4.5, and V_{c1} and V_{c2} represents the upper and lower capacitor voltages respectively. When the zero-sequence component is added to the three-phase sinusoidal reference signals, they are known as three-phase modulated signals and can be represented in equation 4.7.

$$v_{x,\text{mod}} = v_{x,\text{ref}} + v_{zs}, \quad x = a, b, c$$

(4.7)

After adding the zero-sequence component, the signals obtained are compared with the pair of carrier signals that are phase-shifted by 180° to generate the gate signals. The carrier signals are phase-shifted by 180° to reduce the voltage ripple at the DC bus and across the DC bus capacitors. The assumed load at the output is RL so it is reasonable to write the phase load currents are sinusoidal when it is connected to

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a 3-phase 3L-NPC converter depicted in equation 4.8.

$$I_a = I \cdot \cos\left(2\pi f_s t - \varphi\right)$$

$$I_b = I \cdot \cos\left(2\pi f_s t - \frac{2\pi}{3} - \varphi\right) \tag{4.8}$$

$$I_c = I \cdot \cos\left(2\pi f_s t + \frac{2\pi}{3} - \varphi\right)$$

where I is called the peak amplitude of the phase currents, φ is the load power factor angle, and is in between the range [-90°, 90°] and f_s is the fundamental frequency. The gate signals for the four switches of each phase are then generated by comparing the modulated signal with the upper carrier signal that is in the range [0 1 0] and the lower carrier signal that is in the range [0 -1 0] and upper carrier is responsible for the switching of switches at the top part of the leg and lower carrier is responsible for the switching of switches at the lower part of the leg. The analysis is further carried out in [52]. The implementation of this technique is done using MATLAB/Simulink software as shown in Fig. 4-5.
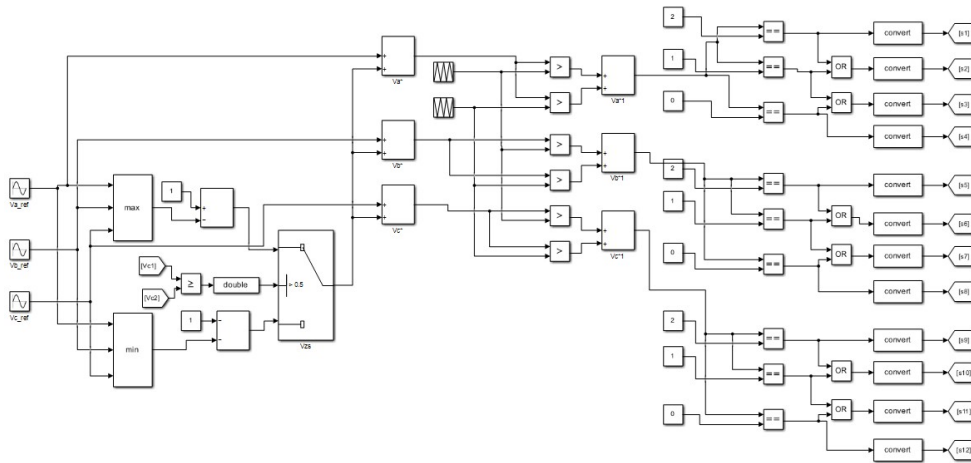
Figure 4-5: Simulink implementation of CB-PWM technique

The three-phase modulated signals obtained after adding a zero-sequence voltage component are shown in Fig. 4-6 whose voltages are shown per unit i.e., pu_V. These modulation signals are then compared with the top carrier signal and the bottom carrier signal to get the gate signals as shown in Fig. 4-7 where phase (a) modulated
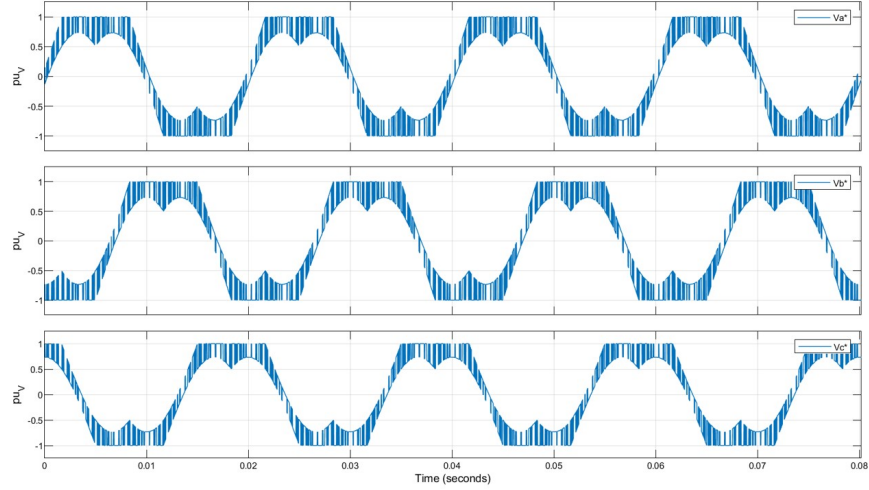
Figure 4-6: Three-phase modulation signals

signal (Va*) is compared with C_{top} and C_{bottom} to get the PWM signals. The obtained
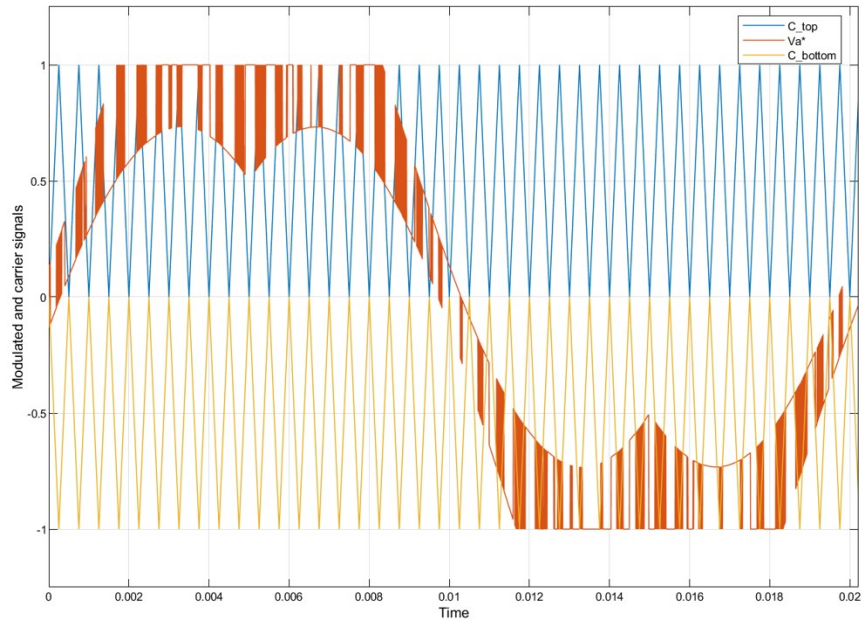
Figure 4-7: Comparison of modulated and carrier signals

PWM signals for the three phases when compared with a pair of carrier signals are shown in Fig. 4-8, where Ga, Gb, and Gc represent the gate signals for phases a, b, and c respectively. These PWM signals lie in the threshold level of [0,1,2].
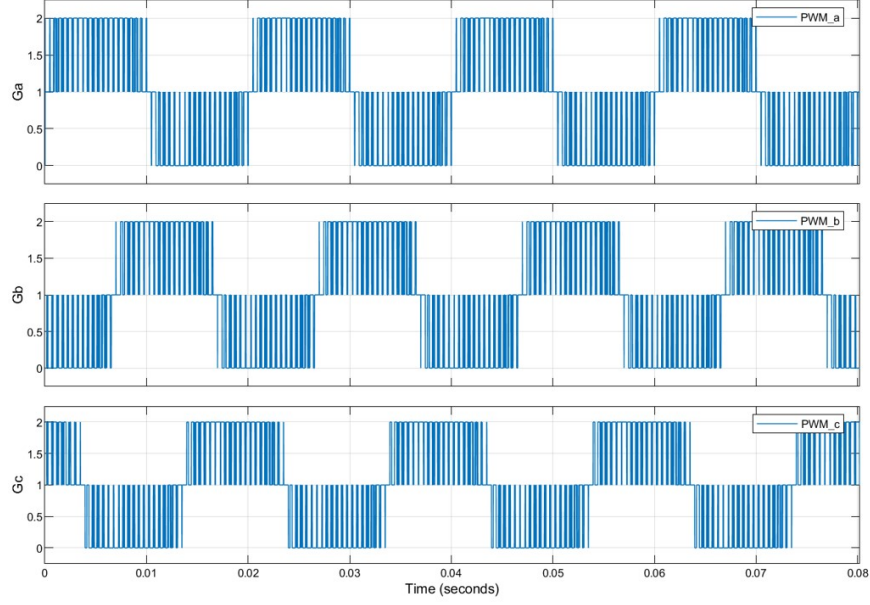
Figure 4-8: Three-phase PWM signals

4.4 Load estimation of 3-phase 3L-NPC converter

The load estimation of the three-phase three-level NPC converter is done based on the rated power of the converter and the output voltage. In this case, the two designs of the converter are made, the main design which is 1.5 MVA, and the other design for testing and utilization of available material is 750 kVA. The load is estimated for both cases and the output voltage in both cases is assumed to be $\left(-\frac{V_{dc}}{2}\right)$ i.e., half of the DC-link voltage, and is considered as the peak output voltage. The following expressions are used for the load estimation when the load is star-connected. The rated power of the three-phase converter i.e., apparent power can be calculated by using equation 4.9.

$$S = \sqrt{3} \cdot V_{\text{L-L}} \cdot I_{\text{L-L}} \tag{4.9}$$

where $I_{\text{L-L}}$, $V_{\text{L-L}}$ are the line-to-line rms output current and the line-to-line rms output voltage. The peak voltage is given so the rms can be obtained by dividing the peak voltage by $\sqrt{2}$. The rms line-to-line voltage can be given by equation 4.10.

$$V_{\text{L-L}} = \sqrt{3} \cdot V_{\text{ph}} \tag{4.10}$$

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The rms output current can be found by using equation 4.9, and it must be noted that the phase and line-to-line currents in the three-phase star-connected load are the same. The per-phase impedance is given in equation 4.11.

$$Z_{\text{ph}} = \frac{V_{\text{ph}}}{I_{\text{ph}}} \tag{4.11}$$

To calculate the per-phase resistance the given expression is used.

$$\text{Pf} = \frac{R_{\text{ph}}}{Z_{\text{ph}}} \tag{4.12}$$

To calculate the inductive reactance equation 4.13 is used.

$$Z_{\text{ph}} = \sqrt{R_{\text{ph}}^2 + X_{L,\text{ph}}^2} \tag{4.13}$$

The inductance per phase is then calculated by using equation 4.14.

$$L_{\text{ph}} = \frac{X_{L,\text{ph}}}{2\pi f} \tag{4.14}$$

Where f is called the fundamental frequency. The active or true or consumed power and the reactive power can be calculated by using equation 4.15.

$$P = \sqrt{3} \cdot V_{\text{L-L}} \cdot I_{\text{L-L}} \cdot \cos(\phi)$$
$$Q = \sqrt{3} \cdot V_{\text{L-L}} \cdot I_{\text{L-L}} \cdot \sin(\phi) \tag{4.15}$$

where ϕ is called the load power factor angle. Table 4.2, shows the values that were used to estimate the load for the 3-phase 3L-NPC converter, and the load is star-connected. Using the above equations from 4.9 to 4.11, the calculated per-phase

Parameter	Values
Rated output Power (S)	1.5 MVA
Per-phase output peak voltage $V_{\text{ph, peak}}$	750 V_{dc}
Power factor (Pf)	0.85

Table 4.2: Parameters used for three-phase load estimation

impedance is $563\,\text{m}\Omega$. Using equations from 4.12 to 4.14, the per-phase resistance and inductance calculated are $478.5\,\text{m}\Omega$ and 0.9454 mH respectively. Similarly, the rated output power is changed from 1.5 MVA to 750 kVA, and rest of the parameters in Table 4.2 are the same and the load is estimated for the three-phase three-level NPC converter having per-phase impedance of $1.125\,\Omega$. Again equations from 4.12 to 4.14 are used and the estimated per-phase resistance and per-phase inductance are $965.25\,\text{m}\Omega$ and $1.886\,\text{mH}$ respectively. It is important to note that it is the per-phase load estimation of a three-phase balanced star-connected load.

4.5 Power loss analysis of 3-phase 3L-NPC converter

The conduction power losses through the semiconductor switches and switching losses of semiconductor devices are included in the power loss analysis of the three-phase three-level NPC converter. It is noted that the DC-link losses are neglected for this analysis. Table 4.3, shows converter design parameters for a 3-phase 3L-NPC converter used in the simulation, and Table 4.4, expresses the analytical calculation of the conduction currents through the semiconductor devices i.e., IGBTs, anti-parallel diodes, and clamping diodes using the conduction current equations from 3.3.1. These analytically calculated currents are then compared with the simulated results. It is important to note that the three-phase load is balanced and star-connected the calculation analysis is done for the single leg of the 3L-NPC converter. The remaining two phases will have the same currents flowing through the devices and 120° phase shifted. The parameters of the semiconductor devices are taken from Table 3.14, from the previous chapter. The average (I_{avg}) and rms (I_{rms}) conduction currents through the IGBTs, anti-parallel diodes, and clamping diodes for phase (a) are shown in Table 4.4 and for phase (b) and phase (c) are going to be the same but phase shifted by 120°. The average power losses per pulse for IGBTs, anti-parallel diodes, and clamping diodes are analytically calculated using equations 3.6 and 3.7 for the switching losses,

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Parameter	Values
DC-link voltage ($V_{\text{dc-link}}$)	1500 Vdc
Rated power (S)	750 kVA
DC-link capacitance (C)	12 mF
Switching (carrier) frequency (f_{sw})	2 kHz
Load frequency (f)	50 Hz
Phase load impedance (Zph)	1.125 Ω
Power factor (Pf)	0.85
Modulation index (m)	1

Table 4.3: Design parameters

Calculation method	IGBT S1, S4	IGBT S2, S3	Anti-parallel diodes d1-d4	Clamping diodes D1, D2
Analytical method	I_{avg} = 169.6 A I_{rms} = 284.1 A	I_{avg} = 209.3 A I_{rms} = 332.5 A	I_{avg} = 2.07 A I_{rms} = 23.1 A	I_{avg} = 64.7 A I_{rms} = 172.9 A
Simulation method	I_{avg} = 142.7 A I_{rms} = 277.6 A	I_{avg} = 211.6 A I_{rms} = 332.5 A	I_{avg} = 3.75 A I_{rms} = 27 A	I_{avg} = 68.9 A I_{rms} = 183 A

Table 4.4: Analytical and simulated current values of devices

and for conduction losses, equation 3.8 is used. Table 4.5, shows the conduction and switching power losses calculated analytically for phase (a). In the below table, the losses are multiplied by 2 or 4 which predicts the number of devices used per phase.

Power losses	IGBT S1,S4	IGBT S2, S3	d1, d2, d3, d4	D1, D2
Conduction losses	0.4284 × 2 kW	0.5396 × 2 kW	0.00407 × 4 kW	0.1497 × 2 kW
Switching losses	0.72 × 2 kW	0.72 × 2 kW	0.22 × 4 kW	0.208 × 2 kW

Table 4.5: Analytical calculation of average power losses of devices

Table 4.6, shows the simulation results of the average power losses including only the conduction losses that are calculated by using the product of voltage times current (P = V × I) through each of the IGBT, anti-parallel diodes of each of the IGBT, and clamping diodes for phase (a). The switching losses are not considered in the simulation of the three-phase 3L-NPC converter. Remember that the 3-phase 3L-NPC converter simulation is done in MATLAB/Simscape platform to analyze the results and average values of conduction power losses are taken over a one-cycle of load frequency using mean value from signal statistics. The design parameters in

Table 4.3 are used for simulation.

Power losses	IGBT S1,S4	IGBT S2, S3	d1, d2, d3, d4	D1, D2
Conduction losses	0.3868×2 kW	0.5602×2 kW	0.008798×4 kW	0.1604×2 kW

Table 4.6: Simulation results of average power losses of devices

Fig. 4-9 and 4-10, show the current, voltage, and instantaneous conduction power losses of BJTs of the IGBTs S1 and S2 of phase (a) and waveform of the 3rd and 4th BJTs of IGBTs S3 and S4 are observed in the same way for phase (a) as both switches are S3 and S4 are complementary of S1 and S2 respectively.
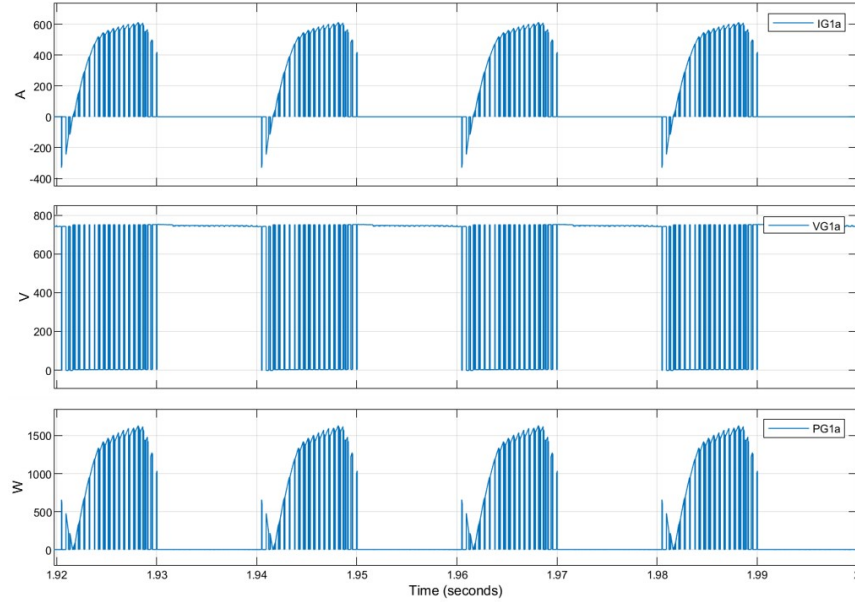
Figure 4-9: V/I/P waveform results of phase (a) (S1)

Similarly, the current, voltage, and instantaneous conduction power loss waveforms of the 1st and 2nd BJTs of IGBTs (S1', S1") and (S2', S2") of phase (b) and (c) are shown in Fig, 4-11, Fig. 4-12, Fig. 4-13, and Fig. 4-14 respectively. The complementary switches waveforms can be analyzed in the same way as it is analyzed for the main switches of both phases (b) and (c) respectively.

When the current flows from the load to the DC-link in that case the anti-parallel diodes have to provide a path to the flow of the current and when these diodes start

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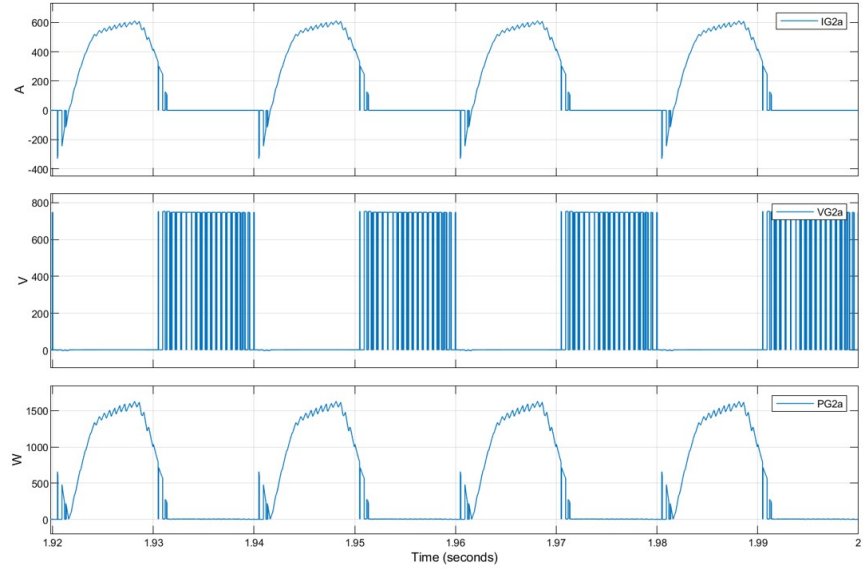
Figure 4-10: V/I/P waveform results of phase (a) (S2)
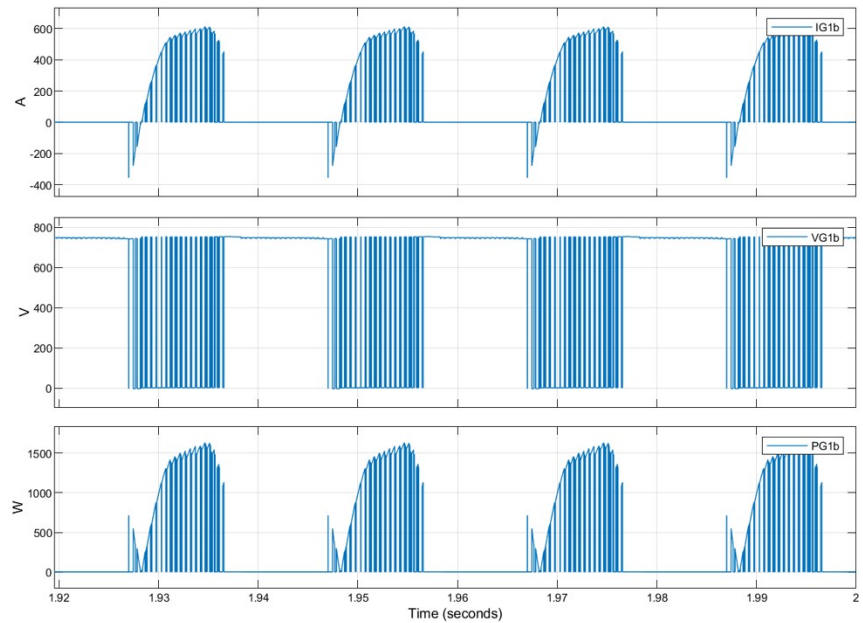
Figure 4-11: V/I/P waveform results of phase (b) (S1')

conducting due to the forward voltage drop and turn on resistance of the diode, the power losses occur and can be shown in Fig. 4-15 to Fig. 4-20, of the 1st and 2nd anti-parallel diodes of 1st and 2nd IGBTs. All the phases are 120° phase shifted and it can also be analyzed from the waveforms that they are phase shifted and as the three-phase load is balanced star-connected load, the remaining switches and their
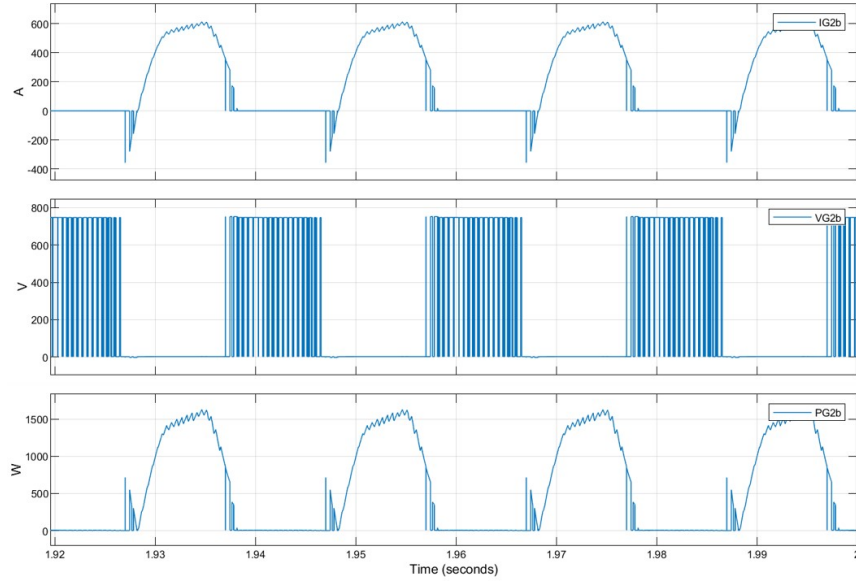
Figure 4-12: V/I/P waveform results of phase (b) (S2')
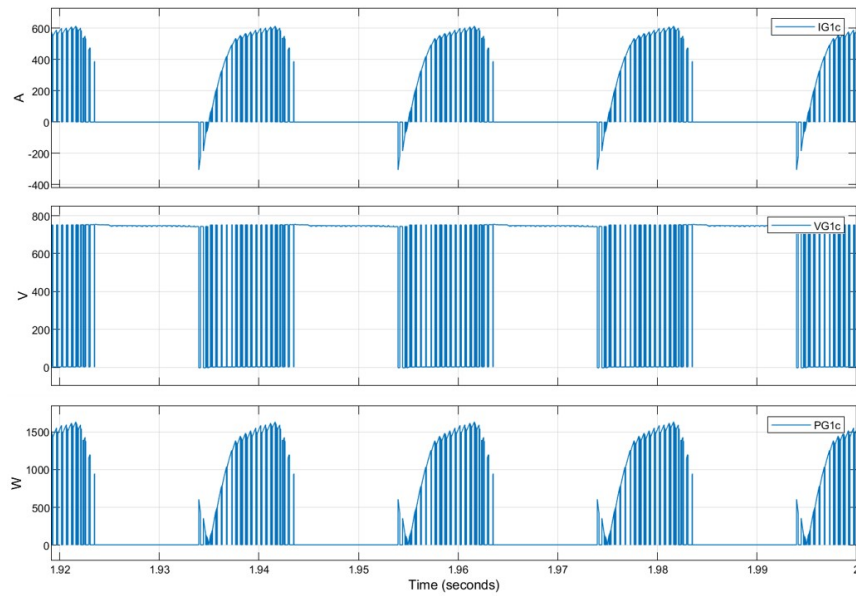
Figure 4-13: V/I/P waveform results of phase (c) (S1")

waveforms are the same.

When the output voltage state is zero then switches S2, S3, and clamping diodes D1 and D2 have to conduct for each phase, and during conduction because of the conduction of the current and forward voltage drop, the power losses happen and these power losses are also called as turn-on power losses because they also depend
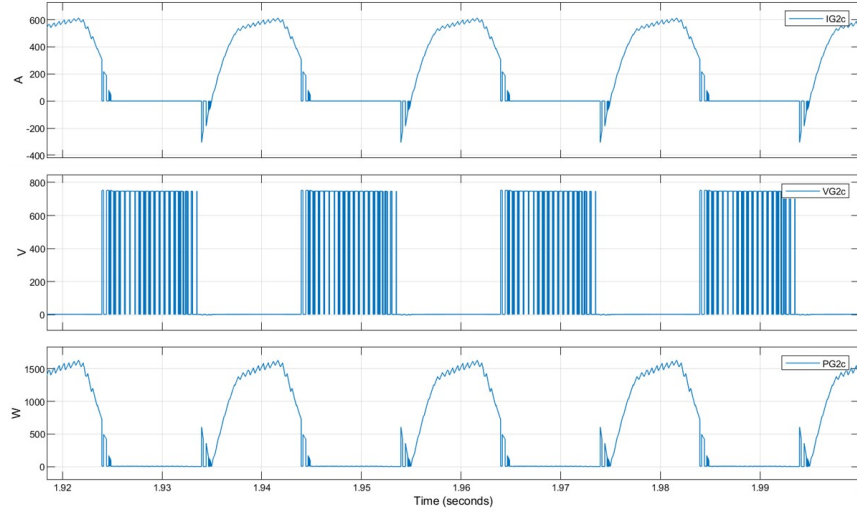
Figure 4-14: V/I/P waveform results of phase (c) (S2")
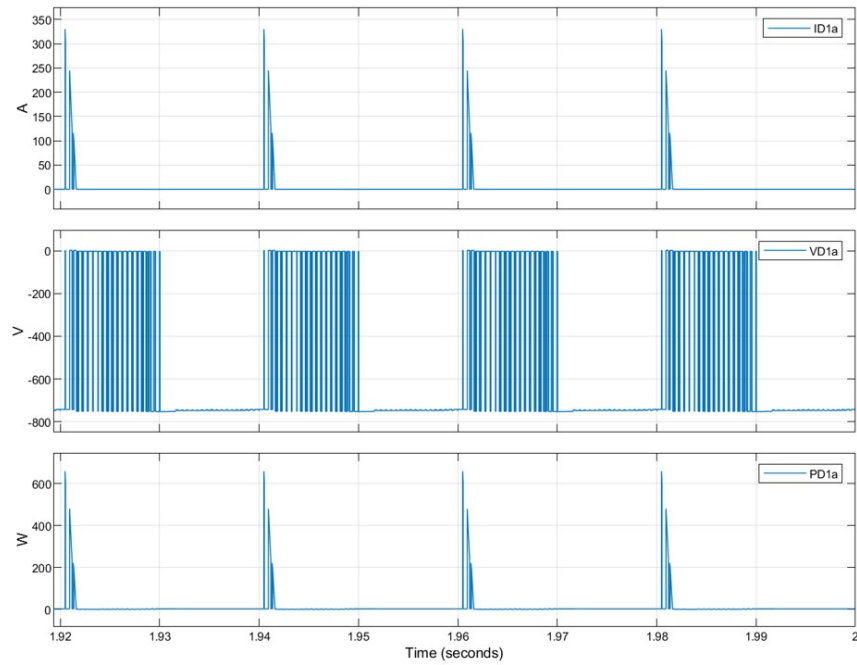
Figure 4-15: V/I/P waveform results of phase (a) anti-parallel diode (d1)

on the on-state resistance of the each device. The waveforms of current, voltage, and instantaneous conduction power loss of each phase clamping diode i.e., D1, D1', and D1" are shown in Fig. 4-21, 4-22, and 4-23 respectively.

Fig. 4-24, shows the three-phase currents flowing through the balanced three-phase star-connected load in which the phase currents and line-to-line currents are equal.

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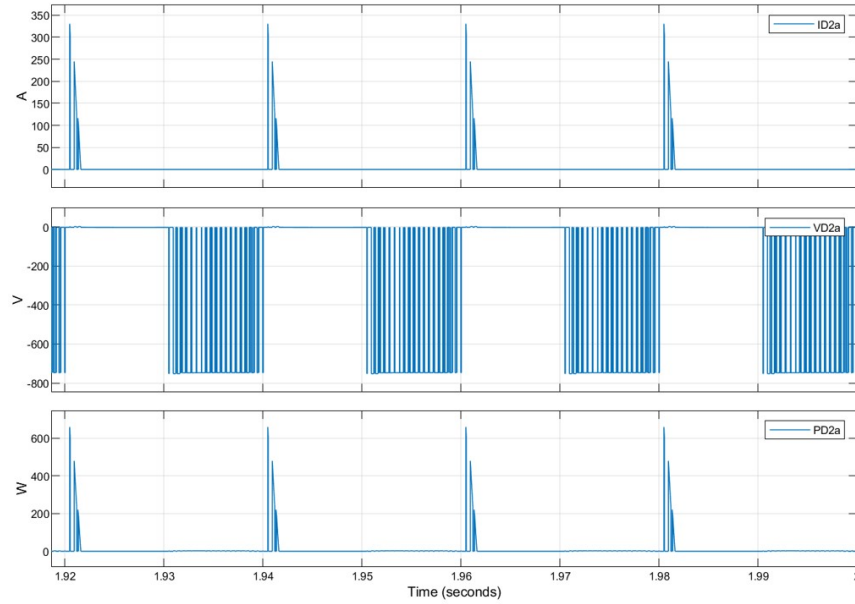
Figure 4-16: V/I/P waveform results of phase (a) anti-parallel diode (d2)
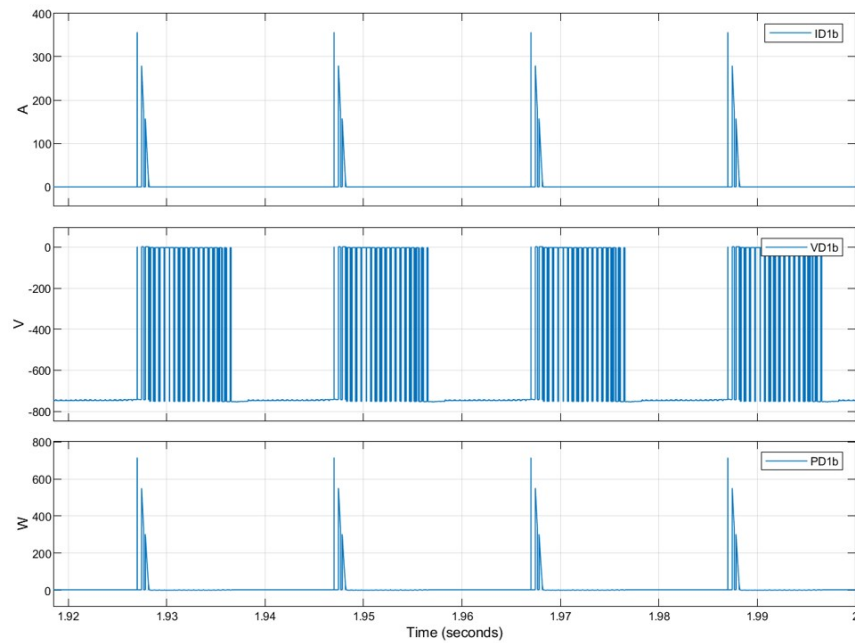
Figure 4-17: V/I/P waveform results of phase (b) anti-parallel diode (d1')

Fig. 4-25, depicts the line-to-line voltages and the phase voltages w.r.to the mid-point of the DC-link for three-phase balanced star-connected load. It must be noted that the line-to-line voltages are $\sqrt{3}$ times phase voltages and line-to-line voltages have the five levels as discussed in 4.1 and five levels can be seen from the line-to-line voltages
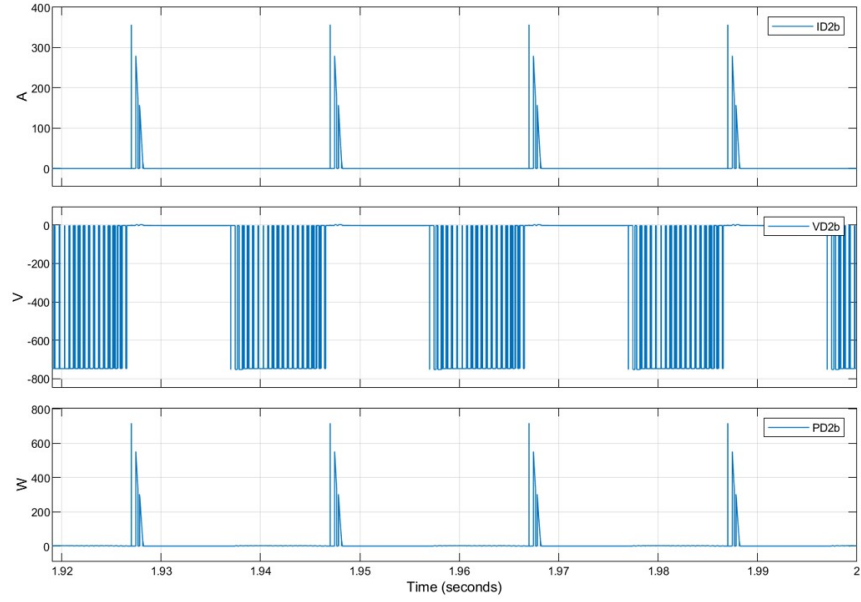
Figure 4-18: V/I/P waveform results of phase (b) anti-parallel diode (d2')
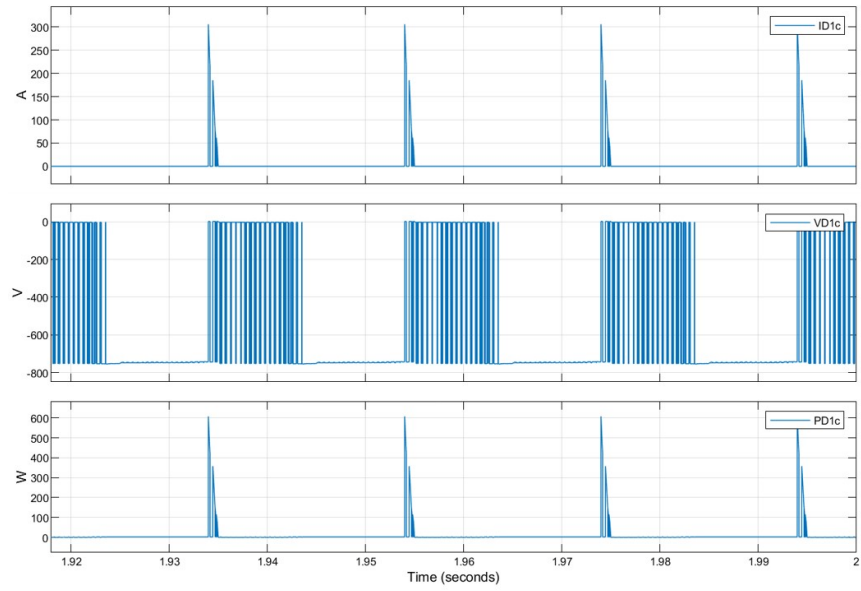
Figure 4-19: V/I/P waveform results of phase (c) anti-parallel diode (d1")

of the three-phase three-level NPC converter.
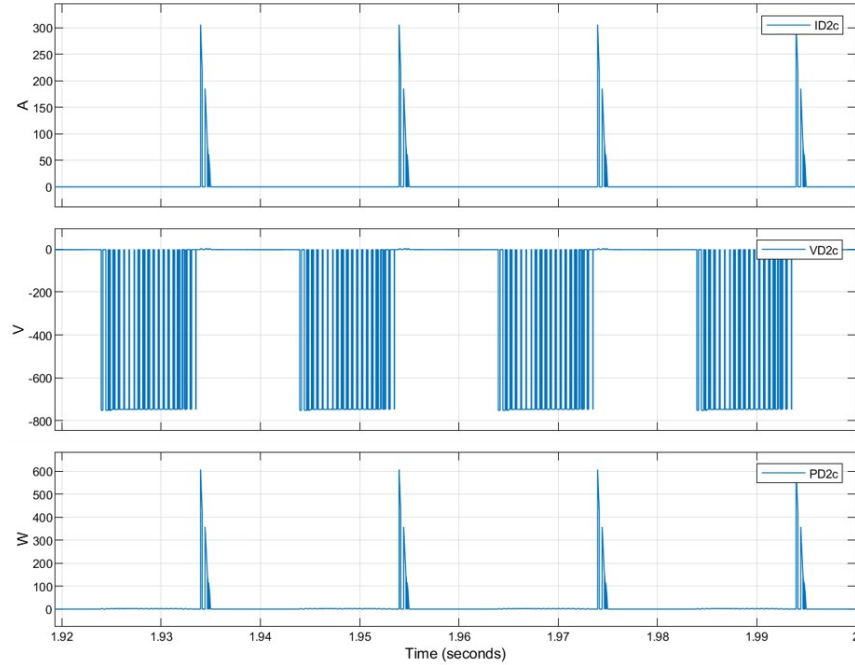
Figure 4-20: V/I/P waveform results of phase (c) anti-parallel diode (d2")
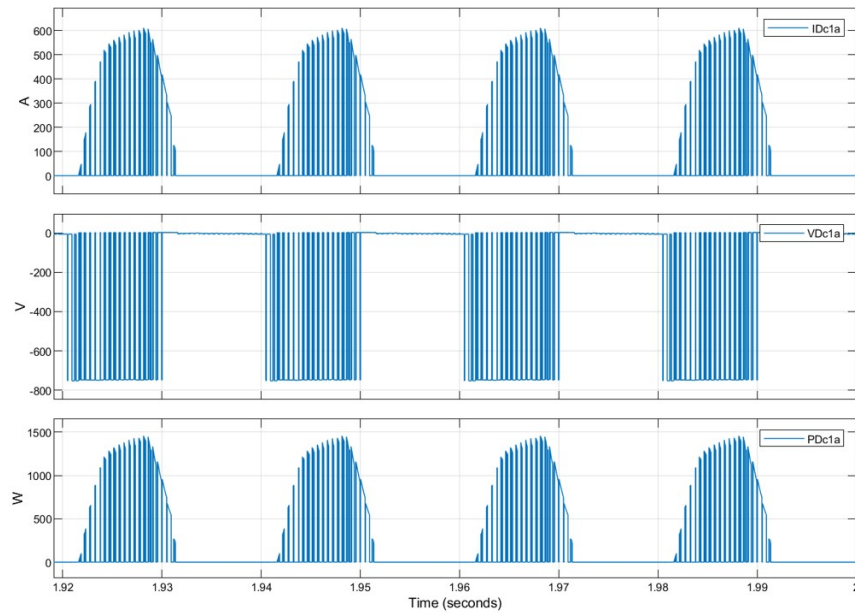
Figure 4-21: V/I/P waveform results of phase (a) clamping diode (D1)

4.6 Efficiency calculation of 3-phase 3L-NPC converter

The discussion about the definition of efficiency and its calculation is briefly explained in 3.4. The efficiency of the three-phase three-level NPC converter is calculated using
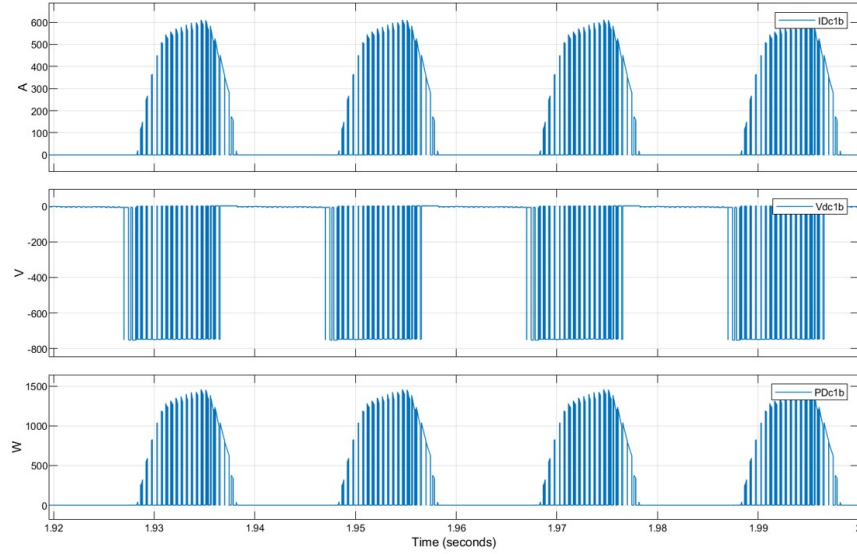
Figure 4-22: V/I/P waveform results of phase (b) clamping diode (D1)
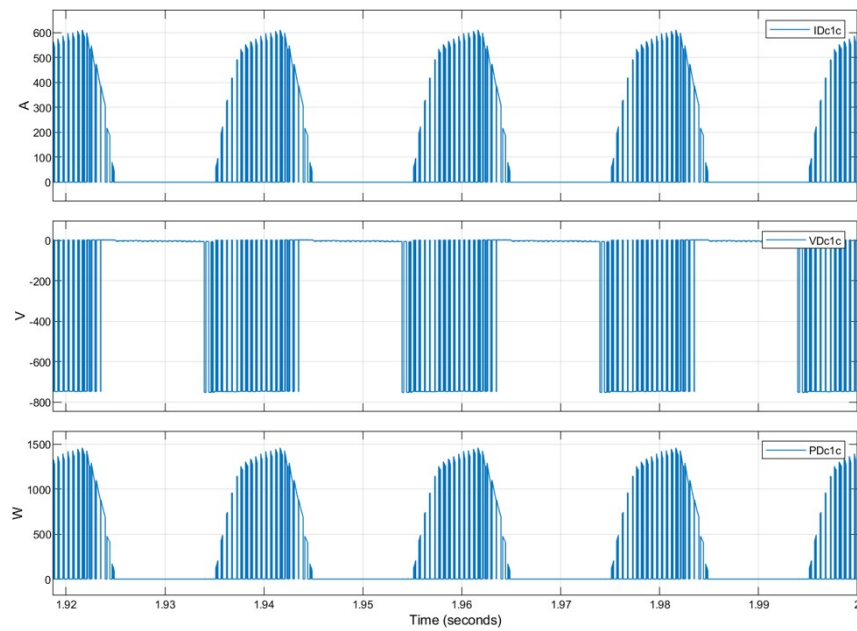
Figure 4-23: V/I/P waveform results of phase (c) clamping diode (D1)

two methods i.e., analytical and simulation methods. Table 4.7, shows the analytically calculated average power losses i.e., conduction and switching per pulse using the calculation of the single phase that has been performed in Table 4.5, and the values in this table are multiplied by 3 because of the balanced three-phase star-connected load.
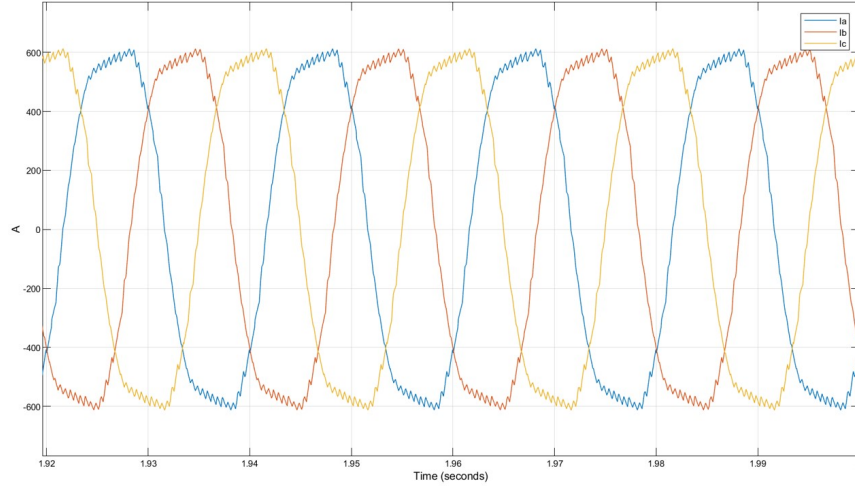
Figure 4-24: Three-phase output currents
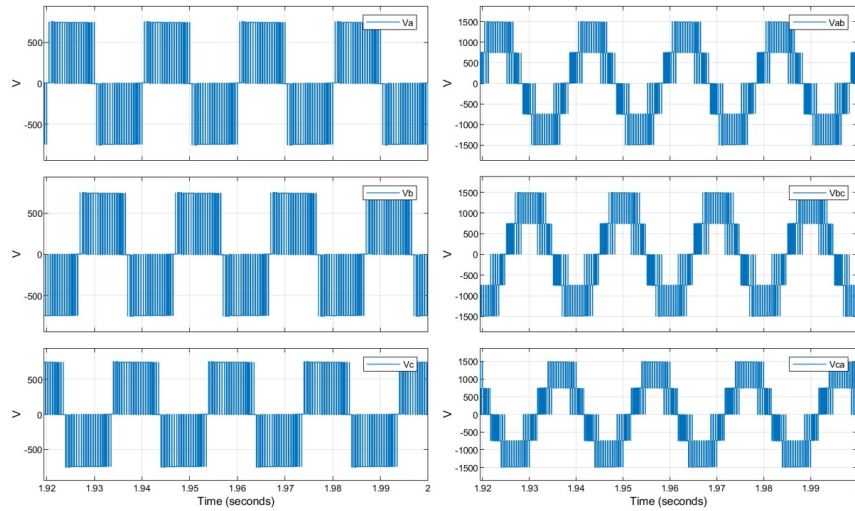
Figure 4-25: Phase and line-to-line voltages of 3-phase 3L-NPC converter

Power losses	IGBT S1,S4	IGBT S2, S3	d1, d2, d3, d4	D1, D2
Conduction losses	1.2852×2 kW	1.6188×2 kW	0.01221×4 kW	0.4491×2 kW
Switching losses	2.16×2 kW	2.16×2 kW	0.66×4 kW	0.624×2 kW

Table 4.7: Analytical calculation of average power losses of three-phase converter

Table 4.8, shows the average conduction power losses per cycle of the load fundamental frequency taken from the simulation of a three-phase three-level NPC converter and is simulated in a MATLAB/Simscape environment. Switching losses and DC-link

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losses are not considered. The values for the single phase are taken from Table 4.6 and values are multiplied by three because of the three-phase balanced star-connected load.

Power losses	IGBT S1,S4	IGBT S2, S3	d1, d2, d3, d4	D1, D2
Conduction losses	1.1604×2 kW	1.6806×2 kW	0.026394×4 kW	0.4812×2 kW

Table 4.8: Simulation results of average power losses of three-phase converter

The efficiency of the three-phase three-level NPC converter is calculated using the expression of calculating efficiency used in 3.4 and the same is used here and efficiency is calculated analytically as shown in Table 4.9. Table 4.10, depicts the efficiency of

Input Power (kW)	Total Power Losses (conduction) + (switching) (kW)	Output Power(kW)	Efficiency ($\eta\%$)
750	19.28	730.72	97.43

Table 4.9: Efficiency calculation by analytical method for 3L-NPC converter

the converter that is calculated using the simulation method in which the input and output average powers are taken over a one-cycle load frequency using the mean value from signal statistics.

Input Power (kW)	Total Power Losses (conduction) (kW)	Output Power(kW)	Efficiency ($\eta\%$)
750	6.75	731.3	97.51

Table 4.10: Efficiency calculation by simulation method for 3L-NPC converter

Table 4.10 shows that the conduction losses of the devices using the PWM technique explained in 4.3 reduce the conduction losses in the semiconductor devices. In this simulation, only conduction losses are considered. Simulation losses are neglected but it can be observed that the semiconductor devices used in the design of this three-phase converter have switching losses. If those switching losses and some of the losses of DC-link are neglected during the analysis and if both losses are added with these conduction losses, then it becomes 18.72 kW of losses in simulation.

The FFT analysis of the current I_a is done in MATLAB/Simulink environment and it is found that the output current has a total harmonic distortion (THD) of 12.98% without any filter design as in Fig. 4-26, which is better compared to a two-level inverter. The THD can be improved by introducing more inductance at the output or by introducing the filter at the output.
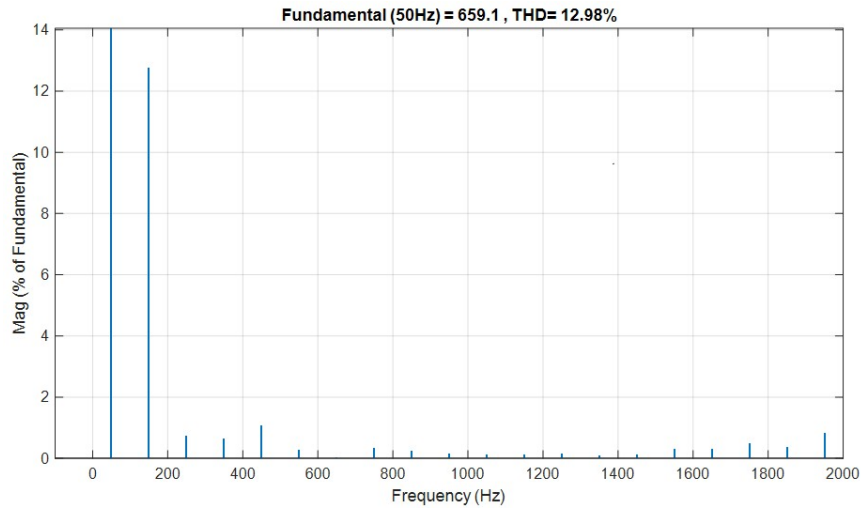
Figure 4-26: FFT and THD analysis of output current of phase (a) (750 kVA)

The efficiency and the FFT analysis are also analyzed for the 1.5 MVA design of a three-phase three-level NPC converter and it is summarized that in the design of 1.5 MVA, the average power losses per pulse obtained is 31 kW and the obtained efficiency is 97.93%. The FFT and THD analysis of the output current is also done in the MATLAB/Simulink platform and it is observed that the THD of the output current of phase (a) is 12.96% as shown in Fig. 4-27.
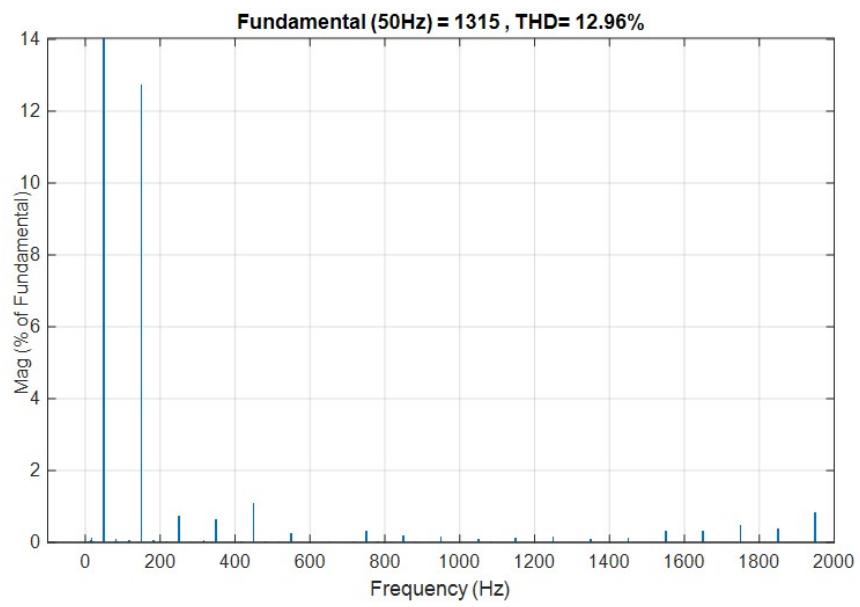
Figure 4-27: FFT and THD analysis of output current of phase (a) (1.5 MVA)

Chapter 5

Hardware design

In this chapter, the discussion about the hardware design of 750 kVA of single-phase three-level NPC converter is done. The discussion includes the selection of the semiconductor devices, the selection of commercial drivers, and controller board, the selection criteria for the DC-link capacitors, and the heat sink design to exit the power losses in the semiconductor devices of single-phase 3L-NPC converter to the environment.

5.1 Selection of IGBT power modules

The IGBT power modules are selected based on the voltage and current ratings that are most suited for the particular application [67]. In this design, it is selected based on the input voltage i.e., the DC-link capacitor voltage, and based on the peak output current.

5.1.1 Voltage rating

The voltage rating of the DC-link in the prototype design of a 750 kVA single-phase three-level NPC converter is 1500 Vdc. The DC-link of the NPC converter is mid-point divided and two capacitors are used for that reason, then the DC-link voltage is divided into $\left(\frac{V_{dc}}{2}\right)$, and the mid-point is called the neutral point. Table 5.1, shows

the voltage rating across the DC-link and the DC-link capacitors.

Parameter	Values
DC-link voltage VDC-link	1500 Vdc
Voltage across capacitor C1	750 Vdc
Voltage across capacitor C2	750 Vdc

Table 5.1: Voltage ratings of DC-link parameters

The voltage rating of IGBT power modules is selected based on the voltage across the individual capacitor of the DC-link i.e., 750 Vdc and it is recommended to select the voltage rating of the IGBT power modules 1.5 times more than the reference voltage i.e., the voltage across the individual capacitor. So, the selected IGBT power module has a voltage rating of 1.2 kV.

5.1.2 Current rating

The IGBT power modules are selected based on the peak output current. In this case, the output peak current is 2 kA, flowing through the output load for less than (1ms) and the selected IGBT power module has a peak current rating of 2.8 kA flowing for a while of 1ms. FF1400R12IP4 IGBT power module [64] model from Infineon Technologies is selected for this three-level converter design. Fig. 5-1 [68], shows the IGBT power module that is used in the hardware design.

5.1.3 Commercial gate drivers

Commercial gate driver boards are widely used for these types of IGBT power modules. The gate driver board selection depends upon the peak gate current, gate voltage, switching frequency, and switching protection functions so based on this information and recommended compatibility, the 2SD300C17A0 gate driver board model from CONCEPT is used. This driver board includes an isolated DC-DC converter, short-circuit protection, failure soft shutdown, short pulse suppression, and supply voltage monitoring setups for driving. This driver board can provide the gate

Figure 5-1: IGBT power module [68]

voltage swing of ±15, output current of 30 A, and 4 W drive power available per channel. It must be noted that this gate driver is a dual-channel driver used to drive the half-bridge IGBT module and can operate up to the switching frequency of 60 kHz [69]. This gate driver board can operate with a supply voltage of +15 V w.r.to ground. The block diagram of the driver core is shown in Fig. 5-2 [70].

The DSP controller model named (F28335) from Texas Instruments as shown in Fig. 5-3 [71] is used along with the gate driver board to control the PWM signals and can provide intelligent control, and precise, reliable, and efficient operation of IGBT power modules.

5.2 Selection of DC-link capacitors

The instantaneous power difference between the source and load is balanced by the DC-link capacitors, and they also minimize the voltage variations at the DC-link [72]. The voltage rating of the capacitor can be selected from 1.2 to 1.5 times more than the DC-link voltage, to account for the capacitor voltage ripple and supply voltage
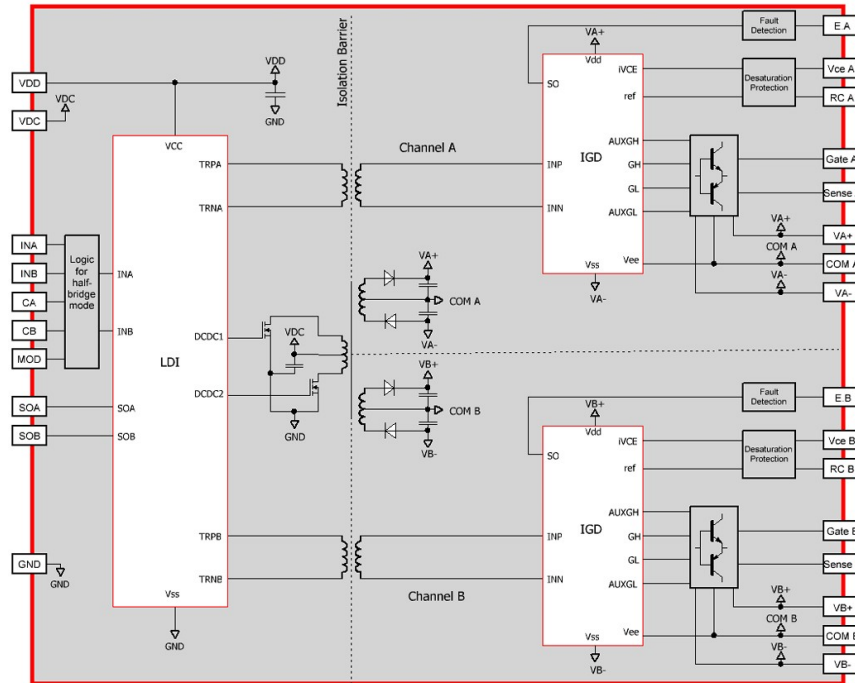
Figure 5-2: Commercial gate driver schematic [70]
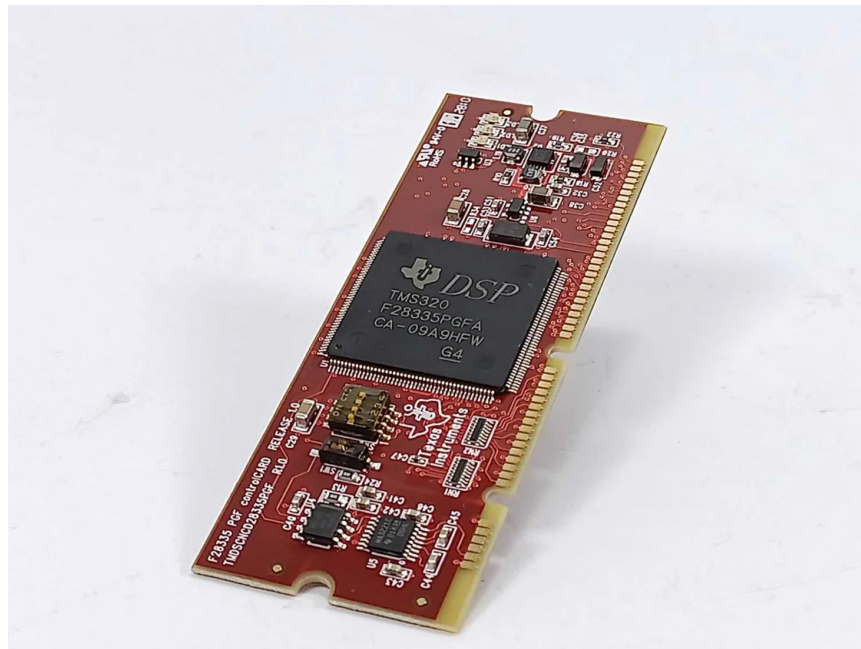
Figure 5-3: DSP controller board

surges [66]. DC-link capacitors can be selected considering the overall requirement of voltage, capacitance, and power losses the capacitor can be selected. The further analysis and sizing design are done in 4.2.

5.3　Heat sink design

The heat sink in power electronics is an important device used to provide a path to dissipate the heat generated by the power electronic components i.e., IGBTs, MOS-FETs, diodes, and other semiconductor devices during their operation. So, it is very crucial to design an effective heat sink to ensure the efficient and reliable operation of the power electronic devices taking into account performance, cost, and several other factors. It is important to note that the performance of the heat sink is impacted by the material selection so the higher the thermal conductivity of the material better the heat sink performance like copper and aluminum. The heat generated by the semiconductor devices during operation can be transferred to the environment through the assistance of heat sink by conduction, convection, and radiation methods.

IGBTs are widely used in different power electronic applications and this concerns about the thermal challenges created by the heat dissipation of IGBTs during the operation. Due to the increased heat losses in the IGBTs, thermal management and cooling solutions are a growing concern. These heat losses include the conduction and switching losses of the IGBTs, during the on-state voltage drop across the IGBT that depends upon the current conduction through it causes the conduction losses, and switching losses are caused by the on and off-state of the IGBTs and these losses strongly depends upon the duty cycle, current flowing, switching voltage, and switching frequency [73].

For the thermal design of the IGBT power modules, the application notes from SEMIKRON are used [74]. The thermal resistance of heat sink to ambient can be calculated by the modeling with the thermal equivalent circuit of IGBT modules including two IGBTs in a half-bridge manner as shown in Fig. 5-4. The thermal equivalent circuit modeling can be done in two different ways;

- A switch specific value $R_{\text{th(j-c)}}X$ + common $R_{\text{th(c-s)}}M$ for the complete module as shown in Fig. 5-5.

- The switch with specific values of $R_{\text{th(j-c)}}X$ and $R_{\text{th(c-s)}}X$ as depicted in Fig. 5-6.
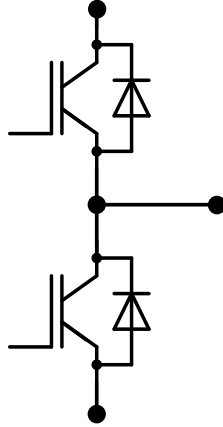
Figure 5-4: IGBT power module
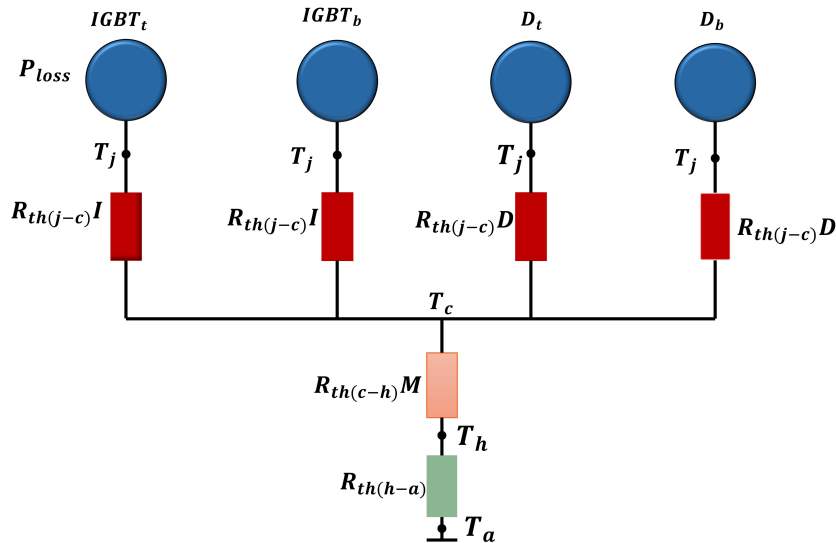
Figure 5-5: Thermal equivalent circuit with common $R_{\text{th(c-h)}}M$ per module

Fig. 5-7, shows the thermal equivalent model of the clamping diode used to calculate the heat sink to ambient thermal resistance.

Where IGBT_{t} and IGBT_{b} represent the top and the bottom IGBTs, D_{t} and D_{b} shows the top and bottom anti-parallel diode of top and bottom IGBTs respectively. $R_{\text{th(j-c)}}\text{I}$, $R_{\text{th(j-c)}}\text{D}$ represents the junction to case thermal resistance of IGBT and anti-parallel diode, $R_{\text{th(c-h)}}\text{I}$ and $R_{\text{th(c-h)}}\text{D}$ explains the case to heat sink thermal resistance of the IGBT and anti-parallel diode respectively. $R_{\text{th(c-h)}}M$ and $R_{\text{th(h-a)}}M$ represent the case to heat sink thermal resistance per module and heat sink to ambient thermal resistance respectively. T_{j}, T_{c}, T_{h}, and T_{a} shows the junction, case, heat sink, and
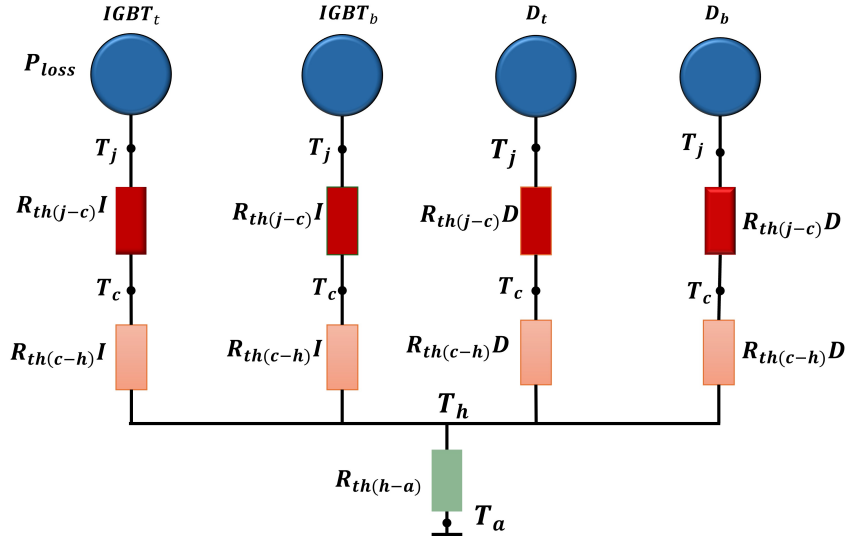
Figure 5-6: Thermal equivalent circuit with separate $R_{\text{th(c-h)}}X$
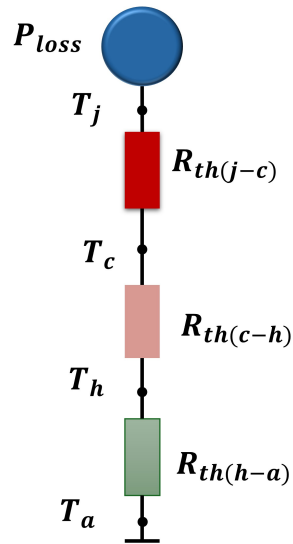
Figure 5-7: Thermal equivalent model of clamping diode

ambient temperatures respectively. The term P_{loss} represents the power losses occurring in the semiconductor devices during operation.

The following are the assumptions considered from the literature that ensure the safe, reliable, and efficient operation of the power electronic converter.

- Junction temperature $T_j = 125°C$

- Ambient temperature $T_a = 125°C$

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- Safety margin $\approx 25-50°C$

Table 5.2, shows the power losses of the semiconductor switches that occurred during the operation of a single-phase three-level NPC converter. For the conduction losses, the simulation results are considered from Table 3.17, and for the switching losses the analytically calculated values from Table 3.16 are considered for the 750 kVA power rating design of single-phase three-level NPC converter.

Power losses	IGBT S1,S4	IGBT S2, S3	d1, d2, d3, d4	D1, D2
Conduction losses	1.642×2 kW	2.292×2kW	0.01908×4 kW	0.539×2 kW
switching losses	0.72×2 kW	0.72×2 kW	0.22×4 kW	0.208×2 kW

Table 5.2: Analytical calculation of average power losses of devices

Table 5.3, represents the thermal resistances of the IGBTs and anti-parallel diodes taken from the datasheet used to calculate the equivalent heat sink to ambient thermal resistance.

IGBT module	$R_{th(j-c)}I$	$R_{th(c-h)}I$	$R_{th(j-c)}D$	$R_{th(c-h)}D$	$R_{th(c-h)}M$
Thermal resistance	19.5 K/kW	9.30 K/kW	36 K/kW	17 K/kW	3 K/kW

Table 5.3: Thermal resistance values of IGBTs and anti-parallel diodes

Equation 5.1, is used to calculate the heat sink to ambient thermal resistance for the design of the heat sink.

$$P_T = \frac{T_x - T_y}{R_{th}(x - y)} \tag{5.1}$$

where x and y belong to the junction to case, case to heat sink, and heat sink to ambient temperatures and thermal resistances respectively.

Using equation 5.1, the calculated heat sink to ambient thermal resistance is 2.02 K/kW. This heat sink to ambient thermal resistance is calculated by finding the heat sink to the ambient thermal resistance of each IGBT power module and then their parallel combination is done to get the minimum value of heat sink to ambient thermal resistance because the lower the thermal resistance better the performance and efficiency of the heat sink is to transfer the dissipated heat from devices to the environment. It is important here to note that for the hardware design, the anti-parallel diodes of the IGBT power module are used as clamping diodes because the

IGBT power module is connected at the place of clamping diodes and no switching signals are provided to those IGBTs and they remain open-circuited. The active heat sink i.e., air-forced heat sink is selected for the design of a 750 kVA single-phase three-level NPC converter. Fig. 5-8, shows the heat sink that is available to use for the design of a single-phase three-level NPC converter.

Figure 5-8: Active heat sink

Chapter 6

Experimental results

This chapter discusses the experimental results of the single-phase three-level NPC converter. In the first part, the testing of the IGBT power modules is discussed, followed by some results of the half-bridge inverter because the IGBT power module contains two IGBTs connected in a half-bridge manner for testing using RL load at the output. MATLAB code generation generates the PWM signals with a duty cycle and a dead band is kept between the switching transition of two IGBTs to avoid short circuits and modules are tested on low-voltage and low-current. The last part explains the hardware implementation and results of the single-phase three-level NPC converter.

6.1   IGBT power module testing

The IGBT power module testing is a preventive measure to ensure the module is safe, functional, and reliable for operation. This testing of IGBT modules is done with the multimeter by keeping it on the diode mode. The IGBT has three terminals i.e., gate, emitter, and collector. The first and foremost object of this testing is to short-circuit the gate-to-emitter of the IGBTs to ensure that electrostatic charges at the gate during the test do not conduct the current. The following two tests have been done to ensure the proper functioning of the IGBT modules.

IGBT power module test-01

Set the multimeter on the diode mode and carry out the following tests.

- Gate-to-emitter of both the IGBTs must be open lead (OL).

- Collector-to-emitter of any of IGBT in a module must be open lead (OL).

IGBT power module test-02

In this test, now reverse the leads of the multimeter and do the following tests.

- Emitter-to-collector of any of the IGBT reveals the voltage drop across the diode.

- Emitter of the second IGBT in a module to the collector of the first IGBT in a module shows double the voltage drop.

Hardware implementation and testing of IGBT power module

After the initial testing of the IGBT power modules as discussed in Test-01 and Test-02, the IGBT module is tested by operating it as a single-phase half-bridge inverter with the mid-point of the DC-link is connected with the load to ensure the proper functioning of the IGBT power module. Table 6.1, shows the design parameters for the testing of the IGBT power module, and the dead band between the transition of two IGBT switches is kept based on the recommendation of the datasheet of the gate driver as it is operating on the direct mode, not on the half-bridge mode of operation. Fig. 6-1, depicts the hardware implementation of the single-phase half-bridge inverter with RL load at the output. In the hardware, the three resistors each have a resistance of 10 Ω and are connected in parallel to reduce the equivalent resistance to pass the maximum current through it. The equivalent resistance is then connected with the inductor of having inductance of 1.1 mH in series. Fig. 6-2 and 6-3, show the output current i.e., I_L, and output voltage of the IGBT power module operating as a half-bridge (HB) inverter at a DC-link voltage of 26V with the modulation index of 1 respectively. The inductor has a maximum range of current to pass is 3 A and if the

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Parameter	Values
DC-link voltage ($V_{\text{dc-link}}$)	26 Vdc @ m = 1; 32 Vdc @ m = 0.5;
DC-link capacitance (C)	2.2 mF
Switching (carrier) frequency (f_{sw})	2 kHz
Load frequency (f)	50 Hz
Load impedance (Z)	3.35 Ω
Power factor (Pf)	0.99
Modulation index (m)	0.5 and 1
Dead band	6.5 µs

Table 6.1: Design parameters
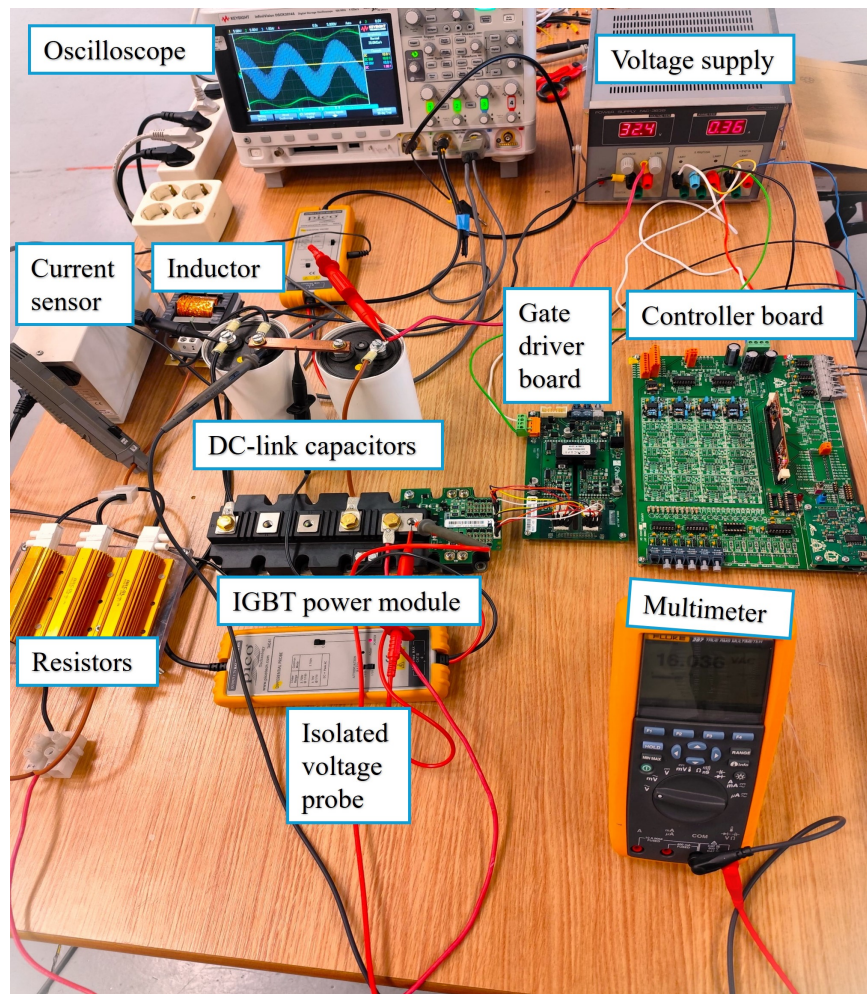
Figure 6-1: Hardware implementation of single-phase HB inverter

current increases more it saturates so maximum current is passed through it.

In Fig. 6-3, it can be seen that the output voltage seems sinusoidal but it should not

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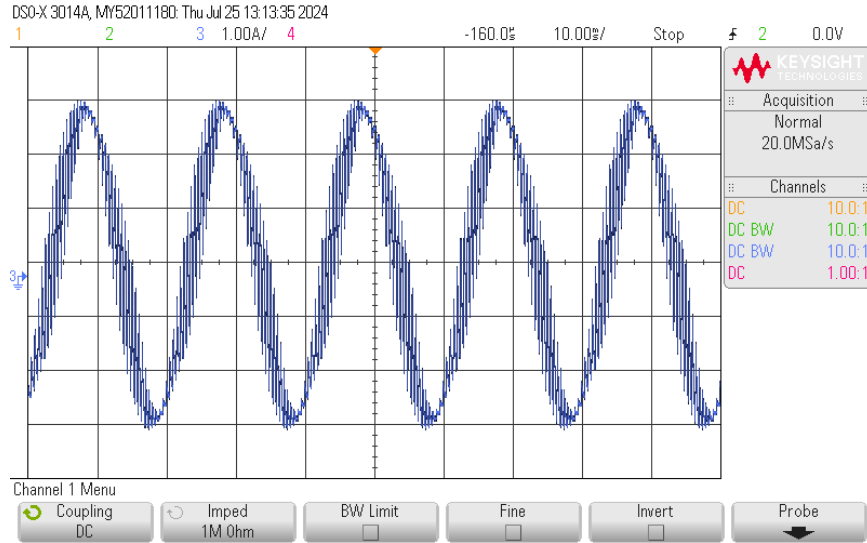
Figure 6-2: Output load current of single-phase HB inverter
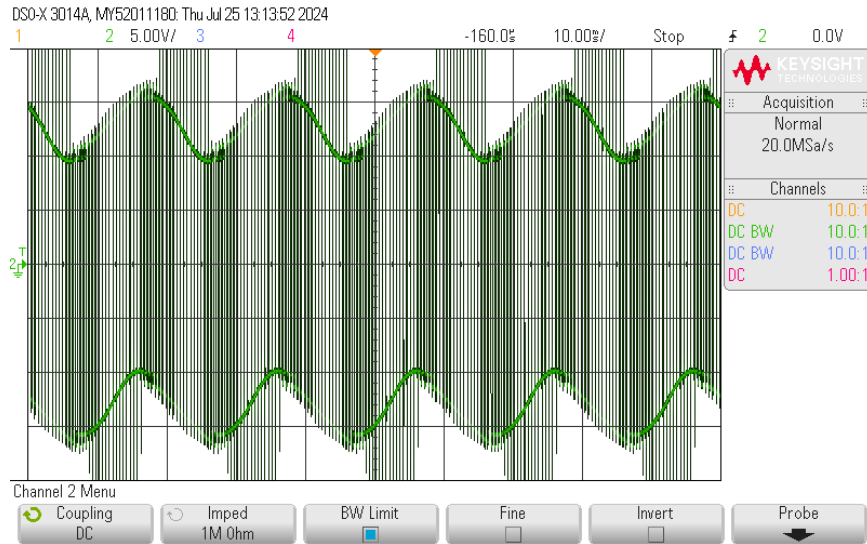
Figure 6-3: Output voltage of single-phase HB inverter

be sinusoidal this happens because the DC-link voltage is not constant. The voltage ripple across the DC-link capacitors can be shown in Fig. 6-4.
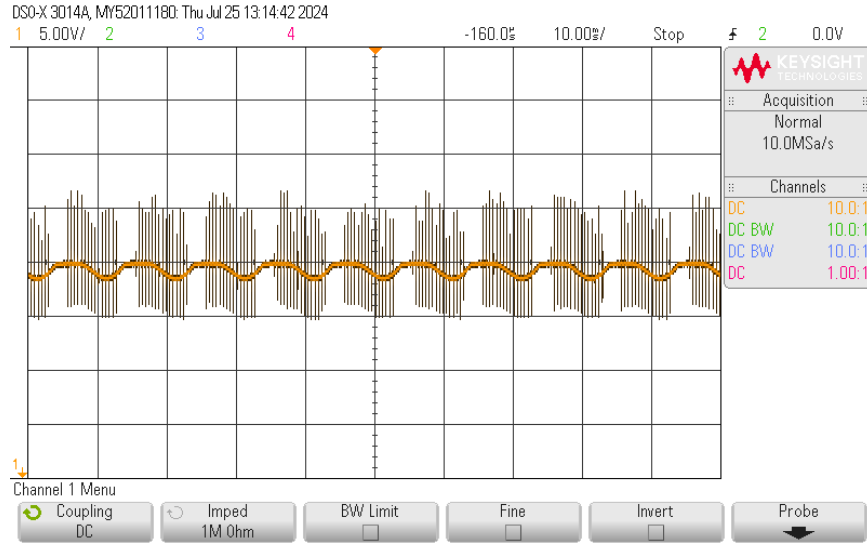
Figure 6-4: Voltage ripple across DC-link capacitors

6.2 Hardware implementation of single-phase 3L-NPC converter

In this section, the hardware design of the single-phase three-level NPC converter explained in 3.1 is implemented. The experimental setup of the hardware design of the three-level converter is shown in Fig. 6-5, where the scaled-down version of the DC-link capacitors is used because of the availability and the main design of the DC-link capacitors and their analysis will be explained in the future work design of three-phase three-level NPC converter. In this design, the battery is used as input voltage supply to the DC-link the rotor windings of the induction motor are used as inductive load and the resistive load is used as in Fig. 6-5. It must be noted that the controller board is operating at +5 V, +15 V, and -15 V w.r.to. ground and two individual sources are used to operate the controller board. The driver boards are operating at +15 V w.r.to. ground which makes the voltage level of the PWM signals to ±15 V. It must be noted that the IGBT turned on at a gate-to-emitter voltage of +15 V and turned off at a gate-to-emitter voltage of -15 V supplied by the gate drivers. The driver boards are operating on the direct mode of operation so the dead band between the switching of two IGBTs is kept the same and is used for

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the testing of the IGBT power module as a single-phase half-bridge inverter that is 6.5 μs. The single-phase leg of the three-phase diode rectifier model UVO 62-12NO7 is used as the clamping diodes because of the availability for the initial testing of the converter design with reverse recovery voltage of 800-1800 V and average current of 63-88 A [75].
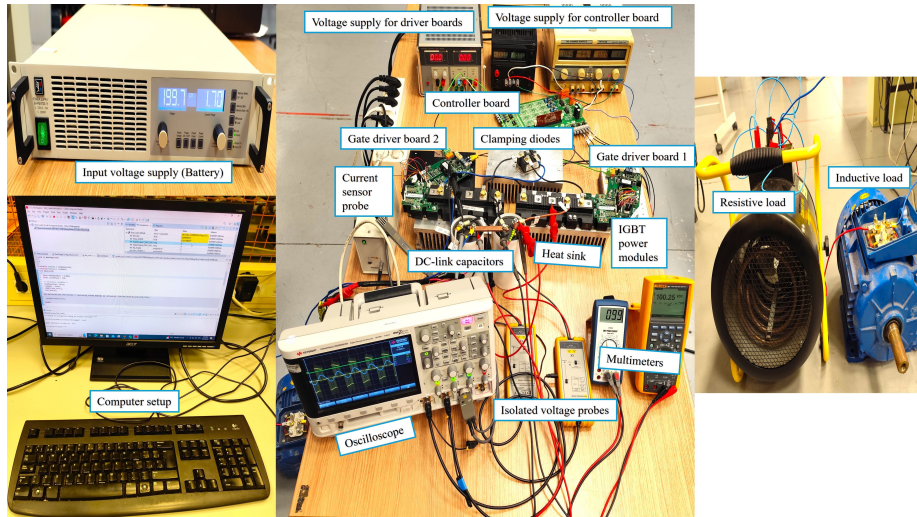
Figure 6-5: Experimental setup of single-phase 3L-NPC converter

6.2.1 POD-PWM technique implementation

The phase opposition disposition pulse width modulation technique explained in 3.1.3 is implemented using the MATLAB code generation platform. The simulation setup of the POD-PWM technique implementation is shown in Fig. 6-6.
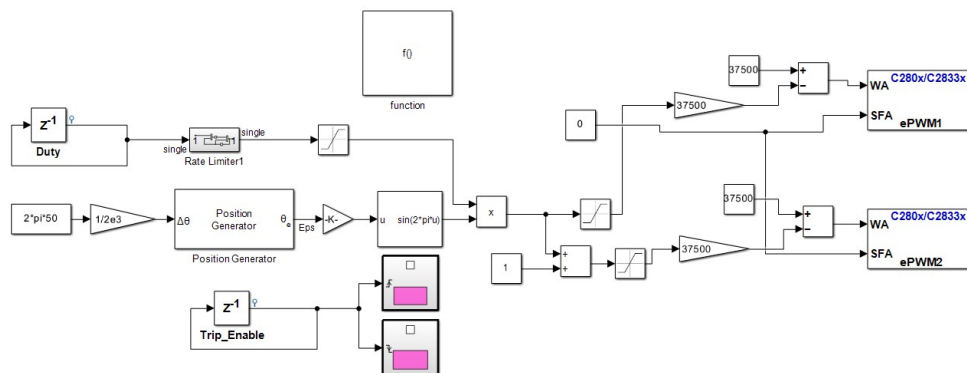
Figure 6-6: POD-PWM implementation using MATLAB code generation

It is important to recall here that in the 3L-NPC converter, the power switches S3 and S4 are the complementary switches of S1 and S2 respectively so the IGBT gate signals for the switches S1 and S2 are shown in Fig. 6-7, and the IGBT gate signals for S3 and S4 are going to be complementary of these two switches.
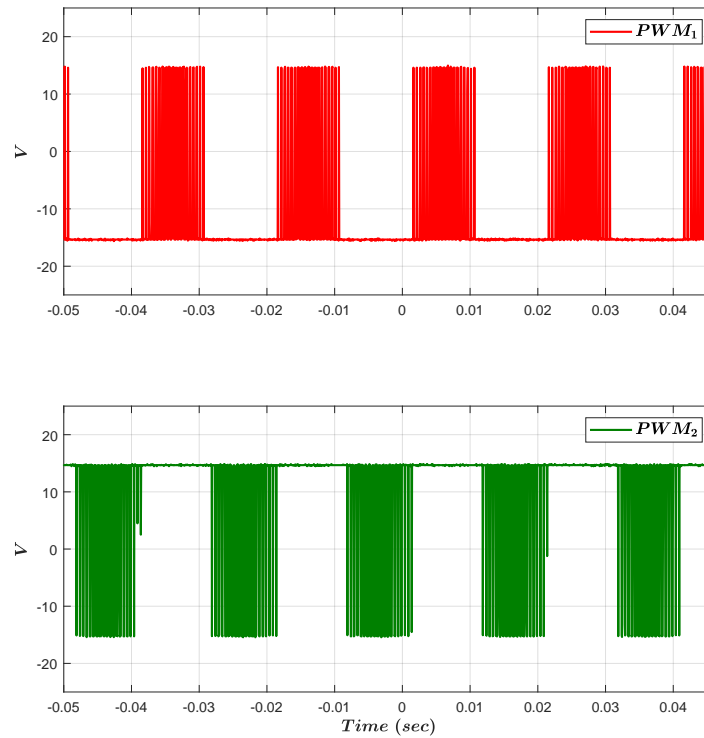
Figure 6-7: IGBT gate signals for switches S1 and S2

6.3   Experimental results

The initial two tests on low-power operation are done on the implemented hardware design of a 750 kVA single-phase 3L-NPC converter to ensure the safe and reliable operation of the design and in both tests, the RL load is used.

Experiment#01

In the first experiment of the hardware design, the series combination of the RL load is used with a parallel combination of two resistors each of value 33.5 Ω connected in series with one rotor winding of the motor having an inductance of 17.5 mH with a

small DC resistance of 1.5 Ω. Table 6.2, shows the experiment parameters, average input, and average output power, and the efficiency based on the test.

Parameter	Value
DC-link voltage ($V_{\text{dc-link}}$)	500 V_{dc}
DC-link capacitance (C)	2.2 mF
Switching frequency (f_{sw})	2 kHz
Load frequency (f)	50 Hz
Load impedance ($Z = R + jX_L$)	19 Ω
Power factor (Pf)	0.96
Modulation index (m)	0.8
Dead band	6.5 µs
Average input power (P_{in})	1.045 kW
Average output power (P_{out})	1.010 kW
Efficiency ($n\%$)	96.7%

Table 6.2: Experiment# 01 parameters

When the DC-link is supplied with a voltage of 500 volts then using parameters mentioned in Table 6.2, the three-level output voltage (V_{out}), DC-link voltage ($V_{\text{dc-link}}$), output current (I_L), and the output power (P_{out}) are shown in Fig. 6-8. It is important to note here that the DC-link capacitors used are the scaled-down version of the main design which is our future design of the three-phase three-level NPC converter hardware and the ripple voltage of the DC-link is 18V which is 3.6% of the DC-bus voltage.

Experiment# 02

In this experiment, the power range is doubled compared to experiment-01 with increased power factor and modulation index as shown in Table 6.3. In this experiment, three resistors are connected in parallel each of 33.5 Ω, and the equivalent of their parallel combination is connected in series with the equivalent parallel combination of two rotor windings each of inductance 17.5 mH with the series resistance of 1.5 Ω is used as the output RL load. Table 6.3, depicts the parameters for the experiment-02.

Fig. 6-9, shows the experiment-02 hardware results of the three-level output voltage (V_{out}) , DC-link voltage ($V_{\text{dc-link}}$), output current (I_L), and the output power (P_{out})
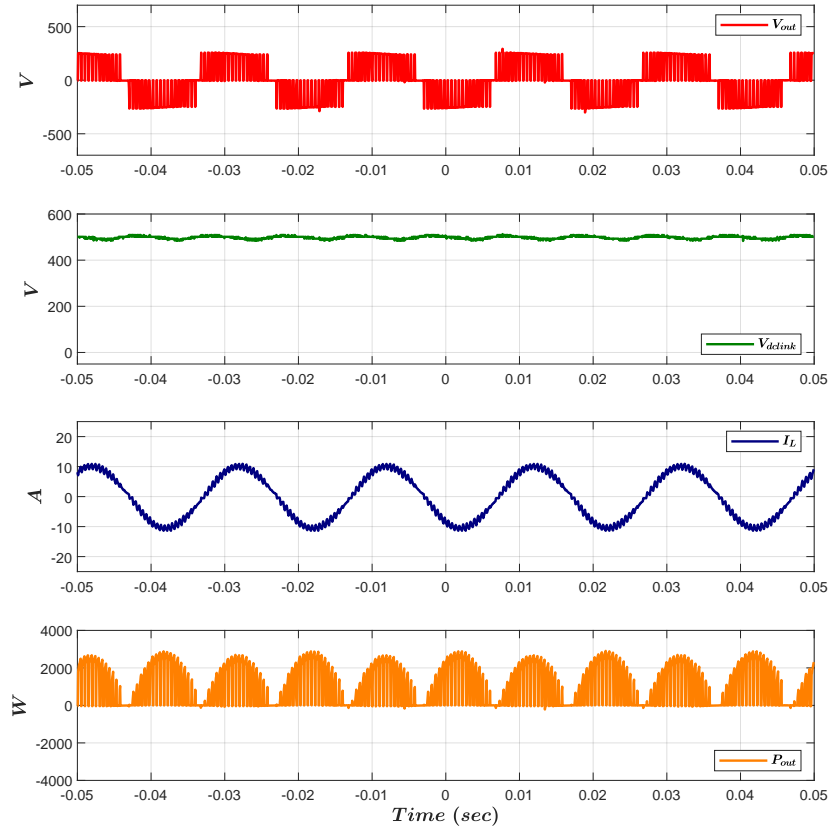
Figure 6-8: Hardware results of experiment# 01

Parameter	Value
DC-link voltage ($V_{\text{dc-link}}$)	500 V_{dc}
DC-link capacitance (C)	2.2 mF
Switching frequency (f_{sw})	2 kHz
Load frequency (f)	50 Hz
Load impedance ($Z = R + jX_L$)	12.067 Ω
Power factor (Pf)	0.97
Modulation index (m)	0.9
Dead band	6.5 µs
Average input power (P_{in})	2.09 kW
Average output power (P_{out})	2.045 kW
Efficiency ($n\%$)	97.84%

Table 6.3: Experiment# 02 parameters

based on the testing parameters in Table 6.3.

It can be seen from the figure that the DC-link ripple voltage is increased to 22V which is 4.4% of the DC-bus voltage because of the change in the active power of

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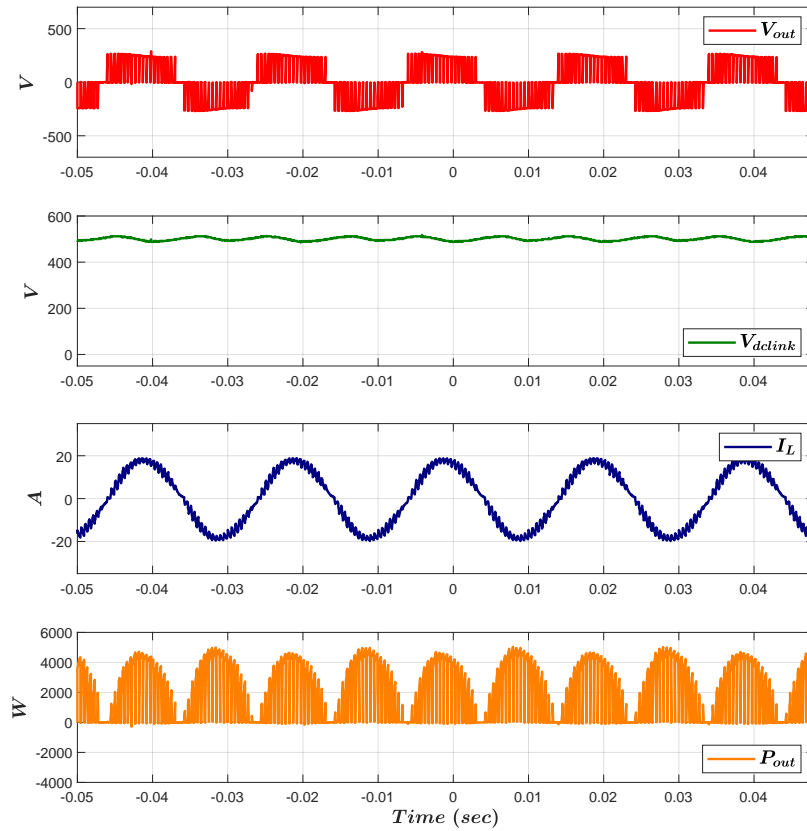
Figure 6-9: Hardware results of experiment# 02

the system because of the change in the output load. It was also analyzed in the analysis of the DC-link capacitor sizing in chapter-3 and chapter-4 that the voltage ripple changes by changing the power factor of the system that means by changing the active power of the system the voltage ripple of the DC-link and DC-link capacitors can be changed.

Chapter 7

Conclusion and future recommendations

7.1 Conclusion

The conventional two-level voltage source converters (2L-VSCs) reflect the problems of high dv/dt due to the synchronous commutation of series devices, static and dynamic voltage sharing of series devices, and provide the high switching frequency harmonic content in converter output voltage in the design of medium-voltage and high-power stack design. To, eliminate these issues in the design of medium-voltage and high-power stacks multilevel converters are used. Moreover, in multilevel converters research started from the three-level voltage source converters and 3L-VSCs offered promising results by reducing high dv/dt issues due to synchronous commutation and providing better harmonic content.

In this research-based thesis project, the the 3L-NPC and 3L-NPP converter topologies are selected from the state-of-art three-level converter topologies, and comparative analysis based on power losses, efficiency, and cost-effectiveness is made the part of initial study to select the more reliable and high-efficient topology among the two converter topologies. For the comparative analysis, the simulation of single-phase 3L-NPC and 3L-NPP converter is done using the MATLAB/Simscape software, and the simulation results are compared with the analytically calculated results and it is

observed that at the design on 750 kVA power stack, the 3L-NPC converter provides low average losses with the efficiency of 98.25% using analytical results and 98.38% using the simulation results and the 3L-NPP depicts 98.07% and 98.26% using analytical and simulation results respectively. So, the 3L-NPC converter topology is selected for the final design because of the interest of the company due to its high efficiency for the high-voltage high-current three-level power stack. The DC-link capacitor sizing and analysis are done on the different load conditions and it is analyzed that with the DC-link voltage of 1500 V, the DC-link capacitors provide a voltage ripple that is less than 5% and that percentage is recommended from the literature for the medium-voltage DC-link capacitor sizing and 12mF DC-link capacitance is suggested for the 1.5MVA power stack design. The 750 kVA and 1.5 MVA three-phase 3L-NPC converter is simulated through MATLAB/Simscape and power loss and efficiency analysis has been performed. The heat sink is designed for the prototype design of 750 kVA to satisfy the thermal behavior of the power stack.

The 750 kVA power stack prototype using single-phase 3L-NPC is designed using IGBT power modules (FF1400R12IP4 model) from Infineon company, and the compatible gate drivers from CONCEPT model 2SD300C17A0 are selected to provide the gate pulses to trigger on and off the IGBT modules. The MATLAB code generation is used to implement the POD-PWM technique and the DSP controller model F28335 from Texas Instruments is used to control the PWM signals. The initial experiments of the prototype are tested on low power because of the availability of the load and devices and two experiments are tested on 1.045 kW and 2.09 kW with a modulation index of 0.8 and 0.9 at a high power factor of 0.96 and 0.97 and the results depict the efficiencies of 96.7% and 97.84% respectively. For these types of converters, when they operate at 80% of power, then they show maximum efficiency.

7.2   Future recommendations

This project can be used as a base to execute the following objectives on this project.

- Design of the DC-link, its optimization, and mechanical design of the DC bus

bar.

- Design of the coupling capacitors in case DC-link is not implemented on the IGBT power modules.

- Design of the voltage sensors and temperature sensors for the DC-link capacitors voltage tracking and thermal evaluation of the IGBT modules during operation.

- Evaluation of the power losses by considering the losses of the DC-link and ESR losses of the capacitors.

- Testing of the single-leg power stack at 750 kVA with modulation index of 0.9 and power factor of 0.85 required by the company.

- The heat sink and prototype design of a 1.5 MVA three-phase power stack using a three-phase three-level NPC converter and its final testing.

- The efficiency of the power stack will be increased to 98.38% when this power stack is operating at 80-85% of the 750 kVA for which it is designed and can be analyzed.

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