Closed Loop Modular Topology to Interface Removable Batteries in an Electric Powertrain With 400 V and 800 V Compatibility

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***Abstract*— To improve the adaptability of electric vehicle (EV) energy management, the inclusion of a removable battery is identified as an alternative method. This option is compatible with both the extensively used 400 V bus standard and the emerging 800 V standard. This paper introduces a flexible topology capable of linking a removable battery to both the 400 V and 800 V buses. The modular topology is based on two DABs connected in Input Parallel Output Series (IPOS) connection, adapting to the possible standard buses without external switches. The primary focus of the research is on the control loops needed to regulate the power supplied by the removable battery to the DC bus. Simulation and experimental results validate the effectiveness of the designed controllers under stability criteria.**

Keywords*— DC-DC converter, dual active bridge, electrical vehicles, reconfigurable topology, removable battery.

I. INTRODUCTION

In recent years, electric vehicles (EVs) have received significant attention as a sustainable transportation solution, with a key focus on improving energy management systems to optimize performance [1,2]. A fundamental component of the energy system in the EV is the on-board battery, which is responsible for storing and supplying energy for both the propulsion system and the auxiliary systems. Battery capacity and technology play crucial roles in overall performance, which can be enhanced by incorporating removable batteries connected to the DC bus, as depicted in Fig. 1, providing greater operational flexibility and potential weight reduction by supplementing the main battery to accommodate varying power demands and driving conditions [3,4].

In [5] a reconfigurable topology is introduced to connect removable batteries to the DC bus. The proposed topology can be adjusted to both 400 V and 800 V buses, in accordance with industry standards. The fundamental unit of the topology is the dual active bridge (DAB) converter, which is well-known for its efficiency and control capabilities [6]. The structure of the DAB converter is shown in Fig. 2. To ensure optimal performance and compatibility with various bus DC voltage standards, a modular approach is adopted, requiring series or parallel connections between DAB converters. When the input voltage is significantly lower than the output voltage, it is advantageous to connect the modules in parallel and modify the output connection according to the DC bus standard [7]. For the 400 V standard, the Input Parallel Output Parallel (IPOP) configuration is suitable, while for the 800 V standard, the use of the Input Parallel Output Series (IPOS) configuration is recommended [8]. The modular topology presented in [5] is based on IPOS connection for both the 400 V and 800 V standards, as shown in Fig. 3. In the low-voltage scenario, DAB1 handles all the power, while DAB2 only

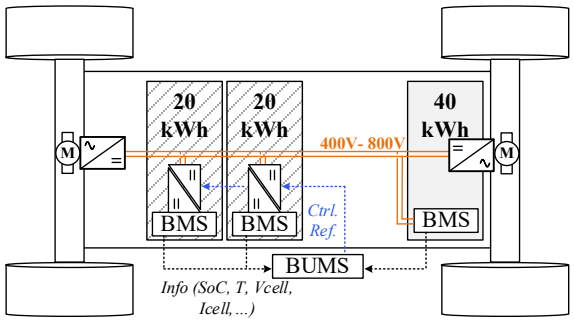


Fig. 1. EV Power system with multiple batteries.

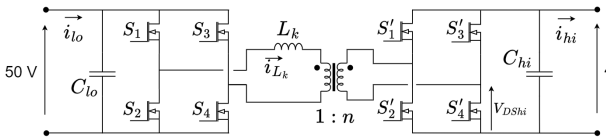


Fig. 2. Structure of the DAB converter.

allows current to pass through it (see Fig. 3(a)). To achieve DAB2 operation, the high-side MOSFETs are permanently in the ON state, while the low-side bridge MOSFETs are permanently in the OFF state. In the high-voltage scenario, both DAB converters operate, each processing a portion of the total power (Fig. 3(b)). Both DABs are designed to operate with voltages on the low side of 50 V and on the high side of 400 V. This modular topology offers several advantages [5]:

- Adaptability to different DC bus standards: the modular approach allows for the connection of a removable battery to both 400 V and 800 V buses.
- Seamless and highly efficient reconfiguration: the topology reconfiguration according the DC bus voltage standard can be effectively managed without external elements.
- Galvanic isolation and bidirectional operation: The DAB converter provides galvanic isolation and bidirectional operation, essential features for energy management in electric vehicles.
- Key benefits of modular topologies: flexibility, scalability, and cost efficiency, enhancing system reliability, performance, and ease of maintenance.

To ensure the proper functioning of the modular topology under different operating conditions, a robust control strategy is crucial. In series-parallel or parallel-series systems, a key challenge is to guarantee proper voltage distribution at the series ports and current distribution at the parallel ports among the individual modules [9]. The DAB converter, which is the

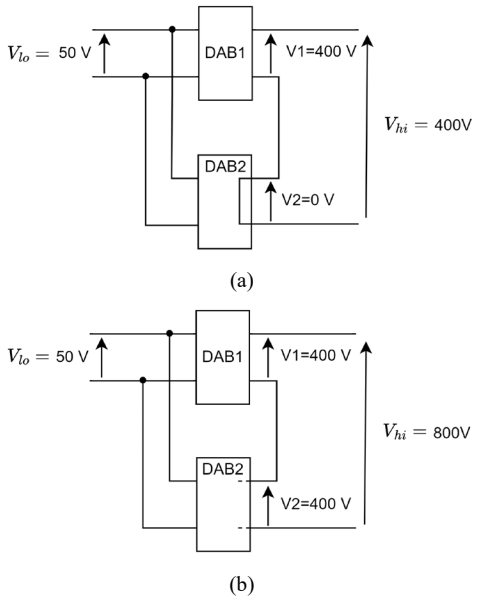


Fig. 3. Modular topologies and configurations for standard bus DC voltages: a) 400 V standard, b) 800 V standard.

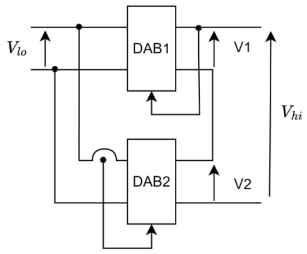


Fig. 4. Description of feedback variables for the control strategy.

fundamental unit of the proposed reconfigurable topology, presents a current source characteristic. This property is very useful in parallel systems, but not in series connections. In the series connection of DABs, a common duty cycle (control variable) can lead to unstable operation, requiring a special approach to achieve voltage sharing [10]. The mathematical study of two DABs in series configuration either at the input or output port leads to equations that depend on both control variables. A possible control strategy consists of applying a decoupling technique and then a PI compensator [11]-[13].

The significant contribution of this paper lies in the design of voltage and current control loops. The proposed modular topology can be configured in two ways, each with distinct control requirements. In the first configuration, the low-voltage scenario (Fig. 3(a)), a single DAB manages all the power, requiring only a current control loop. In the second configuration, the high-voltage scenario (Fig. 3(b)), two DABs share the power, requiring a voltage-sharing strategy and power control. The proposed control strategy involves independently designed voltage and current loops, the current loop operating much faster than the voltage loop. In the first configuration, only the current control is applied, whereas in the second configuration, both independently designed control loops are integrated for proper operation. The structure of the paper is organized as follows. Section II presents the design metodology for voltage and current controllers. The experimental results for the voltage and current control loops are discussed in Section III. Finally, conclusions are presented in Section IV.

II. CONTROL LOOP DESIGN

The control strategy involves independent regulation of voltage and current. DAB1 is responsible for voltage control, while DAB2 regulates the current, as shown in Fig. 4. The voltage reference for DAB1 is defined as half of the bus voltage. Basically, the voltage reference for DAB2 is the difference between the bus voltage and the reference for DAB1.

A possible method for designing the voltage and current loops is based on the study of the averaged model of the DAB. Here, the behavior of the converter is replaced by that of a quadripole, primarily composed of two nonlinear current sources and an ideal transformer [14]. These current sources must behave in the same manner as the average value of the currents they replace. $\bar{i}_{lo}$ is the average current on the low voltage side of the converter, while $\bar{i}_{hi}$ is the average current on the high voltage side.

These expressions are shown below:

$$\bar{i}_{lo} = \frac{(1-d)dTv_{hi}}{nL_k}, \tag{1}$$

$$\bar{i}_{hi} = \frac{(1-d)dTv_{lo}}{nL_k}, \tag{2}$$

where T is half the switching period and d is the duty cycle of the converter calculated as $d = t_c/T$ where t_c corresponds to the interval where a positive voltage is applied to the inductance L_k as shown in Fig. 5.

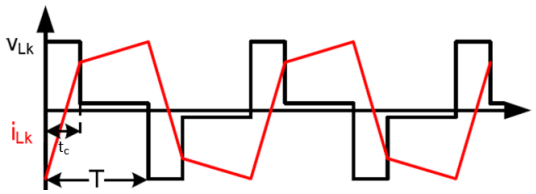


Fig. 5. Current i_{lk} and voltage due to inductance v_{lk} on DAB converter [15].

The first step in the dynamic modeling of the DAB is to obtain the nonlinear averaged model. Then, this model is linearized at an operating point by perturbing the input variables. In this case, the input variables are the duty cycle (d) and the voltages at the input and/or output ports (v_{lo}, v_{hi}). Regarding the notation, for example, $\hat{d}$ represents the perturbation of the instantaneous variable, while D is the value of (d) at the operating point. The small-signal model equations can be derived from the analysis of the averaged model shown in the circuit of Fig. 6. Equations (3) and (4) allow the study of the dynamics of the input and output currents [14]. The corresponding small-signal model is presented in Fig. 7.

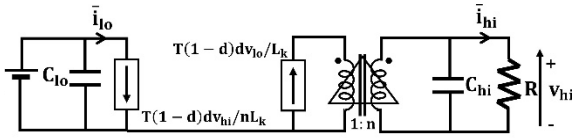


Fig. 6. DAB Converter Average Model.

$$\hat{\imath}_{hi} = \left.\frac{\partial i_{hi}}{\partial d}\right|_o \hat{d} + \left.\frac{\partial i_{hi}}{\partial v_{lo}}\right|_o \hat{v}_{lo} = g_{od}\hat{d} + g_{ov_{lo}}\hat{v}_{lo}\,, \tag{3}$$

$$\hat{\imath}_{lo} = \left.\frac{\partial i_{lo}}{\partial d}\right|_o \hat{d} + \left.\frac{\partial i_{lo}}{\partial v_{hi}}\right|_o \hat{v}_{hi} = g_{id}\hat{d} + g_{iv_{hi}}\hat{v}_{hi}\,, \qquad (4)$$

Where:

$$g_{od} = \frac{V_{hi}(1-2D)}{(1-D)DR}\,, \qquad (5)$$

$$g_{ov_{lo}} = \frac{V_{hi}}{V_{lo}R}\,, \qquad (6)$$

$$g_{id} = \frac{V_{hi}^2(1-2D)}{V_{lo}(1-D)DR} = \frac{V_{hi}}{V_{lo}g_{od}}\,, \qquad (7)$$

$$g_{iv_{hi}} = \frac{V_{hi}}{V_{lo}R}\,, \qquad (8)$$

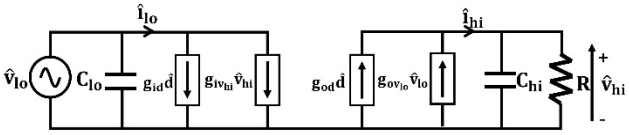


Fig. 7. DAB converter small signal circuit.

Voltage and current control loops are calculated to implement the IPOS configuration. A systematic procedure, employing a Matlab spreadsheet is followed in both cases, and the results are subsequently validated using PSIM software. The controller has been designed considering a scale prototype with voltages $V_{lo} = 10\,V$ and $V_{hi} = 80\,V$. Additionally, a resistance has been placed at the output port instead of a voltage source, as seen in the equivalent circuits in Fig. 6 and Fig. 7.

A. Voltage Loop

From expressions (3) and (4) we can represent the voltage variations on the high side, as a function of the variations in the duty cycle and the voltage on the low side:

$$\hat{v}_{hi} = \frac{R}{RCs+1}\cdot\left(g_{od}\hat{d} + g_{ov_{lo}}\hat{v}_{lo}\right), \qquad (9)$$

The low voltage side variation is going to be always slower when compared with duty cycle, which is employed as the feedback action. Therefore v_{lo}, is assumed as constant and removed from (9).

$$\frac{\hat{v}_{hi}}{\hat{d}} = \frac{V_{hi}(1-2D)}{(1-D)DR}\cdot\frac{R}{RCs+1}\,, \qquad (10)$$

The resulting expression is a first-order function with a pole in the negative half-plane. Fig. 8 shows the Bode diagram of the resulting transfer function, discretized at a frequency of $f_s = 100\,kHz$. Given that the DAB converter has inherent stability under normal operating conditions, a relatively simple control using an integrator is proposed.

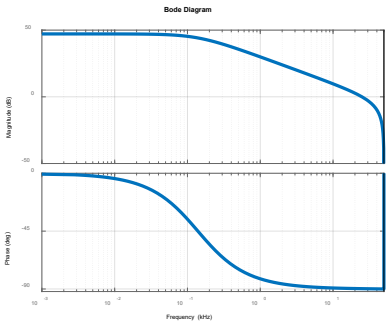


Fig. 8. Bode diagram of the voltage loop function.

Fig. 9 presents the block diagram of the control loop for the DAB converter. The control loop includes components such as controller (H_{PWM}), compensator ($C(z)$), feedback sensor and analog to digital converter ($H_{ADC} \cdot H_{sens}$), and DAB converter plant ($G(z)$) shown on Table I.

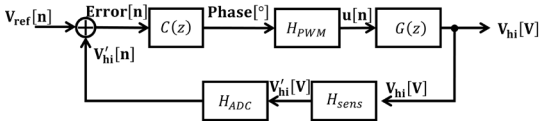


Fig. 9. Block diagram of voltage loop implementation.

TABLE I. MAIN PARAMETERS OF THE VOLTAGE LOOP

Parameter	Value
H_{PWM}	373.7678
H_{ADC}	$9.7752 \cdot 10^{-4}$
H_{sens}	$5.2 \cdot 10^{-3}$

The proposed controller to achieve a fast and overdamped response corresponds to equation (11). Its operation has been validated in PSIM through a step change in the voltage reference, as shown in Fig. 10.

$$C(z) = \frac{100}{(z-1)} \qquad (11)$$

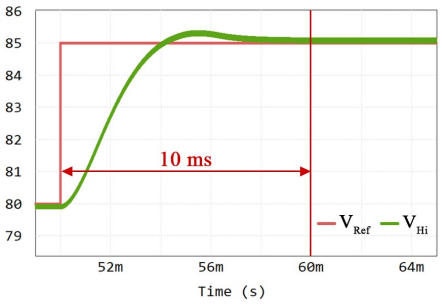


Fig. 10. Validation of the proposed voltage controller using PSIM.

As observed in Fig. 10, with a 5 V increase in the high-bridge voltage, the settling time is 10 ms, and the system exhibits an overdamped response.

B. Current Loop

In the design of the current loop and its subsequent validation in an independent DAB, measurements of current on the low voltage side were considered, where the converter had implemented the sensor with its corresponding conditioning circuit. The expression for the low-side current variation (4) is ideally instantaneous to variations in the duty cycle (control variable), suggesting that ideally, a change in the control variable produces an instantaneous change in current. Therefore, an integrator is chosen to control the current loop, similar to the approach used in the voltage loop.

However, a response 10 times faster is chosen for the current loop than for the voltage loop, considering that the dynamic characteristic is equivalent to double-loop control, where the inner current loop operates much faster than the outer voltage loop. Consequently, the regulator response calculated using Matlab for the current loop (12):

$$C(z) = \frac{800}{(z-1)}, \tag{12}$$

As in the previous case, the block diagram that represents the dynamic behavior of the converter is shown in Fig. 11.

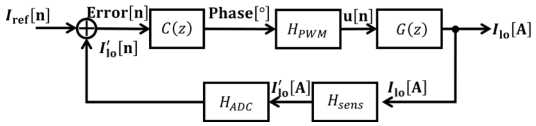


Fig. 11. Block diagram of current loop implementation

Since the same FPGA is used for control, the only value that changes with respect to the voltage loop is the current sensor gain, as shown in Table II.

TABLE II. MAIN PARAMETERS OF THE VOLTAGE LOOP

Parameter	Value
H_{PWM}	373.7678
H_{ADC}	$9.7752 \cdot 10^{-4}$
H_{sens}	0.4

In the Fig. 12 presents simulation results obtained in PSIM. It can be observed that for a 500 mA variation in the current reference, the settling time of the converter is approximately 1.5 ms. The results demonstrate the effectiveness of the control loop, bringing us as close as possible to potential experimental outcomes.

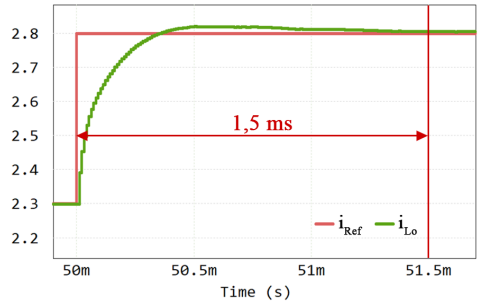


Fig. 12. Validation of the proposed current controller using PSIM.

C. IPOS Configuration

The use of control techniques in the IPOS configuration, where one of the DAB converters implements a current loop and the other a voltage loop, offers significant advantages in terms of system performance and robustness. This configuration allows for the support of high output voltages with lower voltage devices.

Implementing control of a DAB in IPOS requires decoupling techniques in certain cases, as discussed in [12]. This work proposes the use of two loops designed independently as outlined in the previous section: a current loop significantly faster than the voltage loop. Next, the effectiveness of this approach will be explored despite the coupling in the control actions reported in [12].

The converter with a current loop ensures balanced loading and a rapid response to fluctuations in the output current, while the converter with a voltage loop is responsible for maintaining a stable output voltage and distributing the output voltage between the two DABs. As shown in Fig. 4, DAB1 is controlled in voltage, while DAB2 is controlled in current. Fig. 13 shows the dynamic response of the proposed topology in IPOS connection, with voltage source on both sides, obtained in the PSIM software. The voltages on the high side of DAB1 and DAB2 are $V_{Hi-DAB1}$ and $V_{Hi-DAB2}$ respectively, and the corresponding currents in the leakage inductance are $i_{L_{k-DAB1}}$ for DAB1 and $i_{L_{k-DAB2}}$ for DAB2.

In the first part of the simulation ($t < 50\,ms$), both converters operate with a low-side voltage of 10 V and a high-side voltage of 80 V. The total series connection voltage is 160 V. At $t = 50\,ms$, the reference voltage of DAB1 is increased by 5 V (its new reference is 85 V).

The system reaches steady state 40 ms later. The final voltage values of DAB1 and DAB2 are 85 V and 75 V respectively, maintaining the voltage of the series connection constant at 160 V. Figure 13 also shows that the change in voltage reference produces changes in the current of the leakage inductance. DAB2 keeps its current constant, while DAB1 exhibits a slight increase. This increase is to maintain the system power constant.

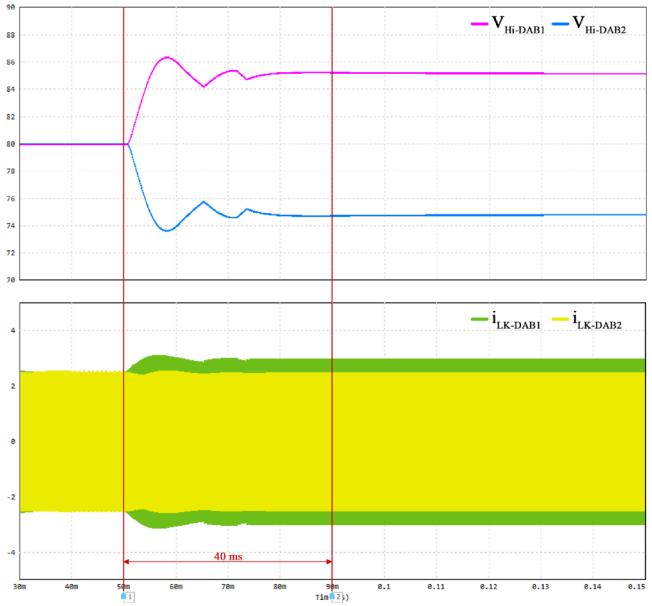


Fig. 13. Simulation of a voltage step in IPOS in PSIM.

III. EXPERIMENTAL RESULTS

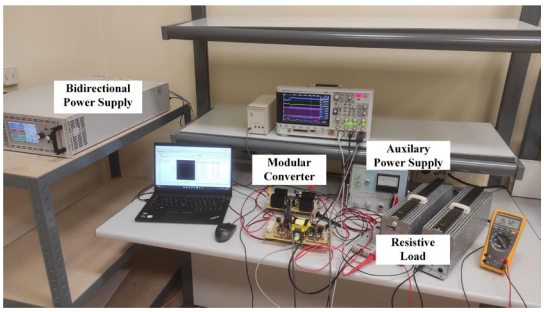
The theoretical results are now being experimentally validated. Two DAB units (DAB1 and DAB2) are used, each rated at 500 W, as shown in Fig. 14. These DABs exhibit slight construction differences in their magnetic elements (leakage inductance (L_k) and in the isolation transformer). In DAB1, L_k is integrated within the transformer itself, while in DAB2, L_k is an external component connected in series with the transformer. These results in minor differences in the values of L_k and the transformation ratio, as demonstrated in Table III.

TABLE III. MAIN PARAMETERS OF THE DABS

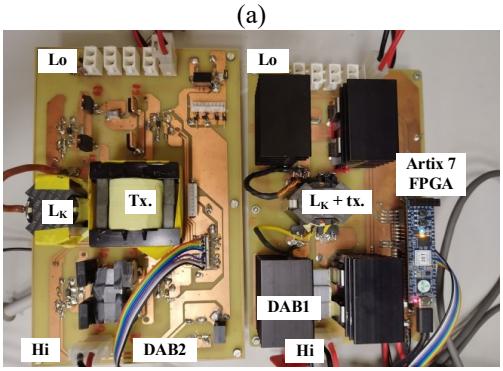
Parameter	DAB1	DAB2
L_k [μH]	6.2	3.3

Parameter	DAB1	DAB2
C_{Lo} $[\mu F]$	50	60
C_{Hi} $[\mu F]$	3	3
n	8	8.4

The DAB converters are controlled by an Artix 7 Cmod A7-35T FPGA, as illustrated in Fig. 14(b), and operate at a fixed switching frequency of 100 kHz.



(a)



(b)

Fig. 14. a) Experimental setup for testing, b) DAB1 and DAB2.

Control parameters are implemented through the FPGA, to operate within the designed voltage and current loops. Initially, experimental tests were conducted only with DAB2, which includes voltage and current sensors. The tests verified the independent performance of the voltage and current loops. The voltage loop experimentation started with a parameter of $k_{i\_v} = 100$, followed by current loop tests with a parameter of $k_{i\_c} = 800$, in accordance with the regulators proposed in (11) and (12). The next step was the validation of the IPOS configuration using a resistive load.

A. *Voltage Loop*

This test exclusively focuses on the DAB2, with the goal of confirming the FPGA programming and validating the design parameters from the theoretical analysis.

The high-side voltage data of the DAB2 was acquired using the HCPL-7520 sensor. Additionally, through the Virtual Input/Output (VIO) environment present in the Vivado software, it was possible to perform a reference voltage step to observe the behavior of the implemented loop.

With a $k_{i\_v} = 100$ in the voltage loop, a reference voltage step corresponding to approximately 6 V was applied. This step resulted in a corresponding increase of 6 V in the high-side voltage, with a settling time of approximately 6 ms. It is observed that this result approaches the characteristics observed in the simulations, indicating a correct implementation of the voltage loop, see Fig. 15. This experiment thus demonstrates the effectiveness of the approach adopted in the system implementation.

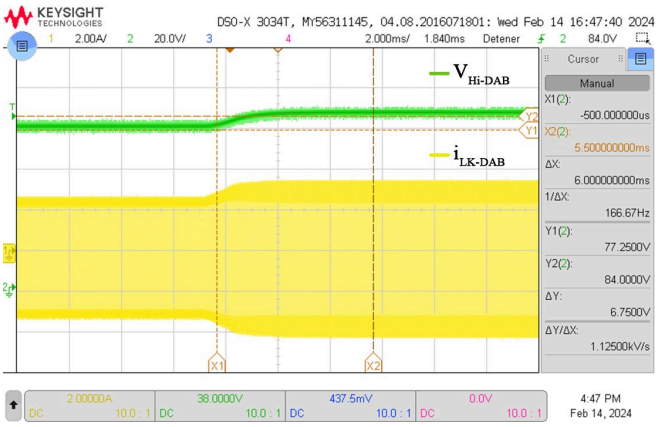


Fig. 15. Experimental waveforms of the voltage loop with $k_{i\_v} = 100$. CH1: i_{L_k}(2 A/div), CH2: V_{hi} (20 V/div), and a time base of 2 ms.

B. *Current Loop*

The current data from the DAB was captured through the ACS711-25 sensor. Through the VIO environment, a test was conducted by applying a jump in the reference current to evaluate the performance of the implemented loop.

During the test conducted with a $k_{i\_c} = 800$, an input current step corresponding to 260 mA was applied, resulting in a practical observation of an increase of 250 mA, with a change time of 1.875 ms. Once again, it was found that the parameterization and design of the loop demonstrated satisfactory and consistent results with the simulations conducted, see Fig. 16. This experiment reinforces the validity of the approach adopted in the implementation of the current control system, highlighting its performance and accuracy in practice.

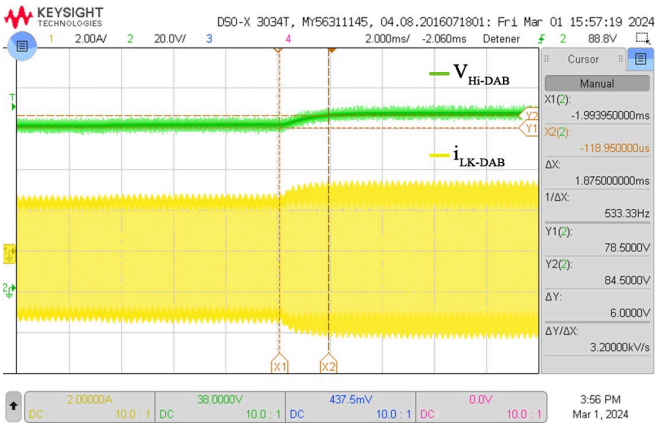


Fig. 16. Experimental waveforms of the current loop with $k_{i\_c} = 800$. CH1: i_{L_k}(2 A/div), CH2: V_{hi} (20 V/div), and a time base of 2 ms.

C. *IPOS Configuration*

After independently validating the voltage and current loops, experimental tests were conducted with both loops in a system that includes two DABs in IPOS configuration. Since there is interaction between both control loops, simulation is crucial to understand the expected behavior in practice. Fig. 17 presents experimental results equivalent to the simulation results presented in Fig. 13. The observed behaviors in the voltage and current responses are equivalent to the simulation results. Experimentally, the converters reach steady state after 60 ms of applying the 5 V change in the voltage reference of DAB1, whereas in simulation the settling time was 40 ms. This difference is due to the non-ideal characteristics of the converters.

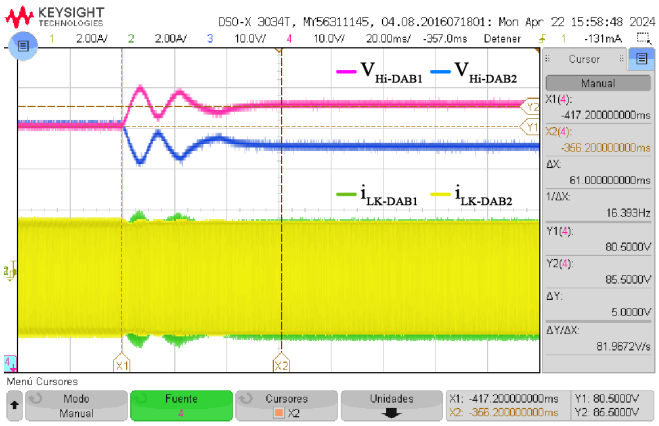


Fig. 17. Experimental waveforms of the voltage loop and current loop with $k_{i\_v} = 100$ and $k_{i\_c} = 800$. CH2: V_{hi_DAB2} (5 V/div), CH3: V_{hi_DAB1} (5 V/div), CH4: $i_{L_{k-DAB1}}$(2 A/div) and a time base of 5 ms.

IV. Conclusions and Future Work

This article proposes a modular topology with two DAB converters to integrate removable batteries into Electric Vehicles (EVs) of 400 V and 800 V. The control loops were designed through simulations tailored to the project specifications and experimentally validated. The results demonstrate the integration of the voltage and current control loops in the IPOS configuration.

Simulation predicts the behavior of results that can be observed in practice, but slight differences are observed due to non-ideal effects present in the devices. Experimental tests validate the stability in the operation of both converters.

As future work, optimization of the control loop implementation on the FPGA and experimental validation is planned. Additionally, experimental tests will be conducted on a prototype operating at nominal voltages and 5 kW power.

Acknowledgment

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