Deep Investigation on SiC MOSFET Degradation under Gate Switching Stress and Application Switching Stress

Alexis A. Gómez [1], Juan R. García-Meré [1], Alberto Rodríguez [1], Juan Rodríguez [1], Carlos Jimenez [2], Jaume Roig-Guitart [2]

[1] Power Supply Systems group (SEA), University of Oviedo; Gijón, Spain
https://sea.grupos.uniovi.es/; gomezalexis@uniovi.es
[2] onsemi; Oudenaarde, Belgium

***Abstract*—This work compares Silicon Carbide (SiC) MOSFET electrical degradation, with special focus on the threshold voltage, under Gate Switching Stress (GSS) and Application Switching Stress (ASS) tests. For this purpose, a dedicated setup has been developed and utilized to dynamically stress devices under different conditions. Remarkably, the degradation differs between GSS and ASS, thus being more pronounced in the latter case. An explanation based on TCAD simulation analysis is provided along with a methodology to adapt GSS testing to obtain hard-switching real application results.**

Keywords—Reliability, Silicon Carbide (SiC), Application switching stress, Gate switching stress, AC Bias Temperature Instability (AC BTI), Dynamic Gate Stress, Dynamic Reverse Bias.

I. INTRODUCTION

The development of Silicon Carbide (SiC) metal-oxide field-effect transistors (MOSFETs) has provided generational advancements for power converters and are becoming the technology of choice for high power applications [1]. Moreover, compared with silicon-based alternatives, these offer greater breakdown voltages, better thermal conductivity and make possible to operate with higher switching frequencies [2]. These characteristics translate into converters with higher power densities and specific power.

Threshold voltage (V_{th}) drift becomes more critical as SiC MOSFETS are more sensitive to it [3]. An increase in V_{th} leads to an increase in the channel resistance which in the case of SiC is more relevant with respect to the total drain to source on-state resistance ($R_{ds,on}$) than for silicon, resulting in greater power losses. A negative V_{th} drift can cause false turn-on events which in some cases can lead to the destruction of the converter. For silicon, a prominent degradation mechanism is Bias Temperature Instability (BTI). BTI can be evaluated by applying a constant voltage to the gate, positive or negative, which produces a positive or negative V_{th} shift in the corresponding direction depending on the stress time and polarity. BTI is even more relevant in SiC MOSFETs due to the higher trap density at the interface or near the interface, thus showing dynamic dependencies when alternating gate biasing between negative and positive voltages.

Dynamic gate stimuli may also lead to a significant degradation, commonly named as Gate Switching Instability (GSI). GSI is nowadays recognized by industry and susceptible to be quantified by SiC specific guidelines for reliability test and methods [4], [5]. This opposes to the exclusively static reliability tests proposed in the past for silicon power devices. Hence, current guidelines suggest testing Gate Switching Stress (GSS) with regular gate drivers and the absence of other electrical or thermal stressors. In this paper, an experimental long-term degradation comparison is conducted between two stress scenarios: GSS and a synchronous boost converter working at light loads, named here as Application Switching Stress (ASS). Our objective is to determine if a simple and cost-effective GSS test is sufficient to predict the degradation of the switches that would result from a more complex ASS test. Experimental results from both stressing approaches are provided with the objective to determine if GSS is enough or further testing is required to accurately determine device aging. These are supplemented with finite element simulations and an explanation of the distinct stages in the switching process that lead to different results.

In section II a description of the developed setup and the employed methodology are provided. Section III describes the experimental results which are elucidated by simulations in section IV. In section V the overall results are discussed, and the conclusions are drawn in section VI.

II. SETUP AND METHODOLOGY DESCRIPTION

GSS, Dynamic Gate Stress (DGS) or AC BTI refer to the same reliability test in which the gate of a MOSFET is pulsed between a low and a high voltage value while the drain and source are short-circuited. It is done at a switching frequency in the order of magnitude of the actual application [4], [5]. As a result of this test, the Device Under Test (DUT) suffers a positive and permanent shift in V_{th} and $R_{ds,on}$ named as GSI that becomes dominant over BTI for relatively large number of switching cycles and more negative driving voltages.

A dedicated setup is designed to perform GSS and ASS tests in the same circuit board, thus ensuring a fair comparison between the two tests. The setup is capable to switch between the two circuit configurations represented in Fig. 1 in a simplified manner by just utilizing jumpers to configure its electrical connections. With regard to the ASS test, a synchronous boost configuration is used (see Fig. 1b) in continuous conduction mode with relatively small current (input current smaller than 2 A). Hence both GSS and ASS tests are done with the same gate driving setup, auxiliary components, parasitic elements and ambient conditions.

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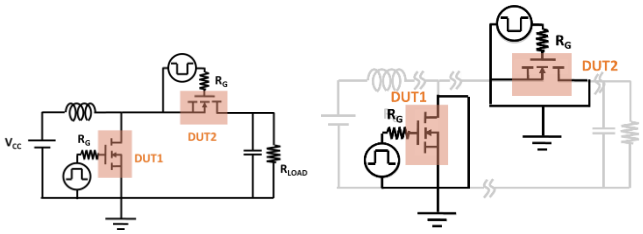
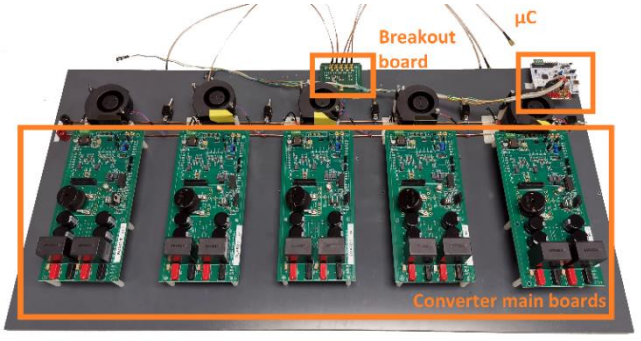


(a) (b)

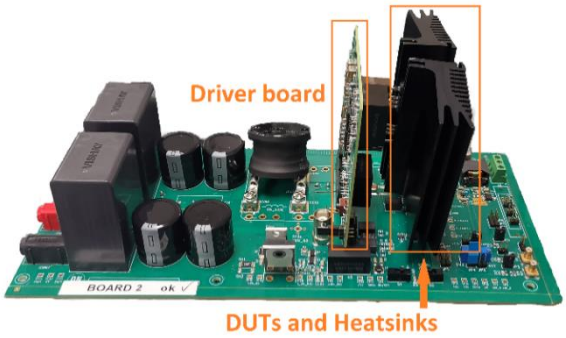
Fig. 1. Simplified setup schematic. (a) For GSS. (b) For ASS

In order to run multiple tests at the same time, the setup includes 5 identical boards, pictured in Fig. 2a, that are equipped with a switching cell, as indicated in Fig. 2b. Each switching cell board includes 2 DUTs in a half-bridge configuration as well as the individual gate drivers, auxiliary power supplies and additional circuitry. Therefore, the complete setup is capable of testing 10 DUTs under the same conditions simultaneously for GSS and two groups of 5 DUTs for ASS, one group for the low-side and other for the high-side of the boost converter.

The test procedure is made up by the following steps. First, a complete parametric analysis, including $R_{ds,on}$ and V_{th}, is performed for all DUTs with a curve tracer and a socket fixture that are external to our test setup. Second, the different DUTs are stressed in GSS or ASS conditions during a given number of cycles. As described in Fig. 3, after a certain number of switching cycles, the GSS or ASS test is interrupted by inspection windows where the DUTs are removed from the switching cells, measured again with the external curve tracer and returned to the testing boards to resume the test. The inspection windows may take a few tens of minutes.



(a)



(b)

Fig. 2. Experimental setup pictures. (a) Main boards, signal breakout board and microcontroller without switching cells. (b) Main board equipped with switching cell (driver board, DUTs and heatsinks).

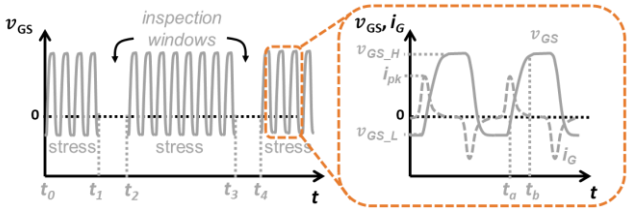


Fig. 3. Illustrative description of test sequence and v_{GS} waveform detail.

However, this is irrelevant due to the permanent nature of the degradation which is confirmed by additional measurements at 24 and 48 hours after the GSS and ASS tests are stopped. It has been also demonstrated in literature that the DUT degradation in GSS is dependent on the number of cycles [3], [6], [7], thus being possible to accelerate the degradation by driving the gate at high frequency. In our experiment, a relatively low frequency of 100 kHz has been defined for both GSS and ASS to avoid self-heating effects in the application test The measurement procedure with the curve tracer always follows the same programmed sequence and includes preconditioning steps to measure V_{th} according to [8].

III. Experimental Results

The devices used for all experimental tests and simulations correspond to engineering samples of a 1200 V SiC MOSFET based on trench technology. This device is rated for 117 A of continuous drain current. The initial V_{th} for these devices is 3.8 V extracted at I_d=20 mA and V_{gs}=V_{ds}.

The driving conditions used for GSS and ASS are within the maximum ratings for the tested semiconductors, meaning a high driving voltage ($V_{gs,h}$) of +18 V and a negative driving voltage ($V_{gs,l}$) of -8 V; at a switching frequency of 100 kHz with the same gate resistor for turn-on and turn-off. For GSS, the tests are done with two different gate resistors, 4.7 Ω and 1 Ω. Other parameters of the boost converter used for the ASS test are listed in Table I.

TABLE I ASS TEST SPECIFICATIONS

Configuration	Boost converter
V_{CC}	400 V
$V_{ds\ max}$	800 V
Duty cycle	0.5
$\overline{i_L}$	1.2 A
$\Delta i_{L,pp}$	1.6 A
R_G	4.7 Ω

It is relevant that the transferred power by the setup when operating as a boost converter is quite small and well below the full capabilities of the devices. These conditions are in agreement to the active version of the Dynamic Reverse Bias test, defined in [4], with a reduced V_{ds_max} to a value closer to the application nominal value.

Fig. 4 shows the analysis of the V_{th} shift (ΔV_{th}) in the different inspection windows for the 10 devices stressed

under GSS. It can be observed a small ΔV_{th} dispersion in relation to the absolute ΔV_{th} values. Furthermore, dispersion remains consistent along different measurements, therefore a large sample size is not needed to properly characterize ΔV_{th}. Additionally, tests with different values and asymmetrical turn-on and turn-off gate resistors were conducted to find a switching event type dominance in the degradation process. All tests reported that different turn-off gate resistors caused no difference in the degradation, and only turn-on gate resistance variations caused a measurable difference. These results are in agreement with [6], [9]. Consequently, in this paper it is considered that the turn-on is dominant in the degradation process.

The device degradation experimental results for GSS and ASS tests are provided in Fig. 5. This figure represents the ΔV_{th} as a function of the number of switching cycles in a logarithmic scale. Every datapoint represents the average value of the different device samples and extrapolation lines have been added to facilitate the visual analysis. In the case of ASS, the curves for high-side and low-side devices are plotted whereas for GSS two curves refer to tests with 4.7 Ω and 1 Ω gate resistor. In the same figure a dashed vertical line marks the end of life at 1×10^{11} cycles for an automotive use case according to [10]. From both GSS test results, it can be concluded that the test with a smaller gate resistor (R_G) has a greater degradation for the same number of cycles, which is consistent with observations in [6], [9]. Test results for ASS show similar ΔV_{th} for high-side and low-side devices and, at the same time, larger ΔV_{th} than GSS for the same number of cycles and R_G. This finding is contrary to the conclusions reported in a previous work [11] where GSS is supposed to mimic the real application GSI by using identical driving conditions. In all cases, negligible ΔV_{th} recovery was observed at 24 and 48 hours after stopping the electrical stress in GSS and ASS tests (see V_{th} distributions for GSS in Fig. 6). The irreversibility of the GSI has been already observed in other publications and it is only recoverable by annealing the devices at temperatures above 250°C [6], [10], [11].

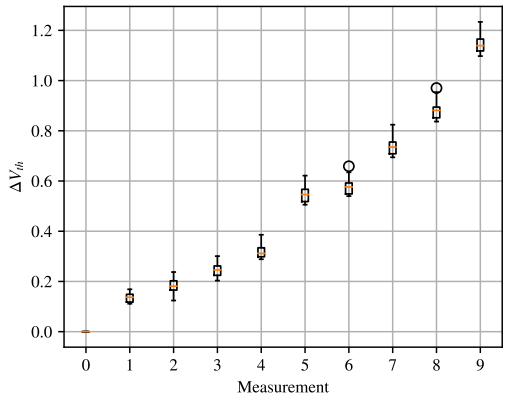


Fig. 4. Different measurements of ΔV_{th} at different aging stages for GSS.

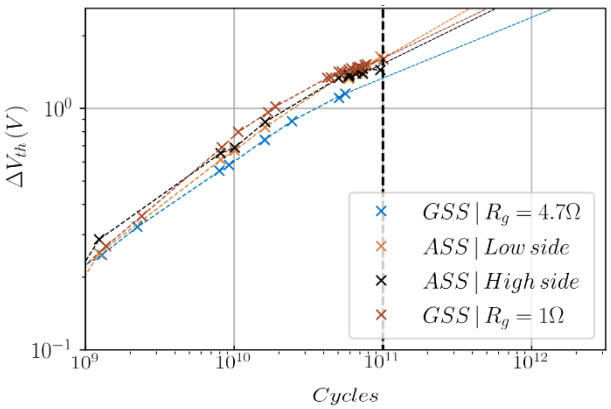


Fig. 5. Experimental ΔV_{th} results as a function of the stressing cycles for different stress conditions.

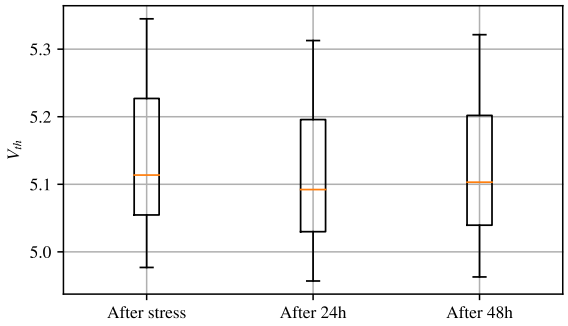


Fig. 6. V_{th} measurements at different times after final stress window.

In Fig. 7, experimental gate-source voltage waveforms are drawn for the same four cases measured in Fig. 5. Table II has been created by extracting gate-source voltage slope (dv_{gs}/dt) utilizing different criteria from Fig. 7 and the current peaks from experimental gate current waveforms (i_g). Comparing the two GSS cases in Table II, it is clear that the curve with smaller R_G has a greater gate-source voltage slope (dv_{gs}/dt) with both criteria due to a larger gate current peak (i_g peak). Interestingly, ASS low and high-side devices show similar dv_{gs}/dt. If we focus our analysis to the time where $v_{gs} < V_{th}$, then the v_{gs} waveforms for low and high-side are identical. As in the GSS R_G=1.0 Ω case, dv_{gs}/dt for ASS low and high-side is larger than GSS R_G=4.7 Ω but this is only true for $v_{gs} < V_{th}$ where the maximum dv_{gs}/dt takes place. However, it is reported in literature that GSI is precisely generated in this time interval due to the transition from deep accumulation to deep inversion [6]. This leads to establish a correlation between a more pronounced ΔV_{th} and a larger dv_{gs}/dt in ASS when comparing to GSS with identical driving conditions. The i_g peaks are extracted from i_g experimental waveforms measured during GSS and ASS tests by means of a Rogowski coil directly at the gate package pin and confirmed with a low voltage differential probe across the gate resistor. The maximum dv_{gs}/dt measurements are realized during the time where $V_{gs,l} < v_{gs} < V_{th}$ as greater dv_{gs}/dt can appear later in the switching waveforms due to measurement noise.

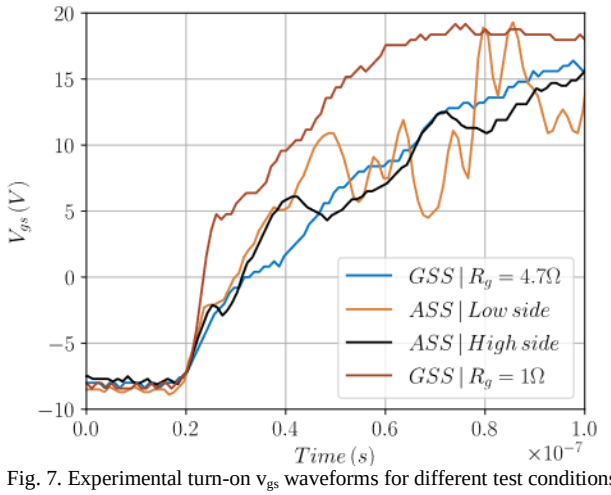


Fig. 7. Experimental turn-on v_{gs} waveforms for different test conditions.

TABLE II TURN-ON CHARACTERISTIC VALUES

Parameter	GSS (R_G=1 Ω)	GSS (R_G=4.7 Ω)
dv_{gs}/dt (10-90 %)	0.72 V/ns	0.25 V/ns
dv_{gs}/dt (max.)	2.16 V/ns	0.83 V/ns
i_g peak	5.5 A	3.1 A

Parameter	ASS (Low-side)	ASS (High-side)
dv_{gs}/dt (10-90 %)	0.28 V/ns	0.26 V/ns
dv_{gs}/dt (max.)	1.57 V/ns	1.50 V/ns
i_g peak	3.3 A	3.1 A

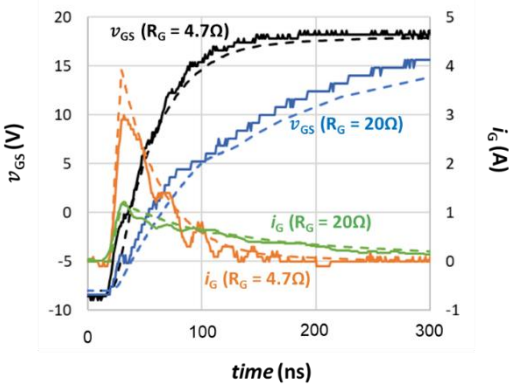
Traditional measurements of the dv_{gs}/dt take into account the entire voltage rise time, potentially masking high dv_{gs}/dt present during specific segments of the curve. If the section in which $v_{gs} < V_{th}$ dominates the aging process, these parameters may not be considered adequate for defining a stress test. More similar maximum dv_{gs}/dt values for $v_{gs} < V_{th}$ are observed for both cases in ASS and GSS (R_G=1 Ω) than for GSS (R_G=4.7 Ω), which correlates to similar degradation levels. This is contrary to what would be expected according to the 10 to 90 % criteria. This suggests that the maximum dv_{gs}/dt for $v_{gs} < V_{th}$ is a more accurate parameter to define this type of stresses.

IV. SIMULATION ANALYSIS

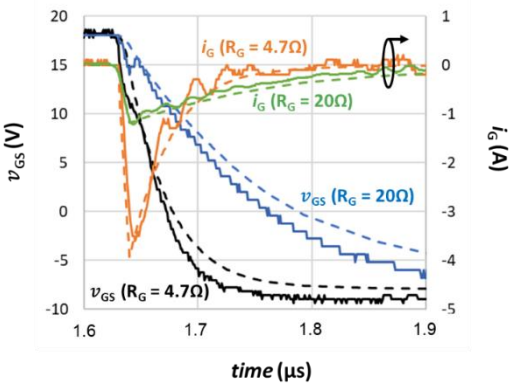
To gain deeper insight into the results from the different cases, mixed-mode TCAD electrical simulations are conducted in conjunction with a SPICE circuit by means of a commercial software [12]. These simulations are based in physics-based finite element modeling and require accurate calibration of the semiconductor properties and deep knowledge on the fabrication process. To examine the validity of the simulation models, several switching events under different conditions are simulated and compared against experimental results. In Fig. 8, two switching events are depicted: In solid lines are the experimental results from the GSS test, whereas the dashed lines represent the simulation results. The black and orange waveforms are the gate-source voltage and the gate current traces for a gate resistor of 4.7 Ω; the blue and green traces represent the same for a gate resistor of 20 Ω. A high correlation between simulation and experimental results for both switching events is observed. Fig. 9 shows the simulated v_{gs} waveforms during a turn-on switching event for the same conditions as the measured waveforms in Fig. 7. All simulated cases exhibit a high correspondence with the experimental results. It is confirmed by simulation that dv_{gs}/dt is larger in ASS compared to GSS for the same driving conditions when $v_{gs}<V_{th}$. This confirmation is relevant in order to reinforce our theory and to dissipate doubts when it comes to possible distortions in measured waveforms.

Aiming a deeper simulation analysis, the internal current distributions for GSS, ASS low-side and ASS high-side are depicted in Fig. 10. The waveforms for v_{gs} and i_g as well as the currents through the drain (i_d), source (i_s) and bulk (i_b) are shown in Fig. 10 following the direction notation indicated in the included transistor graphic. The black dashed lines correspond to the GSS in Fig. 10(a) are kept for ASS in Figs. 10(b) and 10(c) as reference curves. This analysis, not possible by experiment, shows that the internal current distribution is different in the three cases.

For GSS, the switching process starts at t_0 with a rapid increase in i_g. As there are no other currents before t_0, i_g is equal to the sum of i_d, i_b and i_s and it is split almost evenly between i_d and the sum of i_s and i_b. i_g reaches its peak value at t_1 and at t_2 V_{th} is reached. In the case of ASS, distinct current distributions can be seen for the low-side and for the high-side. For the low-side, the switching events starts at t_0 and same as before i_g starts rising towards the maximum value, however i_d has a negligible magnitude and the sum of i_b and i_s can be considered equal to i_g. The peak value of i_g is reached at t_1 and at t_2 V_{th} is reached and current starts flowing through the channel.



(a)



(b)

Fig. 8. Simulation and experimental GSS turn-on and turn off waveforms. (a) Turn-on. (b) Turn-off.

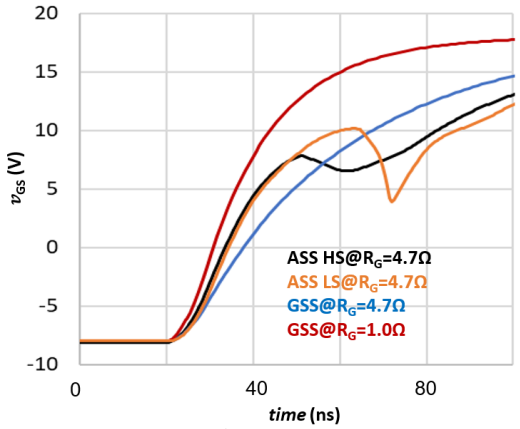


Fig. 9. v_{gs} turn-on simulated waveforms.

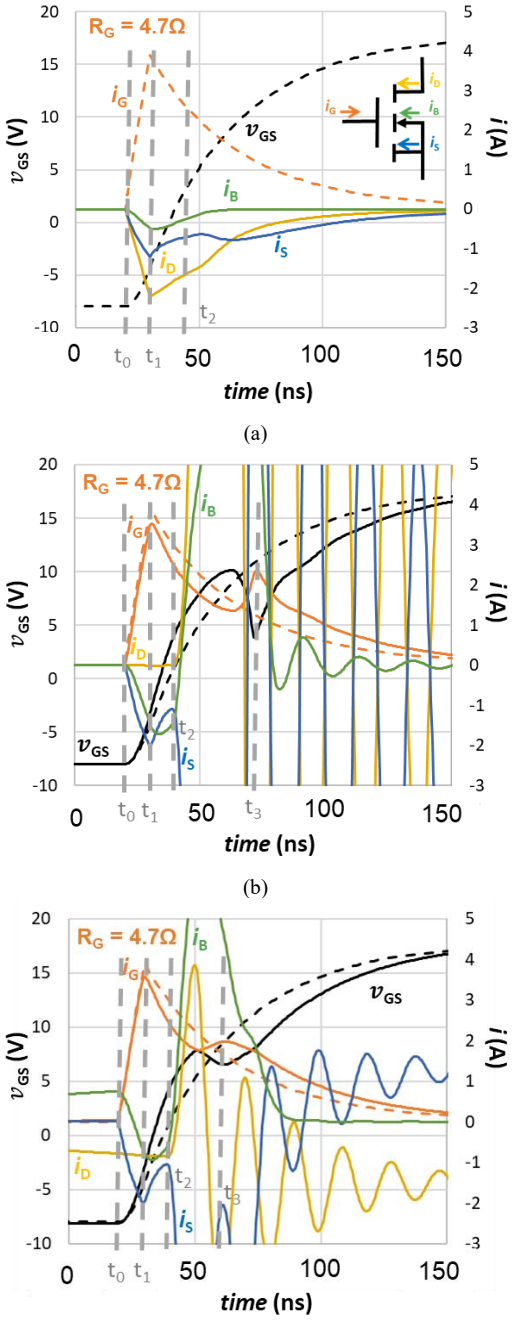


Fig. 10. Simulated i_G, i_S, i_D, i_G and v_{GS} waveforms during turn-on for (a) GSS. (b) ASS low-side. (c) ASS high-side.

After that, oscillations appear in the current waveforms due to the parasitic capacitances and inductances of the main power loop. At t_3 a decrease in v_{gs} is observed and the gate current increases. In the case of the high-side, a reverse current is flowing through the device before t_0. After t_0, i_g rises while the drain current remains unaffected and i_g flows entirely through the source and bulk terminals. At t_1 the peak i_g value is reached and at t_2 v_{gs} arrives at V_{th}, which affects i_d and causes some current oscillations due to parasitic effects. At t_3 a dip in v_{gs} is observed and i_g increases. The dips in v_{gs} for both ASS cases and the corresponding increase in i_g is due to the Miller plateau. The Miller plateau is not observed in the case of GSS as v_{ds} remains constant during the switching event with the drain and source terminal connected.

V. Results Discussion

A crucial feature to explain the different degradation in GSS and ASS is the difference in dv_{gs}/dt observed by experiment and simulation. This difference can be merely explained by the variation of transistor capacitances due to different terminal connections and switching conditions.

In GSS, the drain and source terminals of the DUT are shorted as it was represented in Fig. 1(b). The electrical connection between drain and source makes v_{ds} close to zero. In this configuration, C_{gd} and C_{gs} are connected in parallel in the DUT, being both capacitances the same order of magnitude. This results in a balanced distribution of i_g during the turn-on process between i_d and $i_s + i_b$ to charge C_{gd} and C_{gs} capacitances. As i_g is limited by the driving voltages and the gate resistor, a smaller sum of i_s and i_b results in a slower turn-on. This effect and the typical dependence of C_{gd} and C_{gs} with V_{gs} are illustrated in Fig. 11.

For ASS, high-side and low-side exhibit a similar initial dv_{gs}/dt despite the different internal current distribution and switching conditions. In the low-side case, illustrated in Fig. 12, there is no current flowing prior to the turn-on, therefore the device is withstanding a constant voltage, in this case 800 V. The drain-source voltage causes the value of C_{gd} to be significantly lower during the turn-on compared to its value when v_{ds} tends to zero. As a result, most of i_g flows through the bulk and source to charge C_{gs}, leading to a steeper dv_{gs}/dt for $v_{gs}<V_{th}$. In the case of the high-side, a reverse current is observed in Fig. 10(c) before t_0 which is characteristic of a boost converter when operating in CCM. If this reverse current is large enough or the conduction time of this reverse current is sufficiently long , then the parasitic C_{ds} capacitance would discharge, and the current would start to flow through the parasitic diode. If the switching event takes place under such circumstances, v_{ds} is correspondent with the forward voltage of the parasitic diode. This is referred as Zero Voltage Switching (ZVS). However, in this case as the current magnitude is reduced, see Table I, and the deadtimes were maintained within typical values, at t_0 the voltage between drain and source is approximately 200 V, achieving partial ZVS. Subsequently, high-side experiences a similar C_{gd} reduction for $v_{gs}<V_{th}$ as the one seen by low-side. This is depicted in Fig. 13.

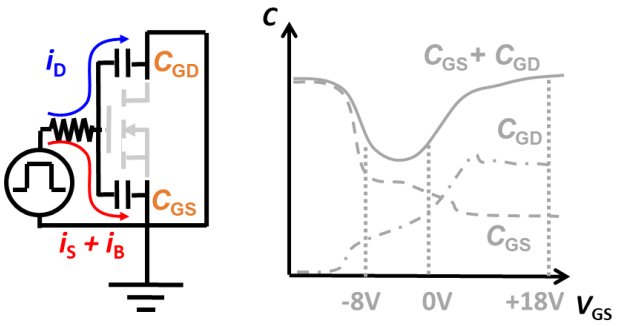


Fig. 11. GSS simplified turn-on schematic with parasitic capacitances (v_{gs} < V_{th}) and illustrative description of C_{gd} and C_{gs} dependence with v_{gs}

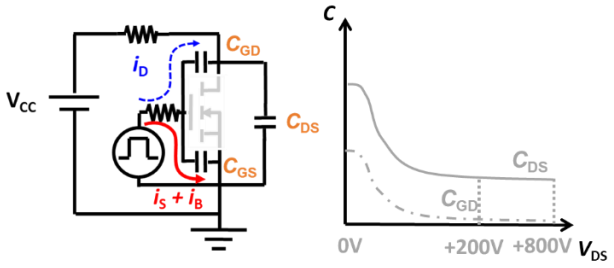


Fig. 12. ASS simplified schematic for DUT parasitic capacitances (v_{gs} < V_{th}) and illustrative description of C_{gd} and C_{ds} dependence with v_{ds}.

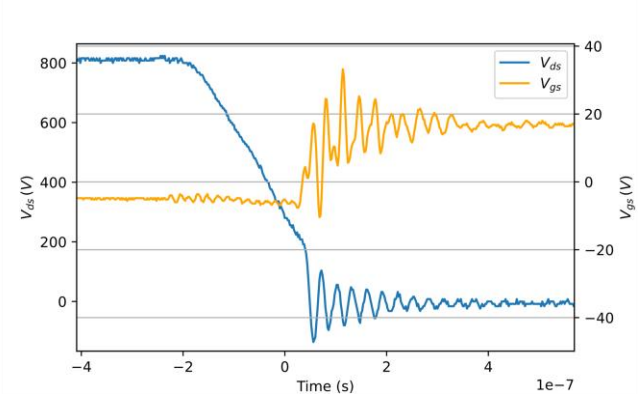


Fig. 13. Experimental turn-on waveforms for ASS high-side device.

Since GSS tests are much simpler to run than ASS tests, it is of interest to be able to utilize GSS test to properly reproduce and predict real application degradation. After the results obtained in this work, it is strongly recommended to adjust the limiting element in the gate loop to obtain a similar dv_{gs}/dt for v_{gs} < V_{th}. This adjustment can be easily implemented by adjusting R_G in the GSS test until fitting dv_{gs}/dt in ASS test. That would make GSS results similar to those of a hard-switching application. This is depicted in Fig. 5 by the ΔV_{th} from GSS at R_G=1 Ω and ASS results.

VI. Conclusions

This work demonstrates that DUT degradation due to GSI may differ between GSS test and ASS test, being the second one representative of the operation in conventional half-bridge hard-switching topologies. It has been observed that GSS definition criteria underestimates the maximum v_{gs} slope for v_{gs} < V_{th} during turn-on in comparison to ASS. This effect has been elucidated by TCAD simulations and parasitic capacitance analysis. To properly evaluate the electrical degradation at the end of life in a real application scenario via GSS a vgs slope adjustment to reflect ASS switching conditions is deemed necessary.

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