ZVS Modulation Strategy for Constant High Frequency Four-Switch Buck-Boost Converters used in Envelope Tracking Power Supplies

Juan R. Garcia-Mere, Juan Rodriguez and Javier Sebastian
Electronic Power Supply Systems Group (SEA)
University of Oviedo
Gijon 33204, Spain
Email: {garciamjuan, rodriguezmjuan, sebas}@uniovi.es

***Abstract*— Envelope Tracking (ET) is a technique used to improve the power efficiency of Linear Power Amplifiers (LPAs). It consists in modulating the LPA supply voltage according to the envelope of the communication signal to be reproduced. In order to accurately reproduce the envelope, Switching-Mode Power Converters (SMPCs) with a switching frequency in the megahertz range are mandatory, leading to high switching losses and degrading the overall performance of the ET system. In this work, a control strategy to achieve Zero Voltage Switching (ZVS) in a Four-Switch Buck-Boost (FSBB) converter with constant frequency is proposed to minimize the switching losses of high-bandwidth SMPCs in ET applications. The operation of a FSBB performing fast output voltage changes and the methodology used to achieve ZVS for any voltage are described. The idea is validated with a 10 MHz GaN-based prototype providing an output voltage that ranges between 0 V and 20 V and handling a peak output power of 45 W.**

Keywords—Envelope Tracking (ET), Zero Voltage Switching (ZVS), Four-Switch Buck-Boost (FSBB), high-frequency converters.

I. INTRODUCTION

In recent years, modern wireless communication systems have experienced a significant increase in the data rate they have to provide. As a result, the modulation schemes used by these networks are becoming more complex, generating signals with larger bandwidths and higher Peak-to-Average Power Ratios (PAPRs). Moreover, the amplification of such sophisticated signals demands high linearity to comply with the restrictive spectrum requirements required by the different wireless communication protocols. Consequently, the use of Linear Power Amplifiers (LPAs) is the most popular approach to be used in the amplification process of modern communication signals. They exhibit a high linearity, but the main drawback in the use of the LPAs is their poor power efficiency, which is even worse as the voltage difference between the supply voltage and the amplitude of the amplified signal increases [1]. Thus, the power efficiency of LPAs supplied with a fixed voltage level will be degraded drastically during the amplification of signals with high PAPRs, since they will only operate occasionally with output voltages close to the voltage supply, where they have their maximum efficiency.

Many radio frequency (RF) strategies have been proposed to enhance the power efficiency of LPAs while preserving the high linearity they provide. One of the most preferred methods is Envelope Tracking (ET), where the supply voltage of an LPA is continuously adjusted according to the envelope of the communication signal to be reproduced (see Fig. 1) [1], [2]. Thus, the LPA always operates close to peak efficiency, reducing power losses. The circuitry in charge of tracking the signal envelope variations and biasing the LPA with the suitable voltage level is usually referred to as the Envelope Amplifier (EA).

Many EA architecture implementations can be found in the literature. The most extended approach involves the use of Switching-Mode Power Converters (SMPCs) [3], [4]. SMPCs exhibit a high-power efficiency in the reproduction of time-varying signals as communication signals envelopes. The main disadvantage of this approach is that the bandwidth of the signal the SMPCs can reproduce is limited by their switching frequency. High switching frequency (MHz range) is mandatory to accurately track the fast envelope changes of current communications signals, resulting in high switching losses, and thus degrading the power efficiency of the overall ET system.

Different approaches can be followed in the design of SMPC-based EA architectures to minimize the switching losses. For instance, complex power topologies based on multilevel and multiphase strategies are presented in [5], [6] to reduce the voltage and current stresses across the switches. Alternatively, solutions based on achieving Zero Voltage Switching (ZVS) to reduce switching losses in SMPCs operating within the MHz range have been also proposed. In [7], a complex architecture based on the combination of multiphase and multilevel topologies is proposed. The converter achieves ZVS by increasing the current ripple through the inductor at the expense of penalizing conduction

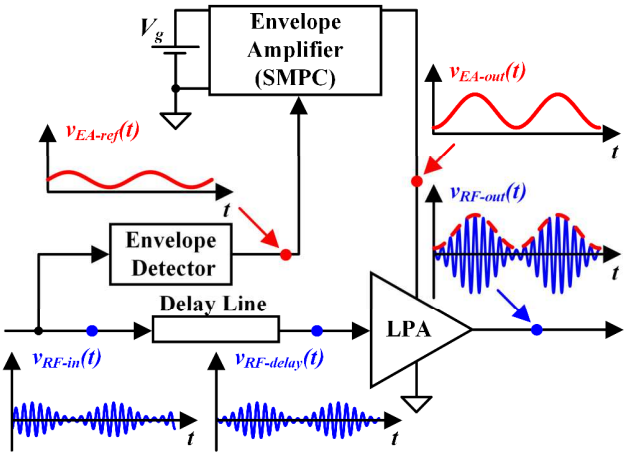


Fig. 1. General scheme of an ET architecture.

losses, especially at low load. In [8] a solution based on modifying the transfer function of a high order output filter in a buck converter is proposed to achieve ZVS. As it can be seen, the main approach to achieve ZVS in an EA implementation is to increase the current ripple by reducing the inductance, which penalizes the power efficiency at light load.

In this work, the use of a Four-Switch Buck-Boost (FSBB) converter (see Fig. 2) that is controlled with a ZVS modulation strategy specially conceived for ET is proposed. The main significant advantage of the use of FSBB converters is the ability to perform voltage step-up and step-down conversion with a single stage, thus avoiding the use of a modular architecture and reducing the number of components. Furthermore, this converter is also used when bidirectional power transfer is required, such as smart grids [9], [10]. Some of the additional applications proposed in the literature for the FSBB converter include the bus pre-regulation of data centers [11] and photovoltaic systems, where the converter must operate with a wide range of input voltages [12], [13]. Regarding ET, the FSBB converter is a promising alternative to implement an EA architecture, due to the wide range of output voltages that the reproduction of envelope waveforms with high PAPRs demands. The proposed modulation strategy differs from previous proposals as it considers the different constraints that the ET technique imposes.

In Section II, the FSBB topology is described, along with the principle of operation under the proposed ZVS modulation. In Section III the determination of the values of the different passive components that made up the FSBB is provided. In Section IV, experimental results verify the operation of the FSBB under the proposed ZVS modulation. Finally, the main conclusions of this work are given in Section V.

II. FSBB Converter and Proposed ZVS Modulation

A. Proposed FSBB Converter for ET Applications

The FSBB converter is made up of an inductor L, an output capacitor C and two pairs of complementary MOSFETs: (S_{1A}, S_{1B}), which can be considered as the half-bridge structure of the buck stage where the switching node will be $v_{sw\text{-}in}$, and (S_{2A}, S_{2B}), which is the half-bridge structure that controls the boost stage, whose switching node is $v_{sw\text{-}out}$. The resistive load R_L connected at the output of the converter in Fig. 2 models the power consumption of the LPA in a full ET scheme. Note that the input voltage is referred to as V_g in Fig. 2, and v_o refers to the output voltage waveform synthesized by the FSBB converter. In conventional operation, only one of the two half-bridges switches, while the other one remains unswitched. For voltage step-down conversion ($v_o < V_g$) S_{2B} is ON, and (S_{1A}, S_{1B}) operate complementarily, like in a synchronous buck converter. If step-up mode is required ($v_o > V_g$), S_{1A} is ON, and (S_{2A}, S_{2B}) operate complementarily, as in a synchronous buck converter.

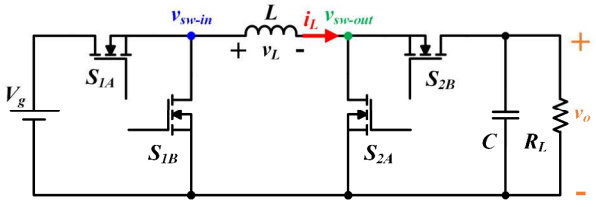


Fig. 2. Schematic of the FSBB converter.

B. Operating Principle of the FSBB Converter in ET Applications

Alternative modulation strategies for the FSBB have been described in the literature to combine both the reproduction of a wide range of input voltages and the optimization of the converter efficiency [14]. In [15], [16], a soft-switching strategy is proposed to achieve ZVS when the FSBB operates as a conventional SMPC (restricted V_g, fixed v_o and variable R_L). The main operating waveforms of this ZVS modulation strategy are shown in Fig. 3. As can be seen, ZVS is achieved in step-up and step-down mode by introducing a negative offset $-I_x$ in the current across the inductor i_L and switching the two half-bridges of the FSBB converter in every switching period. For a better understanding, the driving voltage waveforms of the two half-bridges are included. I_x is the magnitude of the minimum current needed to discharge the output capacitance C_{oss} of the different switches of the converter to achieve ZVS [15], and can be expressed as

$$I_x = \max\{V_g, v_o\}\sqrt{\frac{2C_{oss}}{L}}. \tag{1}$$

In this modulation, the shape of i_L depends on the voltages applied to the inductor v_L during the time intervals T_1, T_2, T_3, and T_4. The voltage v_L is defined as

$$v_L = v_{sw\text{-}in} - v_{sw\text{-}out}\,. \tag{2}$$

In addition, T_1, T_2, T_3, and T_4 will be defined by the switching instants t_1, t_2 and t_3 as follows

$$T_1 = t_1, \tag{3}$$

$$T_2 = t_2 - t_1, \tag{4}$$

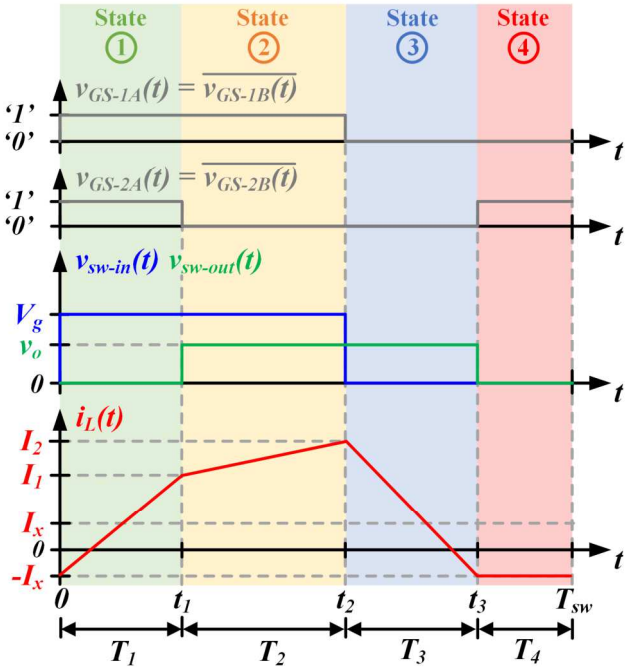
$$T_3 = t_3 - t_2, \tag{5}$$

$$T_4 = T_{sw} - t_3. \tag{6}$$

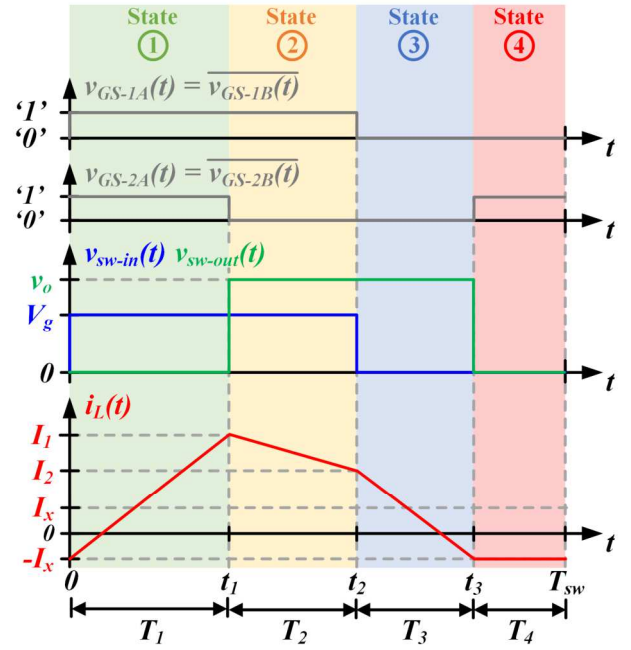
In this work, this ZVS modulation is derived for ET applications, where the FSBB must continuously vary v_o according to the envelope to be reproduced. It should be noted that different constraints must be considered, compared to those used in a conventional SMPC: constant V_g, constant R_L and variable v_o. Furthermore, since this converter is being proposed for ET applications, the switching frequency of the converter $f_{sw} = 1/T_{sw}$ should be high enough to accurately track the highest frequency component of the envelope waveform. Consequently, v_o can be considered constant during several switching periods. These assumptions are considered in the explanation of the circuit and the ZVS modulation strategy.

C. Circuit States

As can be seen in Fig. 3, the operation of the converter in a switching period can be described in terms of four operating states, whose duration depend on the values of the switching instants t_1, t_2 and t_3. A brief description of these states can be found below:



(a)



(b)

Fig. 3. Main waveforms of the FSBB under the ZVS modulation used in this work: (a) Step-down mode. (b) Step-up mode.

- *State 1* [$0 \le t < t_1$, Fig 4 (a)]: initially, at $t = 0$, the current i_L through the inductor L is equal to $-I_x$. At the beginning of the switching period, switches S_{1B} and S_{2A} are ON and $-I_x$ is high enough to ensure the turn on of S_{1A} with ZVS, while turning off S_{1B}. The voltage applied to the inductor v_L is V_g, and i_L increases linearly to value I_1.

- *State 2* [$t_1 \le t < t_2$, Fig 4 (b)]: at t_1, S_{2A} is turned off, and the complementarily controlled switch S_{2B} is turned on with a current level I_1, high enough to achieve ZVS. Note that, to properly perform ZVS, I_1 must verify

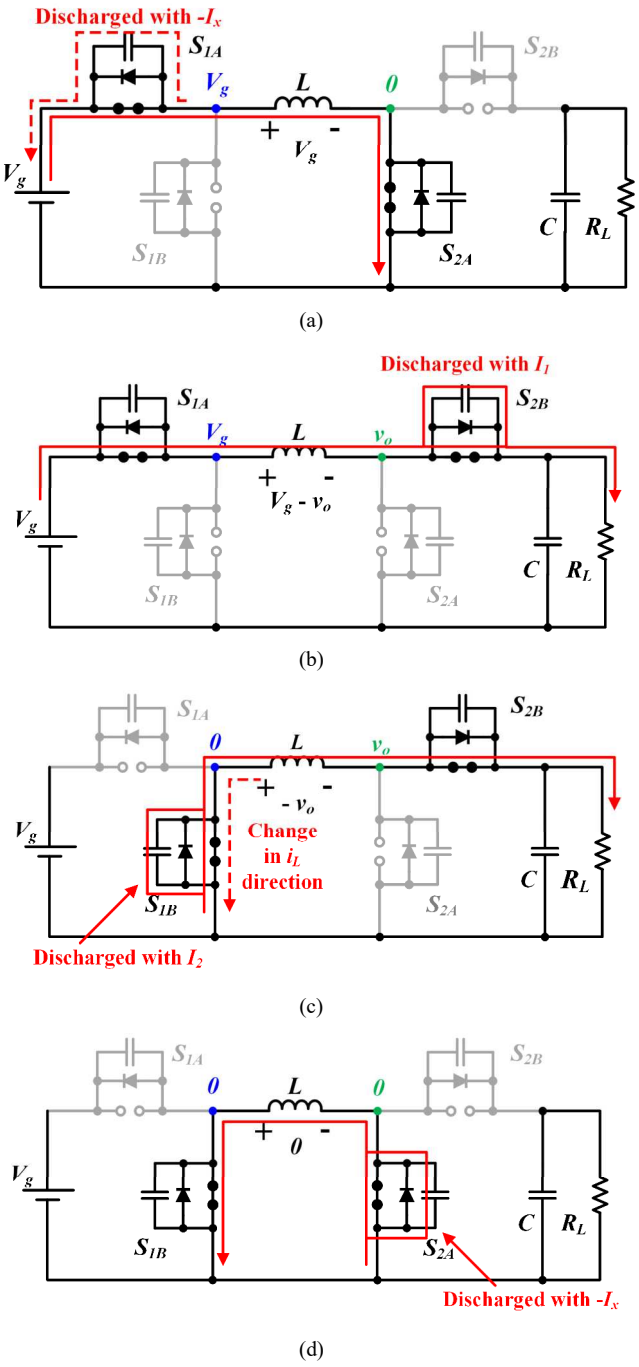


Fig. 4. Inductor current flow in the operation of the FSBB under the ZVS modulation: (a) State 1. (b) State 2. (c) State 3. (d) State 4.

$$I_1 \ge I_x. \tag{7}$$

In this state, $v_L = V_g - v_o$, and i_L increases or decreases depending on whether it operates in step-down mode ($v_o < V_g$) or step-up mode ($v_o > V_g$), respectively. The value of the current i_L at the end of the switching interval is I_2.

- *State 3* [$t_2 \le t < t_3$, Fig 4 (c)]: at the beginning of the switching interval state S_{1A} is turned off and current I_2 is used to turn on S_{1B} with ZVS. If the FSBB converter operates in step-down mode, $I_2 \ge I_1$, and if I_1 fulfills the condition (2), the magnitude of I_2 is high enough to achieve ZVS. Nevertheless, in step-up mode, the value of I_2 must not have decreased below I_x in order to ensure ZVS:

$$I_2 \geq I_x. \tag{8}$$

Regarding the behavior of i_L during this switching interval, since v_L equals $-v_o$, it decreases linearly from I_2 to $-I_x$.

- *State 4* [$t_3 \leq t < T_{sw}$, Fig 4 (d)]: at t_3, current $-I_x$ is used to turn on S_{2A} with ZVS, at the same time S_{2B} is turned off. This state is introduced to clamp i_L ($v_L = 0$), ensuring that the switching frequency is constant and that $i_L = -I_x$ –which is the minimum current required to perform ZVS– at the beginning of the next switching period.

D. ZVS modulation for ET applications

In order to shape i_L to achieve ZVS while reproducing the envelope waveform in an ET scheme, the relationship between the duration of the switching intervals T_1, T_2 and T_3 and the output voltage v_o must be found. In a conventional SMPC, the values of T_1, T_2 and T_3 are solved for a given operating point which is determined by the input voltage V_g, the output voltage v_o and the required output power. Nevertheless, as mentioned before, different assumptions apply in the description of this modulation strategy for ET applications. The introduced ZVS modulation determines the combination of T_1, T_2 and T_3 values which provide ZVS with a wide range of v_o values. In this way, the output power will be fixed by the value of v_o, and cannot be controlled independently, as happens in a conventional SMPC. For the sake of simplicity, only the modulation for step-down operation is explained in detail in this work. Similar assumptions can be considered if the modulation is applied for step-up operation.

The first step in the analysis of the proposed ZVS modulation is to obtain the relationship between V_g and v_o, which can be determined applying the volt·second balance to the inductor L. Thus,

$$V_g T_1 + (V_g - v_o) T_2 - v_o T_3 = 0. \tag{9}$$

Simplifying this expression, the voltage gain M of the converter can be expressed as

$$M = \frac{v_o}{V_g} = \frac{T_1 + T_2}{T_2 + T_3}. \tag{10}$$

As can be seen, there are multiple combinations of time intervals T_1, T_2 and T_3 that leads to a given v_o. However, these instants also affect i_L, which is shaped according to the waveform depicted in Fig. 3(a). In particular, T_1, T_2 and T_3 must be chosen in such a way that ZVS turn-on is ensured for all switches when the converter provides the output current i_o demanded by the LPA at every switching period. The ZVS requirement yields to the following condition

$$i_L(0) = -I_x. \tag{11}$$

This condition can be used to obtain the mathematical expression of current i_L in a switching period. Considering (11) and that v_o is assumed to be constant during the whole switching cycle, i_L can be calculated as

$$i_L(t) = \frac{1}{L}\int_0^t v_L(t)dt - Ix, \tag{12}$$

which yields to the following piecewise function

$$i_L(t) = \begin{cases} -I_x + \dfrac{V_g}{L}t, & 0 \leq t < T_1 \\ i_L(T_1) + \dfrac{V_g - v_o}{L}(t - T_1), & T_1 \leq t < T_1 + T_2 \\ i_L(T_1 + T_2) - \dfrac{v_o}{L}(t - T_1 - T_2), & T_1 + T_2 \leq t < T_1 + T_2 + T_3 \\ -I_x, & T_1 + T_2 + T_3 \leq t < T_{sw} \end{cases} \tag{13}$$

The waveform described by the function (13) has to provide the output current i_o demanded by the LPA, which can be expressed in terms of the average input current $\langle i_g \rangle$ using the transformation ratio M shown in (10)

$$\langle i_g \rangle = M \cdot i_o = M\frac{v_o}{R_L}. \tag{14}$$

Considering the expression (13) and the switching pattern for step-down operation depicted in Fig. 3(a), the input current i_g of the converter is equal to i_L during operation states 1 and 2 (see Fig. 5). Thus, $\langle i_g \rangle$ is

$$\langle i_g \rangle = \frac{1}{T_{sw}}\int_0^{T_1+T_2} i_L(t)dt, \tag{15}$$

which yields to the expression

$$\langle i_g \rangle = \frac{1}{2LT_{sw}}[V_g T_1^2 + (V_g - v_o)T_2^2 + 2V_g T_1 T_2] - I_x\left(\frac{T_1 + T_2}{T_{sw}}\right). \tag{16}$$

Moreover, the optimum combination of T_1, T_2 and T_3 values is the one which minimizes the root mean square (rms) value of the inductance current I_{rms}. With this requirement, the converter conduction losses are minimized. From the expression of i_L shown in equation (13), I_{rms} is

$$\begin{aligned} I_{rms}^2 = \frac{V_g}{T_{sw}Lv_o}\Bigg[&\frac{V_g(V_g + v_o)}{3L}T_1^3 + \frac{(V_g + v_o)^2}{3L}T_2^3 + \\ &+ \frac{V_g^2}{L}T_1^2 T_2 + \frac{V_g(V_g - v_o)}{L}T_1 T_2^2 - \\ &- I_x(V_g - v_o)(T_1^2 + T_2^2) - 2I_x V_g T_1 T_2\Bigg] + I_x^2. \end{aligned} \tag{17}$$

The values of T_1, T_2 and T_3 can be solved for a system of equations determined by conditions (10), (16) and (17) for a given v_o value. From equations (10) and (16) the values of T_1 and T_2 can be found. For the minimization of I_{rms}, it is necessary to express equation (17) as a function of a single variable. Equation (16) allows to find the relationship between T_1 and T_2, shown in the following equation

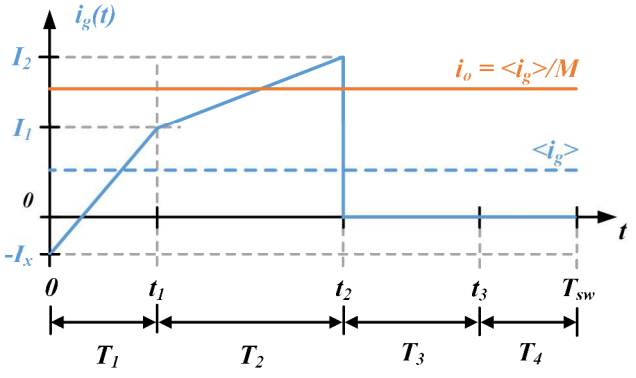


Fig. 5. Representation of the input current i_g waveform and its relationship with the average value $\langle i_g \rangle$ and the ouput current i_o.

$$T_2 = \frac{I_x L - V_g T_1}{V_g - vo} + \\ + \sqrt{\frac{V_g v_o T_1^2 - 2 I_x v_o L T_1 + I_x^2 L^2}{(V_g - v_o)^2} + 2\frac{L T_{sw} v_o^2}{V_g (V_g - v_o) R_L}}. \quad (18)$$

Substituting (18) in (17), I_{rms} can be expressed as a function only of T_1. The optimal value of T_1 will be the one that minimizes (17). However, this value should not only verify (18), but also the condition of equation (7). Thus, it must be considered that all possible values of T_1 must be greater than the minimum possible value of T_1, which is referred to as $T_{1\text{-}min}$. This value is the one that provides the minimum current ZVS at the end of state 1, and it is equal to

$$T_1 = L\frac{2I_x}{V_g}. \quad (19)$$

A similar reasoning can be done for step-up operation, but in this case, the ZVS constraint has to be applied to T_2. Once the optimum T_1 value has been obtained, T_2 can be found by substituting the value of T_1 in equation (18). Alternatively, once the values of T_1 and T_2 are defined, the value of T_3 is set by the value of v_o to be reproduced. By rewriting equation (10), T_3 can be calculated as

$$T_3 = \frac{T_2(V_g - v_o) + T_1 V_g}{v_o}. \quad (20)$$

In the actual implementation of this modulation in an ET architecture, the values of T_1, T_2 and T_3 should be programmed in a Look-Up Table (LUT). In this way, a direct relationship between the values of the time intervals and the output voltage value to be reproduced set by the envelope detector would be implemented (see Fig. 1).

III. Selection of the Components of the FSBB Converter

A. Design of the Inductor L

The inductance L has to be sized in such a way that the modulation method explained above ensures the soft-switching constraints for the whole range of output voltages to be synthesized. In particular, the inductance must ensure always that $i_L(T_{sw}) = -I_x$. Otherwise, the value of i_L may not reach $-I_x$ at the end of the period, not ensuring the ZVS turn-on of neither S_{1A} at the beginning of the next switching period nor S_{2A} at $t = t_3$. The worst-case scenario during the step-down operation will be the one in which v_o is close to V_g. In this case, the required ripple to obtain ZVS is larger than in the rest of the synthesized output voltages, since the output current i_o is also larger. However, the difference between the current ripple and the output current itself is lower, and consequently, large intervals are required to reproduce output voltages close to V_g. In this case, The interval T_4 is minimum ($T_4 = 0$), leading to the following condition

$$T_1 + T_2 + T_3 = T_{sw}. \quad (21)$$

This condition should be satisfied with the synthesis of the maximum output voltage. Otherwise, the increase of the output voltage would be obtained by increasing the ripple of i_L, which would increase the conduction losses. Thus, the optimum value of the inductance will be the one that, verifying the condition (10) in the synthesis of the maximum output voltage, minimizes I_{rms}, shown in equation (17). In order to do this, a methodology similar to the one explained above can be followed, finding the minimum values of the I_{rms} function when expressed as a function of L. Thus, the optimal value of L should be calculated considering the following condition

$$\frac{dI_{rms}}{dL} = 0. \quad (22)$$

In this expression, the values of the intervals T_1 and T_2 will be those that ensure that the converter is synthesizing the maximum output voltage under the condition (21). T_2 can be calculated as

$$T_2 = \frac{T_{sw} v_o - T_1(V_g + v_o)}{V_g}. \quad (23)$$

Alternatively, the value of T_1 in this condition can be found substituting (18) in (16).

B. Design of the Capacitor C

The value of the output capacitor has to be chosen according to the maximum admissible ripple in the output voltage Δv_c. To find the maximum ripple in the converter when synthesizing an output voltage level v_o it will be necessary to consider the output current ripple. Thus, the value of Δv_c can be calculated as

$$\Delta v_c = \frac{1}{C}\int_{T_1}^{T_1 + T_2 + T_3} i_L(t)\, dt. \quad (24)$$

Finally, the value of the capacitor C can be obtained considering the following condition

$$\Delta v_c = \frac{1}{C}\left[\frac{V_g - v_o}{2L} T_2^2 + \frac{V_g}{L} T_1 T_2 + \frac{(V_g - v_o)T_2 + V_g T_1}{2L} T_3 + \right. \\ \left. + L\frac{(I_x + i_o)^2}{2[(V_g - v_o)T_2 + V_g T_1]} T_3 - (I_x + I_o)(T_2 + T_3)\right] \quad (25)$$

IV. Experimental Results

A GaN-based FSBB prototype (Fig. 6) was built in order to verify that the converter is able to vary its output voltage while achieving ZVS. This prototype is based on the EPC9067 EPC Systems development boards, which features EPC8009 GaN transistors from the same manufacturer. The peak output power the prototype can handle is 45 W, the input voltage V_g is 20 V, and it operates with a switching frequency of 10 MHz. The value of the inductor L is 96.7 nH and the value of the output capacitor C is 1 µF. The digital control has been implemented with the Nexys 4 DDR FPGA development platform. The different values of T_1, T_2 and T_3 to be used have been programmed for the desired range of output voltages by means of a LUT. The maximum temporal resolution that this development platform can provide is 2.5 ns, which is considered high enough for the different experiments described in this work.

Fig. 6. GaN-based prototype.

In order to verify the waveform reproduction capability of the FSBB converter, the synthesis of a sinusoidal waveform with a frequency equal to 100 kHz is shown in Fig. 7. The synthesis of the envelope of a multicarrier digital modulation with a bandwidth equal to 100 kHz is shown in Fig. 8 as an example of the reproduction of an arbitrary waveform. Fig. 7 shows the reference waveform v_{ref}, to see the comparative between the experimental results and the target waveform, showing an accurate reproduction of the waveform.

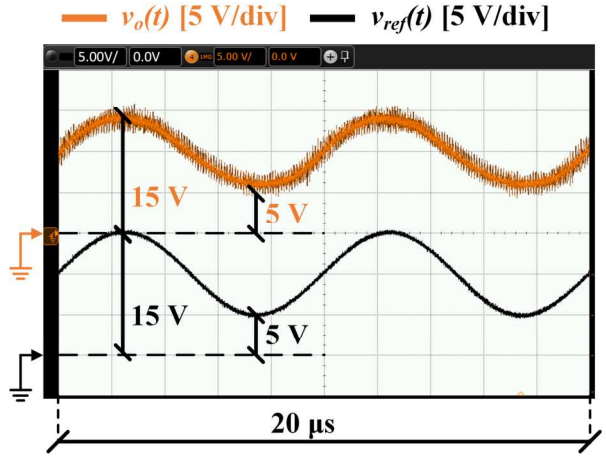


Fig. 7. Reproduction of a sinusoidal waveform with a frequency of 100 kHz

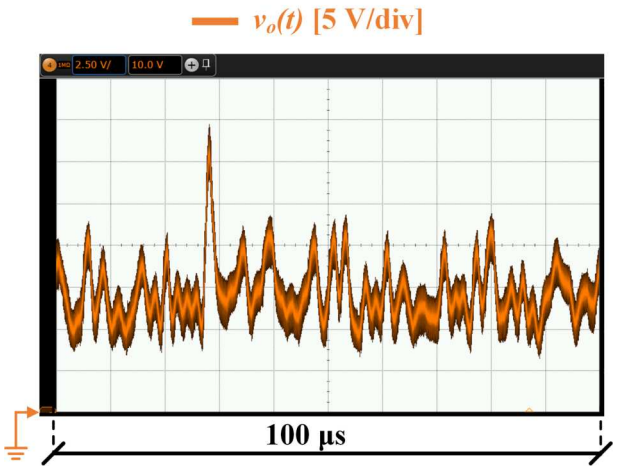
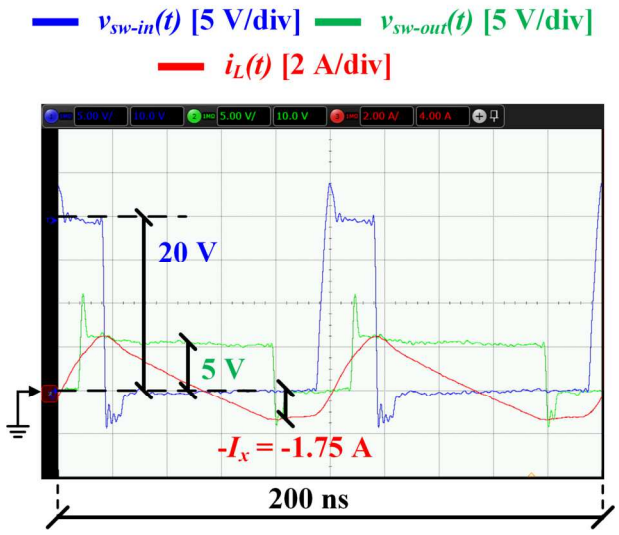
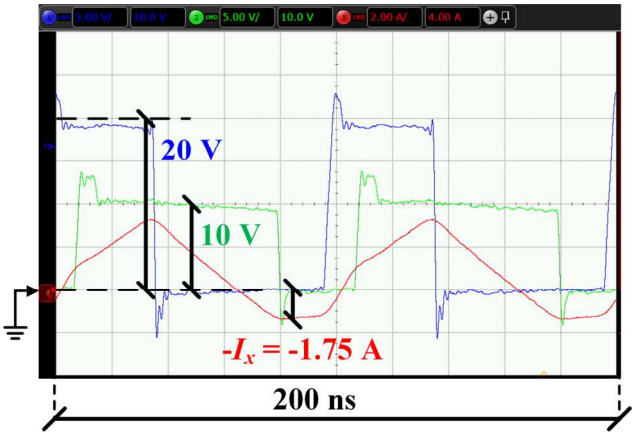


Fig. 8. Reproduction of the envelope of a multicarrier communication signal with a bandwidth of 100 kHz.

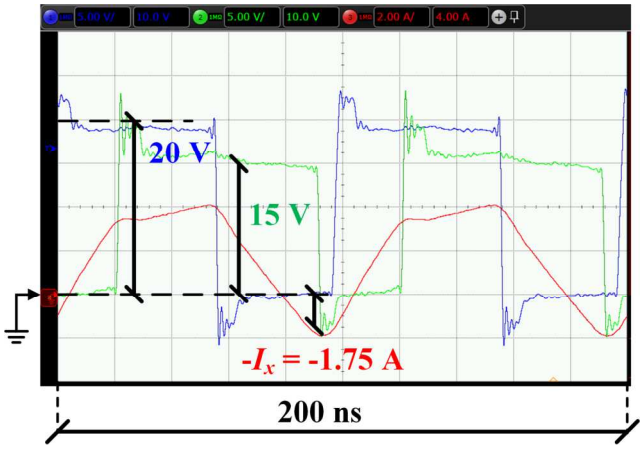
Fig 9 depicts a close-up image of the operation of the prototype during the reproduction of a varying output voltage at three different operating points: v_o = 5 V [Fig. 9(a)], v_o = 10 V [Fig. 9(b)] and v_o = 15 V [Fig. 9(c)]. Only step-down operation is tested, since a detailed description of the ZVS modulation for this mode is described in this work. For these values, the voltage waveform at the switching node of the input half-bridge $v_{sw\text{-}in}$ and the switching node of the output half-bridge $v_{sw\text{-}out}$, along with the waveform of the current i_L



(a)



(b)



(c)

Fig. 9. Operation of the FSBB converter during the reproduction of different values of v_o: (a) v_o = 5 V. (b) v_o = 10 V. (c) v_o = 15 V.

across the inductor are shown. As can be seen, the waveforms closely relate to those described in Fig. 3, achieving a ZVS current I_x equal to 1.75 A. The deadtimes has been exaggerated to verify the operation of the converter under ZVS conditions. Another evidence of the ZVS operation is the lack of ringing noise [17].

V. Conclusions

This paper introduces a control strategy proposed to achieve ZVS to minimize the switching losses of a FSBB during the reproduction of envelope waveforms in ET applications. In addition, some key considerations to design the components of a FSBB converter to be used in ET applications are also described. The proposed idea was evaluated by means of a prototype able to perform changes in its output voltage while achieving ZVS operating with the control method described in this paper. The results of the reproduction of different waveforms, including an arbitrary envelope, are also provided.

Acknowledgment

This work was supported in part by the Spanish Government under Project PID2022-136969OB-I00 and in part by the Principality of Asturias under Project SV-PA-21-AYUD/2021/51931, by the FEDER funding and "Severo Ochoa" Program Grant no. BP20-181.

References

[1] P. Asbeck and Z. Popovic, "ET comes of age: Envelope tracking for higher efficiency power amplifiers," *IEEE Microwave Magazine*, vol. 17, no. 3, pp. 16–25, Mar. 2016.

[2] B. Kim et al., "Push the Envelope: Design Concepts for Envelope-Tracking Power Amplifiers," *IEEE Microwave Magazine*, vol. 14, no. 3, pp. 68-81, May 2013.

[3] O. García, M. Vasić, P. Alou, J. Á. Oliver and J. A. Cobos, "An Overview of Fast DC–DC Converters for Envelope Amplifier in RF Transmitters," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4712-4722, Oct. 2013.

[4] G. T. Watkins and K. Mimis, "How Not to Rely on Moore's Law Alone: Low-Complexity Envelope-Tracking Amplifiers," *IEEE Microwave Magazine*, vol. 19, no. 4, pp. 84-94, June 2018.

[5] P. F. Miaja, A. Rodríguez and J. Sebastián, "Buck-Derived Converters Based on Gallium Nitride Devices for Envelope Tracking Applications," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 2084-2095, April 2015.

[6] J. Rodríguez, J. R. García-Meré, D. G. Aller and J. Sebastián, "Pulsewidth Modulated Three-Level Buck Converter Based on Stacking Switch-Cells for High Power Envelope Tracking Applications," *IEEE Transactions on Power Electronics*, vol. 37, no. 5, pp. 5786-5800, May 2022.

[7] S. Yerra, H. S. Krishnamoorthy and J. Hawke, "Cascaded Switching Capacitor based Multi-phase Three-Level Buck Converter for Communication Envelope Tracking," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 2836-2841.

[8] Y. Zhang, J. Strydom, M. de Rooij and D. Maksimović, "Envelope tracking GaN power supply for 4G cell phone base stations," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 2292-2297.

[9] M. Schulz, N. Schleippmann, K. Gosses, R. Chacon and B. Wunder, "Four Switch Buck/Boost Converter to Handle Bidirectional Power Flow in DC Subgrids," in *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Germany, 2020, pp. 1-8.

[10] H. -S. Lee and J. -J. Yun, "High-Efficiency Bidirectional Buck–Boost Converter for Photovoltaic and Energy Storage Systems in a Smart Grid," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4316-4328, May 2019.

[11] Y. Li and X. Ruan, "An Optimized Inductor Current Control for Intermediate Bus Converter With Hybrid-Switching Structure," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, USA, 2018, pp. 3818-3824.

[12] A. Kumar and P. Sensarma, "A Four-Switch Single-Stage Single-Phase Buck–Boost Inverter," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5282-5292, July 2017.

[13] L. Tian, X. Wu, Z. Zhou and F. Muhammad, "The MPPT Application of the FSBB Converter with MHz ZVS Digital Control," in *2022 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Guangzhou,Guangdong, China, 2022, pp. 1409-1413.

[14] V. Díaz, A. Barrado, A. Lázaro and P. Zumel, "Comparison of several modulation strategies for the Four Switch Buck-Boost converter," in *2023 IEEE 17th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, Tallinn, Estonia, 2023, pp. 1-6.

[15] S. Waffler and J. W. Kolar, "A Novel Low-Loss Modulation Strategy for High-Power Bidirectional Buck + Boost Converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 6, pp. 1589-1599, June 2009.

[16] Z. Zhou, H. Li and X. Wu, "A Constant Frequency ZVS Control System for the Four-Switch Buck–Boost DC–DC Converter With Reduced Inductor Current," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 5996-6003, July 2019.

[17] Y. Zhang, M. Rodríguez and D. Maksimović, "Output filter design in high-efficiency wide-bandwidth multi-phase buck envelope amplifiers," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, USA, 2015, pp. 2026-2032.