Four-switch buck-boost based module block for highly modular power architecture

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***Abstract*—This paper presents a novel power architecture that utilizes modular power blocks capable of working as Solar Array Regulator (SAR), Battery Charge Regulator (BCR), and Battery Discharge Regulator (BDR) without the need for hardware reconfiguration, while enabling parallel operation without centralized control. By eliminating the costs associated with hardware reconfiguration, the design and development time of the power subsystem is significantly reduced. Extensive analysis has been conducted to identify the best converter option, resulting in the selection of the four-switch buck-boost topology. To validate the proposed approach, a prototype representing a modular block has been designed and tested.**

Keywords—DC-DC, modular, SAR, BCR, BDR, Buck-boost

I. Introduction

A common satellite power subsystem in a regulated bus architecture is composed mainly of three blocks[1]: the Solar Array Regulator (SAR), that regulates power extraction from the solar panels, the Battery Charge Regulator (BCR) and the Battery Discharge Regulator (BDR), that take care of injecting or extracting power from the battery. These blocks are designed specifically for every mission and their design can be costly and time consuming. Given the recent trends in spacecraft design [2], where it is paramount to keep cost at a minimum, the use of modular architectures in the power subsystem can become an appealing option to the market.

With this condition in mind, a new architecture for the power subsystem is proposed. The power subsystem is subdivided into smaller power blocks, called Primary Distribution System (PDS). Each block consists of one converter or set of converters that can act as SAR, BCR or BDR without hardware reconfiguration needed. These modules are parallelizable and autonomous from one another, and thus there is no need for a central controller. Each block has a digital local controller. Although there is no direct communication between the modules, an external supervisor block gathers all the relevant telemetry from the modules and configures the role of each of them (house-keeping tasks).

This work focuses on the design of the converter and the rationale followed to select the topology. It is organized as follows. Section II focuses on the qualitative and quantitative analyses performed to select the best topology. Section III discloses the design of what would correspond to one of the modules. Section IV presents the experimental results.

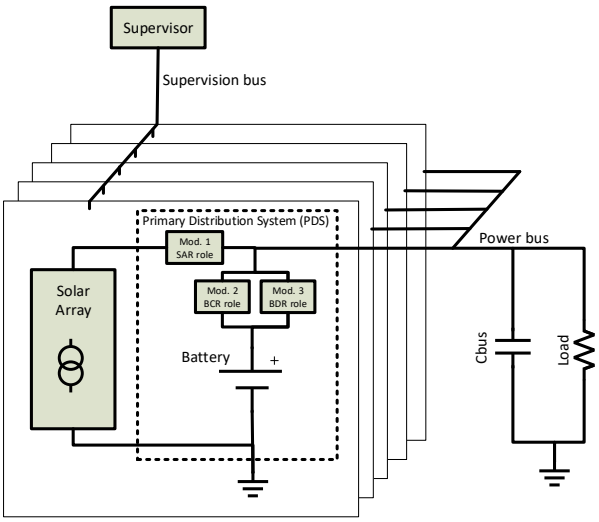

Fig. 1. Block diagram of new modular architecture

Section V covers the conclusions that were gathered in the previous sections.

II. Topology selection

The main objective in this section is to select a converter topology capable of acting as SAR, BDR or BCR. Given the extensive amount of options available and the time it would require to thoroughly analyze all, this selection is performed using a two-method analysis. The first method consists of a qualitative analysis that filters out the great majority of options. The remaining topologies are then subjected to a quantitative analysis that finally selects the best option.

A. Qualitative analysis

The qualitative analysis discards the less optimal options. The criterion to select the best topology is based on several parameters, namely: number of semiconductors, number of magnetic elements, number of capacitors, number of required converters to implement the regulated bus, complexity of the control and supervisor modules, including parallelization, bus limitations (e.g., buck converter can only step-down voltage), efficiency.

A summary of the most relevant topologies that have been analyzed are on TABLE I. Among the three assessed categories, unidirectional topologies are discarded in

TABLE I. TOPOLOGIES STUDIED

Topology	Converters total	Semiconductors	Inductors	Capacitors	Control	Supervisor	Bus lim.	Efficiency
Buck or Boost	3	12	3	6	Simple	Complex	Y	Very High
Weinberg[3]	3	21	6	6	Simple	Complex	Y	High-Very High
Non Inverting BuckBoost	3	18	3	6	Simple-Average	Complex	N	High
Full Bridge, Full wave	3	24	6	9	Simple	Complex	N	High
Push Pull	3	18	6	9	Simple	Complex	N	High
Bidirectional 2-level Switched-Capacitor	2	16	2	8	Complex	Average	Y	High
4-switch BuckBoost[4]	2	12	2	4	Average	Average	N	High
Bidirectional Buck/Boost	2	8	2	4	Average	Average	Y	High
DAB	2	16	4	6	Complex	Average	N	High
Bidirectional LLC Kim 2015[5]	2	24	10	8	Complex	Average	N	High
Teng 2019[6]	2	18	4	6	Complex	Average	N	High
TAB	1	12	3	5	Very Complex	Simple	N	High
Interleaved Boosts with Full bridge (integrated)	1	9	4	3	Very Complex	Simple	Y	High
Three-port asymmetrical Half Bridge	1	8	2	4	Very complex	Simple	Y	Medium-High

comparison to bidirectional ones if used for implementing the regulated-bus scheme of the PDS.

The reason is that no real advantage can be obtained. The simplest unidirectional topology that can be used is the non-inverting buck-boost, as other topologies present problems with the static gain or the connection due to voltage inversion. But using its bidirectional version provides more advantages at almost no cost by replacing the diode with a MOSFET and driver. This does not increase the number of switches or magnetics but reduces in one the number of modules to be implemented in the PDS. Regarding isolated unidirectional topologies, including three transformers when isolation is not actually a requirement implies that the weight and cost of this kind of topologies is deemed too high.

There is a clear advantage of bidirectional topologies over unidirectional ones. Not only size and weight are expected to be reduced due to not needing a full converter to perform battery charge, but also the complexity of the supervisor algorithm and the communication ring is partially alleviated as there are no converters in antiparallel, which may recirculate power instead of driving it between two elements. At the same time, and except for the non-inverting buck-boost, the unidirectional converters have either limited static gains or voltage inversion, limiting their usage. If isolated topologies are brought into the equation, when galvanic isolation is not an actual requirement, the result is a bulky design.

The use of three-port bidirectional converters is an option to consider mainly because of the reduction of components, especially if magnetic integration is achieved. Also, the power flow is not split among different converters, and a single control is required. But focusing only on this option is less than optimal, nonetheless. The main disadvantage is that modularity is not simple and not as accurate as with two port topologies. The number of modules in parallel is determined by the highest required power in each port divided by the rated power of that topology port. Therefore, it is likely that many missions will have more installed power than required in some of the ports.

Having considered all the options and seeing the obvious advantage of bidirectional two port and three port topologies, they seem to be the obvious choice for scalability, compact size and modularity. Among them, the four-switch buck-boost or the bidirectional buck are the best ones. Choosing the former or the latter strongly depends on the possibility of imposing the condition that the voltage in the SA port is always higher than that of the bus, and the bus voltage is always higher than the battery voltage, assuming a bus-regulated scheme.

B. Quantitative analysis

This analysis is performed so that a final figure of merit, which includes losses (i.e., efficiency) and volume of the inductors, is evaluated. This figure of merit (obtained after an optimization process is run for each topology) will be used to compare the selected topologies with a quantitative criterion.

To evaluate the topology, an optimization process is first run to select the most adequate semiconductors and inductors. This process is run evaluating two variables (switching frequency f_{sw} and inductor current ripple ΔI_L) to find the optimum pair. Besides, for each pair of those two optimization variables, all possible combinations of input and

output voltages are evaluated. The results are all obtained at rated power, as the main goal is to compare topologies.

1) Conditions

The analysis is performed considering a bus voltage in the range of 24 to 32 V, a battery voltage in the range of 22 to 34 V and a solar array voltage in the range of 30 to 60 V. The rated power of the module is 500 W. The switching frequency may vary between 30 to 200 kHz and the relative current ripple in the inductor goes from 0.05 to 0.45 (at full load).

2) Optimum semiconductor selection

This study considers that the converters have been optimized to have the lowest losses. This optimization is made for each pair $f_{sw} - \Delta I_L$ and the corresponding required inductor value and for each input and output voltage combination (as it can be seen in Fig. 2). Once again, this inductor value is calculated for the worst case of input and output voltage and kept constant for each $f_{sw} - \Delta I_L$ pair. The output of this selection procedure will be the MOSFET with the lowest losses for each $f_{sw} - \Delta I_L$ and V_{in}-V_{out}. Once all the V_{in}-V_{out} pairs have been assessed for a given $f_{sw} - \Delta I_L$ pair, and the corresponding MOSFETs have been selected, the one with the highest losses will be chosen as the optimum for the $f_{sw} - \Delta I_L$ under assessment, as it will ensure that it can withstand the worst operating conditions in terms of junction temperature.

3) Optimum inductor selection

A similar approach is being followed for the design of the inductor. All the V_{in}-V_{out} pairs are assessed for each $f_{sw} - \Delta I_L$ pair. In each point, an optimized design inductor procedure is called, that minimizes core and copper losses while avoiding core saturation. Thus, the smallest magnetic element that can withstand the losses is obtained. Once all the V_{in}-V_{out} pairs have an optimized inductor assigned, the one with the highest losses is selected for the current $f_{sw} - \Delta I_L$ pair, to assure the inductor withstands the worst conditions.

4) Efficiency estimation

An operating point is defined (V_{in}-V_{out} pair). For it, and for the all the $f_{sw} - \Delta I_L$ pairs, the efficiency is calculated according to the selected MOSFETs in each case. The main difference with the previous point is that efficiency is calculated for a single operating point, considering the best MOSFETs in each $f_{sw} - \Delta I_L$ case. In the same way, the magnetic component is designed for that $f_{sw} - \Delta I_L$ pair (but not specifically for the V_{in}-V_{out} pair).

5) Losses

The losses of the converter are calculated for each operating point (V_{in}-V_{out} pairs) and for the nominal power. It is assumed that in the 4-switch buck-boost, given the possibility of increasing or reducing the voltage, one of the ports is always connected to the bus, while the other port is connected to the solar array or the battery. In the case of the synchronous buck, that is not possible. Hence, the "output port" (to keep consistency with the other topologies) is connected to the solar array or the bus, while the output port may be connected to the bus or the battery. Fig. 3 shows the results of both.

6) Figure of merit

The figure of merit efficiency divided by weight of the magnetic core is calculated for every $f_{sw} - \Delta I_L$ pair. Then, the optimum pair is selected as the one with the highest value on the figure of merit.

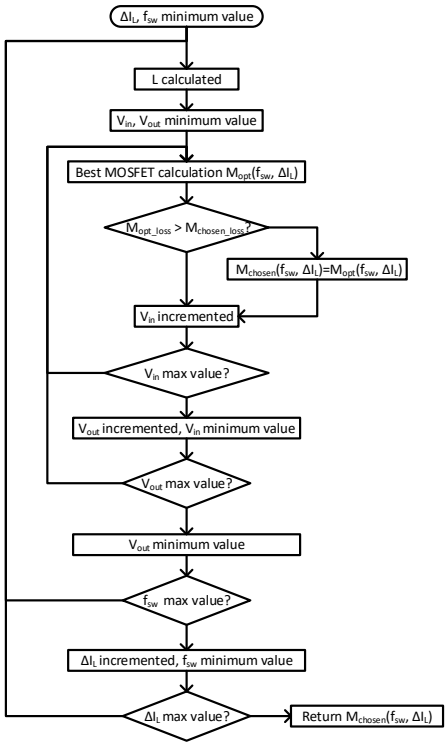

Fig. 2. Flow diagram to select the optimal semiconductor.

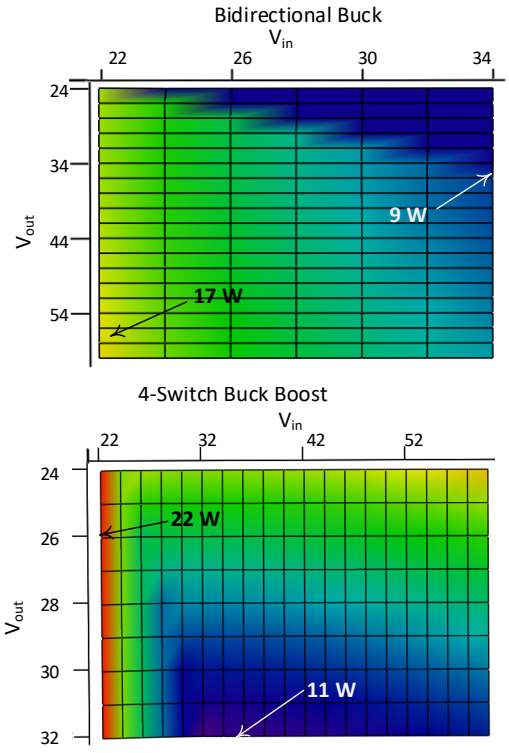

Fig. 3. Losses analysis of the bidirectional buck converter and the 4-switch buck-boost.

Fig. 4 shows the results obtained in the calculation of the figures of merit under different conditions. In general, transitioning to higher ripple and frequencies improves this figure of merit. Nonetheless, given that only real magnetic cores are considered, there are abrupt changes in the weight depending on the core selected by the optimization algorithm. It can also be seen that the advantage of the bidirectional buck

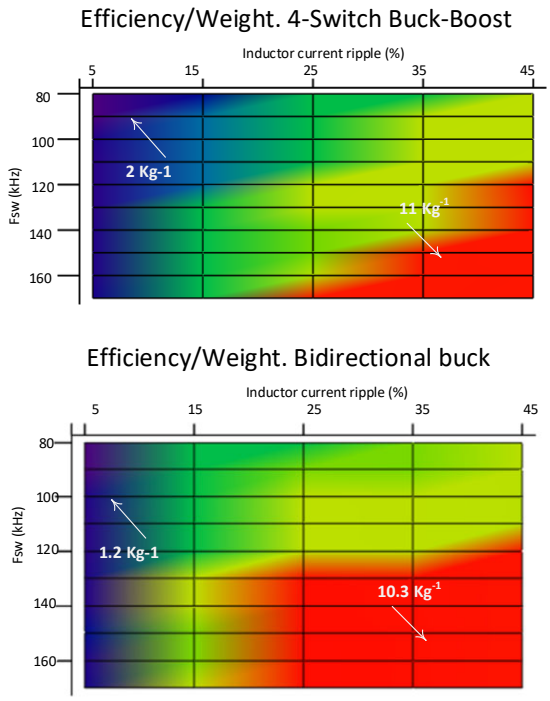

Fig. 4. Figure of merit calculation of the bidirectional buck vs four-switch buck-boost.

is not of much significance over that of the four-switch buck-boost, especially considering that the buck-boost has no voltage limitations when it comes to the static gain.

III. System Implementation

Fig. 5 shows the block diagram that corresponds to each of the modules. Based on the findings from the previous section, a four-switch buck-boost converter is the chosen topology to act as SAR, BCR or BDR with the same hardware configuration and only depending on the control algorithm to be one or the other.

A. Reliability and Component Selection

Although all the components used are Commercial-Off-The-Shelf (COTS), it has been made sure that their radiation-hardened counterparts were available, or components of equivalent characteristics. In terms of reliability, the modules have been designed to be single point failure free [7] and they are compliant with FMECA analysis as per [8]. Given the independent nature of the modules, as they wouldn't need to interact between one another, redundancy can be obtained at block level.

B. Telecommand

The module is externally commanded by an external controller, which in this case it is aimed to be an FPGA. This controller is able to send SET and RESET telecommands to force a turning on or turning off the converter. They are edge triggered. Priority has been given to the RESET signal in case SET and RESET are triggered at the same time. This is a safety method that avoids accidentaly turning on an already deactivated converter.

An additional signal is used that also prevents accidentaly turning the converter on when the FPGA has partial failures and maybe latches the RESET signal. It is the watchdog (WDG) signal, that requires the FPGA to send a clock signal to avoid triggering a turn off of the module. Fig. 6 shows the designed circuit. The SET signal, active LOW, is activated by the FPGA to turn the converter on, and all the protections, RESET, and WDG signals control the turning off. Activation is made through AND operation, given that they are active LOW. This way, every time an event occurs the protections will trigger.

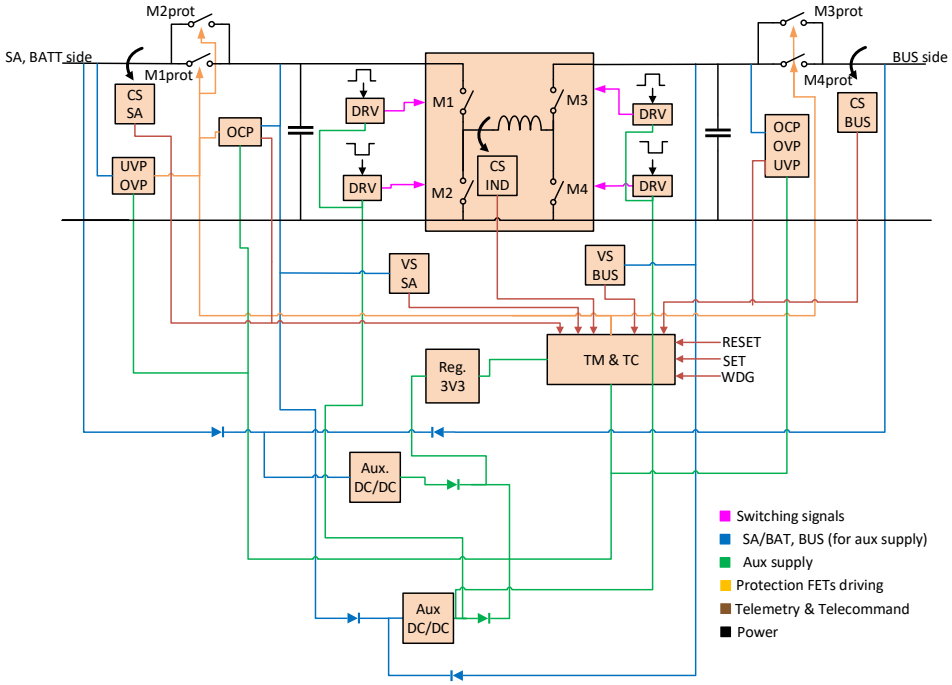

Fig. 5. System block diagram of the proposed converter.

This work has been funded by the Spanish government through the PID2021-127707OB-C21 project, the Principality of Asturias through project SV-PA-21-AYUD/2021/51931 and the Severo Ochoa grant BP21-207 and ESA through contract No. 4000129432/19/NL/AS/hh "Health monitoring of Digitally Controlled Flexible Converters".

C. *Auxiliary supply*

Auxiliary supplies allow initial turn on of the converter by the external controller. The additional circuitry that surrounds the converter (drivers, comparators, sensors, etc) is powered up by two auxiliary switching converter modules that provide 5V to all these elements. Only one of the auxiliary supplies gets power from outside the protection FETs, that are used to turn on the external controller and allow it to send a SET signal to the module. It also provides power to the protections and sensors. Once the protection FETs are on, the auxiliary supply from inside the protection FETs gets activated and powers up in addition to the previously mentioned circuitry the switching drivers. Due to being outside the protection FETs, to comply with FMECA analysis, they have their own protection circuitry, avoiding failure propagation. Fig. 7 shows a block diagram of the auxiliary supply configuration.

D. *Protections*

As it was determined during the qualitative analysis process, the four-switch buck-boost requires additional protection switches to isolate the converter in case of switch failure. Thus, if one of the converter switches fails in shortcircuit (M1, M2, M3 or M4), the module can still be isolated and the failure will not propagate. Therefore, it is still compliant with FMECA and no harm will be caused to other elements in the power subsystem. Switching of these protection FETs is commanded by an external control unit (i.e. an FPGA). Turn off can be activated by either the embedded protections (overvoltage, overcurrent, and undervoltage) or the external control.

E. *Telemetry*

Each module sends input and output voltage and current, and inductor current data to the supervisor. With this information, the supervisor can decide whether the module is still healthy and running or if it should be turned off due to certain damage and its power capabilities accomodated to other modules.

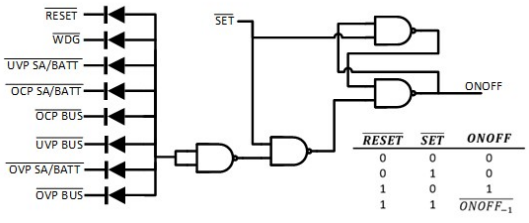

Fig. 6. Logic used to activate the protection switches with its truth table.

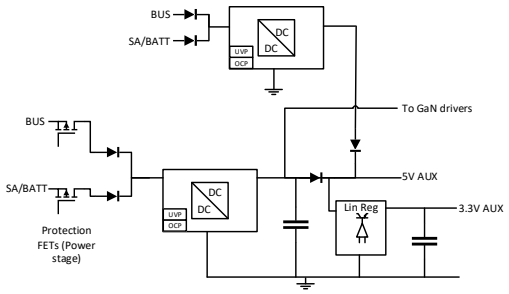

Fig. 7. 5V Auxiliary supply block diagram

IV. RESULTS

A 500 W prototype corresponding to one of the converters has been developed. Given the availability of components at the moment of design, it has been designed for a 100 V bus using gallium nitride as switching elements (GS66516B), whereas the protection FETs employ P-Channel. The voltage range on the battery/solar array side is 80-150 V. A picture of the module is shown in Fig. 8. It has been designed following the specifications listed on TABLE II. All the components used are commercial, but with equivalent radiation-hardened versions available.

To verify bidirectional capabilities, efficiency tests have been run in open loop, simulating power flow in both directions (e.g., battery charge/discharge and solar array regulation), reaching values close to 97%, as it can be seen in Fig. 9. Fig. 10 shows converter operation in boost mode from the solar array/battery side to the bus under worst conditions (minimum input voltage). In the same way, Fig. 11 shows converter operation in buck mode from the solar array/battery side to the bus side under worst conditions (minimum input voltage). V_{BUS} is the bus voltage, V_{BAT} is the voltage from the battery/solar array side, V_{DS_HIGH} is the drain- source voltage of the high side switching element, and I_L is the inductor current.

TABLE II. CONVERTER SPECIFICATIONS

Bus voltage	100 V
Battery voltage	80 V
Solar array voltage	150 V
Output capacitor	35.2 µF
Switching frequency	180 kHz
Inductance	83 µH
Current ripple	2.5 A
Output current	5 A
Bus power	500 W

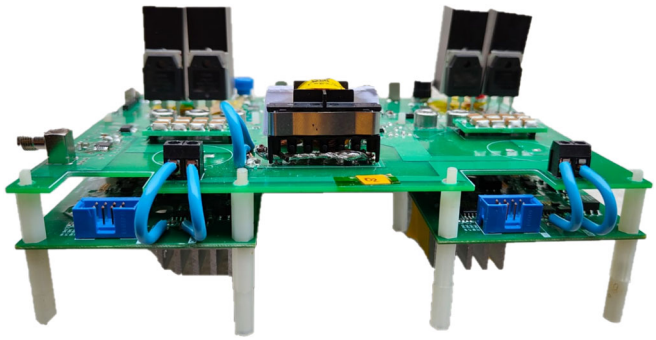

Fig. 8. Prototype built

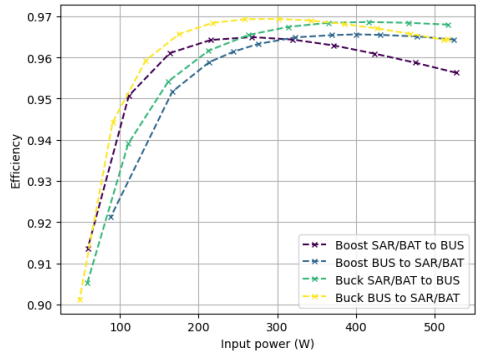

Fig. 9. Module efficiency for buck mode and boost mode

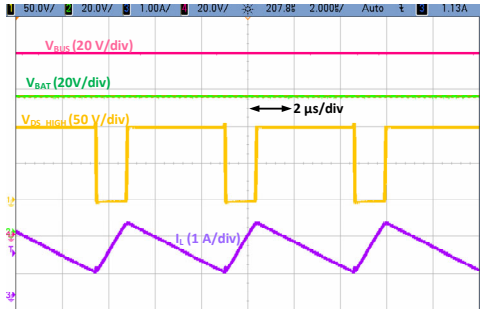

Fig. 10. Module operation in boost mode

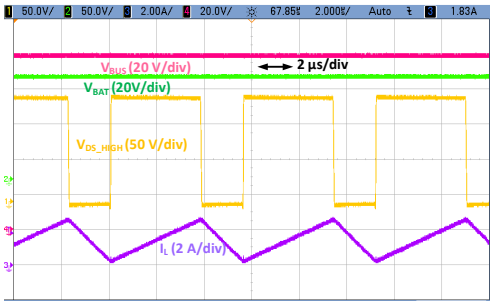

Fig. 11. Module operation in buck mode

V. Conclusions

This work proposes the use of a module that can work as a SAR, BDR or BCR without the need of hardware reconfiguration. It also allows parallelization and avoids the need of using a main error amplifier, becoming a versatile tool to consider in new space missions. A tradeoff to determine the best converter topology to be used on each module has been made, resulting in the four-switch buck-boost converter being the most suitable option. The prototype built has all the components available in a radiation-hardened version or an equivalent one, and the design passes FMECA analysis.

Acknowledgment

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