Low-Cost LED Driver based on a Low-Dropout Current Regulator Combined with a Quasi-Resonant Buck Pre-Regulator

Javier Ribas, *Senior Member, IEEE*, Pablo J. Quintana, *Member, IEEE*, Antonio J. Calleja, *Senior Member, IEEE*, Jesús Cardesín, *Senior Member, IEEE*, Diego Rodríguez, *Student Member, IEEE,* and Marco A. Dalla Costa, *Senior Member, IEEE*

***Abstract*- The ease of control of LEDs allows the development of drivers with luminous flux control without significantly increasing the cost. The preferred control system to minimize light color deviation at low power levels is through pulse width control. However, IEEE PAR1789 recommendations indicate that the frequency of these pulses should be greater than 1.5kHz to eliminate the adverse effects of light flicker. This strongly affects the design of LED drivers. Among other effects, it makes it more difficult to avoid the appearance of audible noise in the magnetic elements and can limit the ratio between the minimum and maximum power achievable without losing linearity.**

In this paper, a new solution based on a quasi-resonant buck in series with a low-voltage-drop current regulator is presented. The quasi-resonant buck is used to minimize the headroom voltage of the dissipative current regulator thus maximizing the efficiency.

The operation of the resonant converter is analyzed using an energy-balance approach to model the circuit behavior during the resonant transitions. Based on this approach, a straightforward design procedure is proposed and applied to a design example. This example is used to build and test a low-cost experimental prototype based on the L6562A control integrated circuit. This paper is accompanied by several LT Spice files demonstrating the basic operation of the proposed circuit.

I. Introduction

In recent years, LED lighting systems have prevailed over other alternative artificial light sources, such as discharge or incandescent lamps, mainly due to their greater efficiency and long working life. Another interesting advantage of LED lamps is their ease of control. This makes it possible to create artificial illumination systems with lighting level control or even with adjustable color by combining LEDs of different spectrums inside the same luminaire. The popularization of the internet-of-things, combined with the cost reduction of all associated systems, has led to a significant growth of the lighting systems with dimming and color control that are available in the market. For all this, developing of simple power topologies that use low-cost components and allow precise control of the current supplied to the LED lamp is particularly interesting.

Pulse width control is the most widely used control strategy to regulate the light level. Other strategies, such as constant current control, give rise to much greater variations in the color of the light produced in most of the LED diodes currently used in lighting systems [1][2]. However, pulse width control can lead to unacceptable flicker levels for many applications.

Currently, the most accepted reference to estimate the maximum allowable flicker level for lighting applications is the IEEE PAR1789 standard [3]. This standard recommends using frequencies above 1.5 kHz for pulse width control to eliminate the adverse effects of light flicker on human health. Complying with this recommendation strongly impacts the design of the LED driver. Among other effects, it makes it more difficult to avoid the appearance of audible noise in the magnetic elements of the electronic converter and can limit the ratio between the minimum and maximum power that can be achieved without losing linearity, especially when the rise and fall times of the LED current become a significant part of the PWM period.

In this work, a new solution based on the combination of a resonant buck converter followed by a low-drop linear current regulator is presented. The simplified schematic of the proposed circuit is shown in Fig. 1. The resonant buck converter is used to minimize the voltage drop across the linear current regulator thus minimizing the power dissipated by this stage. The low drop-out current source regulator (LDOCS) allows precise control of the current waveform supplied to the LED lamp while keeping a high efficiency.

An energy balance approach is used to analyze the behavior of the modified buck converter during the resonant transitions. This technique is similar to the one used by the authors in [4]

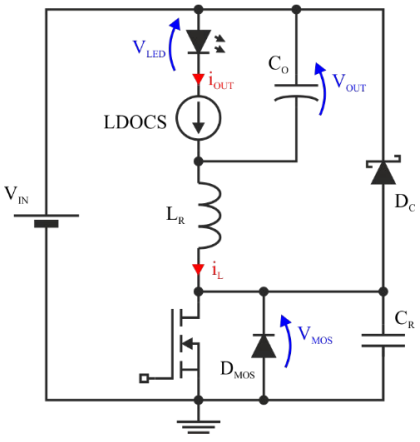

Fig. 1 Simplified schematics of the proposed quasi-resonant buck converter combined with a low-drop current regulator.

and it allows for avoiding the use of the fundamental approach and its subsequent accuracy loss [5].

The remaining of the paper is organized as follows. In first place a brief review of the state of the art is made. Other single-switch resonant converters that can be found in the literature and how they compare with the proposed configuration are discussed. Several alternatives for using low-drop linear regulator for LED current control are also described. In section three, the operation of the proposed converter is thoroughly analyzed, and the static design equations are obtained. These equations are used to obtain some general design charts whose use is described using a practical example. A simplified procedure to obtain the small-signal dynamic model of the converter is described in section four. Section five is used to address the operation of the prototype built for experimental verification. This prototype is based on the L6562A low-cost control integrated circuit. The L6562A is intended for controlling boundary-mode single-switch power factor correction topologies but it can be adapted to control the proposed topology using few additional components. The experimental results obtained with this prototype are presented in section six. The last section is dedicated to summarizing the conclusions of this work.

II. Brief Review of the State-of-the-Art

As mentioned in the previous section, the proposed circuit is based on the combination of a quasi-resonant buck converter and a low-dropout linear regulator. Both types of solutions can be found separately in multiple bibliographical references.

In the late 1980s and early 1990s, numerous papers were published with different proposals for resonant and quasi-resonant converters [6]-[13]. In these converters, the resonant transfer of energy between some of the inductors and capacitors that are part of the circuit is used to minimize switching losses. These configurations allow working at very high frequencies while maintaining high efficiency. For example, some of the references describe resonant converters working at several tens of megahertz [14][15].

However, these converters also have some drawbacks. In first place, the reduction in switching losses is normally associated with an increase in conduction losses when compared to the non-resonant equivalent configuration. Besides, these circuits are more complex to design and analyze. In most resonant topologies, the operating point must be within strict limits to prevent a strong increase in switching losses. Normally, its control requires modifying the switching frequency and, in some designs, the required excursion of the frequency can make it difficult to implement filters for compliance with electromagnetic emission regulations.

Fig. 2 shows the best-known quasi-resonant buck converter configurations as they were described in [6] and [7], published in years 1987 and 1990 respectively. In these configurations, a capacitor and a resonant inductance are added to the basic buck converter to obtain zero-current or zero-voltage switching, thus reducing switching losses. In both references, it is assumed that the resonant transitions are fast enough to consider a constant

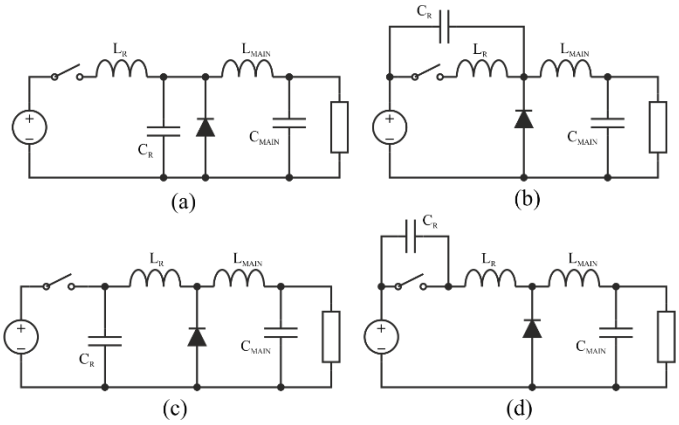

Fig. 2 Basic quasi-resonant buck configurations: (a) L-type current mode, (b) M-Type current mode, (c) T-Type voltage mode and P-Type voltage mode resonant switches.

current through the main inductance, which considerably simplifies circuit calculation. Although the proposed converter can be considered as a simplified version of the quasi-resonant buck converter with M-type or P-Type switches, the presence of an additional inductance not only complicates the analysis of the circuit, but also makes its practical implementation considerably more expensive.

In reference [8], published in 1988, a synchronous quasi-resonant step-down converter whose waveforms and operation are similar to the one proposed is described. However, the presence of two switches makes both the power stage and the control more complex.

Although the largest number of publications per year regarding quasi-resonant converters occurred between the late 1980s and the year 2000, interest in this family of circuits is still very high, and it is possible to find many recent references where they are used for multiple applications [16]-[18], including LED drivers [19]-[25]. Among these publications, the one that presents the greatest similarity with the proposed configuration is [18]. However, in this work the authors neglect the effect of the resonant charge of the switch capacitance, which introduces a significant error, especially when working under low load conditions.

In the present work, the quasi-resonant buck converter is used to minimize the voltage drop in the linear regulator that controls the current through the LED lamp. Low drop-out current regulators can also be found in recent bibliography [26], and there are several control integrated circuits in the market specifically designed to facilitate its practical implementation (e.g. LM3464, LM3463, …), although, most of them are designed to work with PWM frequencies below 500 Hz, which cannot be used if compliance with the flicker recommendations of the IEEE PAR1789 standard is required.

III. Operation of Proposed Circuit

The quasi-resonant buck converter shown in Fig. 1 behaves basically like a standard buck with resonant charging and discharging of the capacitor placed in parallel with the switch. Thus, in addition to the linear charging and discharging stages

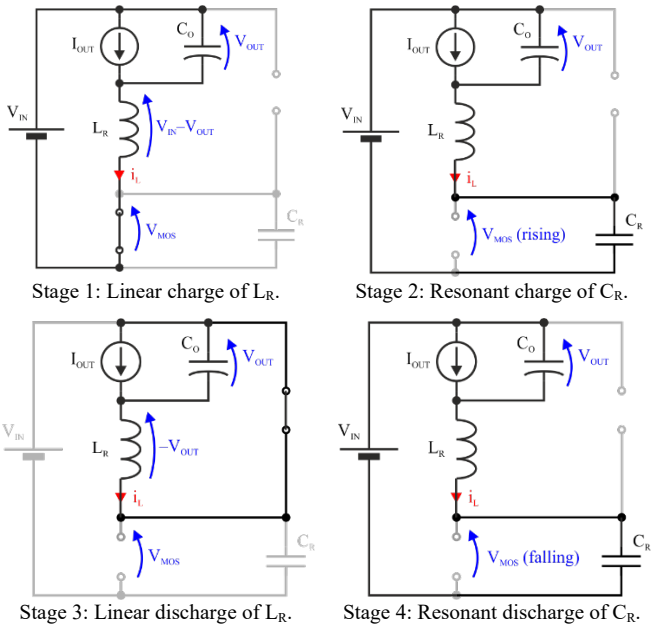

Fig. 3 Operation stages of the proposed circuit.

of the inductance (stages 1 and 3 in Fig. 3), there are two additional stages in which the capacitor C_R is resonantly charged or discharged by energy exchange with the inductor L_R (stages 2 and 4 in Fig. 3).

The value of the output capacitor C_O is high, thus V_{OUT} can be considered constant during a switching cycle and the resonant transitions of stages 2 and 4 are only affected by the values of inductor L_R and capacitor C_R.

To obtain low switching losses it is critical to switch on the transistor when C_R is fully discharged. The control strategy that will be used to fulfill this condition is switching on when the zero crossing of V_{MOS} is detected and using the switch on time t_{ON} as the control parameter of the converter (ZC-t_{ON} control).

Fig. 4 shows the evolution of the inductor current and the MOSFET voltage. As it can be seen, during stage 1 the MOSFET is on, the inductor current i_L increases linearly from i_1 to i_2, and the following expression can be obtained:

$$i_2 - i_1 = \frac{V_{IN}-V_{OUT}}{L_R} \cdot t_{ON}. \quad (1)$$

The MOSFET is switched off at the end of stage 1. During stage 2, part of the energy stored in the inductor is transferred

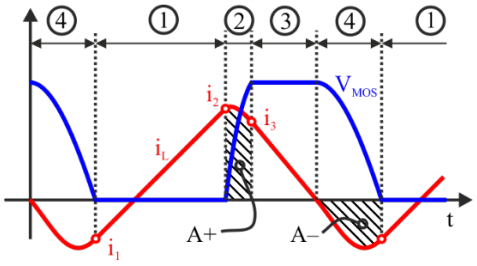

Fig. 4 Basic operation of the proposed quasi-resonant converter.

to capacitor C_R, increasing its voltage from zero to the input voltage V_{IN}. The equivalent circuit at the beginning of stage 2 is represented at the left side of Fig. 5. Considering that a capacitor charged to any initial voltage behaves like the same capacitor discharged and connected in series with a constant voltage source with that initial voltage, the inductor current evolution during stage 2 can also be analyzed with the circuit shown at the right of Fig. 5. The capacitor voltage will also have the same evolution but with an offset equal to V_{IN}-V_{OUT}. In this AC equivalent resonant circuit, power is transferred between C_R and L_R following a sinusoidal pattern at the natural resonant frequency of the circuit ω_R:

$$\omega_R = \frac{1}{\sqrt{L_R \cdot C_R}}. \quad (2)$$

Fig. 6 shows the current and voltage evolution in the AC equivalent during stage 2. The energy balance between the initial and final moments of stage 2 provides the following expression:

$$\frac{1}{2} \cdot L_R \cdot {i_2}^2 + \frac{1}{2} \cdot C_R \cdot (V_{IN} - V_{OUT})^2 = \frac{1}{2} \cdot L_R \cdot {i_3}^2 + \frac{1}{2} \cdot C_R \cdot {V_{OUT}}^2 \quad (3)$$

The duration of stage 2 can be calculated as:

$$t_2 = \sqrt{L_R \cdot C_R} \cdot \left(\cos^{-1}\left(\frac{i_2}{\sqrt{{i_3}^2 + \frac{C_R}{L_R} {V_{OUT}}^2}} \right) + \cos^{-1}\left(\frac{i_3}{\sqrt{{i_3}^2 + \frac{C_R}{L_R} {V_{OUT}}^2}} \right) \right). \quad (4)$$

Once capacitor C_R voltage reaches V_{IN}, the clamping diode D_C starts conducting and the inductor L_R is discharged linearly

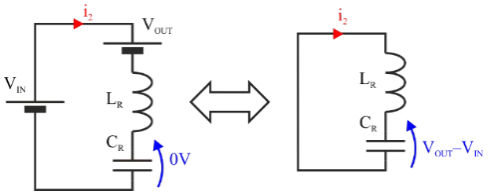

Fig. 5 Capacitor C_R resonant charging circuit at the beginning of stage 2 and its equivalent simplified AC circuit.

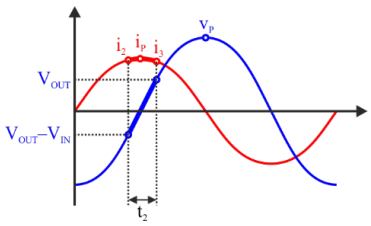

Fig. 6 Voltage and current evolution in the equivalent AC resonant circuit of stage 2.

during stage 3. The duration of this interval can be calculated using the following expression:

$$t_3 = \frac{L_R}{V_{OUT}} \cdot i_3. \quad (5)$$

Once the inductor L_R is fully discharged, the circuit enters stage 4, where C_R gets fully discharged, and the energy stored in it is transferred to the inductor L_R. This stage can be analyzed using the same method as in stage 2. Fig. 7 shows the discharging circuit at the beginning of this stage and its simplified AC equivalent, where the DC sources of the previous circuit have been included in the initial voltage of the capacitor C_R. Fig. 8 shows the voltage and current evolution during this interval, where the energy balance between the initial and final instants provide the following equation:

$$\frac{1}{2} \cdot C_R \cdot {V_{OUT}}^2 = \frac{1}{2} \cdot C_R \cdot (V_{IN} - V_{OUT})^2 + \frac{1}{2} \cdot L_R \cdot {i_1}^2. \quad (6)$$

From this expression, the i_1 value can be calculated as:

$$i_1 = -\sqrt{\frac{C_R}{L_R} \cdot V_{IN} \cdot (2V_{OUT} - V_{IN})}. \quad (7)$$

From which it can be deduced the following design restriction:

$$V_{OUT} > \frac{V_{IN}}{2}. \quad (8)$$

This means that the output voltage of the proposed converter must be higher than half the input voltage to allow a complete discharge of the resonant capacitor before the switch is turned on. The duration of stage 4 can be calculated using the following formula:

$$t_4 = \sqrt{L_R \cdot C_R} \cdot \left(\frac{\pi}{2} + \sin^{-1}\left(\frac{V_{IN} - V_{OUT}}{V_{OUT}}\right)\right). \quad (9)$$

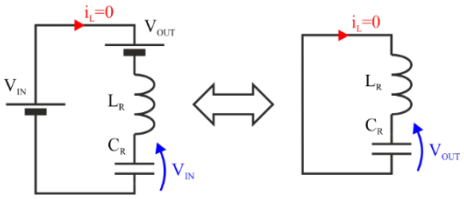

Fig. 7 Capacitor C_R resonant discharging circuit at the beginning of stage 4 and its equivalent simplified AC circuit.

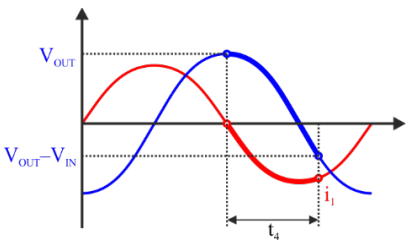

Fig. 8 Voltage and current evolution in the equivalent AC resonant circuit of stage 4.

The converter switching period can be calculated as the duration of all four stages combined:

$$T = t_{ON} + t_2 + t_3 + t_4. \quad (10)$$

And the average output current I_{OUT} can be calculated as:

$$I_{OUT} = \frac{1}{T}\left(\frac{i_1 + i_2}{2} \cdot t_{ON} + \frac{i_3}{2} \cdot t_3\right). \quad (11)$$

Using the values obtained from expressions (4), (5) and (9), equation (10) can be rewritten in the following form:

$$T = F_1(V_{IN}, V_{OUT}, t_{ON}, L_R, C_R). \quad (12)$$

In a similar way, using (1), (3), (5) and (7), equation (11) can be expressed as:

$$I_{OUT} = F_2(V_{IN}, V_{OUT}, t_{ON}, L_R, C_R). \quad (13)$$

These two expressions can be normalized using the following base values for impedance and time:

$$Z_{BASE} = \sqrt{\frac{L_R}{C_R}} \quad (14)$$

$$t_{BASE} = \sqrt{L_R \cdot C_R}. \quad (15)$$

This way, the normalized switch on-time τ_{ON} can be defined as:

$$\tau_{ON} = \frac{t_{ON}}{\sqrt{C_R \cdot L_R}}. \quad (16)$$

The output to input voltage ratio will be defined as:

$$\gamma = \frac{V_{OUT}}{V_{IN}}. \quad (17)$$

This way, the normalized frequency can be obtained from equation (12) and expressed in the following form:

$$\phi = {F'}_1(\gamma, \tau_{ON}). \quad (18)$$

And the normalized ratio between the output current and the input voltage ψ can be calculated as:

$$\Psi = \frac{I_{OUT}}{V_{IN}} \cdot Z_{BASE} = {F'}_2(\gamma, \tau_{ON}). \quad (19)$$

Fig. 9 represents the relation between ψ and γ for different τ_{ON} values obtained from expression (19). As it can be seen, assuming a constant input voltage, for any given γ between 0.5 and 1, it is possible to control the output current by modifying the switch on-time.

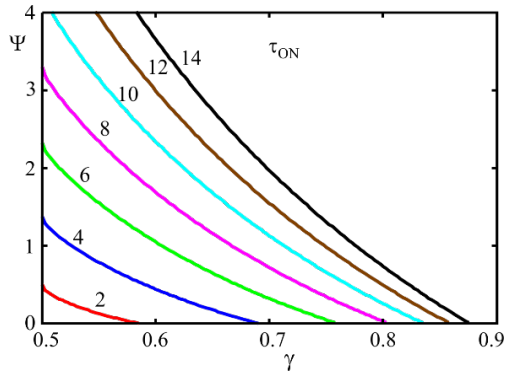

Fig. 9 Normalized I_{OUT}-V_{IN} ratio (Ψ) as a function of the V_{OUT} to V_{IN} ratio (γ) for different values of the normalized switch on-time τ_{ON}.

Expressions (18) and (19) do not depend on the L_R and C_R values and can be used to design the converter in a straightforward way, as it will be discussed in the next paragraph.

A. Design example

As it was previously stated in equation (8), the proposed resonant converter must operate with an output voltage higher than half the input voltage. A suitable range for the output-to-input voltage ratio (γ) will be between 0.55 and 0.75, as lower values will increase the risk of losing ZVS switching, and higher values will lead to excessive reactive power and lower efficiency.

This restriction provides a narrow range for selecting an appropriate input voltage once the load voltage margin is known. In this example, the load was composed of 5 phosphor-converted white LED in series handling a nominal current of 0.6A, according to the maximum and minimum lamp voltage values given by the manufacturer and assuming a 0.5V margin to estimate $V_{OUT(min)}$ (see Table I), the maximum input voltage must be lower than 27V to comply with (8). In this design, a 24V input signal was chosen, giving a γ_{max} of 0.698 and a γ_{min} of 0.594. This 3-volt margin allows the converter to handle up to a 12.5% peak low-frequency input voltage ripple without losing the ZVS condition.

The minimum output power in LED dimming ballasts can easily be well below 5% of its nominal value. Besides, in the proposed circuit, neither the turn-on time of the transistor nor the frequency present strong variations when the output power is low, so both values can be estimated assuming that the minimum design power is approximately zero.

Fig. 10 shows the normalized switching frequency ϕ as a function of the output-to-input voltage ratio γ for different τ_{ON} values. This figure is the graphical representation of expression (18). The curve designated as ψ=0 correspond to zero output current and can be used to estimate the maximum frequency at the minimum output voltage (γ_{min}), providing a ϕ_{max} value of 0.147. In this design, the selected maximum and minimum frequencies were 295 kHz and 100 kHz respectively. To maintain the same proportion, the minimum normalized frequency (ϕ_{min}) must be 0.05, so the curve that relates the normalized frequency to the normalized output voltage at nominal current ($\psi=\psi_{nom}$) should cross the point ϕ_{min} -γ_{max} in Fig. 10. This can be used to obtain the nominal normalized output current to input voltage ratio ψ_{nom}. The resonant inductor and capacitor values can be calculated by de-normalizing ϕ_{min} and ψ_{nom}.

TABLE I
DESIGN EXAMPLE PARAMETERS

LED Lamp Characteristics			
LED type	V_{FWD}(min)@350mA	V_{FWD}(max)@350mA	Configuration
Oslon SSL 80	*2.75 V*	*3.25 V*	*5 LED in series*

Basic Design Parameters		
Input voltage	Min. output voltage	Max. output voltage
V_{IN}=24 V	$V_{OUT(min)}$=14.25 V	$V_{OUT(max)}$=16.75 V
Nominal output current	Min. frequency	Max. frequency
I_{OUT}=0.6 A	f_{min}=100 kHz	f_{min}=295 kHz

Normalized Design Parameters		
Min. output to input voltage ratio	Max. output to input voltage ratio	Min. switch on-time
γ_{min}=0.594	γ_{max}=0.698	$\tau_{ON(min)}$=2.132

Maximum frequency	Minimum frequency	Max. switch on-time	Nom. Output current to input voltage ratio
ϕ_{max}=0.147	ϕ_{min}=0.05	$\tau_{ON(max)}$=13.03	ψ_{nom}=1.79

Calculated Circuit Parameters		
Resonant inductor	Resonant capacitor	Max. switch on-time
L_R=25 μH	C_R=10 nF	$t_{ON(max)}$=6.5 μs

Considering that the control of the current through the LEDs of the proposed design is carried out by making the low-drop current regulator provide a 2 kHz current square wave with variable pulse width, the necessary value of the C_O capacitor can be estimated as indicated below. Assuming that the regulator's bandwidth is significantly lower than 2 kHz, so that the current supplied by the quasi-resonant buck converter to the combination formed by capacitor C_O, LDOCS and LED does not vary significantly during a 2 kHz cycle, the ripple of the V_{OUT} voltage will be mainly due to the fundamental component of the pulsating LED current, being maximum when its duty cycle is 50%. Under these conditions, to obtain a 5% peak-to-peak ripple when the output voltage is minimum (see Table I),

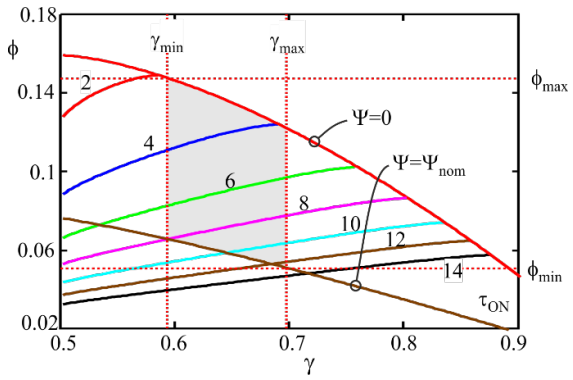

Fig. 10 Normalized frequency ϕ as a function of output-to-input voltage ratio γ for different τ_{ON} values.

the necessary capacitor would be 85 µF. For experimental validation, a value of 100 µF has been used, which provides a ripple of 0.6 volts peak to peak at 2 kHz on V_{OUT}. This ripple has an important effect on the power dissipation in the LDOCS. The greater the ripple, the greater the voltage margin that must be established to maintain a minimum voltage across the LDOCS and avoid distortion in the LED current.

IV. Simplified Small-Signal Dynamic Analysis

As it was previously mentioned, one of the main functions of the resonant converter is to minimize the voltage drop across the LDO regulator thus reducing the power handled by this dissipative stage without losing its current control capability. Therefore, the feedback loop must sense the LDO regulator voltage and control the switch on-time to minimize it.

To design the feedback control loop, the first step is modeling the dynamic behavior of the resonant converter. In the bibliography there can be found different techniques to model the dynamic behavior of resonant converters [23]. These techniques are normally intended to model the complex dynamic effects of the resonant energy transfer that take place during the different modes of operation of this family of converters. However, for the proposed converter, some approximations can be made that greatly simplify the obtention of the dynamic model without a significant loss of accuracy.

The assumption that will be used for simplification is that the dominant dynamics is provided by the output filter capacitor (C_O). In the case of the design used for the experimental verification in this work, the output capacitor is used to keep an approximately constant voltage with a low frequency pulsating current through the load. This pulsating current is due to the 2 kHz PWM control used for LED dimming. Therefore, the slow dynamics provided by the high capacitance required at the output filter makes the dynamic effect of the resonant energy transfer between C_R and L_R to be negligible in comparison. Therefore, the only element that will be considered for this simplified dynamic analysis is capacitor C_O.

The proposed procedure is based on replacing the small-signal static output impedance R_{eq} that can be obtained from the static model given by expression (13), by the parallel between capacitor C_O and resistance R_{eq}. The first step of this procedure is made by linearizing expression (13):

$$\hat{I}_{OUT} = \frac{\partial I_{OUT}}{\partial V_{IN}} \cdot \hat{v}_{IN} + \frac{\partial I_{OUT}}{\partial V_{OUT}} \cdot \hat{v}_{OUT} + \frac{\partial I_{OUT}}{\partial t_{ON}} \cdot \hat{t}_{ON}. \quad (20)$$

This equation can be rewritten as:

$$\hat{v}_{OUT} = \left(-\frac{\partial I_{OUT}}{\partial V_{OUT}}\right)^{-1} \cdot \left(-\hat{I}_{OUT} + \frac{\partial I_{OUT}}{\partial V_{IN}} \cdot \hat{v}_{IN} + \frac{\partial I_{OUT}}{\partial t_{ON}} \cdot \hat{t}_{ON}\right). \quad (21)$$

Where the static small signal output impedance R_{eq} is calculated as:

$$R_{eq} = \left(-\frac{\partial I_{OUT}}{\partial V_{OUT}}\right)^{-1}. \quad (22)$$

The equivalent circuit of expression (21) is shown in Fig. 11. Adding capacitor C_O allows obtaining an approximated model of the small signal dynamics of the resonant converter. The effect of this capacitor combined with the static model given by equation (21) provides the following single-pole small-signal transfer function:

$$\hat{v}_{OUT} = \left(\frac{R_{eq}}{1+R_{eq} \cdot C_O \cdot s}\right) \cdot \left(-\hat{I}_{OUT} + \frac{\partial I_{OUT}}{\partial V_{IN}} \cdot \hat{v}_{IN} + \frac{\partial I_{OUT}}{\partial t_{ON}} \cdot \hat{t}_{ON}\right). \quad (23)$$

Table II shows the small-signal parameters of the model given by (23) using the circuit parameters of the design example described in the previous section. These values were calculated at 100% and 5% of the nominal current for the maximum and minimum expected load voltages.

Table II also includes the transfer function of the controller used for experimental verification. For this design, the input voltage is assumed to be kept constant by a previous stage. The output current can also be assumed constant as it is regulated by the LDOCS placed in series with the LED lamp. This way, the simplified feedback loop of the system is shown in Fig. 12. The purpose of the feedback loop is to control the converter output voltage to minimize the voltage drop in the LDOCS.

Figs. 13 and 14 show the Bode plot of the system loop gain using the parameters of Table II.

V. Example of a Practical Implementation of the Proposed Circuit

The simplified schematics of the circuit used for experimental verification is shown in Fig. 15. The central component for the implementation of the ZC-t_{ON} control is a L6562A low-cost control integrated circuit. This IC is primarily intended to control power-factor-correction (PFC) converters working at critical conduction mode, but it can be adapted to

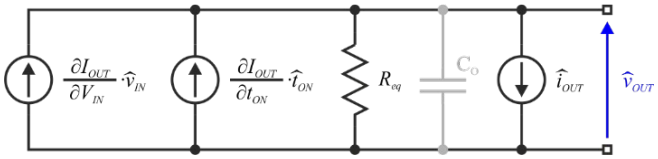

Fig. 11 Simplified small-signal dynamic equivalent for the resonant converter.

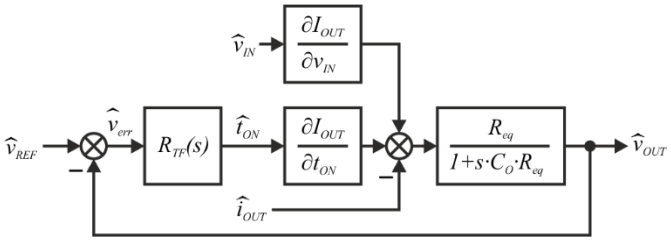

Fig. 12 Simplified feedback loop diagram.

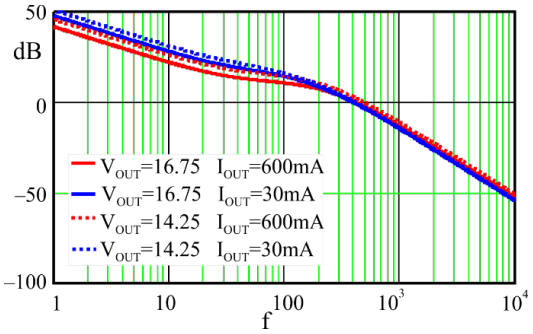

Fig. 13 Bode plot of the magnitude of the system loop gain.

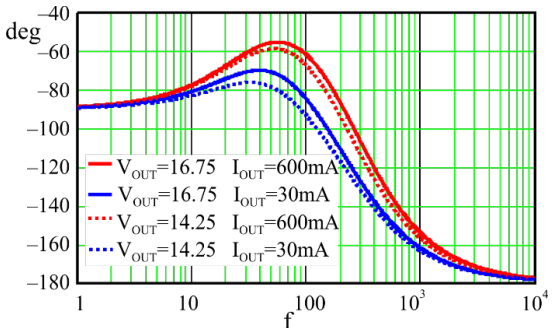

Fig. 14 Bode plot of the argument of the system loop gain.

control the proposed converter using a minimal number of external components. It has a zero-crossing detection input (ZCD) that triggers the gate signal of the MOSFET when its voltage goes below a certain threshold. This input is normally used to detect the complete demagnetization of the inductor in PFC converters, but in this circuit, it is used to detect the instant when capacitor C_R gets fully discharged. It also includes an internal multiplier and an operational amplifier to implement the regulator required for power factor correction. In this case, the regulator is implemented using an external low-cost operational amplifier. The L6562A also has some useful protections, such as the under-voltage lock-out or an automatic restart. This last feature introduces short low-frequency pulses to the MOSFET gate signal when no falling edge is detected on the ZCD pin thus allowing circuit start-up when voltage is initially applied to the converter input.

TABLE II
SMALL-SIGNAL CIRCUIT PARAMETERS

Small-Signal System Parameters				
	$V_{OUT(min)}$=14.25 V		$V_{OUT(max)}$=16.75 V	
	I_{OUT}=600mA	I_{OUT}=30mA	I_{OUT}=600mA	I_{OUT}=30mA
R_{eq}	8.5 Ω	22.1 Ω	6.6 Ω	16.3 Ω
$(2\pi C_O R_{eq})^{-1}$	187 Hz	72 Hz	239 Hz	98 Hz
$\partial I_{OUT}/\partial t_{ON}$	$19 \cdot 10^4$ A/s	$13 \cdot 10^4$ A/s	$14 \cdot 10^4$ A/s	$12 \cdot 10^4$ A/s
$\partial I_{OUT}/\partial V_{IN}$	95 mΩ^{-1}	28 mΩ^{-1}	130 mΩ^{-1}	44 mΩ^{-1}
Control Transfer Function				
$\frac{\hat{t}_{ON}}{\hat{v}_{err}}(s)$	$R_{TF}(s) = 8.04 \cdot 10^{-4} \cdot \frac{1 + \frac{s}{2\pi \cdot 32}}{s \cdot \left(1 + \frac{s}{2\pi \cdot 258}\right)}$			

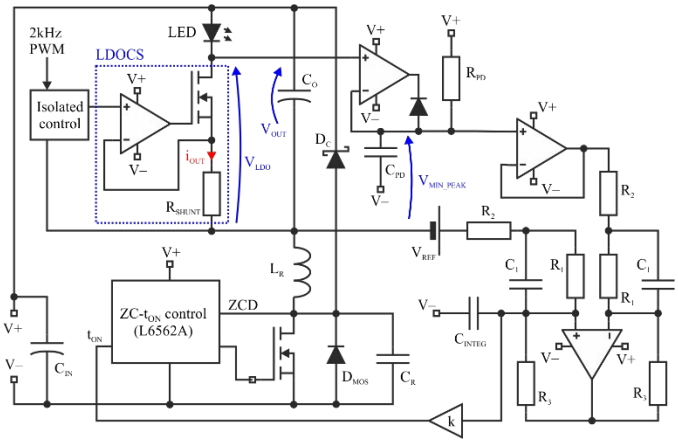

Fig. 15 Simplified schematics of the circuit used for experimental verification.

A low-cost quad general purpose operational amplifier is used for multiple functions: implementing the LDOCS control, the peak detector and the regulator described in the previous section. The operational amplifier inside the LDOCS is used to force that the shunt resistor (R_{SHUNT}) voltage follows the current reference provided by the isolated control (see Fig. 15). The isolated control receives a 2 kHz PWM signal from an external digital controller. When this reference is set to zero, the output of this operational amplifier saturates low, which reduces the width of the actual current pulse through the LED due to the delay introduced by the slew-rate at turn-on. At 2 kHz this effect is not critical and can easily be compensated with a small pulse-width increase at the digital reference.

The peak detector shown in Fig. 15 is used to track the minimum value on signal V_{LDO}. The basic waveforms of this subcircuit are shown in Fig. 16. The upper trace shows the LED current and the voltage across capacitor C_O (V_{OUT}). The LDOCS voltage (V_{LDO}) is equal to V_{OUT} minus the LED voltage. The minimum voltage in V_{LDO} is obtained at the falling edge of the LED current and it must be sufficiently close to zero as to minimize the power dissipated in the LDOCS without losing its current control capability.

Assuming that the LED voltage when the LDOCS is supplying its nominal current of 0.6A presents slow variations the following approach can be used for the small signal dynamic analysis:

$$\hat{v}_{OUT} \approx \hat{v}_{MIN\_PEAK}. \tag{24}$$

Therefore, the feedback is used to regulate the output of the V_{LDO} minimum peak detector (V_{MIN_PEAK}) instead of V_{OUT}. The integral effect of the proposed regulator makes the average value of V_{MIN_PEAK} equal to the internal reference V_{REF}. However, a peak detector is a highly non-linear circuit that modifies the transient response of the control loop. Assuming that the V_{OUT} ripple is small and that the LED voltage is approximately constant during the positive intervals of I_{OUT}, the peak detector output is similar to that of a zero-order-hold circuit with the V_{LDO} signal sampled at the falling edges of I_{OUT}.

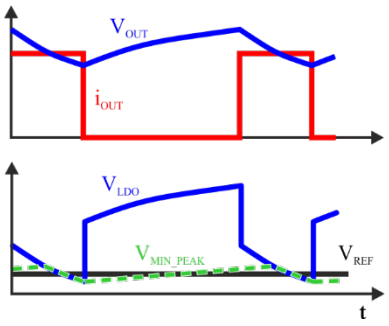

Fig. 16 Operation of the peak detector.

Therefore, the dynamic effect of the peak detector has a small effect on the phase margin obtained from Figs. 13 and 14 [24].

The transfer function of the regulator is provided by the operational amplifier shown in the lower right part of Fig. 15 combined with the gain block 'k'. This last block is given by the L6562A control IC:

$$\hat{t}_{ON} = \frac{-k}{s \cdot C_{INT} \cdot (R_1 + R_2)} \cdot \frac{1 + C_1 \cdot R_1 \cdot s}{1 + C_1 \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot s} \cdot \hat{v}_{OUT}. \quad (25)$$

The C_1, C_{INT}, R_1, R_2 and k values are calculated to match the transfer function shown on Table II. Capacitor C_{INT} in Fig. 15 has a double purpose, it provides the integral term of the regulator transfer function in (25) and allows to shift the floating reference of the LDOCS to adapt it to that of the ZC-t_{ON} control block, which avoids the use of rail-to-rail operational amplifiers.

As previously mentioned, the proposed circuit can be used to keep a constant current through the LEDs, compensating for the variations associated with the low-frequency ripple of the input voltage that could be due, for example, to the use of a power factor correction stage. With an appropriate regulator design, it is possible to eliminate most of this ripple at the quasi-resonant converter stage, and only a fraction of it at the LDOCS in a dissipative way. The part of the ripple that cannot be eliminated by the converter may force increasing the voltage supported by the LDOCS (V_{REF}) with the consequent decrease in efficiency. Using a 10% peak-to-peak input voltage ripple and a frequency of 100 Hz in the proposed design, the output voltage ripple V_{OUT} can be estimated using the following formula derived from the block diagram of the Fig.12:

$$\frac{\hat{v}_{OUT}}{\hat{v}_{IN}} = \frac{\frac{\partial I_{OUT}}{\partial V_{IN}} \cdot \frac{R_{eq}}{1 + s \cdot C_O \cdot R_{eq}}}{1 + R_{TF}(s) \cdot \frac{\partial I_{OUT}}{\partial t_{ON}} \cdot \frac{R_{eq}}{1 + s \cdot C_O \cdot R_{eq}}}. \quad (26)$$

In the proposed design, the maximum peak output voltage at 100 Hz is attenuated by a ratio of 5 with respect to the input, thus the maximum peak output voltage at this frequency is 0.24V.

VI. Experimental Results

To verify the proposed methodology, several simulations were carried out and a laboratory prototype was built and tested (see Fig. 17). The specifications used for these tests were based on the design example described in the previous sections. The simulations were carried out using the LTSpice XVII program and the files used have been included as complementary information for this work. The main objectives pursued with the simulations were: to verify the operating point and the main waveforms at various power levels, to check the accuracy of the approximations used to obtain the small-signal dynamic model of the quasi-resonant buck converter, and to verify that the non-linear effect introduced by the peak detector does not significantly affect the dynamic behavior of the circuit.

Fig. 18 shows the converter efficiency as a function of the duty cycle of the 2 kHz PWM control signal at two different V_{OUT} voltages with and without a 10% ripple at the input voltage. As it can be seen, a maximum efficiency of 91.6% is reached with a duty cycle of 100% and a V_{OUT} of 16.7 volts. As expected, lower values of V_{OUT} result in lower efficiency, due to the lower output power and the higher switching frequency of the resonant buck converter. For a V_{OUT} voltage of 14.3 volts, the efficiency drops to 89.5%. Although the value of V_{REF} used has not been modified, the input ripple slightly reduces the efficiency of the circuit. At nominal current the measured

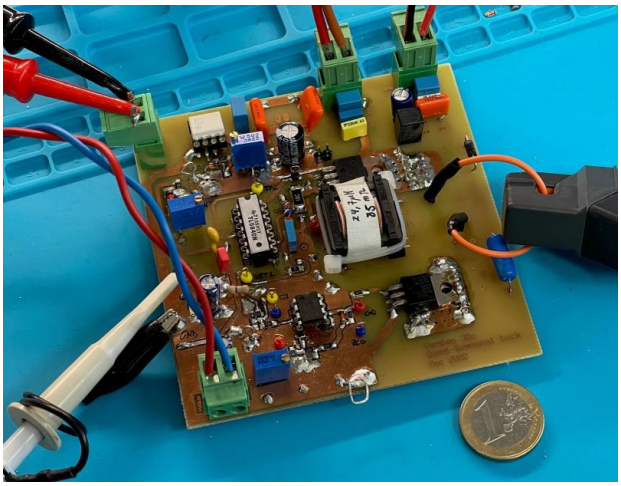

Fig. 17 Prototype used for experimental verification.

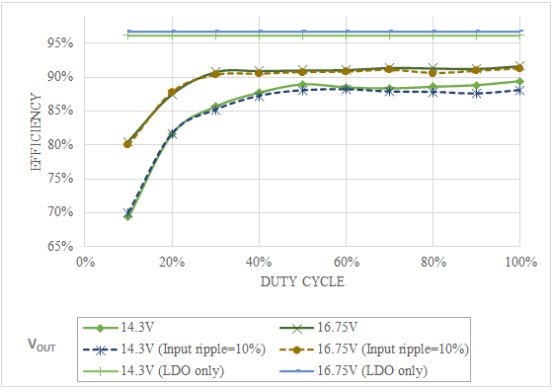

Fig. 18 Efficiency as a function of the PWM duty cycle at two different V_{OUT} values, with a peak-to-peak input voltage ripple of 10% (dashed lines) and without ripple (solid lines) compared to the maximum theoretical efficiency of the LDOCS.

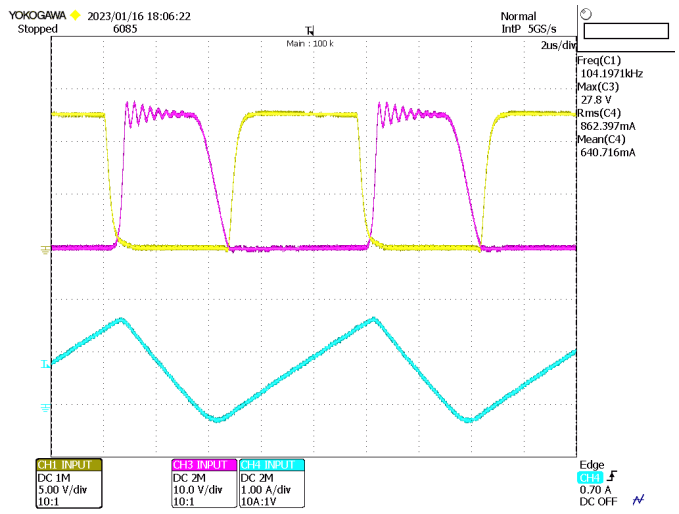

Fig. 19 MOSFET V_{GS} signal (CH1), MOSFET V_{DS} signal (CH3) and inductor current i_{LR}. (CH4) at nominal power.

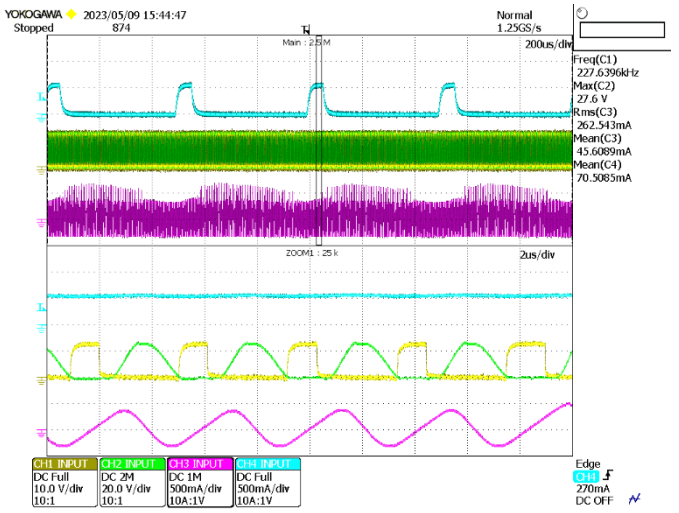

Fig. 20 MOSFET gate signal (CH1), MOSFET voltage (CH2), inductor current (CH3) and lamp current (CH4) at a dimming level of 10%.

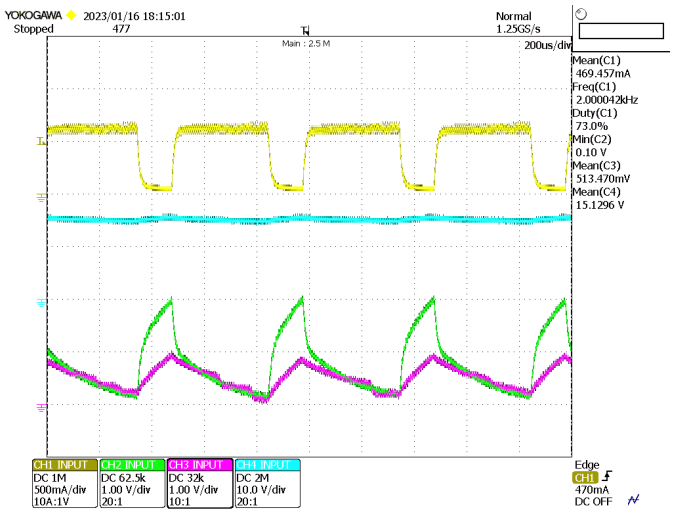

Fig. 21 Lamp current (CH1), LDOCS voltage (CH2), peak detector output (CH3) and V_{OUT} voltage (CH4) at 25% duty cycle.

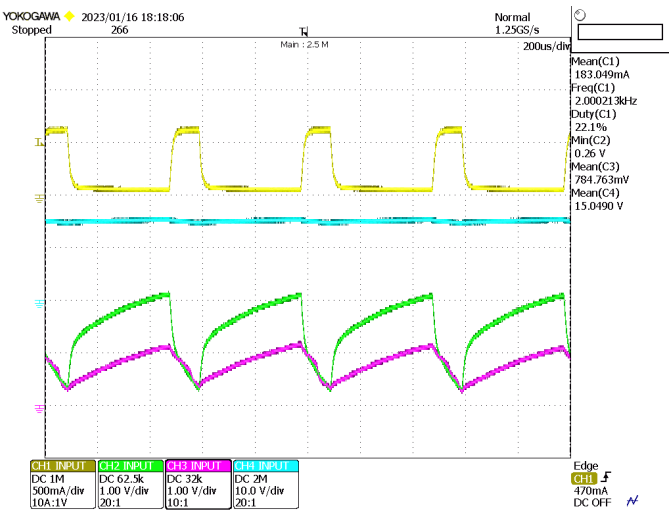

Fig. 22 Lamp current (CH1), LDOCS voltage (CH2), peak detector output (CH3) and V_{OUT} voltage (CH4) at 75% duty cycle

efficiency is 91.2% and 88.2% for the maximum and minimum output voltages respectively. The traces on the upper part correspond to the maximum theoretical efficiency that could be obtained considering only the effect of LDOCS.

Figs. 19 and 20 show the main waveforms of the quasi-resonant buck converter at nominal and 10% output current respectively, both for a V_{OUT} of 15V. As it can be seen, the resonant capacitor is fully discharged before the MOSFET is switched on thus providing zero voltage switching. The ringing in V_{DS} signal observed in Fig. 19 is mainly due to the resonance between the resonant capacitor and the stray inductance of the clamping diode D_C.

Figs. 21 and 22 show the lamp current, the LDOCS voltage, the peak detector output and V_{OUT} voltage at 75% and 25% duty cycle of the PWM control signal. As it can be seen, the LDOCS voltage present a much smaller variation compared to the idealized behavior shown in Fig. 16. This is due to the filter capacitor placed in parallel with the lamp, which prevents its voltage from falling to zero when the current is canceled.

Fig. 23 shows the effect of the 100 Hz input ripple in the V_{OUT} voltage and the lamp current with a 75% duty cycle. As can be seen, the current through the lamp is not affected and the output voltage presents a 100 Hz ripple that is significantly lower than that of the input, although the effects of low frequency ripple are combined with those associated with the 2 kHz PWM dimming signal.

VII. Conclusions

In this paper, a new low-cost LED driver based on a quasi-resonant buck converter in series with a low-voltage-drop current regulator was presented. The proposed quasi-resonant converter was obtained by adding a resonant capacitor in parallel with the MOSFET of a standard buck converter. The

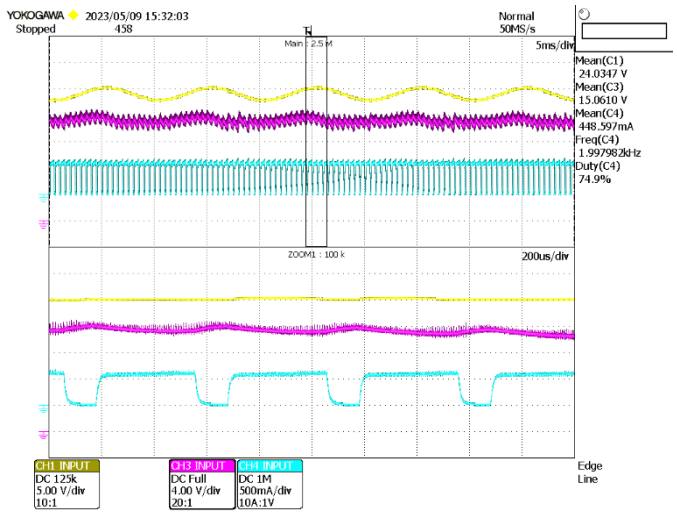

Fig. 23 Input voltage (CH1), output voltage V_{OUT} (CH3) and lamp current (CH4) for an input peak-to-peak voltage ripple of 10%.

charging and discharging of this capacitor are done by the resonant transfer of energy with the inductance of the buck converter. In this way, soft switching is obtained at the cost of increasing the inductor current ripple with respect to that of a standard buck converter operating in discontinuous conduction mode. The control of this quasi-resonant converter was implemented using a L6562A, which is a low-cost integrated circuit that was designed to control single-switch boundary-mode power factor correction stages. This integrated circuit was used to implement what was called: ZC-t_{ON} control. In this control, the MOSFET is switched on after the zero crossing of its drain-source voltage and its on-time is used as the control parameter of the feedback loop.

A low-drop current regulator was used to control the LED lamp current and provide PWM dimming at 2 kHz. This PWM frequency was used to comply with the light flicker recommendations of IEEE PAR1789. The combination of the quasi-resonant converter with the low-dropout linear regulator allows to reduce the 2 kHz current component that passes through the inductance of the circuit, strongly reducing the audible noise produced by magnetostriction that is typical in many circuits working in burst mode.

The operation of the resonant converter was analyzed using an energy-balance approach to model the circuit behavior during the resonant transitions. This procedure avoids using the fundamental approach and its subsequent accuracy loss.

A straightforward procedure to obtain a simplified small-signal dynamic model of the quasi-resonant converter was also described in the paper.

Based on these approaches, a simplified design procedure was proposed and applied to a design example. This example was simulated using LTSpice XVII software and implemented in a laboratory prototype. The simulation files are provided as complementary material of present work. Both simulation and experimental verification were in good agreement with the values calculated using the proposed analysis procedure.

A maximum efficiency of 91.6% was obtained in the laboratory prototype working at nominal current and the maximum LED design voltage of 16.25V. The L6562A control integrated circuit was able to maintain ZVS switching throughout the entire dimming range.

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