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Capacitance Analysis for Volume Reduction Based on Integrated Buck and Buck-Boost LED Driver

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***Abstract*—This paper presents a design methodology to improve the power density of integrated converters operating at universal input voltage fulfilling the standards of connection to the grid and load. The proposed integrated two-stage converter is composed of the power factor correction (PFC) stage behaving as a current source to the bus, and the power control (PC) stage which provides continuous energy to the LED load. Traditionally, the low-frequency ripple (LFR) filtering process is performed by the bus capacitor placed in the output of the PFC stage, while the PC stage output capacitor works only as a high-frequency (HF) filter. The idea is to explore the lower and fixed operating voltage characteristics of the PC stage to share the LFR filtering with the PFC stage. Thus, a mathematical analysis is carried out, considering the influence of the LED characteristics, bus voltage, and capacitances to predict the LFR in the LED current. A case study, composed of an integrated buck and buck-boost converter to supply a 75W LED load, is presented. For the traditional design method, the LED driver needs an 820uF/160V PFC bus capacitor and a 10uF/80V output capacitor to filter the HF components, representing a total capacitors' volume of 17.9cm³. With the proposed analysis, the optimized driver circuit requires a 220uF/160V PFC bus capacitor and a 470uF/80V output capacitor, resulting in a total capacitors' volume of 9.7cm³, providing a volume reduction of approximately 45%.**

***Index Terms*— Capacitance Reduction, Integrated Converters, LED Drivers, Light-Emitting Diodes, Low-Frequency Ripple.**

I. INTRODUCTION

ONE of the strongest feature of power light-emitting diodes (LEDs) is their ability to continuously produce light output for many years of use, in contrast to most conventional light sources, forcing users to go through repeated and frequent failure-and-replacement cycles [1]. The selection of LEDs and appropriate drivers is a highly complex goal, depending on power level, efficiency, and cost factors. Also, the LED performance is mainly ruled by the reliability of the driver circuits interfacing with the utility grid that has an intermittent nature, mainly in terms of voltage stability [2].

Since LED drivers are generally supplied from an AC source, the electronic circuit should be properly designed to drive the LEDs and to fulfill all the required standards and recommendations, which is particularly complex in converters operating at universal input voltage. From the grid connection side, the IEC 61000-3-2 Class C [3] establishes the limits for the input current harmonic content. Besides, the power factor (PF) must be higher than 0.9, as specified by the U.S. Energy Star program [4]. From the LED connection, it is desired to fulfill the recommended practices given by IEEE Std. 1789-2015, to mitigate the effects of light flicker in high-brightness LEDs [5].

Numerous types of electronic circuits have been proposed in the literature. The simplest driver structure is based on a single-stage topology [6]. In this solution, accurate output control and good power quality are achieved. Besides, the bulk capacitor voltage is applied directly to the LED, leading to a low component count. However, this feature makes it difficult to fulfill the standards and operate with universal input voltage simultaneously [7], [8]. To overcome this drawback, a two-stage structure presents the ability to ensure the energy quality drive from the grid through a power factor correction (PFC) stage and a power control stage (PC) connected in cascade to provide the desired DC voltage and current to the load. However, this structure has two switches and gate drivers, leading to a bigger size and higher cost [9].

A solution to overcome the mentioned issues is the integrated power converters (IPC), where both topologies share a single controlled switch, which usually provides lower switching losses [10]. To ensure the energy quality, the PFC stage must be operated in discontinuous conduction mode (DCM), behaving as a resistance to the grid, thus no PFC control strategy is required. The control loop of the IPC aims to regulate the LED current and must have a slow response to not affect the input and output variables, therefore representing an extremely simple control [11].

Due to the input PFC stage and the DC behavior of the LEDs, the input power is certainly presented in the pulsating form at twice the line frequency. Thus, the bulky capacitor is mandatory to smooth the low-frequency ripple (LFR) and balance the instantaneous difference between input and output power, to keep the output power constant [12]. However, the filtering process leads to large bus capacitors, mainly when operated under universal input voltage. Also, the inductors in both stages occupy a large portion of the board, hence most of the converter volume is due to passive elements.

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To overcome this drawback, wide-bandgap semiconductors, such as gallium nitride, have emerged as promising devices as they offer lower losses under high frequency, significantly reducing the volume of the magnetic elements [13]. However, the capacitors that filter the LFR at 120Hz do not benefit from the increase in the switching frequency. Therefore, capacitance reduction has become a hot research topic in the literature, mainly proposing alternative control strategies [14]–[19] or with alternative topologies [20]–[24]. The drawback is the use of two or more active switches. Also, a solution using integrated parallel stages, with the PC stage working as a ripple reduction stage is proposed, presenting a good performance to low-power converters [10].

Regarding the IPC flicker-free solutions found in the literature, the following works can be highlighted: [25] presented a buck-flyback integrated, operating in voltages from 184-276 V_{rms}. In [26] an integrated boost-forward is proposed, operating in voltages from 90-135 V_{rms}. [27] shows a sepic-flyback with 220 V_{rms} operating voltage. [28] presents an integrated sepic and class E, operating in 127V_{rms}. All these solutions use the output capacitor only as a high-frequency (HF) filter and in a narrow input voltage range.

Against this background, the contribution of this paper is to perform a comprehensive analysis regarding the volume and capacitances in IPCs, when operated under a universal input voltage range. The main idea is to use the PC stage output capacitor not only as an HF filter but also as a low-frequency (LF) filter, since it operates at lower and fixed voltages when compared to the wide voltage range of the bus capacitor, helping to fulfill the flicker recommendation.

In the case study, a buck DCM converter performs the PFC at the limit of the bus voltage values and a buck-boost DCM converter performs the PC delivered to the LEDs. The integrated buck and buck-boost converter (IBBBC) is projected to supply a 75W LED load, using a commercial bus capacitor. To find the most suitable solution, 4 LED loads with different forward voltages and currents are compared, and the influence of LED parameters in the LFR transmission is analyzed.

The paper is organized as follows. In section II the operating principle of the converter is presented. Section III presents the analytical results. Section IV presents the experimental results. Finally, Section V presents the main conclusions of this work.

II. ANALYSIS OF THE PROPOSED LED DRIVER

One of the characteristics of integrated converters is the operation with a fixed duty cycle and frequency, representing the loss of one degree of freedom in the project. Considering that, the response of the converter to variation in the duty cycle can be neglected, since the control loop of IPCs has a slow response, conventionally one decade below the grid frequency [9]. Also, the modeling is evaluated considering independent stages connected in cascade, thus, the PFC stage behaves as a current source and the PC stage performs the second stage as a resistance.

The proposed analysis aims to define the relationship between the bus and LED currents, to verify the ability of the PC stage to filter the LFR to different combinations of bus and output capacitances. The buck-boost converter is used as the PC stage since it is the solution that most decrease naturally the LFR [29]. Also, as the converter is designed to operate in a universal input voltage range, it is desired to fulfill all the required standards while presenting a low bus voltage mainly when the converter operates in high input voltages to avoid unnecessary bulky capacitors, and the buck converter is a solution that fits all these requirements. The IBBBC is shown in Fig. 1 and the detailed derivation is presented in [30].

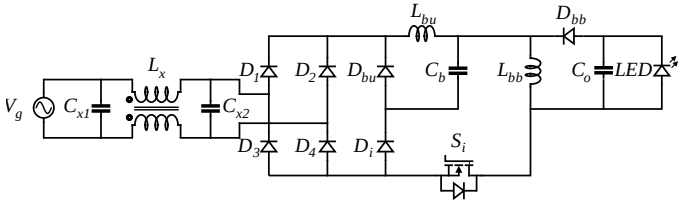

Fig. 1. Integrated buck and buck-boost converter.

A. Design Guidelines

According to the input current, two PFC stages can be listed: The ideal PFC stage and the quasi-PFC stage [31], [32]. The buck converter is a quasi-PFC stage and presents a non-sinusoidal input current. Its electrical characteristic is of equivalent resistance in series with a voltage source that represents the bus voltage, V_b. The average input current over a switching period ($I_g(t)$) is calculated as the following:

$$i_g(t) = \frac{\left(V_g \sin \omega_L t - V_b\right) D^2 T_S}{2L_{bu}} \qquad (1)$$

where V_g is the grid peak voltage, ω_L is the angular frequency of the main, D is the switch duty cycle, T_s is the switching period, and L_{bu} is the inductance of the PFC stage. Thus, the average input power over a switching period ($p_g(t)$) is given by:

$$p_g(t) = \frac{V_g \sin \omega_L t \left(V_g \sin \omega_L t - V_b\right) D^2 T_S}{2L_{bu}} \qquad (2)$$

As the converter under study presents the relation $V_b = V_g \sin \Theta$, where $\Theta = asin(V_b/V_g)$ is the conduction angle caused by the characteristics of buck PFC converter. After processing (2), the input power can be expressed as follows:

$$p_g(t) = \frac{{V_g}^2 D^2 T_S}{2L_{bu}} (1 - \cos 2\omega_L t - 2 \sin \theta \sin \omega_L t) \qquad (3)$$

Assuming lossless operation, the output current delivered by the PFC stage to the bus capacitor and PC stage is calculated dividing (3) by V_b, producing:

$$i_b(t) = \frac{{V_g}^2 D^2 T_S}{2V_b L_{bu}} (1 - \cos 2\omega_L t - 2 \sin \theta \sin \omega_L t) \qquad (4)$$

By integrating (3) over half a line period, the average input power (P_g) is found, given by:

$$P_g = \frac{{V_g}^2}{2}\frac{D^2 T_S}{2L_{bu}}\left(1 - \frac{2\theta}{\pi} - \frac{sin\,2\theta}{\pi}\right) \quad (5)$$

Thus, using the expression from (5), the DC component of the bus current (I_b) can be found by (6):

$$I_b = \frac{P_g}{V_b} = \frac{{V_g}^2}{2V_b}\frac{D^2 T_S}{2L_{bu}}\left(1 - \frac{2\theta}{\pi} - \frac{sin(2\theta)}{\pi}\right) \quad (6)$$

Different from the ideal PFC stage, in the buck PFC converter the input current is only sinusoidal within a certain interval of the line period [33]. Therefore, the DC component and the AC component present different magnitudes, and the topology is called a quasi-PFC converter. Thus, the AC component is calculated as the following:

$$\hat{I}_b = \int_o^{\pi} i_b(t) - I_b\, d\theta \quad (7)$$

Considering (4) and (6), and Θ relation previously defined, the AC component is given by:

$$\hat{I}_b = \frac{{V_g}^2}{V_b}\frac{D^2 T_S}{2L_{bu}} \cdot \left[2\theta + \int_{\theta}^{\pi-\theta} \frac{1 - cos\,2\omega_L t - 2\,sin\,\theta\,sin\,\omega_L t}{1 - \frac{2\theta}{\pi} - \frac{sin\,2\theta}{\pi}} d\theta\right] \quad (8)$$

Regarding the critical duty cycle of buck PFC and buck-boost PC stages, both are calculated through the DC transfer function, yielding:

$$D_{bu} = \frac{V_b}{V_g} \quad (9)$$

$$D_{bb} = \frac{V_o}{V_o + V_b} \quad (10)$$

On the other hand, the constant defined as the resistance of the PC stage converter (R_{PC}) is given by:

$$R_{PC} = \frac{2L_{bb}}{D^2 T_S} \quad (11)$$

By replacing R_{PC} with the equivalent expression ${V_b}^2/P_b$ and isolating the variable of (11), the buck-boost inductance (L_{bb}) is found as:

$$L_{bb} = \frac{{V_b}^2}{P_b}\frac{D^2 T_S}{2} \quad (12)$$

Thus, to calculate the buck inductor, first, the general expression of V_b which relates the PFC and PC stages is found by multiplying (6) and (11), yielding:

$$V_b = \frac{{V_g}^2}{2V_b}\frac{D^2 T_S}{2L_{bu}}\left(1 - \frac{2\theta}{\pi} - \frac{sen(2\theta)}{\pi}\right)\frac{2L_{bb}}{D^2 T_S} \quad (13)$$

Therefore, simplifying the previous equation and isolating L_{bu}, the general equation to calculate the inductance of the PFC stage is shown in (14).

$$L_{bu} = \frac{{V_g}^2 L_{bb}}{2{V_b}^2}\left(1 - \frac{2\theta}{\pi} - \frac{\mathrm{sen}(2\theta)}{\pi}\right) \quad (14)$$

B. Buck-boost Dynamic Model

To perform the proposed analysis of obtaining the LED current ripple characteristic in terms of the bus capacitor, C_b, and the output capacitor, C_o, it is necessary to obtain the dynamic model of the PC converter. The first step is to define the DCM averaged switch model of the PC stage, replacing the switches by equivalent sources to find a linear circuit. These sources represent the average values by switching periods of current and voltage in the components, thus, the harmonic content resulting from the switching of the converters is neglected.

Thus, the average model of the buck-boost converter is defined as shown in Fig. 2, where the switch is modeled as an effective resistor, and the diode is substituted by a dependent power source, with power equal to the power dissipated in R_{PC} [34]. The terminals I_1, V_1, I_2, and V_2, are the voltages and currents of the controlled switch and diode, respectively, V_γ and R_γ are the threshold voltage and the equivalent resistance of the LED load, V_o and I_o are the LED output voltage and current, respectively. Fig. 3 presents the switch as well as the diode currents and voltages at a high-frequency period.

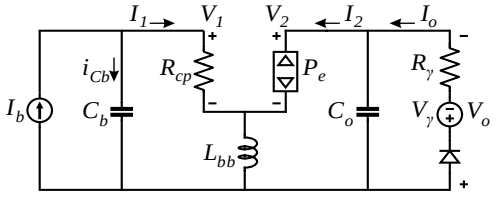

Fig. 2. Average buck-boost PC stage circuit.

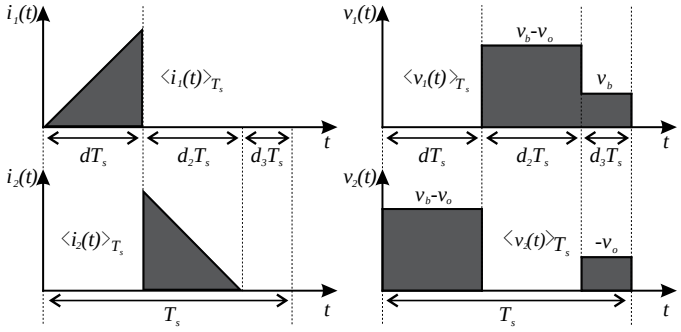

Fig. 3. High-frequency waveforms of buck-boost PC stage.

However, this is a non-linear model, because of the multiplication of time-varying parameters. Therefore, it is necessary to perform a small signal analysis of the buck-boost PC circuit, as presented in Fig. 4. To obtain the AC model parameters of the converter, it is necessary to fix an operation point of the equivalent average model (V_1, V_2, D), disturb around this point, and then linearize it.

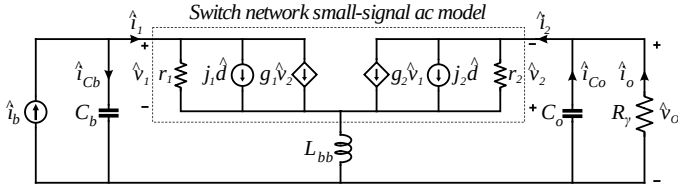

Fig. 4. Buck-boost PC ac model.

Concerning the average values, the voltage in terminal 1 is equal to the bus voltage, and in terminal 2 equal to the LED voltage, thus, the operation point is (V_b, V_o, D). Regarding the average terminal currents, the resultant in terminal 1 and terminal 2 is given by the relation of the constant R_{PC} by the voltage, as follows:

$$\langle i_1(t)\rangle_{Ts} = \frac{\langle v_b(t)\rangle_{Ts}}{R_{PC}(d)} = f_1(v_b, v_o, d) \tag{15}$$

$$\langle i_2(t)\rangle_{Ts} = \frac{\langle v_b(t)\rangle_{Ts}{}^2}{\langle v_o(t)\rangle_{Ts} R_{PC}(d)} = f_2(v_b, v_o, d) \tag{16}$$

Using Taylor's Series, the current in terminal 1 is given by:

$$I_1 + \hat{\imath}_1(t) = \frac{V_b}{R_{PC}(D)} + \frac{1}{r_1}\hat{v}_b(t) + g_1\hat{v}_o(t) + j_1\hat{d}(t) \tag{17}$$

Therefore, the AC coefficients are as the following:

$$\frac{1}{r_1} = \left.\frac{\partial f_1(V_b, V_o, D)}{\partial V_b}\right|_{v_b=V_b} = \frac{1}{R_{PC}(D)} \tag{18}$$

$$g_1 = \left.\frac{\partial f_1(V_b, V_o, D)}{\partial V_2}\right|_{v_o=V_o} = 0 \tag{19}$$

$$j_1 = \left.\frac{\partial f_1(V_b, V_o, D)}{\partial D}\right|_{d=D} = \frac{2V_b}{DR_{PC}(D)} \tag{20}$$

Likewise, for terminal 2, the current is found as:

$$I_2 + \hat{\imath}_2(t) = \frac{V_b{}^2}{V_o R_{PC}(D)} + \frac{1}{r_2}\hat{v}_o(t) + g_2\hat{v}_b(t) + j_2\hat{d}(t) \tag{21}$$

And the AC coefficients are as the following:

$$\frac{1}{r_2} = -\left.\frac{\partial f_2(V_b, V_o, D)}{\partial V_o}\right|_{v_o=V_o} = \frac{1}{M^2 R_{PC}(D)} \tag{22}$$

$$g_2 = \left.\frac{\partial f_2(V_b, V_o, D)}{\partial V_b}\right|_{v_b=V_b} = \frac{2}{MR_{PC}(D)} \tag{23}$$

$$j_2 = \left.\frac{\partial f_2(V_b, V_o, D)}{\partial D}\right|_{d=D} = \frac{2V_b}{MDR_{PC}(D)} \tag{24}$$

where $M=V_o/V_b$ is the voltage gain. Based on the circuit of Fig. 4, to find the transfer function between the output load current and the input bus current, first, the bus current is found by applying Kirchhoff's current law (KCL), as the following:

$$\hat{\imath}_b(t) = \hat{\imath}_1(t) + \hat{\imath}_{Cb}(t) \tag{25}$$

$$\hat{\imath}_b(t) = \frac{1}{r_1}\hat{v}_b(t) + g_1\hat{v}_o(t) + j_1\hat{d}(t) + C_b\frac{d\hat{v}_1(t)}{dt} \tag{26}$$

Considering no perturbation in d and knowing that $g_1=0$, the equation is rewritten as:

$$\hat{\imath}_b(t) = \frac{1}{R_{PC}}\hat{v}_b(t) + C_b\frac{d\hat{v}_b(t)}{dt} \tag{27}$$

And the Laplace transform is given as:

$$\hat{\imath}_b(s) = \frac{1}{R_{PC}}\hat{v}_b(s) + sC_b\hat{v}_b(s) \tag{28}$$

$$\hat{\imath}_b(s) = \hat{v}_b(s)\overbrace{\left[\frac{1}{R_{PC}} + sC_b\right]}^{A} \tag{29}$$

Similar to the previous, the KCL in the output node is:

$$i_2(t) = i_{Co}(t) + i_O(t) \tag{30}$$

$$\frac{1}{r_2}\hat{v}_o(t) + g_2\hat{v}_b(t) + j_2\hat{d}(t) = C_o\frac{d\hat{v}_o(t)}{dt} + \frac{\hat{v}_o(t)}{R_\gamma} \tag{31}$$

Considering no perturbation in d and substituting the coefficients, the result is:

$$-\frac{R_\gamma}{M^2R_{PC}}i_O(t) + \frac{2}{MR_{PC}}\hat{v}_b(t) = C_o\frac{d\hat{v}_o(t)}{dt} + i_O(t) \tag{32}$$

Which Laplace transform is given by:

$$\hat{\imath}_O(s)\overbrace{\left[sC_oR_\gamma + \overbrace{\frac{R_\gamma}{M^2R_{PC}}}^{B} + 1\right]}^{C} = \hat{v}_b(s)\frac{2}{MR_{PC}} \tag{33}$$

Finally, by dividing (33) by (29), the transfer function that relates the output load current to the input bus current is

presented in (34). This equation allows obtaining the LED current ripple as a function of C_b and C_o, which gives the possibility of finding the best design in terms of capacitance volume.

$$G(s) = \frac{\hat{\imath}_O(s)}{\hat{\imath}_b(s)} = \frac{C}{A\,B} = \frac{2MR_{PC}}{s^2E + sF + G} \quad (34)$$

$$E = 2M^2R_{PC}^2R_\gamma C_bC_o \quad (35)$$

$$F = 2M^2R_{PC}R_\gamma C_o + R_{PC}R_\gamma C_b + M^2R_{PC}^2C_b \quad (36)$$

$$G = M^2R_{PC} + R_\gamma \quad (37)$$

III. ANALYTICAL RESULTS OF THE PROPOSED CONVERTER

Using the previous equations and the circuit illustrated in Fig. 1 of the IBBBC, the converter will be designed to operate0020at a universal input voltage ($90V_{rms}$-$240V_{rms}$) and line frequency of 60 Hz. Also, the switching frequency is 60 kHz. Both buck and buck-boost inductances ensure the full DCM operation. Using the equations from the former sections and considering $s=j\omega$ where $\omega=2\pi120Hz$:

$$G(j\omega) = \frac{2MR_{PC}}{j\omega^2E + \omega F + G} \quad (38)$$

The amplitude of the output CA component is obtained by the product of the input CA component and the module of (38), producing:

$$\hat{I}_O = |G(j\omega)|\,\hat{I}_b = \sqrt{Re[G(j2\pi120)]^2 + Im[G(j2\pi120)]^2}\,\hat{I}_b \quad (39)$$

Finally, using the previously-defined equations and knowing that the current ripple is double the modulating amplitude, the equation that describe the output current ripple is given by the division of the peak-to-peak current ripple and average value, leading to the following expression:

$$\hat{I}_o\% = \frac{\hat{I}_O}{I_O} = \frac{\hat{I}_b}{I_O}\left|\frac{2MR_{PC}}{(j2\pi120)^2E + (j2\pi120)F + G}\right| \quad (40)$$

A. Definition of the LED Loads

4 LED models are analyzed to compose an LED luminaire of 75 W, resulting in different LED characteristics. The idea is to verify the LFR response of the PC stage to the LED parameters and find the LED model that reduces the required capacitances. Thus, Table I presents the parameters of the single LEDs, and Table II the final LED loads.

TABLE I
LED MODELS PARAMETERS (1 SINGLE LED)

LEDs Parameters	Rated Current	Forward Voltage	Series resistance
CREE CMA 2550	2.13 A	31.5 V	1.75 Ω
CREE CMT 2870	1.46 A	47.5 V	2.67 Ω
LUMILEDS 1208	1.08 A	29.35 V	5 Ω
LUMILEDS CSP HL1	0.40 A	2.7V	0.33 Ω

TABLE II
LED LUMINAIRES PARAMETERS

LED Lamp	Output Current	Threshold voltage	Series resistance	Output Voltage
CREE CMA 2550 (1 LED)	2.13 A	31.5 V	1.75 Ω	35.2 V
CREE CMT 2870 (1 LED)	1.46A	47.5 V	2.67 Ω	51.4 V
LUMILEDS 1208 (2 LED)	1.08 A	58.7 V	10 Ω	69.5 V
LUMILEDS CSP HL1 (2 STRINGS/33 LEDs)	0.8 A	89.1V	5.5 Ω	93.5 V

B. Considerations Regarding the Flicker Limits

The IEEE 1789-2015 presents the modulation limits of the luminous intensity of LEDs. Following the limits, the LED drivers certainly have a low level of human perception of the light flicker, and the biological effects are minimized.

To have a low level of light flicker and follow the recommendations, the peak-to-peak LED current ripple must be lower than 19.2% [5], [35]. Also, when the converter is projected to follow the recommended practices, the critical point is at the perfect ac power line conditions in low-rated input voltage, i.e., $110V_{rms}$ [5], considered in this work.

C. Definition of Maximum Bus Voltage

The buck PFC has the input characteristic of equivalent resistance in series with a voltage source. Thus, the operating point must be carefully selected so that high harmonic content can be avoided, thus improving the converter's volume utilization [36]. [37] define the input current conduction angle to be higher than 129.1º, to assure that all current harmonics attend to the requirements of the IEC 61000-3-2 standard. This definition is also given by the relation $V_s=V_b/V_{g\_rms}$, representing a V_s of 0.608.

However, [38] presented the influence of the bus voltage LFR in these results. As the ripple increases, the harmonic content of the input current also increases. Thus, considering $\hat{V}_b\%$ of 40%, the maximum V_s decreases to 0.587, leading to a maximum V_b of 64.57V when operated in $110V_{rms}$.

D. LFR Filtering only with the Bus Capacitor

Typically integrated LED drivers are projected with the output capacitor as an HF filter and the bus capacitor as an LF filter. Based on this, [35] presents the analysis of the LFR transmission for the PC stage buck-boost converter, defining the maximum bus voltage ripple ($\hat{V}_{b\_max}\%$) to attend the IEEE

1789-2015. Considering the analysis, the $\hat{V}_{b\_max}$% to the LEDs shown in Table II is from 10.05% to 11.1%.

The converter must have a bulky capacitance when operating at $110V_{rms}$ and withstand the highest bus voltage when operating at $240V_{rms}$. With higher bus voltage, the conduction angle of the converter becomes smaller, leading to high harmonic content and low PF. On the other hand, a lower bus voltage results in higher RMS and peak inductor currents, making the volume reduction of capacitors negligible due to the lower operating voltage concerning the increase in the volume of the inductors due to higher currents.

As the main idea of this paper is the volume improvement of storage capacitances, the operating point of V_b selected is 61V to the rated input voltage of $110V_{rms}$ and the duty-cycle of the converter is 0.29, leading to a V_s relation of 0.554, which fulfills all the grid connection standards with a safe margin. As V_s is fixed, when the converter operates with a maximum input voltage of $240V_{rms}$, the average bus voltage will be 133V. Thus, using the previously defined $\hat{V}_{b\_max}$% from 10.05% up to 11.1%, the minimum calculated bus capacitors are from 801µF to 725µF. Therefore, the commercial capacitor to fit all the LED luminaires is 820µF/160V. To filter the HF components, an output capacitor of 10µF is sufficient.

E. LFR Filtering with Bus and Output Capacitors

Using the defined bus voltage and solving (40) to each LED load, the analysis of the LFR transmission is presented, considering that the PC stage output capacitor is used also as an LFR filter. The idea is to transfer the LF filtering process as much as possible to the output, which presents lower and fixed voltages, leading to a volume reduction. Also, when the converter operates under a universal input voltage range, the bus capacitance must withstand a rated voltage of 160V, leading to very bulky capacitances.

Thus, to demonstrate the analysis, three cases of commercial capacitors are used in the bus of the PFC stage while the output capacitor is used as a variable that varies between 0 and 1000 µF. The results are presented in Fig. 5, where the green line represents the limit of the recommended standards. In addition, some values are taken from Fig.5 to Table III, which presents the summary of capacitors of the IBBBC considering the possible options to attend the IEEE Std. 1789-2015 standard, with the minimum values of rated voltage indicated for each load.

In the case of an 820µF/160V bus capacitor, representing 9.5% of bus voltage ripple, only an HF output filter capacitor of 10µF/100V fulfills the recommended practices for the 4 LED loads. As shown in Table III, the total capacitors´ volume is 17.9cm³.

In the case where the bus capacitance is reduced to 470µF/160V, the voltage ripple increases to 16%. At this condition, only an HF output filter capacitor is not enough to have safe modulation levels. The increase in output capacitance decreases the LFR of the LEDs, mainly in the LED loads with higher equivalent series resistance. Both LED Lumileds 1208 and Lumileds HL1, with series resistance higher than 5 Ω, present better results compared to cases CREE 2550 and CREE 2870, with series resistances below 3 Ω. The LED Lumileds 1208 follows the recommended practices with an output capacitor of 220µF/80V, resulting in a total capacitance volume of 11.4 cm³. On the other hand, the load composed of the Lumileds HL1 needs an output capacitor of 330µF/100V, leading to a total volume of 13.5 cm³.

As in the previous case the Lumileds 1208 load presented a good result with a relatively small output capacitor; the bus capacitor is reduced to 220µF/160V, representing a bus voltage ripple of 30%. Using an output capacitor of 470µF/80V, the Lumileds 1208 presents a substantial volume reduction, leading to a total capacitance volume of 9.7cm³, representing approximately 45% volume reduction compared to the case with an 820µF/160V bus capacitor and only an HF output filter capacitor of 10µF.

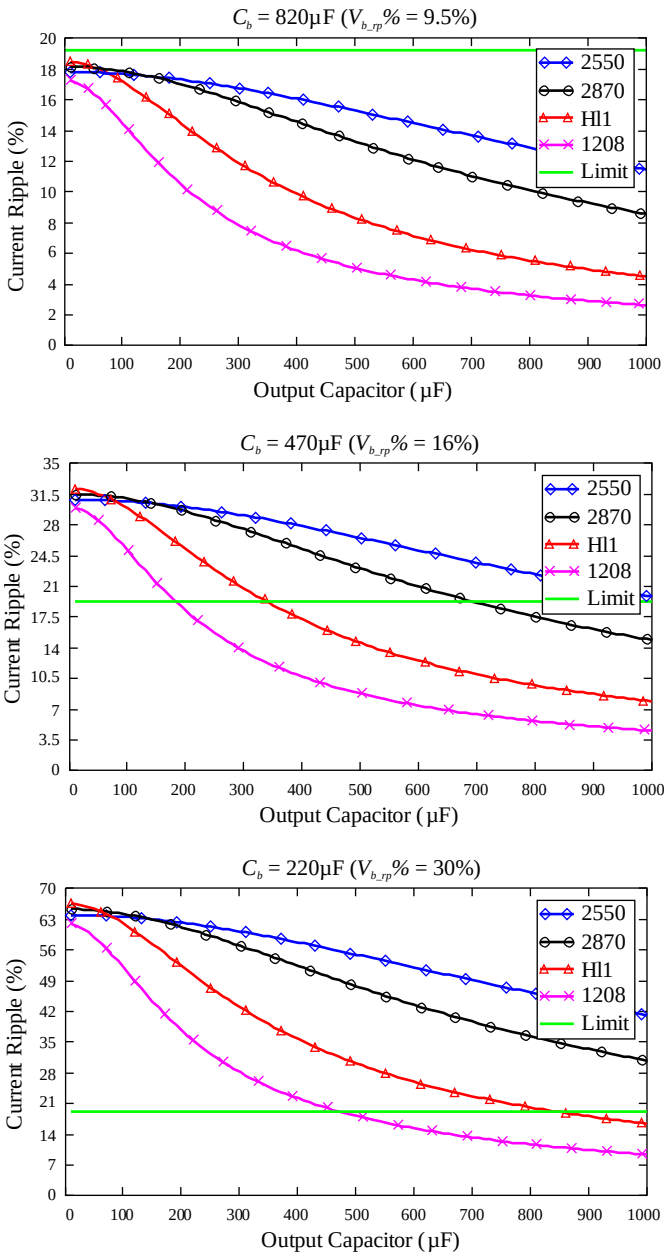

Fig. 5. Current ripple considering C_b of 820µF, 470µF, and 220µF.

TABLE III
CAPACITORS SUMMARY

160V	2550 (50V)		2870 (63V)		HL1 (100V)		1208 (80V)	
C_b (µF)	C_o (µF)	Vol. cm³	C_o (µF)	Vol. cm³	C_o (µF)	Vol. cm³	C_o (µF)	Vol. cm³
820	10	17.9	10	17.9	10	17.9	10	17.9
680	330	16.3	330	16.7	180	17.2	33	15.3
560	680	14.5	560	14.5	330	15.4	150	12.7
470	1000	13.7	680	13.1	470	13.5	220	11.4
330	1800	15	1200	14.2	560	14.2	330	10.3
220	-	-	-	-	820	15.1	470	9.7
100	-	-	-	-	-	-	1000	10

F. Inductors Volume

The inductors of the IBBBC are designed using (8) and (11). As can be seen through the design equations, the LED parameters do not influence the inductors´ values. Also, the 4 LEDs presented equal cores to PFC and PC stages. Therefore, there is no advantage in the inductors' volume changing the LED model and operating point.

The PFC inductor, L_{bb}, inductance is 36µH implemented in an EFD 30x15x9 core. The PC stage inductor, L_{bu} is 52µH implemented in an EFD 30x15x9 core.

IV. EXPERIMENTAL VERIFICATION OF THE IBBBC

To verify the theoretical analysis, a 75W laboratory prototype with Lumileds 1208 load was built. The complete components list is presented in Table IV.

TABLE IV
COMPONENTS LIST

Component	Symbol	Value
Input filter inductor	L_x	TDK B82732F2701B001
Input filter capacitor	C_{x1} C_{x2}	2x220nF film cap.
Buck inductor	L_{bu}	TDK EFD 30x15x9, 52µH, N=37, 55xAWG 34, l_g=0.79mm
Buck-boost inductor	L_{bb}	TDK EFD 30x15x9, 31.5 µH, N=21, 35xAWG 34, l_g=0.61mm
Switch	S_i	Fairchild FCP11N60
Bridge diodes	D_1 D_2 D_3 D_4	GBU806
Buck and int. diodes	D_{bu} D_{int}	STTH1R06
Buck-boost diode	D_{bb}	MUR 460
Bulk capacitor	C_b	220µF/160V electrolytic cap.
Output capacitor	C_o	470 µF/80V electrolytic cap.

The results were acquired with a Keysight DSOX4024A oscilloscope and the efficiencies were measured with a Yokogawa WT1800 power analyzer. Fig. 6 shows the comparison between the laboratory prototype, in (a) and (c), and the version with the output capacitor only as an HF filter, with an 820µF/160V bus capacitor in (b).

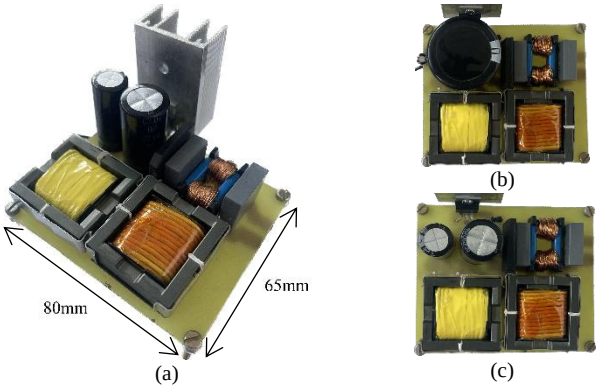

Fig. 6. (a) Proposed IBBBC, (b) Conventional C_b, and (c) Reduced C_b.

The input and output waveforms of the converter at full load operating in $90V_{rms}$ and $240V_{rms}$ are shown in Fig. 7 and Fig. 8, respectively, demonstrating that the proposed IBBBC works in universal input voltage.

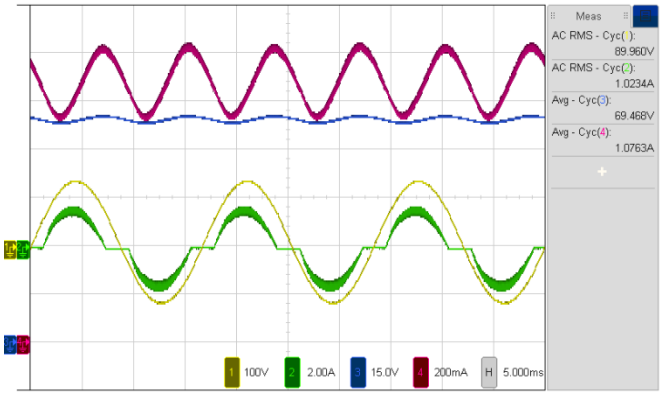

Fig. 7. IBBBC at $90V_{rms}$. AC main voltage (CH1), AC main current (CH2), LED voltage (CH3), and LED current (CH4).

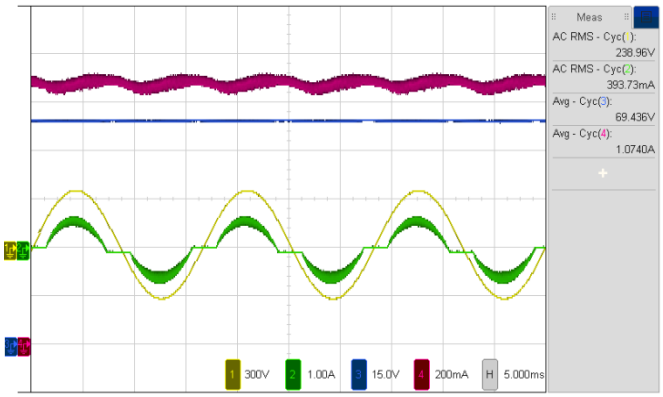

Fig. 8. IBBBC at $240V_{rms}$. AC main voltage (CH1), AC main current (CH2), LED voltage (CH3), and LED current (CH4).

Regarding the ripple transmission, the bus voltage and the LED current were tested at an input voltage equal to $110V_{rms}$. As shown in Fig. 9, the bus voltage ripple is equal to 18.6V, which is equivalent to 30.3%. On the other hand, the LED current ripple is equal to 194.3mA, which is equivalent to 18.1%, attending the IEEE 1789-2015 recommendation.

Likewise, Fig. 10 shows the results at an input voltage equal to 220V_{rms}. The bus voltage ripple is equal to 7.8V, representing 6.5% of the ripple over the average value. Regarding the LED current ripple, the value is 40mA, which is equivalent to 3.7%.

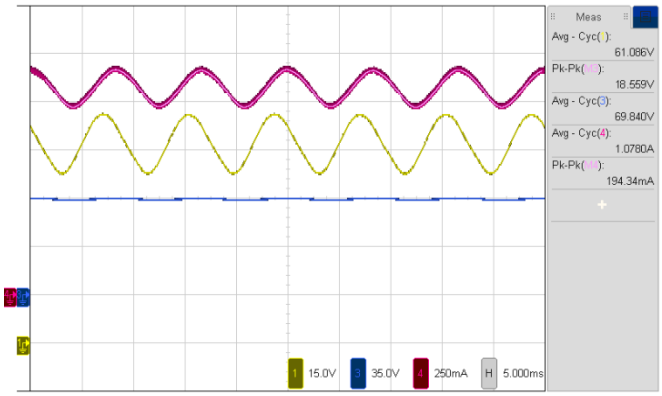

Fig. 9. IBBBC at 110V_{rms} input voltage, bus voltage (CH1), output voltage (CH3), and LED current (CH4).

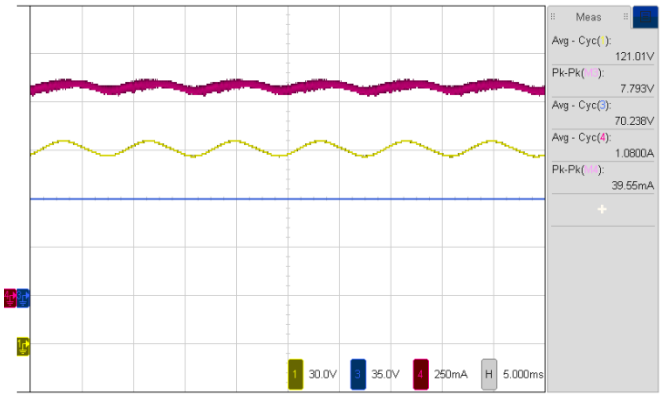

Fig. 10. IBBBC at 220V_{rms} Input voltage, bus voltage (CH1), output voltage (CH3), and LED current (CH4).

Analyzing the input waveforms at full load, the PF is equal to 0.95 and THD is equal to 25.8%. Also, to dimming conditions, the result is kept, since the buck converter conduction angles do not change. The breakdown of the harmonic content, illustrated in Fig. 11, shows that the converter meets the IEC 61000-3-2 Class C limit.

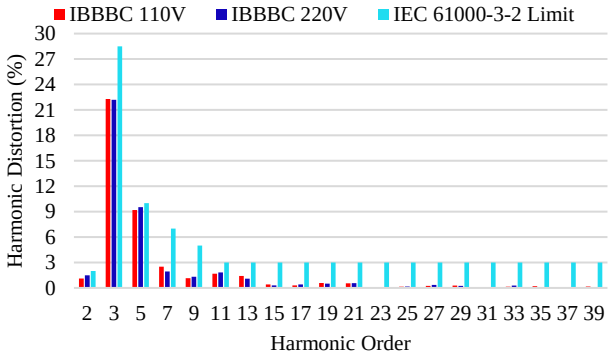

Fig. 11. Input current harmonic at 110V_{rms} and 220V_{rms}.

The performance of the driver has also been tested in the universal input voltage range. Fig. 12 shows the measured efficiency and LED current ripple versus the input voltage, with efficiency peak values above 88%. The increase in the input voltage decreases the efficiency but also decreases the LED current ripple.

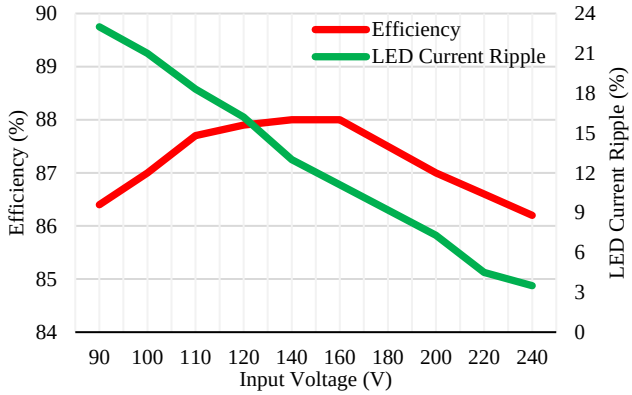

Fig. 12. Efficiency and LED current ripple related to the input voltage at full load.

Finally, Fig. 13 presents the efficiency result versus the percent output power, obtained experimentally. Concerning efficiency, it varies between 87.7% and 88.8% in 110V_{rms}.

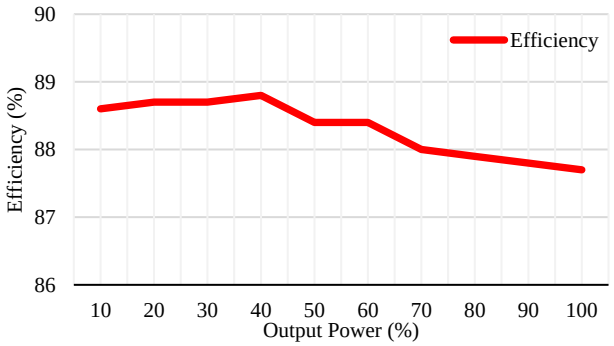

Fig. 13. Efficiency related to the output power to 110V_{rms}.

V. CONCLUSIONS

In integrated converters, the loss of independence between stages makes it impractical to adopt active control techniques for eliminating the low-frequency ripple in the output current without distorting the input variables and causing degradation in the quality of the energy drawn from the utility grid. Additionally, when integrated converters operate with a universal input voltage, the bus capacitor must be oversized, since the capacitance should be designed for the minimum input voltage and its rated voltage for the maximum input voltage. This results in the need for a very bulky capacitor.

This paper presented a new approach regarding the integrated LED driver analysis, considering the output capacitor working also as an LF filter. The dynamic model of the proposed circuit and its counterpart were evaluated, validated, and used to determine the optimum operating point, where the LFR filtering process has transferred the maximum

as possible to the output capacitor, which works with fixed and lower voltage, providing both high-quality input energy and low levels of low-frequency ripple in the LED current, while decreasing the driver volume.

The work was performed using 4 different LED devices, considering the LED electrical characteristics on the LFR transmission. First, the bus capacitance is defined in the case where the output capacitor works only as a HF filter. In this case, a minimum bus capacitor of 820µF/160V is required to fulfill the IEEE 1789-2015 recommendation for the 4 LED models, and the capacitance volume in the circuit is equal to 17.9cm³. Thereafter, filtering the LFR with both capacitors, the biggest volume reduction is reached when the load is composed of 2 Lumileds 1208 in series. In this optimized case the bus capacitance is reduced to 220µF/160V and the output capacitor is increased to 470µF/80V, reducing the volume of the total capacitance to 9.7cm³, representing a volume reduction of approximately 45% using the proposed methodology.

Thus, the IBBBC topology is used to drive an LED load of 75W. Experimental results with universal input voltages from 90Vrms to 240Vrms were presented, with PF of 0.95 and fulfilling IEC 61000-3-2 Class C limits. To full load operation, the circuit efficiency is from 86% to above 88%. Also, the LED current ripple is equal to 18.1% working with an input voltage of 110Vrms and 3.7% when operated with 220Vrms.

Compared with the conventional integrated LED drivers, the proposed technique offers the usage of approximately half of the capacitance volume, while keeping the same operating conditions of conventional converters. Therefore, the proposed technique offers high power density and price reduction through the optimization of energy storage. Also, other semiconductor technologies can be explored in future work, such as SiC switches and other diode technologies, aiming to improve system operation and increase overall efficiency.

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