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Reducing Low-Frequency Ripple Using Alternative Output Capacitor Connection on Integrated Converters for LED Drivers

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***Abstract*—Although advantageous in several aspects, the integration of converters leads to a loss of independence between the converter's stages, since both stages are controlled by the same active switch. This condition makes it impractical to adopt control techniques that act on the duty-cycle to mitigate the low-frequency ripple at the output current without distorting the line current. The low-frequency ripple transferred from the bus voltage to the LED current has been studied for integrated converters operated at constant duty-cycle. To comply with IEEE 1789-2015 recommendation, the integrated converters use large capacitors to mitigate the low-frequency ripple. Converters operating in discontinuous conduction mode (DCM) have been widely adopted because they transfer less ripple to the output than converters operating in continuous conduction mode (CCM). A novel circuit arrangement for the buck-boost power control (PC) stage integrated with a buck-boost power factor correction (PFC) stage is explored in this paper as a technique to minimize the low-frequency output ripple for converters operating at constant duty-cycle and CCM. The proposed circuit provides current feedback to the bus capacitor, acting to reduce the output current and bus voltage low-frequency ripple. A dynamic model for the proposed converter in CCM is obtained and used to determine the output current modulation as a function of converter parameters. It is shown that the proposed topology leads to a smaller low-frequency ripple than a conventional counterpart at the same operating point. A 95 W design example and a prototype supplying an LED load of 98.8 V / 960 mA for the proposed circuit and the conventional counterpart are presented. The experimental results show that the proposed arrangement can achieve similar results to the conventional circuit in efficiency, THD, or semiconductor stress, while the obtained output current modulation equals to 8.66 % is 3.5 times lower than that in the conventional circuit at same operating point and component values.**

***Index Terms*—Integrated converters, Light-emitting diodes, ripple reduction, capacitor reduction, flicker.**

I. Introduction

LEDs have been replacing conventional light sources for more than a decade. Features like long life span, smaller size, fast response, efficacy and color rendering make them the first choice for a wide range of applications [1], [2]. To better take advantage of the good features of LEDs and to provide a constant light output, it is important to properly design the power supply circuit. Therefore, the thermal, electrical, and optical characteristics of the lighting system should be considered together [3].

Single-stage drivers operate simultaneously as a power factor correction (PFC) stage and a constant output current source, known as Power Control (PC) stage. Buck, buck-boost, and flyback are the most commonly used topologies because they feature good output current regulation while achieving acceptable power quality, e.g., meeting IEC 61000-3-2 class C at low-cost [2], [4], [5]. To ensure a high power factor and design simplicity, any of these converters generally operate in discontinuous conduction mode (DCM), or in critical conduction mode (CrCM) [6]. The single-stage driver configuration is usually adopted in low and medium power ($<$50 W) applications [4]. One of the significant drawbacks of this type of arrangement is the large ripple of the output current [7], [8]. The attempt to reduce such ripple, and to reach flicker levels compatible with IEEE 1789-2015, without compromising the power factor and harmonic distortion of the input current, high-capacitance output electrolytic capacitors are required [7], [9], which besides being undesirable in terms of cost and useful life, also impair the dynamic behavior of the converter.

As a way to maintain the commitment of the low harmonic content of the input current associated with high power factor, as well as to achieve low ripple in the output current with smaller capacitances and faster dynamics, two-stage drivers have become the most used solution for medium and high power applications ($>$50 W) [10], [11]. Two-stage drivers are composed of a PFC stage and a PC stage [12]. The independence of each stage make it possible to apply control

techniques acting on the second stage duty-cycle to mitigate the low-frequency ripple. However, although two-stage converters have a significantly better operation, they are also more expensive.

A consolidated solution to overcome the disadvantages mentioned above is converter integration. The integration consists of a two-stage system with only one controlled switch, which means lower switching losses with a less expensive circuit. In this way, it is possible to leverage the advantages of two-stage operation while retaining some benefits of single-stage converters [13]–[15].

Although advantageous in several aspects, the integration of converters leads to a loss of independence between the stages, since only one controlled switch is used to operate both stages. This aspect makes it unfeasible to adopt control techniques that act directly on the duty cycle, aiming to eliminate the low-frequency ripple in the output current without simultaneously distorting the input current and, consequently, degrading the harmonic content and power factor of the driver. Usually, high-capacitance output electrolytic capacitors are required to smooth the pulsating power absorbed from the main and transferred to the output.

When operating under a constant duty-cycle, the PC stage transfers the low-frequency ripple from the bus voltage to the LED current. The amount of transferred ripple depends on the topology type and operation mode [16], [17]. In [18]–[21], the DCM was determined as the operation mode that transfers the minimum low-frequency ripple to the output, and no publications using the PC stage operating in CCM were issued since then. In [16], the low-frequency ripple transfer ratio (LFRTR) from the bus to the LED current is analyzed for the three main non-isolated DC-DC converters, buck, boost, and buck-boost operating in DCM.

The proposed work presents the potential of a novel architecture in the literature. The output capacitor (C_o) of the buck-boost converter in a PC stage is connected in feedback to the bus capacitor to mitigate the output current low-frequency ripple in converters operating under constant duty-cycle conditions and CCM. A previous version of this paper was presented in [22], where the initial idea was evaluated through simulation results. In the present work, the study was extended and experimental verification of a numerical example is used to validate the theoretical analysis. The following sections of the paper demonstrate that the proposed arrangement can reduce the LFRTR and put converters operating in CCM back to the alternatives for integrated converters.

Section II presents the configuration of the proposed topology. In Section III, the mathematical dynamic model is obtained. Section IV details a comparative study between the proposed topology and the conventional counterpart circuit. In Section V, a numerical design is performed. The proposed idea is validated through an experimental circuit in section VI. Finally, section VII provides a conclusion about the contribution of this work.

II. Proposed Topology

The proposed topology can be understood through the circuit in Fig. 1a, where the two-stage, non-integrated converter, composed of a buck-boost PFC and a boost PC is presented. The PC stage operates in CCM with the same gate signal as the PFC stage. Note that the load is not connected to the PC stage, as a conventional configuration, but between the positive terminal of the output capacitor and the positive terminal of the bus capacitor. The idea is that the voltage applied to the load, which is composed of the difference between the bus voltage and the output voltage of the PC stage, has a lower low-frequency ripple than in a conventional converter, where the load is placed in parallel to the output capacitor. Fig. 2 shows the voltage waveforms with low-frequency ripple at the two capacitors and the resulting load voltage.

Another way to visualize the proposed circuit is through Fig. 1b. This figure shows the PC stage composed of a buck-boost converter with alternative capacitor connection. The output capacitor's alternative connection provides a feedback way from the output to the bus capacitor and this is the objective of the study presented in this paper. The circuit shown in Fig. 1a and 1b has no connection modification between the components. The nodes have been colored in both circuits to highlight the equivalence between the electrical schematics. The circuit in Fig.1c is identical to the proposed circuit except for the way the output capacitor is connected. This circuit will be used for comparison purposes throughout this paper.

For any of the circuits in Fig. 1:

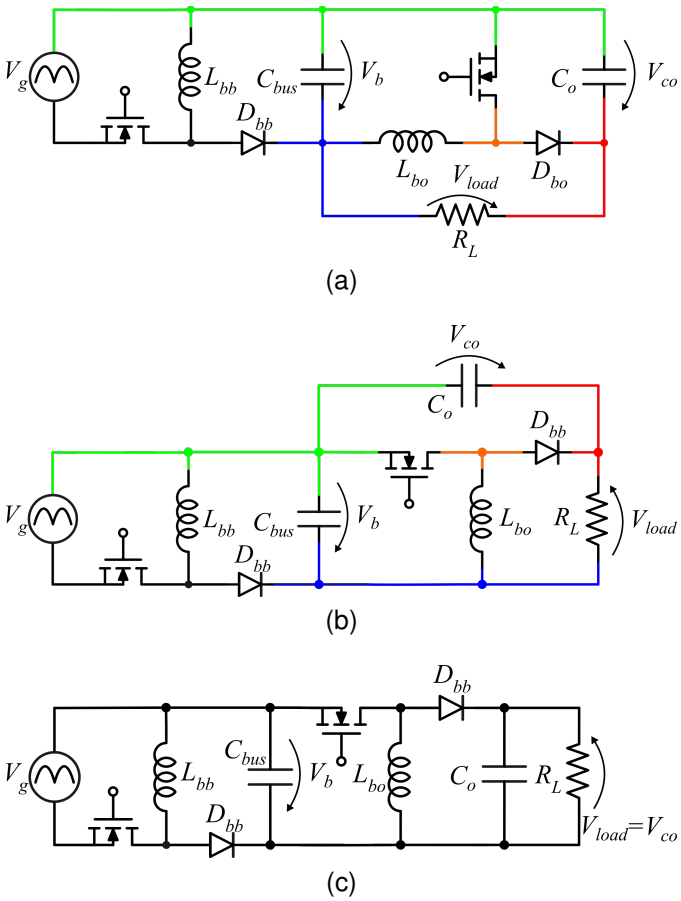


Fig. 1. Equivalent circuits. (a) Alternative load connection. (b) Alternative capacitor connection. (c) Conventional circuit.

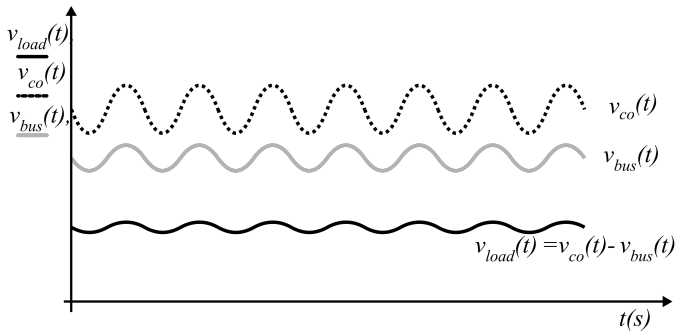


Fig. 2. Voltage waveforms for capacitors and load under proposed topology.

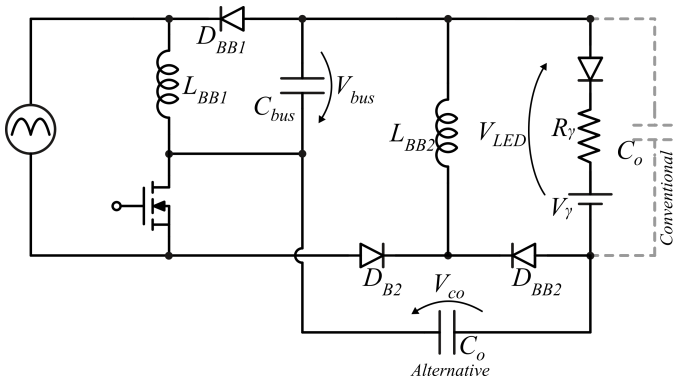


Fig. 3. Proposed Topology - Integrated buck-boost PFC and buck-boost PC with alternative output capacitor connection.

$$V_{load} + V_b - V_{co} = 0 \tag{1}$$

Considering the PC stage operating in CCM, it is found from the circuit illustrated in Fig. 1a, that the relationship between the output voltage V_{co} and V_b is defined by the boost converter static gain:

$$V_{co} = \frac{1}{1-D} \cdot V_b \tag{2}$$

Substituting (1) into (2), and taking into account the polarity adopted for V_{load}, we have,

$$\frac{V_{load}}{V_b} = M = \frac{D}{1-D} \tag{3}$$

It can be inferred from (3) that the relationship between the load voltage and bus voltage, despite the load or capacitor in alternate connection, is the same as that of a conventional buck-boost converter.

Using the integration techniques proposed in [23], a two-stage integrated converter, as shown in Fig. 3, can be obtained from the circuit depicted in Fig. 1b. An additional diode D_{B2} is appended, and the load is represented by the LED model, which consists of the characteristic resistance R_γ and the threshold voltage V_γ.

The following sections will examine the transference of a low-frequency ripple from the bus voltage to the LED current when a buck-boost converter with the alternative capacitor connection is used as a PC stage of the integrated converter in Fig. 3.

III. Dynamic Model

This section presents the dynamic model for the proposed circuit. Regarding the PFC stage influence on the system dynamics, the pole associated with the first stage inductor is located at high frequencies and has minimal or no effect on the low-frequency response. Therefore, the PFC inductor is neglected and only the bus capacitor is analyzed together with the second stage inductor and capacitor.

The PFC converter behaves as a resistor seen by the main, denominated as R_{pfc}. The instantaneous power drawn from the grid can be expressed as follows [24]:

$$p_g(t) = \frac{V_g^2 sin^2 \omega_L t}{R_{pfc}} = \frac{V_g^2}{2R_{pfc}} \cdot (1 - \cos 2\omega_L t) \tag{4}$$

Where ω_L represents the angular frequency of the main. Assuming lossless operation, the output current delivered by the PFC stage to the bus capacitor and PC stage can be calculated as follows:

$$i_{g\_bus}(t) = \frac{p_g(t)}{V_b} = \frac{V_g^2}{2V_b R_{pfc}} \cdot (1 - cos 2\omega_L t) \tag{5}$$

It can be seen in (5) that the output current of the PFC stage has a DC component and an AC component, both with the same magnitude:

$$I_{g\_bus} = \hat{I}_{g\_bus} = \frac{V_g^2}{2V_b R_{pfc}} \tag{6}$$

According to [24], in typical applications, virtually the entire AC component of PFC output current circulates through the bus capacitor reactance, generating an AC voltage ripple at the bus capacitor, that is finally transferred to the load through the second stage. However, this is not valid for the proposed circuit with the alternative capacitor connection. In this case, the DC component of the bus current is transferred to the load through the buck-boost static gain, while the AC component transference will be analyzed using a transfer function.

Fig. 4 shows the proposed buck-boost converter with an alternative capacitor fed by a current source that represents the output of the PFC stage. The nonlinear devices array is highlighted and interpreted as a two-port network with polarities defined in the figure by v_1, i_1, v_2, and i_2.

In CCM, the average currents are described as follows:

$$\langle i_1(t) \rangle_{Ts} = d \cdot \langle i_L(t) \rangle_{Ts} \tag{7}$$

$$\langle i_2(t) \rangle_{Ts} = d' \cdot \langle i_L(t) \rangle_{Ts} \tag{8}$$

Where, d is the duty-cycle of the controlled switch, and $d' = 1 - d$. Ts represents the switching period.

Considering the volt-second balance for the inductor, its average voltage in steady state is zero. Therefore, the average voltage values at the two ports are:

$$\langle v_1(t) \rangle_{Ts} = d' \cdot \langle v_{co}(t) \rangle_{Ts} \tag{9}$$

$$\langle v_2(t) \rangle_{Ts} = d \cdot \langle v_{co}(t) \rangle_{Ts} \tag{10}$$

The relationship for the two ports' current and voltages are:

$$\langle i_1(t) \rangle_{Ts} = \frac{d}{d'} \cdot \langle i_2(t) \rangle_{Ts} \tag{11}$$

$$\langle v_1(t)\rangle_{Ts} = \frac{d'}{d}\cdot\langle v_2(t)\rangle_{Ts} \tag{12}$$

It can be seen from (11) and (12) that, in CCM, the average voltage and current values for the nonlinear cell formed by the switch and diode have the behavior of an ideal transformer. Thus, the nonlinear components (switch and diode) can be replaced by an ideal transformer with a suitable transformer ratio, as illustrated in Fig. 5.

Applying Kirchoff's voltage law (KVL) to the closed path that encompasses the bus capacitor, the two ports of the ideal transformer, and the LED load, we have:

$$\begin{aligned} -v_b(t) + \langle v_1(t)\rangle_{Ts} + \langle v_2(t)\rangle_{Ts} - V_\gamma - v_{R\gamma}(t) = 0 \\ v_b(t) = \frac{d'}{d}\langle v_2(t)\rangle_{Ts} + \langle v_2(t)\rangle_{Ts} - v_{LED}(t) \\ \langle v_2(t)\rangle_{Ts} = (v_b(t) + v_{LED}(t))\cdot d \end{aligned} \tag{13}$$

Similarly:

$$\begin{aligned} v_b(t) = \langle v_1(t)\rangle_{Ts} + \frac{d}{d'}\cdot\langle v_1(t)\rangle_{Ts} - v_{LED}(t) \\ \langle v_1(t)\rangle_{Ts} = (v_b(t) + v_{LED}(t))\cdot d' \end{aligned} \tag{14}$$

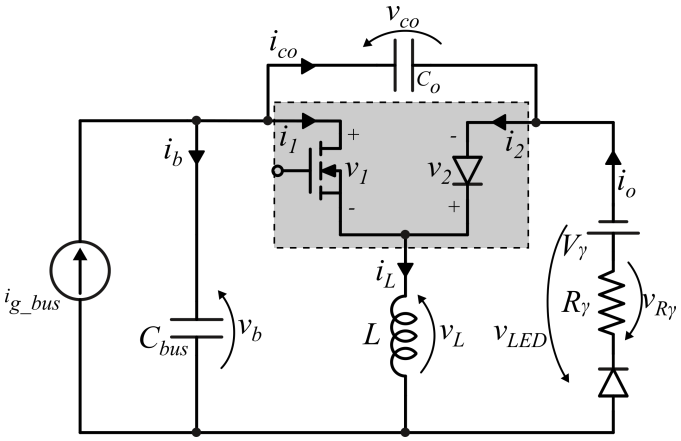


Fig. 4. Buck-boost with alternative capacitor connection with highlighted nonlinear devices array.

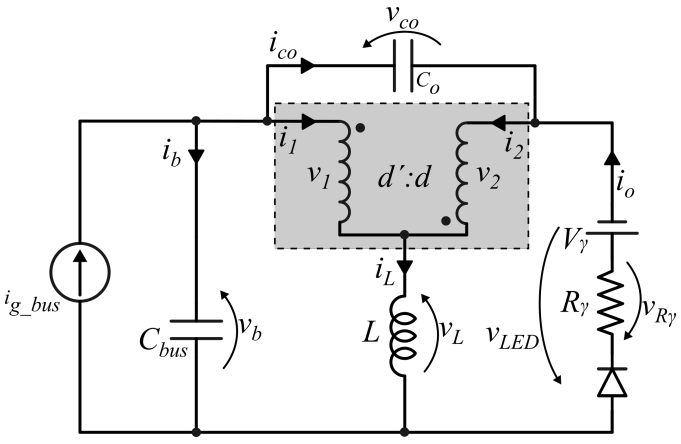


Fig. 5. Buck-boost with alternative capacitor connection and nonlinear devices array replaced by equivalent ideal transformer.

The dynamic equation for the inductor is given by:

$$L\cdot\frac{di_L(t)}{dt} = v_L(t) = \langle v_2(t)\rangle_{Ts} - v_{LED}(t) \tag{15}$$

To obtain a dynamic equation as a function of state variables and input signals, we can manipulate (15) and (10) to obtain:

$$L\cdot\frac{di_L(t)}{dt} = v_L(t) = d\cdot v_b(t) - v_{LED}(t) \tag{16}$$

that is equivalent to:

$$L\cdot\frac{di_L(t)}{dt} = v_b(t) - d'v_{co}(t) \tag{17}$$

For the capacitors currents we have:

$$\begin{aligned} i_b(t) = \langle i_2(t)\rangle_{Ts} - i_o(t) \\ C_o\cdot\frac{dv_{co}(t)}{dt} = d'\cdot i_L(t) - \frac{v_{co}(t)}{R_\gamma} + \frac{v_b(t)}{R_\gamma} + \frac{V_\gamma}{R_\gamma} \end{aligned} \tag{18}$$

And for the alternatively connected capacitor:

$$\begin{aligned} i_b(t) = i_{g\_bus}(t) - \langle i_1(t)\rangle_{Ts} - i_{co}(t) \\ C_{bus}\cdot\frac{dv_b(t)}{dt} = i_{g\_bus}(t) - i_L(t) + \frac{v_{co}(t)}{R_\gamma} - \\ - \frac{v_b(t)}{R_\gamma} - \frac{V_\gamma}{R_\gamma} \end{aligned} \tag{19}$$

Thus, (17), (18), and (19) make up the equation system that represents the dynamic behavior of the circuit. The model is presented in matrix form as follows:

$$\begin{aligned} \overbrace{\begin{bmatrix} L & 0 & 0 \\ 0 & C_o & 0 \\ 0 & 0 & C_{bus} \end{bmatrix}}^{K}\cdot\begin{bmatrix} \dot{i_L}(t) \\ v_{co}(t) \\ v_b(t) \end{bmatrix} = \\ = \overbrace{\begin{bmatrix} 0 & -d' & 1 \\ d' & -\frac{1}{R_\gamma} & \frac{1}{R_\gamma} \\ -1 & \frac{1}{R_\gamma} & -\frac{1}{R_\gamma} \end{bmatrix}}^{A}\cdot\begin{bmatrix} i_L(t) \\ v_{co}(t) \\ v_b(t) \end{bmatrix} + \\ + \overbrace{\begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{R_\gamma} \\ 1 & -\frac{1}{R_\gamma} \end{bmatrix}}^{B}\cdot\begin{bmatrix} i_{g\_bus(t)} \\ V_\gamma \end{bmatrix} \end{aligned} \tag{20}$$

$$\begin{aligned} \begin{bmatrix} i_L(t) \\ v_{co}(t) \\ v_b(t) \end{bmatrix} = \overbrace{\begin{bmatrix} 1 & 0 & 0 \\ 0 & \frac{1}{R_\gamma} & -\frac{1}{R_\gamma} \\ 0 & 0 & 1 \end{bmatrix}}^{C}\cdot\begin{bmatrix} i_L(t) \\ v_{co}(t) \\ v_b(t) \end{bmatrix} + \\ + \overbrace{\begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_\gamma} \\ 0 & 0 \end{bmatrix}}^{E}\cdot\begin{bmatrix} i_{g\_bus(t)} \\ V_\gamma \end{bmatrix} \end{aligned} \tag{21}$$

The transfer function relating the disturbance in load current as a function of a disturbance in the input current of the PC stage can be obtained by applying the matrix equation (22)

$$G_1(j\omega) = \frac{D(1-D) + C_o L\omega^2}{D^2 - \omega^2 \cdot (C_o L + C_{bus} L) + jR_\gamma \omega (C_{bus}(D^2 - C_X L\omega^2 - 2D + 1) + C_o)} \tag{23}$$

$$G_2(j\omega) = \frac{D(1-D)}{D^2 - \omega^2 \cdot C_{bus} L + jR_\gamma \omega (C_{bus}(D^2 - C_X L\omega^2 - 2D + 1) + C_o D^2)} \tag{24}$$

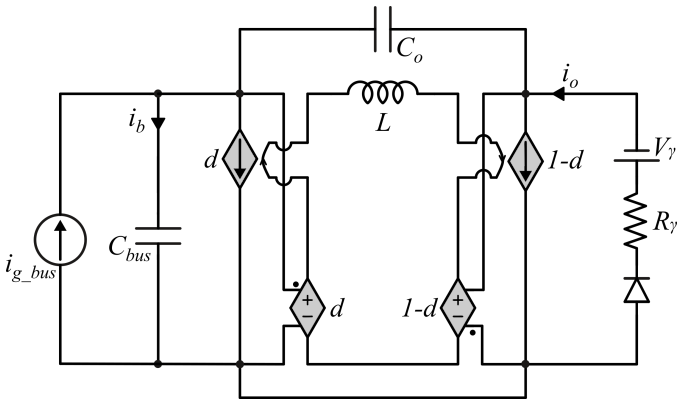


Fig. 6. Averaged equivalent circuit using controlled sources replacing ideal transformer.

to the system defined by (20) and (21), and making $s = j\omega$, resulting in (23). Aiming to compare the proposed circuit with the conventional counterpart, a similar approach can be done and its transfer function is given by (24).

$$G(s) = C_P \cdot (sI - A_P)^{-1} B_P + E_P \tag{22}$$

where,

$$A_P = K^{-1} A$$

$$B_P = K^{-1} B$$

$$C_P = C$$

$$E_P = E$$

To simulate the linear circuit in Fig. 5 under DC conditions, the transformer must be replaced by appropriate controlled sources with adequate gains, as shown in Fig. 6. Since the math model was obtained from the linear circuit, without any simplification, both, the transfer function or the linear model in Fig. 6 performs precisely the same response and these outputs are valid for large signals.

IV. Comparative Study Between buck-boost Converter with Alternative and Conventional Capacitor Connection

The transfer functions obtained in section III will be used to determine the output current modulation as a function of converter parameters for both, the proposed circuit and the conventional one. An expression for the output current modulation according to IEEE 1789-2015, can be obtained using the DC component and the AC component of the load current. Since the PC converter operates in CCM, the DC component of the output current can be related to the DC component of i_{g_bus} through the static gain of the converter:

$$I_o = \frac{1-D}{D} \cdot I_{g\_bus} \tag{25}$$

The AC component of the output current can be related to the AC component of the input current through (26). By making $\omega = 2\pi \cdot 2f_{line}$, where f_{line} is the grid voltage frequency,

$$\begin{aligned} \hat{I}_o &= |G_1(j4\pi f_{line})| \cdot \hat{I}_{g\_bus} = \\ &= \sqrt{\mathrm{Re}\left(G_1(j4\pi f_{line})\right)^2 + \mathrm{Im}\left(G_1(j4\pi f_{line})\right)^2} \cdot \hat{I}_{g\_bus} \end{aligned} \tag{26}$$

The output current modulation can be obtained by combining (25) and (26):

$$\begin{aligned} Mod_{alt\_ccm} &= 100 \times \frac{\overbrace{(I_o + \hat{I}_o)}^{I_{\max}} - \overbrace{(I_o - \hat{I}_o)}^{I_{\min}}}{\underbrace{(I_o + \hat{I}_o)}_{I_{\max}} + \underbrace{(I_o - \hat{I}_o)}_{I_{\min}}} = \\ &= 100 \times \frac{\hat{I}_o}{I_o} = 100 \times M_{bb\_ccm} \cdot |G_1(j4\pi f_{line})| \end{aligned} \tag{27}$$

Where, $M_{bb\_ccm} = \frac{D}{1-D}$, is the static gain module for the buck-boost converter in CCM.

An Equivalent equation for the conventional converter can be obteined by replacing $G_1(j\omega)$ by $G_2(j\omega)$ in (27). The output current modulation for the conventional converter in continuous conduction mode can be obtained by:

$$Mod_{conv\_ccm} = 100 \times M_{bb\_ccm} \cdot |G_2(j4\pi f_{line})| \tag{28}$$

Equation (6) leads to the conclusion that input current i_{g_bus} modulation is fixed to 100 %. Through (27) and (28), the output current modulation can be determined for both, the alternative buck-boost converter and the conventional counterpart as a function of the following circuit parameters: D, $R\gamma$, L, C_o, and C_{bus}.

The two capacitors and duty-cycle are the most suitable parameters for designing the low-frequency output ripple, as the pole associated with the inductor is situated in close proximity to the switching frequency, resulting in negligible effect on the system response at the double line-frequency. Consequently, the inductor can be chosen based on additional criteria such as cost, efficiency, or CCM margin. Moreover, the intrinsic resistance of the LED affects the modulation of the output current, but it is generally treated as an input parameter of the converter design as it is linked to the selection of

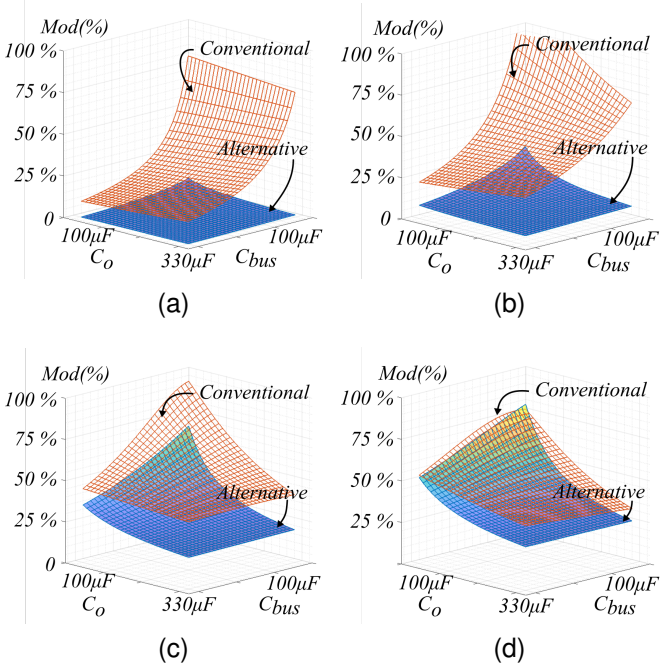


Fig. 7. Theorical modulation of the conventional and alternative converters as a function of the gain M and the capacitors C_o and C_{bus} in CCM. (a) $M = 0.32$. (b) $M = 0.50$. (c) $M = 1$. (d) $M = 1.25$.

the LED which is primarily determined by power, luminous efficacy, or even price.

A. Comparing Output Current Modulation Using Equal Capacitance for Both Converters

Fig. 7 displays the output current modulation of alternative and conventional converters, as a function of C_o and C_{bus} capacitors, using practical values as the domain for four different static gains. The surfaces were generated using (27) and (28), with the specified parameters of a 1200 µH inductor and LED from the numerical example in the following section.

The parameter D is related to both the PFC stage and the PC stage of an integrated converter. Specifically, D defines the equivalent resistance seen by the grid in the PFC stage, and the static gain of the second stage ($M = V_{LED}/V_b$). The comparative graphs in Fig. 7 use the static gain in lieu of D as it is more descriptive.

By inspecting the images, it is evident that the modulation for the alternative converter is always lower than the conventional counterpart when the converters are implemented using the same output capacitance value.

It is observed that the low-frequency ripple of both converters decreases as the static gain decreases, and it is possible to obtain lower ripples with lower capacitance values. Under this circumstance, the capacitor contribution in the alternative connection is less significant.

Particularly, the surfaces in Fig. 7c and 7d demonstrate that, as the static gain increases, the effect of the bus capacitor on output ripple reduction becomes less pronounced as C_o increases.

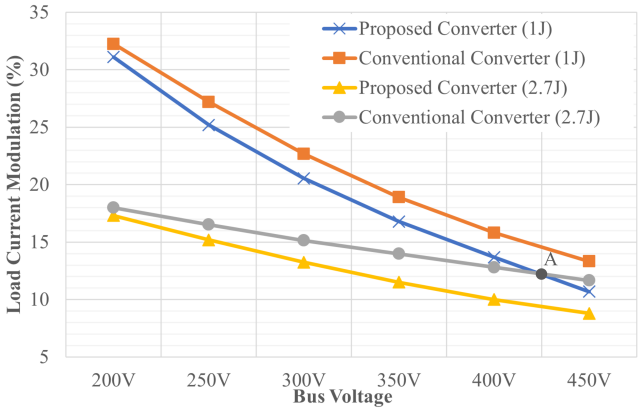


Fig. 8. Comparison of output current modulation in alternative and conventional converters with 1 J and 2.7 J of stored energy with respect to a bus voltage variation from 200 V to 450 V.

B. Comparison for the Output Current Modulation at Fixed Output Capacitors Energy

As illustrated in the previous subsection, the proposed topology always ensures lower ripple than the conventional counterpart when fixing the same capacitance values and at the same operating point. However, the voltage across the capacitors is different. In the conventional topology, the output capacitor must withstand the load voltage (V_{LED}), while in the alternative topology, the output capacitor must withstand the sum of the load and bus voltages ($V_{LED} + V_b$). At this point, it is mandatory to analyze the energy stored in the capacitance and determine which topology performs better in terms of capacitor's energy. Thus, this subsection examines the situation where the same amount of energy is stored in both capacitors, comparing the resulting LED current modulation.

Fig. 8 shows the output current modulation of both the alternative and conventional converters with respect to variations in the bus voltage, from 200 V to 450 V. This figure presents the modulation of both converters considering 1 J and 2.7 J of energy stored, which corresponds to the conventional topology employing output capacitors of 200 μF and 540 μF, respectively. Therefore, the capacitance of the conventional converter remains constant across the entire voltage range for the same energy, while the capacitance of the alternative converter decreases as the bus voltage increases.

Tables I and II provide details about the operating points in Fig. 8 for 1 J and 2.7 J, respectively. The tables display the theoretical output current modulation calculated using equations (27) and (28). For each bus voltage, the capacitances and V_{co} related to the 1 J and 2.7 J reference energy are also displayed.

As can be seen that the output current modulation of the alternative converter is lower than that of the conventional converter when the same amount of energy is stored in both converters' output capacitor. Moreover, as the bus voltage increases, the output current modulation of the alternative converter is much lower compared to the conventional converter. Taking point A in Fig. 8 as an example, for $V_b = 425$ V,

TABLE I
OPERATION PARAMENTERS FOR 1 J STORED ENERGY.

	Alternative			*Conventional*		
V_b	C_o	V_{co}	$Mod_{\%}$	C_o	V_{co}	$Mod_{\%}$
200 V	22.5 µF	300 V	31.1 %	200 µF	100 V	32.3 %
250 V	16.6 µF	350 V	25.2 %	200 µF	100 V	27.2 %
300 V	12.6 µF	400 V	20.5 %	200 µF	100 V	22.7 %
350 V	10 µF	450 V	16.8 %	200 µF	100 V	18.9 %
400 V	8.1 µF	500 V	13.7 %	200 µF	100 V	15.8 %
450 V	6.7 µF	550 V	10.7 %	200 µF	100 V	13.3 %

TABLE II
OPERATION PARAMENTERS FOR 2.7 J STORED ENERGY.

	Alternative			*Conventional*		
V_b	C_o	V_{co}	$Mod_{\%}$	C_o	V_{co}	$Mod_{\%}$
200 V	60 µF	300 V	17.3 %	540 µF	100 V	18 %
250 V	44 µF	350 V	15.2 %	540 µF	100 V	16.5 %
300 V	34 µF	400 V	13.2 %	540 µF	100 V	15.2 %
350 V	26.7 µF	450 V	11.5 %	540 µF	100 V	13.4 %
400 V	21.6 µF	500 V	10 %	540 µF	100 V	12.8 %
450 V	17.9 µF	550 V	8.8 %	540 µF	100 V	11.7 %

the proposed converter with 1 J of stored energy presents the same load current modulation as the conventional converter with 2.7 J, which represents a reduction of 2.7 times of the stored energy.

V. DESIGN PROCEDURE OF THE LABORATORY PROTOTYPE

This section presents a design procedure for the experimental verification performed in section VI. The proposed circuit and a conventional converter with C_o connected in parallel to the load, as shown by the dashed capacitor in Fig. 3, were designed at the same operating point. The circuits will drive a series connection of 2 Cree XLamp 2890 LEDs [25] and operate it at 95 W. The input voltage and line frequency are assumed to be $V_g = 220\,\mathrm{V}$ and $f_{line} = 60\,\mathrm{Hz}$, respectively.

A buck-boost PFC stage will be designed to operate in DCM to meet the IEC 61.000-3-2 class C limits. The buck-boost PC stage will operate in CCM. For comparative purposes, the proposed circuit is designed to provide an output current 120 Hz ripple to fulfill the IEEE 1789-2015 recommendation, and the conventional counterpart is tested at the same conditions.

For the specified output power, an average load current determined by the LED characteristic curve evaluated from the manufacturer datasheet [25] is $I_o = 960\,\mathrm{mA}$, and its corresponding voltage when two LEDs are in series connection is:

$$V_{LED} = V_\gamma + R_\gamma \cdot I_o = 98.8\,\mathrm{V} \tag{29}$$

where, $V_\gamma = 86\,\mathrm{V}$ and $R_\gamma = 13.3\,\Omega$.

According to Fig. 7, multiple static gains for the PC stage can be selected and the low-frequency ripple is always smaller for the proposed topology than the conventional counterpart. To validate the model, a static gain $M = 0.32$ was chosen. based on the output voltage, the corresponding bus voltage must be $V_b = 300\,\mathrm{V}$.

The duty-cycle for a PC stage buck-boost operating in CCM and providing the static gain defined above is:

$$D = \frac{V_{LED}}{V_b + V_{LED}} = 0.248 \tag{30}$$

The critical duty-cycle for a PFC stage with $V_b = 300\,\mathrm{V}$ and nominal input voltage $V_g = 220\,\mathrm{V}$ operating in DCM is:

$$D_{crit} = \frac{V_b}{220\,\mathrm{V} \cdot \sqrt{2}} = 0.96 \tag{31}$$

Since the operating duty-cycle calculated in (30) is smaller than the critical duty-cycle, it is possible to design the PFC stage operating in DCM at the established input and bus voltages. Considering lossless stages, the converter equivalent resistance seen from the mains can be calculated by:

$$R_{PFC} = \frac{V_{rms}^2}{P} = 510\,\Omega \tag{32}$$

And the PFC stage inductor that will define the input power, when $fs = 100\,\mathrm{kHz}$ and $D = 0.24$, can be calculated as follows:

$$L_{PFC} = \frac{R_{PFC} \cdot D^2}{2 \cdot fs} = 156\,\mu\mathrm{H} \tag{33}$$

For the PC stage inductor, which in turn operates in CCM, a high-frequency ripple $\Delta i = 800\,\mathrm{mA}$ was arbitrarily selected. Thus, the PC stage inductor is given by:

$$L = \frac{V_b \cdot D}{\Delta i \cdot fs} = 1200\,\mu\mathrm{H} \tag{34}$$

Finally, the DC and AC components for the i_g_bus current supplied by the PFC stage are:

$$I_{g\_bus} = \hat{I}_{g\_bus} = \frac{P}{V_b} = 316\,\mathrm{mA} \tag{35}$$

A cross-section from Fig. 7a at $C_{bus} = 33\,\mu\mathrm{F}$ is shown in Fig. 9. The selection of a small bus capacitor in this study is done to better demonstrate the impact of the alternative converter and to allow for the use of a non-electrolytic technology. From the curve, it can be seen that a capacitor $C_o = 82\,\mu\mathrm{F}$, should lead to an output current modulation below IEEE1789-2015 recommendation at 120 Hz ($< 10\,\%$).

The selected capacitors, $C_{bus} = 33\,\mu\mathrm{F}$ and $C_o = 82\,\mu\mathrm{F}$ lead to the following theoretical output current modulations for the proposed topology and its conventional counterpart:

$$Mod_{alt\_ccm} = M_{bb\_ccm} \cdot |G_1(j2\pi 120\,\mathrm{Hz})| = 8.05\,\% \tag{36}$$

$$Mod_{conv\_ccm} = M_{bb\_ccm} \cdot |G_2(j2\pi 120\,\mathrm{Hz})| = 27.55\,\% \tag{37}$$

VI. EXPERIMENTAL VERIFICATION

This section presents the experimental results obtained from the laboratory prototype based on the design procedure performed in section V.

Table III summarizes the parameters used in the experiments.

Fig. 10 shows the prototype used in the tests. Both, the proposed topology and the conventional counterpart can be mounted using the same PCB. Two PQ3220 core sizes were

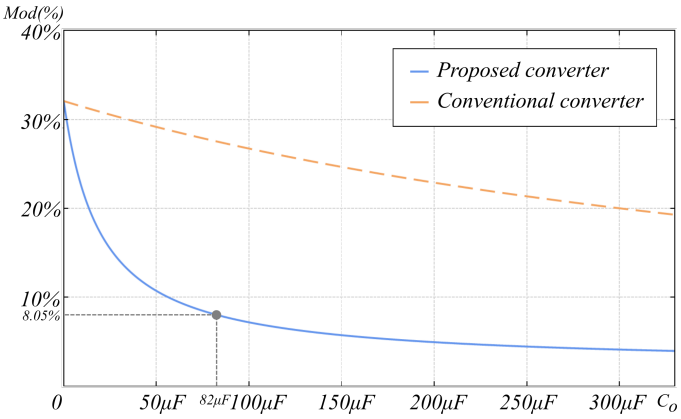


Fig. 9. cross-section from Fig. 7d. Output current modulation as a function of C_o, using $M = 1.5$ and $C_{bus} = 33\,\mu$F.

used to construct the PFC and PC inductors. The inductors are detailed in Table IV, where semiconductors and input LC differential filter are listed as well.

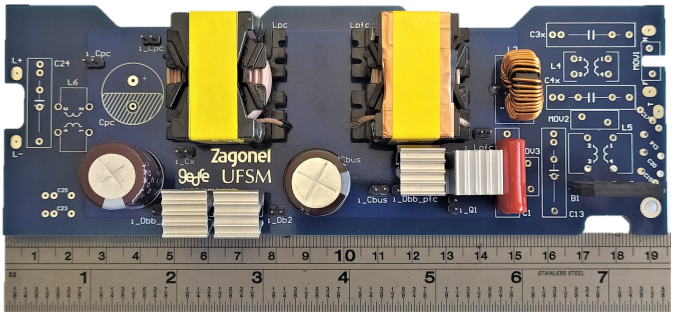


Fig. 10. Prototype photograph. Integrated buck-boost PFC and buck-boost PC with alternative and conventional output capacitor configuration.

The line voltage and input current waveforms are shown in Fig. 11, where it can be inferred a sinusoidal current shape. The analysis for IEC 61.000-3-2 class C standard was evaluated using a Keysight DSO-X 4024 digital oscilloscope with a power quality analysis package at 220 V. The harmonic content is below the limits, THD is 2.49 %, and PF 0.99. It can be checked that the proposed converter meets the IEC 61.000-3-2 Class C limits [26]. The harmonic content of the input current, which was obtained from measurements, is illustrated in Fig. 12. The vertical scale maximum was set to 5 % for improved visualization, despite the 3rd, 5th, 7th, and 9th harmonic limits are 30 %, 10 %, 7 %, and 5 %, respectively.

TABLE III
EXPERIMENTAL PARAMETERS

Parameter	*Symbol*	*Value*
Switching frequency	fs	100 kHz
Duty-cycle	D	0.24
Designed bus voltage	V_b	300 V
PC converter inductance	L	1200 μH
PFC converter inductance	L_{PFC}	156 μH
Bus capacitor	C_{bus}	33 μF
Output capacitor	C_o	82 μF

TABLE IV
PROTOTYPE BILL OF COMPONENTS

Component item	*Part number*	*Description*
L_{PFC}	156 μH	PQ3220, 56 turns AWG34x17
L_{PC}	1200 μH	PQ3220, 95 turns AWG34x17
MOSFET	IPA95R450P7	MOSFET N-CH 950 V 14 A
D_{BB1}	SCS208AM	DIODE SCHOTTKY 650 V 8 A
D_{BB2}, D_i	BYC10DX-600	Hyperfast diode 600 V 10 A
C_{bus}	33 μF	400 V electrolytic capacitor
C_o	82 μF	450 V electrolytic capacitor
Filter Capacitor	680 nF	250 V AC filter capacitor
Filter Inductor	180 uH	14 mm, 90 turns AWG27x1

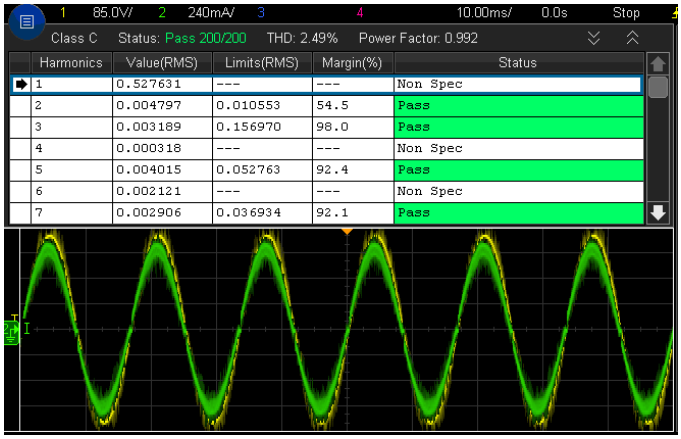


Fig. 11. Input current IEC 61.000-3-2 class C test for the proposed converter.

Fig. 13 shows the load current for the alternative and the conventional converter under the above conditions (pink waveform). It can be inferred that low-frequency ripple is smaller for the proposed topology, not only for output current, but also for bus voltage (yellow waveform).

The modulation for the output currents in both converters,

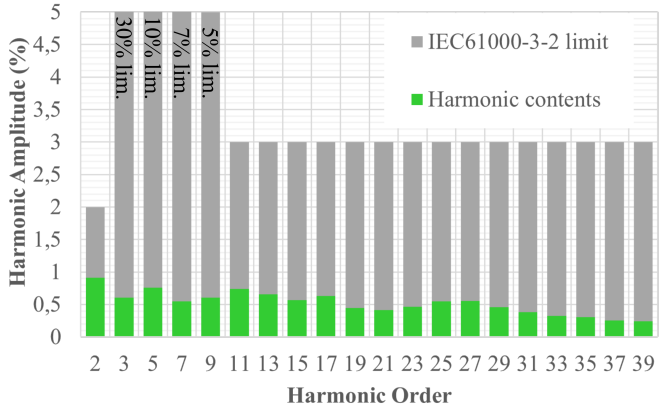
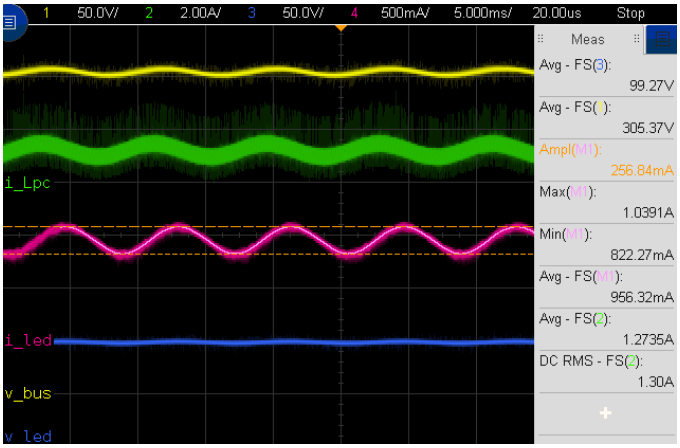
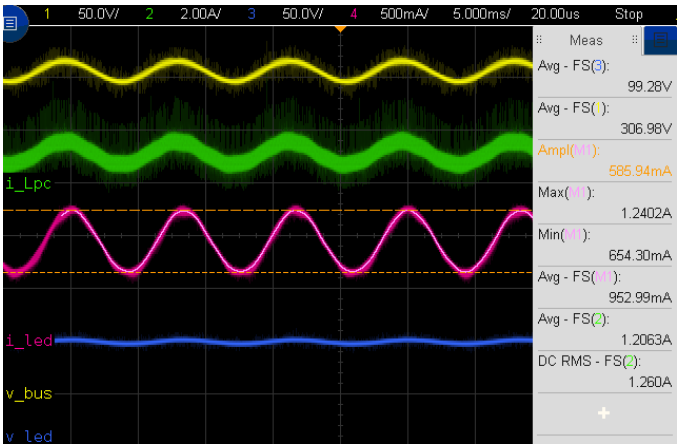


Fig. 12. Input current harmonic contents and IEC 61000-3-2 limits for 220 V rms input voltage.



(a)



(b)

Fig. 13. Output current waveforms. (a) Proposed converter. (b) Conventional converter.

obtained through the experiments, are the following:

$$Mod_{alt\_ccm} = \frac{I_{o\_pk} - I_o}{I_o} = \\ = \frac{1.0391\,\text{A} - 956.32\,\text{mA}}{956.32\,\text{mA}} = 8.66\,\% \tag{38}$$

$$Mod_{conv\_ccm} = \frac{I_{o\_pk} - I_o}{I_o} = \\ = \frac{1.2402\,\text{A} - 952.99\,\text{mA}}{952.99\,\text{mA}} = 30.14\,\% \tag{39}$$

It can be seen that both agree with the theoretical values, shown in (36) and (37). It means that the ripple for the proposed topology is a third of the conventional converter ripple. The former complies with IEEE Std. 1789-2015 recommendation, while the conventional converter does not meet the flicker recommendations.

Table V presents measurements of voltage and current for the elements of the two compared circuits, both, for the laboratory prototype and for simulation. The LED average current and the voltage of C_{bus} capacitor demonstrate that both circuits were operating at the same point. The capacitor current C_{bus} in the alternative converter is smaller than the current through the same capacitor in the conventional counterpart. It is an important effect since the capacitor ripple current is an important selection parameter and impacts directly the capacitor lifespan. There is no difference in current or voltage MOSFET stresses when operating in any of the compared circuits. The current in capacitor C_o is very similar in both cases, although, the voltage level for the alternative converter is higher than the conventional counterpart, being the main drawback. As shown in Fig. 1, the buck-boost converter in the alternative connection of capacitor C_o is equivalent to a boost converter with the load in the alternative connection. Therefore, the voltage at capacitor C_o is always greater than or equal to the bus voltage.

Finally, the efficiency was measured using WT1800 Yokogawa precision power analyzer. It is important to highlight that the design was not optimized for efficiency, and both converters were compared at a single input voltage, and no significant changes in semiconductor current or voltage were detected. Only the bus capacitor RMS current had a significant decrease in the proposed topology, with no significant impact on overall efficiency. It can be seen that the circuits achieved similar efficiency.

The simulation results were obtained using PSIM software from Powersim. Although the simulation results are very close to the experimental results, there are some differences related to the fact that simulation uses ideal components, and there are no losses. The output current modulation obtained through simulation are even closer to the theoretical prediction than the real laboratory prototype, reinforcing the model validation.

TABLE V
MEASUREMENTS RESULTS - EXPERIMENTAL AND SIMULATION

Parameter	***Proposed Circuit***		***Conventional Circuit***	
Method	**Experim.**	**Simul.**	**Experim.**	**Simul.**
MOSFET I_{rms}	1.86 A	1.605 A	1.88 A	1.61 A
MOSFET V_{max}	613.7 V	610 V	620.3 V	607 V
C_{bus} I_{rms}	909 mA	804 mA	1.34 A	1.18 A
C_{bus} V_{avg}	305.37 V	296 V	306.98 V	296 V
C_o I_{rms}	690 mA	606 mA	864 mA	618 mA
C_o V_{avg}	402 V	395 V	99.28 V	98.84 V
L_{PC} I_{rms}	1.30 A	1.32 A	1.26 A	1.354 A
LED I_{avg}	1.1 A	972 mA	1.1 A	967 mA
LED I_{pk-pk}	256.8 mA	184 mA	585.9 mA	543.7 mA
LED $Mod_{\%}$	8.66 %	8.12 %	30.14 %	27.68 %
$Efficiency_{\%}$	89.31 %	-	89.12 %	-

VII. CONCLUSION

The IEEE 1789-2015 is a recommendation for measuring and assessing the amount of flicker from light sources. This document also provides guidance for determining the acceptability of flicker levels, considering the duration and frequency of the flicker, and the potential impacts on human observers. Despite the fact that the constancy of the light intensity is also affected by different factors such as thermal and optical issues, the current ripple is an key factor regarding light quality.

In integrated converters, the loss of independence between the stages makes it impractical to adopt control techniques that act directly on the duty cycle, aiming to actively eliminate

the low-frequency ripple in the output current without distorting the input current causing degradation of input current harmonic content and, consequently of the power factor.

This paper presented a novel topology to reduce the required capacitance for LED drivers, considering the IEEE 1789-2015 recommendations, in which the output capacitor of the buck-boost converter in the PC stage is connected in feedback to the bus capacitor to mitigate the low-frequency ripple in the output current for converters operating under constant duty-cycle conditions. The dynamic models for the proposed circuit and its counterpart were evaluated, validated and used to determine the output current modulation as a function of converter parameters.

A comparative study between the proposed topology and a conventional two-stage integrated converter was performed by two different approaches. The first method was based in the case when the same capacitance value is used in both circuits. It was shown that the proposed topology always achieve better output ripple than the conventional topology, but at the cost of higher voltage at the output capacitor, and consequently higher stored energy. The second method compared the modulation when different capacitances but equivalent energy ratings are used in both circuits. It was shown that the proposed topology can achieve better results than the conventional counterpart, allowing the circuit to comply with IEEE 1789-2015 recommendations using smaller capacitors.

When integrated converters are operated under universal input voltage, the bus voltage presents a high variation. Thus, the design of the bus capacitor becomes non-optimal. In this scenario, using a lower bus capacitance associated with a higher output capacitance for low frequency ripple mitigation purposes becomes an option for optimizing the capacitors' design.

The experimental verification showed that no degradation on efficiency or input current harmonic content is occasioned by the proposed technique, and the obtained results demonstrate that theoretical mathematical models can be used to predict the performance of the proposed topology.

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VIII. Biography Section

Nelson da S. Spode received the B.Sc. and M.Sc. degrees in electrical engineering from the Federal University of Santa Maria (UFSM), Santa Maria, Brazil, in 2005 and 2018, respectively. Since 2005, he has been a Hardware and Software Engineer with the industry (Zagonel SA.). He has been a Researcher with the GEDRE – Intelligence for Lighting Group, UFSM since 2016. His research interests include lighting systems, control systems, power electronics, EMC, computer programming languages, and IoT.

Marco A. Dalla Costa (S'03, M'09, SM´17) received his B.S. and M.Sc. degrees in Electrical Engineering from the Federal University of Santa Maria, Brazil, in 2002 and 2004, respectively. He earned his Ph.D. degree (with honors) in Electrical Engineering from the University of Oviedo, Spain, in 2008. Since 2009, he has been a Professor at the Federal University of Santa Maria, Brazil. He has co-authored more than 200 journal and conference papers. His research interests include power electronics applied to lighting systems, LED drivers, LED modeling, horticultural lighting, and visible light communication systems. Dr. Dalla Costa is currently serving as an Associate Editor for the IEEE Transactions on Industrial Electronics and for the IEEE Journal of Emerging and Selected Topics in Power Electronics. He also chaired ILDC (2019-2020) and MSDAD (2020-2021), both from the IEEE Industry Applications Society.

Guirguis Z. Abdelmessih (S'15, M'23) received his B.Sc. degree in Electrical Engineering from the University of Ain Shams, Egypt, in 2013. He received his M.Sc. degree in "Electrical Energy Conversion and Power Systems" and his Ph.D. degree (with honors) on "analysis and development of improved converters for LED drivers with special focus on efficiency and dimming" from the University of Oviedo, Gijón, Spain, in 2015 and 2020, respectively. He is currently working as a Professor Assistant at the electromechanical department of the University of Burgos, Spain. Dr. Guirguis is the co-author of more than 20 journal and conference publications, including 7 publications in highly referenced journals. His research interests include light-emitting diodes, LED drivers, dc/dc converters, ac/dc converters, PFC stages, dimming systems, renewable energy, and power systems.

J. Marcos Alonso (F'22). He received the M. Sc. Degree and Ph. D. (with honors) both in electrical engineering from the University of Oviedo, Spain, in 1990 and 1994, respectively. Since 2007, he is a full Professor at the Electrical Engineering Department of the University of Oviedo. Prof. Alonso is the co-author of more than 450 journal and conference publications, including 130 publications in highly referenced journals. He has published 3 books and 2 book chapters. His research interests include electronic lighting, dc-dc converters, resonant inverters, wireless power transfer, and single-phase high-frequency switching converters in general. He is the holder of 8 national and international patents. Prof. Alonso has been awarded with the Early Career Award of the IEEE IES in 2006. He was honored with the University of Oviedo Electrical Engineering Doctorate Award. He also holds 12 IEEE paper awards. He currently serves as Co-Editor-in-Chief of the IEEE Transactions on Power Electronics. He has been Guest Editor of several IEEE journal special issues and has organized many IEEE conference special sessions. He was Chair of the IAS Industrial Lighting and Displays Committee (2017-2018). He has served as Member-at-Large of the IEEE IAS Executive Board (2013-2016), IAS Newsletter Editor (2013-2018), and Chair of the IAS Awards Department (2017-2019).

Renan Rodrigo Duarte was born in Santo Augusto, Brazil, in 1992. He received his B.S., M.Sc. and PhD degrees in electrical engineering from the Federal University of Santa Maria, Brazil, in 2015, 2017 and 2022, respectively. He is currently a postdoctoral student at the same institution. Since 2020 he has been working as R&D engineer at Zagonel S.A. in Brazil, developing hardware and software solutions for heating systems and LED lighting. Dr. Duarte is member of the Brazilian Society of Power Electronics and from 2016 to 2018 he was vice president of the IEEE UFSM Student Branch and the IAS chapter at the same institution.