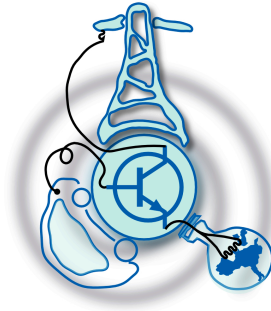


Design of a Switched Mode Latching Current Limiter for Aerospace applications

by
Javier Prado Pico



Submitted to the Department of Electrical Engineering, Electronics,
Communications and Systems
in partial fulfillment of the requirements for the degree of
Master of Science in Electrical Energy Conversion and Power Systems
at the
UNIVERSIDAD DE OVIEDO

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Abstract

Limiting Current Lockout (LCL) circuits are used to protect satellite-connected loads from overcurrents. Their main function is to restrict the maximum current generated during a specific predetermined period of time when an overload occurs. If the overcurrent persists during this time frame, the LCL disconnects the load from the main power bus. The critical element in the LCL's operation is the semiconductor device responsible for current limitation. LCL topologies traditionally used P-channel devices due to their ease of control. However, recent advancements in Wide Band Gap (WBG) materials, such as Silicon Carbide (SiC), have opened up the possibility of using N-channel SiC MOSFETs as current-limiting devices.

In this context, this work presents the design of an LCL architecture based on SiC N-channel MOSFETs, operating in a switching mode during the current limitation stage. This approach aims to reduce the thermal stress on the current-limiting device during an overload. The work outlines the design considerations for selecting and implementing the topology in relation to magnetic components. Additionally, experimental results from a switched LCL prototype based on the proposed topology are provided.

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This final master thesis is dedicated to my father, who saw me start this work but never saw me finish it, and without whom I would not be in this position.

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Chapter 1

Introduction

It is critical for the safety of a satellite to supervise and control the amount of current drawn from each payload as to not discharge the battery too fast or create a short circuit in the bus that could affect other payloads. In case of a short circuit or an overcurrent, the satellite should be able to isolate the faulty payload from the rest of the bus.

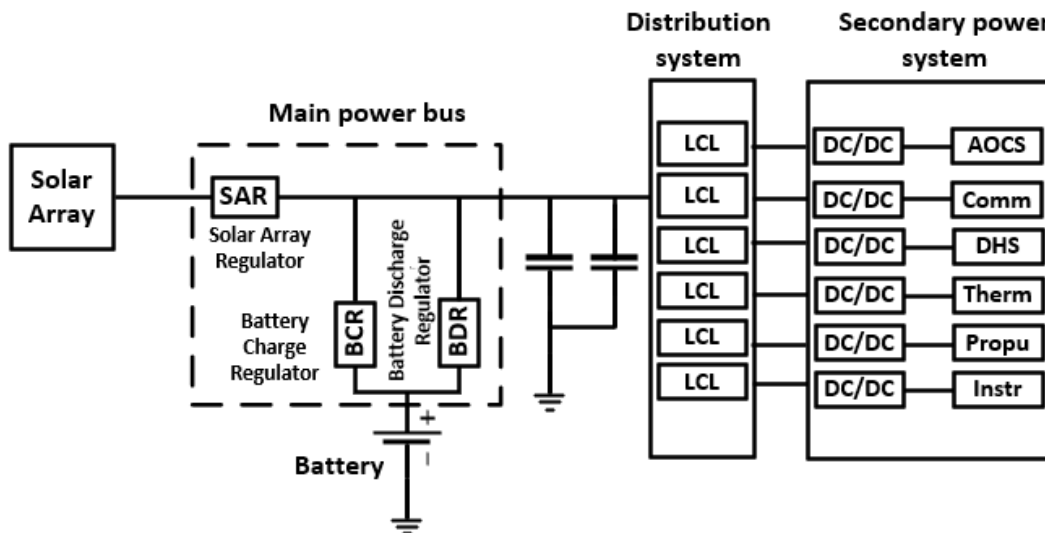


Figure 1-1: Regulated power bus in a satellite

Traditionally, linear current limiters have been used. These devices use a P channel MOSFET in linear region, working as a variable resistor to adjust the current in the payload. However, this comes with a series of disadvantages, not only do P channel MOSFETs have a higher ON resistance (R_{ds}) than N-channel, but also working in this point produces a lot

of heat, difficult to dissipate in space. Although other designs have been proposed using N-channel MOSFETS, they are still working in the linear region to control the current.

This thesis aims to design and test a new kind of current limiter known as "latching current limiter" (LCL), able to turn on and off loads but also regulate load for longer amounts of time without overheating.

Part of the work proposed in this document was published and presented in the "Seminario anual de automática, electrónica industrial e instrumentación" SAAEI.

1.1 Work organization

This work is divided in 4 main chapters:

- Chapter 1: Introduction. In this chapter the need of current limiters is explained, and the aim of the project.
- Chapter 2: Background research and state of the art. Introduction to satellite power schemes, regulations and current circuits to regulate load. In the context of the project regarding the "European space agency" (ESA).
- Chapter 3: Latching current limiter design proposal. Main equations and design parameters that manage the LCL working behaviour.
- Chapter 4: Simulations and results. Simulated operation of the LCL and comparison with the built prototype.

Chapter 2

Background knowledge and state of the Art

The term "payload" refers to the instruments, equipment, or devices that are carried on board a satellite for a specific purpose or function. These are connected to a DC bus fed from solar panels or nuclear generators and batteries. For the safety and power quality of the DC bus, it is mandatory that each payload has a current limiter to avoid an excessive current demand that could drain the battery or a short circuit in the bus, affecting other payloads.

While consumer electronics use a fuse, this is not practical for space applications as it is almost impossible to replace it in case of a short term overload. One way to represent the working principle of a LCL is as a "smart retriggerable fuse". An usual solution for satellite applications is based on the use of P MOSFETS[10] (Fig. 2-1), working in ohmic region. In case of a short circuit, it will increase its resistance to limit the current. As it is based on a semiconductor, it can be re-armed in case the fault disappears. In Fig.2-2 it can be seen the current profile of the linear LCL.

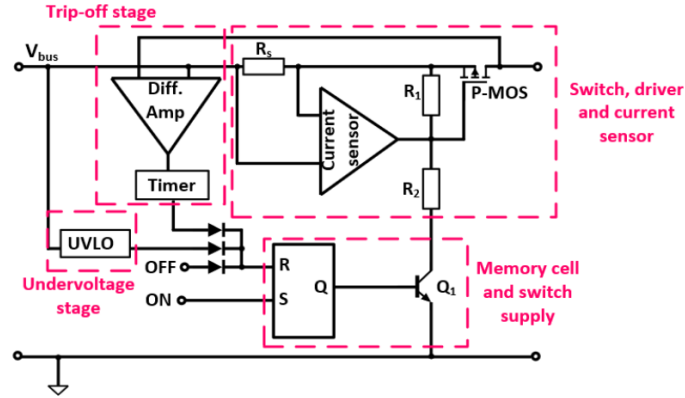


Figure 2-1: Traditional PMOS current limiter architecture

However, P channel MOSFETS have higher R_{ds} in saturation than N channel MOSFETS, leading to higher power losses. On top of that, the transistor is bearing all the bus voltage while fixing a current, dissipating a large amount of power.

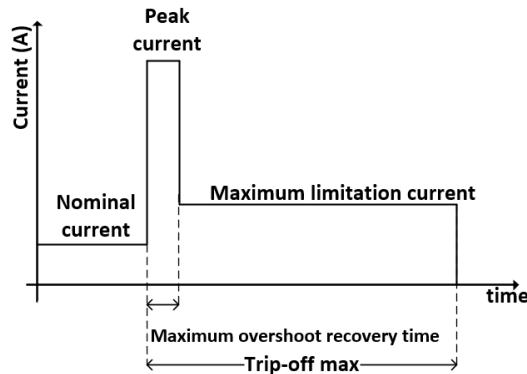


Figure 2-2: Current profile for a linear LCL

Some studies [8], [7] about using silicon carbide (SiC) N-MOSFETs have been presented in the literature, showing some key points related to the driving circuitry, transistor selection, and power supply.

Other topologies have been proposed using N-channel MOSFETs as the one on [6] and represented in Fig.2-3. In this case an N channel MOSFET was used, turned ON by an isolated DCX converter, that applies a gate source voltage (V_{gs}) to a Sic MOSFET. This topology greatly reduces the ON state resistance, but in the fault scenario, the device is still working in linear region.

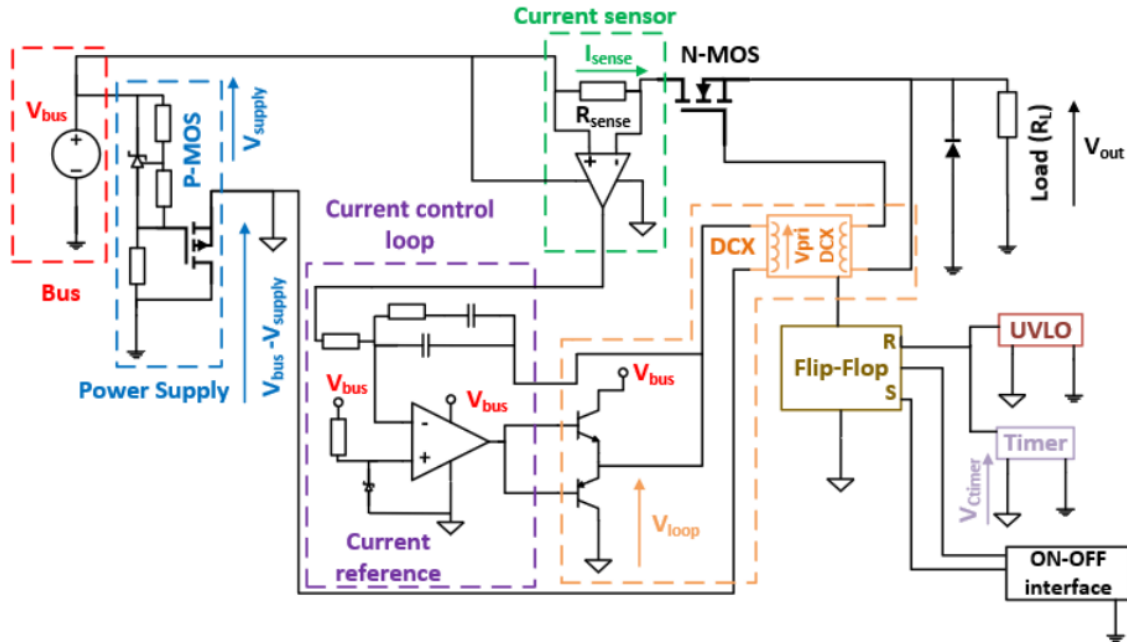


Figure 2-3: SiC NMOS based LCL architecture

2.1 European Space Agency regulations for current limiters

The European Space Agency (ESA) issues a series of regulation to ensure the safety and standardization of all components used in their missions. These requirements are found in the ECSS [4, 3, 2] (European Cooperation for Space Standardization).

- Current limiters will be grouped in classes according to their nominal current configuration. They are typically integer numbers (1A, 2A, 3A...) and fractions (0,25A, 0,5A) for lower power and also by trip-off time, maximum dissipated power and required voltage drop.
- Current in the load during a fault must be kept between 1.1 and 1.4 of the nominal values.
- Under voltage protection is needed to ensure bus stability

- All loads must have a diode in anti-parallel to ensure safety when disconnecting inductive loads.

Current profile is represented in Fig. 2-4

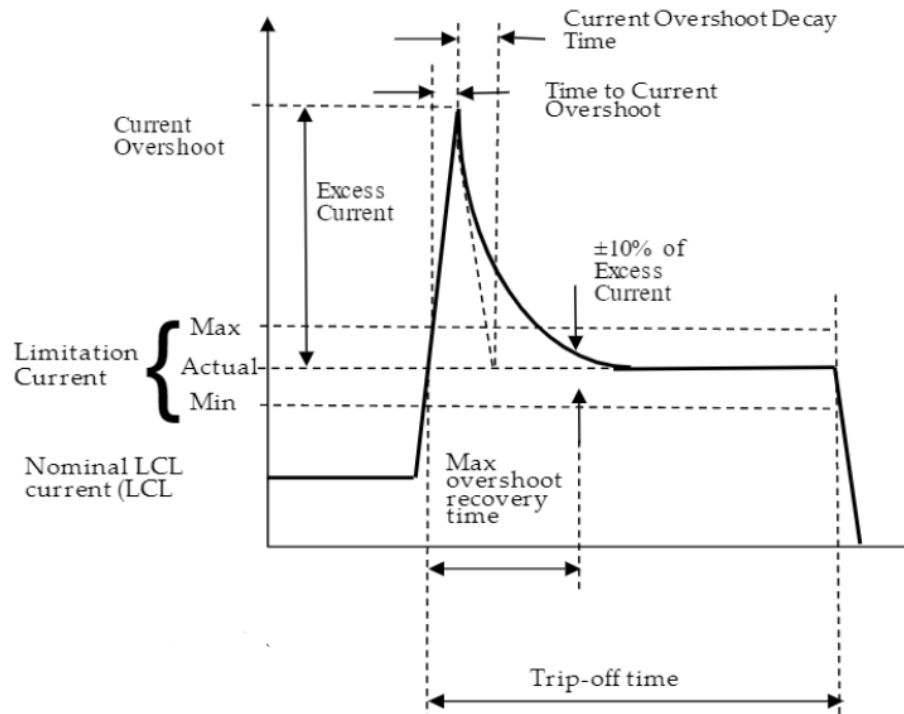


Figure 2-4: Desired current profile under a fault [2]

After operating in normal conditions, a fault appears and a current overshoot is created. After that, the device limits the current within the tolerance band and, after the trip-off time, it disconnects the load.

2.2 Latching current limiter motivation

As previously discussed, the current limiter device uses a semiconductor operating in the linear region, along with an anti-parallel diode as required by the regulations outlined in section 2.1. This configuration is similar to the buck converter, with the exception of an inductor and a capacitor.

By incorporating an inductor into the design, the device would be able to switch, which would alleviate stress on the semiconductor and simplify control. The capacitor is not necessary, as the objective is to regulate current through the inductor, not to the load. The topology of the resulting converter is shown in the figure 2-5.

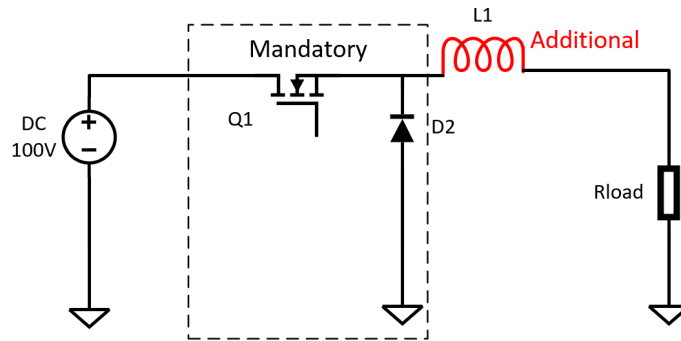


Figure 2-5: Switched LCL structure using a N-MOS device

The developed alternative is a switched latching current limiter, that will be explained in the next section.

Chapter 3

Switched latching current limiter design proposal

3.1 Working principle

The operation of the LCL can be divided in three operation regions: Normal operation, current regulation or fault condition and load disconnection.

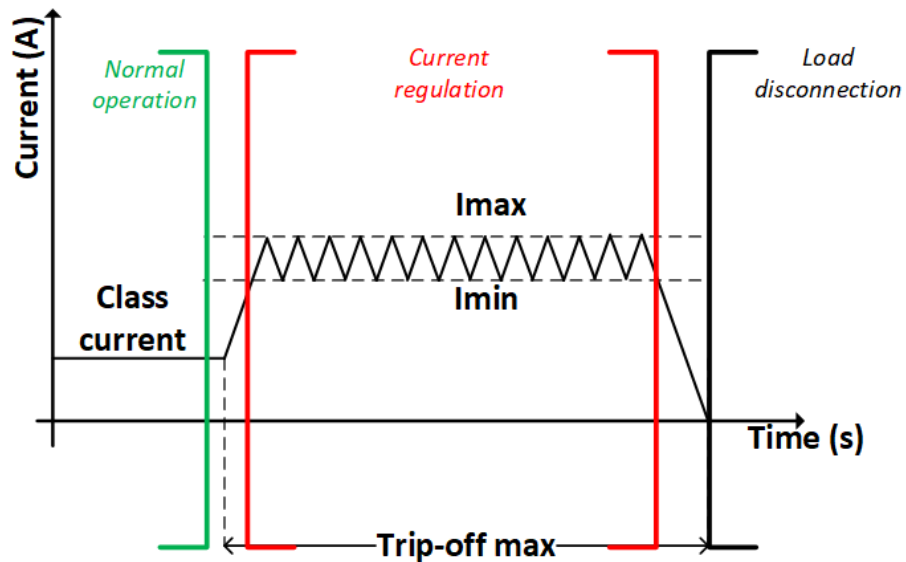


Figure 3-1: Inductor current during normal and fault operation

3.1.1 Normal operation

During normal operation, the MOSFET remains in the ohmic range with the lowest R_{ds} and feeds the load. In this mode, the losses are only in the measuring shunt resistor, MOSFET resistor, and inductor DC resistance.

3.1.2 Fault operation

In the event of a fault, the device detects an over-current and switches OFF the MOSFET. The current should continue to flow through the inductor, so the diode conducts and feeds the load. The current in the inductor will decrease following equation 3.1, where V_{shct} is the remaining voltage on the load.

$$I_L(t) = \frac{1}{L} \int -V_{shct} dt \quad (3.1)$$

It will continue to decrease until it reaches the lower limit, at which point the MOSFET turns ON, diode turns OFF, and the current through the inductor starts to increase following 3.2.

$$I_L(t) = \frac{1}{L} \int V_{bus} - V_{Load} dt \quad (3.2)$$

3.1.3 Load disconnection

During the current regulation region there are two possible outcomes: Returning to nominal value or maintaining the fault.

In the first case, current will return to nominal values before the trip-off time reaches its maximum, with the system returning to its normal operation.

Second option, failing to return to nominal conditions before the trip-off time reaches maximum, the load is disconnected from the main bus. This is not a permanent state, and it can be re-initialized later by telecommand.

3.2 Magnitude measurements

The current through the inductor needs to be controlled. The easiest way to measure the current is by taking the measurement right after the inductor (Fig.3-2). At this point, the current waveform is filtered by the inductance, producing a clean signal that could be measured with a sensor. The selection of the sensor must be careful, as it needs to have a high bandwidth. For space application, the variety of sensors is limited. Currently there is not space qualified hall-effect sensor with enough bandwidth to meet the application, therefore, the only option left is to use shunt resistors.

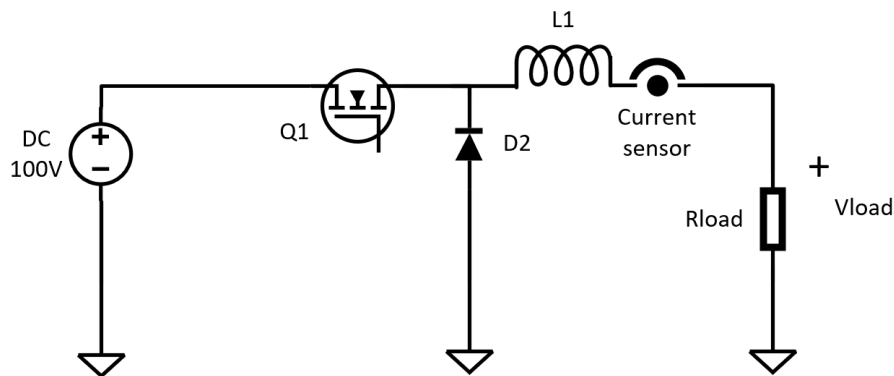


Figure 3-2: Current measurement circuit after the inductor

A possible solution is to make the signal conditioning using a bipolar junction transistor (BJT) sensor (which will be discussed later in Section 3.2.1), but to ensure the reliable working of the sensor, a minimum voltage is needed to bias the transistors. In the worst-case scenario, if there is a short-circuit at the output of the LCL, the voltage at this point will be zero, and the sensor will not work properly. This can be seen in the test performed in Fig.3-3, while supplying the shunt resistor with a constant current and a positive voltage in the load (V_{load}), the sensor measurement is as expected. However, when the V_{load} voltage goes to zero, the measurement gets affected, although the current remains constant.

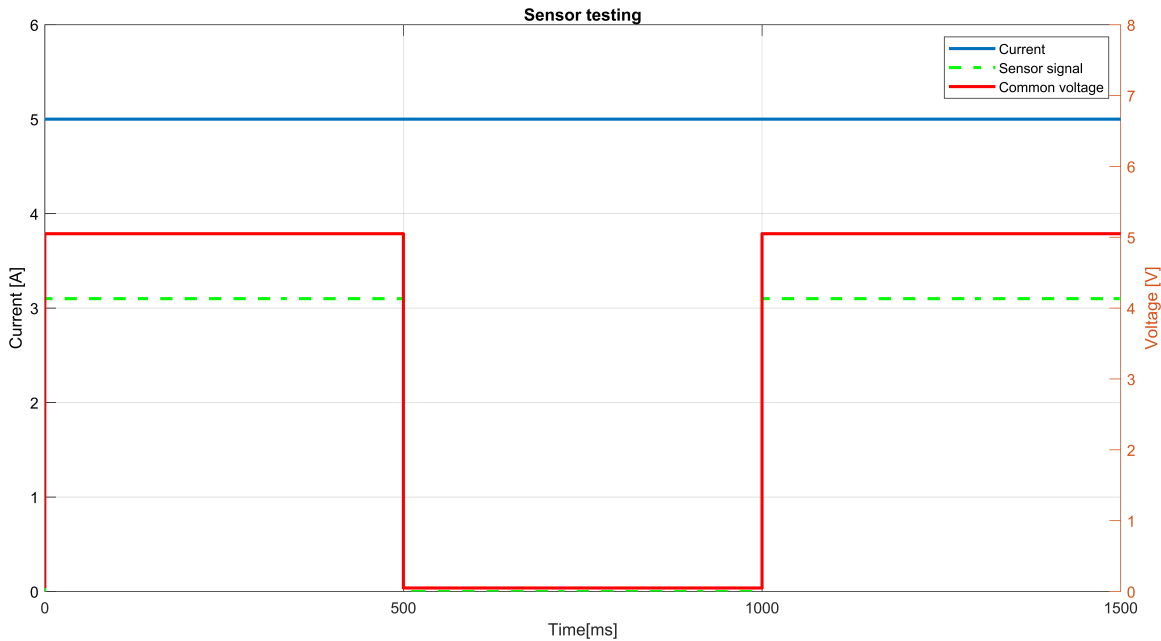


Figure 3-3: Current measurement after the inductor

The second option is to measure at the switching node, right before the inductor (Fig.3-4). At this point the current waveform could be affected by the switching noise, but enough polarizing voltage would be supplied to the current mirror.

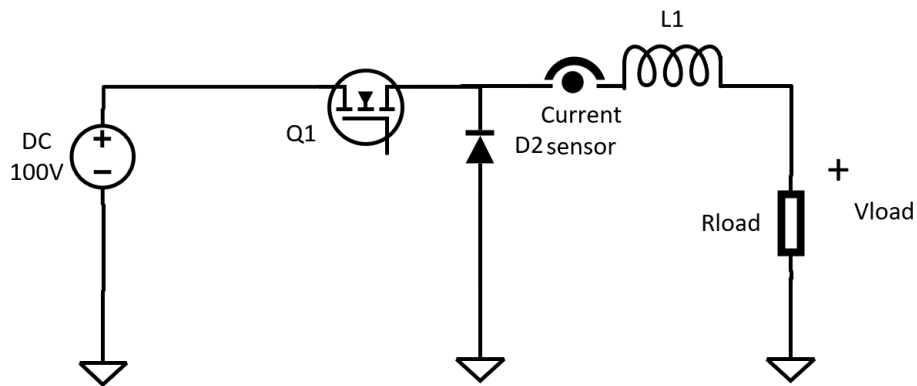


Figure 3-4: Current measurement circuit before the inductor

Measuring at this point, could be difficult due to the high voltage swings at the node. Although the measurement is differential in the shunt, the common voltage swing made the measurement noisy needing high amounts of common mode rejection ratio, proving non efficient.

Other way to measure it would be to measure the current in both the MOSFET and

the diode separately (Fig.3-5) and then reconstruct the information. In this case, two shunt resistors were used with separately signal conditioning. Current through the MOSFET will be tied to a fixed voltage, either ground for the current through the diode, or to the input bus voltage in the case of the MOSFET.

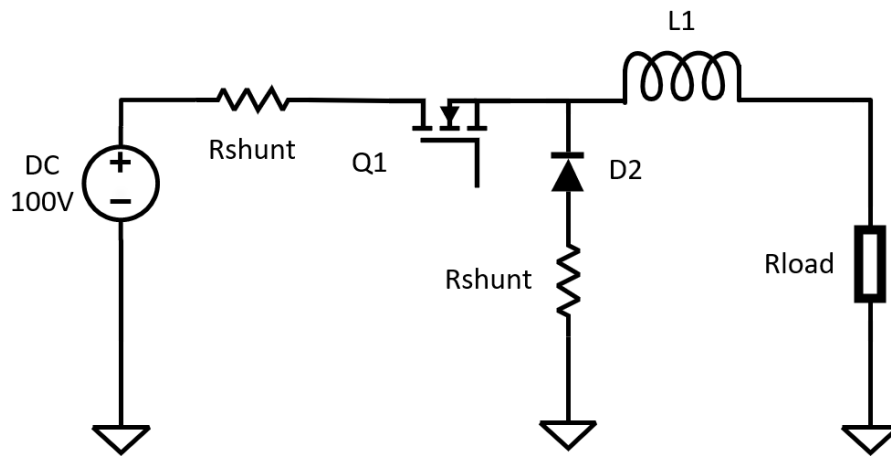


Figure 3-5: Split current measurement

From here, one option is to add both signals using an operational amplifier. This way we obtain the reconstructed current through the inductor. However as the sensors output switching is not instantaneous, the resultant waveform appears noisy, with peaks at the turn ON and turn OFF that may interfere with the current limits. This effect can be seen in Fig. 3-6-A, where the reconstructed signal has high peaks due to the difference in the rise time of the sensors, separated in 3-6-B.

The proposed method will decouple each measurement: current through the MOSFET will control the turn OFF, and current through the diode will control the turn ON. This also allows to use different gains depending on the sensors.

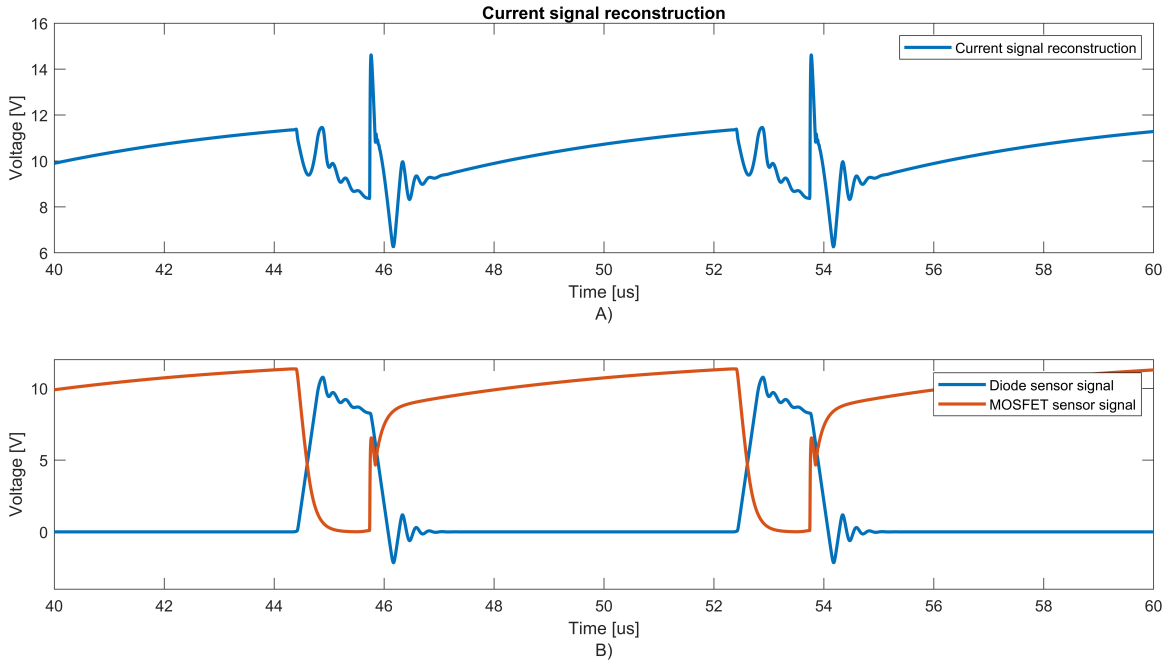


Figure 3-6: Current measurement and reconstruction

3.2.1 MOSFET current measurement

To measure the current through the MOSFET the proposed circuit is represented below. It will consist in a shunt resistor (R_{shunt}) of 20 m Ω , that will produce a voltage (V_{shunt}) proportional to the current through the MOSFET (I_{mos}) following:

$$V_{Shunt} = I_{mos} * R_{shunt} \quad (3.3)$$

In order to mitigate noise, the signal will be amplified by means of a current mirror, with the circuit of Fig.3-7. The current mirror exhibits simplicity in terms of its number of components, low noise and high accuracy. The principle of a current mirror is based on the fact that two identical transistors, when biased properly, will have nearly identical collector currents flowing through them.

In a simple current mirror circuit, a reference or input current is applied to the base of one transistor, known as the input transistor. The collector current of the input transistor flows through a load resistor and produces a voltage drop across it. The second transistor, known as the output transistor, is connected with the same biasing conditions as the input

transistor, and its collector current is forced to match the collector current of the input transistor.

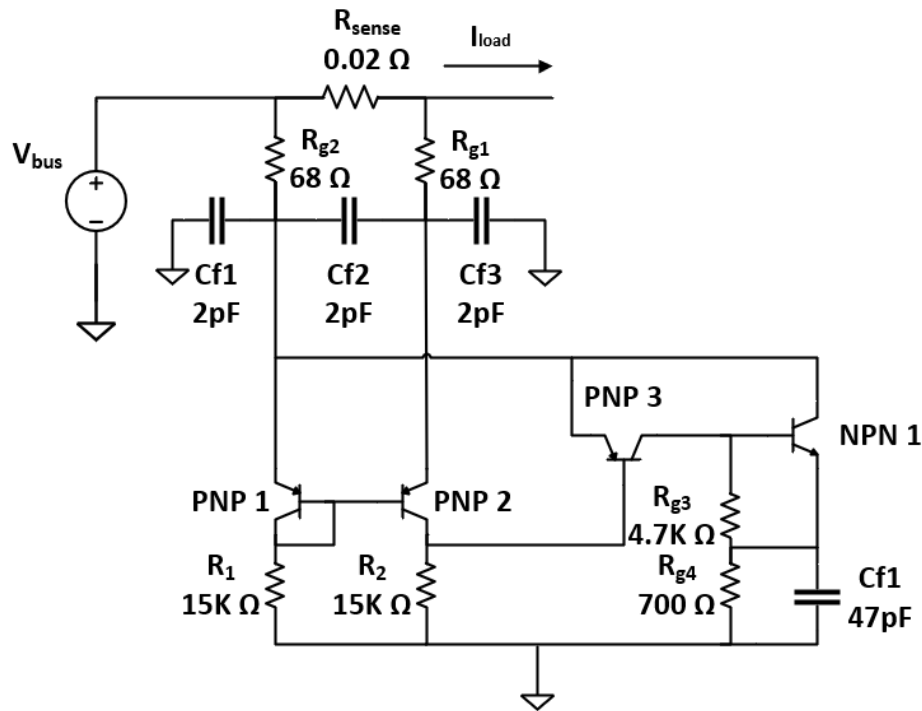


Figure 3-7: Current mirror for MOSFET current measurement

A more in depth analysis of the equations will be performed in appendix 5.1. The selected gain of the amplifier stage is 40, reaching 0.8 V per amp.

3.2.2 Diode current measurement

Diode measurement is simplified, as it is measured as a signal referenced to ground instead of a differential voltage as the MOSFET current measurement.

Current will flow from the ground and will produce a negative voltage (V_{shunt} diode), that will need amplification. To do so, a double stage amplifier was selected, allowing to split the gain between two amplifiers, achieving a higher bandwidth. The output of the conditioning stage will be fed to the comparison stage to compare with the current reference.

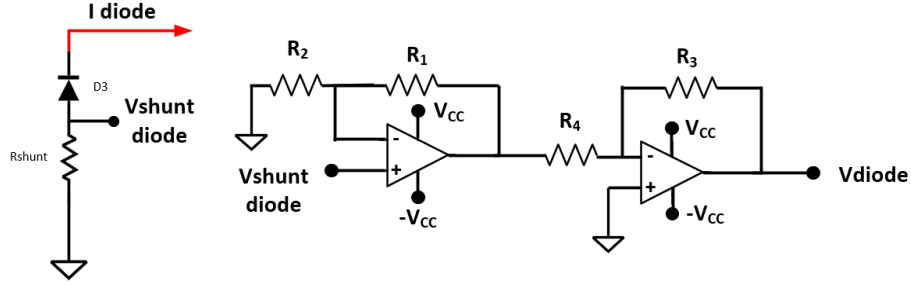


Figure 3-8: Diode signal conditioning

The selected gain was 40, split between two amplifiers with the same gain of 6.32. However, the first one will have a non-inverting topology to take advantage of the high input impedance of the amplifier, while the second one will invert the signal to be positive. Using normalized resistors, the gains and equations will follow Eq.3.4. The obtained signal V_{diode} , is the sensor output for the diode current, that will be compared with the reference.

$$\begin{aligned}
 G_{nonInverting} &= 1 + \frac{R_1}{R_2} = 6.32 \approx 1 + \frac{33K\Omega}{6.2K\Omega} \\
 G_{inverting} &= -\frac{R_3}{R_4} = 6.32 \approx -\frac{43K\Omega}{6.8K\Omega}
 \end{aligned}
 \tag{3.4}$$

3.3 Digital control logic

The LCL is implemented using non-programable digital logic, this is, no microcontroller or FPGA was used. Rather, the design has been implemented using discrete logic integrated circuits that have been approved within the context of space applications to ensure the reliability and robustness of the LCL.

3.3.1 Comparators and limit references

After the measurement of the sensor, these signals are connected to a LM339 high speed comparator [5]. These signals are compared with a set voltage references. The printed circuit board (PCB) is prepared for two case scenarios: with and without microcontroller supervision.

Considering a microcontroller, it provides an analog signal (filtered pulse width modulation (PWM)) to the input of the comparator, allowing to change the limits and with

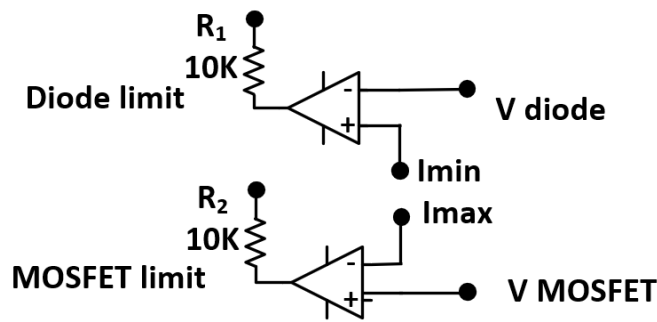


Figure 3-9: Comparators circuit

it, the current value allowing to reconfigure the current limits to the different devices or calibration. If no microcontroller is used for the control, the value can be fixed using a voltage divider or a potentiometer.

In Fig.3-9 it can be seen the two comparators and their input signals: I_{max} and I_{min} set the values for the current limits; V_{MOSFET} and V_{diode} are the signals coming from their respective sensors. In case the current through the MOSFET exceeds the I_{max} limit, the comparator output will be set to high, turning OFF the MOSFET. Current through the diode works in a similar way, we want it to be turned ON when the current is under the limit so, it is inverted at the inputs of the LM339. This was simulated and can be seen in Fig.3-10. In 3-10-A, when the MOSFET sensor reaches the current limit, the comparator activates its output briefly to reset the MOSFET.

In the case of the current through the diode, it has to be active when it is below the current limit, so it turns ON the MOSFET again. However, as the measurements are decoupled, while the MOSFET is ON, the current through the diode is zero, below the limit, activating the MOSFET without need. This can be seen in Fig.3-10-B, where the output is high when the values are below the reference, and goes to zero when its above.

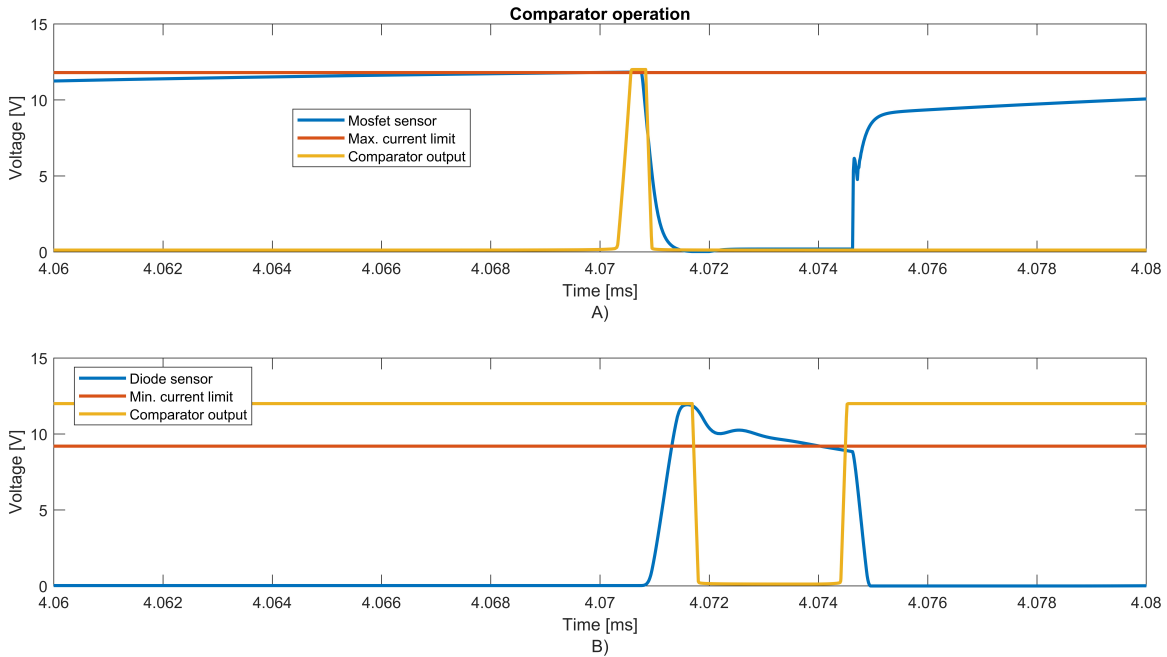


Figure 3-10: Comparator testing

As the LM339 has 4 comparators in a single package, the other two comparators can be used for the trip-off and under-voltage comparator. One advantage of this design is that all the references and limits are translated to a voltage in the comparator, allowing to easily change the references.

3.3.2 J-K Flip-Flop

The solution to the previous issue is based on a J-K flip-flop, as the CD4027BC. This device has two types of inputs: Asynchronous (Set, Reset), Synchronous (J, K) and a clock signal (clk). Set and reset will change the output independently of the clock and J-K pins. However, when there is a rising clock pulse, the output value will change depending on the values set on the J and K pins.

Going back to the signals of the comparators we want:

- Output = 0 when the current through the MOSFET is higher than the limit.
- Output = 0 when tripoff protection is triggered
- Output = 1 when the current through the diode just crossed the lower current limit.

- Output = 1 when forced from an external device (Forced start)
- Output = 0 when forced from an external device (Forced reset)

This can be easily matched with the behaviour of the J-K flipflop, with the circuit represented in Fig. 3-11

- MOSFET limit comparator →RESET
- Tripoff →RESET
- Reset →RESET
- Force start →SET
- Diode limit comparator →CLK. With J connected to VCC and K connected to ground.

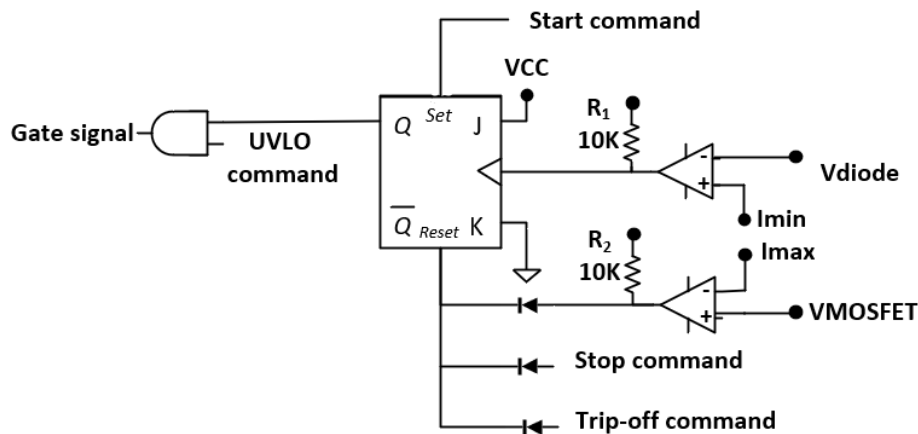


Figure 3-11: Digital signals circuit

3.3.3 AND Gate

Flip-Flop output and under voltage lockout (UVLO) signals will then be connected to an AND gate, as we do not want all the payloads of the system to be reseted when bus voltage is under the limit. Only temporarily stop the modulation and, if the over-current is still present in the faulty node after the trippoff time, disconnect it without affecting the rest of the payloads.

3.3.4 Isolation stage

Finally, the switching command to the gate driver needs to change references in order to isolate the digital signal. The selected circuitry uses an optocoupler, the TLP700. It will produce an optical isolation barrier, and could be used as a gate driver directly, however, for reasons state in section 3.6, it will work only as a digital isolator .

Acording to the datasheet [11], the recommended current is 7.5 to 10 mA, with a forward voltage in the diode of 1.57 to 1.75V. To protect the diode, a protection resistor was used. To calculate this value, equations 3.5 were used, obtainig a standard resistor value of 1.2K

$$\begin{aligned} i_{f_{max}} &= \frac{V_{in} - V_{f_{min}}}{R_{opto}} \\ i_{f_{min}} &= \frac{V_{in} - V_{f_{max}}}{R_{opto}} \end{aligned} \quad (3.5)$$

3.4 Power stage

To power the circuit, three auxiliary voltages are needed: 12V, -12V and 15V. The first 12 and -12 can be obtained from a single integrated DC-DC converter as they are both referenced to the common ground. The third voltage +15V will be used to turn ON the gate of the MOSFET, and needs to be referenced to the source pin of the MOSFET, in order to produce a positive VGS voltage.

3.5 MOSFET selection

The requested limiter device by the ESA for this project is a silicon carbide (SiC) N-channel MOSFET. Among their advantages, the reduced R_{ds} , allowing for more efficient operation when the LCL is not switching; higher temperature operation, critical for space operation where there is no convection cooling and managed powers are high; Higher switching speeds, as in this application there is not a defined frequency, the parameters that will control the switching frequency are the remaining load voltage during failure and the transmission delays in the circuit. Operating at higher frequencies, will allow to use a smaller inductance, reducing weight and volume.

The required MOSFET must be able to withstand, at least, voltages 1.4 time above the nominal voltage and currents 2 times above the nominal current. The proposed MOSFET by the ESA is the NTHL045N065SC1, a SiC MOSFET with a maximum drain-source voltage (Vds) of 650V and a current capability of 66A. However, due to supply chain issues, an equivalent non SiC MOSFET was used.

3.6 Gate driving

To switch the MOSFET, the gate driver EL7202C [9] is used. To limit the current provided by the driver, a 3 Ω gate resistor. To turn ON the MOSFET, the applied voltage must be positive and higher than the threshold voltage (Vth) with respect to the source pin. During the design of the the gate driving circuit, two parameters need to be taken into account: MOSFET driving levels and gate capacitance.

SiC MOSFETs often need higher voltage levels than traditional silicon MOSFETs, requiring special circuitry. The designed gate driver will be fed from a 2W DC-DC converter providing +15V.

It is also needed to pay special attention to the MOSFET gate charge. Power losses in a gate driver follow Eq.3.6. This value depends on the switching frequency and the gate charge, and as the value of the gate resistance (Rgate) is small, we can assume that most of the power losses are in the driver [1]. As we are operating with variable switching frequency, it must be ensured that the power dissipated by the driver does not exceed its limits.

$$\begin{aligned}
 P_{drv_{on}} &= \frac{1}{2} x \frac{R_{Hi} V_{DRV} Q_G f_{DRV}}{R_{Hi} + R_{Gate} + R_{G,I}} \\
 P_{drv_{off}} &= \frac{1}{2} x \frac{R_{Lo} V_{DRV} Q_G f_{DRV}}{R_{Lo} + R_{Gate} + R_{G,I}} \\
 P_{drv} &= P_{drv_{on}} + P_{drv_{off}}
 \end{aligned} \tag{3.6}$$

In equation 3.6, RHi and RLow are the resistances of the driver Ic, Qg is gate capacitance, Vdrv is the gate driver voltage and Rgate is the external gate resistor, and RG,I is the gate mesh resistance.

With a maximum power dissipation of 1.05W using the MOSFET parameters and a gate

resistance of 3Ω , the maximum allowed switching frequency is above 1 MHz, well beyond the range of the circuit.

3.7 Inductor selection

Inductor design is a critical step in every power electronics application, even more if it is for space application. Adding to the already complex task of designing an inductor, this device should work with a variable frequency, and have extremely low DC resistance (R_s). Typically, power losses in an inductor follow the graph in Fig.3-12. Core losses decrease with the number of turns, while the copper losses increase with the number of turns. For a switching application, the goal is to minimize the total power losses, working at point 1. However the switched LCL will work most of its time as a close circuit, this is, not switching, as core losses are dependant on the switching current, this are neglected and the design goal should be based on the reduction of the number of turns as much as possible. This is not always possible as there is a minimum amount of turns needed to avoid saturation of the core.

The optimal design for the LCL is the minimum amount of turns that ensures that no saturation is going to happen (point 2). A more in depth analysis is performed in Appendix 5.2.

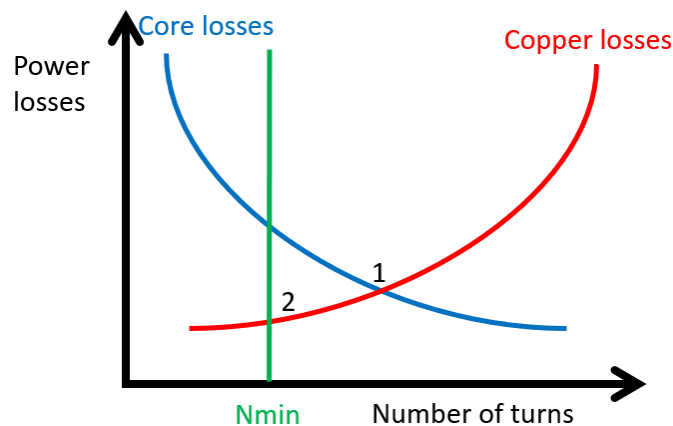


Figure 3-12: Simplified inductor power losses in terms of the number of turns

3.8 Under-voltage lockout stage

To ensure that critical components power of the satellite are prioritize when there is a payload failure, an under voltage lockout detector is implemented. In case the voltage of the bus decreases from the nominal value, all the non vital payloads are disconnected, returning the voltage to a safe level.

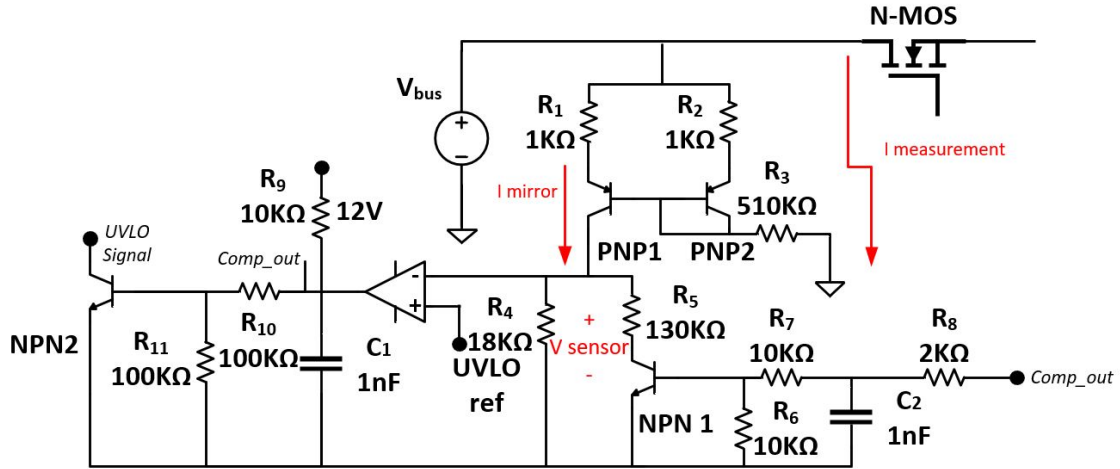


Figure 3-13: Under-voltage lockout circuit

To measure the bus voltage, the current mirror in Fig.3-13 is used. The voltage at the bus will be transformed into a current, $I_{\text{measurement}}$, following Eq.3.7, where V_{bus} is the bus voltage, and V_{ce} is the transistor (PNP2) voltage drop between collector and emitter. This value will be matched by the other transistor (PNP1) in the mirror (I_{mirror}).

$$I_{\text{measurement}} = \frac{V_{\text{bus}} - V_{\text{ce}}}{R_2 + R_3} \quad (3.7)$$

$$I_{\text{mirror}} = I_{\text{measurement}}$$

This current I_{mirror} , flowing through a resistor will produce a voltage, V_{sensor} . There are two options depending on the state of the UVLO: While the UVLO has not been triggered, all the current will flow through R_4 , producing a voltage proportional to its resistance. If the UVLO was triggered, the NPN1 transistor will start conducting, so the effective resistance seen by that current is going to be the parallel of this two resistances. Both equations can be seen in Eq. 3.8

$$\begin{aligned} V_{sensor} &= I_{mirror} * R_4 \rightarrow \text{HysteresisOFF} \\ V_{sensor} &= I_{mirror} * \frac{R_5 R_4}{R_5 + R_4} \rightarrow \text{HysteresisON} \end{aligned} \tag{3.8}$$

Chapter 4

Final results

4.1 Simulations

To test the operation of the device after the design process, it was tested in LTSpice, however this simulations do not take into account the effect of noise, that will be discussed later on. Although the simulations were performed in LTSpice, they were represented in Matlab.

4.1.1 Sensors

MOSFET current sensor

In Fig.4-1 it is shown the results of the designed sensor, (note that the gain have been adjusted to match the current trace) following the charge of an inductor after a voltage step, simulating the operation of the sensor in the final application. The voltage signal follows the desired signal, with an small offset of 50mV with respect to the expected results due to transistor unidealities.

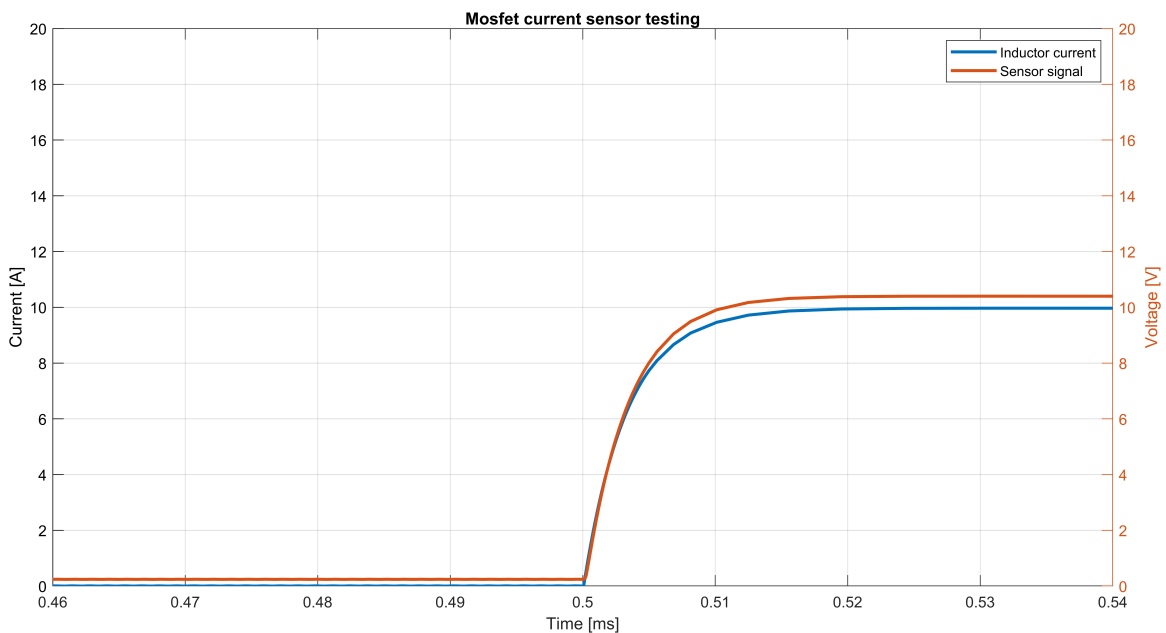


Figure 4-1: MOSFET current sensor testing

Diode current sensor

As stated previously, the measurement through the diode was performed using two cascade amplifiers, to achieve a gain of 40 (0.8V/A) with high bandwidth. To test the performance of this sensor, the discharge of the inductor through a resistor was simulated. In Fig.4-2 it can be seen the results of the simulation, (note that the gain have been adjusted to match the current trace), although the gain matches perfectly, the signal has some resonance from the commutation.

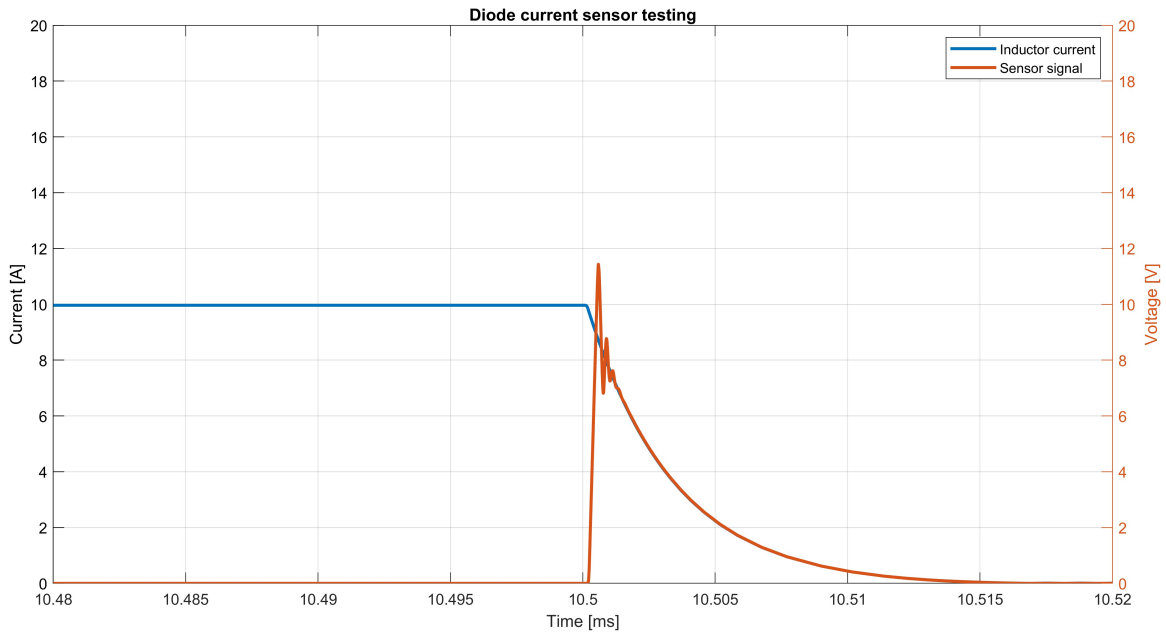


Figure 4-2: Diode current sensor testing

4.1.2 Digital circuitry

First, the comparators input and outputs are shown in Fig.4-3. In Fig.4-3-A when the current through the MOSFET is above the limit, it turns ON its output. In the diode current sensor, Fig.4-3-B, the output is always ON unless it is under the current limit, and generates a rising edge when it crosses the limit downwards. According to the digital implementation, the comparators are directly fed to the J-K flipflop. In Fig.4-4-A, it can be seen in blue the inductor current waveform and the current limits, as well as the flip-flop output. In Fig.4-4-B, the comparator limits are shown, where the blue line is the maximum current comparator; orange is the minimum current comparator and yellow is the output of the flip-flop. This is, when the current in the inductor(sensor signal) is above the limit, the I_{max} comparator will generate a high signal, and, when the current goes under the limit, it will produce a rising edge, making the JK flipflop generate a logic 1 on its output.

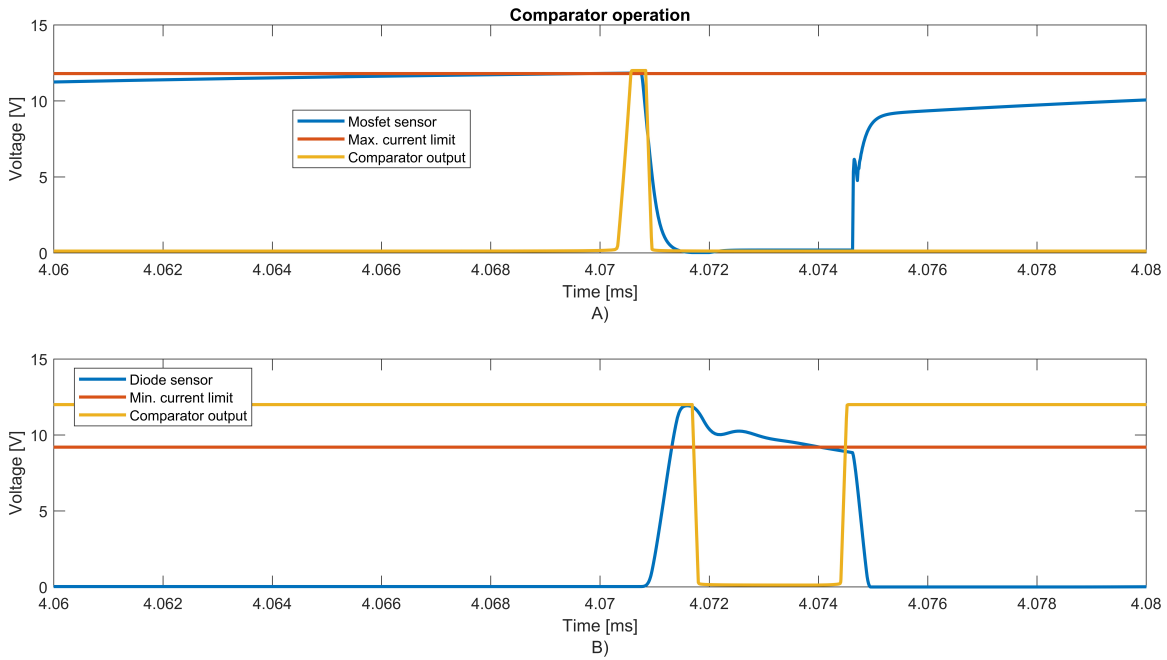


Figure 4-3: Comparator simulation

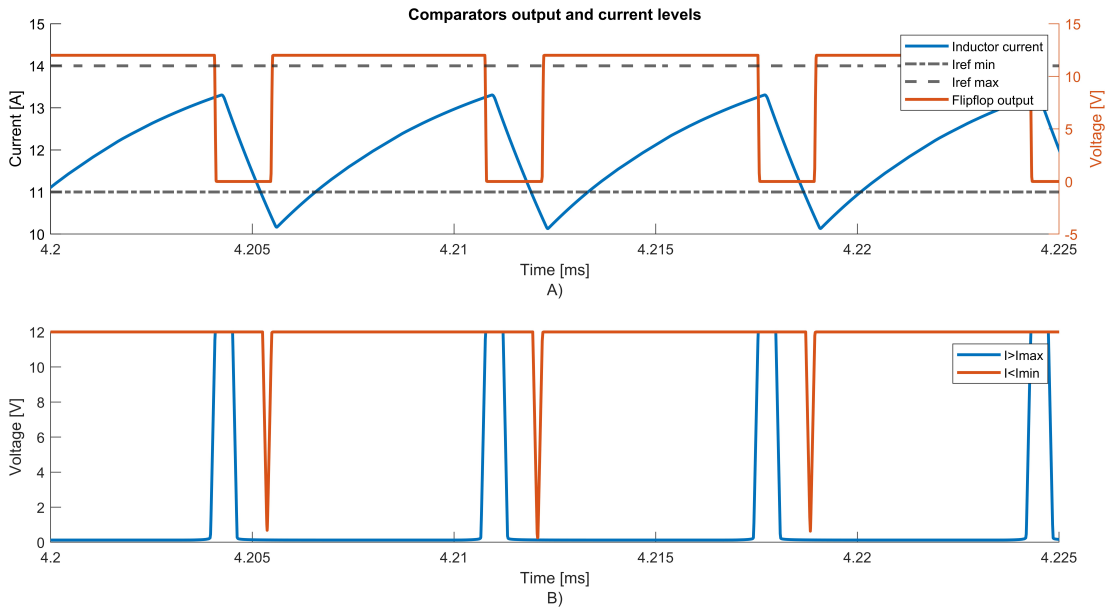


Figure 4-4: Flip-flop inputs, outputs and current levels

4.1.3 Under-voltage lockout section

To test the operation of the under-voltage protection, a triangular wave is used to simulate a variation on the bus voltage. This value will be measured by a current mirror and then compared with a voltage reference. In the case that the voltage is below this reference, the sensor will generate a zero voltage level. Then, when the voltage rises above the limit considering the hysteresis value, the output will return to normal values. This can be seen in Fig.4-5-A, the bus voltage is varying from nominal to 60V, once it crosses the 80V limit, the output of the UVLO goes to zero and does not return until it surpasses the limit +10V of the reference

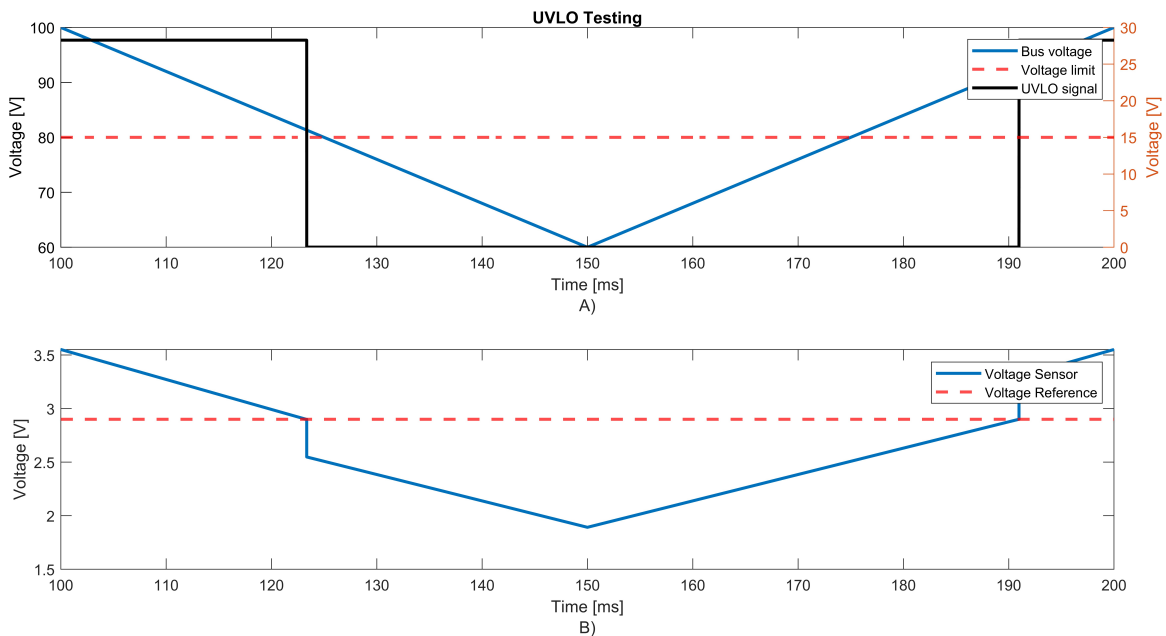


Figure 4-5: UVLO testing under varying bus voltage

4.1.4 Current regulation

In Fig.4-6 it can be seen the general working principle of the circuit. At $t=2\text{ms}$, the start command is applied and current starts flowing through the inductor, consuming 5 A. At $t=4\text{ms}$, a short circuit is produced, and the LCL starts the switching current limiting process, after 4 seconds, the fault is cleared and the device returns to normal values.

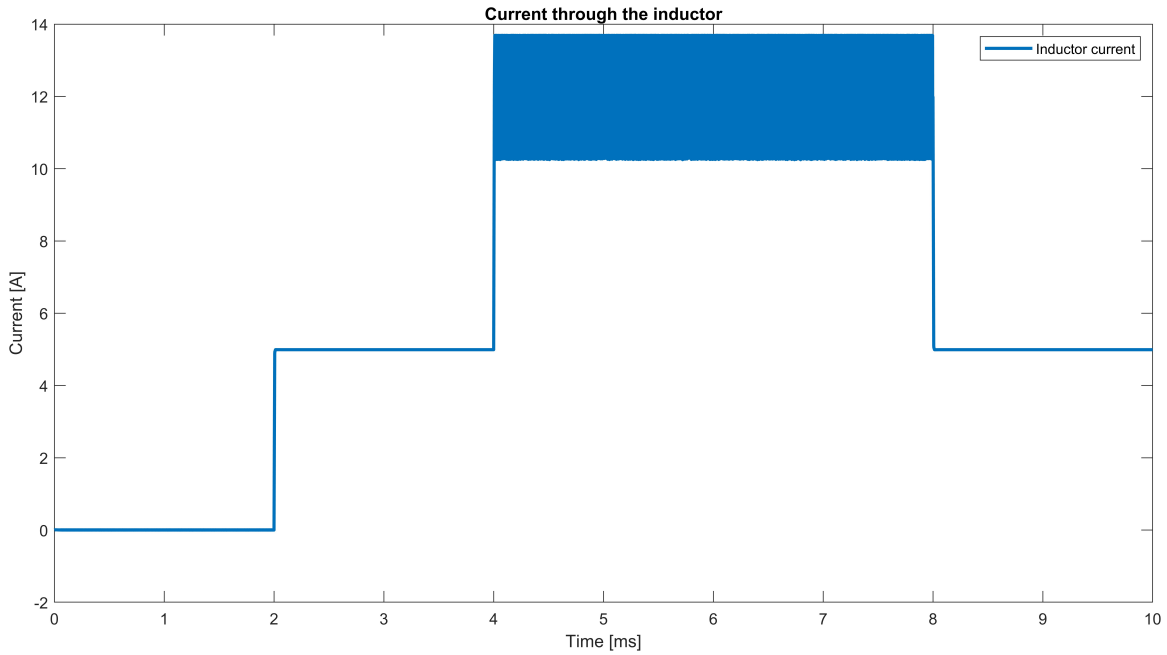


Figure 4-6: Switched mode LCL current profile

In Fig.4-7 it can be seen in detail the switching process. Seeing how the current through the MOSFET and diode reconstruct the current through the inductor.

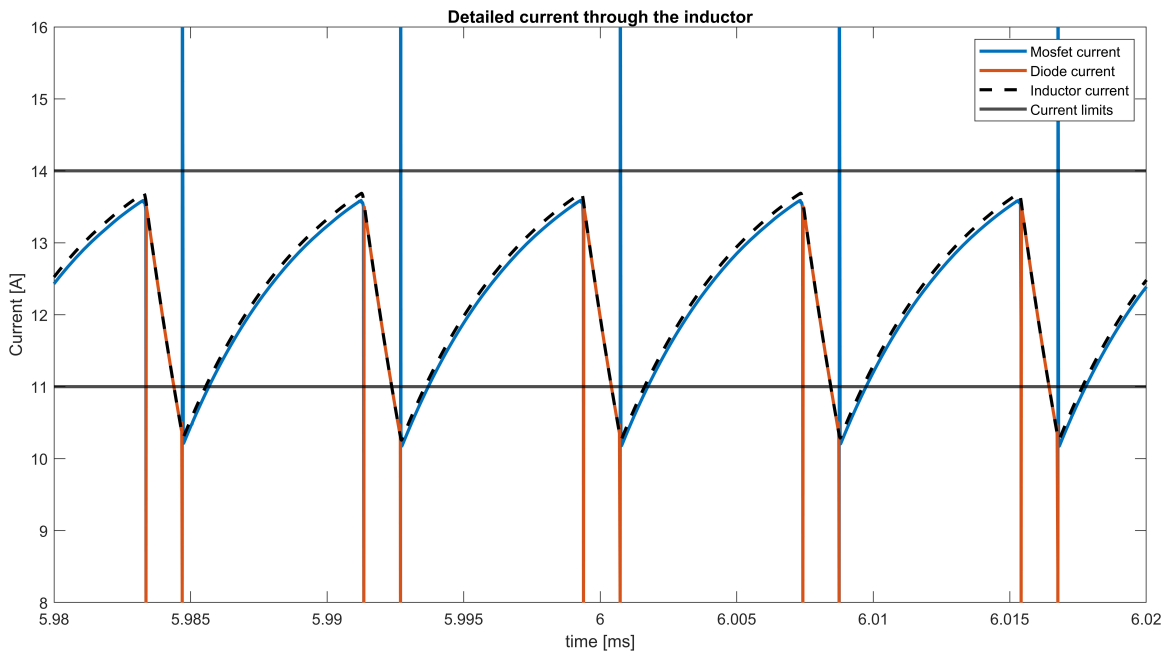


Figure 4-7: Switched mode LCL current waveforms

However, it is clear that the device is not reaching the upper band but is surpassing the bottom limits, reaching a peak of 13.7 A and 10.2 A, in contrast with the 14 A and 11 A of the bands. There are two reasons for this, and they can be seen in Fig.4-8. Due to the offset in the MOSFET current sensor, it switches OFF before the actual current reaches 14A. In the case of the lower band, it is due to the addition of the delays in the sensor and digital logic.

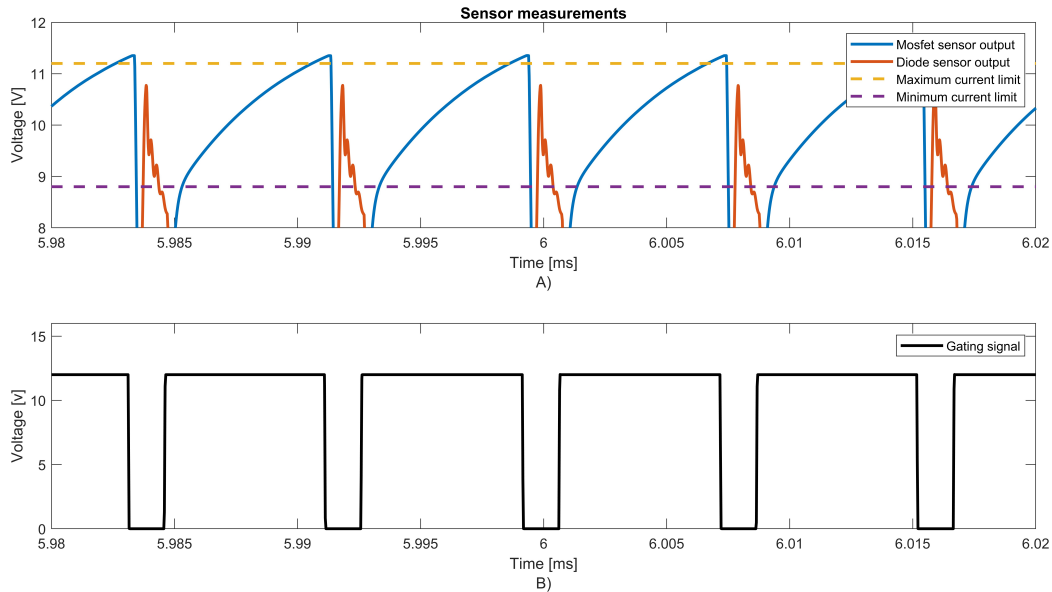


Figure 4-8: Sensor measurement

This overshoot could be solved by using faster electronics or using higher values of inductances, limiting the di/dt .

4.2 Experimental results

4.2.1 PCB design

To test the system, a prototype PCB was built in Kicad. The goal was to design the hole system in a two layer board, taking special care to the routing between analog and digital signals. To do so, an area for digital signals was designed far from the analog signals. This will help to reduce the crosstalk between high speed traces.

In Fig.4-9 it can be seen the backside of the PCB, with each of the differentiated parts.

The total footprint is 78x65mm, however, this design has not been optimized for volume yet. At the bottom of the PCB it can be seen the voltage dividers that produce the voltage reference for the current limits and UVLO. Going up the, digital section and fast rising signals are grouped and finally, at the borders, away from the digital electronics, the sensors are placed.

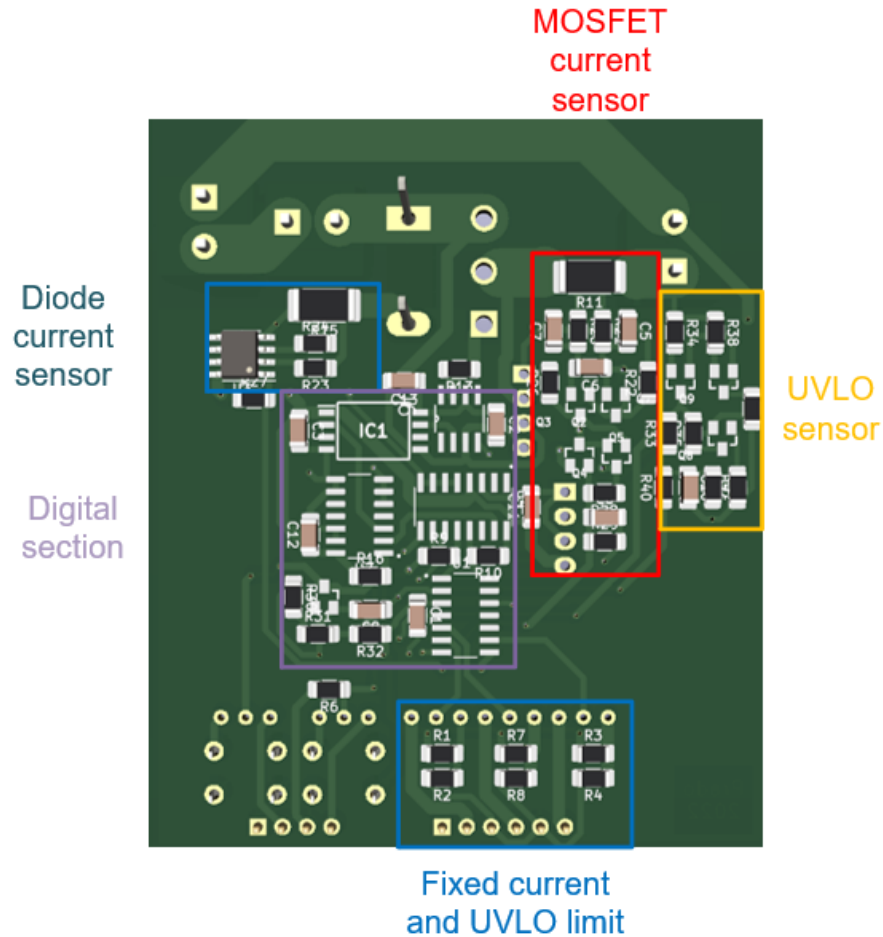


Figure 4-9: PCB BOTTOM side

Fig.4-10 shows the front side of the PCB. To easily change inductors and loads, it was populated with connectors instead of soldering the leads directly. At the bottom, it can be seen the pins to connect the microcontroller and the selectors to switch between microcontroller and manual setup. Finally, the buttons to manually test the operation of the limiter device.

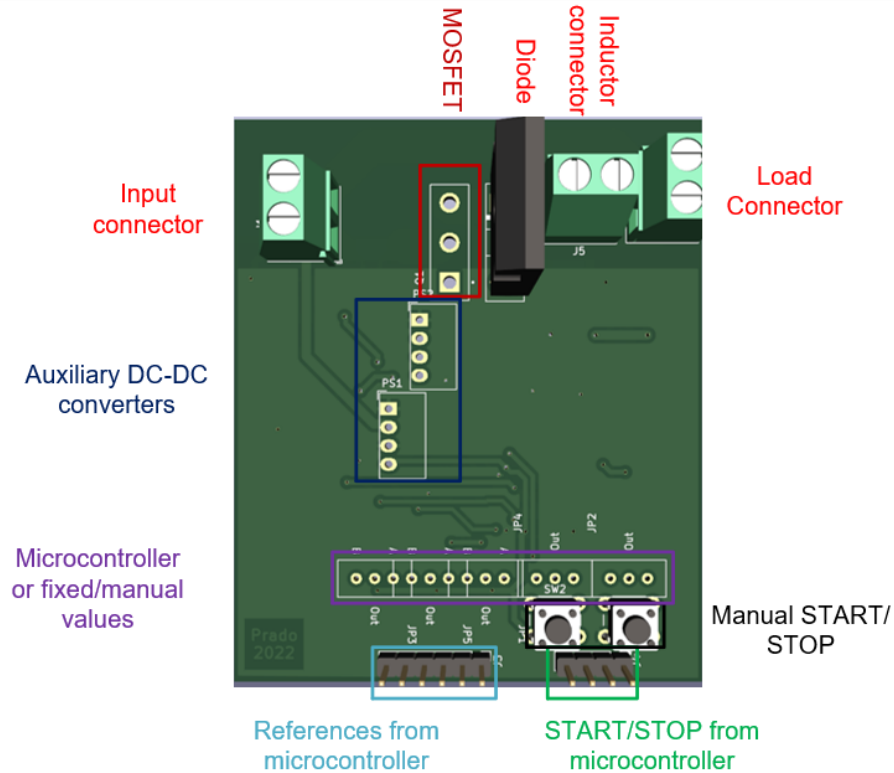


Figure 4-10: PCB TOP side

4.2.2 Current regulation

To test the regulation capabilities of the device, it was connected to a resistive load, and operating a switch, the overcurrent was simulated. In Fig.4-11 it can be seen the device working at lower currents, in yellow the current waveform, in red the upper limit and in blue the lower limit, matching the expected waveform and regulating between the set limits. However, the delay between the current passing through the limits and the switching of the semiconductor is about 4 μ s, almost twice than in simulation, mainly from the optocoupler, that was not modeled in LTSpice. It can also be seen noise in the current waveform at the turn-OFF of the device, leading to false switch.

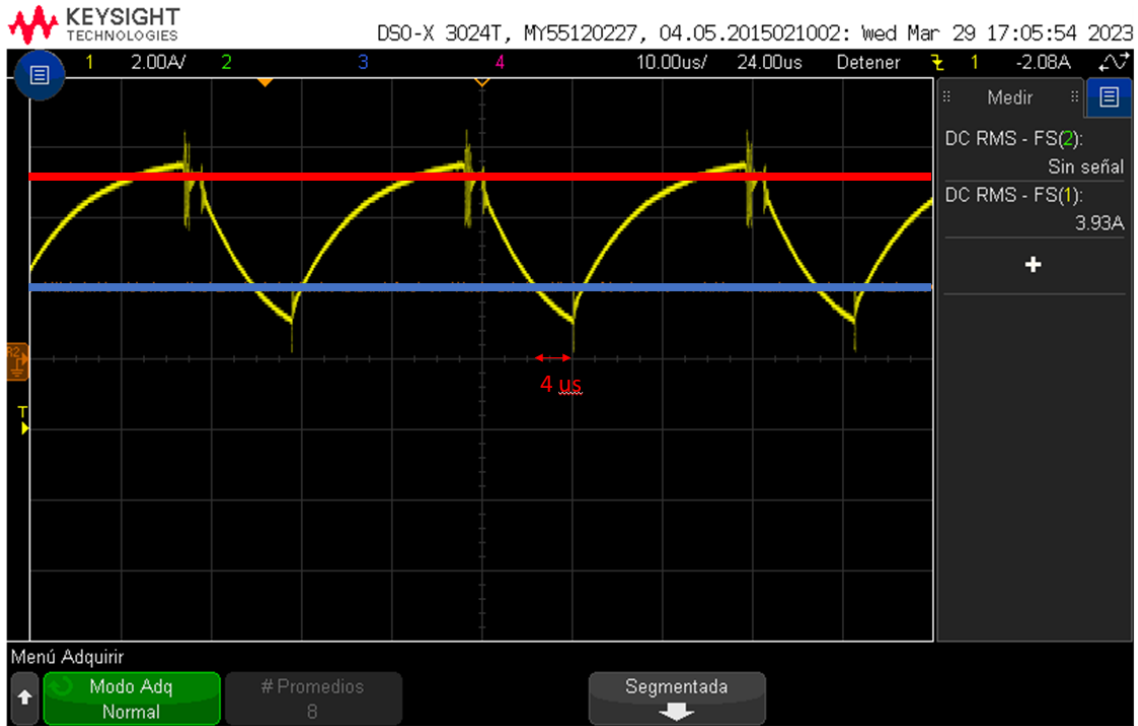


Figure 4-11: Regulated current waveform

4.2.3 Sensors

The response of the MOSFET and diode sensors were tested and are shown in Fig.4-12 and 4-13 respectively. It can be seen that the MOSFET current sensor (green trace), follows the current waveform in yellow (gains have been adjusted to match both waveforms). However, it is clear that at the switching point, ripple appears on the output of the sensor, due to the common mode electro-magnetic noise. The same happens when the diode is conducting current in 4-13, although the sensor follows the waveform of the signal, the common mode noise is affecting the general waveform.

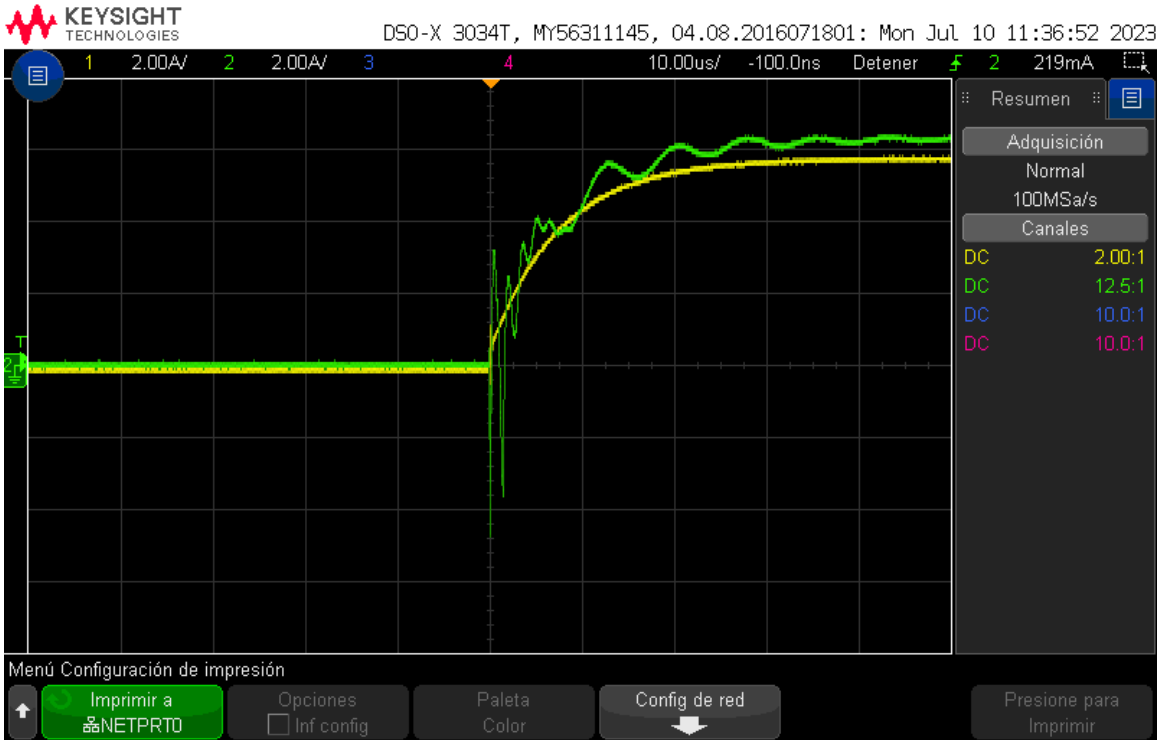


Figure 4-12: MOSFET sensor output

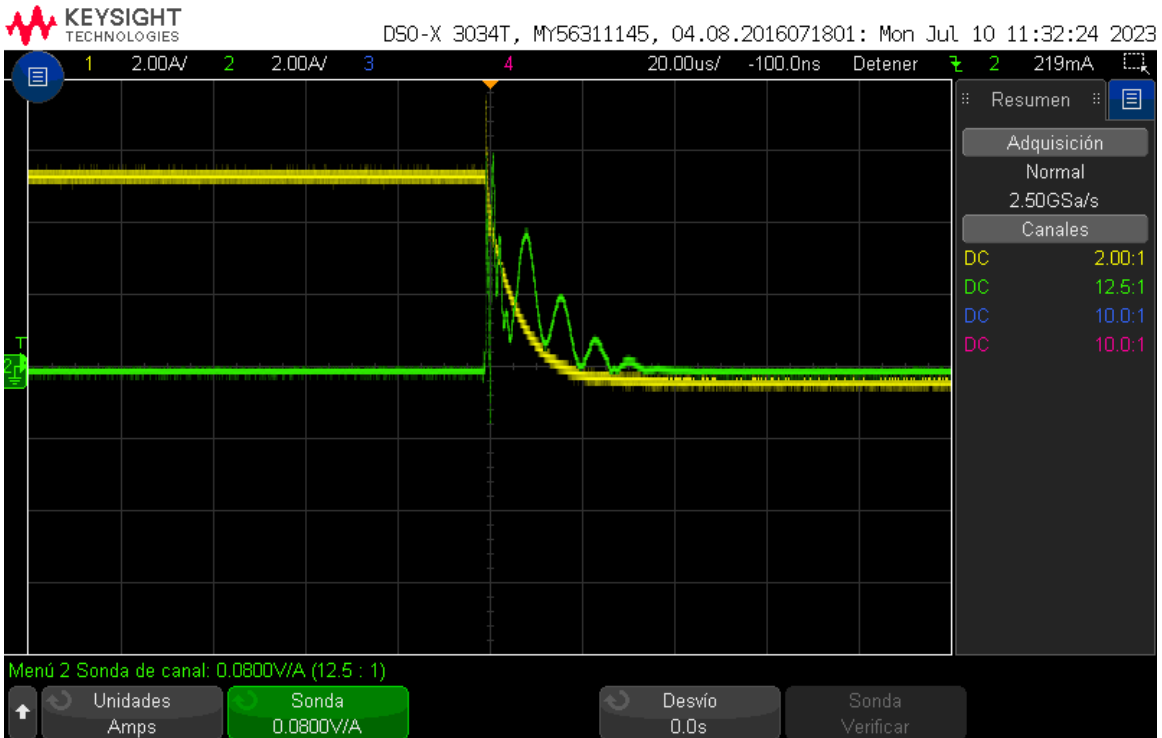


Figure 4-13: Diode sensor output

4.2.4 Digital signals

This noise is prominent in the digital signals shown in 4-14. The yellow trace corresponds to the current reference, green to the current and blue the comparator output. It can be seen how at the switching moment, the same noise affects to all three signals. From this graph we can also measure the delay from this comparator, measuring at around 800ns.



Figure 4-14: MOSFET comparator circuit results

This can also be seen in the diode comparator circuit 4-15, where the blue trace is the reference, green is the measurements and pink is the comparator output. However this time the delay is around 2.1us, much more than expected, reducing the operation frequency. The effect of this extra delay can also be seen in Figs.4-17 and 4-16 where the turn-OFF regulation is worse than the turn on due to this delay, having a bigger overshoot.

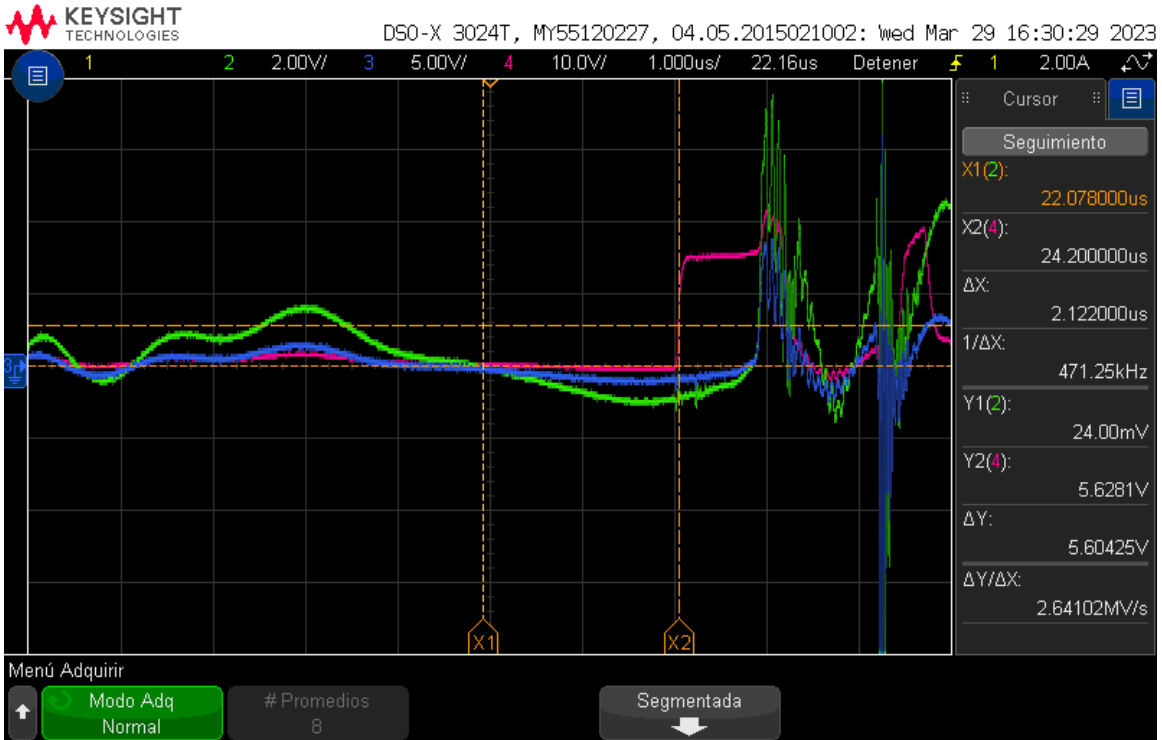


Figure 4-15: Diode comparator circuit results

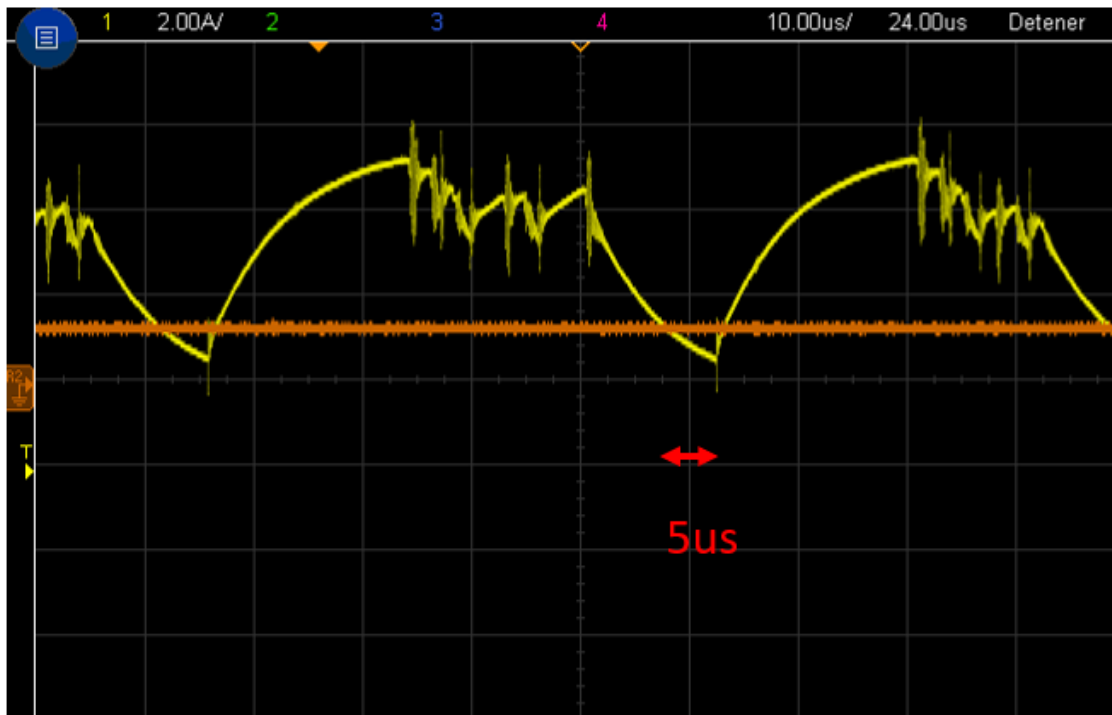


Figure 4-16: Turn OFF delay

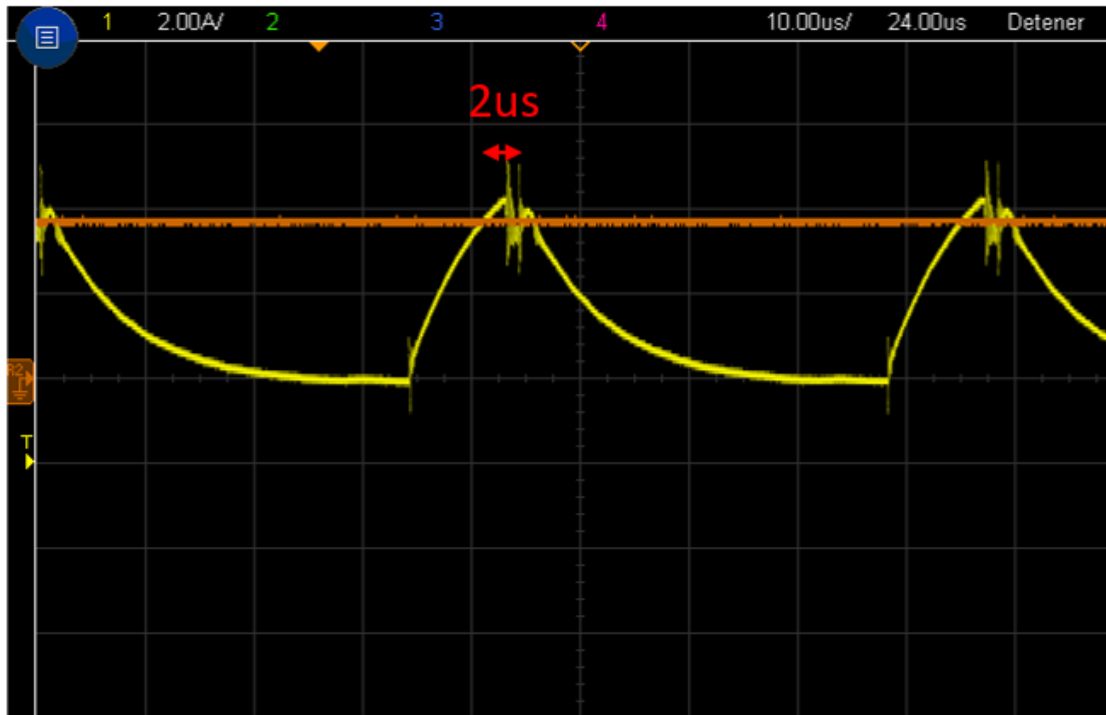


Figure 4-17: Turn ON delay

4.2.5 Noise

The same setup was tested at nominal conditions, 10 A nominal 100 V. However, as the noise scales with voltage and current, it overpowered the signal coming from the sensors. This produced two types of outcomes:

In the first one, once the overshoot is produced, the upper limit is reached and the MOSFET is turned OFF. Then the current decreases below the lower limit, and the MOSFET turns ON, the noise produced by the conmutation will produce an instantaneous reset, disabling the device and reaching 0A.

In the second outcome, the device starts switching, but due to the noise, the current limits are not met. In this case, the current limits will depend on the delays in the signal path and the remaining load voltage and in a smaller extend, the current limits, loosing current control capabilities.

4.3 Conclusions

The main objective of this work was the development of a switched latching current limiter (LCL) for space applications. This new topology would allow to replace P-channel and N-channel MOSFETS used in their linear region. Working as a switched device would allow to reduce the total power losses in the device and paired with SiC MOSFETS increase the robustness of the limiter.

Multiple topologies were discussed focusing in the instrumentation and control of the device, supported by simulation and prototypes. From building and testing the prototype, some conclusions can be drawn about the design:

- As the MOSFET is only supporting the full bus voltage during short periods of time, the MOSFET rating selection process can be optimized, facing the traditional LCL topologies based on the limiters devices working in active region.
- If the measurements are referenced to the ground, the common mode voltage is very limiting, needing complex solutions as the one presented in this work.
- The differential delay between measurement circuits is critical to obtain a clean signal, making the split measurement system proposed here a good solution.
- To obtain high frequency switching, special care should be taken in the PCB design to minimize noise.
- As seen in the implementation results, the effect of the noise makes the prototype not function properly. One proposed future work that might work is the floating measurement, with the circuitry referenced to the switching node.

Chapter 5

Appendix A

5.1 Current mirror

In this section, the equations for the current mirror are presented.

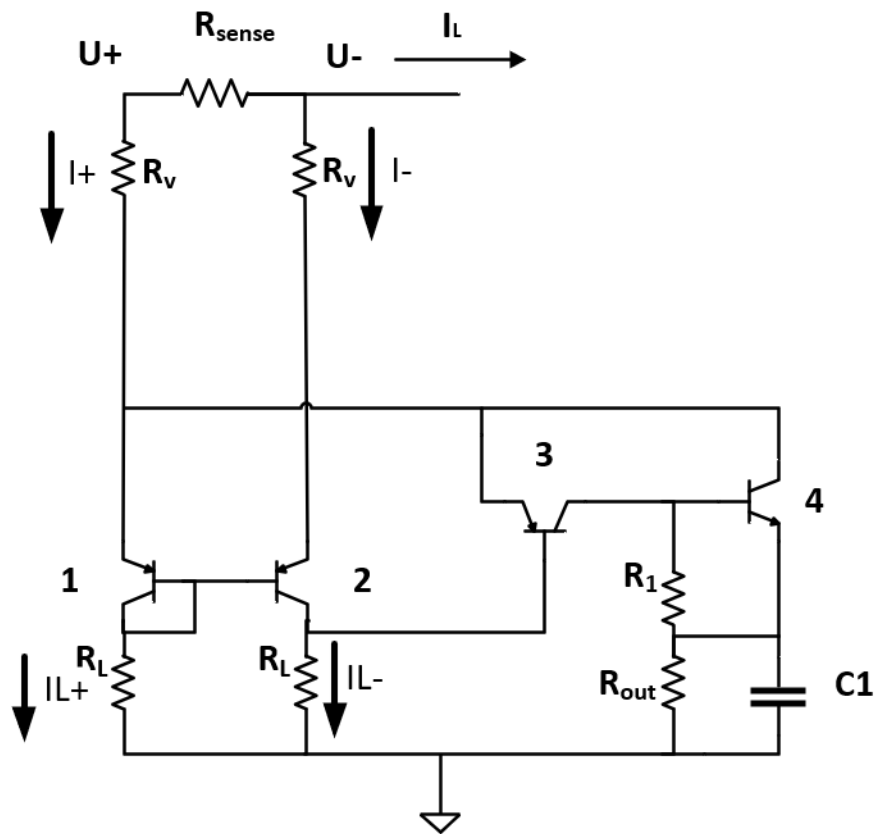


Figure 5-1: Current mirror for MOSFET current measurement

Following Fig.5-1, first assumption is that transistors 1 and 2 are matched so:

$$\begin{aligned} U_{B1} &= U_{B2} = U_B \\ U_{E1} &= U_{E2} = U_E \end{aligned} \quad (5.1)$$

Then, the current flowing through each transistor will be:

$$\begin{aligned} I_+ &= \frac{U_+ - U_e}{R_v} \\ I_- &= \frac{U_- - U_e}{R_v} \end{aligned} \quad (5.2)$$

Analyzing for transistor 1 and 2:

$$\begin{aligned} \left. \begin{aligned} I_+ &= I_{E3} + I_{E1} \\ I_- &= I_{E2} \end{aligned} \right\} = I_+ - I_- = \frac{U_+ - U_-}{R_v} - \frac{U_- - U_E}{R_v} = I_{E1} + I_{E3} - I_{E2} \\ U_+ - U_- &= R_v * (I_{E1} + I_{E3} - I_{E2}) \end{aligned} \quad (5.3)$$

Analyzing the transistor themselves:

$$\left. \begin{aligned} I_{E1} &= I_{C1} + I_{B1} \\ I_{E2} &= I_{C2} + I_{B2} \end{aligned} \right\} = I_{E1} - I_{E2} = I_{E1} - I_{E2} = I_{C1} + I_{B1} - I_{C2} - I_{B2} \quad (5.4)$$

For the lower resistances:

$$I_{L+} = \frac{U_B}{R_L} = \frac{U_{E1} - U_{knee}}{R_L} = I_{C1} + I_{B1} + I_{B2} \quad (5.5)$$

$$I_{L-} = \frac{U_{E1} - U_{knee}}{R_L} = I_{C2} + I_{B3} \quad (5.6)$$

Now assuming that Q1=Q3:

$$I_{L+} = I_{L-} \quad (5.7)$$

$$R_v(I_{C1} + I_{B1} + I_{C3} + I_{B3} - I_{C2} - I_{B2}) = R_v(I_{L+} - I_B - I_{L-} - I_{C3} - I_{B2}) \quad (5.8)$$

$$\Delta U = U_+ - U_- = R_V(I_{C1} + I_{B1} - I_{C2} - I_{B2} + I_{E3}) \quad (5.9)$$

$$\Delta U = R_V(I_{E3} - 2I_{B2} + I_{B3}) \quad (5.10)$$

$$\Delta U = R_V(I_{C3} + 2I_{B3} - 2I_{B2}) \quad (5.11)$$

If every transistor is in active zone:

$$\Delta U = R_V(I_{C3}) \longrightarrow I_L * R_{sense} = R_V \frac{V_{out}}{R_{out}} \quad (5.12)$$

Finally

$$V_{out} = \frac{R_{sense} R_{out}}{R_V} I_L \quad (5.13)$$

5.2 Inductor calculations

To calculate the inductor value L it is needed to know the load seen by the limiter device, $R_{failure}$ following:

$$R_{failure} = \frac{R_L R_{sc}}{R_L + R_{sc}} \quad (5.14)$$

To ensure that the device starts switching we need to define a maximum resistance to ensure that higher limit is reached, so:

$$R_{critical} = \frac{V_{bus}}{I_{max}} = \frac{V_{bus}}{1.4V_{nom}} \quad (5.15)$$

If the $R_{failure}$ is greater than the critical one, the device will not switch, stressing more the semiconductor. Therefore, the goal is to discover a formula that connects the switching frequency (Fsw) to the failure resistance value. By doing so, it would be feasible to determine a minimum inductance value (L) for the buck converter.

To derive an expression linking the value of Fsw to $R_{Failure}$, we can analyze the functioning of the N-MOS device in the buck converter. When the N-MOS turns ON during the switching process, the voltage applied to the inductor (VL) follows the expression described in 5.16. This allows us to determine the duration of the coil magnetization (tON)

described in 5.17

$$V_L = V_{in} - V_o = L \frac{di(t)}{dt} \quad (5.16)$$

$$t_{on} = \frac{L\Delta i}{V_{in} - V_o} = \frac{L\Delta i}{V_{in} - R_{failure}I_{avg}} \quad (5.17)$$

Where V_{in} is the value of V_{bus} , V_o is the output voltage of the LCL, I_{avg} is the average current value through $R_{failure}$, and Δi is the current increment between I_{max} and I_{min} . The same can be applied to the turn OFF in Eq. 5.18 and 5.19

$$V_L = -V_o = L \frac{di(t)}{dt} \quad (5.18)$$

$$t_{off} = \frac{-L\Delta i}{V_o} = \frac{-L\Delta i}{R_{failure}I_{avg}} \quad (5.19)$$

Now, an expression of the T_{sw} as a function of $R_{failure}$ can be written:

$$T_{sw} = T_{on} + T_{off} = \frac{L\Delta i}{V_{in} - (R_{failure}I_{avg})} + \frac{L\Delta i}{R_{failure}I_{avg}} \quad (5.20)$$

In order to determine the minimum value of the parameter $R_{failure}$ 5.21, we can take the derivative of expression (7) with respect to $R_{failure}$ and set it equal to zero. This will allow us to find the minimum value for $R_{failure}$, which in turn will lead to the minimum switching period of the N-MOS device (5.22).

$$R_{failuremin} = \frac{V_{in}}{2I_{avg}} \quad (5.21)$$

$$T_{swmin} = \frac{4\Delta i L}{V_{in}} \quad (5.22)$$

Knowing T_{swmin} , bus voltage V_{in} and the hysteresis band(Δi), we can calculate the maximum switching frequency for a given inductance, as shown in Eq.5.24

$$F_{swmax} = \frac{V_{in}}{4\Delta i L} \quad (5.23)$$

In the same way, fixing the switching frequency we can obtain the minimum inductor value:

$$L_{min} = \frac{V_{in}}{4\Delta i F_{swmax}} \quad (5.24)$$

In our case, with a bus voltage of 100 V, a maximum switching frequency of 500 KHz and a class 10 LCL, the critical resistance would be 7.14 Ω and the minimum inductance needed L_{min} , 20 μ H.

5.2.1 Thermal design of the inductor

The thermal design of the coil in the switched LCL topology has been conducted by considering its two operating zones. Initially, the calculation of copper losses (PCu) and core losses (Pcore) in the coil was taken into account for both zones. When the LCL operates within its nominal zone, the coil losses are mainly attributed to PCu. Since the high-frequency AC component of the current experiences minimal variation in this zone, Pcore losses are negligible.

In contrast, when the LCL operates in the switching zone during the trip-off time, both PCu and Pcore contribute to the total coil losses. Despite the LCL primarily operating in its nominal zone, the most significant losses are due to copper resistance in this operating zone. However, it is crucial to ensure that the magnetic core does not saturate when a fault occurs.

To ensure that, first the minimum number of turns will be calculated to avoid core saturation using Eq.5.25 and then obtaining the value of the copper losses using Eq. 5.26.

$$N_{min} = \frac{LI_{max}}{B_{sat}A_e} + 0.5 \quad (5.25)$$

$$P_{cu} = \rho_{cu} \frac{l_m I_{nom}^2}{A_w f_w} N_{min}^2 \quad (5.26)$$

Where N_{min} is the minimum amount of turns, L is the inductance, B_{sat} is the saturation flux of the core and A_e is the effective area of the core.

In equation 5.26, ρ_{cu} is the copper resistivity, $1.75 \cdot 10^{-8}\Omega m$, l_m is average turn length,

A_w is the core window area and f_w is the window factor, fixed at 0.3

Finally, to select the magnetic core size, the copper temperature T_{Cu} was calculated from the P_{Cu} as well as the final copper temperature $T_{finalCu}$ at the end of the trippof time.

$$T_{Cu} = \frac{P_{Cu}}{2} \cdot \left[\frac{0,001}{A_w} + \frac{(2W_L + W_d)}{2A_w \cdot f_w \cdot \Lambda_{thCu}} \right] + T_o \quad (5.27)$$

$$T_{finalCu} = T_{Cu} + \frac{1}{C_{th}} \cdot \Delta P_{Cu} \cdot trip_off \quad (5.28)$$

Eq.5.27 depends on parameters related with the magnetic core dimensions (W_d, W_L), copper thermal conductivity Λ_{thCu} , window factor f_w , copper loses P_{Cu} and ambient temperature T_o in this case set to 40°C. Eq.5.28 the specific heat capacity C_{th} , that can be calculated using Eq.5.29

$$C_{th} = C_{thCu} \cdot V_e \cdot D_{eCu} \quad (5.29)$$

where C_{thCu} is the specific heat capacity of the copper, fixed a t 386 J/(Kg°C), V_e is the effective volume for each core and D_{eCu} is the specific density of the copper, fixed at 8960 Kg/m^3 . It is also needed to calculate ΔP_{Cu} from the difference between the copper losses before the fault and during the fault. Finally, fixing the maximum final copper temperature to 80°C we can calculate the smallest magnetic core, being it a E25/13/7.

5.3 PCB footprint

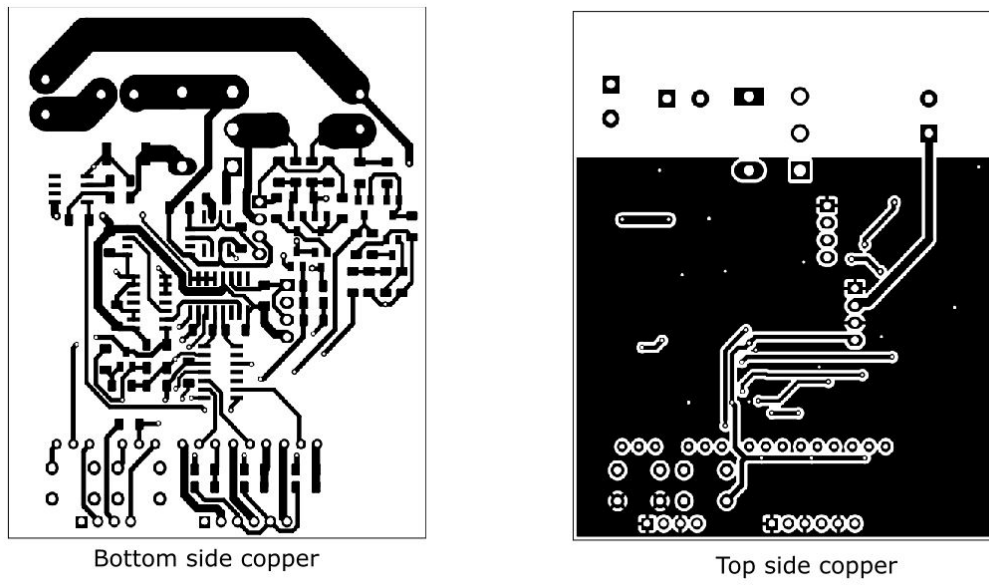


Figure 5-2: PCB footprint

5.4 Bill of materials

List of materials used in this project. Although for passive components it is easy to obtain the cost, in the case of the space-grade components it is much harder to obtain a quotation for the actual prices so, their non-space-grade equivalent was used.

Working hours budget				
Number	Unit number	Concept	Unitary price	Subtotal
1	100	Research hours (Background research, simulation, etc)	30 €	3.000 €
2	170	Laboratory hours (Prototybe building and testing)	35 €	5.950 €
3	100	Documentation hours	30 €	3.000 €
TOTAL LABOUR COST:				11.950 €

Table 5.1: working hours budget

5.5 Components total cost

COMPONENTS BUDGET OF THE PCB				
Number	Unit number	Concept	Unitary price	Subtotal
1	1	NTHL045N065SC1:Power MOSFET	14,02€	14,02€
2	5	MMBT2907A:PNP transistor	0,385€	1,925€
3	3	NPN transistor	0,26€	0,78€
4	1	Power inductor	5,22€	5,22€
5	1	RF1501NS3STL:Power diode	1,53€	1,53€
6	1	TLP700:Optocoupler	1,85€	1,85€
7	1	THT Capacitor 2200uF	0,4€	0,4€
8	4	SMD Capacitor 2pF	0,2€	0,8€
9	1	SMD Capacitor 4.7uF	0,2€	0,2€
10	1	SMD Capacitor 47pF	0,2€	0,2€
11	2	SMD Capacitor 1nF	0,2€	0,4€
12	4	SMD Capacitor 4.7uF	0,2€	0,8€
13	1	SMD Resistor 1206 1.3K	0,2€	0,2€
14	2	SMD Resistor 1206 18K	0,2€	0,4€
15	1	SMD Resistor 1206 33K	0,2€	0,2€
16	1	SMD Resistor 1206 3.6K	0,2€	0,2€
17	2	SMD Resistor 1206 9.1K	0,2€	0,4€
18	1	SMD Resistor 1206 2.4K	0,2€	0,2€
19	2	SMD Shunt Resistor 20mO	1€	2€
20	1	SMD Resistor 1206 3O	0,2€	0,2€
21	7	SMD Resistor 1206 1K	0,2€	1,4€
22	2	SMD Resistor 1206 68	0,2€	0,4€
23	2	SMD Resistor 1206 15K	0,2€	0,4€
24	4	SMD Resistor 1206 10K	0,2€	0,8€
25	1	SMD Resistor 1206 4.7K	0,2€	0,2€
26	1	SMD Resistor 1206 700	0,2€	0,2€
27	2	SMD Resistor 1206 100K	0,2€	0,4€
28	1	SMD Resistor 1206 130K	0,2€	0,2€
29	1	SMD Resistor 1206 510K	0,2€	0,2€
30	1	SMD Resistor 1206 2K	0,2€	0,2€
31	2	Switch button 6mmx5mm	0,12€	0,24€
32	5	Jumper P2.54	0,6€	3€
33	1	PinHeader 1x06 P2.54mm	0,66€	0,66€
34	1	PinHeader 1x04 P2.54mm	0,44€	0,44€
35	3	TerminalBlock 1x02 P5.08mm Horizontal	2,2€	6,6€
36	1	LM339: Quad High speed comparator	0,55€	0,55€
37	1	TL082: JFET Input Low Noise Amplifier	1,02€	1,02€
38	1	CD4027BE: CMOS dual J-K FLIP-FLOP	0,3€	0,3€
39	1	EL7202CN: High Speed, Dual Channel Power MOSFET Drivers	3,59€	3,59€
40	1	CD4081BE:Quad 2 inputs AND gate	0,46€	0,46€
TOTAL COMPONENT COST				53,185€

Table 5.2: Component cost

5.6 Total execution cost

Total budget	
Material	53,18 €
Labour	11.950 €

Total cost	12.003,18 €
Indirect costs(15%)	1.800,48 €

Total partial cost	13.803,66 €
Industrial bennefit (15%)	2.070,55 €
V.A.T.(21%)	3.333,58 €

TOTAL EXECUTION COST	19.207,79 €
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Table 5.3: Total execution cost

The total cost for the development of the project sums up to 19.207,79 €, **NINETEEN THOUSAND TWO HUNDRED SEVEN POINT SEVEN NINE EUROS.**

Ferrol, 14th of Juy, 2023

Signed, Javier Prado Pico

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