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# A Family of DC-DC Converters Based on Y-Source Impedance Network and Boost Module

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***Abstract*—A novel family of high-gain converters based on the Y-source impedance network is proposed in this paper, providing novel solutions to high voltage gain applications. Compared with the traditional improved Y-source topology, the proposed new topologies relocate the switch from the output side to the input side, which effectively reduces the stress of the switching device, and the topology combines different boost modules, which effectively improves the boost ability. In order to show the characteristics of the proposed topologies, the operating principles and analyses are given detailed in this paper. Experimental results verify the feasibility of the proposed converters.**

***Index Terms*—Y-source impedance network, Boost module, Switched Inductor, high-voltage gain converters**

## I. Introduction

With the increasing need for high step-up converters in PV and fuel cell applications, many different topologies are proposed. In recent years, impedance-source inverters (ISI) have been proposed to show good step-up characteristics [1-10]. For example, the Z-source inverter is a typical impedance-source inverter that can improve gain and alleviate distortions with only one stage [11]. In recent years, more research has been given to use the impedance network structure to realize DC-DC converters.

Some improvements are introduced to the Z-source inverter subsequently to pursue a better performance that can also be adopted in DC-DC condition, one of which is the quasi-Z-source inverter proposed in [12]. For the sake of increasing the boost ratio and reducing components simultaneously, various coupled-inductor impedance-source inverters (CISI) have been proposed [13-16]. Different coupled inductors can be seen in Fig. 1. T-source inverter (TSI) is the simplest one among CISIs, which is a high-efficiency structure with a passive diode, a capacitor, and a two-winding coupled inductor [13]. A high boost ratio can be achieved by adjusting the turns ratio of the coupled inductors rather than adding extra components.

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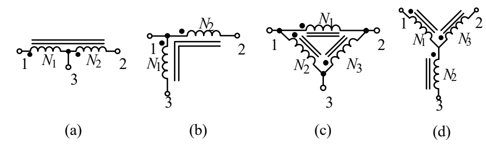



Fig. 1 Different coupled inductors. (a) T type (b) Γ type (c) Δ type (d) Y type

The Y source impedance network is an emerging one with flexible adjustment characteristics. Among them, Y-source appears to be both promising and versatile, which is a high-gain network with more generic winding design flexibility for the coupled magnetics [17-28]. The gain of the Y-source converter is indeed higher than other classical impedance networks even working at a smaller shoot-through duty cycle. One shortcoming is that the input current is discontinuous.

The continuous input current Y source structure topology is shown in Fig. 2(a). An inductor and a capacitor are added to the traditional Y source structure, which effectively overcomes the problem of the discontinuous input current of traditional Y source topology. The voltage gain $G$ is $1/(1-D(K+1))$, where $D$ is the duty cycle of the switch, $K$ is the winding factor, $K=(N_1+N_3)/(N_3-N_2)$. However, one shortcoming of the Y source topology is high switch voltage stress.

Based on the continuous input current Y-source topology, to further optimize the topology performance and reduce the stress of the switch, the switch is transferred from the output side to the input side [29]. The front switch Y-source topology is shown in Fig. 2(b). The voltage gain $G$ is $(1+DK)/(1-D)$, The meanings of $D$ and $K$ remain the same as the improved Y-source converter.

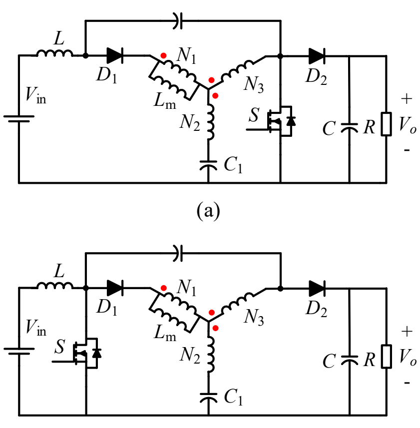



Fig. 2 Topology diagram comparison. (a) Continuous input current Y-source converter (b) Front switch Y-source converter.

To further improve the step-up ability, this paper presents a novel family of front-switch Y-source converters based on different boost modules. The structure of the proposed converter is shown in Fig. 3. The boost ratio of the topology is further improved by replacing the input inductor with different boost modules.

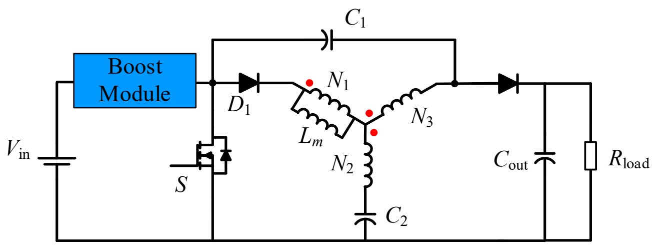



Fig. 3 Structure of the proposed converter.

There are three types of boost modules, named Type-I boost cell, Type-II boost cell, and Type-III boost cell, as shown in Fig. 4.

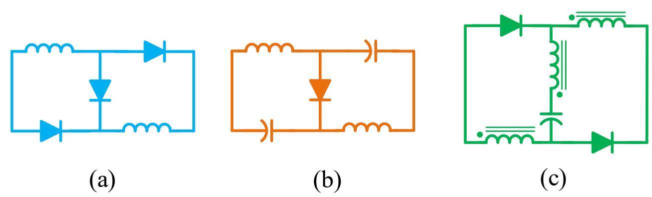



Fig. 4 Boost modules. (a) Type-I boost cell. (b) Type-II boost cell. (c) Type-III boost cell.

Based on the work in [1], using the boost module in the topology can effectively improve the boost ratio without changing the characteristics of the Y-source network in the original topology. It can improve the stability and flexibility of the system.

The operating modes analysis of the three different improved front switch Y-source converters in Section II, a comparative analysis with the conventional Y impedance source converter in Section III, experimental results in Section IV, and conclusions in Section V.

## II. Operation of the Proposed Converters

For the convenience of analysis, some assumptions are made as follows:

(1) All capacitors are large enough that voltage across the capacitors can be seen as constant.

(2) The coefficient of the coupling inductor is assumed to be 1, and the influence of leakage inductance is not considered.

(3) All the switches and diodes are ideal where the on-resistance and conduction voltage are ignored.

### *A. Type-I Front Switch Y-source converter*

The Type-I switched-inductor is used to replace the input inductor in the original topology, the Type-I boost cell is shown in Fig. 4(a). The Type-I switched-inductor includes diodes $D_1$, $D_2$ and $D_3$ and inductors $L_1$ and $L_2$, where $L_1$ equals to $L_2$. The proposed Type-I front switch Y-source topology (I-F-Y-source converter) is shown in Fig. 5.

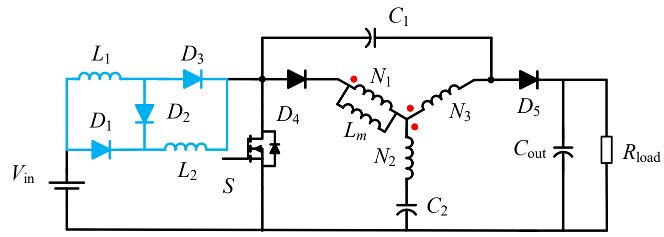



Fig. 5 Type-I front switch Y-source converter.

According to the switching state of the I-F-Y-source converter, the circuit operating modes can be divided into shoot-through state and non-shoot-through state, as shown in Fig. 6.

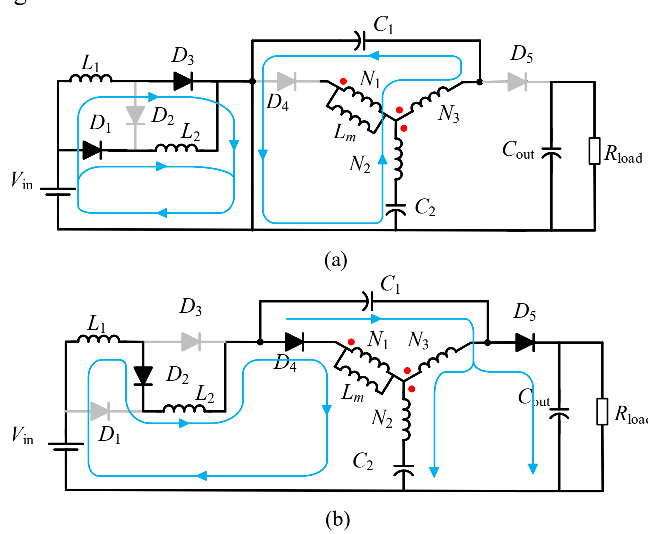



Fig. 6. Operating states of the I-F-Y source converter. (a) Shoot-through state. (b) Non-shoot-through state.

#### *1) Shoot-through state*

At this time, the circuit mode is shown in Fig. 6(a), the switch $S$ is on, and the diodes $D_2$, $D_4$, and $D_5$ are turned off. At this time, the capacitor $C_1$ is charged, the capacitor $C_2$ is discharged, the inductors $L_1$ and $L_2$ are connected in parallel, and the current increases linearly, based on KVL, the following equations can be derived:

$$V_{in} = V_{L1} \tag{1}$$

$$V_{in} = V_{L2} \tag{2}$$

$$V_{C1} + V_{N3} = V_{C2} + V_{N2} \tag{3}$$

#### *2) Non-Shoot-through state*

At this time, the circuit mode is shown in Fig. 6(b), the switch $S$ is turned off, the diodes $D_1$ and $D_3$ are turned off, the capacitor $C_1$ begins to discharge, the capacitor $C_2$ is charged, and $L_1$ and $L_2$ are connected in series at this time, and the current flowing decreases linearly:

$$V_{in} = V_{L1}^{'} + V_{L2}^{'} + V_{N1}^{'} + V_{N2}^{'} + V_{C2} \tag{4}$$

$$V_{in} + V_{C1} = V_{L1}^{'} + V_{L2}^{'} + V_{o} \tag{5}$$

$$V_{C2} + V_{N2}^{'} = V_{o} + V_{N3}^{'} \tag{6}$$

According to the coupling relationship between the three winding Y source coupled inductor, (7) can be obtained:

$$V_{N1} = V_{Lm}, V_{N2} = \frac{N_2}{N_1} V_{Lm}, V_{N3} = \frac{N_3}{N_1} V_{Lm} \tag{7}$$

Based on the above equations and the volt-second balance relationship of each winding, the capacitor voltage and voltage gain can be obtained:

$$V_{C1} = \frac{D(1+D)K}{1-D} V_{in} \tag{8}$$

$$V_{C2} = \left[(K-1)D+1\right]\frac{1+D}{1-D} V_{in} \tag{9}$$

$$G = \frac{1+DK}{1-D}(1+D) \tag{10}$$

where the winding factor $K$ is:

$$K == \frac{N_3+N_1}{N_3-N_2} \tag{11}$$

Compared with the boost ratio $G$ of the original topology, which is $(1+DK)/(1-D)$, the boost ratio of the Type-I improved topology is increased by $(1+D)$ times. The adoption of the Type-I boost cell can effectively improve the operation of the original topology voltage output.

### B. Type-II Front Switch Y-source converter

The Type-II front switch Y-source topology (II-F-Y source converter) uses a Type-II boost cell, as shown in Fig. 4(b), to replace the input inductors. The Type-II switched-inductor includes diode $D_1$, capacitors $C_{n1}$, $C_{n2}$ and inductors $L_1$ and $L_2$, where $C_{n1}$ equals $C_{n2}$, $L_1$ equals $L_2$, as shown in Fig.7.

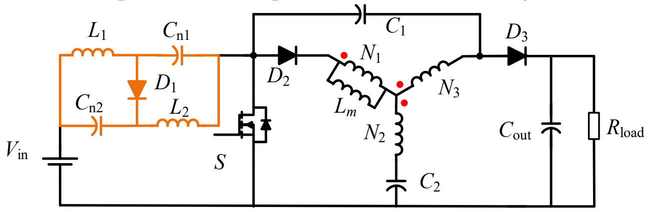



Fig. 7. Type-II front switch Y-source converter.

According to the operation condition, the circuit is also divided into shoot-through state and non-shoot-through state, as shown in Fig.8.

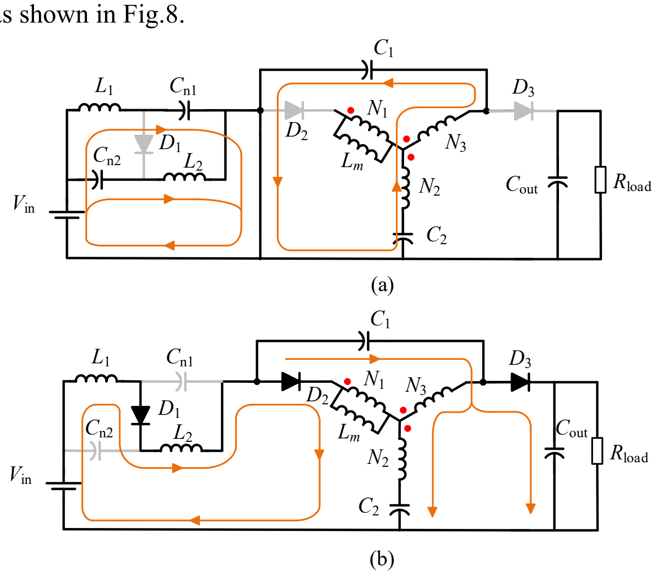



Fig. 8. Operating states of the II-F-Y source converter. (a) Shoot-through state. (b) Non-shoot-through state.

#### 1) Shoot-through state

At this state, the operating mode is shown in Fig. 8(a), the switch $S$ is on, all the diodes are in the off state, the capacitors $C_{n1}$ and $C_{n2}$ discharge to the inductors $L_1$ and $L_2$ respectively, the two branches are connected in parallel, and the capacitor $C_1$ charges while $C_2$ discharges:

$$V_{cn1} + V_{in} = V_{L1} \tag{12}$$

$$V_{cn2} + V_{in} = V_{L2} \tag{13}$$

$$V_{C1} + V_{N3} = V_{C2} + V_{N2} \tag{14}$$

#### 2) Non-Shoot-through state

At this state, the circuit mode is shown in Fig. 8(b), the switch $S$ is off, all the diodes are in the conducting state, the capacitor $C_1$ is discharged, the capacitor $C_2$ is charged, $L_1$ and $L_2$ are now connected in series, transmitting energy to the output side.

$$V_{in} = V_{L1}^{'} + V_{L2}^{'} + V_{N1}^{'} + V_{N2}^{'} + V_{C2} \tag{15}$$

$$V_{in} + V_{C1} = V_{L1}^{'} + V_{L2}^{'} + V_{o} \tag{16}$$

$$V_{C2} + V_{N2}^{'} = V_{o} + V_{N3}^{'} \tag{17}$$

$$V_{cn1} + V_{L2}^{'} = 0 \tag{18}$$

$$V_{cn2} + V_{L1}^{'} = 0 \tag{19}$$

Based on these above equations, the capacitor voltage and voltage gain can be obtained:

$$V_{C1} = \frac{DK}{1-2D} V_{in} \tag{20}$$

$$V_{C2} = \frac{1-D+DK}{1-2D} V_{in} \tag{21}$$

$$V_{cn1} = V_{cn2} = \frac{D}{1-2D} V_{in} \tag{22}$$

$$G = \frac{1+DK}{1-2D} \tag{23}$$

Compared with the boost ratio of the original topology, under the same duty cycle $D$, the boost ratio of the II-F-Y source converter reduces the denominator term, and the $G$ is also much higher. At the same time, the adjustment range of the switch duty cycle is between 0 to 50%.

### C. Type-III Front Switch Y-source converter

The Type-III front switch Y-source topology (III-F-Y source converter) uses a Type-III boost cell, as shown in Fig. 4(c). The Type-III switched-inductor includes diodes $D_1$ and $D_2$, capacitor $C_n$ and a three-winding coupled inductor T. For the coupled inductor $T$, the number of turns of the windings $T_1$ and $T_3$ is the same, and the number of turns of the winding $T_2$ is $n$ times that of the windings $T_1$ and $T_3$, that is, $nN_{T1} = N_{T2} = nN_{T3}$, as shown in Fig. 9.

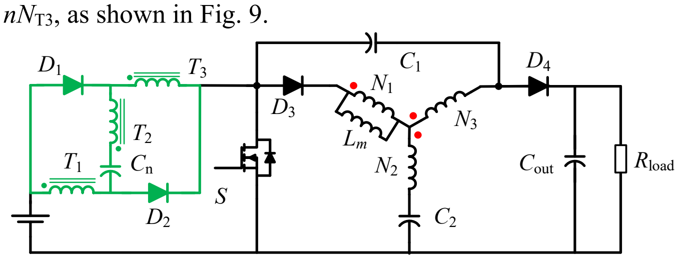



Fig. 9. Type-III front switch Y-source converter.

According to the operating condition, the circuit is also divided into shoot-through state and non-shoot-through state, as shown in Fig. 10. Further, the main voltage and current waveforms are shown in Fig. 11.

#### 1) Shoot-through state

During this operating mode, the equivalent circuit is shown in Fig. 10(a), the diodes $D_1$ and $D_2$ are turned on, the capacitors $C_n$ and $C_1$ are charged, and $C_2$ is discharged:

$$V_{cn} = V_{T1} + V_{T2} \tag{24}$$

$$V_{in} = V_{T1} = V_{T3} \tag{25}$$

$$V_{C1} + V_{N3} = V_{C2} + V_{N2} \tag{26}$$

For the coupling inductor $T$, there is also the following relationship:

$$V_{T1} = V_{LmT}, V_{T2} = \frac{N_{T2}}{N_{T1}} V_{LmT}, V_{T3} = \frac{N_{T3}}{N_{T1}} V_{LmT} \tag{27}$$

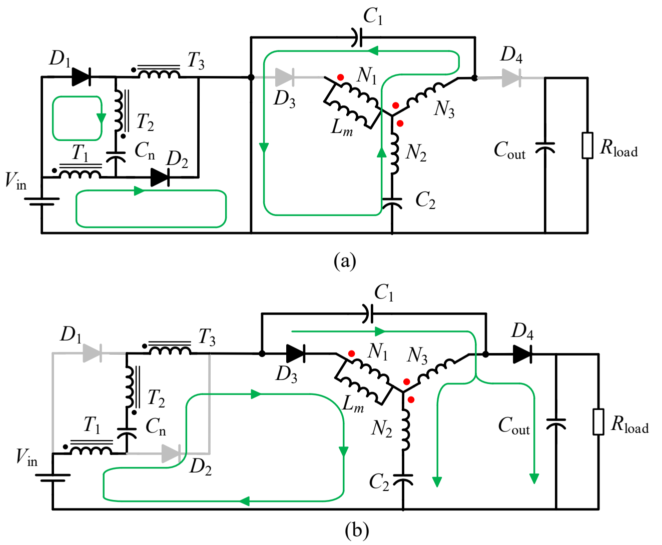



Fig. 10. Operating states of the II-F-Y source converter. (a) Shoot-through state. (b) Non-shoot-through state.

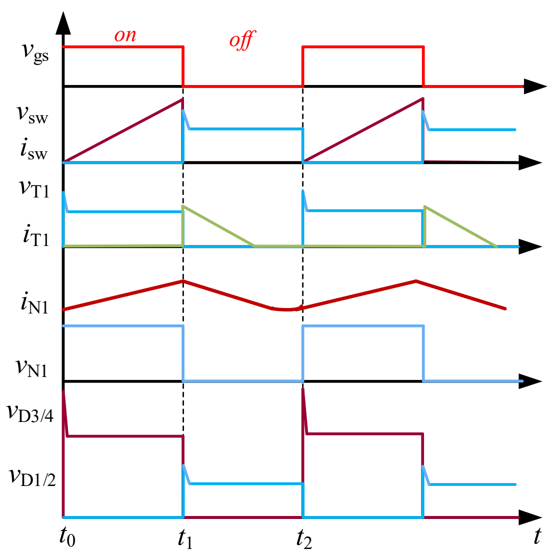


Fig. 11. Main voltage and current waveforms of the II-F-Y source converter.

#### 2) Non-Shoot-through state

At this time, the circuit mode is shown in Fig. 10(b), the diodes $D_1$ and $D_2$ are turned off, the capacitors $C_n$ and $C_1$ are discharged, and $C_2$ is charged:

$$V_{in} + V_{cn} = V'_{T1} + V'_{T2} + V'_{T3} + V'_{N1} + V'_{N2} + V_{C2} \tag{28}$$

$$V_{in} + V_{cn} + V_{C1} = V'_{T1} + V'_{T2} + V'_{T3} + V_o \tag{29}$$

$$V_{C2} + V'_{N2} = V_o + V'_{N3} \tag{30}$$

Based on these above equations, the capacitor voltage and voltage gain can be obtained:

$$V_{cn} = (1+n) V_{in} \tag{31}$$

$$V_{C1} = \frac{DK}{1-D}(2+n) V_{in} \tag{32}$$

$$V_{C2} = \frac{(1-D+DK)}{1-D}(2+n) V_{in} \tag{33}$$

$$G = \frac{1+DK}{1-D}(2+n) \tag{34}$$

Compared with the boost ratio of the original topology, the boost ratio of the III-F-Y source converter is increased by (2+$n$) times, which is much higher than the boost ratio of the original topology. III-F-Y source converter can obtain an additional high boost ratio by adjusting the turns ratio of the switch coupled inductor.

## III COMPARISON AND ANALYSIS OF DIFFERENT TOPOLOGIES

The proposed family of improved impedance source converter based boost cells are compared with the original topology, including the voltage gain and some key device stresses.

### A. Comparisons on Voltage Gain

Fig.12 shows the voltage gain comparison of the proposed topologies, including the front switch Y-source (F-Y), the improved topologies based on boost cell (I-F-Y, II-F-Y, III-F-Y).

As shown in Fig.12, the voltage gain of the improved topologies based on boost cell is higher than that of F-Y in the full duty cycle adjustment range. Among the proposed topologies, Type II and Type III topologies have higher boost capability than Type I, however need larger number of magnetics. The duty cycle range of the type II topology is 0-50%, and the duty cycle range of the other topologies is 0-100%. Compared with the traditional Y-source converter, the duty cycle adjustment range has been widened, and effectively reduce the stress of the switching device.

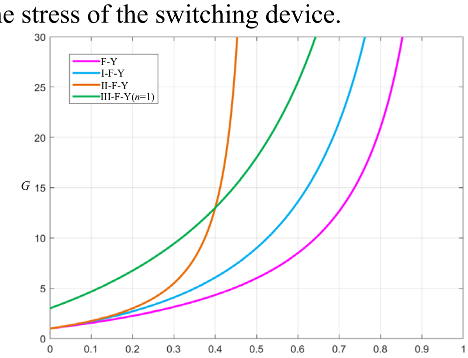



Fig. 12 Voltage gain comparison of four converters

### B. Voltage stresses of components

According to the previous theoretical derivation, the device voltage stress of each topology can be obtained, as shown in Table I, which includes the voltage stress of switch, diodes, capacitors, and some devices included in the improved topology based on boost cells.

Table I Voltage Stresses of Components in Different Topologies.

| Topologies | Switch | $D_{\text{Y-source}}$ | $D_{\text{out}}$ | $C_1$ | $C_2$ | other |
|---|---|---|---|---|---|---|
| F-Y | $\frac{1}{1-D}V_{\text{in}}$ | $\frac{K}{1-D}V_{\text{in}}$ | $\frac{1}{1-D}V_{\text{in}}$ | $\frac{DK}{1-D}V_{\text{in}}$ | $\left(1+\frac{DK}{1-D}\right)V_{\text{in}}$ | |
| I-F-Y | $\frac{1+DK}{1-D}V_{\text{in}}$ | $\frac{1+D}{1-D}KV_{\text{in}}$ | $\frac{1+DK}{1-D}V_{\text{in}}$ | $\frac{D(1+D)K}{1-D}V_{\text{in}}$ | $\left[(K-1)D+1\right]\frac{1+D}{1-D}V_{\text{in}}$ | $V_{\text{D1}}=V_{\text{D3}}=\frac{D}{2(1-D)}V_{\text{in}}$ <br> $V_{\text{D2}}=V_{\text{in}}$ |
| II-F-Y | $\frac{1}{1-2D}V_{\text{in}}$ | $\frac{K}{1-2D}V_{\text{in}}$ | $\frac{1}{1-2D}V_{\text{in}}$ | $\frac{DK}{1-2D}V_{\text{in}}$ | $\frac{1-D+DK}{1-2D}V_{\text{in}}$ | $V_{\text{D1}}=\frac{1}{1-2D}V_{\text{in}}$ <br> $V_{\text{cn1}}=V_{\text{cn2}}=\frac{D}{1-2D}V_{\text{in}}$ |
| III-F-Y | $\frac{2D}{1-D}(2+n)V_{\text{in}}$ | $\frac{K}{1-D}(2+n)V_{\text{in}}$ | $\frac{1+DK}{1-D}(2+n)V_{\text{in}}$ | $\frac{DK}{1-D}(2+n)V_{\text{in}}$ | $\frac{(1-D+DK)}{1-D}(2+n)V_{\text{in}}$ | $V_{\text{D1}}=V_{\text{D2}}=\frac{1}{1-D}(1+n)V_{\text{in}}$ <br> $V_{\text{cn}}=(1+n)V_{\text{in}}$ |

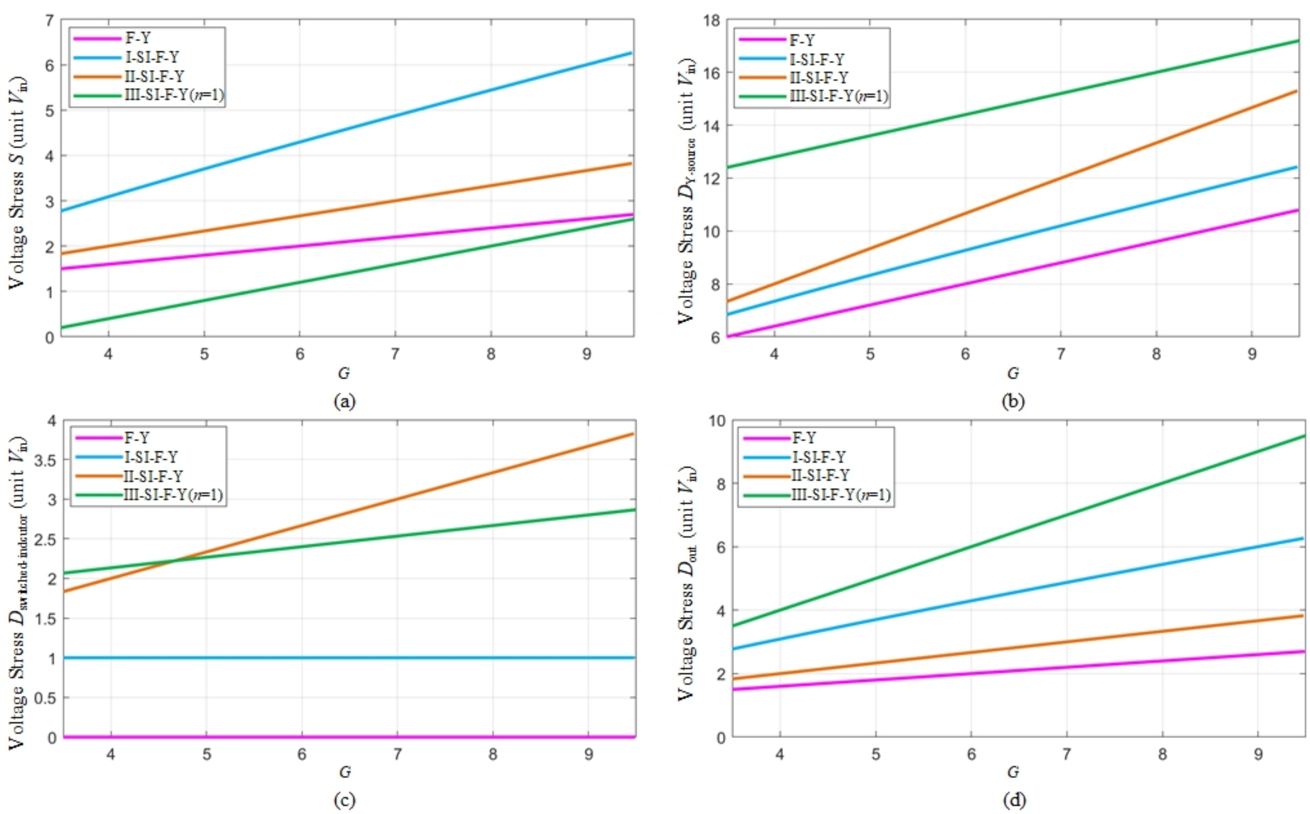



Fig. 13 Comparisons of voltage stresses between different topologies. (a) Nominalized switch voltage stress. (b) Nominalized voltage stress of the diode connecting with winding $N_1$. (c) Nominalized voltage stress of the diode in switched inductor module. (d) Nominalized voltage stress of the diode in output side.

Under the condition of $K$ = 4, Fig. 13 shows the comparative analysis of voltage stress of semiconductor devices with voltage gain $G$ in the range (4.5~9.5) of four topologies. From the perspective of components number and type: for type I boost cell, it consists of two discrete inductors and three diodes which can help to reduce the module volume. For type II boost cell, it consists of two discrete inductors, one diode and two capacitors, the capacitor volume is usually larger than the diode, thus, the module should be larger than the type I module. For type III boost module, it consists of one coupled inductor, two diodes and one capacitor, which can only use one magnetic core, however, it needs three windings. From the perspective of voltage stress: The voltage stress of the switch of the I-F-Y-source converter is the highest, and the switch voltage stress of the III-F-Y-source converter is the lowest. However, in contrast, the voltage stress of the $D_{\text{Y-source}}$

in the I-F-Y topology is the lowest and that in the III-F-Y-source converter is the highest among the proposed three topologies. For the voltage stress of diodes in the boost cell, the diode voltage stress of III-F-Y-source converter is the highest, meanwhile, the output side diode voltage stress of the III-F-Y-source converter is also the highest among the three topologies. From the perspective of step-up ability and efficiency: III-F-Y-source converter can achieve the highest output voltage, however, the components loss is also the highest, thus, the efficiency of III-F-Y converter cannot be very impressive. For the I-F-Y converter, because of little components loss, the efficiency can be maintained in a high level. In general, for high efficiency and high power density, I-F-Y converter should be adopted, and for extremely high step-up, III-F-Y converter should be adopted, and for II-F-Y converter, it can be used in the feature gap between I-F-Y and II-F-Y, which can help to achieve a compromised performance.

## V. Experimental Results

In order to further verify the correctness of theoretical analysis, corresponding prototypes are built. The planar coupled inductor is a very important component. For PCB-based planar coupled inductor, the most feature characteristics is the winding structures which can be modified flexibly. Thus, how to determine optimal winding structure is very important.

Fig. 14 shows three different winding structures. The winding structure with the least leakage inductance is expected.

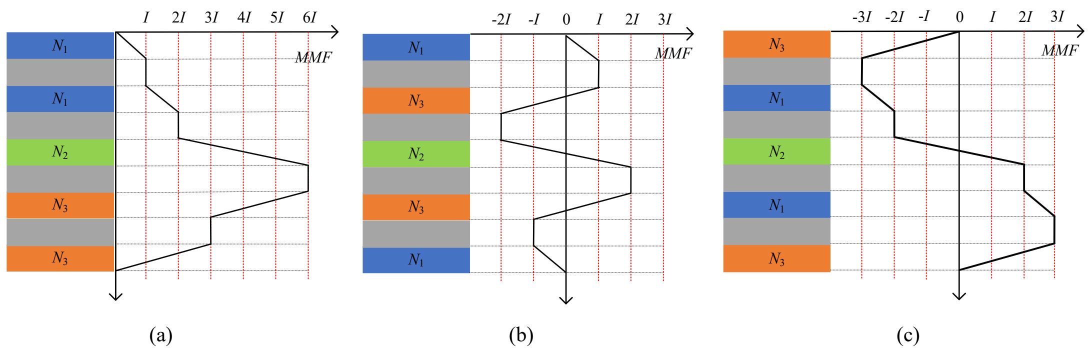



Fig. 14 Diagram of three different winding structures. (a) structure 1, (b) structure 2, (c) structure 3.

The leakage inductance can be calculated from the perspective of energy stored in each winding layers, which can be calculated as follows:

$$E_{lk} = \frac{\mu_0}{2} \sum \int_0^h H^2 \cdot l_w \cdot b_w \cdot dx \tag{35}$$

where $H$ is the magnetic field intensity, here, the value is assumed to be constant alongside the horizontal direction of winding as Fig. 14 shows, and $H$ varies alongside the vertical direction, which can be represented as:

$$H = \frac{I}{b_w} \bullet \frac{x}{h} \tag{36}$$

Based on above equation, the leakage inductance of the above three winding structures can be calculated as (37), (38) and (39) show:

$$L_{lk1} = \mu_0 \cdot \frac{l_w}{b_w} \left( \frac{5h_1 + 28h_2 + 45h_3}{3} + 50h_\Delta \right) \tag{37}$$

$$L_{lk2} = \mu_0 \cdot \frac{l_w}{b_w} \left( \frac{2h_1 + 16h_2 + 18h_3}{3} + 10h_\Delta \right) \tag{38}$$

$$L_{lk3} = \mu_0 \cdot \frac{l_w}{b_w} \left( \frac{50h_1 + 16h_2 + 18h_3}{3} + 26h_\Delta \right) \tag{39}$$

where $h_1$, $h_2$ and $h_3$ represent the thickness of conductor, $h_\Delta$ represents the thickness of insulator, $l_w$ represents the length of conductor in each layer, $b_w$ is the width of conductor in each layer. Based on above equations, the leakage inductance of different winding structures can be calculated to be $L_{lk1}$ = 1285.13 (nH), $L_{lk2}$ = 261.5 (nH), $L_{lk3}$ = 677.7 (nH). Thus, it can be seen that winding structure 2 contributes to the smallest leakage inductance.

Besides the leakage inductance, the winding resistance, especially the winding AC resistance, plays a very important role to affect the performance of coupled inductor. The ratio between AC resistance and DC resistance under the $m$-th layer can be represented by:

$$\frac{R_{ac,m}}{R_{dc,m}} = \frac{\xi}{2} \left[ \frac{\sinh \xi + \sin \xi}{\cosh \xi - \cos \xi} + (2m-1)^2 \cdot \frac{\sinh \xi - \sin \xi}{\cosh \xi + \cos \xi} \right] \tag{40}$$

$$m = \frac{F(h)}{F(h) - F(0)} \tag{41}$$

where $\xi = h/\delta$, $h$ still represents the thickness of the conductor, $\delta$ is skin depth. $F(0)$ and $F(h)$ represents magnitude of magnetomotive force in the top and bottom side of the insulator layer. According above equations, Fig. 15 can be plotted. From the curves, it can be seen that larger $m$ leads to higher AC resistance under the same DC resistance condition.

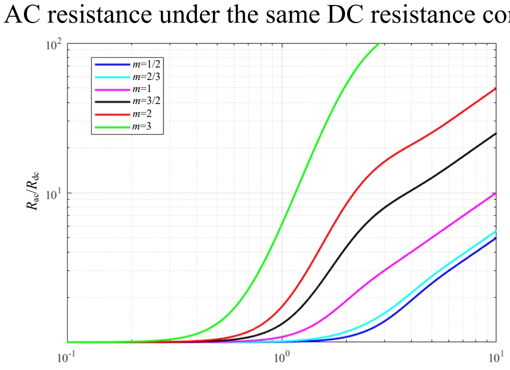



Fig. 15. The ratio between AC resistance and DC resistance

According to the equations and Fig. 15, the value of $m$ can be calculated under different winding structures. From Table II, it can be seen that the overall $m$ value is the smallest in structure 2 among the three different winding structures.

Table II The value of $m$ under different winding structures

| | *Structure 1* | *Structure 2* | *Structure 3* |
|---|---|---|---|
| $m_{N1\_1}$ | 1 | 1 | 3 |
| $m_{N1\_2}$ | 2 | 1 | 3 |
| $m_{N2}$ | 1.5 | 1/2 | 1/2 |
| $m_{N3\_1}$ | 2 | 2/3 | 1 |
| $m_{N3\_2}$ | 1 | 2/3 | 1 |

Thus, from the perspective of leakage inductance and AC winding, the winding structure of the PCB planar coupled inductor is selected to be structure 2, which is shown in Fig. 16.

Based on the designed Y coupled inductor, the pictures of the prototypes are shown in Fig. 17. For the proposed step-up converters, the applications focus on the renewable energy utilization, especially for the PV and fuel cell applications. The experimental parameters are shown in Table III.

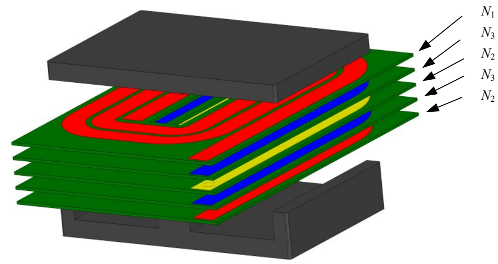
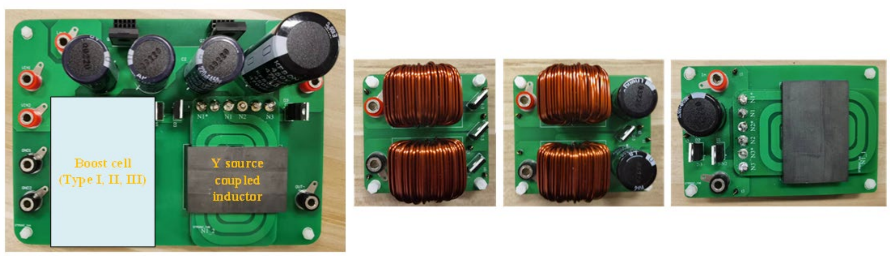



Fig. 16 Selected winding structure of the planar coupled inductor

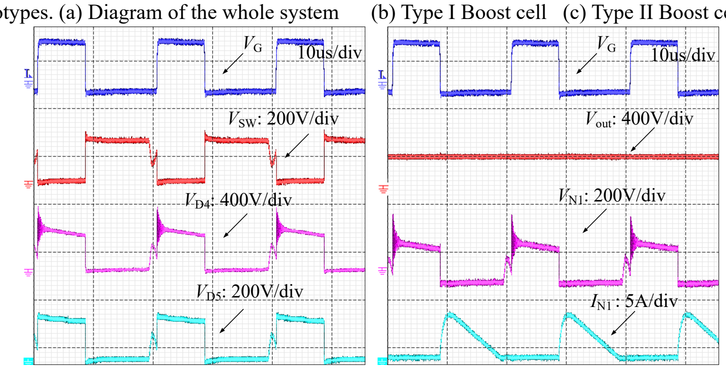
Table II Experimental Parameters

| Component | Specifications | Component | Specifications |
|---|---|---|---|
| Input Voltage | 40V | $C_1$, $C_2$, $C_{out}$ | 470µF |
| Output Voltage | 240V | Turns ratio of Y-source | $N_1$:$N_2$:$N_3$=2:1:2 |
| $R_{load}$ | 200Ω(280W) | Diode | CI10S65 |
| Frequency | 50kHz | Switch | SCT3060AL |



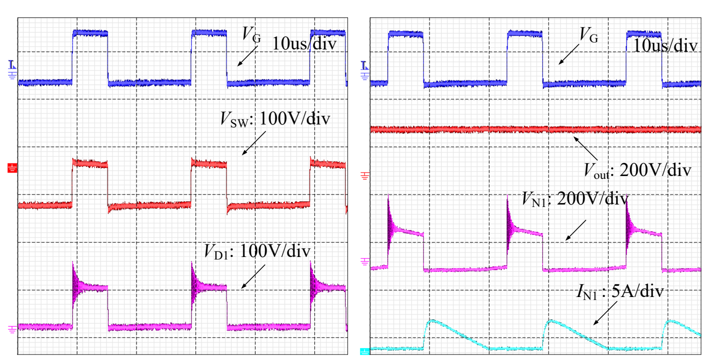

(a) (b) (c) (d)

Fig. 17 Pictures of the proposed prototypes. (a) Diagram of the whole system (b) Type I Boost cell (c) Type II Boost cell (d) Type III Boost cell



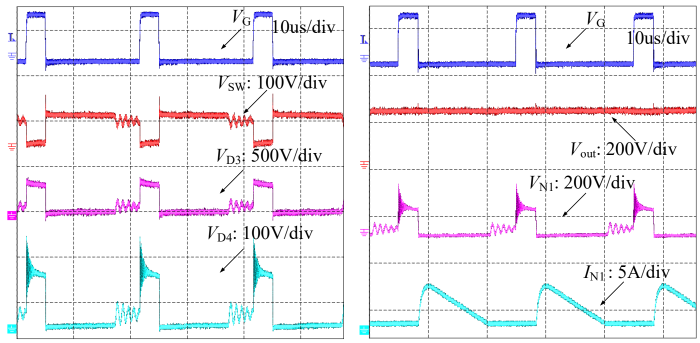

(a) (b)

Fig. 18 Main voltage and current waveforms of I-F-Y converter. (a) Switch and diodes voltage. (b) Output voltage, winding voltage and current.




(a) (b)

Fig. 19 Main voltage and current waveforms of II-F-Y converter. (a) Switch and diodes voltage. (b) Output voltage, winding voltage and current.




(a) (b)

Fig. 20 Main voltage and current waveforms of III-F-Y converter. (a) Switch and diodes voltage. (b) Output voltage, winding voltage and current.

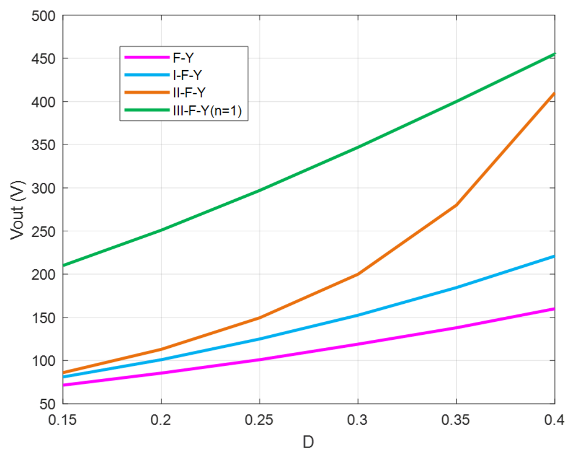



Fig. 21 Output voltage comparison curve.

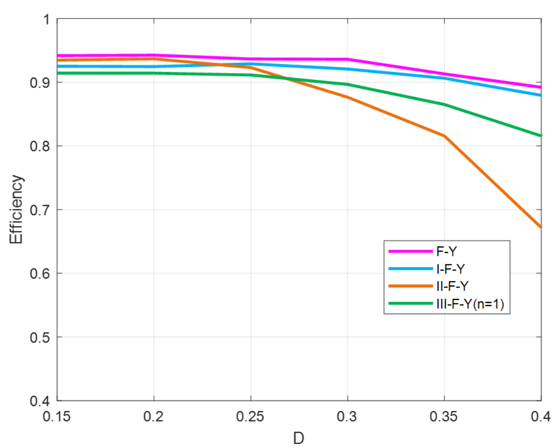



Fig. 22 System efficiency comparison curve.

Fig. 18 shows the main voltage and current waveforms of I-F-Y prototype, the voltage stress results are: $V_{SW}$=196V, $V_{D1}$=$V_{D3}$ =18V, $V_{D2}$=45V, $V_{D4}$=397V, $V_{D5}$=187V, and the output voltage $V_{out}$=238V, where the voltage stresses of the switches and diodes are consistent with the theoretical analysis, some oscillations occur during the mode transition procedure because of the ringing between parasitic inductance and capacitance. The current of winding $N_1$ decreases to zero during the switch-off period. Fig. 19 shows the main voltage and current waveforms of II-F-Y prototype, the voltage stresses are $V_{SW}$=$V_{D1}$ =$V_{D3}$=109V, $V_{D2}$=435V and $V_{out}$=238V, which are still consistent with the analysis results, the oscillations occur during switch off to on transition. Fig. 20 shows the main voltage and current waveforms of III-F-Y prototype, the voltage stresses are $V_{SW}$=$V_{D1}$ =$V_{D3}$=109V, $V_{D2}$=435V and $V_{out}$=238V, which are still consistent with the analysis results. The current of winding $N_1$ decreases to zero during the switch-off period.

Fig. 21 and Fig. 22 shows the output voltage and system efficiency comparison of the proposed three improved topologies and the conventional front switch Y-source converter. As can be seen, under the same duty cycle, the III-F-Y shows the best step-up ability. And the proposed three improved topologies all have higher output voltage than the conventional one. Compared the typical front-side converter, the proposed three topologies based on boost modules cause more loss because of more passive and active devices. However, the efficiency decrement can be accepted compared the improved step-up ability. For the II-F-Y topology, the efficiency drops quickly when the duty cycles around 0.4 because the duty cycle limitation of the topology is 0.5. Thus, when the duty cycle comes to the limitation, the effect of the parasitic resistance become serious. Among these three topologies, I-F-Y shows the best efficiency performance. Based on above analysis, without extreme duty cycle and winding factor, also avoiding multiple cascaded step-up converters, the proposed topologies can achieve higher voltage gain with increased stability and flexibility.

## VI. Conclusion

This paper proposes three improved DC-DC converters based on Y-source impedance network and boost modules, which own high feasibility and enhanced boost capacity. Under the same duty cycle, the III-F-Y shows the best step-up ability. Under the same voltage gain, the I-F-Y shows the lowest switch voltage stress. Type II and Type III topologies have higher boost capability than Type I, however need larger number of magnetics. Appropriate improved topology can be selected according to the needs of different occasions. Working principles and comparisons are presented. Experimental results verify the feasibility of the proposed converters, which provides more advanced topologies for future step-up converters.

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