



## Article Study of Multiple Discontinuous Conduction Modes in SEPIC, Ćuk, and Zeta Converters

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Abstract: In this paper, we studied the discontinuous conduction modes (DCMs) of modified versions of the SEPIC, Ćuk, and Zeta converters. The modified versions of these converters were obtained by adding an extra diode to the classical versions of these converters; thus, we obtained converters with multiple DCMs. In the case of the SEPIC and Ćuk converters, the additional diode was added in series with the inductor placed at the input port, thus resembling the connection of a four-diode bridge rectifier at the input (where these converters work as power factor correctors in AC/DC conversion). The 2 diodes of the modified versions of these converters define 4 possible conduction modes: 1 continuous conduction mode (CCM) and 3 DCMs. In this paper, the 4 conduction modes were exhaustively studied, calculating their voltage conversion ratios and the equations of the curves that define the borders between conduction modes in both open- and closed-loop operations. The conduction modes and the straight line that describes the converter operation are represented in a plane called the " $k_1k_2$  plane". As in the case of other characteristics exhibited by the SEPIC, Ćuk, and Zeta converters, the conduction modes, the voltage conversion ratios in each conduction mode, and the boundaries between conduction modes, coincide for the three studied converters. Finally, all theoretical predictions resulting from the analysis were verified experimentally through a reconfigurable converter prototype, working as both modified SEPIC and modified Ćuk converters.

**Keywords:** DC/DC converters; SEPIC; Ćuk and Zeta converters; multiple discontinuous conduction modes

## 1. Introduction

A DC/DC converter with a single inductor and a single diode can operate in a continuous conduction mode (CCM) or a discontinuous conduction mode (DCM) [1]. In CCM, the current passing through the converter inductor never reaches zero, while in the so-called DCM, the current reaches zero and remains at this value until the transistor conduction occurs again [2]. In CCM, the standard converters have low output impedance in open-loop operations and their voltage conversion ratios only depend on the duty cycle (*d*). This situation changes markedly in DCM, where the voltage conversion ratios still depend on the duty cycle, but also depend on the load (*R*), the inductance (*L*), and the switching period (*T*). Consequently, the voltage conversion ratios can be expressed mathematically as follows:

$$N = \left[\frac{V_o}{V_g}\right]_{CCM} = f_{CCM}(d),\tag{1}$$

$$M = \left[\frac{V_o}{V_g}\right]_{DCM} = f_{DCM}(d, R, L, T).$$
<sup>(2)</sup>



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**Copyright:** © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). In many cases, DC/DC converters are designed to operate in CCM for the main part of the load variation range. However, there are some attractive features derived from the operation in DCM [3–5], such as:

- Low switching losses due to diode operations with zero current switching (ZCS).
- Small-sized inductors.
- High voltage conversion ratio.
- Simple small-signal transfer functions in basic converters in comparison with their equivalents in CCM.
- Lack of zeros in the right half-plane (RHP) in the small-signal transfer functions corresponding to the boost and buck-boost converters.
- Possibility of operation with high power factors when some of these converters work as power factor correctors (PFCs) with constant duty cycles during the entire line period.

However, DCMs also lead to drawbacks, such as higher RMS values of the currents in passive and active components. This fact makes the output filter design and current sampling more complex [6].

One advantage of the DCM operation is loss reduction due to the ZCS in some specific switching instants. An example is presented in [7], where the transformer's operation in DCM in a dual active bridge converter allows obtaining ZCS in all semiconductors. However, the best-known application of DC–DC converters operating in DCM is the power factor correction (PFC) in a single-phase rectifier [8]. However, a DC–DC converter can also operate as a PFC on the border between the CCM and DCM, known as the critical conduction mode [9]. The operation properties in DCM were especially used in low-power and low-cost PFC applications. Another application of relevant interest is the intentional operation in DCM to achieve a higher voltage conversion ratio. This property is used in renewable energy systems, data centers, fuel cell systems, electrical vehicles, and motor drives [10,11]. Consequently, a DCM operation is the recommended conduction mode to use in an application with requirements of high-voltage conversion ratios, simple PFC operations, low energy consumption, or reduced size.

In general, the study of a DCM is limited to a DC/DC converter with a single-inductor and a single-diode, where it is well known that only 1 CCM and 1 DCM exist. In order to determine whether the converter operates in CCM or DCM, the dimensionless parameter kand its critical value  $k_c$  must be compared. The k value is defined for each operation point by the expression:

k

$$=\frac{2L}{RT},$$
(3)

where  $k_c$  corresponds to the border between CCM and DCM. In addition,  $k_c$  is defined for both the open- and closed-loop conditions and its values are specific to each converter. The conduction modes can be determined from k and  $k_c$  as follows:

- if  $k > k_c$ , then the converter operates in CCM,
- if  $k < k_c$ , then the converter operates in DCM.

The previous analysis assumes that there is only 1 diode in the converter. However, when the converter has more than one diode in inductive branches, multiple DCMs can appear and their study is not evident. The first approach to this study was presented in [12]. In this work, a modified version of the SEPIC converter was introduced. The modification carried out consists of adding an additional diode in series with the input inductor. After this modification, the SEPIC converter becomes a multi-diode and multi-inductor topology, where multiple DCMs can appear. Thus, 1 CCM and 3 DCMs were clearly identified in [12]. However, the authors only studied the small-signal model corresponding to one of the DCMs, whereas the other DCMs and their characteristics and boundaries were not addressed in that paper.

The SEPIC, Cuk, and Zeta converters belong to the buck-boost family of converters [13]. The main feature of these converters is their ability to step-up/step-down output voltage [14,15]. This property makes these converters attractive for applications that require a wide range of voltage conversion ratios. Moreover, these converters also belong to the so-called family of high-order buck-boost converters, because they have 4 reactive elements, 2 capacitors, and 2 inductors. As a consequence of having 2 inductors, multiple DCMs can appear if an additional diode is connected in a proper place.

This paper introduces all of the possible DCMs that the SEPIC, Ćuk, and Zeta converters present when an additional diode is added in the proper place, which is in series with the input inductor in the case of the SEPIC and Ćuk converters and in series with the intermediate inductor in the case of the Zeta converter. The case of these modified versions of the SEPIC and Ćuk converters is especially interesting because the additional diode resembles the operation of a four-diode rectifier connected at the input ports. The reason to connect the aforementioned rectifier is to use these converters as the active parts of a PFC. However, operating these converters as PFCs requires more research, which is beyond the scope of this work and will be addressed in another paper. The study presented here is the first step toward that objective. In this paper, the modified SEPIC converter is completely studied for the first time. The main contributions of this paper are as follows:

- Analysis of the modified versions of the SEPIC, Cuk, and Zeta converters. In all cases, the possible conduction modes were identified and their features (both in open and closed loops) are obtained.
- Graphical representation of the evolution of the converter operation point (according to [16]).
- Experimental validation of the theoretical analyses in the modified SEPIC and Cuk topological cases, through a reconfigurable converter prototype.

The structure of this paper is as follows: concepts to study the multiple DCMs are explained in Section 2. The analysis of the SEPIC converter modified by adding a diode at the input port is presented in Section 3, and a similar study of the modified version of the Ćuk converter is included in Section 4. A generalization to the case of the Zeta converter with an additional diode in series with the intermediate inductor, and common characteristics of the modified SEPIC, Ćuk, and Zeta converters are presented in Sections 5 and 6. Experimental results in both open- and closed-loop operations are presented in Section 7 to validate the mathematical analysis. Finally, Section 8 provides the conclusions of this research and future works.

# 2. Review of the Study of Multiple Discontinuous Conduction Modes in Simple DC/DC Converters

Extended information on the concepts presented in this section is available at [16].

#### 2.1. Determination of the Number n

In multi-diode and multi-inductor topologies, multiple DCMs can appear. To have several DCM modes, there must be at least 2 non-redundant diodes in inductive branches in the equivalent circuit of the converter when the transistor is in the blocking state.

## 2.2. Calculation of the Number of Conduction Modes

Calculating the number of non-redundant diodes n is important to determine the total number of conduction modes. If n > 2, then there are multiple DCMs, in total,  $2^n$  conduction modes, 1 of them will be the CCM, and the remaining  $2^n - 1$  modes will be the DCMs. Each conduction mode corresponds to certain characteristics of the current waveforms in the diodes. To establish a correlation between waveforms and the name assigned to each mode, a vector  $D = (D_1, D_2, D_3, \dots D_n)$  can be defined, where the value of  $D_x$  is 1 if the diode is conducting at the end of the switching period and 0 if it is in the blocking state at that moment. The value  $D = (1, 1, 1, \dots, 1)$  corresponds to CCM, while the remaining  $2^n - 1$  cases correspond to DCMs.

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#### 2.3. Converter Trajectories in k-Space

Each *n* diode used to determine number *n* is placed in an inductive branch, where it prevents the current reversal during the transistor OFF interval. In this inductive branch, there will be an inductor  $L_x$ , which defines a dimensionless parameter  $k_x$  as follows:

$$k_x = \frac{2L_x}{RT},\tag{4}$$

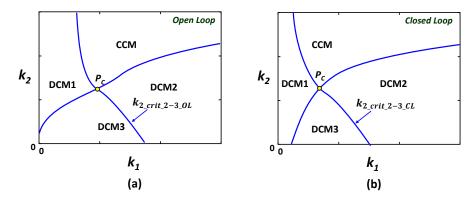
where *R* is the load resistance connected to the converter output, *T* is the switching period, and *x* satisfies  $1 \le x \le n$ . The set of values of  $k_x$  defines an *n*-dimensional space known as "*k*-space". The values that  $k_x$  verify:

$$k_n = \frac{L_n}{L_{n-1}} k_{n-1}, \ k_{n-1} = \frac{L_{n-1}}{L_{n-2}} k_{n-2} \ \dots \ k_2 = \frac{L_2}{L_1} k_1.$$
 (5)

Each Equation (5) determines a hyperplane of the n - 1 dimension in the k space. There are n - 1 hyperplanes of n - 1 dimensions. The intersection is given by Equation (5) and is always a straight line drawn in the k-space. This line is called a "trajectory" in the k-space. All possible trajectories pass through the origin of the k-space and remain completely defined once the value of each inductor  $L_x$  is selected. The operation point of the converter in the k-space will always be a point of the trajectory. That point will be the origin of the k-space when R tends to infinity. The trajectory in the k-space only depends on the R value, once the inductors and the switching frequency values are selected.

## 2.4. Borders between Conduction Modes in k-Space

In the *k*-space, each conduction mode will be a space of *n* dimensions and the border between modes will be an n - 1 dimensional space. These borders depend on the control strategy. Thus, there will be certain borders if the converter operates in an open loop at a constant duty cycle and input voltage, and others if it operates in a closed loop at a constant voltage conversion ratio and input voltage. Borders can always be calculated by equaling the voltage conversion ratios corresponding to two adjacent conduction modes. An example of the *k*-space for n = 2 is shown in Figure 1, both for open- and closed-loop operation conditions. It can be noted that for n = 2, the *k*-space and the regions in the *k*-space corresponding to each conduction mode have 2 dimensions while the borders between modes have 1 dimension.

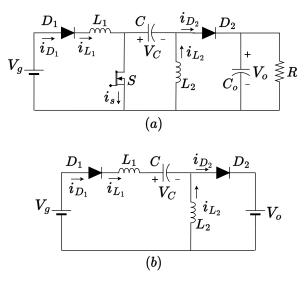


**Figure 1.** Example of the *k*-space for n = 2: (a) open loop, (b) closed loop.

## 3. SEPIC Converter with a Diode at the Input Port

## 3.1. Modified SEPIC Analysis

The SEPIC converter with a diode at the input port is shown in Figure 2a. As mentioned before, the additional diode resembles the operation of a four-diode bridge rectifier connected at its input port, which is the case of using this converter in PFC applications. However, the operation of this converter as PFC needs a deeper analysis, which is beyond the scope of this paper due to the continuous and synchronous variation of the input voltage and the load seen by the converter when it works as a resistor emulator (RE) [17]. Figure 2b shows that there are 2 diodes conducting inductive currents when the transistor is in the blocking state and, therefore, n = 2. Consequently, there will be 4 possible conduction modes, 1 CCM, and 3 DCMs. The vector D will be  $D = (D_1, D_2)$ . Therefore, this converter has the conduction modes listed in Table 1. The waveforms corresponding to each mode are shown in Figure 3.



**Figure 2.** (a) SEPIC converter modified with an additional diode at the input port, (b) equivalent circuit when the transistor is OFF.

<i>D</i> <sub>1</sub>	D <sub>2</sub>	Conduction Mode	Region Name
1	1	CCM	CCM
1	0	DCM	DCM1
0	1	DCM	DCM2
0	0	DCM	DCM3

Table 1. Conduction modes for the modified SEPIC converter.

Some general considerations were made in order to simplify the subsequent calculations. In the conduction mode D = (1, 1), which is the CCM, and D = (1, 0), which is the DCM1, the diode  $D_1$  conducts throughout the entire switching period; consequently, the voltage drop in  $D_1$  is always 0. The average voltage evaluation in the mesh formed by voltage source  $V_g$ , diode  $D_1$ , inductor  $L_1$ , capacitor C, and inductor  $L_2$ , leads to the following conclusion:

$$V_{\rm C} = V_g. \tag{6}$$

In the conduction mode D = (1, 1), which is the CCM, and D = (0, 1), which is the DCM2, the diode  $D_2$  conducts throughout the entire interval, where the transistor is in a blocking state. By applying the volt-second balance to inductor  $L_2$ , we obtain:

$$V_o = \frac{d}{1-d} V_C. \tag{7}$$

In all conduction modes, the average value of currents  $i_{D_1}$  and  $i_{D_2}$ ,  $I_{D_1}$  and  $I_{D_2}$ , respectively, must verify the power balance of the converter. Therefore,

$$I_{D_1} = \frac{V_o I_{D_2}}{V_g} = \frac{V_o^2}{RV_g}.$$
(8)

As the average value of the current passing through capacitor  $C_0$  is zero, the average value of  $i_{L_2}$ ,  $I_{L_2}$ , satisfies:

$$I_{L_2} = I_{D_2} = \frac{V_o}{R}.$$
 (9)

In the conduction modes, where diode  $D_1$  stops conducting during the interval when the transistor is in the blocking state, the peak value of current  $i_{D_1}$  can be computed from Faraday's law as follows:

$$T_{D_{1p}} = \frac{V_g}{L_1} dT,$$
 (10)

therefore, the average value of current  $i_{D_1}$  will be:

$$I_{D_1} = \frac{1}{2} i_{D_{1p}} (d + d_1).$$
(11)

Equations (10) and (11) are valid for case D = (0, 1), which is the DCM2, and for case D = (0, 0), which is the DCM3.

In the next subsection, the conduction modes and the borders between modes of this converter will be studied exhaustively.

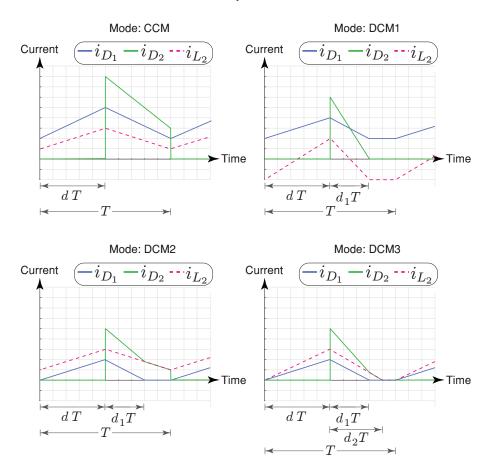


Figure 3. Current waveforms in each conduction mode.

## 3.2. Voltage Conversion Ratio in CCM

The conversion ratio in this mode is very well-known:

$$N = \left[\frac{V_o}{V_g}\right]_{CCM} = \frac{d}{1-d}.$$
(12)

### 3.3. Voltage Conversion Ratio in DCM1

This mode coincides with the only DCM that exists in the conventional SEPIC converter, i.e., without diode  $D_1$ . In this situation, it is also well known [18,19] that the voltage conversion ratio is:

$$M_{1} = \left[\frac{V_{o}}{V_{g}}\right]_{DCM1} = \frac{d}{\sqrt{\frac{k_{1}k_{2}}{k_{1}+k_{2}}}},$$
(13)

where,

$$k_1 = \frac{2L_1}{RT},$$

$$k_2 = \frac{2L_2}{RT}.$$
(14)

## 3.4. Voltage Conversion Ratio in DCM2

This is a new mode that appears after the inclusion of diode  $D_1$ . In this case, Equation (6) is not satisfied. However, Equation (7) is satisfied in this case. The average voltage evaluation in the mesh formed by the source  $V_g$ , diode  $D_1$ , inductor  $L_1$ , and transistor *S* leads to the following conclusion:

$$d_1 = d \frac{V_g}{V_o + V_C - V_g}.$$
 (15)

Using (7), (8), (10), (11) y (15), the voltage conversion ratio can be obtained:

$$M_2 = \left[\frac{V_o}{V_g}\right]_{DCM2} = \frac{k_1 + \sqrt{k_1(4+k_1)}}{2k_1}d.$$
 (16)

## 3.5. Conversion Ratio in DCM3

In this conduction mode, the currents passing through both inductors start from zero. Applying a charge balance on capacitor *C*, it can be obtained:

$$d_1 = \frac{L_1}{L_2} \frac{V_C}{V_g} d.$$
 (17)

Applying Faraday's Law, the peak value of the current  $i_{L_2}$  is easily obtained:

$$i_{L_{2p}} = \frac{V_C}{L_2} dT.$$
 (18)

The triangular waveform of  $i_{L_2}$  in this mode determines:

$$I_{L_2} = \frac{1}{2} i_{L_{2p}} (d + d_2).$$
<sup>(19)</sup>

where  $d_2$  is the duty cycle of the diode  $D_2$ . By applying the volt-second balance to inductor  $L_2$ , the following relationship between  $d_2$  and the converter duty cycle can be achieved:

$$d_2 = \frac{V_C}{V_o} d. \tag{20}$$

After several algebraic operations, from Equations (9), (18)–(20), we obtain:

$$V_C = \frac{-d + \sqrt{d^2 + 4k_2}}{2d} V_o.$$
 (21)

Using Equations (15), (17), and (21), we obtain:

$$M_{3} = \left[\frac{V_{o}}{V_{g}}\right]_{DCM3} = \frac{A + \sqrt{A^{2} + \frac{16k_{2}^{2}}{k_{1}}}}{4k_{2}}d,$$
(22)

where,

$$A = -d + \sqrt{d^2 + 4k_2}.$$
 (23)

#### 3.6. Open-Loop CCM Borders

To calculate the borders between regions in the  $k_1k_2$  plane when the converter operates in an open loop, the first step is to find the borders of the CCM with the remaining modes, which will be achieved by equaling the conversion ratio expressed by (12) and those corresponding to the other modes. Thus, the border with DCM1 is obtained equaling N and  $M_1$ :

$$k_{2\_crit\_0-1\_OL} = \frac{k_1(1-d)^2}{k_1 - (1-d)^2}.$$
(24)

In the same way, to find the border with the region of the DCM2 mode, N and  $M_2$  will be equalized, obtaining:

$$k_{1\_crit\_0-2\_OL} = \frac{(1-d)^2}{d}.$$
(25)

The curves corresponding to (24) and (25) converge at the point  $P_c = (k_{1c}, k_{2c})$ , whose coordinates are:

$$k_{1c} = \frac{(1-d)^2}{d},$$

$$k_{2c} = (1-d).$$
(26)

Therefore, the region corresponding to the CCM is delimited by the points  $(k_1, k_2)$  that simultaneously satisfy:

$$k_{1} > k_{1\_crit\_0-2\_OL}, k_{2} > k_{2\_crit\_0-1\_OL}.$$
(27)

### 3.7. Borders of the DCM3 in an Open Loop

The furthest mode from CCM is DCM3. Its borders with DCM2 are obtained by equaling  $M_2$  and  $M_3$  in (16) and (22):

$$k_{2\_crit\_2-3\_OL} = (1-d).$$
<sup>(28)</sup>

Similarly, the borders between DCM3 and DCM1 can be calculated, obtaining:

$$k_{1\_crit\_1-3\_OL} = k_2 \frac{-d + \sqrt{d^2 + 4k_2}}{2d}.$$
(29)

It can be easily verified that the curves corresponding to (28) and (29) also converge at point  $P_c$ . Therefore, this point is really the center of the map of regions since it is the point common to all of them. Therefore, the region corresponding to DCM3 is delimited by the points ( $k_1$ ,  $k_2$ ) of the positive quadrant that simultaneously fulfill the following inequalities:

$$k_{1} < k_{1\_crit\_1-3\_OL} < \frac{(1-d)^{2}}{d},$$

$$k_{2} < k_{2\_crit\_2-3\_OL}.$$
(30)

The map of regions shown in Figure 4a is easily drawn with the previous information. In this map, the trajectories of the converter can be represented, as seen in Figure 4b. The trajectories correspond to the following equation:

$$k_2 = \alpha k_1, \tag{31}$$

where  $\alpha$  is the trajectory slope, also defined as  $\alpha = \frac{L_2}{L_1}$ . There are 2 types of possible trajectories:

- If  $\alpha > \frac{d}{1-d}$ , then the trajectory is one of the types of CCM-DCM2-DCM3-DCM1.
- If  $\alpha < \frac{d}{1-d}$ , then the trajectory is one of the types of CCM-DCM1.

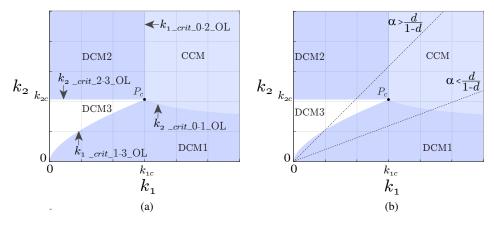


Figure 4. (a) Map of conduction regions in an open loop, (b) possible trajectories.

## 3.9. Closed-Loop Duty Cycle Values for Given Voltage Conversion Ratios

From the voltage conversion ratios given by Equations (12), (13), (16), and (22), the duty cycle equations can be obtained as functions of the conversion ratios,  $k_1$  and  $k_2$ . The resulting equations are the following:

$$d_{CCM} = \frac{N}{1+N'}$$
(32)

$$d_{DCM1} = M_1 \sqrt{\frac{k_1 k_2}{k_1 + k_2}},\tag{33}$$

$$d_{DCM2} = \frac{-k_1 + \sqrt{k_1(4+k_1)}}{2} M_2.$$
(34)

The mathematical expression of  $d_{DCM3}$  can be obtained by solving Equation (22) for *d*.

### 3.10. Closed-Loop Borders

These borders are obtained by equaling the duty cycles corresponding to adjacent regions. Calling *M* the voltage conversion ratio, the following relationships can be derived:

$$k_{2\_crit\_0-1\_CL} = \frac{k_1}{(1+M)^2 k_1 - 1},$$
(35)

$$k_{1\_crit\_0-2\_CL} = \frac{1}{M(M+1)},$$
(36)

$$k_{2\_crit\_1-3\_CL} = Mk_1, (37)$$

$$k_{2\_crit\_2-3\_CL} = 1 - \frac{-k_1 + \sqrt{k_1(4+k_1)}}{2}M.$$
(38)

## 3.11. Closed-Loop Region Maps

The closed-loop region maps and trajectories shown in Figure 5 can be easily drawn with the information provided by (35)–(38). The point of convergence of the regions can be expressed as a function of M, where:

$$k_{1c} = \frac{1}{M(M+1)},$$

$$k_{2c} = \frac{1}{M+1}.$$
(39)

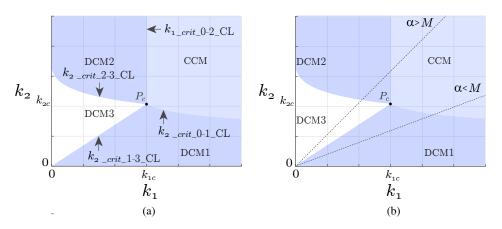


Figure 5. (a) Map of conduction regions in closed loops, (b) possible trajectories.

There are 2 types of trajectories:

- If  $\alpha > M$ , then the trajectory is one of the types of CCM-DCM2-DCM3.
- If  $\alpha < M$ , then the trajectory is one of the types of CCM-DCM1.

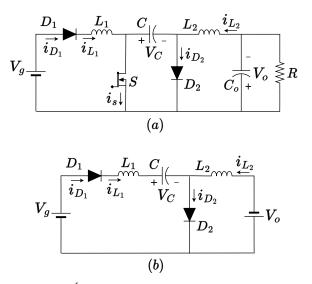
### 4. Ćuk Converter with a Diode at the Input Port

As in the case of the SEPIC converter, an additional diode can be connected in series with the input inductor of a Ćuk converter, as shown in Figure 6. When the transistor is in the OFF state, 2 diodes are placed in inductive branches, thus allowing multiple DCMs. As n = 2, then 4 conduction modes, 1 CCM, and 3 DCMs are possible, which was the same for the SEPIC converter previously studied. Therefore, the conduction modes shown in Table 1 and the waveforms shown in Figure 3 are also valid for the Ćuk converter with input diodes. In this section, the different conduction modes of the modified Ćuk are studied.

It should be noted that some of the equations already presented for the SEPIC converter are also valid for the Ćuk converter. Such is the case of (8), (10), and (11). On the other hand, other equations are not valid for the analysis of the Ćuk converter. This is the case of (15), which corresponds to computing the diode  $D_1$  duty cycle for modes DCM2 and DCM3. As diode  $D_1$  stops conducting earlier than diode  $D_2$  in mode DCM3, the volt-second balance applied to inductor  $L_1$  leads to:

$$d_1 = \frac{V_g}{V_c - V_g} d. \tag{40}$$

After these general considerations, the voltage conversion ratios of each conduction mode can be easily deduced.



**Figure 6.** (a) Ćuk modified converter with a diode at the input port, (b) equivalent circuit when the transistor is OFF.

## 4.1. Voltage Conversion Ratio in CCM

In the CCM, the additional diode  $D_1$  is always conducting and, therefore, the converter behaves as a standard Ćuk converter. Consequently, (12) is also valid for the modified Ćuk converter.

### 4.2. Voltage Conversion Ratio in DCM1

Due to the same reason, (13) is also valid for the modified Ćuk converter.

## 4.3. Voltage Conversion Ratio in DCM2

Applying the volt-second balance to inductor  $L_2$ , we obtain:

$$V_c = \frac{V_o}{d}.\tag{41}$$

Using (8), (10), (11), (40), and (41), it is easily obtained (16). Therefore, as in the two previous cases, the voltage conversion ratio in DCM2 is the same for the SEPIC and Ćuk converter.

### 4.4. Voltage Conversion Ratio in DCM3

Applying a charge balance on the capacitor *C* in this mode, we obtain:

$$d_1 = \frac{L_1}{L_2} \frac{V_C - V_o}{V_g} d.$$
 (42)

Applying the volt-second balance to inductor  $L_2$ , we obtain:

$$d_2 = \frac{V_C - V_o}{V_o} d.$$
 (43)

From Faraday's law, the peak value of the current  $i_{L_2}$  is easily obtained:

$$i_{L_{2p}} = \frac{V_C - V_o}{L_2} dT.$$
 (44)

After some algebraic operations, the value of  $V_C$  is easily obtained from Equations (9), (19), (43), and (44):

$$V_{\rm C} = \frac{d + \sqrt{d^2 + 4k_2}}{2d} V_o. \tag{45}$$

Using Equations (40), (42), and (45), we obtain (22). Therefore, the voltage conversion ratio for the SEPIC and the Ćuk converter also coincide when both converters are operating in DCM3.

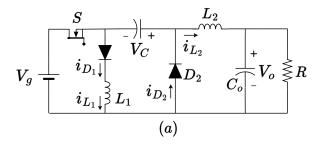
### 4.5. Analysis of Results

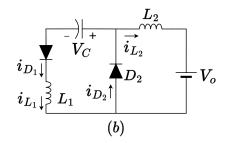
As verified in previous sub-sections, the equations corresponding to the voltage conversion ratio for the modified SEPIC converter and the modified Ćuk converter always coincide, whatever the conduction mode is. Since both converters have the same equations for each of the 4 possible conduction modes, the borders between modes, and the maps of the conduction regions (in both open and closed loops) will coincide for both converters. Thus, Figures 4 and 5 are valid not only for the modified SEPIC converter but also for the modified version of the Ćuk converter.

# 5. The Case of the Zeta Converter with an Extra Diode in Series with the Intermediate Inductor

The studies presented in the previous sections show that the modified versions of the SEPIC and Ćuk converters have the same maps of conduction regions in both open and closed loops. In both cases, the additional diode connected in series with the inductor at the converter input port could represent the unidirectional current effect of a four-diode bridge rectifier connected at the input port when these converters work as PFCs. As mentioned before, the study of these converters working as PFCs is beyond the scope of this paper due to its complexity [17]; the study presented here is the first step toward that objective.

On the other hand, it is well known that the Zeta converter belongs to the family of high-order buck-boost converters. As this converter does not have an inductor in the input port, the connection of a four-diode bridge rectifier at the input port does not modify the conduction modes. To have extra conduction modes, a diode must be connected in series with the intermediate inductor, as shown in Figure 7. This modification of the standard topology neither improves the converter characteristics nor resembles its practical use in a specific application. However, a detailed study of the modified Zeta converter concludes that all of the aforementioned conclusions regarding the modified versions of the SEPIC and Ćuk converters can extend to the modified version of the Zeta converter.





**Figure 7.** (a) Zeta-modified converter a with diode at the input port  $L_2$ , (b) equivalent circuit when the transistor is OFF.

## 6. Other Common Characteristics of the Modified SEPIC, Ćuk, and Zeta Converters

The main conclusion from the previous sections is that the modified versions of the SEPIC, Ćuk, and Zeta converters given in Figures 2, 6 and 7 have identical region maps

in open and closed loops, as shown in Figures 4 and 5. Moreover, it is also possible to obtain some characteristic curves of these converters when operating in open and closed loops from the analyses carried out in the previous sections. These characteristic curves are introduced in the following subsections.

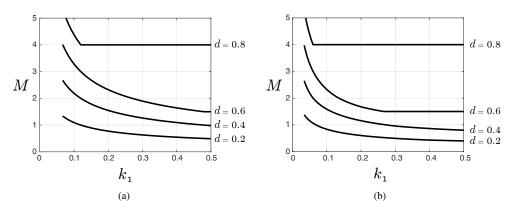
#### 6.1. Families of Open-Loop Characteristic Curves with Constant Duty Cycle

The relationships between M and k were plotted on the  $Mk_1$  plane for each value of the duty cycle d and for a given value of the inductor ratio  $\alpha$ . It should be noted that  $k_1$  is inversely proportional to R, which means that the obtained plots are representations of the variations of the voltage conversion ratios when the normalized output conductance changes. A couple of examples of these plots are shown in Figure 8. As previously mentioned, there are 2 types of possible trajectories, depending on the d value. Thus, the trajectory will be CCM-DCM2-DCM3-DCM1 if:

$$d < \frac{\alpha}{1+\alpha}.\tag{46}$$

Otherwise, the trajectory will be CCM-DCM1 if:

$$d > \frac{\alpha}{1+\alpha}.\tag{47}$$



**Figure 8.** Families of open-loop characteristic curves with constant duty cycles: (a) case  $\alpha = \frac{1}{2}$ , (b) case  $\alpha = 2$ .

Regarding the plot shown in Figure 8a,  $\alpha = \frac{1}{2}$  and, therefore, the output characteristics correspond to a trajectory of CCM-DCM2-DCM3-DCM1 when  $d < \frac{1}{3}$  and to a trajectory of CCM-DCM1 when  $d > \frac{1}{3}$ . On the other hand,  $\alpha = 2$  in Figure 8b, which means a trajectory of CCM-DCM2-DCM3-DCM1 when  $d < \frac{2}{3}$  and a trajectory of CCM-DCM1 when  $d > \frac{2}{3}$ . In all cases, the values of  $k_1$  corresponding to a border between conduction modes can be easily deduced from Equations (24), (28), (29), and (31). These values are:

$$k_{1\_crit\_0-1\_OL} = \frac{1+\alpha}{\alpha} (1-d)^2,$$
(48)

$$k_{1\_crit\_2-3\_OL} = \frac{1}{\alpha}(1-d), \tag{49}$$

$$k_{1\_crit\_1-3\_OL} = \frac{1+\alpha}{\alpha^3} d^2.$$
 (50)

The border between the CCM and the DCM2,  $k_{1_{crit}_{0}-2_{OL}}$ , is directly given by (25).

#### 6.2. Families of Closed-Loop Characteristic Curves with a Constant Conversion Ratio

Regarding the operation in a closed loop, a similar process can be followed. The relationship between d and  $k_1$  can be plotted on the  $dk_1$  plane for each value of the voltage

conversion ratio M and for a given value of the inductor ratio  $\alpha$ . Moreover, a few examples of these plots are shown in Figure 9. There are also 2 types of possible trajectories, depending on the M value. The trajectory will be CCM-DCM2-DCM3 if:

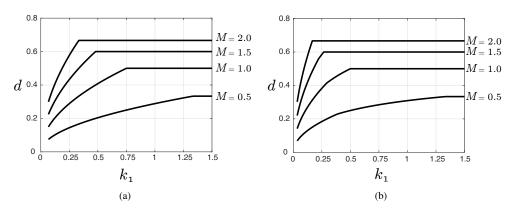
Λ

М

$$\Lambda < \alpha. \tag{51}$$

Otherwise, the trajectory will be CCM-DCM1 if:

$$> \alpha.$$
 (52)



**Figure 9.** Families of closed-loop characteristic curves with a constant conversion ratio: (**a**) case  $\alpha = \frac{1}{2}$  and (**b**) case  $\alpha = 2$ .

Regarding the plot shown in Figure 9a,  $\alpha = \frac{1}{2}$ ; therefore, the output characteristics correspond to a trajectory of CCM-DCM2-DCM3 when  $M < \frac{1}{2}$  and to a trajectory of CCM-DCM1 when  $M > \frac{1}{2}$ . On the other hand,  $\alpha = 2$  in Figure 9b, which means a trajectory of CCM-DCM2-DCM3 when M < 2 and a trajectory of CCM-DCM1 when M > 2.

As in the case of open loop operations, the values of  $k_1$  corresponding to the borders between CCM and DCM1 and between DCM2 and DCM3 can be easily deduced from Equations (31), (35), and (38). These values are:

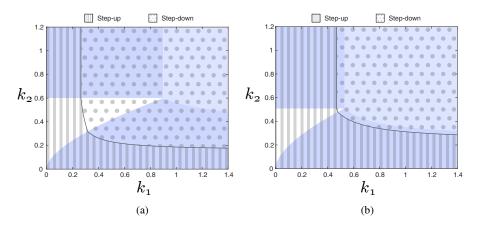
$$k_{1\_crit\_0-1\_CL} = \frac{1+\alpha}{\alpha(1+M)^2},$$
(53)

$$k_{1\_crit\_2-3\_CL} = \frac{M^2 - M + 2\alpha - M\sqrt{(M-1)^2 + 4\alpha}}{2\alpha(\alpha - M)}.$$
(54)

The border between the CCM and the DCM2,  $k_{1\_crit\_0-2\_CL}$ , is directly given by (36). Finally, It should be noted that a transition between DCM1 and DCM3 is not possible, as Figure 5b shows.

#### 6.3. Border between Step-Down and Step-Up Modes at a Constant Duty Cycle

Converters belonging to the buck-boost family can operate in a step-down mode or a step-up mode. When operating in the CCM, these converters always work in a step-down mode if d < 0.5 However, the voltage conversion ratio of these converters increases when they start working in any DCM, as Figure 8 shows. Therefore, they can operate in a step-up mode when d < 0.5 if they are working in any of the DCMs at proper values of  $k_1$  and  $k_2$ . Consequently, the operating regions in a step-down mode and a step-up mode can be delimited in the maps of regions in the  $k_1k_2$  planes corresponding to work in an open loop with d < 0.5. The boundary between the step-down mode and step-up mode will be easily obtained by replacing  $M_x$  with 1 in (13), (16), and (22). The results of this action are three curves, one for each DCM (i.e., the border between step-down mode and step-up mode in each region). Figure 10 shows two examples, one for d = 0.4 and the other for d = 0.49. As



d = 0.49 is very close to the limit value d = 0.5, the main part of the points in DCM regions belongs to the step-up mode in this case.

**Figure 10.** Step-down and step-up borders with constant duty cycles: (a) d = 0.4, (b) d = 0.49.

## 7. Experimental Results

The validation of the analysis presented in the previous sections was carried out in the setup shown in Figure 11. A reconfigurable prototype of 200 W was built to implement SEPIC and Ćuk converters. We present the description of the power converter components in Table 2. The inductor values were  $L_1 = L_2 = 47 \mu$ H, which means  $\alpha = 1$  in this design. The same tests were performed on the SEPIC and Ćuk converters in order to verify the common characteristics identified in these high-order buck-boost converters. These tests were carried out both in open-loop and closed-loop conditions at constant input voltages. In open-loop operations, the duty cycle was constant, whereas, in the closed-loop operations of the voltage conversion ratio, the quantity was constant during the tests. Duty cycles and voltage conversion ratios were conveniently selected to obtain the 2 possible types of trajectories for each control loop operation. The results were duty cycles 0.4 and 0.6 and voltage conversion ratios 0.7 and 1.4. On the other hand, the values of the load resistor were selected to operate in points placed in each region, far from the borders. The operation points and their corresponding theoretical powers are shown in Table 3. The input voltage and the switching period remained constant in all of the tests:  $V_g = 10 \text{ V}$ ,  $T = 10 \mu$ s.

Table 2. Component description of the built prototype.

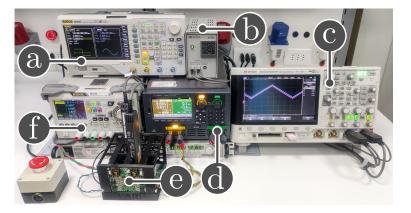
Component	Description	Туре
S	Power MOSFET	IRFB4510PBF
$D_1, D_2$	Diode	Schottky Power MBR60H100CTG
$L_1, L_2$	Inductor	Wurth Elektronik 74435584700, 47 µH
$C_1, C_2$	Multilayer Ceramic Capacitor	TDK C5750X7S2A106M230KB, 10 µF

Table 3. Operation points tested in SEPIC and Ćuk converters.

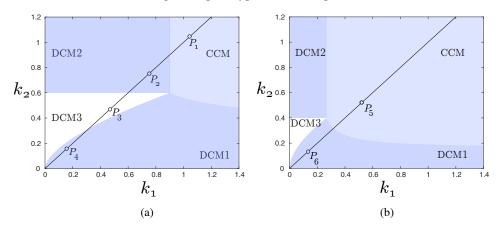
Operatior Mode	ı	Open Loop				Closed Loop					
Ratio		d = 0.4			d = 0.6		M = 0.7			M = 1.4	
Point	$P_1$	$P_2$	$P_3$	$P_4$	$P_5$	$P_6$	$P_7$	$P_8$	$P_9$	$P_{10}$	$P_{11}$
$R[\Omega]$	9	12.5	20	60	18	70	9.5	13	20	18	35
Power[W]	4.9	3.9	3.6	3.4	12.4	7.7	5.1	3.8	2.5	10.8	5.6

The operation points are shown in Figures 12 and 13. The ones corresponding to the open-loop control are given in Figure 12, where two trajectories are considered: the trajectory that satisfies the condition  $\alpha > \frac{d}{1-d}$  is obtained selecting d = 0.4 (see Figure 12a),

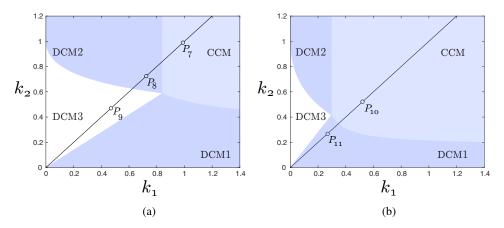
whereas the trajectory that satisfies the condition  $\alpha < \frac{d}{1-d}$  corresponds to d = 0.6 (see Figure 12b). Likewise, Figure 13 shows the corresponding operation points for the closed-loop control: the trajectory of Figure 13a satisfies  $\alpha > M$ , because M = 0.7, whereas the trajectory of Figure 13b satisfies  $\alpha < M$ , since M = 1.4.



**Figure 11.** Experimental setup for testing in SEPIC and Ćuk converters: (**a**) arbitrary waveform generator to program the duty cycles, (**b**) auxiliary power supply to current probes, (**c**) oscilloscope, (**d**) electronic load, (**e**) reconfigurable prototype, and (**f**) DC power source.

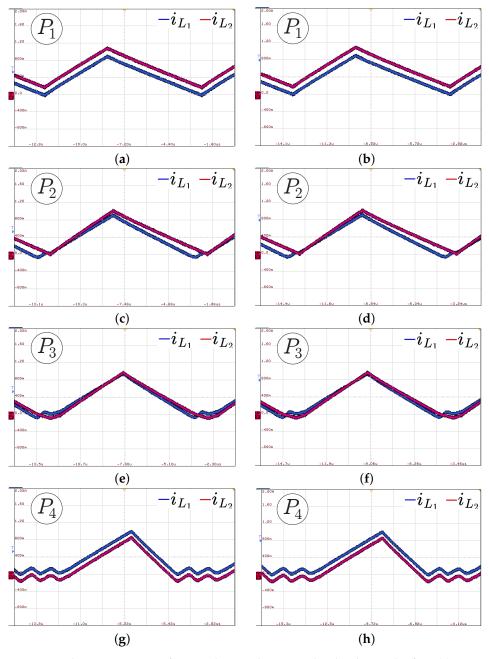


**Figure 12.** Map of the conduction regions in an open loop for either SEPIC or Ćuk converters: (a) d = 0.4 and (b) d = 0.6. The points corresponding to the experimental results are highlighted.

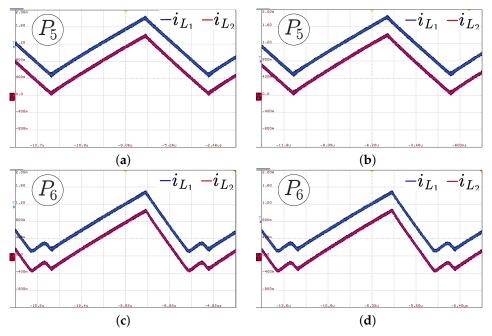


**Figure 13.** Map of conduction regions in closed loops for either SEPIC or Ćuk converters: (**a**) M = 0.7 and (**b**) M = 1.4. The points corresponding to the experimental results are highlighted.

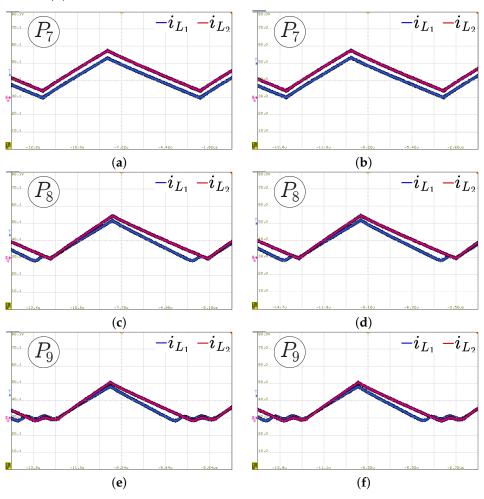
Experimental results in the open-loop operation are shown in Figures 14 and 15, while closed-loop results are depicted in Figures 16 and 17. In each case, the inductor current waveforms obtained for the SEPIC and the Ćuk converter are compared. The waveforms given in Figure 14 for the open loop correspond to d = 0.4, while those of Figure 15 were obtained when d = 0.6. Regarding the closed-loop control, Figure 16 shows waveforms for M = 0.7, whereas Figure 17 shows waveforms for M = 1.4. The comparison of the results obtained shows the same behaviors of the inductor currents for both the SEPIC and Ćuk converters in all operation points. Finally, it should be noted that the experimental waveforms obtained are in good agreement with the theoretical waveforms. Table 4 summarizes the experimental results in a closed loop, where efficiency, current ripple, and voltage conversion ratio are presented for all operation points.



**Figure 14.** Inductor current waveforms in the open-loop control with a duty cycle of 0.4: (a) SEPIC in point  $P_1$ , (b) Ćuk in point  $P_1$ , (c) SEPIC in point  $P_2$ , (d) Ćuk in point  $P_2$ , (e) SEPIC in point  $P_3$ , (f) Ćuk in point  $P_3$ , (g) SEPIC in point  $P_4$ , and (h) Ćuk in point  $P_4$ , (400 mA/div, DC coupling, and a time base of 1.4  $\mu$ s).

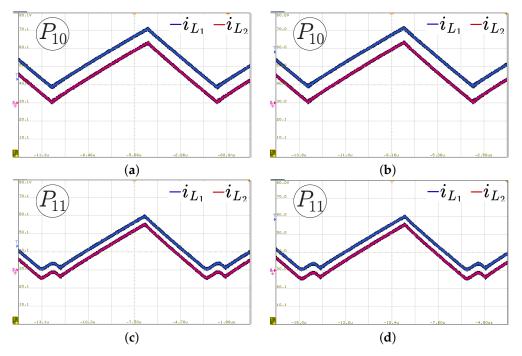


**Figure 15.** Inductor current waveforms in the open-loop control with a duty cycle of 0.6: (a) SEPIC in point  $P_5$ , (b) Ćuk in point  $P_5$ , (c) SEPIC in point  $P_6$ , and (d) Ćuk in point  $P_6$ , (400 mA/div, DC coupling, and a time base of 1.4  $\mu$ s).



**Figure 16.** Inductor current waveforms in the closed-loop control with a voltage conversion ratio of 0.7: (a) SEPIC in point  $P_7$ , (b) Ćuk in point  $P_7$ , (c) SEPIC in point  $P_8$ , (d) Ćuk in point  $P_8$ , (e) SEPIC in point  $P_9$ , and (f) Ćuk in point  $P_9$ , (400 mA/div, DC coupling, and a time base of 1.4 µs).

A further comparison between the experimental results and the theoretical analysis is shown in Figure 18. The voltage conversion ratio at each closed-loop operation point was obtained by applying the duty cycle calculated through the theoretical analysis. Figure 18a shows the results for the SEPIC converter, while Figure 18b shows the results for the Cuk converter. The comparison includes both M = 0.7 and M = 1.4 cases for each converter. It can be seen in Figure 18 how theoretical and experimental results match better for condition M = 0.7. This difference between theoretical and experimental values is a function of the losses in the energy conversion process of the converter, which will be higher as the voltage conversion ratio increases, as it happens for condition M = 1.4.



**Figure 17.** Inductor current waveforms in a closed-loop control with a voltage conversion ratio of 1.4: (a) SEPIC in point  $P_{10}$ , (b) Ćuk in point  $P_{10}$ , (c) SEPIC in point  $P_{11}$ , and (d) Ćuk in point  $P_{11}$ , (400 mA/div, DC coupling, and a time base of 1.4 µs).

	SEPIC				Ćuk			
	Current Ripple [A]		Voltage Efficiency Conversion [%]		Current Ripple [A]		Voltage Conversion	Efficiency [%]
	$\iota_{L_1}$	$\iota_{L_2}$			$\iota_{L_1}$	$\iota_{L_2}$		
$P_7$	0.95	0.95	0.64	89.8	0.95	0.95	0.64	89.5
$P_8$	0.90	1.00	0.66	93.9	0.90	1.00	0.67	94.8
$P_9$	0.75	0.82	0.68	90.0	0.75	0.82	0.68	89.7
$P_{10}$	1.25	1.3	1.29	90.7	1.25	1.30	1.30	91.5
P <sub>11</sub>	1.15	1.15	1.33	83.7	1.15	1.15	1.33	84.2

Table 4. Analysis of the experimental results.



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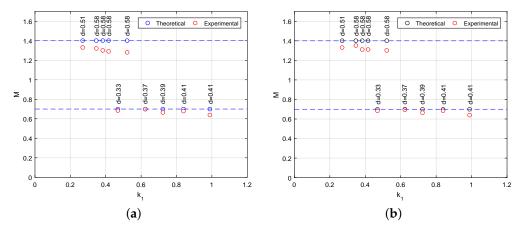


Figure 18. Theoretical and experimental comparison: (a) SEPIC and (b) Ćuk.

#### 8. Conclusions

In this paper, the multiple conduction modes that appear when an additional diode is connected at the input port of the SEPIC and Cuk converters were studied. The study was extended to the Zeta converter, in this case adding the additional diode in series with the intermediate inductor. These converters exhibit 4 conduction modes (1 CCM and 3 DCMs), which can be located in the  $k_1k_2$  plane. The study shows that these modified versions of the SEPIC, Cuk, and Zeta converters present exactly the same maps of the conduction regions in the  $k_1k_2$  plane. This result is valid for both possible types of control strategy (open and closed loops). Another important result is that there is a confluence point of the 4 conduction modes. The position of this confluence point depends on the control strategy. When the load changes, the converter operation point follows a straight line in the  $k_1k_2$ plane, called the trajectory. The trajectories always pass through the origin and their slopes depend on the inductor ratios. There are 2 types of trajectories for each control strategy, depending on the relative position of the confluence point with respect to the trajectory. Thus, one type corresponds to the confluence point on the right side of the trajectory, whereas the other one corresponds to the opposite. Finally, the theoretical predictions resulting from the proposed analysis were experimentally verified in a reconfigurable prototype. Future works will focus on the study of SEPIC and Cuk converters as power factor correctors, operating in the different discontinuous conduction modes identified in this research.

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## Abbreviations

The following abbreviations are used in this manuscript:

CCM	continuous conduction mode
DCM	discontinuous conduction mode
MOSFET	metal-oxide-semiconductor field-effect transistor
PFC	power factor correction
RE	resistor emulator
RHP	right half-plane
RMS	root mean square
SEPIC	single-ended primary-inductor converter
ZCS	zero current switching

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