Universidad de Oviedo

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Tesis Doctoral
Programa de Doctorado en Energía y Control de Procesos

Análisis dinámico y desarrollo de sistemas de control distribuidos en celdas de potencia y convertidores multipuerto para integración en red de recursos distribuidos

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Ph.D. THESIS DISSERTATION

Dynamic analysis and development of distributed control systems in power cells and multiport converters for grid integration of distributed resources

Dissertation submitted in fulfilment of the requirements for the degree of Doctor of Philosophy in the Energy and Process Control PhD program of the University of Oviedo with International Mention

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Universidad de Oviedo
Departamento de Ingeniería Eléctrica, Electrónica, de Comunicaciones y de Sistemas

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TESIS DOCTORAL

Análisis dinámico y desarrollo de sistemas de control distribuidos en celdas de potencia y convertidores multipuerto para integración en red de recursos distribuidos

Tesis presentada en cumplimiento de los requisitos para la obtención del título de Doctor en el programa de doctorado de Energía y Control de Procesos de la Universidad de Oviedo con Mención Internacional

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Gijón, Febrero 2022

A mis padres, hermanos, familia y amigos...

Agradecimientos

Dedicado a mi director de tesis, mis compañeros de universidad, mi familia y mis amigos.

Universidad de Oviedo

RESUMEN DEL CONTENIDO DE TESIS DOCTORAL

1.- Título de la Tesis	
Español: **Análisis dinámico y desarrollo de sistemas de control distribuidos en celdas de potencia y convertidores multipuerto para integración en red de recursos distribuidos**	Inglés: **Dynamic analysis and development of distributed control systems in power cells and multiport converters for grid integration of distributed resources**

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RESUMEN (en español)

El objetivo de esta tesis es el desarrollo de sistemas de control adaptados a convertidores de potencia multipuerto para integración en red de recursos distribuidos. El estudio pretende dar respuesta a un cambio en el paradigma en el diseño de sistemas de control para convertidores de potencia, desde unidades de potencia con un diseño rígido y específico para cada aplicación de generación centralizada hacia implementaciones alternativas con un diseño adaptativo y genérico que pueda ser integrado en múltiples aplicaciones de generación distribuida.

El trabajo desarrollado se centra en la explotación de un convertidor de potencia modular formado a partir de celdas básicas de potencia, a fin de proponer una configuración multipuerto que permita la interconexión de unidades de potencia de diversa naturaleza, la integración con la red eléctrica y el apoyo de sistemas de almacenamiento de energía.
Por tanto, inicialmente, se realiza una revisión de los diferentes diseños de celdas de potencia para determinar la opción más adecuada para la implementación del convertidor.

Una vez seleccionada la configuración del convertidor, se lleva a cabo el modelado matemático del mismo en espacio de estados a partir del modelo promediado de gran señal. El modelo es adecuado para realizar el análisis dinámico del sistema a fin de comprender su comportamiento y posteriormente ser utilizado en el diseño del sistema de control.
Este modelo matemático es validado mediante la comparación con el modelo conmutado del convertidor, obteniéndose unos resultados equivalentes con la ausencia del rizado de alta frecuencia derivado de la conmutación de los interruptores de potencia.
Utilizando la información adquirida a partir del modelo matemático, se establecen los requerimientos para determinar el sistema de control distribuido más adecuado para la explotación del convertidor de potencia modular multipuerto.

Llegados a este punto, se propone una arquitectura de control distribuido para el convertidor multipuerto.
Esta arquitectura se desarrolla para tener en cuenta la configuración modular del convertidor, por lo que sigue una estructura jerárquica formada por diversos controladores distribuidos, los cuales gestionan las tareas de control a nivel de celda de potencia, supeditados a un controlador central, el cual gestiona las tareas de control a nivel de sistema y aplicación.
Los controladores distribuidos a cargo de las celdas de potencia son diseñados para seguir una estructura común y adaptable, con el fin de habilitar la integración de diferentes unidades de potencia en el convertidor sin grandes modificaciones en la arquitectura de control.

Posteriormente, se integra el controlador central en un sistema embebido basado en un microprocesador de propósito general, proporcionando versatilidad, escalabilidad y capacidad computacional al mismo tiempo.

El microprocesador se maneja mediante un sistema operativo Linux para aprovechar su gran soporte y facilitar la ejecución de tareas auxiliares no críticas, junto con una extensión en tiempo real que habilita la ejecución de tareas de control críticas y con restricciones firmes de tiempo real.
La validación del sistema embebido para su integración en el sistema de control se determina analizando la correcta ejecución de tareas en tiempo real, demostrando una operación determinista con un número despreciable de incumplimientos de plazos.

Finalmente, se desarrolla e implementa una aplicación basada en el uso de un convertidor multipuerto controlado mediante el sistema de control distribuido propuesto.
Dicha aplicación permite la operación de una unidad de potencia bidireccional siguiendo un determinado perfil de potencia, bajo restricciones de potencia máxima de red, y con el apoyo de un sistema de almacenamiento de energía híbrido.
Para este propósito, se implementa un algoritmo de reparto de potencia para la integración del sistema de almacenamiento de energía híbrido con el fin de suavizar el perfil de potencia de la red, considerando eventos de saturación y condiciones de aislamiento de red.

RESUMEN (en inglés)

The objective of this thesis is the development of control systems adapted to multiport power converters for grid integration of distributed resources, in order to consider a paradigm shift in the design of control systems for power converters, from power units with a rigid and specific design for each centralized generation application to alternative implementations with an adaptive and generic design that can be integrated in multiple distributed generation applications.

The work developed focuses on the exploitation of a modular power converter formed from basic power cells, in order to propose a multiport configuration that allows the interconnection of power units of different nature, the integration with the electrical grid and the support of energy storage systems.
Therefore, initially, a review of the different power cell designs is performed to determine the most suitable option for the implementation of the converter.

Once the converter configuration has been selected, mathematical modeling in state space is carried out from the large-signal average model. The model is suitable for conducting dynamic analysis to understand its behavior and later to be used in the control system design.
This mathematical model is validated by comparison with the converter switching model, obtaining equivalent results with the absence of the high-frequency ripple resulting from the switching.
Using the information acquired from the mathematical model, the requirements to determine the most suitable distributed control system for the operation of the multiport modular power converter are established.

At this point, a distributed control architecture for the multiport converter is proposed.
This architecture is developed to take into account the modular configuration of the converter, so it follows a hierarchical structure formed by several distributed controllers, which manage the control tasks at power cell level, subordinated to a central controller, which manages the control tasks at system and application level.
The distributed controllers in charge of the power cells are designed to follow a common and adaptable structure, in order to enable the integration of different power units in the converter without major modifications in the control architecture.

Afterwards, the central controller is integrated into an embedded system based on a general-purpose microprocessor, providing versatility, scalability and computational capacity at the same time.
The microprocessor is handled by a Linux operating system to take advantage of its wide support and facilitate the execution of non-critical auxiliary tasks, together with a real-time extension that enables the execution of critical and firm real-time control tasks.
The validation of the embedded system for its integration into the control system is determined by analyzing the correct execution of tasks in real time, demonstrating a deterministic operation

with a negligible number of missed deadlines.

Finally, an application based on the use of a multiport converter controlled by the proposed distributed control system is developed and implemented.
This application allows the operation of a bidirectional power unit following a given power profile, under maximum grid power constraints, and with the support of a hybrid energy storage system.
For this purpose, a power sharing algorithm is implemented for the integration of the hybrid energy storage system in order to smooth the grid power profile, considering saturation events and islanding conditions.

SR. PRESIDENTE DE LA COMISIÓN ACADÉMICA DEL PROGRAMA DE DOCTORADO EN ENERGÍA Y CONTROL DE PROCESOS

Resumen

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Abstract

The objective of this thesis is the development of control systems adapted to multiport power converters for grid integration of distributed resources, in order to consider a paradigm shift in the design of control systems for power converters, from power units with a rigid and specific design for each centralized generation application to alternative implementations with an adaptive and generic design that can be integrated in multiple distributed generation applications.

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Abbreviations and acronyms

1ph	Single-Phase
3L	Three-Level
3ph	Three-Phase
5L	Five-Level
AC	Alternating Current
ACK	Acknowledge
A/D	Analog-To-Digital
ANN	Artificial Neural Network
ANPC	Active NPC
API	Application Programming Interface
C^3S	Common Cross-Connected Stage
CAES	Compressed Air Energy Storage
CAN	Controller Area Network
CAN FD	CAN Flexible Data-Rate
CM	Compute Module
CNT	Controllable Network Transformer
CRC	Cyclic Redundancy Check
CPU	Central Processing Unit
DC	Direct Current
DPS	Distribution Power System
DRC	Direct RC
DSP	Digital Signal Processor
DVC	Direct Voltage Control
ESS	Energy-Storage System

EtherCAT	Ethernet for Control Automation Technology
FACTS	Flexible AC Transmission System
FC	Fuel Cell
FESS	Flywheel ESS
FFT	Fast Fourier Transform
FLC	Fuzzy Logic Control
FLL	Frequency Locked Loop
GPU	Graphics Processing Unit
GUI	Graphical User Interface
HAL	Hardware Abstraction Layer
HDMI	High-Definition Multimedia Interface
HES	High-Energy Storage
HESS	Hybrid ESS
HMI	Human-Machine Interface
HPF	High-Pass Filter
HPS	High-Power Storage
HV	High Voltage
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
IDE	Integrated Development Environment
IMU	Impedance Measurement Unit
IoT	Internet of Things
IP	Internet Protocol
IPC	Inter-Process Communication
iPEBB	Intelligent PEBB
IRQ	Interrupt Request
LC	Inductor-Capacitor
LPF	Low-Pass Filter
LV	Low Voltage
MF	Multi-Fed
MMC	Modular Multilevel Converter
MNPC	Mixed-Voltage NPC
MPC	Model Predictive Control

MV	Medium Voltage
NMT	Network Management
NPC	Neutral-Point Clamped
OS	Operating System
OSI	Open Systems Interconnection
PCB	Printed Circuit Board
PCC	Point of Common Coupling
PDO	Process Data Object
PEBB	Power Electronics Building Block
PET	Power Electronic Transformer
PFC	Power Factor Correction
PI	Proportional-Integral
PLL	Phase-Locked Loop
POSIX	Portable Operating System Interface
PR	Proportional-Resonant
PSH	Pumped Storage Hydropower
PSO	Particle Swarm Optimization
PWM	Pulse-Width Modulation
QSG	Quadrature Signal Generator
QVC	Quadratic Voltage Control
RAM	Random Access Memory
RBC	Rule-Based Control
RC	Repetitive Controller
RPi	Raspberry Pi
RT	Real-Time
RTR	Remote Transmission Request
SDO	Service Data Object
SFLA	Shuffled Frog-Leaping Algorithm
SOGI	Second-Order Generalized Integrator
SMC	Sliding Mode Control
SMES	Superconducting Magnetic Energy Storage
SOC	State Of Charge
SPI	Serial Peripheral Interface

STATCOM	Static Synchronous Compensator
SVR	Second Voltage Regulation
SYNC	Synchronization
TCP	Transmission Control Protocol
TEES	Thermo-Electric Energy Storage
THD	Total Harmonic Distorsion
UART	Universal Asynchronous Receiver-Transmitter
UI	User Interface
USB	Universal Serial Bus
VCD	Virtual Capacitance Droop
VRD	Virtual Resistance Droop
VSC	Voltage Source Converter
WCA	Water Cycle Algorithm
WiMAX	Worldwide Interoperability for Microwave Access
ZCT	Zero-Current Transition
ZPS	Zero-Phase-Shift
μP	Micro-Processor

Contents

Chapter 1

Introduction

1.1 Background and motivation

Traditionally, the generation of electrical energy was carried out in large plants in a centralized manner, in order to take advantage of the characteristics of fossil and nuclear fuels. This is due to the fact that the thermal processes produced with this type of technology obtain better performance in conjunction with a larger plant size. In addition, the extraction of the raw material to carry out the combustion/fission process is located in those areas where there is availability, which further encourages centralization.

Nevertheless, with the course of the last years, there has been an increasing development of renewable energies, which are based on energy sources with different characteristics from the traditional ones. These renewable energy sources (sun, wind) are considered virtually inexhaustible and are available in all places to a greater or lesser extent. Due to the integration of this type of sources in the energy mix, there is an evolution from a centralized model to an increasingly distributed model. In this model, the aim is to generate electricity close to where it will be consumed, in order to make it more accessible, favour self-consumption, reduce distribution costs and allow operation in the event of disconnections from the electrical grid.

All this entails a modification of the power converter topologies in order to adapt to distributed generation and take advantage of all its benefits. Traditional power converters are specifically designed to fulfill a particular purpose in the most efficient way and, therefore, they are not very customizable. In a centralized and rigid model of electricity generation, whose requirements are well known and little modifiable, this type of converter allows cost savings. However, taking into account that their adaptation capacity is reduced, it makes them less suitable for a distributed generation model, where generation requirements are more changeable. This is where modular power converters come into play.

A modular power converter consists of a series of power cells that joined together and configured in a certain way carry out a certain purpose. Thus, depending on the arrangement of the cells and the programming implemented in each of them, the converter can vary its behavior and adapt to the needs of each moment. Therefore, this type of converter provides the advantage of having great flexibility, since a repositioning and reprogramming of these cells would allow you to vary its purpose without further cost. This feature is appealing to carry out the development of distributed generation, due to the continuous evolution it is undergoing.

In addition to flexibility, the use of power cells to form the modular converter provides other advantages. On the one hand, it facilitates the scalability of the system as it allows to increase the voltage and current rating of the converter by adding more cells in series or parallel. On the other hand, the reliability of the converter can be improved by adding redundant cells to the existing ones, which could hot-swap one of the main cells in case there is a failure in them.

Renewable energy sources are considered to be inexhaustible but some of them cannot guarantee uninterrupted power generation due to their dependence on resources with variable availability. This is the case for any generator based on solar or wind energy, as the sun and wind are influenced by weather, seasonal and climatic conditions. Therefore, the controllability of the power generated from these types of sources is limited and subject to environmental conditions. This phenomenon is even more aggravated when power consumption profiles are taken into account, since consumption peaks do not always coincide with the most favorable sun and wind conditions.

To mitigate the problem, the development and introduction of energy storage devices in power systems is being encouraged, with a wide range of possibilities available: electrochemical (batteries), electrical (supercapacitors), kinetic (flywheels), gravitational (pumping). This way, surplus power generation can be stored in periods of higher supply or lower demand (off-peak hours) for use in periods of lower supply or higher demand (peak hours). Therefore, the integration of all the power devices belonging to a distributed generation system entails the need for power converters with multiple connection points to manage all the sources and loads, as well as auxiliary energy storage elements to improve system performance.

At this point, the concept of the multiport power converter arises, a device that provides multiple connection ports to interconnect various power units and integrate them into the electrical grid. Following a modular development, a multiport power converter can be formed by connecting a specific number of power cells depending on the number of distributed resources to be integrated into the grid. Therefore, unlike more conventional converter topologies, the control system of a multiport converter requires a high number of inputs/outputs to be able to interact with all the power cells that make up the converter and, in addition, a large computational capacity necessary to ensure the correct execution of the control algorithms within specified time ranges.

To address this issue, a single high-performance digital controller can be used to provide a sufficient number of hardware resources to handle the number of inputs

and outputs required by the application. In this way, the entire control algorithm would be implemented in this device, taking care of the complete management of the multiport power converter. However, this solution conflicts with the modularity concept put forward for the integration of distributed resources, since the integration of the control system in a single device hinders scalability, especially in terms of having enough resources available to handle all the required inputs and outputs. While it is true that the digital controller could be oversized to meet future needs and facilitate the scalability of the converter, this would imply a non-optimal design with limitations on the maximum number of inputs and outputs.

Following a modular design, it is possible to distribute part of the control system within each of the power cells that form the modular multiport converter, by integrating cost-effective digital controllers within each of the cells for the implementation of specific control algorithms for autonomous management. This means that the high-performance digital controller of the control system is freed from having a large number of inputs and outputs, which are now distributed within the local cell controllers, taking care of coordinating the operation of the cells with a global approach at the converter level. Thus, greater scalability is achieved for the multiport converter, making it easier to upgrade the converter for the integration of new power units.

The motivation for this work arises from the lack of distributed control systems for the management of modular power converters based on power cells. For this purpose, the proposal in this thesis is to transform the power cell into an intelligent one by introducing a local control system, allowing self-management for the internal control variables. Improving the performance of the power cell in this respect facilitates the development of multiport converters capable of handling multiple power units of different nature without requiring bespoke hardware designs for the central control system. This could potentially bring an improved integration of distributed generation systems with hybrid energy storage systems.

However, the implementation of a multiport converter based on intelligent power cells with a distributed control system involves a number of challenges that must be considered. First, it is desirable to have a single power cell implementation that is capable of configuring all power conversions required by the multiport converter through cell replication. Moreover, the development of a distributed control system requires the integration of a digital controller for each cell, which must be conveniently programmed to perform the local autonomous control. Local control must be designed to be versatile enough to enable the use of the cell for different power topologies.

In addition, the introduction of multiple connection ports to handle as many power units as necessary places increasing requirements on the number of inputs and outputs managed by the control system of the converter. Since these inputs/outputs are distributed among the local controllers of the power cells, the control system becomes more complex to optimally operate the resources available in the cells. Thus, although the power cells have their own controller for self-management, a higher control layer is necessary to synchronize all of them for establishing the global operation of the converter. This results in ever-increasing computational requirements and the need for

high performance communication channels, issues addressed during the development of the thesis.

1.2 Thesis objectives

The main objective of this work is the development of a distributed control system architecture for the operation of modular power converters formed from the combination of multiple power cells, with the final purpose of controlling multiport converters capable of integrating distributed resources. For this purpose, the distributed control system is designed to manage power converter topologies based on the interconnection of several units of an unique power cell which consists of a specific set of active and passive elements necessary for the utilization of the cell in different power conversion scenarios. In addition, to meet the requirements of different applications, a programmable control system will be integrated into the cell itself, providing it with greater intelligence and adaptability. In order to achieve all above, the following objectives are defined:

I. A state-of-the-art review related to the thesis motivation and the corresponding objectives, covering the following topics:

   - Review of modular power converters based on the development of a power cell, considering different converter configurations and applications where this concept is applied.
   - Review of the distributed control approach in power converters, focusing on the structure in layers of this type of control, the different implementations available in literature and the communication protocols used to interconnect the control agents.
   - Review of different implementations of Real-Time Operating Systems, which can be used for the development of a digital controller in a Micro-Processor to provide enhanced support and connectivity.
   - Review of power sharing in multiport converters for the integration of multiple power units to take advantage of their specific characteristics. The study focuses on the exploitation of hybrid energy storage systems.

II. Dynamic modeling of a power cell with the necessary power and control devices for building different configurations of modular power converters by making diverse power cell arrangements, depending on the requirements of the application.

III. Development of a distributed digital control system platform capable of handling modular power converters. It is based on a versatile control structure that allows its adequate operation for different operating cases.

IV. Analysis of the latency in a controller based on a open-source Real-Time Operating System to validate the implementation of a digital controller in a general-purpose Micro-Processor.

V. Implementation of a multiport power converter operated by a distributed control system for an application based on multiple energy-storage devices and power loads/sources to counteract power limitation in the main electric grid.

VI. Simulation and experimental validation. To check the feasibility of the proposed solutions, several simulations are performed using MATLAB/Simulink. In addition, to further enhance validation, some experimental tests are carried out in a controlled environment within the laboratory of the LEMUR researching group of the University of Oviedo, Spain.

1.3 Thesis contributions

The contributions of the work carried out during the course of this thesis are presented below:

Distributed Control System for Modular Power Converters [CP2]

First contribution is found in the development of a control system distributed into various devices following a hierarchical structure, making it suitable for its integration in modular power converters.

For this purpose, several distributed controllers are located in each of the power cells of the converter to perform the local control, with a central controller in charge of operating all of them to achieve the requirements established at an application level.

The analysis focuses on the implementation of versatile digital controller in the distributed devices based on resonant approaches to guarantee a proper operation for both AC and DC power units. This enables the possibility of building a multiport power converter controlling an arbitrary number of power units.

Power Sharing Solutions for a Multiport Converter [JP1, CP1]

Second contribution is found in the proposal of compensation alternatives for power sharing mismatches occurring during the operation of multiport converters based on distributed control systems.

The connection of several power loads and sources together with different energy-storage units requires a specific distribution of the power flow among the different devices to maintain a stable operation of the whole system. Therefore, a power sharing algorithm is integrated in the distributed control system to address this issue.

Nevertheless, either errors in the measurements, power limitations in the units or islanding operation can provoke mismatches in the power sharing. Thus, several compensation alternatives are proposed to counteract this problem.

Distributed Control Deployment in a Digital Platform based on a μP under RTOS [IPR1, SLA1]

Final contribution is related to the implementation of the central controller of a distributed control system in a general-purpose Micro-Processor. This is done by integrating a Real-Time extension in a conventional open-source Operating System. This way, firm real-time operation is guaranteed to execute high-priority tasks regarding control operation, while keeping low-priority services typically available in an OS.

1.4 Thesis publications

The work developed for the thesis has resulted in the writing of several conference and journal papers, as shown below. In some of them [JP1, CP1, CP2], the author contribution is strictly the result of the research contributions in this thesis; in the others, the author of this thesis has contributed either by providing the control platform for the experimental validation or in the writing and reviewing process.

1.4.1 Peer-reviewed journal papers

JP1 **G. Villa**, S. Saeed, P. García, C. Gómez-Aleixandre and R. Georgious, "Compensation Alternatives for Power Sharing Mismatch in Multiport DC–DC–AC Converters," in *IEEE Transactions on Industry Applications*, vol. 57, no. 6, pp. 6221-6236, Nov.-Dec. 2021, doi: 10.1109/TIA.2021.3115721.

JP2 I. Peláez, P. García, **G. Villa** and S. Saeed, "Real-Time Measurement of Li-Ion Battery Cells Using Power Converter Pulse-Signal Injection and Fusion Methods," in *IEEE Transactions on Industry Applications*, vol. 57, no. 6, pp. 6350-6361, Nov.-Dec. 2021, doi: 10.1109/TIA.2021.3101777.

JP3 A. Suárez-González, P. García, Á. Navarro-Rodríguez, **G. Villa** and J. M. Cano, "Sensorless Unbalance Modeling and Estimation as an Ancillary Service for LV Four-Wire/Three-Phase Power Converters," in *IEEE Transactions on Industry Applications*, vol. 55, no. 5, pp. 4876-4885, Sept.-Oct. 2019, doi: 10.1109/TIA.2019.2918046.

1.4.2 Peer-reviewed conference papers

CP1 **G. Villa**, S. Saeed, P. García, C. Gómez-Aleixandre and R. Georgious, "Compensation Alternatives for Power Sharing Errors in Multi-Port Converters for

Hybrid DC/AC Microgrids," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 6929-6939, doi: 10.1109/ECCE.2019.8912879.

CP2 **G. Villa**, C. Gómez-Aleixandre, P. García and J. García, "Distributed Control Alternatives of Modular Power Converters for Hybrid DC/AC Microgrids," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 6379-6386, doi: 10.1109/ECCE.2018.8557556.

CP3 J. M. Piedra, P. García, R. Georgious, **G. Villa** and M. B. Gebremariam, "Transformer-less Alternative Topologies of a Unified Power Quality Conditioner with Embedded Hybrid Energy Storage," *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 3176-3181, doi: 10.1109/ECCE47101.2021.9595585.

CP4 C. Gómez-Aleixandre, Á. Navarro-Rodríguez, **G. Villa**, C. Blanco and P. García, "Sharing Control Strategies for a Hybrid 48V/375V/400Vac AC/DC Microgrid," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 3900-3907, doi: 10.1109/ECCE44975.2020.9235472.

CP5 M. Crespo, R. Georgious, P. García and **G. Villa**, "Active equalization of series/parallel Li-ion battery modules including no-load conditions," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 4431-4437, doi: 10.1109/ECCE44975.2020.9236250.

CP6 C. Gómez-Aleixandre, **G. Villa**, P. García, A. Suárez-González and Á. Navarro-Rodríguez, "Homopolar harmonic injection and grid synchronization in distributed control systems for grid-tied intelligent power electronic blocks in 4-wire 3-phase converters," *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, 2019, pp. 3906-3911, doi: 10.1109/IECON.2019.8927413.

CP7 C. Gómez-Aleixandre, P. García, Á. Navarro-Rodríguez and **G. Villa**, "Design and Control of a Hybrid 48v/375v/400Vac AC/DC Microgrid," *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, 2019, pp. 3977-3982, doi: 10.1109/IECON.2019.8926709.

CP8 I. Peláez, P. García, **G. Villa** and S. Saheed, "Li-ion Batteries Parameter Estimation Using Converter Excitation and Fusion Methods," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 2491-2498, doi: 10.1109/ECCE.2019.8912968.

CP9 M. Crespo, P. García, R. Georgious, **G. Villa** and J. García, "Design and Control of a Modular 48/400V Power Converter for the Grid Integration of Energy Storage Systems," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 1421-1428, doi: 10.1109/ECCE.2019.8912775.

CP10 I. Peláez, S. Saheed, **G. Villa** and P. García, "Optimization Method for the Integration of Hybrid Energy Storage Systems in Industrial Applications," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 6646-6653, doi: 10.1109/ECCE.2018.8557882.

CP11 A. Suárez-González, P. García, Á. Navarro-Rodríguez, **G. Villa** and J. M. Cano, "Sensorless unbalance correction as an ancillary service for LV 4-wire/3-phase power converters," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 4799-4805, doi: 10.1109/ECCE.2017.8096816.

1.5 Thesis software with intellectual property rights

The work developed for the thesis has also resulted in the development of a software with intellectual property rights [IPR1], in order to enable the exploitation of part of the knowledge acquired during the course of the thesis at a business level.

IPR1 *Software name*: DECiSivE - Development of Energy Control SystEms.
Holder: University of Oviedo.
Authors: Pablo García, Marcos Cuadrado and **Geber Villa**.
Registration authority: General Registry of Intellectual Property, Ministry of Culture and Sport, Spain.
Request number: O-308-2020.
Request date: 29 September 2020.
Registration number: 05/2020/432.
Registration date: 30 November 2020.

The explotation of the software is currently active, since a 5-year software license agreement [SLA1] has been signed with the company Enfasys Ingeniería S.L. for the development of part of its products using the software with intellectual property rights derived from the thesis work.

SLA1 *Software name*: DECiSivE - Development of Energy Control SystEms.
Vendor company: University of Oviedo Foundation on behalf of University of Oviedo.
User company: Enfasys Ingeniería S.L.
Authors: Pablo García (10% share in user company), Marcos Cuadrado (30% share in user company) and **Geber Villa** (10% share in user company).
Reference number: PAT-20-003.
Start date: 10 November 2020.
End date: 10 November 2025.

1.6 Thesis outline

The thesis document is organized in seven chapters and an appendix according to the following structure:

- **Chapter 1** introduces the background and motivation behind the realization of this thesis. From that, the fundamental objectives of this work are determined and the contributions which support the thesis are presented. In addition, an enumeration of the different journal and conference publications derived from the thesis work is shown. Finally, the structure of the document is described to facilitate its understanding.
- **Chapter 2** shows a literature review and a state-of-the-art analysis related to the use of distributed control systems in modular power converters. The concept of power cell is initially presented, giving some examples of converter configurations and applications where modular converters based on this concept are used. After that, a generic structure for the distributed control is described, from which different implementations are found in literature. Moreover, a review of different approaches and developments of Real-Time Operating Systems valid for digital controller implementations is carried out. Finally, power sharing in multiport power converters is analyzed, focusing on the exploitation of hybrid energy storage systems.
- **Chapter 3** presents the dynamic modeling of the power of the modular converter approach with the added instrumentation and control devices required to operate it conveniently for a distributed control scheme.
- **Chapter 4** addresses the analysis and development of the distributed digital control system needed for a versatile operation of the modular power converter, so that it can operate multiple power units with different electrical characteristics (DC, single-phase AC or three-phase AC).
- **Chapter 5** shows an analysis of latency in the Real-Time Operating System used for the implementation of the central controller in the distributed control system. The analysis is performed to validate firm real-time operation, which is necessary for the correct performance of the central controller.
- **Chapter 6** presents the implementation of a multiport power converter based on the results achieved in previous chapters, operating a system with several power units, such as load, source and energy-storage devices. The power sharing algorithm used to properly distribute the power flow among the different units is discussed, including compensation techniques to counteract power mismatches due to measurement errors, power limitation and islanding operation.
- **Chapter 7** describes the conclusions derived from all the work carried out during the thesis, as well as the future work that can be developed starting with the results obtained.

Chapter 2

Literature review and state of the art

2.1 Introduction

In this chapter, a review of the literature related to the different topics covered in the development of the thesis is carried out to support the contributions presented in future chapters.

The main objective of this work is the development of a distributed control system suitable for the implementation of a modular power converter with a multiport structure based on the use of basic power blocks.

Therefore, an initial review of different configurations of modular converters based on basic power blocks is performed. In this way, it is possible to determine the most suitable modular converter structure to meet the objectives set. For this purpose, information is sought about the concept of the basic power block, the characteristics it provides and why it is suitable for the construction of modular power converters. After that, different configurations of power converters based on a basic power block and proposed applications using these converters are reviewed in the literature.

Once the state of the art on modular power converters based on basic power blocks has been analyzed, the literature is reviewed for distributed control systems that allow the proper management of these converters. Initially, information about the structuring of distributed control systems is sought, and then different implementations that can be made in this type of control are discussed. All this in order to understand how to make the most appropriate configuration to meet the objective of implementing a distributed control system suitable for a multiport converter.

An essential requirement for the realization of a distributed control system is to have a communications system that interconnects the different control units with each

other. Therefore, the organization of communications in different layers is analyzed to then review various existing protocols with different characteristics depending on the needs of each specific application.

In addition, the implementation of a distributed control system for multiport converters imposes a high computational burden to manage and synchronize the operation of all distributed control units, as well as interactivity to facilitate local or remote monitoring. Therefore, a review of the different implementations of Real-Time Operating Systems is made in order to integrate the central controller in a high-performance microprocessor. In this way, it is possible to execute high-priority tasks with firm real-time constraints related to critical control tasks, at the same time as low-priority tasks related to auxiliary control or monitoring tasks.

2.2 Modular power converters

Modular power converters are based on the development of a basic power block that can be replicated several times in order to build the power conversion stage required for the relevant application. In this way, a flexible converter is formed, which is adaptable to changing requirements for use in a variety of applications, all without the need for a complete redesign of the converter.

The modular power converter concept is exploited in the development of Modular Multilevel Converters (MMCs) [2.1], which are based on the series connection of several identical submodules in each branch in order to increase the voltage level that the converter can withstand, thus enabling its integration in HVDC applications. By designing a submodule with a fixed power stage that can be replicated several times to meet the specific requirements of each application, it is possible to provide the converter with a modular structure, which gives it flexibility in its sizing and therefore great scalability. Fig. 2.1 shows the implementation of the MMC based on submodules (SM) with a fixed power stage.

Following the MMC approach, a modular approach can be applied to other types of converters to take advantage of enhanced functionality, improving performance in a variety of applications.

Considering all the above, different implementations of basic power blocks capable of building modular power converters are reviewed in this section. After that, different converter configurations based on these building blocks and, in turn, different applications where they can be employed are discussed.

2.2.1 Power Electronics Building Block (PEBB)

The idea of using a basic power block for the construction of power converters is reflected in the definition of the Power Electronics Building Block (PEBB) concept

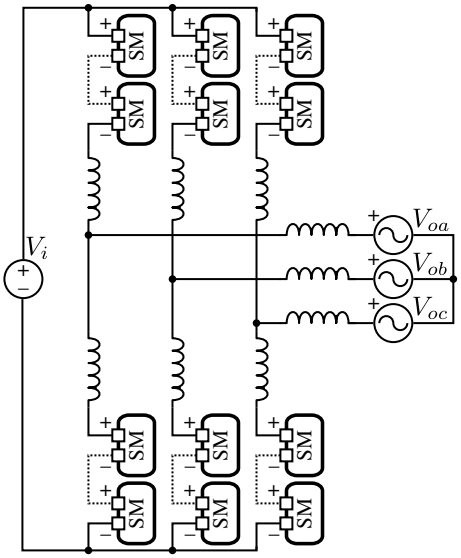

Figure 2.1: MMC based on submodules (SM) with a fixed power stage.

[2.2, 2.3]. The main objective associated with this concept is to standardize a power block with a certain structure that can be reused in multiple applications.

From a conventional point of view, the construction of a specific power converter for a given application involves a design and validation process with a considerable cost. At the same time, the implementation of this converter is associated with installation and maintenance costs that are not negligible. The design of reusable PEBBs can reduce these costs. The objective is to focus the engineering effort on the design of the PEBB, with all the costs that this entails, in order to reduce them in the medium and long term by integrating the PEBB into various converters that can be used in multiple applications. Providing a PEBB enables an open plug-and-play converter design methodology, in which the design of a converter focuses on knowing the characteristics of the PEBB to interconnect them in a certain way to develop the desired application.

The design of the PEBB is critical to comply with a user-friendly methodology based on the interconnection of functional blocks. Therefore, the building block must contain all those elements necessary to fulfill its purpose. First, those components that make up the power stage must be available, whether they are active (power switches) or passive energy-storage elements (inductors and capacitors). Next, switching control logic such as gate drivers, modulators and comparators must be integrated. Finally, cooling systems to dissipate heat, sensors to know the current state of the PEBB and protections to act in case of malfunction must be introduced.

Similar approaches to the PEBB concept have been explored, such as Power Block Geometry (PBG) [2.4]. In this case, the authors propose the creation of several basic power units that can be put together like a puzzle, depending on the power conversion

step to be performed. This confirms the growing interest and development of modular topologies based on basic power blocks, resulting in different implementations of PEBBs proposed over time.

Starting with the simplest implementations, PEBB based on the half-bridge topology can be found in the literature. The starting point is to integrate in a single functional block two power switches connected in series and the drivers and control electronics to operate them properly. This allows to obtain a basic PEBB with half-bridge topology that can be used in different power converters [2.5]. To improve the performance of the PEBB and reduce its dependence on external elements, additional passive elements can be added to this topology, such as a DC capacitor [2.6] or a midpoint LC filter [2.7], generating new PEBBs more suitable for various applications. Considering all the above, Fig. 2.2 shows several options for PEBBs based on the half-bridge topology.

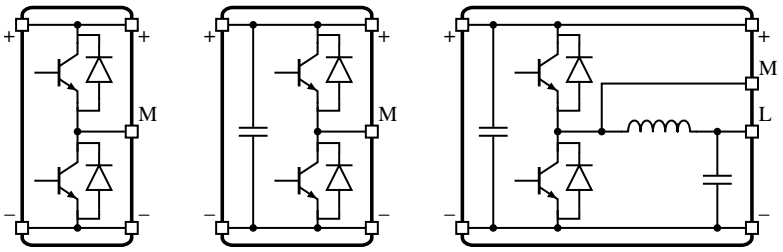

Figure 2.2: PEBB implementations based on the half-bridge topology.

While it is true that the combination of several PEBBs based on the half-bridge topology allows the configuration of various types of power converters, the implementation of the full-bridge topology in a PEBB facilitates the development of certain modular converters. This is achieved by connecting two half-bridge branches in parallel and introducing the necessary drivers and control electronics to handle the new topology [2.8]. The introduction of additional DC capacitors [2.9], midpoint inductive filters or power switches [2.10, 2.11] allows the PEBB to be adapted to the requirements of each specific application. Additionally, an embedded digital controller can be introduced in order to provide the PEBB with some intelligence [2.12, 2.13]. All things considered, Fig. 2.3 shows several options for PEBBs based on the full-bridge topology.

Some converters require the introduction of electrical isolation between the different ports of the converter to meet the requirements imposed by the application. The application of this feature to the case of modular power converters involves the integration of a transformer isolation stage within the PEBB itself to electrically isolate both sides of the power conversion [2.14], as shown in Fig. 2.4.

Going back to the origins of modular power converters, multilevel approaches have also been developed to meet the requirements of MMCs, in order to increase voltage/power rating of conventional power converters to adapt them for HVDC applications. In particular, there are examples of PEBBs implementing a 3L-NPC leg [2.8], a

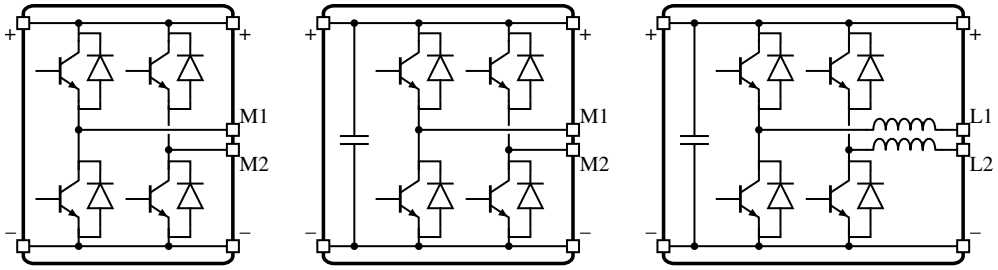

Figure 2.3: PEBB implementations based on the full-bridge topology.

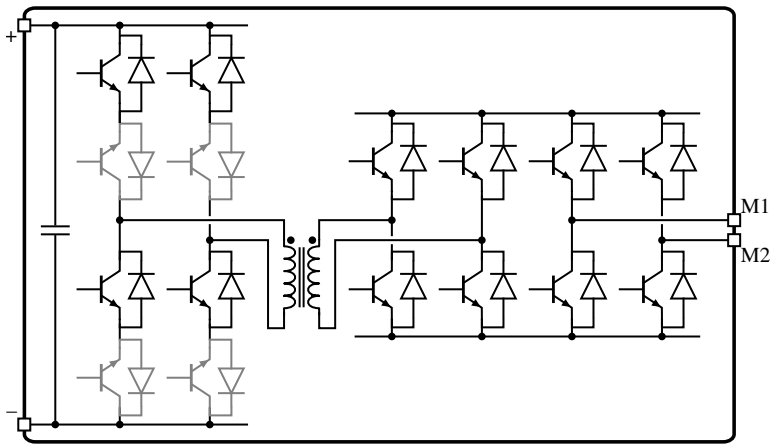

Figure 2.4: PEBB implementation based on the full-bridge topology with isolation between both conversion sides. Gray power switches are only needed to block negative voltages in the left side of the PEBB for AC sources/loads.

3L-MNPC leg with hybrid switches [2.15] and a dual 3L-ANPC-VSC phase-leg [2.16]. These PEBB implementations are shown in Fig. 2.5.

PEBB concept also allows the integration of power units with greater complexity or adapted to a more specific set of applications, in case the power unit needs to be replicated repeatedly. Several examples of PEBBs designed for specific applications are found in the literature. This is the case for the development of a PEBB to function as a converter phase-leg with ZCT via auxiliary switches and a LC resonant tank [2.17], as shown in Fig. 2.6a. Moreover, the implementation of a PEBB to operate as a Common Cross-Connected Stage (C^3S) for a 3ph-5L-ANPC-VSC has also been carried out [2.18], as shown in Fig. 2.6b.

Also noteworthy is the construction of an AC PEBB by building a branch with two bidirectional AC power switches and midpoint connection, using four power transistors and four active snubbers [2.19], as shown in Fig. 2.7. In addition, the integration of a whole multiport power converter in a PEBB has been accomplished, as is the particular

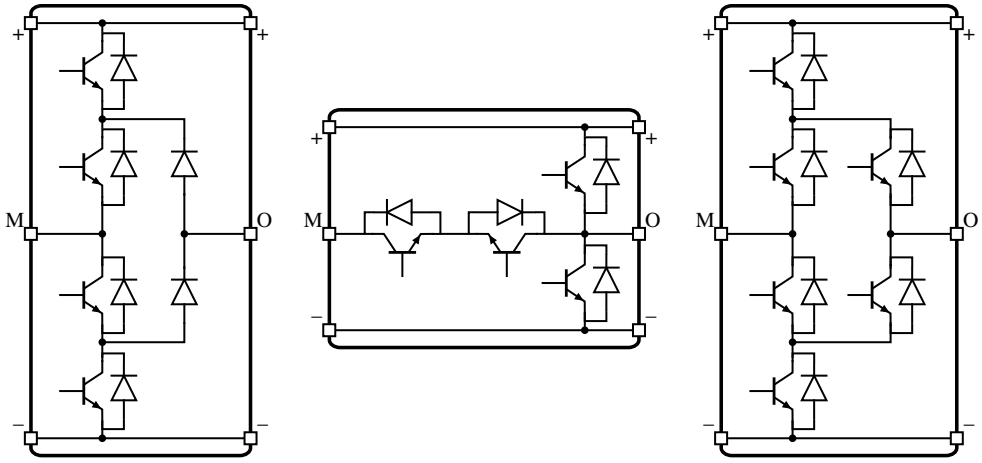

Figure 2.5: PEBB implementations based on 3L-NPC leg topologies.

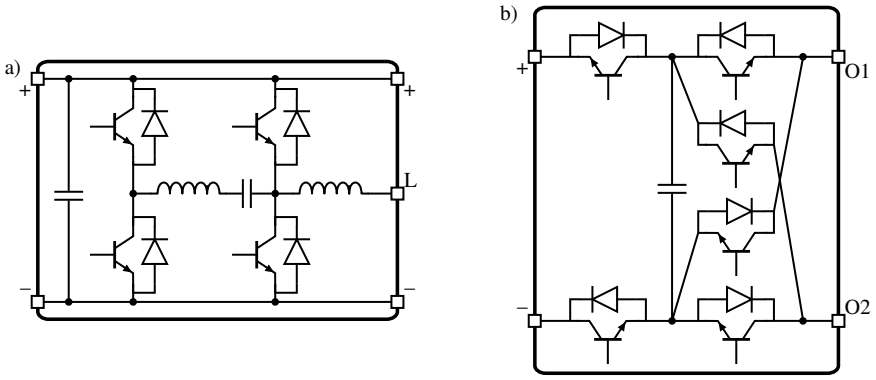

Figure 2.6: Complex PEBB implementations: a) Converter phase-leg with ZCT via auxiliary switches and a LC resonant tank; b) C^3S for a 3ph-5L-ANPC-VSC.

case of a MF-PET [2.20].

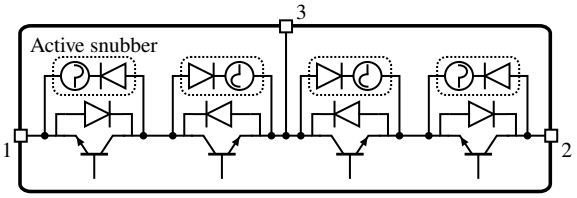

Figure 2.7: AC/AC PEBB implementation based on a branch with two bidirectional AC power switches and midpoint connection, using four power transistors and four active snubbers.

In relation to what was discussed at the beginning of this section, the use of PEBBs to build a modular power converter facilitates the validation of the final assembly, since the completion of a successful test on the PEBB allows to certify the operation of a large part of the converter. In this respect, there are several cases in which a PEBB is tested. This is the case of the electrothermal modeling of a full-bridge PEBB [2.21], the reliability analysis in a half-bridge PEBB [2.22] and the predictive accuracy of power converter modeling based on PEBB [2.23].

2.2.2 Converter configurations

Starting from the previous design of one or more PEBBs, it is possible to build the desired modular power converter by positioning and connecting these PEBBs in a certain arrangement. In this way, different configurations of converters based on PEBBs are documented in the literature.

To begin with, regarding DC/DC power conversion, bidirectional buck and boost converters have been implemented by directly using one half-bridge PEBB with DC capacitors and midpoint inductor [2.7, 2.24], as shown in Fig. 2.8. For applications requiring a voltage stepping down through a buck converter, input voltage (V_i) has to be connected between the upper (+) and lower terminals (-) of the half-bridge PEBB obtaining a lower output voltage (V_o) between series inductor (L) and lower (-) terminals, with a magnitude depending on the duty cycle of the power switches. If input and output voltages are swapped, the half-bridge PEBB actuates as a boost converter, which is suitable for applications requiring a voltage stepping up. The connection in series of both buck and boost converters by interconnecting both series inductor (L) and lower terminals enables the implementation of a buck-boost converter, as shown in Fig. 2.9, allowing for both voltage stepping down and voltage stepping up.

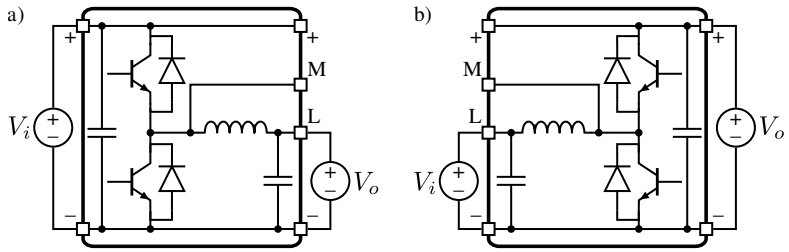

Figure 2.8: Bidirectional DC/DC power converters based on half-bridge PEBBs with DC capacitors and midpoint inductors: a) Buck power converter; b) Boost power converter.

In addition, the interconnection of several half-bridge PEBBs with a different arrangement than in previous cases enables the development of DC/AC power conversion. For this purpose, unlike in glsdc/DC power conversion, both the upper (+) and lower (+) terminals of all the used PEBBs are connected between them, establishing a common bus to which the DC voltage source/load can be connected. This way, the series

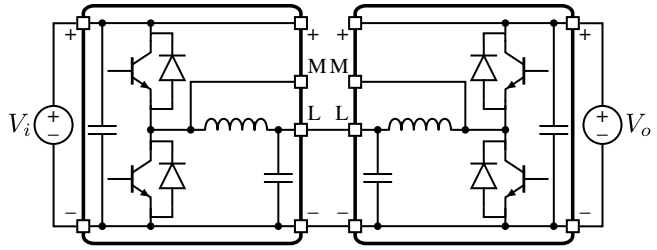

Figure 2.9: Bidirectional buck-boost DC/DC power converter based on half-bridge PEBBs with DC capacitors and midpoint inductors.

inductor terminal (L) of each PEBB represent an AC source/load phase, so that the number of PEBBs is determined depending on the number of phases required by the AC side of the power conversion. Considering all the above, DC/1ph-AC and DC/3ph-AC converters based on several half-bridge PEBBs with DC capacitors and midpoint inductors have been developed [2.5, 2.7, 2.24], as shown in Figs. 2.10 and 2.11.

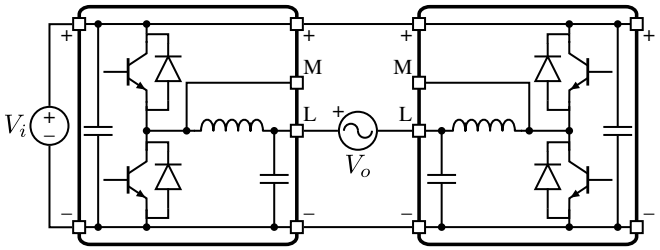

Figure 2.10: DC/1ph-AC power converter based on half-bridge PEBBs with DC capacitors and midpoint inductors.

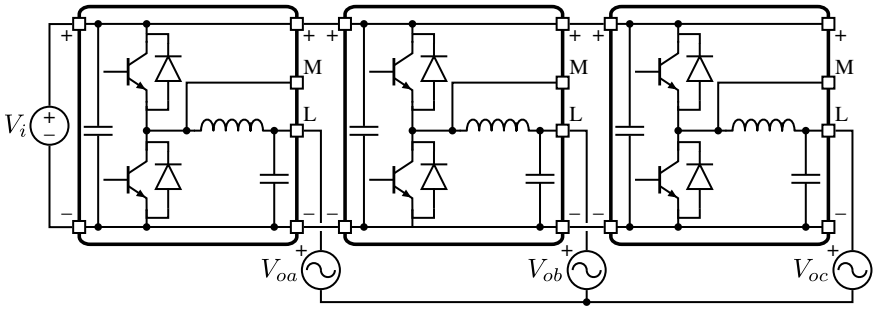

Figure 2.11: DC/3ph-AC power converter based on half-bridge PEBBs with DC capacitors and midpoint inductors.

In the specific case of a modular DC/4wire-3ph-DC power converter, it is necessary to use a power switch branch for each of the three AC active phases and an additional

one for the AC neutral phase, requiring a total of four half-bridge PEBBs for implementing the whole converter. However, the utilization of a full-bridge PEBB instead of the half-bridge one allows the total number of PEBBs by half, facilitating improved reliability as well as cost reduction. In this way, the implementation of DC/4wire-3ph-DC power converter based on two full-bridge PEBBs with DC capacitors and midpoint inductors is found in literature [2.8, 2.9], by following the schematic shown in Fig. 2.12.

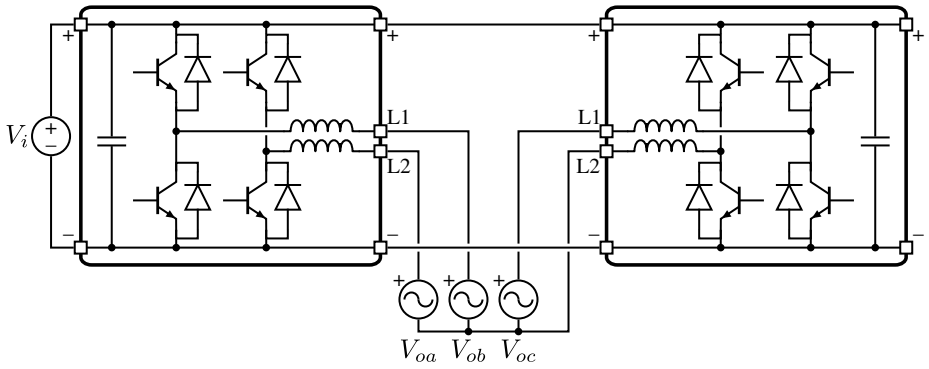

Figure 2.12: DC/4wire-3ph-AC power converter based on full-bridge PEBBs with DC capacitors and midpoint inductors.

As mentioned in the previous section, the development of PEBBs facilitates the implementation of multilevel power converters. By connecting several PEBBs in series, it is possible to form a converter with a certain number of levels and therefore operate with a higher voltage than in a conventional converter. In a first approach, power cells based on half-bridge or full-bridge topologies can be used for this purpose. By using the PEBB based on the full-bridge topology with internal electrical isolation shown in Fig. 2.4, it is possible to form DC/3ph-AC, 3ph-AC/1ph-AC and 3ph-AC/3ph-AC isolated multilevel converters [2.14], as shown in Fig. 2.13.

In addition, multilevel converters have been built using PEBBs based on NPC topologies. This is the case of DC/AC converters based on 3L-NPC PEBB legs for either 1ph [2.8] or 3ph [2.25] AC sources/loads, as shown in Fig. 2.14, easing the development of back-to-back converters by connecting two DC/AC converters between them through a common DC bus. The use of the C^3S PEBBs shown in Fig. 2.6b facilitates the implementation of a 3ph-5L-ANPC converter with cascaded C^3S modules [2.18], as shown in Fig. 2.15.

Throughout this section, the implementation of different converter topologies using a modular approach with the use of power cells has been developed. However, and going back to the concept of MMC shown in Fig. 2.1, the implementation of this type of converter using PEBBs for the submodules (SM) is found in literature, as is the case of a MMC based on full-bridge PEBBs [2.26]. Starting from a common PEBB integrating a full-bridge topology with a DC capacitor and midpoint inductors, and depending on the connection arrangement between the different PEBBs, it is possible

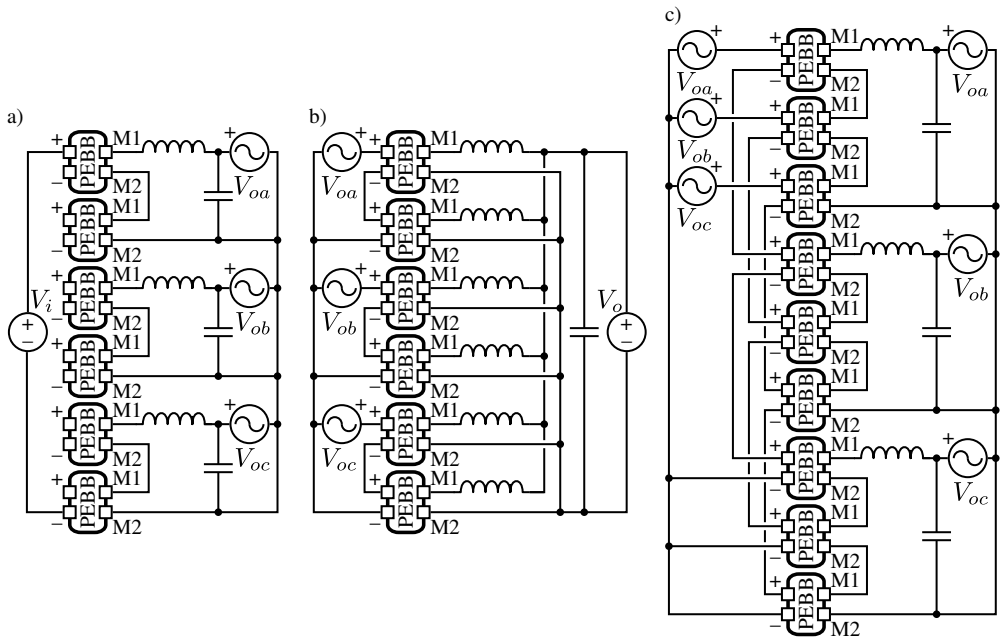

Figure 2.13: Isolated multilevel converters based on isolated full-bridge PEBB from Fig. 2.4: a) DC/3ph-AC power converter; b) 3ph-AC/1ph-AC power converter; c) 3ph-AC/3ph-AC power converter.

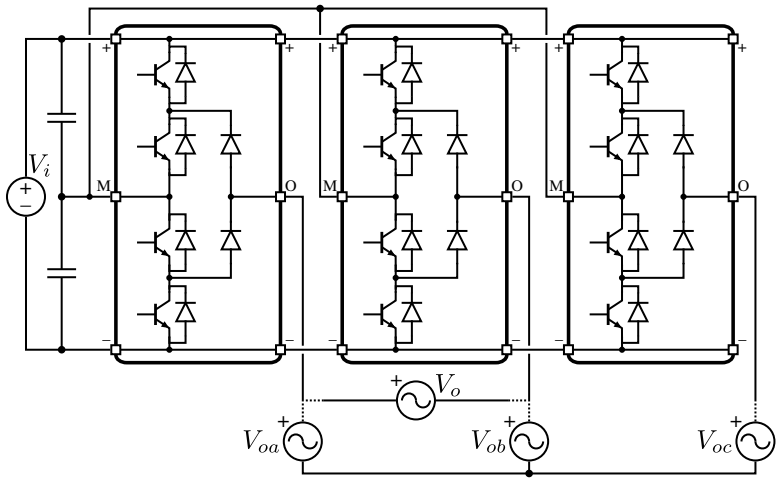

Figure 2.14: DC/AC power converter based on 3L-NPC PEBB legs for either 1ph or 3ph AC sources/loads.

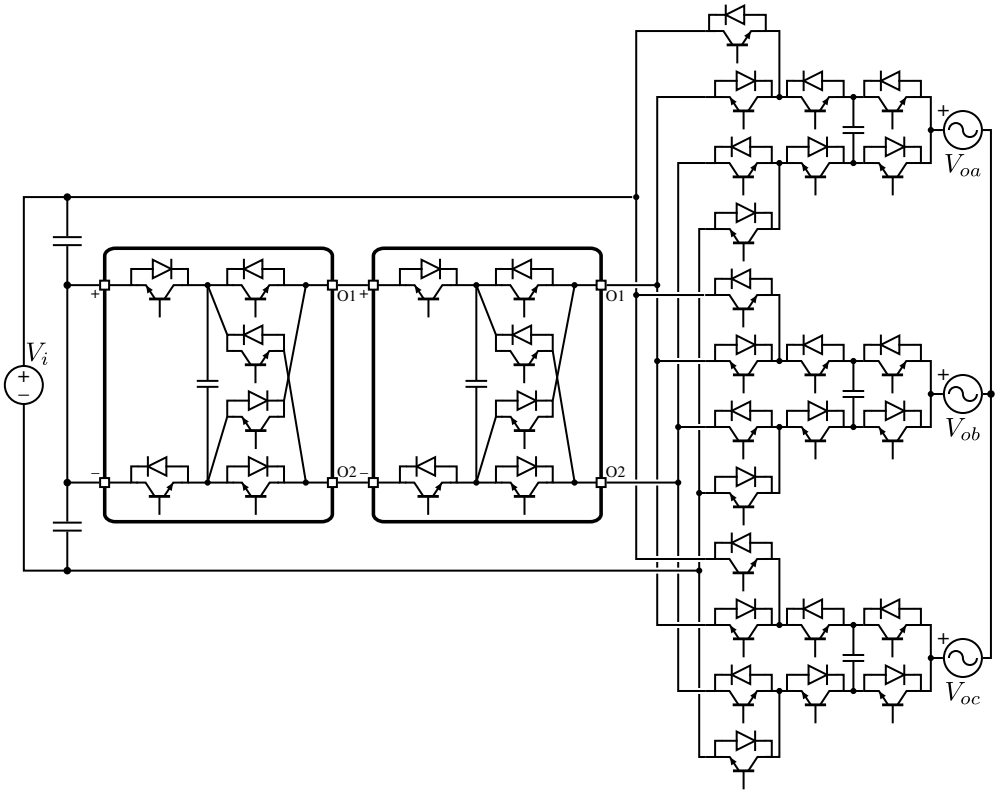

Figure 2.15: 3ph-5L-ANPC power converter based on C^{3}S PEBBs.

to implement at the same time a cascaded multilevel converter (series connection) and a modular interleaved converter (parallel connection) [2.27].

Finally, there is the implementation of more complex power converters, reaching the development of a hybrid DC/3ph-AC converter with three full-bridge units and a back-to-back DC/3ph-AC converter, both based on 3L-NPC PEBBs [2.28]. Also noteworthy is the construction of a Controllable Network Transformer (CNT) based on the AC PEBBs shown in Fig. 2.7 [2.19].

2.2.3 Proposed applications

Having explored various configurations of converters formed from PEBBs, several applications based on the use of this type of converters are here shown, in order to demonstrate the applicability of modular power converters based on PEBBs. The target applications have in common that are based on power converter topologies with a larger number of devices, thus demanding important resources in terms of inputs and

outputs as well as computational power from the control system. All these applications can exploit the natural distributed control idea drawn from the PEBBs concept.

First application is related to the stability analysis of a microgrid by characterizing both the source-output and load-input impedances. The development of an Impedance Measurement Unit (IMU) allows estimating these impedances to determine whether the system is stable for a given operating range and thus ensure proper behavior when operating it. The integration of a IMU for a MVDC system on a ship is found in the literature [2.27, 2.29]. In this application, the use of PEBBs for the implementation of the IMU enables the possibility of developing different operation modes depending on the arrangement of the modular converter. Starting from a PEBB based on a full-bridge topology with DC capacitor and inductor filters, it is possible to configure a shunt current mode, more suitable for source-output impedance characterization, by connecting three PEBBs in series and hence forming a cascaded multilevel converter; and a series voltage mode, more suitable for load-input impedance characterization, by connecting three PEBBs in parallel and hence forming an interleaved modular converter.

FACTS applications require good output voltage quality with low THD at the PCC to comply with the regulations and standards. To avoid increasing the switching frequency for improving the output voltage quality, multipulse VSCs are commonly operated for these type of applications. This way, the use of PEBBs is also suitable for FACTS applications, since it facilitates the development of multipulse configurations that require the integration of the same power unit multiple times. For example, there is an application in which 12 3L-NPC PEBBs are connected in parallel to a common DC bus in order to develop a VSC with an output voltage of quasi 48 pulses [2.30].

The PEBB concept can also be applied to build all the converters of a Distribution Power System (DPS). By using a PEBB based on the half-bridge topology, it is possible to build a DC DPS consisting of a 4-wire DC/3ph-AC converter (4 PEBBs) to interface with the power grid, a DC-3ph-AC converter (3 PEBBs) to connect an electric motor/generator and a DC/DC converter (2 PEBBs) to connect a DC load/source [2.24]. In case new power units are to be incorporated into the system, extra PEBBs could be used to build the corresponding converter, facilitating its set-up due to the preliminary validation of the PEBB.

As discussed above, the increasing integration of renewable energy sources into the power grid is strongly related to distributed generation, which encourages the development of modular converters that provide the flexibility and scalability needed to respond to the requirements imposed at any given time. Therefore, the exploitation of renewable energy sources also benefits from the use of PEBBs, as in the case of the development of different wind turbine converter configurations for off-shore applications [2.25], using 3L-NPC PEBBs.

2.3 Distributed control in power converters

Traditionally, the development of a power converter for a given application is associated with a single controller responsible for managing the entire converter. Each of the power devices may include integrated drivers in order to facilitate its operation, but not control loops as such. Therefore, the concentration of the control algorithm in a single location makes this type of control known as centralized control.

Having developed a modular converter in its power stage, a decentralization of the converter control system is the next step in order to maximize the modularity of the converter as a whole. Thus, while centralized control is suitable for conventional power converters, it does not provide the flexibility required for a modular converter. This is where the concept of distributed control comes into play.

In a distributed control system, the control algorithm is not concentrated in a single control device but are distributed among different control units along the power converter. For this purpose, it is necessary to organize the control system in different layers, starting from a specific local control close to the power switches to a more generic global control close to the operation of the power converter as a whole. Therefore, the structure of the distributed control system to be implemented in a modular power converter will be discussed below.

2.3.1 Distributed control structure

Starting from the PEBB concept to develop a modular power converter, a generic distributed control scheme applicable to this type of converters has been established in the literature in order to facilitate its standardization [2.31–2.33]. For this purpose, the control system has been classified in five different layers taking into account functional and temporal criteria, as shown in Fig. 2.16:

- First layer is known as hardware control layer and it manages everything directly related to the power switches. Therefore, it provides functions such as gate control, galvanic isolation, safe switching (snubbers) and hardware protections. The sampling frequency is usually between 1 MHz and 10 MHz.
- Second layer is known as switching control layer and it is in charge of the modulation and pulse generation. It also includes extra protection logic, such as trip-zone event management, to avoid catastrophic failures. Note that these functions are generic and applicable to any power converter regardless of the final application. The sampling frequency is usually between 100 kHz and 1 MHz.
- Third layer is known as converter control layer and it provides the fundamental algorithms that control the electric magnitudes in the power converter branches. Thus, this layer includes current/voltage control loops, sensor measurements, duty cycle computation and any functionality that manages essential converter

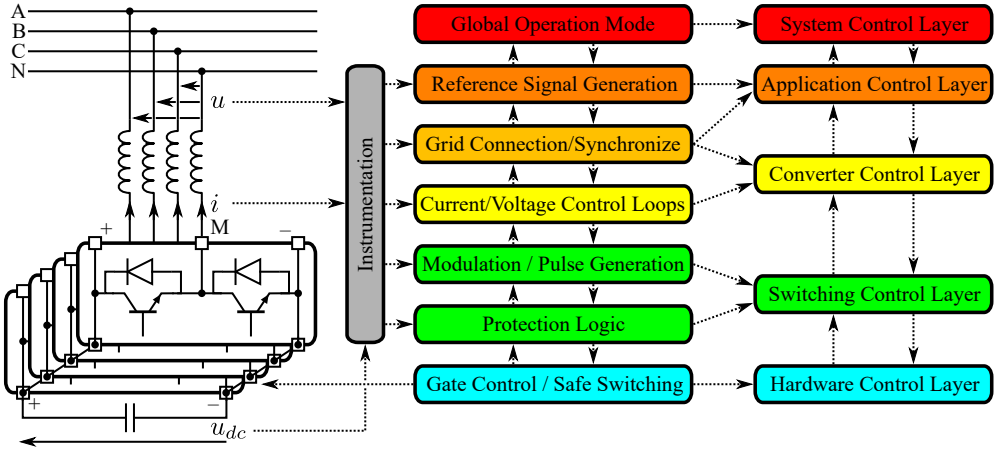

Figure 2.16: Distributed control structure with a five-layer classification suitable for PEBBs.

variables. In some specific cases, this control layer could also include grid connection and synchronization techniques. The sampling frequency is usually between 1 kHz and 100 kHz.

- Fourth layer is known as application control layer and it carries out all the computations needed to use the power converter for a specific application. Hence, this layer includes active/reactive power management (droop control), current/voltage reference computation for the converter control layer and could include grid connection and synchronization techniques. The sampling frequency is usually lower or equal than 1 kHz.

- Fifth layer is known as system control layer and it determines the system behavior as a whole and how it interacts with the main grid. Therefore, this layer includes the selection of the power converter operation mode depending on the existing conditions and any human-machine interface needed to monitor with the whole system. The sampling frequency is usually lower or equal than 100 Hz.

Considering the aforementioned structure, the control system can be organized for its classification into the different layers. In this way, by integrating each of the layers in various devices connected to each other, the implementation of a distributed control system can be achieved.

2.3.2 Distributed control implementations

Once the layered structure for a distributed control system has been defined, its implementation in various interconnected devices is not arbitrary, since the organization between these devices must be determined. Regarding distributed control, different

implementations can be found in the literature. Broadly speaking, these implementations can be classified into two main categories: multi-agent control and hierarchical control.

2.3.2.1 Multi-agent control

Multi-agent control consists of having fully distributed control over the different control units, which are interconnected and follow a horizontal organizational structure, as shown in Fig. 2.17. In this way, the control units start from an initial situation of equality when making decisions, although they can establish arbitration procedures between them to prioritize some units over others according to the global state of the system.

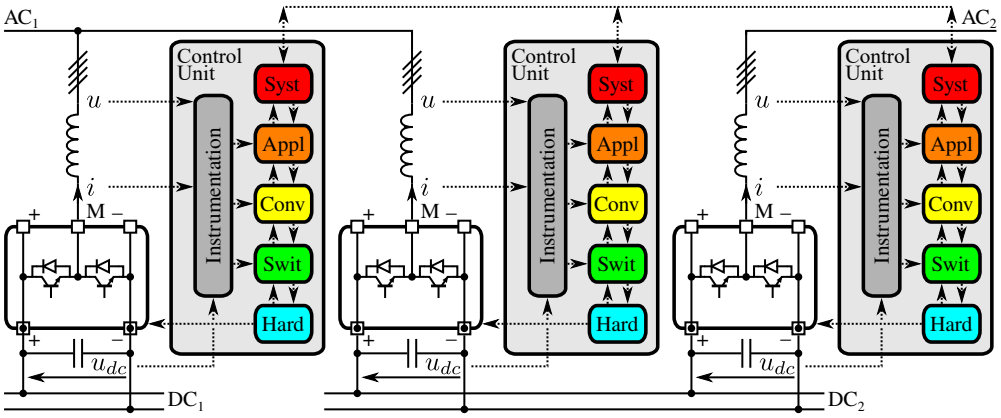

Figure 2.17: Multi-agent control structure based on a five-layer distributed control system.

This is the case of a modular power system with several distributed photovoltaic generation units [2.34]. All of them are connected to a DC bus via a DC/DC converter and a DC/AC converter is available to connect the entire system to the AC grid. Each converter has its own controller responsible for making it work independently and, therefore, requires an arbitration system between the different controllers for the system to work correctly as a whole. To do this, each controller monitors the voltage level on the DC bus to determine the required operating mode at all times.

The use of a physical quantity that all the converters have in common to intercommunicate the different controllers allows a fast and simple arbitration system. However, there are cases where more advanced synchronization between controllers is required, which entails introducing a communications system to exchange more complex information between the control units.

Examples of multi-agent control with a communications system are found in the literature. For example, a power system consisting of several DC/AC converters connected together either through an AC grid or through a DC bus, as shown in Fig. 2.17,

takes advantage of this type of control to coordinate their operation [2.35]. Each of the converters is managed by an agent that has various operating modes depending on system conditions. In turn, all the agents are interconnected with each other by means of a communications system based on the Ethernet standard. Initially, the agents start in monitoring mode, which consists of analyzing the converter operating conditions to detect violations in the power quality requirements. When an agent detects a problem in its associated converter, it enters broker mode, determining the allocation of the required compensation among the other agents based on the information received from them. Each of the agents that are not in broker mode can enter in compensation mode, in order to consider the references sent by the agent in broker mode to operate the associated converter conveniently.

In addition, this type of control can be used in a pure DC grid in combination with a series of DC/DC converters that interface with the available loads/sources [2.36].

The practical implementation of the existing controller in each converter can be carried out using a DSP to integrate the hardware, switching, converter and application control layers, whereas the implementation of the system control layer would be carried out in a microcomputer that can provide the necessary computing power and connectivity to communicate with the rest of the controllers [2.37]. The connection between the DSP and the microcomputer would be carried out using a communications protocol such as SPI, CAN, I^2C or UART, whereas the interconnection between the different agents would be carried out using protocols such as Ethernet, Wi-Fi, WiMAX or any other mobile technology.

2.3.2.2 Hierarchical control

Hierarchical control consists of having a distributed control following a vertical organizational structure, in which there are a series of local controllers that perform a series of specific tasks and which are commanded by a central controller who is in charge of coordinating them all with each other, as shown in Fig. 2.18. In this way, the central controller is in charge of deciding how the system should operate, receiving information from the different local controllers and sending the necessary commands to make them work as required. The local controllers would only have limited decision-making capacity for those fault events that require immediate intervention, in order to avoid a major problem in the system as a whole.

Examples of hierarchical control with a communications system are found in the literature. For example, a power system consisting of several DC/AC converters connected to the AC grid takes advantage of this type of control [2.38]. System control layer is implemented in the central controller to optimize the task sharing of the local controllers integrated in the power converters. In addition, this type of control can be used in a pure DC grid in combination with a series of DC/DC converters that interface with the available loads/sources [2.39]. The central controller is in charge of establishing the power references for the local controllers inside the power converters.

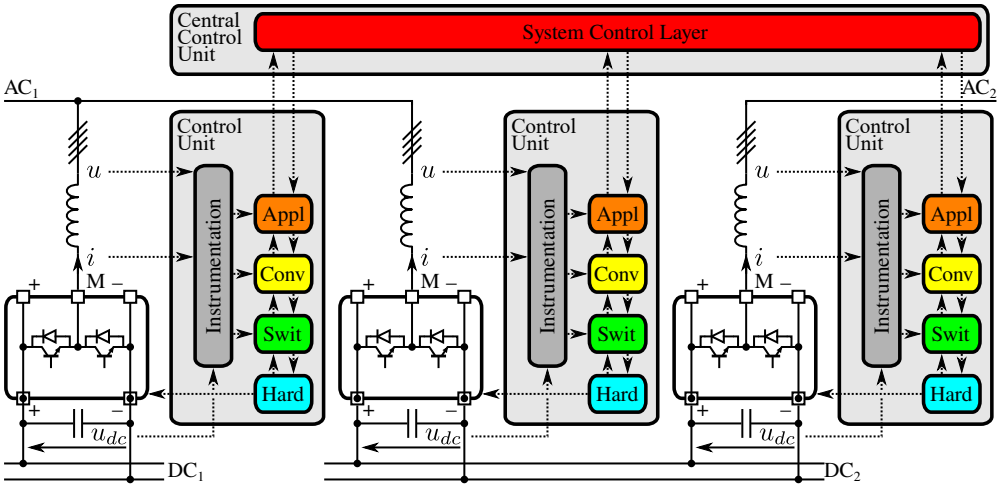

Figure 2.18: Hierarchical control structure based on a five-layer distributed control system.

Hierarchical control is also applied in the case of a PET [2.40]. In this case, the proposed control method reduces the computational load of the central controller and, in turn, simplifies the communication system. This is because the central controller only executes the part of the control algorithm that allows the coordination of the converters and, therefore, the information exchanged between the central controller and the local controllers is limited.

2.3.3 Communications protocols

The implementation of a distributed control system requires the need to communicate the different controllers with each other. Although communication can be done by taking advantage of the behavior of a physical magnitude, this is usually not sufficient for control systems that require greater complexity. Therefore, a communications protocol needs to be established to communicate the different controllers reliably.

There are several communications protocols documented in the literature, each with certain characteristics that make them more suitable for different applications. These protocols establish the requirements of a certain part of the communications system that must be met by all the devices belonging to it in order to exchange information properly.

The Open Systems Interconnection (OSI) model [2.41–2.44] standardizes the communications system by structuring it in different layers according to the operations carried out in the data flow during the course of the entire communications process, from the physical transmission of bits through a given medium to the management of information at the application level. In order to be applied to any type of com-

munications system, the OSI model is highly abstract and therefore divided into 7 layers:

- Layer 1: Physical layer. It manages the transformation of raw bits in a device into a physical signal in the transmission medium. Therefore, it provides the electric and mechanical specifications of the communication system, such as voltage levels, signal timing, data rate, pin layout and line impedance.
- Layer 2: Data link layer. It enables the reliable exchange of data frames between two nodes directly connected through a transmission medium. Therefore, it provides the protocol for establishing the connection between two nodes and the error detection and correction mechanisms. Flow control is also considered in order to avoid overwhelming of a receiving node due to a faster transmitting node.
- Layer 3: Network layer. It allows the exchange of data packets between two nodes without direct connection between them through the transmission medium. Therefore, it provides addressing to identify every node, routing protocols to determine the path of every packet and traffic control to avoid saturation of the network.
- Layer 4: Transport layer. It manages the transmission of variable-size data by partitioning the information into segments to be transferred over the network. Therefore, it provides segmentation/desegmentation procedures and may include reliability checking (flow and error control) although it is not a strict requirement in this layer.
- Layer 5: Session layer. It controls the opening, pausing, resuming and closing of communication sessions between devices at software level.
- Layer 6: Presentation layer. It translates the information received from the network into a manageable format at the application level. Thus, it may include character encoding, data compression techniques and encryption/decryption algorithms.
- Layer 7: Application layer. It consists of those high-level tasks responsible for processing the data received from the network to obtain relevant information for the end users.

Layers 1 (physical) to 3 (network) are considered medium layers since they cover the part of the communication process within the physical transmission medium, whereas layers 4 (transport) to 7 (application) are considered host layers since they cover the part of the communication process that occurs internally in the device. Applying the OSI model strictly is not straightforward since it is difficult to establish the boundaries between layers in some cases. For example, this is the case of the Internet Protocol Suite (TCP/IP model) [2.45, 2.46], which combines layers 5, 6 and 7 of the OSI model into a single application layer in the TCP/IP model.

In the case of internal communications within a PCB between ICs and embedded peripherals, the use of serial communications such as SPI or I^2C is widespread [2.47]. UART is also used in certain cases of low-speed communications, either internally on a PCB or externally between devices.

Serial Peripheral Interface (SPI) is a 4-wire full-duplex synchronous serial communications interface with a master-slave architecture. A single master communicates with one or more slaves via a clock signal (SCLK) generated by the master, a slave select signal (SS) for each slave, a data line from master to slaves (MOSI: Master Out Slave In) and a data line from slaves to master (MISO: Master In Slave Out). SPI does not follow a strict specification since only the pin layout and the signal timing are defined, only describing part of the physical layer. Therefore, this allows maximum customization of the communications protocol to adapt it to the needs of each application. Data rate is not predefined, with some implementations reaching speeds of tens of Mb/s. Some applications of SPI are found in literature [2.48–2.50].

Inter-Integrated Circuit (I^2C) is a 2-wire half-duplex synchronous serial communications interface with a multi-master/slave architecture. Multiple devices communicate with each other via a clock line (SCL) and a data line (SDA) with 7-bit addressing for the slaves and data divided into 8-bit segments. It is electrically designed for the logic low state (0) to be dominant, so that arbitration occurs when several masters want to access the communication bus at the same time. Therefore, I^2C considerably reduces the number of communication lines in the case of multiple devices connected to the bus (2 wires in I^2C vs. 3 wires + 1 wire per slave in SPI). In addition, it allows the interconnection of multiple masters if necessary. However, the level of customization is not as high as in SPI, due to the addressing and arbitration process required to comply with the specifications, which cover a description of the physical and data link layers. Only certain data rates are allowed, the most common being 100 kb/s in standard mode and 400 kb/s in fast mode and, in latest revisions, 10 kb/s in low speed mode, 1 Mb/s in fast mode plus and 3.4 Mb/s in high speed mode. Some applications of I^2C are found in literature [2.51–2.55].

Universal Asynchronous Receiver-Transmitter (UART) is a 2-wire full-duplex asynchronous serial communications interface with a point-to-point architecture. Two devices communicate with each other via a transmitter line (TX) as the output and a receiver line (RX) as the input, with configurable data rate, data length, parity bit and number of stop bits. Settings have to be the same in both devices in order to establish a proper communication channel. Most common date rates are 9.6 kb/s for low-speed applications and 115.2 kb/s for high-speed applications. However, the data rate is freely configurable and can reach speeds of the order of Mb/s for certain implementations. To enable flow control, two additional lines can be added: an input to determine whether data can be transmitted to the remote device (CTS: Clear To Send) and an output to indicate whether data can be received from the remote device (RTS: Request to Send). UART only covers the pin layout and the signal timing, whereas the physical implementation can be based on different standards such as RS-232 [2.56], RS-422 [2.57] or RS-485 [2.58]. Some applications of UART are found in literature [2.59–2.62].

More advanced communications protocols can be used to perform external communications between devices in a more reliable way in industrial environments. This is the case for protocols such as CAN [2.63], Modbus [2.48], EtherCAT [2.64] or PROFINET [2.65–2.68].

2.3.4 Control reconfiguration

It should be noted that a distributed control system may require the reconfiguration of a certain part of the control algorithm, even reaching the switching control layer, depending on the operation mode of the power converter. In this way, the system would be provided with the necessary versatility to operate correctly under different scenarios. For this purpose, three different types of control reconfiguration are proposed in literature [2.69].

First type of control reconfiguration consists of having various control possibilities preprogrammed so that you can switch between them on the fly depending on the situation. The advantage is that it is not necessary to reprogram any control unit as such, but simply send a command to change its operation, facilitating the operation. The disadvantage is the lack of rigidity when modifying the control algorithms during the operation of the equipment, as these are predefined. Therefore, it is recommended to use this option for the most critical functionalities of the system, such as a change of the operation mode in the event of a failure.

Second type of control reconfiguration consists of enabling the possibility of loading new control algorithms on the fly into the control units depending on system requirements. The advantage is that it allows maximum flexibility in reconfiguring the control units and thus increases the versatility of the system. The disadvantage lies in the complexity and time of on-the-fly programming, which adds some delay in changing the operation of the control unit. Therefore, it is recommended to use this option for auxiliary system functionalities, such as the monitoring of certain variables and the computation of certain indexes for power quality estimation.

Third type of control reconfiguration consists of a dynamic assignment of control units to the different power units. The advantage is that it allows the operation of a power unit to be maintained even if the control unit initially associated with it fails if a new control unit is assigned to it. The disadvantage is that it requires a communication and arbitration system between the different control and power units. Therefore, it is advisable to use this option in order to increase the reliability of the system, since it is able to counteract failures in the control units.

2.4 Real-Time OSes

The growing development of the Internet of Things (IoT), which encourages the connection of any device with a certain intelligence to a common network such as the

Internet, implies the need to provide interactivity and extra functionality to embedded systems that traditionally had an isolated operation. Therefore, the number of tasks to be executed in parallel increases to meet the new needs of the industry, causing a redesign of the implementation of control systems.

A possible solution to this problem would be to implement into the control system a Operating System (OS), which is capable of executing a multitude of processes at the same time by managing and sharing the hardware resources with the help of a scheduler.

Traditional implementations of OSes are based on cooperative multitasking, in which the OS scheduler gives control of the hardware resources to a given process and the latter only yields it voluntarily at certain specific points that have been explicitly programmed. In this case, each process is divided into a series of coroutines that run uninterruptedly when control is assigned to them and until they explicitly yield it.

This allows a great deal of control over the allocation of hardware resources since the developer decides when the execution of a process is interrupted. The scheduler simply allocates control to each process when it is its turn and recovers it when it yields it. However, this requires careful planning and programming of all processes running in the OS to function properly. If a process does not yield or disposes of hardware resources for too long, the behavior of the system can be catastrophic.

Nowadays, the large number of processes running on any OS would make it impractical to use cooperative multitasking. Therefore, modern implementations of OSes are based on what is known as preemptive multitasking, in which the scheduler is able to interrupt the execution of one process without its cooperation (preemption) and then allocate the hardware resources to another process.

In order to achieve this purpose, different priorities are established among the executed processes in order to give preference to the most relevant ones. In this way, the most critical processes will be attended to as soon as possible so as not to delay their operation. Nevertheless, preempting a process requires a context switch to store the state of the process so that it can be restored to resume execution at a later time. The problem is that context switches are generally computationally intensive, which can deteriorate the raw performance of the system if a large number of them occur. Because of this, and in order not to lose performance, OSes try to optimize the number of preemptions to achieve a trade-off between raw performance and responsiveness.

There are a multitude of implementations in order to optimize the design of the scheduler according to those characteristics that are to be maximized [2.70–2.81]. In any case, the final behavior depends on the OS and scheduler design. This can cause the execution of certain tasks to occur with a certain delay, resulting in inadequate system performance when running processes under hard or firm real-time conditions.

2.4.1 Native RTOSes

The execution of critical tasks has very strict restrictions as they have to be attended to as soon as possible. Although it is possible to give maximum priority to them in an OS, immediate execution cannot always be guaranteed, so that time constrains (deadlines) are not met, causing catastrophic failures for certain real-time tasks. Real-time tasks can be classified into three different categories: hard real-time tasks, which are not allowed to miss any deadline; firm real-time tasks, which are allowed to miss deadlines infrequently; and soft real-time tasks, which are allowed to miss deadlines frequently.

Standard OSes are not prepared to guarantee the deadlines of a real-time task. In order to compensate for this problem, OSes have been developed specifically to guarantee this mode of operation, known as Real-TimeOperating Systems (RTOSes). In this way, real-time tasks can be executed correctly, especially for cases of hard and firm real-time tasks. Several options are available on the market depending on the features they offer and the hardware devices on which they can be implemented.

Same examples of RTOSes based on proprietary code are: Azure RTOS [2.82], embOS [2.83], INTEGRITY [2.84], Junos OS [2.85], LynxOS [2.86], MQX [2.87], Nucleus RTOS [2.88], OS-9 [2.89], OSE [2.90], PikeOS [2.91], QNX [2.92], SAFERTOS [2.93], VxWorks [2.94].

Same examples of RTOSes based on open-source code are: Apache Mynewt [2.95], Apache NuttX [2.96], ChibiOS [2.97], ERIKA Enterprise [2.98], FreeRTOS [2.99], Fuchsia [2.100], RIOT [2.101], RT-Thread [2.102], RTEMS [2.103], seL4 [2.104], TI-RTOS [2.105], TRON [2.106], µC/OS [2.107], Zephyr [2.108].

2.4.2 Real-time extensions for standard OSes

While it is true that a RTOS would solve the problem of executing tasks with strict deadlines requirements, they are either expensive and difficult to afford or do not provide all the resources of widely used standard OSes (Windows, Linux, macOS).

Real-time extensions for open-source OSes have been developed over the last few years to counteract this problem by providing these systems with the ability to run high-priority tasks that require an immediate response upon the occurrence of certain events. In this way, it is possible to execute control tasks and have them behave deterministically while maintaining all the advantages provided by a standard OS.

Due to its open source philosophy, the focus will be on Linux-based operating systems. In order to improve real-time performance, there is a patch called RT_-PREEMPT [2.109] applicable to the Linux kernel, which enables a more aggressive preemption to minimize response time for real-time tasks.

Another option is to introduce a microkernel working in parallel to the standard Linux kernel (dual kernel) based on the HAL (Hardware Abstraction Layer) concept. In this way, modifications to the Linux kernel are non-intrusive, minimizing the impact

on non-critical tasks executed in the OS. Moreover, the microkernel has direct access to the hardware and can catch IRQs (Interrupt Requests) without intervention from the Linux kernel. Therefore, the execution of critical (real-time) tasks can be performed in the microkernel to improve response time. This is the case for RTAI [2.110] and Xenomai [2.111] real-time extensions.

2.4.3 System performance and control applications

Performance analyses of real-time extensions have been done to determine their suitability for executing real-time tasks, either for the RT_PREEMPT patch [2.112, 2.113], RTAI [2.113, 2.114] and Xenomai [2.112, 2.114–2.117].

These studies demonstrate the validity of these real-time extensions for performing firm real-time task execution and even hard real-time task execution. However, due to the uncertainties inherent to this type of implementations, it is advisable to perform a specific analysis on the hardware system where this type of real-time extensions are introduced in order to ensure their feasibility when executing critical tasks.

In literature, control applications of these real-time extensions are found [2.118–2.122], confirming their correct performance when executing tasks with strict timing requirements.

2.5 Power sharing in multiport power converters

The development of a multiport power converter allows the integration of different power units, whether they are sources, loads or energy storage devices in a single power converter [2.123, 2.124]. A common scenario for the development of multiport converters is the integration of multiple distributed energy resources in a microgrid, consisting of distributed generation resources (e.g., photovoltaic modules, wind turbines), supported by energy storage systems, for powering local loads and with the possibility of connection to the utility grid [2.125–2.129], as shown in Fig. 2.19.

This implies the need to manage the power sharing between the different power units so that there is a balance in the converter as a whole. Assuming that the sources and loads in the system have certain power flows imposed on them, the maneuverability of the converter lies in the energy storage units. Therefore, the literature concerning power sharing techniques focused on Energy-Storage Systems (ESSs) is reviewed, particularly in Hybrid ESSs (HESSs).

Firstly, different cases of HESSs are studied, considering the characteristics of the different devices that can be part of them, in order to determine the performance that can be obtained from them and therefore their suitability in different applications. From there, several techniques of power sharing between the different elements of the HESS are analyzed, taking into account their characteristics and the requirements imposed by the proposed application.

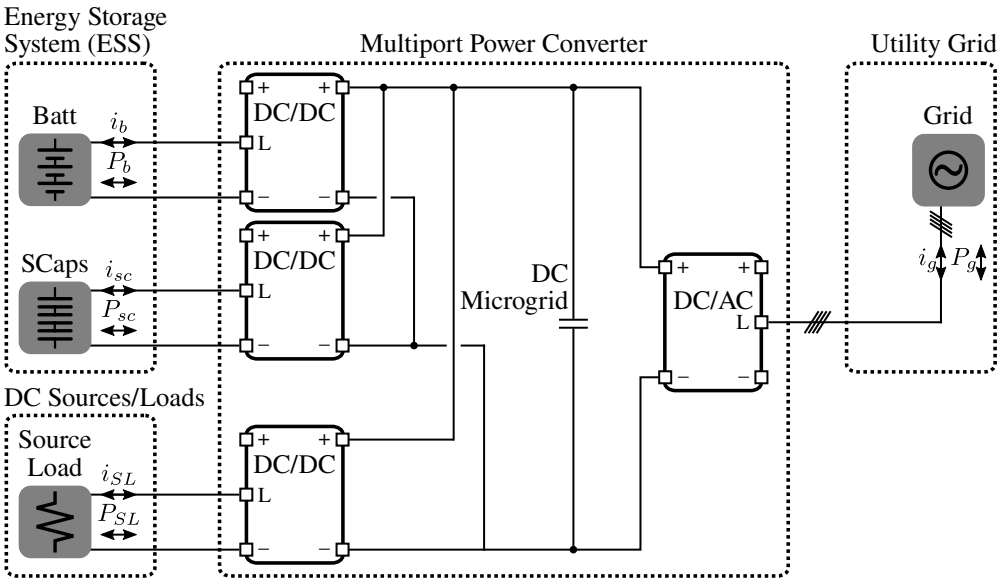

Figure 2.19: Multiport power converter for the integration of distributed energy resources in a DC microgrid: DC sources/loads, energy storage systems and possibility of connection to the utility grid.

2.5.1 Hybrid Energy-Storage Systems (HESSs)

Local small-scale power systems are being developed to promote the introduction of renewable energies, since they are closely related to distributed generation unlike the conventional ones. The concept of microgrid appears in order to categorize this type of systems, which are evolving over time [2.130]. Microgrids usually have some energy storage units to support the renewable power generation, which is non-deterministic.

Different kind of ESSs can be installed, some of them being more dedicated to the energy needs while others show their advantages in terms of power capability [2.131, 2.132]. Various energy storage technologies can be used for this purpose: batteries, supercapacitors, fuel cells, flywheels, superconductive magnetic energy storage, compressed air energy storage, pumped storage hydropower, thermoelectric energy storage.

Batteries are electrochemical devices that produce electrical energy by performing a series of internal chemical reactions. Their operation is based on the concept of a galvanic cell, which is capable of generating electric current from spontaneous redox reactions. Similarly, electrolytic cells are capable of producing non-spontaneous redox reactions by circulating an electric current through them. Therefore, the conjunction of both types of cells makes it possible to form an electrochemical cell capable of both generating electrical energy and storing it, depending on the voltage applied to the cell. There are several implementations of electrochemical cells depending on the type of chemistry used, with different performance in terms of voltage, current,

efficiency, energy density, power density, cycle life and self-discharge: Pb-Acid, Ni-Cd, Ni-MH, Li-Ion, NaS. Considering the above, the series and parallel connection of several electrochemical cells allows to form a battery with the desired nominal voltage and current values. Batteries have relatively high energy density but they are not suitable when suffering high variations of power. This is because the internal electrochemical reactions inside the battery produce a process of degradation [2.133, 2.134].

Supercapacitors are capacitors with a much higher capacitance value than conventional capacitors. This is achieved by a combination of electrostatic double-layer capacitance and electrochemical pseudocapacitance, unlike conventional capacitors that use solid dielectrics. Due to their capacitive behavior, supercapacitors allow a much faster exchange of electrical energy than batteries, increasing the number of charge and discharge cycles. In addition, they provide higher efficiency and power density, although their energy density is not too great and the level of self-discharge is high. Therefore, their use is recommended for applications with a high number of short-term power exchange cycles [2.135–2.137].

Fuel Cells (FCs) are electrochemical devices that produce electricity from the chemical reaction of hydrogen (fuel) with oxygen, generating water as a residue in the process. Their operation can be regenerative by integrating a water electrolysis process for hydrogen production. However, because they are usually optimized for either electricity generation or hydrogen production, the overall performance is reduced in the case of regenerative FCs. This fact, together with the degradation of their lifetime in dynamic applications, implies the recommendation to use them together with other energy storage systems tolerant to rapid power variations.

Flywheel ESS (FESS) is based on a mechanical device capable of storing rotational energy based on the law of conservation of angular momentum. This is achieved by spinning a rotating mass at very high speed, since its energy is linearly proportional to the moment of inertia and quadratically proportional to the angular velocity. The rotational mass is connected to an electric motor/generator through a rolling-element bearing to interact with the electric power system. In terms of performance, FESSs are very high power density devices, capable of withstanding a large number of charge/discharge cycles, require little maintenance and hence have a long service life. In addition, they have a considerable energy density on a par with batteries. However, their level of self-discharge is high due to the energy lost by friction in the bearings and air resistance. This can be minimized by using magnetic bearings and encapsulating the flywheel in a vacuum chamber, increasing the cost. Therefore, the use of FESSs is recommended for applications where a large number of short-term power pulses needs to be mitigated. It should be noted that the construction of a FESS requires certain minimum mass, area and volume values to avoid excessive rotational speed and thus ensure proper operation, making it more suitable for systems without strict size restrictions.

Compressed Air Energy Storage (CAES) is a technology that allows energy to be stored in the form of compressed air, in order to be used later through an expansion process. The great challenge of this type of storage is the complexity in its development,

since air compression/expansion is an exothermic/endothermic process that must be taken into account. Therefore, its use is limited to specific applications with favorable conditions for this technology, such as natural caverns as air reservoirs, and then only recommended for high power installations.

Pumped Storage Hydropower (PSH) is a technology that stores energy by pumping water to a certain height, so that it can later be used for hydroelectric generation via turbines. For an efficient implementation, large water reservoirs are required, which is generally carried out by taking advantage of natural watercourses such as rivers. Therefore, this technology is only recommended for very high power installations.

Superconducting Magnetic Energy Storage (SMES) is capable of storing energy in the form of a magnetic field by circulating a direct current through a superconducting coil. This requires a cooling system powerful enough to cryogenically cool the coil so that it reaches temperatures below the characteristic critical temperature. This endows this technology with one of the highest densities of ESSs, as well as high efficiency and low self-discharge. In addition, it has a very fast dynamic behavior. However, the cost of superconductors is high, so it is not usually a cost-effective technology except for specific applications requiring high performance.

Power converters are required to integrate the different ESSs into the power grid. Batteries, supercapacitors and FCs are considered as DC voltage sources, so they can be connected to a DC bus by using DC/DC converters to adapt their voltage. These converters have to be bidirectional to allow both absorption and supply of electrical power, following a boost topology if the bus has higher voltage and a buck topology otherwise. The DC bus can be connected to the electrical grid by means of an AC/DC power converter. SMES functions as a current source, so its integration can be done using an H-bridge. In FESSs, the flywheels is connected to an electrical machine, so two AC/DC power converters can be used in a back-to-back configuration for their integration into the electrical grid. The use of a matrix converter is also possible in the case of FESSs.

Considering the different characteristics of the various ESSs, it can be observed that certain technologies are more suitable as energy reservoirs, since they have better energy density and lower self-discharge level, while others are more suitable as power reservoirs, since they have better power density, better dynamic behavior and withstand a greater number of cycles during their useful life. In this way, by using different storage technologies in a joint ESS, it is possible to obtain an improved combined performance suitable in terms of both energy and power.

Such systems are known as Hybrid Energy-Storage Systems (HESSs), typically combining two types of ESSs, the first one focused on energy management (slow dynamics) and the other focused on power management (fast dynamics) [2.131]: battery and supercapacitor, battery and FESS, battery and SMES, FC and battery/supercapacitor. CAES and PSH are usually reserved to function as energy supplies for utility-scale applications.

In any case, the interconnection of High-Energy Storage (HES) and High-Power

Storage (HPS) units can be carried out using different configurations. Thus, HESSs can be classified into several topologies [2.131, 2.138–2.140]: passive, semi-active and active.

Passive interconnection topology consists in a direct connection in parallel of both HES and HPS units without using any power converter to interface with the DC bus. Therefore, this is the simplest and cheapest approach but has a lot of limitations:

- There is no control flexibility and the distribution of the power depends on the ESS impedances. Therefore, ESSs do not work in their optimal operating point.
- Both ESSs have to operate at the DC bus voltage due to the direct connection. This can produce fluctuations in the DC bus voltage.
- The system is not fault tolerant in the event of glsdc bus contingencies.

Semi-active interconnection topologies consist in introducing of a power converter for controlling one of the ESSs. This way, the performance of the HESS is improved since either the HES or the HPS is actively controlled. The most common configuration is that with controlled HPS, which allows the HPS to manage short-term power pulses, so that the HES simply manages the remaining energy with slow dynamics. Since HESSs usually provoke less voltage variations, this option provides less fluctuations on the DC bus voltage. However, the configuration with controllable HES can be used to maximize the lifetime of the HES, as it allows the power flowing through it to be precisely managed. On the downside, DC bus fluctuations are increased compared to the previous configuration. In any case, this type of topologies has the following characteristics:

- There is partial control flexibility and the distribution of the power greatly depends on the operation of the controlled ESS. However, the uncontrolled ESS is exposed to any unexpected power flow not properly managed by the power converter, which can affect its lifetime.
- Only the uncontrolled ESS has to operate at the DC bus voltage, reducing the fluctuations.
- The system is fault tolerant for the controlled ESS, but not for the uncontrolled ESS.

Active interconnection topologies consist in introducing separate power converters for controlling each of the ESSs. This way, the performance of the HESS is further improved since both the HES and the HPS are actively controlled. There are two possible configurations for active interconnection topologies: cascaded and parallel. In cascaded configuration, HES and HPS are cascaded with the power converters, being all of them connected in series. While this configuration allows both ESSs to be decoupled from the DC bus, it requires that the power converter directly connected to DC bus

is rated to the total power of the HESS. Moreover, a failure in the front-end power converter causes a malfunction of the entire HESS. In parallel configuration, each ESS is connected in parallel to DC bus through a specific power converter. This configuration reduces the rating of the power converters and ensures fully independent operation of each ESS. Therefore, parallel configuration is widespread for the implementation of active interconnection topologies, having the following characteristics:

- There is full control flexibility and the distribution of the power completely depends on the operation of both ESS. This eliminates any unexpected power flow in the ESSs, improving their performance and increasing their lifetime.
- Both ESSs are decoupled from the DC bus through the power converters, which allows them to operate with different voltage ratings and mitigates DC bus voltage fluctuations.
- The system is fault tolerant for both ESSs, so that they can be isolated from contingencies in the DC bus and can be independently disconnected from the power system due to internal malfunctions.

2.5.2 Power sharing techniques

The use of a HESS requires a power sharing strategy between the different ESSs in order to use each of them in the most optimal operating conditions. Focusing on the case of a combined use of batteries and supercapacitors in an active interconnection topology, several implementations of power sharing strategies are found in literature [2.138, 2.139, 2.141, 2.142].

This is the case of the power sharing strategy based on filtering. For this purpose, the power flowing through the HESS is classified into high-frequency and low-frequency components. The high-frequency components should flow through the supercapacitor since it offers better dynamic performance, whereas the low-frequency components should flow through the battery since it offers higher energy density to deal with steady-state power transfer. This can be done by using a Low-Pass Filter (LPF) to compute the low frequency components to flow through the battery or, similarly, by using a High-Pass Filter (HPF) to compute the high frequency components to flow through the supercapacitor. The remaining energy is to flow through the other ESS. Rate limiters can also be introduced to limit the maximum power variation per second in the battery.

Other type of power sharing strategy is based on Rule-Based Control (RBC). To carry out this strategy, a series of rules related to the state of the ESSs are defined to determine the global state of the HESS, in order to perform the most appropriate power sharing at each moment. One way to implement it is by means of a decision tree. This starts from an initial node that branches into different paths according to several conditions until it reaches one of the final nodes, which contains the information about the required power sharing.

Another implementation option for RBC is through the use of a state machine. It consists if the definition of a series of predefined states of the system, in which different tasks are carried out, related to the required power sharing for this case. The evolution from one state to another is marked by the transitions, which agglutinate those conditions that have to be fulfilled to make the change of state. The system is at all times in one of the predefined states, executing the associated tasks, and subsequently evaluating the transitions that originate in that state. If the conditions associated with one of these transitions are fulfilled, the system will go through it to change to the state where the transition ends.

Droop control can also be applied to implement the power sharing strategy. This type of control applied in hybrid storage systems is basically formed by a controller based on the existence of a virtual resistor connected in series at the output of the battery converter, known as Virtual Resistance Droop (VRD), and a controller based on the existence of a virtual capacitor at the output of the supercapacitor converter, known as Virtual Capacitance Droop (VCD). To improve its performance, mechanisms for voltage/SOC offset compensation can be introduced, either by implementing an integral controller in the VRD or via SVR controllers.

In addition, more complex control techniques can be used for implementing the power sharing strategy: Sliding Mode Control (SMC), Model Predictive Control (MPC), Fuzzy Logic Control (FLC), Artificial Neural Network (ANN), Particle Swarm Optimization (PSO), Water Cycle Algorithm (WCA), Shuffled Frog-Leaping Algorithm (SFLA).

2.6 Summary and research opportunities

In this chapter, a review of the state of the art has been made for those topics that are related to the development of a distributed control system for a multiport power converter based on power cells for the integration of distributed resources. After the review, several aspects have been detected where to develop a line of research, which are developed in the work of this thesis and shown below:

- The study of different PEBBs shows multiple implementations differentiated according to the power converter to be developed and the application where the converter is to be used. This approach is correct for the case where the converter topology is delimited and only some modularity is needed to improve its scalability depending on the application. However, for the case of a multiport converter, the integration of distributed resources implies differentiated power stages for each of the power resources, which in turn have to be replicated multiple times. Therefore, the approach of designing a versatile PEBB for easy replication with integrated measurement and its own control system appears. This allows to provide the PEBB with some intelligence to allow an autonomous control supervised

by a central controller, in order to facilitate the development of the converter control system. Regarding this topic, the modeling and dynamic analysis of a PEBB with integrated intelligence (iPEBB) adapted for use in multiport converters is carried out in the work of this thesis.

- The analysis of the structure of distributed control systems for power converters shows several possibilities for the organization of the various control layers that are part of it. For the case of the multiport converter to be managed in this thesis, the distributed controllers within the power blocks are simply in charge of performing autonomous control of the integrated power branch, but have no awareness of the power converter at a global level. Therefore, it becomes necessary to introduce a central controller for monitoring and sending references to the distributed controllers, receiving information from them for global decision making at system, application and converter level. In this way, the work of this thesis shows the implementation of a distributed control system adapted to multiport converters that follows a hierarchical structure based on distributed controllers integrated in the power blocks and a central controller in charge of managing them to operate the converter at a global level.

- The comparison of OSes shows different options for the management of hardware resources within a general purpose µP. The use of a general purpose µP allows the development of a digital platform suitable for a controller with extended features, combining in the same platform great computing capacity for the execution of complex algorithms, large storage capacity for the recording of historical data and graphic processing for flexibility in the development of HMIs. All this facilitating the access of the resources and tools available in an OS to the developer and user, providing great versatility to the digital platform. However, standard OSes do not provide the ability to execute tasks with firm RT constraints, as they do not guarantee responsive and deterministic behavior in the execution of critical high-priority tasks. Therefore, in the course of this thesis, the design of a digital platform based on a general purpose µP is proposed, in order to enable the implementation of the central controller of a distributed control system with extended functionality. Special attention is given to the integration of the OS inside the µP, showing the necessary modifications to enable the launching of tasks with RT constraints, a necessary condition for the execution of critical control tasks.

- The review of different ESSs used together with power converters shows the best combinations for the implementation of a HESS in a multiport converter. Such integration requires a power sharing algorithm that determines the power flow in both devices (power unit and energy unit) in order to maximize system performance. For the work developed in this thesis, a HESS consisting of a battery and a supercapacitor is integrated in a multiport converter connected to a grid with power constraints, in order to smooth the grid power flow profile when supplying a bidirectional local load. For this purpose, several compensation

methods for the power sharing algorithm are designed to operate under saturation conditions when the maximum grid power is reached and even under islanding conditions.

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Chapter 3

Dynamic modelling and design for the Intelligent PEBB (iPEBB)

3.1 Introduction

The use of modular power converters has become more widespread in recent years due to a greater integration of distributed generation with respect to traditional centralized generation. This has been largely driven by increased penetration of renewable energy generation, creating the concept of microgrids. As discussed in Chapter 2, this has resulted in the development of the Power Electronics Building Block (PEBB) concept.

However, most PEBB implementations do not have sufficient versatility to make them suitable for a wide range of applications. In some cases, this is due to the lack of intelligence within the PEBB whereas, in others, it is due to the implementation of a specific control for the proposed application. Because of this, the objective of this chapter is to develop a PEBB with sufficient intelligence to provide it with the necessary versatility for operation in AC/DC and DC/DC power conversion applications. The resulting PEBB will be known as Intelligent PEBB (iPEBB).

In this way, the combination of several iPEBBs makes it possible to form different power converter topologies depending on the needs of each application, as shown in Fig. 3.1. In the course of this chapter, the internal iPEBB structure required to enable the construction of multiple power converter topologies with a single iPEBB design is presented.

Initially, several widely used topologies for DC/DC, single-phase and three-phase

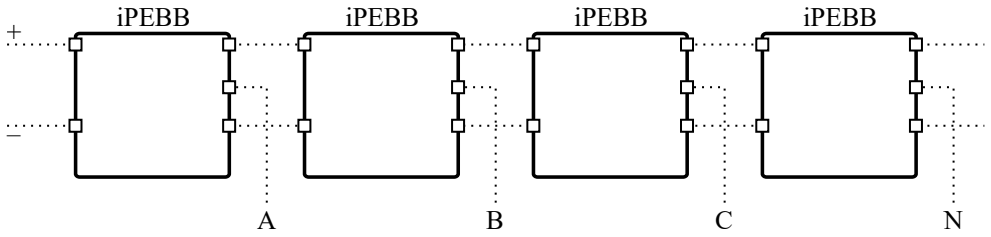

Figure 3.1: Power converter topology formed from iPEBBs.

DC/AC power conversions are analyzed, in order to propose a power stage for the iPEBB that is suitable to form different configurations of modular power converters.

Once the power stage for the iPEBB has been defined, the mathematical modeling in state-space representation of different power converter configurations based on the iPEBB is carried out.

Following the modeling of the power stage, the integration of the measurement and control system in the iPEBB is studied. In this way, the iPEBB is provided with the necessary intelligence to autonomously manage its operation, following a control law that determines the triggering of the power switches according to the estimated state of the system. Having concluded the above, the design of the iPEBB as an individual entity is finalized.

From this point on, power converter implementations based on the final iPEBB design are proposed, taking into account the different power conversions necessary for the integration of any power unit. At the same time, the distributed control structure necessary to manage the power converter as a whole is introduced, in order to set the starting point for a detailed analysis in future chapters.

3.2 Modeling of the iPEBB

The iPEBB design will be structured in three distinct parts. First, the dynamic modeling of the power stage will be studied, since it determines the main functionality of the iPEBB. Next, the measurement required to know the state of the iPEBB will be analyzed. Finally, the control devices required to operate the iPEBB properly will be described.

3.2.1 Power stage

The modeling of the power stage must be done in a way that allows versatile operation for AC/DC and DC/DC power conversion applications.

Regarding AC/DC power conversion, the AC grid can be single-phase or three-phase. In the case of a single-phase AC grid, there is the possibility of using a half-bridge topology or a full-bridge topology, as shown in Fig. 3.2. In the case of a three-phase AC grid, there is the possibility of using a 3-wire or 4-wire three-phase AC/DC power converter, as shown in Fig. 3.3. All these topologies have one or more parallel branches consisting of two power switches connected in series, with a top, bottom and middle connection point.

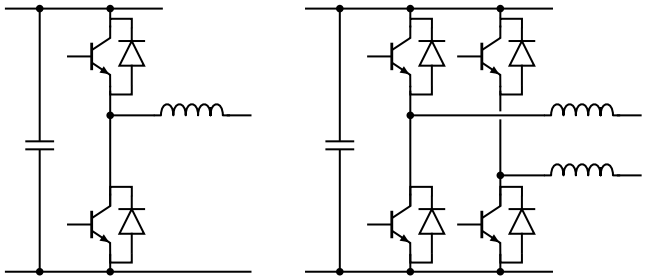

Figure 3.2: Single-phase AC/DC power converters: half-bridge and full-bridge topologies.

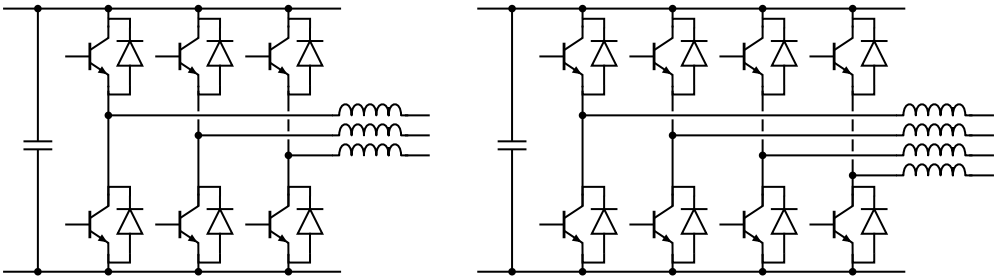

Figure 3.3: Three-phase AC/DC power converters: 3-wire and 4-wire topologies.

The interface of the converter with the DC side is made by interconnecting all the upper connection points of the branches to the positive terminal while the lower connection points are connected together to the negative terminal. A capacitive element is usually placed between the two terminals in order to filter possible variations in the DC voltage.

The output interface of the converter is made by connecting the middle point of each of the branches to an inductive or inductive-capacitive element, which acts as a filter to smooth the waveform of the current consumed/supplied to the load.

Regarding DC/DC power conversion, there are three main topologies of switching power converters: buck, boost and buck-boost. These topologies are shown in Fig. 3.4. All these topologies use one (buck and boost) or two (buck-boost) branches consisting of two power switches connected in series, with a top, bottom and middle connection point. In addition, they have a filtering element (generally an inductance) connected

to the middle connection point and may have a capacitive element at the converter output.

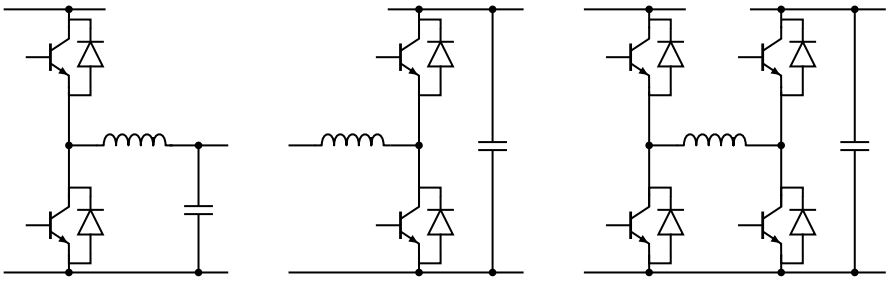

Figure 3.4: DC/DC power converters: buck, boost and buck-boost topologies.

Considering all of the above, the power stage of the iPEBB will consist of a branch with two power switches connected in series with a capacitor in parallel to the top and bottom connection points and an inductance in series to the midpoint of the power switches, as shown in Fig. 3.5.

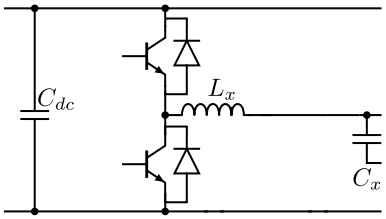

Figure 3.5: iPEBB: power stage.

3.2.2 State-space representation

The state-space representation allows to mathematically model the dynamic behavior of physical systems represented by differential equations (continuous domain) or difference equations (discrete domain). For this purpose, a set of internal states of the system (x) is defined, whose variation over time ($\dot{x}$) is given by their current value and by the value of a set of externally imposed inputs (u). From the value of the state variables and the value of the input variables, it is possible to determine the value of the output variables of the system (y). The relationship between states, inputs and outputs is given by four matrices (A, B, C, D), as shown in (3.1) and (3.2), resulting in the diagram shown in Fig. 3.6.

$$\dot{x} = Ax + Bu \tag{3.1}$$

$$y = Cx + Du \tag{3.2}$$

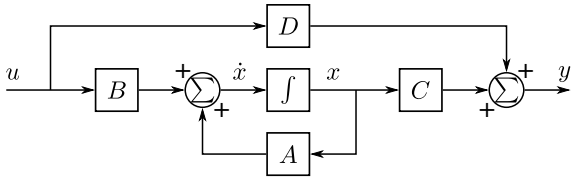

Figure 3.6: Diagram of state-space representation that enables a vector of system states (x) and outputs (y) to be obtained from a vector of system inputs (u).

Due to the aforementioned characteristics, the state-space representation has been used for modeling power converters [3.1–3.5], allowing a purely mathematical analysis of them and thus facilitating the simulation of their behavior by means of computer tools.

However, the use of a high frequency PWM for the operation of power converters would require a very small simulation time step (at least 20 times smaller than the switching period), which would imply a large number of iterations to appreciate relevant changes in the fundamental operating frequency. Assuming that the converter control actions are delivered once per switching period, the ripple inherent in a high-frequency modulation does not provide relevant information (provided the filtering is adequate) and its effect could be omitted. For this purpose, averaging methods based on the switching function concept can be used [3.6–3.11].

The switching function concept is based on defining a basic switching unit, known as a switching cell, and then defining its behavior for all realizable states during the switching period. From there, the mathematical function that encompasses such behavior, commonly known as the switching function, can be obtained. Starting from the switching function, and establishing a relationship between the PWM duty cycle and the operating time of each cell state during the switching period, it is possible to obtain the average function representative of the cell for each switching cycle. The value of this function for each switching period will depend directly on the duty cycle, so that the ripple effect caused by the high frequency modulation is eliminated, facilitating the analysis of the converter.

Considering all the above, the rest of the section shows a study of the expressions that determine the large-signal average model of the power converter configurations that are used in the development of the thesis, to then obtain the state-space representation of each one of them. In particular, the mathematical model of a half-bridge configuration for a DC/DC conversion, of a full-bridge configuration for a DC/1ph-AC conversion and of a three half-bridge configuration for a DC/3ph-AC conversion is obtained. From this point on, by analyzing the previous models, the modeling is generalized for configurations with an arbitrary number of half-bridge branches. In this way, a programmatic methodology applicable to the modeling of hybrid multiport power converters, which are formed by an arbitrary number of different power configurations, is obtained.

3.2.2.1 Half-bridge configuration

The most basic configuration that can be implemented with the iPEBB is a half-bridge converter, as it requires the use of a single unit to develop the power stage, as shown in Fig. 3.7. From Fig. 3.7, it is possible to determine the behavior of the large-signal average model, as given by (3.3)-(3.7), resulting in the diagram shown in Fig. 3.8.

$$i_{sw} = d \cdot i_L \tag{3.3}$$

$$u_{sw} = d \cdot u_{dc} \tag{3.4}$$

$$i_{dc} - i_{sw} = i_{Cdc} = C_{dc}\frac{\mathrm{d}u_{dc}}{\mathrm{d}t} \tag{3.5}$$

$$u_{sw} - u_{Cx} = u_L = L_x\frac{\mathrm{d}i_L}{\mathrm{d}t} \tag{3.6}$$

$$i_L + i_x = i_{Cx} = C_x\frac{\mathrm{d}u_{Cx}}{\mathrm{d}t} \tag{3.7}$$

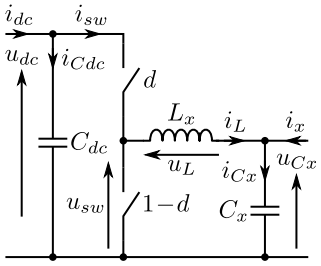

Figure 3.7: Electrical schematic of the half-bridge configuration.

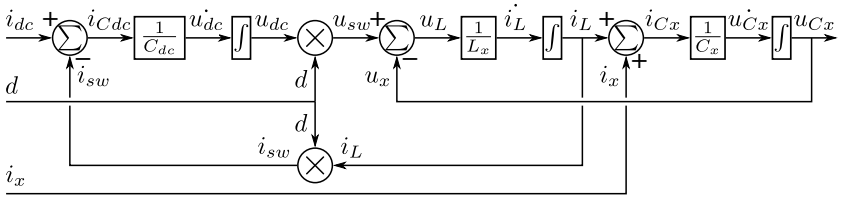

Figure 3.8: Large-signal average model of the half-bridge configuration.

This way, the inputs of the system would be the DC bus current (i_{dc}), the universal side current (i_x) and the duty cycle (d). Nevertheless, the large-signal average model is non-linear, as it can be seen in (3.3) and (3.4), which implies the appearance of time-varying elements in some matrices of the state-space representation. To address this issue, there are two representation options: either to include the duty cycle in some elements within matrix A (representation option 1), or to include the duty cycle in the input vector (u) by introducing other system variables into matrix B (representation

option 2). In any case, the state-space model become no-constant and operating-point dependent. The state variables are those affected by an integrator, which in this case correspond to the DC bus voltage (u_{dc}), the inductor current (i_L) and the universal side voltage (u_{Cx}). To simplify the modeling, the output variables are the same as the state variables. Therefore, the mathematical model of the half-bridge converter in state space is given by (3.8) and (3.9) for the representation option 1, and by (3.10) and (3.11) for the representation option 2.

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} u_{dc} \\ i_L \\ u_{Cx} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-d}{C_{dc}} & 0 \\ \frac{d}{L_x} & 0 & \frac{-1}{L_x} \\ 0 & \frac{1}{C_x} & 0 \end{bmatrix}\begin{bmatrix} u_{dc} \\ i_L \\ u_{Cx} \end{bmatrix} + \begin{bmatrix} \frac{1}{C_{dc}} & 0 \\ 0 & 0 \\ 0 & \frac{1}{C_x} \end{bmatrix}\begin{bmatrix} i_{dc} \\ i_x \end{bmatrix} \tag{3.8}$$

$$\begin{bmatrix} u_{dc} \\ i_L \\ u_{Cx} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} u_{dc} \\ i_L \\ u_{Cx} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} i_{dc} \\ i_x \end{bmatrix} \tag{3.9}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} u_{dc} \\ i_L \\ u_{Cx} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{L_x} \\ 0 & \frac{1}{C_x} & 0 \end{bmatrix}\begin{bmatrix} u_{dc} \\ i_L \\ u_{Cx} \end{bmatrix} + \begin{bmatrix} \frac{1}{C_{dc}} & 0 & \frac{-i_L}{C_{dc}} \\ 0 & 0 & \frac{u_{dc}}{L_x} \\ 0 & \frac{1}{C_x} & 0 \end{bmatrix}\begin{bmatrix} i_{dc} \\ i_x \\ d \end{bmatrix} \tag{3.10}$$

$$\begin{bmatrix} u_{dc} \\ i_L \\ u_{Cx} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} u_{dc} \\ i_L \\ u_{Cx} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{dc} \\ i_x \\ d \end{bmatrix} \tag{3.11}$$

3.2.2.2 Full-bridge configuration

The next configuration that can be implemented with the iPEBB is a full-bridge converter, as it requires the use of two units to develop the power stage, as shown in Fig. 3.9. From Fig. 3.9, it is possible to determine the behavior of the large-signal average model, as given by (3.12)-(3.15) for the DC side of the converter, (3.16)-(3.19) for the filtering inductors, (3.20)-(3.21) for the load side filtering capacitors, and (3.22)-(3.26) for the voltage of the common point of the load side filtering capacitors (u_{cn}),

resulting in the diagram shown in Fig. 3.10.

$$i_{swA} = d_A \cdot i_{LA} \tag{3.12}$$

$$i_{swB} = d_B \cdot i_{LB} \tag{3.13}$$

$$i_{swA} + i_{swB} = i_{sw} \tag{3.14}$$

$$i_{dc} - i_{sw} = i_{Cdc} = 2C_{dc}\frac{\mathrm{d}u_{dc}}{\mathrm{d}t} \tag{3.15}$$

$$u_{swA} = d_A \cdot u_{dc} \tag{3.16}$$

$$u_{swB} = d_B \cdot u_{dc} \tag{3.17}$$

$$u_{swA} - (u_{CxA} + u_{cn}) = u_{LA} = L_x\frac{\mathrm{d}i_{LA}}{\mathrm{d}t} \tag{3.18}$$

$$u_{swB} - (u_{CxB} + u_{cn}) = u_{LB} = L_x\frac{\mathrm{d}i_{LB}}{\mathrm{d}t} \tag{3.19}$$

$$i_{LA} + i_{xA} = i_{CxA} = C_x\frac{\mathrm{d}u_{CxA}}{\mathrm{d}t} \tag{3.20}$$

$$i_{LB} + i_{xB} = i_{CxB} = C_x\frac{\mathrm{d}u_{CxB}}{\mathrm{d}t} \tag{3.21}$$

$$\sum i_{Lk} + \cancelto{0}{\sum i_{xk}} = \cancelto{0}{\sum i_{Cxk}} \tag{3.22}$$

$$\sum i_{Lk} = 0 \tag{3.23}$$

$$\sum u_{Cxk} = 0 \tag{3.24}$$

$$\sum u_{swk} - \left(\cancelto{0}{\sum u_{Cxk}} + 2u_{cn}\right) = \sum u_{Lk} = L_x\frac{\mathrm{d}\cancelto{0}{\sum i_{Lk}}}{\mathrm{d}t} \tag{3.25}$$

$$\frac{1}{2}\sum u_{swk} = u_{cn} = \frac{\sum d_k}{2}u_{dc} \tag{3.26}$$

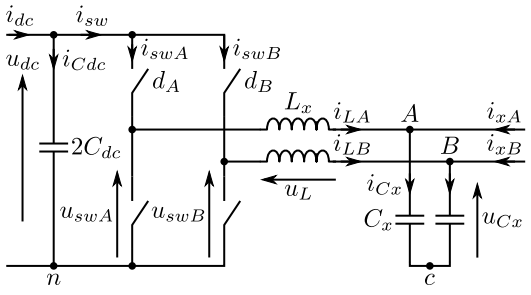

Figure 3.9: Electrical schematic of the full-bridge configuration.

By carrying out an analysis similar to the one described in Section 3.2.2.1, the mathematical model of the full-bridge converter in state space is obtained, as given by (3.27) and (3.28) for the representation option 1, and by (3.29) and (3.30) for the

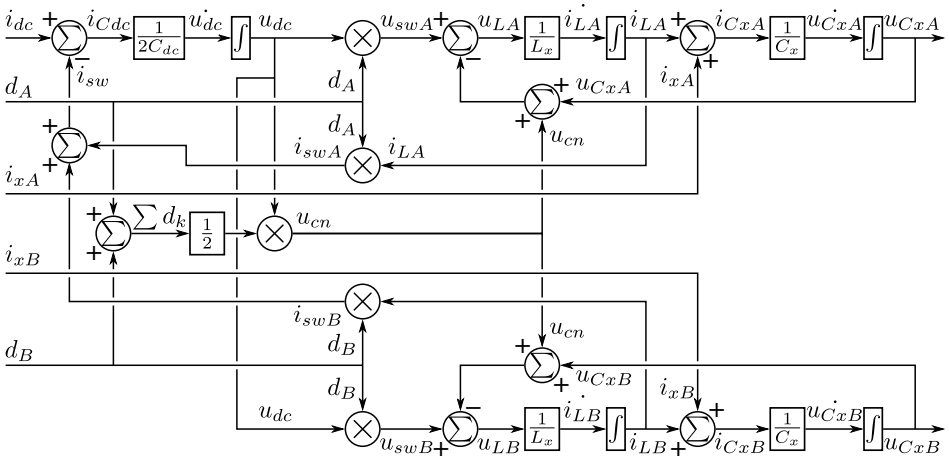

Figure 3.10: Large-signal average model of the full-bridge configuration.

representation option 2.

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ u_{CxA} \\ u_{CxB} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-d_A}{2C_{dc}} & \frac{-d_B}{2C_{dc}} & 0 & 0 \\ \frac{d_A - \sum d_k/2}{L_x} & 0 & 0 & \frac{-1}{L_x} & 0 \\ \frac{d_B - \sum d_k/2}{L_x} & 0 & 0 & 0 & \frac{-1}{L_x} \\ 0 & \frac{1}{C_x} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_x} & 0 & 0 \end{bmatrix} \begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ u_{CxA} \\ u_{CxB} \end{bmatrix} + \begin{bmatrix} \frac{1}{2C_{dc}} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{1}{C_x} & 0 \\ 0 & 0 & \frac{1}{C_x} \end{bmatrix} \begin{bmatrix} i_{dc} \\ i_{xA} \\ i_{xB} \end{bmatrix} \tag{3.27}$$

$$\begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ u_{CxA} \\ u_{CxB} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ u_{CxA} \\ u_{CxB} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{dc} \\ i_{xA} \\ i_{xB} \end{bmatrix} \tag{3.28}$$

$$\begin{aligned} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ u_{CxA} \\ u_{CxB} \end{bmatrix} &= \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_x} & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_x} \\ 0 & \frac{1}{C_x} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_x} & 0 & 0 \end{bmatrix} \begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ u_{CxA} \\ u_{CxB} \end{bmatrix} \\ &+ \begin{bmatrix} \frac{1}{2C_{dc}} & 0 & 0 & \frac{-i_{LA}}{2C_{dc}} & \frac{-i_{LB}}{2C_{dc}} \\ 0 & 0 & 0 & \frac{1}{2}\frac{u_{dc}}{L_x} & \frac{-1}{2}\frac{u_{dc}}{L_x} \\ 0 & 0 & 0 & \frac{-1}{2}\frac{u_{dc}}{L_x} & \frac{1}{2}\frac{u_{dc}}{L_x} \\ 0 & \frac{1}{C_x} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_x} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{dc} \\ i_{xA} \\ i_{xB} \\ d_A \\ d_B \end{bmatrix} \end{aligned} \tag{3.29}$$

$$\begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ u_{CxA} \\ u_{CxB} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ u_{CxA} \\ u_{CxB} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{dc} \\ i_{xA} \\ i_{xB} \\ d_A \\ d_B \end{bmatrix} \tag{3.30}$$

3.2.2.3 Three-phase half-bridge configuration

To address DC/3ph-AC power conversion, a three-phase half-bridge configuration can be implemented with the use of three iPEBBs, as shown in Fig. 3.11. From

Fig. 3.11, it is possible to determine the behavior of the large-signal average model, as given by (3.31)-(3.39), resulting in the diagram shown in Fig. 3.12.

$$k = \{A, B, C\} \tag{3.31}$$

$$i_{swk} = d_k \cdot i_{Lk} \tag{3.32}$$

$$\sum i_{swk} = i_{sw} \tag{3.33}$$

$$i_{dc} - i_{sw} = i_{Cdc} = 3C_{dc}\frac{\mathrm{d}u_{dc}}{\mathrm{d}t} \tag{3.34}$$

$$u_{swk} = d_k \cdot u_{dc} \tag{3.35}$$

$$u_{swk} - (u_{Cxk} + u_{cn}) = u_{Lk} = L_x\frac{\mathrm{d}i_{Lk}}{\mathrm{d}t} \tag{3.36}$$

$$i_{Lk} + i_{xk} = i_{Cxk} = C_x\frac{\mathrm{d}u_{Cxk}}{\mathrm{d}t} \tag{3.37}$$

$$\sum u_{swk} - \left(\sum \cancelto{0}{u_{Cxk}} + 3u_{cn}\right) = \sum u_{Lk} = L_x\frac{\mathrm{d}\cancelto{0}{\sum i_{Lk}}}{\mathrm{d}t} \tag{3.38}$$

$$\frac{1}{3}\sum u_{swk} = u_{cn} = \frac{\sum d_k}{3}u_{dc} \tag{3.39}$$

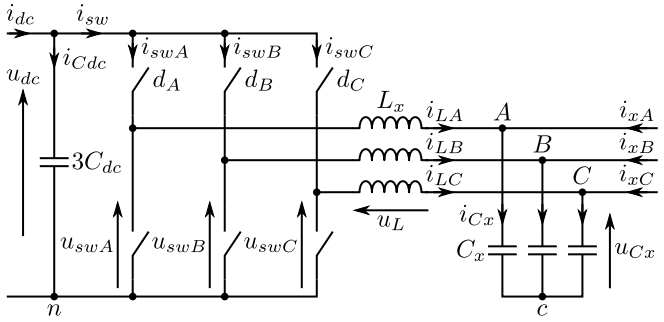

Figure 3.11: Electrical schematic of the three-phase configuration.

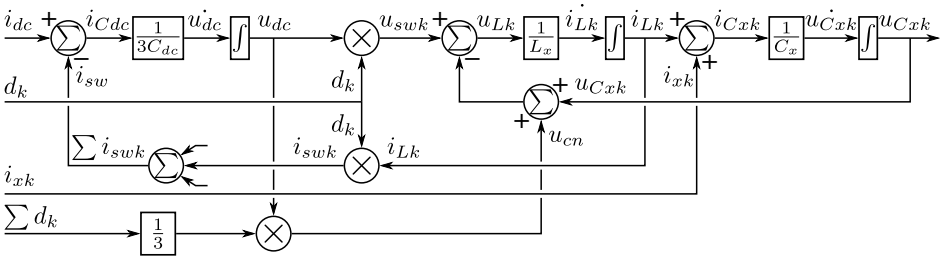

Figure 3.12: Large-signal average model of the three-phase configuration.

By carrying out an analysis similar to the one described in Section 3.2.2.1, the

mathematical model of the three-phase half-bridge converter in state space is obtained, as given by (3.40) and (3.41) for the representation option 1, and by (3.42) and (3.43) for the representation option 2.

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ i_{LC} \\ u_{CxA} \\ u_{CxB} \\ u_{CxC} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-d_A}{3C_{dc}} & \frac{-d_B}{3C_{dc}} & \frac{-d_C}{3C_{dc}} & 0 & 0 & 0 \\ \frac{d_A - \sum d_k/3}{L_x} & 0 & 0 & 0 & \frac{-1}{L_x} & 0 & 0 \\ \frac{d_B - \sum d_k/3}{L_x} & 0 & 0 & 0 & 0 & \frac{-1}{L_x} & 0 \\ \frac{d_C - \sum d_k/3}{L_x} & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_x} \\ 0 & \frac{1}{C_x} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_x} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_x} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ i_{LC} \\ u_{CxA} \\ u_{CxB} \\ u_{CxC} \end{bmatrix} + \begin{bmatrix} \frac{1}{3C_{dc}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_x} & 0 & 0 \\ 0 & 0 & \frac{1}{C_x} & 0 \\ 0 & 0 & 0 & \frac{1}{C_x} \end{bmatrix} \begin{bmatrix} i_{dc} \\ i_{xA} \\ i_{xB} \\ i_{xC} \end{bmatrix} \tag{3.40}$$

$$\begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ i_{LC} \\ u_{CxA} \\ u_{CxB} \\ u_{CxC} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ i_{LC} \\ u_{CxA} \\ u_{CxB} \\ u_{CxC} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{dc} \\ i_{xA} \\ i_{xB} \\ i_{xC} \end{bmatrix} \tag{3.41}$$

$$\begin{aligned} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ i_{LC} \\ u_{CxA} \\ u_{CxB} \\ u_{CxC} \end{bmatrix} &= \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_x} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_x} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_x} \\ 0 & \frac{1}{C_x} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_x} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_x} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ i_{LC} \\ u_{CxA} \\ u_{CxB} \\ u_{CxC} \end{bmatrix} \\ &+ \begin{bmatrix} \frac{1}{3C_{dc}} & 0 & 0 & 0 & \frac{-i_{LA}}{3C_{dc}} & \frac{-i_{LB}}{3C_{dc}} & \frac{-i_{LC}}{3C_{dc}} \\ 0 & 0 & 0 & 0 & \frac{2}{3}\frac{u_{dc}}{L_x} & \frac{-1}{3}\frac{u_{dc}}{L_x} & \frac{-1}{3}\frac{u_{dc}}{L_x} \\ 0 & 0 & 0 & 0 & \frac{-1}{3}\frac{u_{dc}}{L_x} & \frac{2}{3}\frac{u_{dc}}{L_x} & \frac{-1}{3}\frac{u_{dc}}{L_x} \\ 0 & 0 & 0 & 0 & \frac{-1}{3}\frac{u_{dc}}{L_x} & \frac{-1}{3}\frac{u_{dc}}{L_x} & \frac{2}{3}\frac{u_{dc}}{L_x} \\ 0 & \frac{1}{C_x} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_x} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_x} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{dc} \\ i_{xA} \\ i_{xB} \\ i_{xC} \\ d_A \\ d_B \\ d_C \end{bmatrix} \end{aligned} \tag{3.42}$$

$$\begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ i_{LC} \\ u_{CxA} \\ u_{CxB} \\ u_{CxC} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} u_{dc} \\ i_{LA} \\ i_{LB} \\ i_{LC} \\ u_{CxA} \\ u_{CxB} \\ u_{CxC} \end{bmatrix} \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{dc} \\ i_{xA} \\ i_{xB} \\ i_{xC} \\ d_A \\ d_B \\ d_C \end{bmatrix} \tag{3.43}$$

To improve the state-space representation, it is possible to pack the state, input (including the duty cycle) and output variables in three-phase column vectors, as shown in (3.44) and (3.45).

$$\left[i_L\right]_{3x1} = \begin{bmatrix} i_{LA} \\ i_{LB} \\ i_{LC} \end{bmatrix};\ \left[u_{Cx}\right]_{3x1} = \begin{bmatrix} u_{CxA} \\ u_{CxB} \\ u_{CxC} \end{bmatrix};\ \left[i_x\right]_{3x1} = \begin{bmatrix} i_{xA} \\ i_{xB} \\ i_{xC} \end{bmatrix} \tag{3.44}$$

$$\left[d\right]_{3x1} = \begin{bmatrix} d_A \\ d_B \\ d_C \end{bmatrix};\ \left[d'\right]_{3x1} = \left[d\right]_{3x1} - \frac{\sum \left[d\right]_{3x1}}{3} \tag{3.45}$$

This way, the final state-space model of the three-phase half-bridge configuration is obtained, as shown in (3.46) and (3.47) for the representation option 1, and (3.48) and (3.49) for the representation option 2.

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} u_{dc} \\ \left[i_L\right]_{3x1} \\ \left[u_{Cx}\right]_{3x1} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{3C_{dc}}\left[d^T\right]_{1x3} & \left[0\right]_{1x3} \\ \frac{1}{L_x}\left[d'\right]_{3x1} & \left[0\right]_{3x3} & -\frac{1}{L_x}\left[I\right]_{3x3} \\ \left[0\right]_{3x1} & -\frac{1}{C_x}\left[I\right]_{3x3} & \left[0\right]_{3x3} \end{bmatrix}\begin{bmatrix} u_{dc} \\ \left[i_L\right]_{3x1} \\ \left[u_{Cx}\right]_{3x1} \end{bmatrix} + \begin{bmatrix} \frac{1}{3C_{dc}} & \left[0\right]_{1x3} \\ \left[0\right]_{3x1} & \left[0\right]_{3x3} \\ \left[0\right]_{3x1} & \frac{1}{C_x}\left[I\right]_{3x3} \end{bmatrix}\begin{bmatrix} i_{dc} \\ \left[i_x\right]_{3x1} \end{bmatrix} \tag{3.46}$$

$$\begin{bmatrix} u_{dc} \\ \left[i_L\right]_{3x1} \\ \left[u_{Cx}\right]_{3x1} \end{bmatrix} = \left[I\right]_{7x7}\begin{bmatrix} u_{dc} \\ \left[i_L\right]_{3x1} \\ \left[u_{Cx}\right]_{3x1} \end{bmatrix} + \left[0\right]_{7x4}\begin{bmatrix} i_{dc} \\ \left[i_x\right]_{3x1} \end{bmatrix} \tag{3.47}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} u_{dc} \\ [i_L]_{3x1} \\ [u_{Cx}]_{3x1} \end{bmatrix} = \begin{bmatrix} 0 & [0]_{1x3} & [0]_{1x3} \\ [0]_{3x1} & [0]_{3x3} & -\frac{1}{L_x}[I]_{3x3} \\ [0]_{3x1} & -\frac{1}{C_x}[I]_{3x3} & [0]_{3x3} \end{bmatrix} \begin{bmatrix} u_{dc} \\ [i_L]_{3x1} \\ [u_{Cx}]_{3x1} \end{bmatrix} + \begin{bmatrix} \frac{1}{3C_{dc}} & [0]_{1x3} & -\frac{1}{3C_{dc}}[i_L^T]_{1x3} \\ [0]_{3x1} & [0]_{3x3} & \frac{u_{dc}}{L_x}\left([I]_{3x3} - \frac{1}{3}\right) \\ [0]_{3x1} & \frac{1}{C_x}[I]_{3x3} & [0]_{3x3} \end{bmatrix} \begin{bmatrix} i_{dc} \\ [i_x]_{3x1} \\ [d]_{3x1} \end{bmatrix} \tag{3.48}$$

$$\begin{bmatrix} u_{dc} \\ [i_L]_{3x1} \\ [u_{Cx}]_{3x1} \end{bmatrix} = [I]_{7x7}\begin{bmatrix} u_{dc} \\ [i_L]_{3x1} \\ [u_{Cx}]_{3x1} \end{bmatrix} + [0]_{7x7}\begin{bmatrix} i_{dc} \\ [i_x]_{3x1} \\ [d]_{3x1} \end{bmatrix} \tag{3.49}$$

3.2.2.4 N-branches half-bridge configuration

The comparison between the models obtained for the full-bridge configuration (Section 3.2.2.2) and the three-phase half-bridge configuration (Section 3.2.2.3) reveals a similar structure for both cases, only conditioned by the number of branches (2 for full-bridge configuration, 3 for three-phase half-bridge configuration). Thus, starting from the model shown in (3.44)-(3.49), a generic model for a N-branches half-bridge configuration can be proposed, as shown in (3.50)-(3.52) for representation option 1, and (3.53)-(3.54) for representation option 2.

$$[d']_{Nx1} = [d]_{Nx1} - \frac{\sum [d]_{Nx1}}{N} \tag{3.50}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} u_{dc} \\ [i_L]_{Nx1} \\ [u_{Cx}]_{Nx1} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{NC_{dc}}[d^T]_{1xN} & [0]_{1xN} \\ \frac{1}{L_x}[d']_{Nx1} & [0]_{NxN} & -\frac{1}{L_x}[I]_{NxN} \\ [0]_{Nx1} & -\frac{1}{C_x}[I]_{NxN} & [0]_{NxN} \end{bmatrix} \begin{bmatrix} u_{dc} \\ [i_L]_{Nx1} \\ [u_{Cx}]_{Nx1} \end{bmatrix} + \begin{bmatrix} \frac{1}{NC_{dc}} & [0]_{1xN} \\ [0]_{Nx1} & [0]_{NxN} \\ [0]_{Nx1} & \frac{1}{C_x}[I]_{NxN} \end{bmatrix} \begin{bmatrix} i_{dc} \\ [i_x]_{Nx1} \end{bmatrix} \tag{3.51}$$

$$\begin{bmatrix} u_{dc} \\ [i_L]_{Nx1} \\ [u_{Cx}]_{Nx1} \end{bmatrix} = [I]_{(2N+1)x(2N+1)} \begin{bmatrix} u_{dc} \\ [i_L]_{Nx1} \\ [u_{Cx}]_{Nx1} \end{bmatrix} + [0]_{(2N+1)x(N+1)} \begin{bmatrix} i_{dc} \\ [i_x]_{Nx1} \end{bmatrix} \tag{3.52}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} u_{dc} \\ [i_L]_{Nx1} \\ [u_{Cx}]_{Nx1} \end{bmatrix} = \begin{bmatrix} 0 & [0]_{1xN} & [0]_{1xN} \\ [0]_{Nx1} & [0]_{NxN} & -\frac{1}{L_x}[I]_{NxN} \\ [0]_{Nx1} & -\frac{1}{C_x}[I]_{NxN} & [0]_{NxN} \end{bmatrix} \begin{bmatrix} u_{dc} \\ [i_L]_{Nx1} \\ [u_{Cx}]_{Nx1} \end{bmatrix} + \begin{bmatrix} \frac{1}{NC_{dc}} & [0]_{1xN} & -\frac{1}{NC_{dc}}[i_L^T]_{1xN} \\ [0]_{Nx1} & [0]_{NxN} & \frac{u_{dc}}{L_x}\left([I]_{NxN} - \frac{1}{N}\right) \\ [0]_{Nx1} & \frac{1}{C_x}[I]_{NxN} & [0]_{NxN} \end{bmatrix} \begin{bmatrix} i_{dc} \\ [i_x]_{Nx1} \\ [d]_{Nx1} \end{bmatrix} \tag{3.53}$$

$$\begin{bmatrix} u_{dc} \\ [i_L]_{Nx1} \\ [u_{Cx}]_{Nx1} \end{bmatrix} = [I]_{(2N+1)x(2N+1)} \begin{bmatrix} u_{dc} \\ [i_L]_{Nx1} \\ [u_{Cx}]_{Nx1} \end{bmatrix} + [0]_{(2N+1)x(2N+1)} \begin{bmatrix} i_{dc} \\ [i_x]_{Nx1} \\ [d]_{Nx1} \end{bmatrix} \tag{3.54}$$

Following this structure, it is possible to obtain the dynamic behavior of a power converter with an arbitrary number of branches, such as a 4-wire three-phase converter. Substituting N for the number of branches (4 in this case), it is possible to compute the mathematical model in state space. The validity of the model is performed by using the MATLAB/Simulink simulation tool, since it allows a comparison between the switching model provided by the software itself and the large-signal average model obtained in this section.

For this purpose, each model is introduced in a separate implementation of the same power system, so as to reproduce a similar evolution in the inputs of the converter models on both sides. The results obtained for the switching model are shown in Fig. 3.13 for the dynamic evolution of the inputs and in Fig. 3.14 for the dynamic evolution of the outputs, whereas the results of the average model are shown in Fig. 3.15 and Fig. 3.16 respectively.

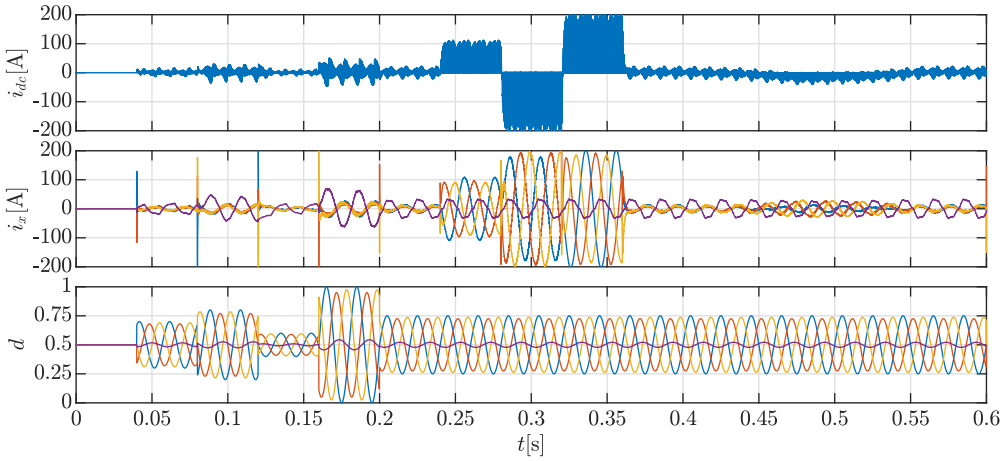

Figure 3.13: Dynamic evolution of the switching model of a 4-wire three-phase power converter: input vector.

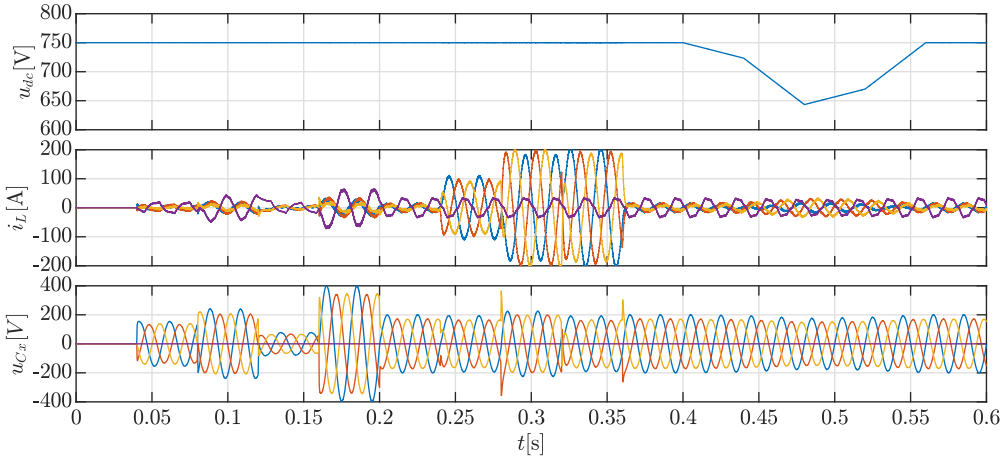

Figure 3.14: Dynamic evolution of the switching model of a 4-wire three-phase power converter: output vector.

As can be seen, the results of both models are equivalent except for the effect of the high frequency modulation, confirming a correct large-signal average model in the

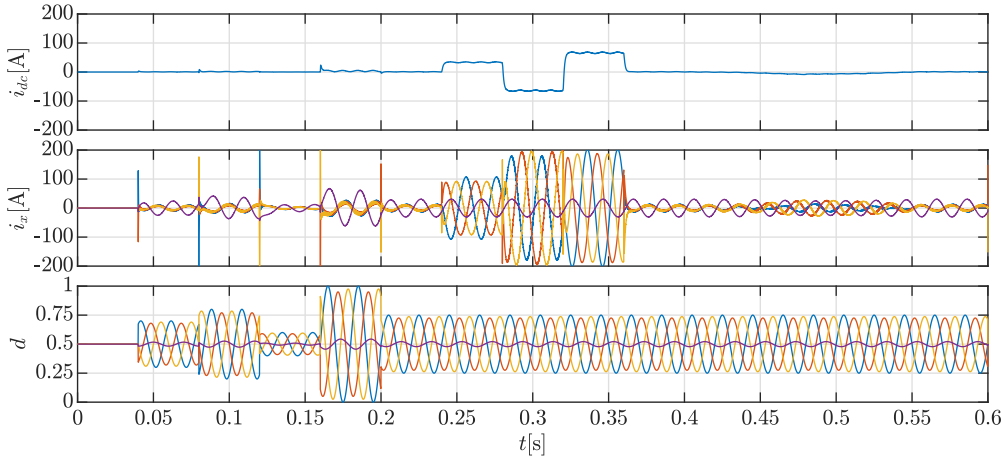

Figure 3.15: Dynamic evolution of the average model of a 4-wire three-phase power converter: input vector.

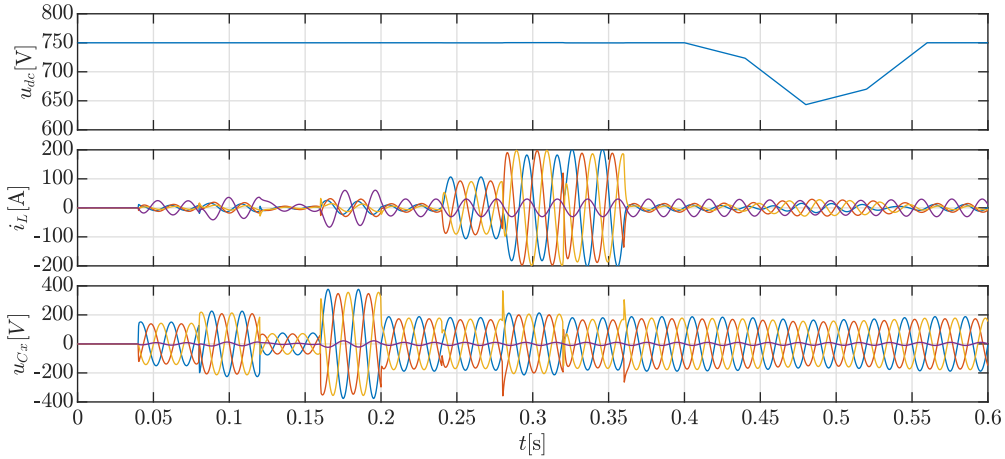

Figure 3.16: Dynamic evolution of the average model of a 4-wire three-phase power converter: output vector.

state space, allowing information to be obtained about the dynamic behavior of the power converter.

3.2.2.5 Hybrid multiport configuration

The configurations discussed in Sections 3.2.2.1, 3.2.2.2 and 3.2.2.3 have in common the interface to the DC bus, which is done by connecting the top and bottom terminals of each power switch branch to the DC bus with a capacitor in parallel. Therefore, it

is possible to form a hybrid multiport converter by integrating an arbitrary number of half-bridge, full-bridge and three-phase configurations sharing the same DC bus.

Focusing on representation option 1 and hence comparing (3.8), (3.27) and (3.46), and (3.9), (3.28) and (3.47), there is a great similarity between the matrices defining the state-space model of the different configurations. The only differences are in the duty cycles (d_k) and overall capacitance on the DC bus side (nC_{dc}), thus affecting only matrices A and B, whereas matrices C and D remain unchanged. Therefore, by following a procedure similar to the one outlined in Section 3.2.2.3 and resulting in (3.44) and (3.45), it is possible to package the multiple occurrences of each variable of similar nature in the different configurations of the multiport converter into column vectors. Assuming X half-bridge configurations, Y full-bridge configurations and Z three-phase configurations, the variable vector size (N), as shown in (3.55), obtaining the column vectors in (3.56) and (3.57).

$$N = X + 2Y + 3Z \tag{3.55}$$

$$\left[i_L\right]_{Nx1} = \begin{bmatrix} i_L^{hb1} \\ i_L^{hb2} \\ \vdots \\ i_L^{hbX} \\ \hline \left[i_L^{fb1}\right]_{2x1} \\ \left[i_L^{fb2}\right]_{2x1} \\ \vdots \\ \left[i_L^{fbY}\right]_{2x1} \\ \hline \left[i_L^{3ph1}\right]_{3x1} \\ \left[i_L^{3ph2}\right]_{3x1} \\ \vdots \\ \left[i_L^{3phZ}\right]_{3x1} \end{bmatrix}; \left[u_{Cx}\right]_{Nx1} = \begin{bmatrix} u_{Cx}^{hb1} \\ u_{Cx}^{hb2} \\ \vdots \\ u_{Cx}^{hbX} \\ \hline \left[u_{Cx}^{fb1}\right]_{2x1} \\ \left[u_{Cx}^{fb2}\right]_{2x1} \\ \vdots \\ \left[u_{Cx}^{fbY}\right]_{2x1} \\ \hline \left[u_{Cx}^{3ph1}\right]_{3x1} \\ \left[u_{Cx}^{3ph2}\right]_{3x1} \\ \vdots \\ \left[u_{Cx}^{3phZ}\right]_{3x1} \end{bmatrix}; \left[i_x\right]_{Nx1} = \begin{bmatrix} i_x^{hb1} \\ i_x^{hb2} \\ \vdots \\ i_x^{hbX} \\ \hline \left[i_x^{fb1}\right]_{2x1} \\ \left[i_x^{fb2}\right]_{2x1} \\ \vdots \\ \left[i_x^{fbY}\right]_{2x1} \\ \hline \left[i_x^{3ph1}\right]_{3x1} \\ \left[i_x^{3ph2}\right]_{3x1} \\ \vdots \\ \left[i_x^{3phZ}\right]_{3x1} \end{bmatrix} \tag{3.56}$$

$$[d]_{Nx1} = \begin{bmatrix} d^{hb1} \\ d^{hb2} \\ \vdots \\ d^{hbX} \\ \hline [d^{fb1}]_{2x1} \\ [d^{fb2}]_{2x1} \\ \vdots \\ [d^{fbY}]_{2x1} \\ \hline [d^{3ph1}]_{3x1} \\ [d^{3ph2}]_{3x1} \\ \vdots \\ [d^{3phZ}]_{3x1} \end{bmatrix}; \; [d']_{Nx1} = [d]_{Nx1} - \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ \hline \sum [d^{fb1}]_{2x1}/2 \\ \sum [d^{fb2}]_{2x1}/2 \\ \vdots \\ \sum [d^{fbY}]_{2x1}/2 \\ \hline \sum [d^{3ph1}]_{3x1}/3 \\ \sum [d^{3ph2}]_{3x1}/3 \\ \vdots \\ \sum [d^{3phZ}]_{3x1}/3 \end{bmatrix} \tag{3.57}$$

This way, knowing that the number of DC side capacitors in parallel is equal to variable vector size (N), the final state-space model of the hybrid multiport configuration is obtained, as shown in (3.58) and (3.59).

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} u_{dc} \\ [i_L]_{Nx1} \\ [u_{Cx}]_{Nx1} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{NC_{dc}}[d^T]_{1xN} & [0]_{1xN} \\ \frac{1}{L_x}[d']_{Nx1} & [0]_{NxN} & -\frac{1}{L_x}[I]_{NxN} \\ [0]_{Nx1} & -\frac{1}{C_x}[I]_{NxN} & [0]_{NxN} \end{bmatrix}\begin{bmatrix} u_{dc} \\ [i_L]_{Nx1} \\ [u_{Cx}]_{Nx1} \end{bmatrix} + \begin{bmatrix} \frac{1}{NC_{dc}} & [0]_{1xN} \\ [0]_{Nx1} & [0]_{NxN} \\ [0]_{Nx1} & \frac{1}{C_x}[I]_{NxN} \end{bmatrix}\begin{bmatrix} i_{dc} \\ [i_x]_{Nx1} \end{bmatrix} \tag{3.58}$$

$$\begin{bmatrix} u_{dc} \\ [i_L]_{Nx1} \\ [u_{Cx}]_{Nx1} \end{bmatrix} = [I]_{(2N+1)x(2N+1)}\begin{bmatrix} u_{dc} \\ [i_L]_{Nx1} \\ [u_{Cx}]_{Nx1} \end{bmatrix} + [0]_{(2N+1)x(N+1)}\begin{bmatrix} i_{dc} \\ [i_x]_{Nx1} \end{bmatrix} \tag{3.59}$$

3.2.3 Measurement

Having determined the power stage non-linear state-space average modelling, the next step involves measurement or estimation procedures to operate it conveniently at all times. To this end, the iPEBB must be provided with the appropriate instrumentation, so that the magnitude of certain variables representative of the state of the system can be measured. In particular, sensors will be placed in order to know the current state of three variables of the system.

The first measurement is the capacitor voltage between the positive and negative rails of the power switch branch. In the case of AC/DC power conversion, this measurement is important since it represents the DC voltage bus value, a fundamental variable for developing DC voltage control. In the case of DC/DC power conversion, its measurement is also relevant for conversions where it represents the output voltage, as in the case of boost and buck-boost topologies. In any case, it always represents a DC voltage, so it will be referred to as the DC voltage in the iPEBB design.

The second measurement is the series inductance current that is connected to the midpoint of the power switch branch. In the case of AC/DC power conversion, this measurement is important since it represents the value of current flowing through the inductive filter and, therefore, the current that is absorbed/supplied to the AC grid, a fundamental variable to develop the current control. In the case of DC/DC power conversion, its measurement is also relevant to carry out the input current control in the buck topology, the output current control in the boost topology and the intermediate current control in the buck-boost topology. Depending on the case, it can represent an AC or DC current, so it will be referred to as the universal current in the iPEBB design.

The third measurement is the voltage between the unconnected point of the series inductance and the bottom connection point of the power switch branch. In the case of AC/DC power conversion, this measurement is important since it represents the AC voltage value, a fundamental variable for developing AC grid synchronization techniques. In the case of DC/DC power conversion, its measurement is also relevant for conversions where it represents the output voltage, as in the case of buck topology. Depending on the case, it can represent an AC or DC voltage, so it will be referred to as the universal voltage in the iPEBB design.

The result of introducing all the instrumentation to the power stage is shown in Fig. 3.17.

3.2.4 Control system

Having determined all the instrumentation in the iPEBB, the final step consists of introducing the control system that can operate the power switches to meet the required objectives, all depending on the control loops implemented and depending on the information received from the instrumentation. For this, the control system has

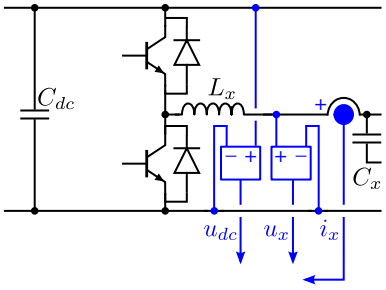

Figure 3.17: iPEBB: instrumentation.

to meet several requirements to be able to interact correctly with the power stage and the instrumentation.

First, an electronics stage is needed to adapt the analog signals emitted by the sensors so that they can be correctly interpreted. In addition, another electronics stage is needed to drive the gate of the power switches and carry out the required modulation. Finally, connectivity must be available to enable communication with external agents, since the exchange of information with the other controllers within a modular converter is essential for proper performance.

Based on the above, a control system based on a Digital Signal Processor (DSP) as the central element will be used, since there are options with integrated Analog-to-Digital (A/D) converters for reading analog sensors, with Pulse-Width Modulation (PWM) outputs for handling power switches, and with different communications protocols that provide connectivity. Around the DSP, all the necessary electronics will be included to adapt its voltage and current levels to those of the sensors, the power switch gates and the communications protocol. The result of introducing the control system to the iPEBB is shown in Fig. 3.18.

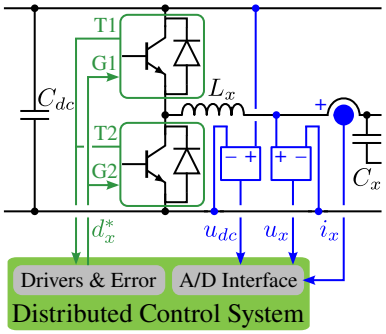

Figure 3.18: iPEBB: control system.

3.2.5 Final power block

External access shall be provided to the top and bottom connection points, which correspond to the positive (+) and negative (−) terminals, and to the point of the series inductance that is not connected, which corresponds to the inductance terminal (L). This will provide a basic power block that can be combined to build different AC/DC and DC/DC power conversion topologies, as shown in Fig. 3.19.

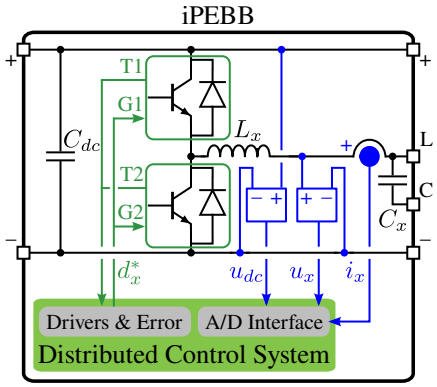

Figure 3.19: iPEBB: final power block.

3.3 Implementation of a multipurpose digital control in the iPEBBs

The main objective of each distributed controller is to manage the power supplied/absorbed by each iPEBB to/from each power unit. For this purpose, a current control loop is implemented to establish the required power flow in each of the iPEBBs.

In the particular case of having AC power units, there are is a new issue to consider in order to provide a complete operation by the system. It consists in the grid synchronization of the iPEBB if the power unit is an AC power generator, in order to provide a current/power correctly aligned with the AC supply voltage. Grid synchronization is necessary to determine the AC supply voltage frequency and phase, parameters that are used in the current control loop to generate an iPEBB current with the same fundamental frequency and the required phase shift. Therefore, grid synchronization is integrated into the distributed controllers of iPEBBs that are connected to AC power units.

Taking into account all the above, the structure of the iPEBB control system is determined, as shown in the Fig. 3.20. Each distributed controller integrated into a iPEBB receives as inputs the corresponding power magnitude (S^*) and phase shift (θ_S^*) references. From the universal voltage measurement (u_x), the grid synchronization is

carried out by estimating the fundamental frequency (f_e), the phase angle (θ_e) and the amplitude of the universal voltage (U_x). Using this information together with the power magnitude and phase shift references, the universal current reference (i_x^*) is computed. A current control loop is implemented, which compares the universal current measurement (i_x) with the reference to obtain the required duty cycle (d^*) for operating the power switches. The universal and DC-link voltage measurements are required to properly calculate the duty cycle, which is used by the PWM unit to trigger the power switches. Moreover, the estimation of the fundamental frequency is also required to adequately tune the controller under variations in the fundamental frequency of the power source.

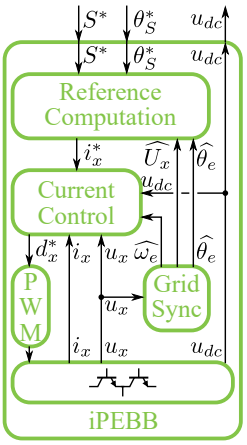

Figure 3.20: Structure of the iPEBB control system.

This section presents the implementation of the control system in the distributed controllers of the iPEBBs. The main subsystem is the current control loop so this section begins with an analysis of it and then focus on the other auxiliary subsystems that accompany it in order to achieve its purpose.

3.3.1 Analysis of the current control loop

The objective of the current control loop is to manage the current flowing through the series inductance so that it tracks the value imposed by a current reference and rejects any type of disturbance that is introduced into the system. This way, the iPEBB is able to control the current, and hence the power, exchanged with the power unit connected to it. The electrical diagram for the current control loop is shown in Fig. 3.21.

As can be seen, a variation in the inductance voltage (u_{Lx}) provokes a variation in the inductance current (i_x). Thus, the managing of the voltage generated by the triggering of the power switches (u) enables the modification of the inductance voltage

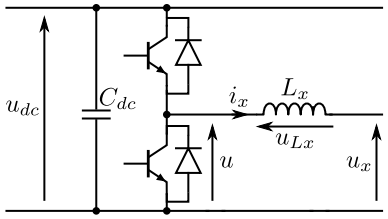

Figure 3.21: Electrical diagram for the current control loop.

and therefore the control of the current. Pulse-Width Modulation (PWM) is used to trigger the power switches in order to reduce the THD of the produced current, since the high-frequency harmonics present in the generated voltage are easily filtered by the inductance. The transfer functions and equations that define the behavior of the system are given by (3.60) and (3.61).

$$G_{Lx}(s) = \frac{i_x(s)}{u_{Lx}(s)} = \frac{1}{L_x s} \tag{3.60}$$

$$u_{Lx} = u - u_x \tag{3.61}$$

Taking all the above into account, a closed control loop is implemented as shown in the graphical diagram of Fig. 3.22. As can be seen, the error between the reference (i_x^*) and the measured value (i_x) is calculated, by which the control action to be applied on the system (u_{Lx}^*) is obtained according to the control law integrated in a digital controller (C). The duty cycle (d_x^*) is then computed depending on the nature of the power unit (DC or AC), in order to be used by the PWM subsystem to properly trigger the power switches.

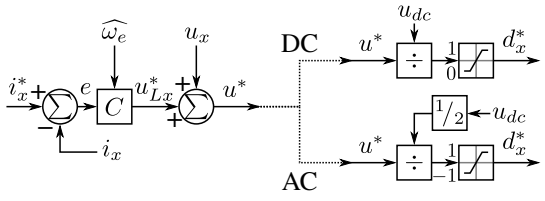

Figure 3.22: Implementation of the current control loop.

The power units connected to the iPEBBs can be either AC or DC. Therefore, in order to avoid distortion, the iPEBBs have to be able to control currents with constant and sinusoidal waveforms. In addition, harmonic compensation may be required in the case of interaction with AC sources/loads. Thus, the iPEBBs have to properly handle harmonic components of multiples of the fundamental frequency of the system. Due to the above, the analysis focuses on the study of resonant controllers, particularly the Proportional-Resonant (PR) controller and the Repetitive Controller (RC).

3.3.2 Selection of the optimal controller

3.3.2.1 Proportional-Resonant (PR) controller

The PR controller is a generalization of a Proportional-Integral (PI) controller centered at an arbitrary frequency. The PI controller is capable of achieve zero steady-state error for DC references (0 Hz) whereas the PR controller has to be capable of achieve zero steady-state error at the central frequency. The continuous transfer function of the PR controller is given by [3.12].

The implementation of a PR controller in discrete domain can be achieved both by discretization methods (often Tustin with pre-warping is used) or by direct-discrete design techniques. The first approach is easier to implement, but tracking of higher harmonics becomes difficult if the sample-time delay is not considered. In this chapter, direct-discrete design is used in order to extend the controller capabilities.

The derivation of the PR controller in discrete domain is obtained from the discrete PI expression shown at (3.62).

$$C_{PI}(z) = C_P(z) + C_I(z) = K_p + \frac{K_i T_s}{z-1} \tag{3.62}$$

Applying the same derivation as in [3.12] to (3.62), as shown in (3.63), the discrete PR controller is obtained. This PR controller has infinite gain at the resonance frequency (ω), and thus zero steady-state error at that frequency. When considering multiple harmonics, the expressions in (3.64) and (3.65) are obtained, which is related to the block diagram shown in Fig. 3.23.

$$C_{RES}(z) = C_{PI}(ze^{+j\omega T_s}) + C_{PI}(ze^{-j\omega T_s}) \tag{3.63}$$

$$C_{PR}(z) = C_P(z) + \sum C_{RES}(z) \tag{3.64}$$

$$C_{PR}(z) = K_p + \sum_{h\in\mathbb{Z}^*} \frac{2K_{ih}T_s\left[\cos(h\omega T_s)z - 1\right]}{z^2 - 2\cos(h\omega T_s)z + 1} \tag{3.65}$$

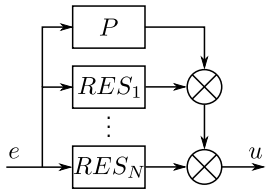

Figure 3.23: Proportional-Resonant (PR) controller.

As it can be observed, the coefficients of the PR controller have to be calculated using the fundamental frequency of the system, and the number of resonant controllers in parallel depends on the number of harmonics which is going to be taken into account. This makes this multiple-parallel-connected PR approach tedious to implement [3.13].

3.3.2.2 Repetitive Controller (RC)

The RC is mainly based on the concept that it is possible to generate a periodic signal with a fixed period by means of a system with a pure time delay equal to the signal period (T) and a unitary positive feedback around this delay [3.14]. Applying the internal model principle [3.15], it is possible to design a controller capable of tracking a periodic variable by including the model inside its scheme. The resultant controller is shown in (3.66) and Fig. 3.24.

$$C_{RC}(s) = K_{RC}\frac{e^{-sT}}{1-e^{-sT}} \tag{3.66}$$

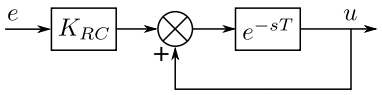

Figure 3.24: Repetitive Controller (RC).

The implementation of the RC into a digital control system is straightforward since the pure time delay is transformed into a number of control periods delay depending on the sampling frequency.

As stated before, the RC digital implementation offers simplicity as a main advantage. Nevertheless, the stability of this controller is compromised since the RC introduces a unitary positive feedback. Therefore, the final scheme of the RC has to be tweaked a little bit. The presented discrete RC is known as Direct RC (DRC) [3.16, 3.17]. The delay is now determined by an integer number of samples (N) and its expression is shown at (3.67) and Fig. 3.25.

$$C_{DRC}(s) = K_{RC}\frac{z^{-N}}{1-Q(z)z^{-N}}G_f(z) \tag{3.67}$$

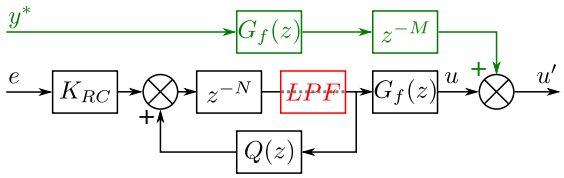

Figure 3.25: Direct RC (DRC) with feed-forward term (green path) and optional LPF in direct path (red block).

Compared to Fig. 3.24, in Fig. 3.25 there are two additional blocks, the robustness filter $Q(z)$ and the stability filter $G_f(z)$. The robustness filter is used to avoid a perfect positive feedback which could lead to an unstable system. There are several options for the robustness filter: constant value slightly lower than one, LPF, moving average

filter, etc. The stability filter is computed in order to achieve a Zero-Phase-Shift (ZPS) compensator [3.17], so that the dynamics of the power converter filter are compensated and its influence is attenuated: $G_f(z) = \hat{G}_{OL}^{-1}(z)$.

Compared to the multiple-parallel-connected PR, the DRC is easier to implement since it provides an infinite number of resonances at multiples of the fundamental frequency without need of parallelization. However, this behavior implies that the RC reacts to high-frequency harmonics, which can lead to an unstable behavior due to high-frequency noise. In order to avoid this behavior, two different topologies are accounted: 1) Robustness filter $Q(z)$ with constant value slightly lower than one and without LPF $\Rightarrow$ DRC; 2) $Q(z) = 1$ and LPF after the pure delay z^{-N} (Fig. 3.25 with red block) $\Rightarrow$ DRC_LPF.

Additionally, the RC has a drawback in the form of one fundamental period delay in order to track references (learning period). In order to reduce this effect, a feed-forward component of the reference through the block $G_f(z)$ is added to the action control of the controller as shown in Fig. 3.25 [3.18]. Note that $G_f(z)$ is not a proper system in this case, so an additional pure delay (z^{-M}) is included in the feed-forward path to make the resultant system biproper.

The iPEBBs of the modular converter are not computationally very powerful, so that the control topology is focused on the use of repetitive controllers to reduce the complexity of the computations as stated in Section 3.3.2.1. In particular, the DRC with LPF will be used to limit the bandwidth of the system.

3.3.2.3 Frequency shifts

The main problem of resonant controllers appears when the fundamental frequency is shifted with regard to the nominal frequency. In order to solve this problem, an adaptive frequency-dependent version of the resonant controllers has to be implemented.

Similarly, operation under variable frequency for the DRC case requires to adapt the delay value, as it depends on the ratio between the sampling frequency and the fundamental frequency. However, an integer relationship has to be kept according to the controller expression. Therefore, variations of the fundamental frequency cannot be fully compensated in a first approach (non-integer ratio). There are two options to solve this problem: 1) modifying the sampling frequency to achieve an integer delay or 2) implementing a fractional delay (z^{-F}) computation. The chosen option is the second one since the first would increase the complexity and the cost of the system. It is possible to halve the minimum delay of the controller as stated in [3.19] ($\omega_1 = 2$ and $\omega_2 = -1$ for even and odd harmonic compensation) but a better solution is addressed in [3.20], which is capable of compensating any kind of fractional delay by using a Lagrange-interpolating-polynomial-based fractional delay filter. A cubic interpolating polynomial is used: $z^{-F} \approx H_0 + H_1 z^{-1} + H_2 z^{-2} + H_3 z^{-3}$. The z^{-F} estimation block is placed just after the integer delay block (z^{-N}).

In this way, under frequency shifts, the integer part of the new ratio between sampling frequency and fundamental frequency will be considered by shifting the coefficients of the DRC (pure delay variation) whereas the non-integer part will be considered by changing the coefficients of the fractional delay filter.

3.3.3 Grid synchronization

In case the iPEBB is connected to an AC power source, it is necessary to synchronize with it to perform the required active and reactive power exchange by correctly aligning the current with the AC supply voltage. For this reason, a grid synchronization unit is integrated in the iPEBB distributed controller. The implementation consists in a Second-Order Generalized Integrator based Quadrature Signal Generator (SOGI-QSG) together with a Frequency Locked Loop (FLL) [3.21], as shown in Fig. 3.26.

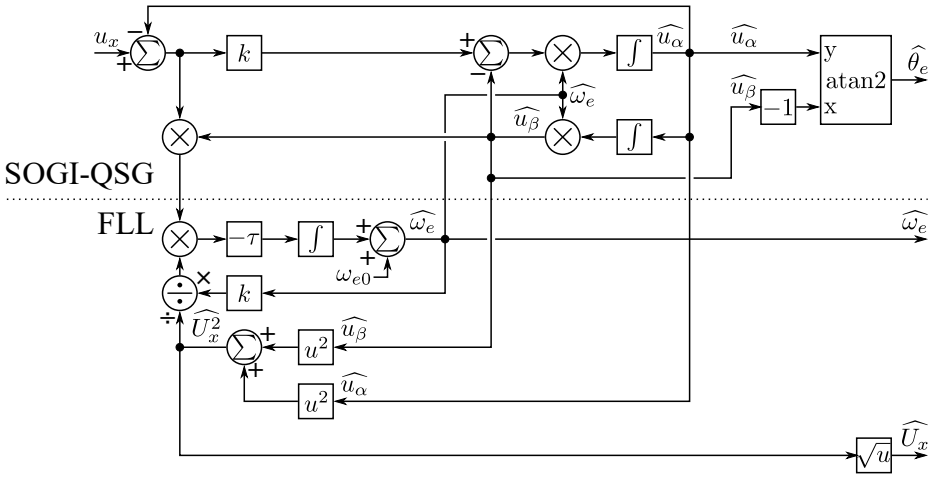

Figure 3.26: Grid synchronization unit: Second-Order Generalized Integrator based Quadrature Signal Generator (SOGI-QSG) together with a Frequency Locked Loop (FLL).

From the universal voltage measurement (u_x) and the fundamental frequency estimation (ω_e), the SOGI-QSG computes the in-phase (u_α) and quadrature-phase (u_β) components of the voltage. The arctangent (atan2) of these components determines the estimation of the phase angle (θ_e). In-phase and quadrature-phase components together with an initial value of the fundamental frequency (ω_{e0}) are used by the FLL to compute a estimation of the fundamental frequency (ω_e). In the process, an estimation of the magnitude of the universal voltage (U_x) can also be calculated.

Regarding all the information obtained from the grid synchronization unit, the fundamental frequency estimation is used by the resonant controller of the current control loop to tweak its gains conveniently, whereas the phase angle and voltage magnitude estimations are used by the reference computation unit to properly calculate the current reference for the current control loop.

3.3.4 Reference computation

The current control loop discussed in Section 3.3.1 requires a current reference in time domain (i_x^*) to be compared with the current measurement (i_x). However, the references received from the central controller are in terms of magnitude and phase shift. Thus, a reference computation unit is integrated into the iPEBBs to translate the information given by the central controller into a reference manageable for the current control loop.

In a dq0 synchronous reference frame, both the active and reactive power can be calculated using the expressions in (3.68) and (3.69).

$$P = \frac{3}{2}\left(u_d i_d + u_q i_q + 2u_0 i_0\right) \tag{3.68}$$

$$Q = \frac{3}{2}\left(u_q i_d - u_d i_q\right) \tag{3.69}$$

These expressions consider a voltage with non-zero q-axis and 0-axis components. Nevertheless, if the voltage source is practically balanced and free of harmonics, q-axis and 0-axis components of the voltage are negligible while d-axis component is constant. This way, power calculation is simplified, obtaining the expressions in (3.70) and (3.71) for the active and reactive power, and therefore (3.72) and (3.73) for the complex power.

$$P = \frac{3}{2} U_d I_d \tag{3.70}$$

$$Q = -\frac{3}{2} U_d I_q \tag{3.71}$$

$$\bar{S} = P + jQ = S\underline{/\theta_S} \tag{3.72}$$

$$\bar{S} = \frac{3}{2} U_d \left(I_d - jI_q\right) = \frac{3}{2} U_d I\underline{/-\theta_I} \tag{3.73}$$

By comparing (3.72) and (3.73) and applying them for the universal voltage/current case, the magnitude and phase shift of the current reference can be calculated from the information sent by the central controller as shown in expressions (3.74) and (3.75), and therefore the current reference in time domain for the current control loop as shown in (3.76). The final implementation of the reference computation unit is shown in Fig. 3.27.

$$I_x^* = \frac{2}{3}\frac{S^*}{\widehat{U_x}} \tag{3.74}$$

$$\theta_{Ix}^* = -\theta_S^* \tag{3.75}$$

$$i_x^* = I_x^* \sin\left(\widehat{\theta_e} + \theta_{Ix}^*\right) \tag{3.76}$$

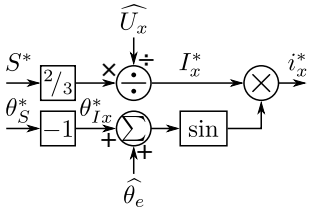

Figure 3.27: Reference computation unit.

3.4 Power converter implementation

Once the iPEBB is defined, it is possible to combine and connect several of them in order to build the desired power converter topology. This section will show several of the options that can be constructed using the iPEBB as the basic power unit, focusing on AC/DC and DC/DC power conversion.

3.4.1 AC/DC power converter

Regarding AC/DC power conversion, in the case of single-phase topologies, it is possible to opt for a half-bridge configuration by using a single iPEBB or a full-bridge configuration by using two iPEBB connected to each other through the DC port, as shown in Fig. 3.28.

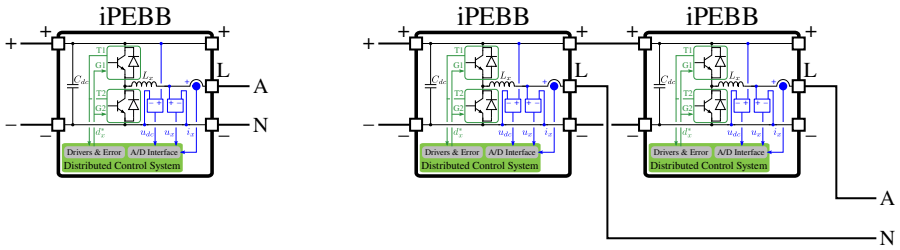

Figure 3.28: iPEBB single-phase AC/DC power converter.

The DC side is given by the positive (+) and negative (−) terminals, while the AC side is given by the inductance terminal (L) for the phase connection and the negative terminal (−) for the neutral connection in the half-bridge topology, and by the inductance terminals (L) of both iPEBB in the full-bridge topology.

For three-phase topologies, a 3-wire (without neutral connection) or 4-wire (with neutral connection) configuration can be built by using three or four iPEBB respectively connected to each other through the DC port, as shown in Fig. 3.29.

The DC side is given by the positive (+) and negative (−) terminals, while the AC side is given by the inductance terminals (L) of the iPEBB for the phase connections

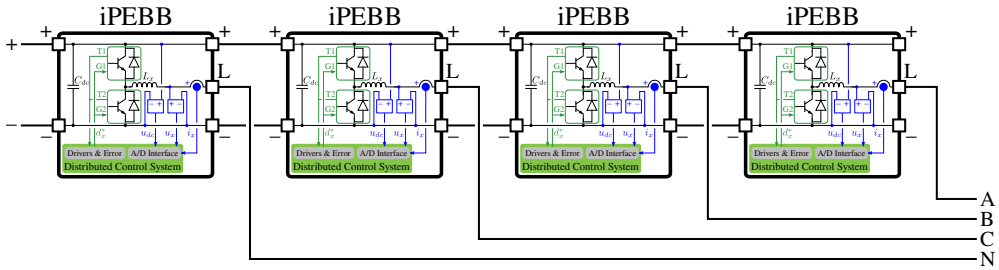

Figure 3.29: iPEBB three-phase AC/DC power converter.

and also for the neutral connection in the 4-wire configuration.

3.4.2 DC/DC power converter

Regarding DC/DC power conversion, it is possible to opt for a buck configuration by using a single iPEBB, a boost configuration by using a mirrored iPEBB and a buck-boost configuration by connecting a normal iPEBB and a mirrored iPEBB in series through the inductance (L) and the negative (−) terminals, as shown in Fig. 3.30.

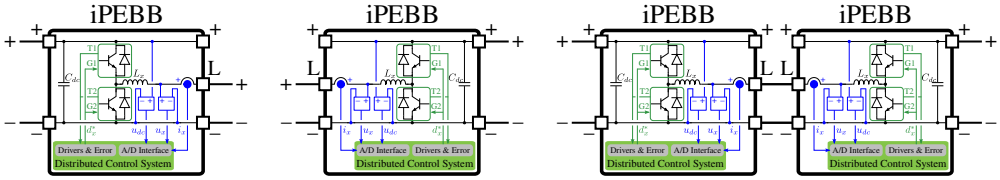

Figure 3.30: iPEBB DC/DC power converter.

For the buck topology, the input DC side is given by the positive (+) and negative (−) terminals whereas the output DC side is given by the inductance (L) and the negative (−) terminals. For the boost topology, the input DC side is given by the inductance (L) and negative (−) terminals whereas the output DC side is given by the positive (+) and the negative (−) terminals. For the buck-boost topology, the input DC side is given by the positive (+) and negative (−) terminals of the first iPEBB whereas the output DC side is given by the positive (+) and negative (−) terminals of the second iPEBB.

3.5 Distributed control structure

As seen in Section 3.4, the combination of iPEBBs allows the construction of different power converter topologies. However, and as discussed in Section 3.2, each iPEBB has an independent control system that must be properly programmed according to the

final application. In order to coordinate all iPEBBs with each other, the use of a hierarchical distributed control system based on a central controller in charge of managing the information received from the distributed controllers in the iPEBBs to command them properly and obtain the desired final operation in the converter is proposed, as shown in Fig. 3.31. The central controller will be based on a generic microprocessor with real-time capabilities and a fast communication channel to allow a proper coordination of all the system.

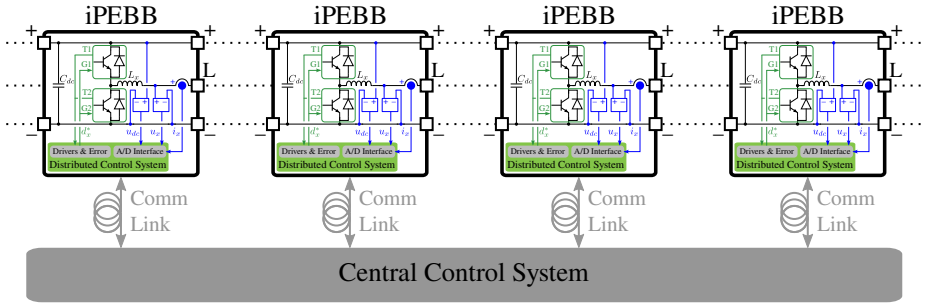

Figure 3.31: iPEBB distributed control.

The iPEBBs provide the interface with the global power system and hence their objective is to measure the electric variables (voltages and currents) and give the switching command to the drivers turning on/off the switches according to the desired control action. The central controller determines the application of the whole system by sending messages to the iPEBBs with information about the operating point. Therefore, considering the distributed control structure mentioned in Section 2.3.1, the distributed controllers in the different iPEBB will integrate the hardware and switching control layers, whereas the central controller will integrate the application and system control layers. Regarding the converter control layer, its integration will be divided between the two controllers to a greater or lesser extent depending on the system requirements.

The interface between the operator and the power converter is carried out through the central controller. Therefore, any adjustment that modifies the control algorithm or any of its parameters must be notified to the distributed controllers so that they can act accordingly. Analyzing the different options studied in Section 2.3.4, it has been decided to perform an initial programming of the distributed controllers by the central controller according to the implemented application, adding the possibility of reprogramming on the fly certain non-critical parameters of the control system.

The detailed analysis of the distributed control system will be carried out in the following chapters, where, in order to validate the feasibility of a power converter based on power cells, the final application to be implemented, the control loops required in the central controller and the distributed controllers, and the communication protocol that allows them to exchange information will be determined.

3.6 Conclusions

During the course of this chapter, the concept of a versatile power cell capable of forming various power converter configurations to meet different power conversion needs (DC/DC, DC/AC, DC/3ph-AC) has been developed, which is known as iPEBB.

Once the power stage of the iPEBB has been defined, the large-signal average mathematical modeling with state-space representation of the power converter topologies used in the development of this thesis has been presented, obtaining a modeling methodology for configurations with an arbitrary number of half-bridge branches, as well as for hybrid multiport configurations consisting of different topologies interconnected to each other through a common DC bus.

At the same time, the measurement elements introduced in the iPEBB, as well as the integrated control system, have been enunciated in order to provide the iPEBB with sufficient intelligence to operate autonomously.

Finally, several power converter topologies have been formed from the final design of the iPEBB, and the distributed control structure necessary for the control of the converter as a whole has been introduced, demonstrating the validity of the iPEBB concept developed throughout the chapter.

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Chapter 4

Analysis and development of a modular distributed digital control system platform

4.1 Introduction

Nowadays, the penetration of renewable energy generation is encouraging an evolution towards distributed generation systems, with the appearance of local small-scale power systems known as microgrids [4.1]. Microgrids opt for implementing hybrid generation using batteries, supercapacitors and flywheels [4.2, 4.3] to have a flexible and reliable operation. The increasing requirements regarding the number of switches, the switching frequency and the communication needs are driving the change of the control systems, moving from the central DSP/DSC based architecture to decentralized architectures [4.4]. The benefits of this approach can be summarized as: 1) scalability in terms of the needed inputs (A/D) and outputs (PWM), 2) flexibility and 3) reliability. However, there are some drawbacks that make the implementation more difficult than the one based on a central controller. In particular, the need of synchronization and communications as well as a change in the control design.

In order to accomplish a modular power converter, different proposals can be found in the literature using basic power cells [4.4, 4.5] to interface with the power system. This power cell is known as Power Electronics Building Block (PEBB) [4.5] and has to be controlled according to the desired power converter topology. Therefore, a distributed control system has to be developed in order to achieve a proper behavior of the modular power converter. This control consists of an individual autonomous control for each of the power blocks (inner current and voltage control loops), and a central controller to coordinate all the power blocks and provide a specific function to the

whole power converter (application-level control loops).

In a generic application-agnostic approach, the inner control loop of each power cell has to be capable of tracking references and rejecting disturbances of different polynomial order. In this chapter, the analysis is restricted to AC/DC and DC/AC power conversion, in which references and disturbances are expected at the fundamental harmonic frequency and its multiples. Based on the internal mode principle [4.6], the controllers need an internal harmonic generator model to properly manage harmonic references/disturbances. In this way, a theoretical zero steady-state error is achieved at the harmonic frequencies. Control techniques which meet this requirement are Proportional-Resonant (PR) controllers [4.7–4.9] and Repetitive Controllers (RC) [4.10–4.12].

The outer control loop of the central controller shall provide the control goals, i.e. references to the PEBB and receive the feedback signals for the control of the complete power converter through a communication channel, which implies the appearance of pure delays. The impact on the performance of these intrinsic pure delays have to be considered during the control system design.

The objective of this chapter is to tackle the control issues for the system explained above. The studied case will be a 4-wire 4-leg grid-tied inverter. Particular emphasis will be placed in the reference tracking and disturbance rejection of fundamental and non-fundamental harmonics. The behavior under changes in the fundamental frequency will be analyzed. Communication delays will also be taken into account.

In Chapter 3, the dynamic mathematical model in state space of different configurations of iPEBBs have been obtained, which has allowed the analysis of the inner control loop implemented in the distributed controllers for the iPEBBs, so that they are able to track power/current references with a fundamental frequency and harmonic content, as well as to reject disturbances that could distort the correct performance of the system. Therefore, it is possible to have an autonomous control of each iPEBB, but it does not enable a coordinated operation of all the iPEBBs as a whole for the final operation of a modular power converter.

This chapter shows the analysis and development of a modular distributed digital control system platform, consisting of an arbitrary number of distributed controllers in charge of the autonomous operation of each iPEBB and a single central controller in charge of coordinating the distributed controllers with each other. The central controller uses both information provided by the distributed controllers and information provided externally at a system level to determine the power/current references supplied to each distributed controller. In this way, full control of the modular power converter is achieved to ensure proper operation of the converter for integration into various applications. Part of the contents of this chapter is based on contribution "Distributed Control System for Modular Power Converters [CP2]" shown in Chapter 1.

4.2 Global structure

Starting from the iPEBB design explored in Chapter 3, the ultimate goal is to integrate a multiport converter that allows different AC and DC sources/loads to be connected together to exchange power with each other. Such iPEBBs have been designed to allow AC/DC and DC/DC power conversions, thus having one DC side and the other side configurable as AC or DC. Therefore, the different iPEBBs will be interconnected to each other through a DC bus via the positive (+) and negative (−) terminals, as shown in Fig. 4.1. The AC and DC power units will be connected to the inductance (L) and negative (−) terminals of the iPEBBs.

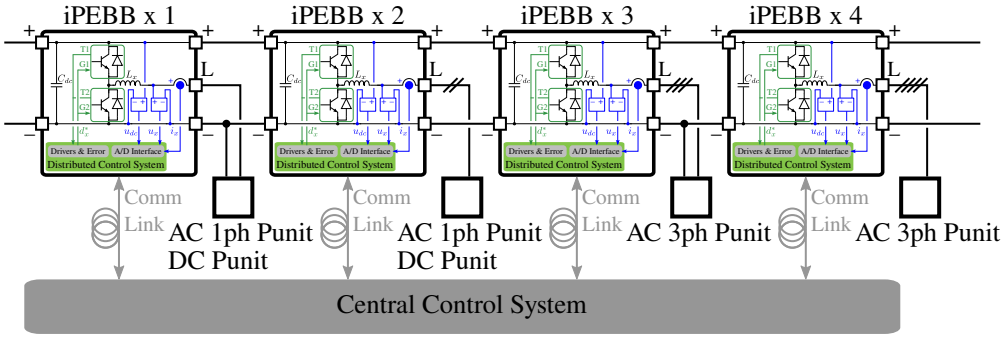

Figure 4.1: Global structure of the modular power converter for different types of power unit (Punit).

Taking the above into account, the proposed control system must manage, on the one hand, those variables that affect the overall system and, on the other hand, those variables that affect each of the iPEBBs and power units individually.

The central controller has to provide the power references to the distributed controllers depending on the system requirements. One of these requirements consists in controlling the DC-link voltage to a fixed value. This way, if the DC bus voltage is kept constant in steady state, the net power in the DC bus will be zero and power exchanges will only be done between the power units. Therefore, a DC-link voltage control loop is implemented into the central controller and whose control action is the power to be introduced into the DC bus.

The required DC-link power can be provided by any of the power units. Thus, there is an infinite number of combinations of power sharing between all the iPEBB. To solve this problem, a power sharing algorithm is integrated into the central controller to decide where to take the required power. This algorithm takes into account the characteristics and status of the different power units together with the required DC-link power to determine the power reference for each iPEBB.

In the particular case of having AC power units, there are is a new issue to consider in order to provide a complete operation by the system It consists in the capability to exchange reactive power with the power unit through the iPEBB. The phase shift of the

iPEBB current determines, together with its magnitude, the reactive power provided by the iPEBB. Thus, a phase shift reference has to be provided to the distributed controllers of the iPEBBs in addition to the power magnitude reference. Because of that, the central controller considers the required active power in certain loads/sources together with the DC-link voltage control loop and the reactive power in the power units to compute both the power magnitude and phase shift for each iPEBB.

Taking into account all the above, the overall structure of the distributed control system is determined, as shown in the Fig. 4.2.

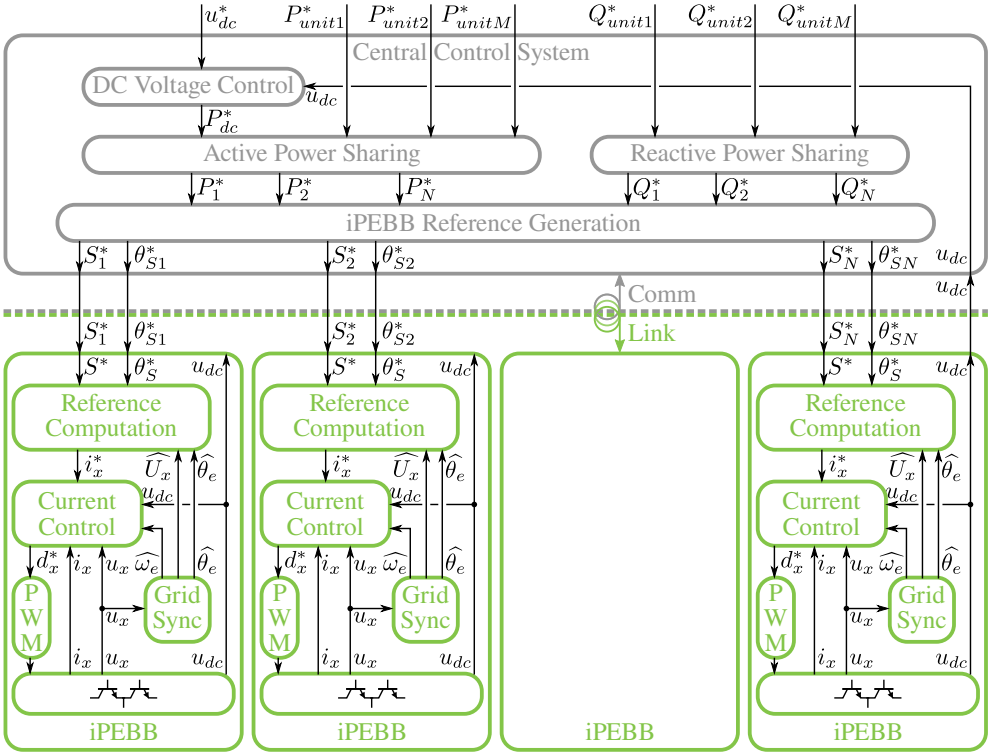

Figure 4.2: Global structure of the distributed control system.

The central controller receives as inputs the DC-link voltage reference (u^*_{dc}), the active power required at certain loads (P^*_{Loads}) and sources ($P^*_{Sources}$), and the reactive power to be exchanged with the different power units (Q^*_{unit1}, Q^*_{unit2}, ..., Q^*_{unitM}). It is responsible for computing the DC voltage control loop by using the actual DC-link voltage value (u_{dc}) measured by the iPEBBs together with the provided reference (u^*_{dc}), and whose output is the required DC power (P^*_{dc}). This power is used together with the required active power for certain loads/sources (P^*_{Loads}, $P^*_{Sources}$) by an active power sharing algorithm to determine the active power distribution among the different iPEBBs (P_{ipebb1}, P_{ipebb2}, ..., P_{ipebbN}). In the same way, a reactive power sharing algo-

rithm determines the reactive power distribution among the different iPEBBs (Q_{ipebb1}, Q_{ipebb2}, ..., Q_{ipebbN}) depending on the requirements of each power unit (Q^*_{unit1}, Q^*_{unit2}, ..., Q^*_{unitM}). Taking both the active and reactive power reference for each iPEBB, the output iPEBB power magnitude (S^*_1, S^*_2, S^*_N) and phase shift (θ^*_{S1}, θ^*_{S2}, θ^*_{SN}) references are calculated.

Having defined the overall structure, the following sections will explain the distributed control system in detail for the central controller.

4.3 Development of the central control in a general-purpose μP with RT capabilities

This section presents the development of the control system in the central controller, which is in charge of managing the iPEBBs to establish the behavior of converter as a whole. The main subsystem is the DC voltage control loop so this section begins with an analysis of it and then focus on the other auxiliary subsystems that accompany it in order to achieve its purpose.

4.3.1 Analysis of the DC voltage control loop

The objective of the DC voltage control loop is to manage the voltage located in the DC bus that interconnects all iPEBBs so that it tracks the value imposed by a voltage reference and rejects any type of disturbance that is introduced into the system. This way, the central controller is able to control the DC-link voltage to keep it constant and hence enabling power exchange between the iPEBBs through the DC bus. The electrical diagram for the DC voltage control loop is shown in Fig. 4.3.

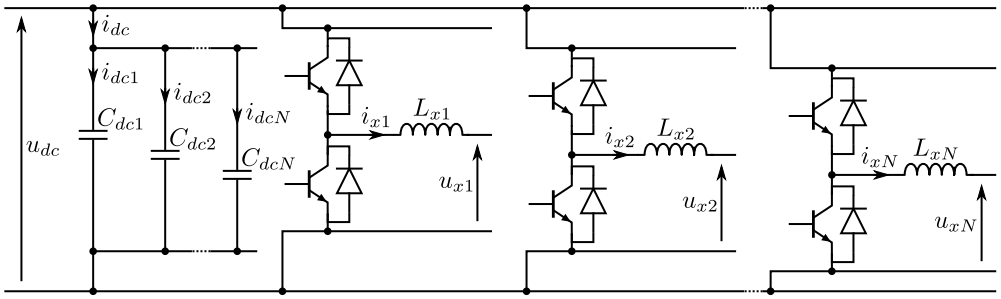

Figure 4.3: Electrical diagram for the DC voltage control loop.

As can be seen, a variation in the current flowing through the DC capacitors (i_{dc}) provokes a variation in the capacitance voltage (u_{dc}). Thus, the managing of the net power between all the iPEBBs enables the modification of the DC capacitor current

and therefore the control of the voltage. The transfer functions and equations that define the behavior of the system are given by (4.1)-(4.4).

$$G_{dc}(s) = \frac{u_{dc}(s)}{i_{dc}(s)} = \frac{1}{C_{dc}s} \tag{4.1}$$

$$P_{dc} = u_{dc} i_{dc} \tag{4.2}$$

$$P_{xi} = u_{xi} i_{xi} \tag{4.3}$$

$$P_{dc} + \sum_{i=1}^{N} P_{xi} = 0 \tag{4.4}$$

Taking all the above into account, a closed control loop can be implemented as shown in the graphical diagram of Fig. 4.4(a). As can be seen, the error between the reference (u^*_{dc}) and the measured value (u_{dc}) is calculated, by which the control action to be applied on the system (P^*_{dc}) is obtained according to the control law integrated in a digital controller. The voltage reference is expected to follow a constant or stepwise model, so that a PI controller (PI) is used to avoid steady-state error under reference tracking and disturbance rejection.

Figure 4.4: Implementation of the DC voltage control loop following (a) Direct Voltage Control (DVC) and (b) Quadratic Voltage Control (QVC) approaches.

Since the control loop manages directly the voltage, this scheme is known as Direct Voltage Control (DVC) [4.13]. An improved approach is to use the voltage squared by the control loop, a scheme called Quadratic Voltage Control (QVC) [4.13]. Fig. 4.4(b) shows its graphical diagram. Due to its improved performance and the direct obtaining of the required DC power (P^*_{dc}) from the control action of the controller, QVC is the selected option for the final implementation of the DC voltage control loop.

4.3.2 Active and reactive power sharing

The integration of different power units connected to the iPEBBs implies a power distribution among the units depending on the system state and the requirements imposed by external agents. Therefore, a power sharing algorithm is implemented in the central control system to perform accordingly the power distribution. This affects both active and reactive power, having a specific power sharing for each case depending on the requirements and restrictions.

Regarding active power sharing, (4.4) shows the need for a balance between the power flowing through all iPEBBs and the DC bus capacitors. Thus, active power sharing has to consider the required DC power obtained from the voltage control loop

to properly follow the DC-link voltage reference. This implies a flexible power flow in at least one of the power units to manage the power required by the DC bus. Considering all the above, an example of active power sharing is shown in Fig. 4.5(a). Active power sharing among the different power resources is further analyzed in Chapter 6, considering saturation events in the power conversion and their influence on the dynamic behavior of the system.

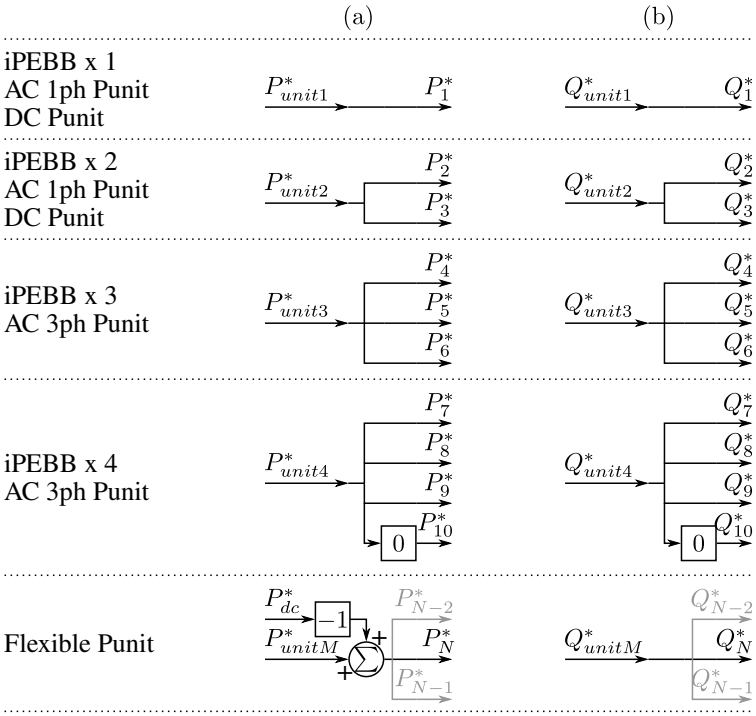

Figure 4.5: Example of active (a) and reactive (b) power sharing implementation.

Regarding reactive power sharing, unlike active power case, a balance between all the power units is not required to operate the whole system. Thus, there are no global restrictions when managing reactive power. The only limit is given by the sizing of the iPEBBs in terms of voltage and current. Considering all the above, an example of reactive power sharing is shown in Fig. 4.5(b).

4.3.3 iPEBB reference generation

Having done the power sharing to control the DC-link voltage and meet the system requirements, it is necessary to determine the setpoints for the iPEBBs to operate the converter conveniently. To do this, the central controller computes the complex power ($\bar{S}^*_i$) in polar form from the active (P^*_i) and reactive (Q^*_i) power references,

obtaining a magnitude (S_i^*) and phase angle (θ_{Si}^*) reference for each iPEBB, as shown in (4.5)-(4.7). The final implementation is shown in Fig. 4.6.

$$\bar{S_i^*} = P_i^* + jQ_i^* = S_i^* \angle \theta_{Si}^* \ , \quad i = 0, 1, ..., N \tag{4.5}$$

$$S_i^* = \sqrt{(P_i^*)^2 + (Q_i^*)^2} \tag{4.6}$$

$$\theta_{Si}^* = \text{atan2}\,(y = Q_i^*, x = P_i^*) \tag{4.7}$$

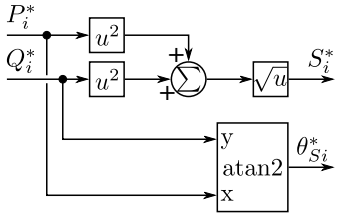

Figure 4.6: Implementation of iPEBB reference generation.

4.4 Analysis of the communication bus between central and distributed controllers

This section shows the development of a communication bus between the central and distributed controllers to allow the exchange of information between the different units of the system and thus enable the overall operation of the control system. For this purpose, an analysis of the layers of the OSI model for the communication channel common to all control units are studied. Due to the difficulty of performing a clear separation of all the layers, the analysis is structured in two parts. First, a joint analysis of the protocol addressing the higher-level layers is performed. After that, the focus is on the lower-level layers to select the option that best suits the needs of the system.

4.4.1 Development of the higher-layer protocol

In order to facilitate development, the communications bus should be based on standards that are widely used, well documented and easily accessible. Thus, the development of higher-layer protocol of the communication bus is based on CANopen standard. This standard is specially designed for implementation in embedded systems for automation applications, which makes it suitable for the proposed control system architecture. Although it was initially developed for use in conjunction with the lower-level CAN layer protocol, its implementation is sufficiently abstract to be used on different physical media.

Devices belonging to a network based on the CANopen protocol must have three main features for their correct implementation. The first feature is a communications

unit that manages the different types of messages that are part of the protocol to exchange information with the other nodes in the network. For this purpose, each device has a unique identifier and uses a state machine to perform device initialization/reset, pre-operation, operation and stop.

The second feature is an object dictionary that contains all those variables that contain information related to the operation of the device and must be exchanged over the communication bus. This object dictionary consists of an array of objects with 16-bit addressing (via index), which in turn consist of an array of variables with 8-bit addressing (via subindex). Therefore, each variable in the object dictionary is defined by an index/subindex, a name, data type and read/write attributes. It should be noted that certain indexes are reserved for the configuration of certain parameters of the standard and that only the range from 0x2000 to 0x5FFF should be used for custom variable definitions.

The final feature is an application unit that executes the main functionality of each device once it is properly initialized and therefore in an operational state. This unit interacts with the communications unit to exchange information with other nodes through the use of variables in the object dictionary.

CANopen frame is structured following the standard CAN frame format. Thus, it contains a 11-bit CAN identifier, a Remote Transmission Request (RTR) bit, a 4-bit data length field and 0 to 8 bytes of data. Moreover, the 11-bit CAN identifier is separated into a 4-bit function code referring to the type of CANopen message and a 7-bit CANopen node identifier, allowing up to 127 devices since 0 is reserved for broadcast.

Depending on the type of message indicated in the function code, several communication models are used between the different nodes. Master/slave model is used in Network Management (NMT) messages (function code: 0x0), where the master node sends commands to the slave nodes in order to perform the transitions in their internal state machines.

Client/server model is used in Service Data Object (SDO) messages (function code: 0xB for SDO transmission and 0xC for SDO reception), where the client sends a SDO reception message requesting an operation in a object dictionary variable (index/subindex) to be addressed by the server with the corresponding CANopen node identifier, which answers with a SDO transmission message with relevant information.

Producer/consumer model is used in Process Data Object (PDO) messages (function code: 0x3, 0x5, 0x7 and 0x9 for PDO transmission, and 0x4, 0x6, 0x8 and 0xA for PDO reception), where the producer sends messages with system information due to internal events (e.g., threshold limit or timer overflow), consumer request (RTR) or Synchronization (SYNC) producer message (function code: 0x1) to be addressed by the consumer. Heartbeat messages (function code: 0xE) also follows this model, where the producer informs the consumers about its availability by sending a cyclic message.

In the proposed architecture, the central controller takes the master role whereas all the distributed controllers operate as slaves. The state machine of each device

starts in initialization state and automatically evolves to pre-operation state while sending a boot-up (heartbeat) message in the transition. After that and during pre-operational state, the central controller (master) sends SDO messages to the distributed controllers (slaves) with configuration parameters and a NMT message at the end to move the slaves from pre-operational to operational state. Slaves confirm the transition by sending a heartbeat message. Once all the confirmation messages are received, the master evolves to operational state and the system starts to run the control algorithm.

At this point, the control system can operate either in asynchronous or synchronous mode. In asynchronous mode, each iPEBB updates the reference value and the central controller updates the corresponding measurement asynchronously once the communication is carried out. Accumulative delays take place between iPEBB variables, so that virtual unbalances appear. In synchronous mode, a SYNC message is added to the communication protocol in order to synchronize the different elements of the system. Only after this message, the elements of the system update their references/measurements, so that the accumulative delay effect disappears. Thus, synchronous mode is selected.

During normal operation, the central controller sends a cyclic SYNC message each iteration of the control loop together with transmit PDOs with relevant information for the distributed controllers, such as magnitude (S_i^*) and phase angle (θ_{Si}^*) references. Moreover, distributed controllers use the SYNC message to synchronize their operation and answer to the message with transmit PDOs with relevant information for the central controller, such as DC-link voltage (u_{dc}).

External references for the central controller, such as DC-link voltage reference (u_{dc}^*), active (P_{uniti}^*) and reactive (Q_{uniti}^*) power unit references, are sent by an external agent via SDO messages.

The implementation of CANopen protocol in the digital controllers is based on a free software CANopen framework called CanFestival, which is specially designed to develop master or slave CANopen nodes on RT IPCs and microcontrollers.

4.4.2 Selection of the physical and data link layers

CANopen protocol standard addresses network, transport, session, presentation and application layers of the OSI model. Therefore, only physical and data link layers remain to be analyzed.

The communication nodes of the control system are located in different devices, which makes SPI and I^2C communication standards not suitable for this application, since nodes are not located in the same PCB.

Regarding UART standards, RS-232 does not allow high transmission speeds (typically up to 115.2 kb/s) and does not have native multi-drop capabilities, so it is not recommended for this application. RS-422 standard allows higher transmission speeds (typically up to 10 Mb/s) and limited multi-drop capabilities (1 driver and 10 receivers), so it is only recommended for applications with low number of iPEBBs. RS-485 standard allows similar transmission speeds and truly multi-point networks (32 drivers and

32 receivers), being more suitable for the proposed application. In any case, these standards do not have a built-in arbitration method to avoid collision and use a weak error-detection technique such as bit parity. Thus, the software to operate them should include collision avoidance and better error-detection technique such as CRC to improve the communication bus performance.

CAN protocol overcomes this problem by introducing a 15-bit CRC and ACK check for error detection, and a dominant state for the logical 0 to introduce collision avoidance by prioritizing nodes with lower CAN identifier number. Moreover, number of nodes is not limited in the specification. Maximum transmission speed is 1 Mb/s, which is enough for the proposed application. In any case, a new specification called CAN FD allows transmission speeds up to 5 Mb/s if required. Considering all the above, CAN bus protocol is selected to implement both the physical and data link layers of the communication bus.

4.5 Control issues

The modular implementation approach used in this chapter implies the appeareance of some control issues, which are discussed hereunder: reference reconstruction and reference differentiability correction.

4.5.1 Communication channel

A communication channel is required in order to connect the central controller and the power cells. This implies an additional problem in comparison to conventional control schemes, which is the appearance of stochastic pure delays between the outer and the inner control loop. In the analyzed case, the central controller sends references to the power cells (current magnitude and phase shift) and receives measurements from them (DC link voltage). In order to reduce the cost and the complexity of the system, a common communication channel is used for the entire system. Two operation modes are considered in relation to the communication channel:

- Asynchronous mode. Each power cell updates the reference value and the central controller updates the corresponding measurement asynchronously once the communication is carried out. Accumulative delays take place between power cell variables, so that virtual unbalances appear.

- Synchronous mode. A synchronization message is added to the communication protocol in order to synchronize the different elements of the system. In this case, the synchronization message is sent after all the references/measurements sequence. Only after this message, the elements of the system update their references/measurements, so that the accumulative delay effect disappears.

In this chapter, the asynchronous mode is considered in order to avoid the need of synchronization among the different cells. This operation mode will be analyzed, and its effect over the error of the generated current will be considered as the figure of merit.

4.5.2 Reference reconstruction

The central controller is in charge of sending references to the individual iPEBBs. Since the control loop frequency of the power cells is higher than the control loop frequency of the central controller (a ratio of 10 for this research), the iPEBBs have a constant value for the reference between external loop iterations, thus leading to step-wise reference changes that cause additional distortion in the system, as shown in Fig. 4.7(a).

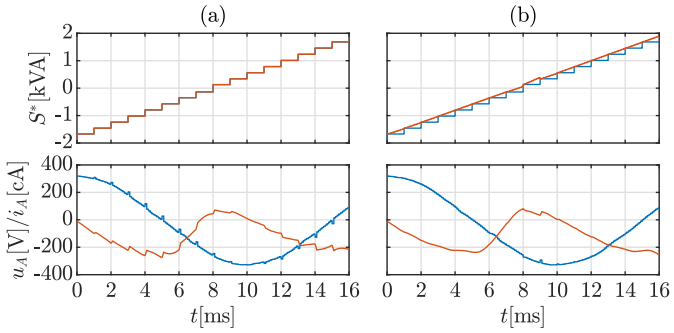

Figure 4.7: Comparison between the initial case (a) and the reconstructed reference case (b) for one phase of the converter. Top figures: blue, reference sent by the central controller; orange, reference built by the single-phase controller via extrapolation. Bottom figures: blue, converter voltage; orange, converter current.

To mitigate this problem, a linear extrapolation process at the iPEBB is proposed in this research in order to obtain a reference with a smoother shape for the intermediate iterations of the distributed current control with regard to the centralized voltage control, as shown in Fig. 4.8. The numerical expression is shown in (4.8).

$$x_k = \frac{x_{k'} - x_{(k-1)'}}{k_0 - k_{-1}} (k - k_0) + x_{k'} \tag{4.8}$$

After applying the linear extrapolation to the received reference, the results shown in Fig. 4.7(b) are obtained. As can be seen, the spikes in the converter voltage because of sharp reference changes are mitigated, and thus the converter current is smoother. Note that, the extrapolation used in this case is linear but higher order extrapolation algorithms can be used in order to improve slightly the performance.

This algorithm is applied in the iPEBB to the magnitude reference (S^*) but not to the phase shift (θ^*) in order to avoid an overcorrection of the whole reference.

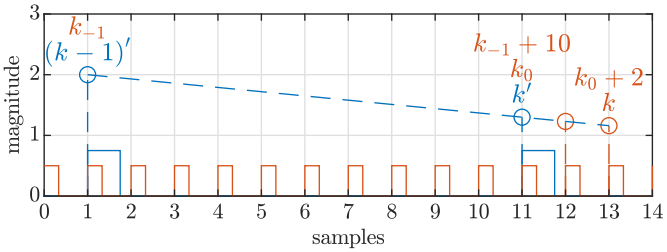

Figure 4.8: Graphical representation of the linear extrapolation process used to generate a smooth reference for the intermediate iterations of the distributed current control. Circular marks represent the samples of the control loops and square signals represent the control loop periods. Blue variables are related to the centralized voltage control whereas orange variables are related to the distributed current control.

4.5.3 Reference differentiability correction

As stated in Section 4.5.2, an extrapolation process is performed to determine the reference for the iPEBBs. In order to enhance the obtained result, the differentiability of the references given by the central controller can be improved. Whereas the phase shift (θ^*) can take any value, the magnitude (S^*) can only take positive values (modulus function), provoking differentiability issues when close to zero. Magnitude and phase shift represent the complex power reference of the central controller in polar form, so the expression in (4.9) is fulfilled.

$$S^* \angle \theta^* = (-1)^n S^* \angle \theta^* + n\pi \ , \ n \in \mathbb{Z} \tag{4.9}$$

This way, it is possible to assign negative values to the magnitude by modifying the phase shift, so that the differentiability is improved. Therefore, the central controller can apply corrections to the generated references in order to reduce non-differentiable occurrences whilst keeping the expected behavior of the system. The computation of the parameter n is designed with the purpose of reducing the difference between two consecutive samples of the phase shift (θ^*_k and θ^*_{k-1}) as much as possible. The resultant correction to be implemented in the central controller is shown in (4.10)-(4.12), obtaining the new corrected references ($S^{*\prime}_k$ and $\theta^{*\prime}_k$).

$$n = \lfloor 1/2 - (\theta^*_k - \theta^*_{k-1})/\pi \rfloor \tag{4.10}$$

$$S^{*\prime}_k = (-1)^n S^*_k \tag{4.11}$$

$$\theta^{*\prime}_k = \theta^*_k + n\pi \tag{4.12}$$

A graphical representation of this correction is shown in Fig. 4.9. As can be seen, the corrected phase shift has less variations than the original one and, as a consequence, the corrected magnitude has a smoother shape. This phenomenon allows the iPEBBs to improve the reconstruction of the magnitude reference used in the current control loop.

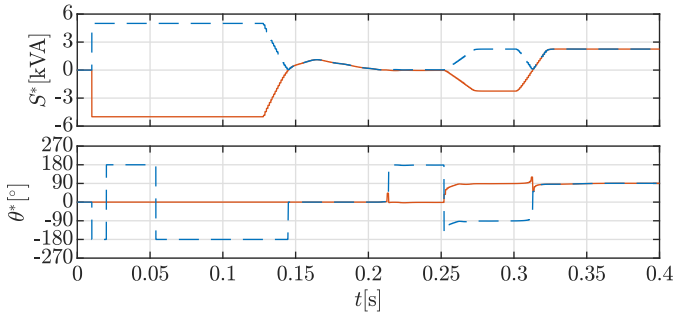

Figure 4.9: Graphical representation of applying a differentiability correction to the magnitude (S^*) and phase shift (θ^*) references. Blue: original case; red: corrected case.

4.6 Testing setup

In order to validate the proposed architecture, the modular converter will behave as a 4-wire 4-leg STATCOM connected to the grid. An schematic of the proposed architecture for the power converter is shown in Fig. 4.10. Therefore, the main objective of the test application is to compensate reactive power and mitigate unbalances and harmonics produced by the connection of local loads, so that the current at the PCC is balanced and does not contain any non-fundamental harmonics. Four iPEBBs are used to carry out the current control of the three active phases and the neutral phase (homopolar injection), whereas the central controller is in charge of the DC voltage control and the reactive power compensation. The DC voltage control uses a quadratic implementation to obtain directly the required power as control action [4.13].

The central controller sends messages with references of complex power magnitude (S^*) and phase shift (θ_S^*) to the iPEBBs depending on the requirements of the DC voltage control and the reactive power compensation, given by the DC voltage reference (u_{dc}^*) and the estimated load reactive power ($\widehat{Q_L}$). In addition, current references for the compensation of load unbalances and harmonics are sent to the iPEBBs ($i_{uh,n}^*$) by the central controller, depending on the estimated load current unbalances ($\widehat{i_{Labc,unb}}$) and harmonics ($\widehat{i_{Labc,har}}$).

Since the system is connected to the grid and is working with resonant single-phase controllers, a SOGI-FLL is implemented for each iPEBB to carry out the grid synchronization. This way, each iPEBB is capable of estimating the grid frequency and the grid voltage phase, and thus it can tune properly its resonant controller and compute the reference for the current control loop.

Taking all the above into account, the current control loop of the iPEBBs together with the reference computation unit are defined as shown in Fig. 4.11, whereas the central control system is implemented as shown in Fig. 4.12.

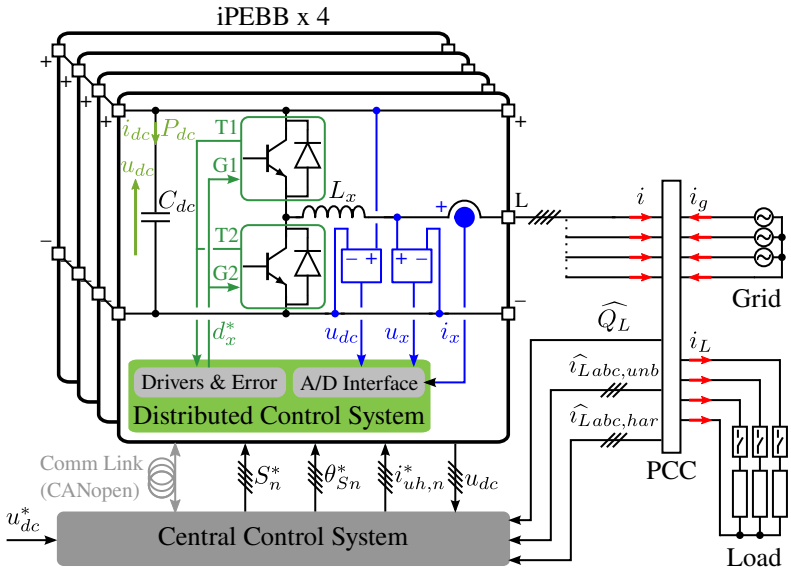

Figure 4.10: Proposed architecture for a modular power converter based on iPEBB. The application is for a 4-wire 4-leg STATCOM connected to the grid.

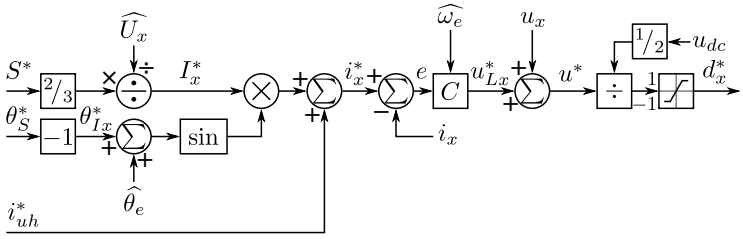

Figure 4.11: Implementation of the current control loop and reference computation unit for a 4-wire 4-leg STATCOM connected to the grid.

4.7 Simulation results

The simulation results are based on the system architecture shown in Fig. 4.10. The parameters are detailed in Table 4.1.

In order to determine the system performance, four different tests will be conducted: 1) Reactive power management and frequency shifts, 2) Connection of local linear loads, 3) Connection of local non-linear loads, and 4) Error from communication delays. The complete simulation profile is shown in Fig. 4.13. For the subsequent analysis, the three-phase variables will be shown in a theoretical synchronous reference frame (dq0) in order to ease the understanding of the results.

As shown in Fig. 4.13, different operating conditions are evaluated: 1) At 0.01 s,

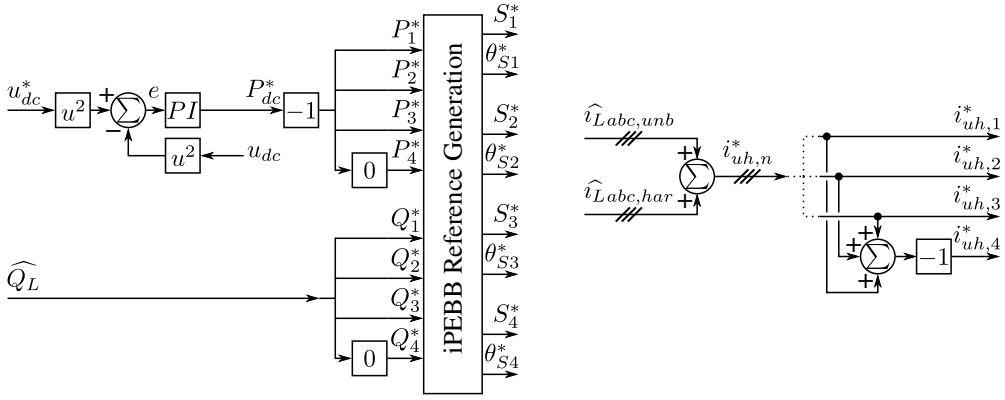

Figure 4.12: Implementation of the central control system for a 4-wire 4-leg STATCOM connected to the grid.

Table 4.1: System parameters.

Parameter	Value
Active phase filter inductance (L)	7 mH
Active phase filter resistance (R)	0.3 Ω
Neutral phase filter inductance (L_n)	3 mH
Neutral phase filter resistance (R_n)	0.06 Ω
DC link total capacitance (C_{dc})	5.04 mF
Nominal DC link voltage (U_{dc})	750 V
Sampling/PWM frequency	10 kHz
Current (iPEBB) control loop frequency	10 kHz
DC link voltage (central) control loop frequency	1 kHz
Nominal grid line RMS voltage	400 V
Nominal grid frequency	50 Hz

the control is enabled; 2) At 0.2 s, a three-phase resistive load of 3 kW is connected to the PCC with a bandwidth of 100 Hz; 3) At 0.25 s, the load starts operating with a capacitive power factor of 0.8 with a bandwidth of 100 Hz; 4) At 0.3 s, the load starts operating with an inductive power factor of 0.8 with a bandwidth of 100 Hz; 5) At 0.4 s, the grid frequency is changed from 50 Hz to 47.2 Hz; 6) At 0.5 s, the grid frequency is changed from 47.2 Hz to 50 Hz; 7) At 0.6 s, a load of 1 kW with an inductive power factor of 0.8 is connected to the PCC between phase A and neutral phase; 8) At 0.66 s, a load of 1 kW with an inductive power factor of 0.8 is connected to the PCC between phase B and neutral phase; 9) At 0.72 s, a load of 1 kW with an inductive power factor of 0.8 is connected to the PCC between phase C and neutral phase.

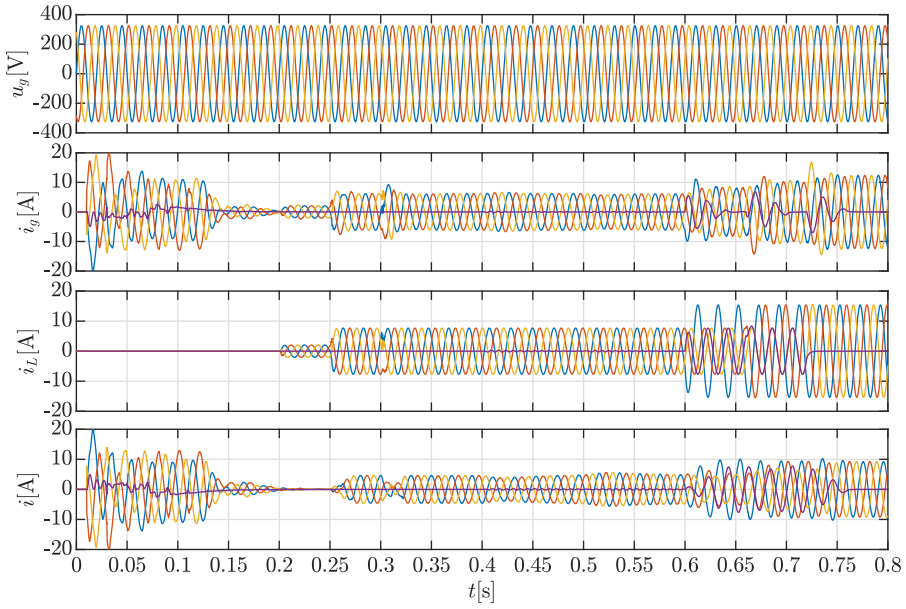

Figure 4.13: Global simulation results. Variables are shown in phase coordinates (abcn): blue, phase A; red, phase B; orange, phase C; purple, phase N. 1) Grid voltage, 2) Grid current, 3) Load current, 4) Converter current.

4.7.1 Reactive power management and frequency shifts

The initial test consists in managing the reactive power which is injected/consumed into/from the grid by following the reference profile which was previously defined. The results are shown in Fig. 4.14 and Fig. 4.15.

As can be seen, the DC link voltage reaches its nominal value at 0.2 s, which is maintained almost constant under changes in the load current. The converter properly deals with the connection of a three-phase load by controlling the reactive power required by the load, so that the main grid only needs to manage the load active power in steady-state conditions. During transient operation under load power changes, the previous statement is not totally fulfilled. The grid provides some reactive power during 2 fundamental periods (40 ms) after the load power change. Note that the DRC implemented in the current control loop of the iPEBBs has a learning period of a fundamental period. The system operator provides information to the central controller of the power converter with an estimation of the load reactive power. Because of the load power change bandwidth (100 Hz) and the system operator estimation bandwidth, grid provides a significant amount of reactive power during the first learning period. At the end of this period, the power converter has relevant information about the load reactive power. Thus, during the second learning period, the power converter compensates most of the reactive power. At this moment, the estimation of the load reactive power

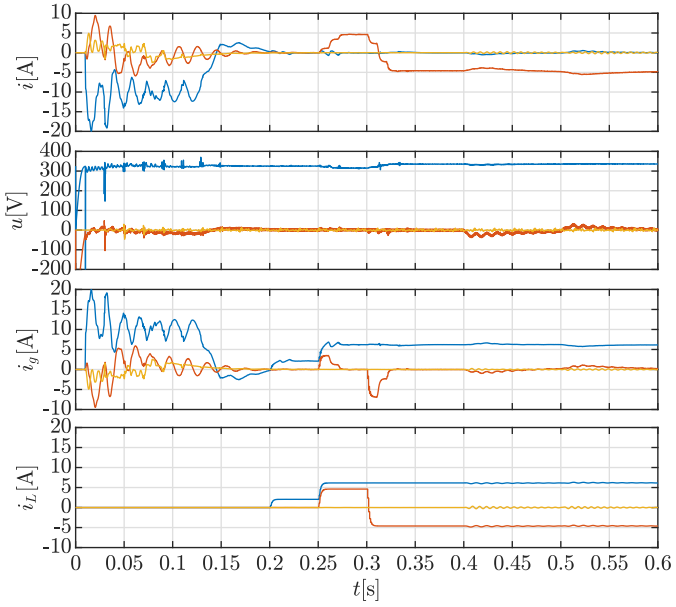

Figure 4.14: Simulation results for reactive power management. Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. 1) Converter current; 2) Control action of current controller; 3) Grid current. 4) Load current.

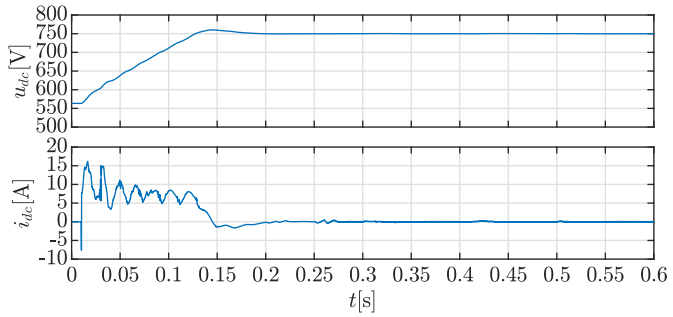

Figure 4.15: Simulation results for reactive power management. 1) Converter DC link voltage; 2) Converter DC link current.

is already precise, so that at the end of this period, the power converter compensates all the reactive power and the grid only provides active power.

In addition, the grid frequency changes are properly compensated in about 3 fundamental periods (60 ms). Note that, a huge step changes in the grid frequency are tested (50 Hz to 47.2 Hz and then back to 50 Hz) whereas the grid frequency variations are much slower in a real application. The selection of the simulation final frequency value is not arbitrary, since it gives (10000/47.2) an integer delay of 211 samples and a

fractional delay of 0.8644. This way, the fractional delay is quite high and its compensation is also tested. The THD at the beginning of the first frequency change (50 Hz to 47.2 Hz) is 0.3724% for the converter current and 0.1025% for the grid current, which is reduced to 0.0373% and 0.0120% respectively after three fundamental periods. The THD at the beginning of the second frequency change (47.2 Hz to 50 Hz) is 0.1861% for the converter current and 0.0921% for the grid current, which is reduced to 0.0168% and 0.0086% respectively after three fundamental periods.

4.7.2 Connection of local linear loads

Disturbance rejection capabilities are demonstrated with a set of single-phase linear loads which are connected to the grid at different times. With the proposed control scheme, both negative sequence and homopolar currents are supplied by the converter, making the grid isolated from the disturbances in steady state, only supplying balanced currents.

The results of this test are shown in Fig. 4.16. As can be seen, the behavior is similar to the one shown in Section 4.7.1. The converter starts receiving the information with the current references needed to compensate unbalances during the first fundamental period. During the second fundamental period, precise information of the unbalanced current references is already available, so that unbalance compensation keeps improving. This way, at the start of the third fundamental period, unbalances are totally compensated. Therefore, unbalances are compensated by the converter in 2 fundamental periods (40 ms) by injecting negative sequence and homopolar current into the local grid. The main grid only supplies the needed balanced power.

The THD of the grid current at the connection of the first load is 2.3090%, which is reduced to 0.1178% after three fundamental periods; at the connection of the second load is 2.3914%, which is reduced to 0.0711%; and at the connection of the third load is 1.6190%, which is reduced to 0.0002%.

4.7.3 Connection of local non-linear loads

In order to see the disturbance rejection against non-fundamental harmonics, a set of non-linear loads is now connected instead of the linear loads of Section 4.7.2. The non-linear loads absorb a power equivalent to the linear loads (same RMS current) but the current shape is now almost square (full-wave rectifier connected to an inductive load). Odd harmonics up to the 13^{th} order are considered for this analysis.

The results of this test are shown in Fig. 4.17. Similar performance when compared to the linear load case is obtained. In this case, the harmonics produced by the load are absorbed in steady state by the power converter together with the load unbalances, having a transient response that lasts 2 fundamental periods (40 ms).

The THD of the grid current at the connection of the first load is 3.4034%, which is reduced to 0.1037% after three fundamental periods; at the connection of the second

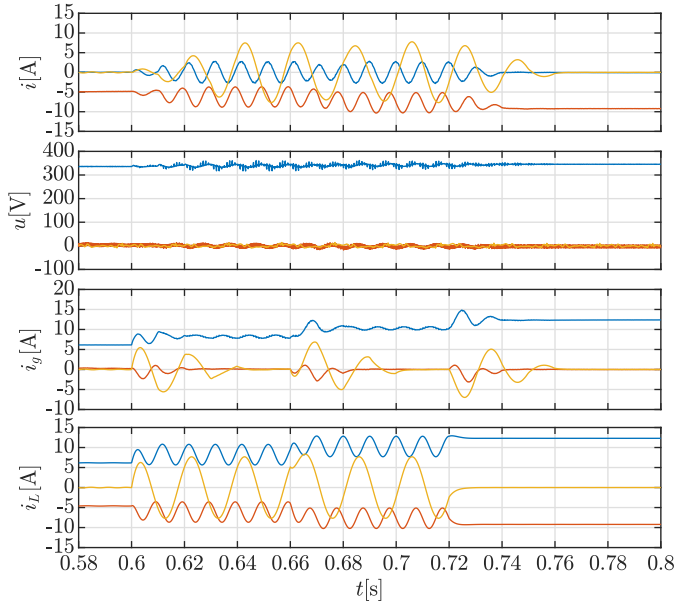

Figure 4.16: Simulation results for local linear load connection. Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. 1) Converter current; 2) Control action of current controller; 3) Grid current; 4) Load current.

load is 2.7024%, which is reduced to 0.0584%; and at the connection of the third load is 1.9339%, which is reduced to 0.0035%.

4.7.4 Effect of reference reconstruction and differentiability correction

As stated in Section 4.5, a reference differentiability correction is performed by the central controller in order to help the iPEBBs to improve the process of reference extrapolation. A comparison between the original case without reference extrapolation and differentiability correction, and the corrected one is shown in Fig. 4.18.

As can be seen, the results are similar for both cases, but the reconstructed and corrected reference case has less harmonic distortion. This is due to the reference extrapolation process, which makes the shape of the reference for the iPEBB current control loop smoother, in addition to an improved differentiability of the reference, which allows a better reference extrapolation.

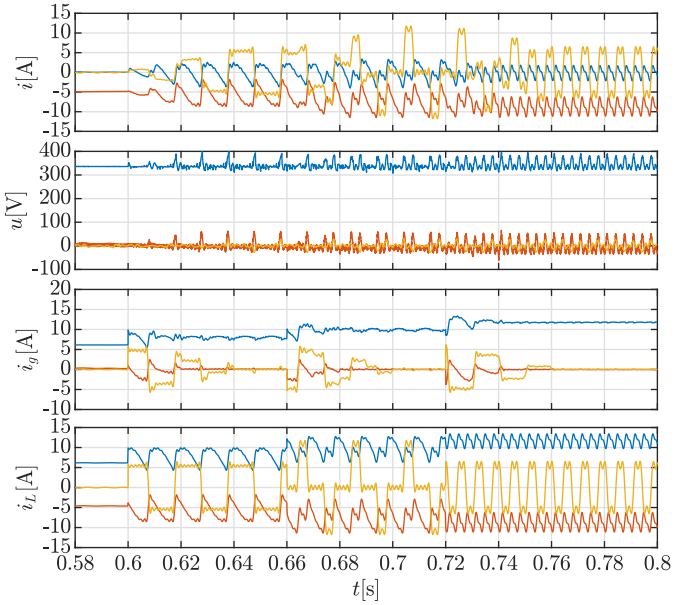

Figure 4.17: Simulation results for local non-linear load connection. Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. 1) Converter current; 2) Control action of current controller; 3) Grid current; 4) Load current.

4.7.5 Error from communication delays

As stated in Section 4.5.1, communication delays can affect the error of the resultant current since the output current reference is affected by the delay in the communication channel. Several cases are analyzed in order to detail the effect of this phenomenon.

In Case 1, both the central and the single-phase controllers work at the maximum frequency (10 kHz) without any delays (ideal case). This case is used as reference. In Case 2, the central and the single-phase controllers work at the nominal frequency (1 kHz and 10 kHz) without any delays (perfect real case). In Case 3, the central and the single-phase controllers work at the nominal frequency with the same random communication delay for all the single-phase controllers (quasi-random real case), using a normal distribution with a mean value of 0 (no delay) and a variance of 2% of the nominal communication period. In Case 4, the central and the single-phase controllers work at the nominal frequency with different random communication delay for each single-phase controller (random real case), using the same distribution as in Case 3.

To determine the effect of communication delays, a cumulative trapezoidal integration of the absolute value of the error is performed. This way, the area between the actual value and the reference value is calculated, so that the deviation from the reference value is obtained. Results from Case 1 are used as the reference value for the rest of the cases.

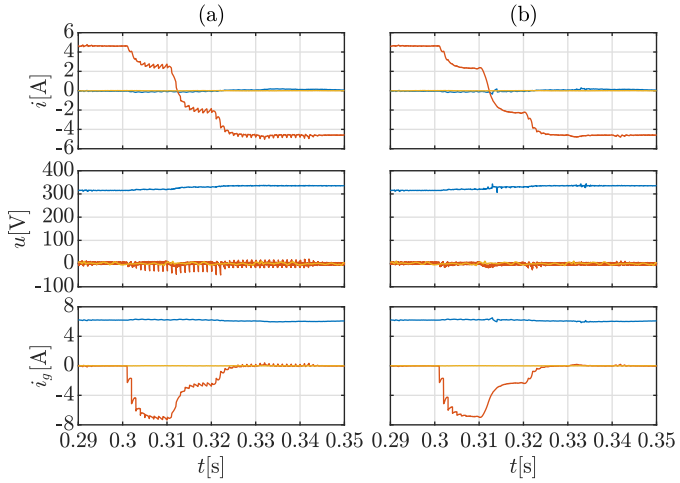

Figure 4.18: Simulation results to address the effect of the reference reconstruction and differentiability correction. (a) Initial case without reference reconstruction and differentiability correction, (b) reconstructed and corrected reference case. Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. 1) Converter current; 2) Control action of current controller; 3) Grid current.

Applying the described cases to the first reactive current reference change, the results of Table 4.2 are obtained. As can be seen, the error results get worse if communication delays are considered. Nevertheless, the reference reconstruction implementation reduces the effect of delays into the system, regardless of the analyzed case.

Table 4.2: Cumulative error [A.ms] results from communication delays. Case 1 is used as a reference for the rest of the cases. a) Without reference reconstruction; b) With reference reconstruction.

	CASE2		CASE3		CASE4	
TIME [s]	A)	B)	A)	B)	A)	B)
$0.30 \div 0.35$	613.0	605.6	624.9	619.2	624.3	618.0
$0.30 \div 0.31$	130.7	128.3	134.4	132.8	133.8	132.1
$0.31 \div 0.32$	168.0	164.3	174.6	171.6	174.4	171.1
$0.32 \div 0.33$	110.3	108.9	112.0	110.7	112.2	110.7
$0.33 \div 0.34$	101.7	101.7	101.6	101.7	101.7	101.7
$0.34 \div 0.35$	102.3	102.4	102.2	102.3	102.2	102.3

4.8 Experimental results

The modular power converter proposed during this chapter is also tested experimentally. For that purpose, the experimental setup shown in Fig. 4.19 is used. The

experimental tests analyze three features of the modular converter: reactive power compensation, non-fundamental harmonics mitigation and negative sequence correction.

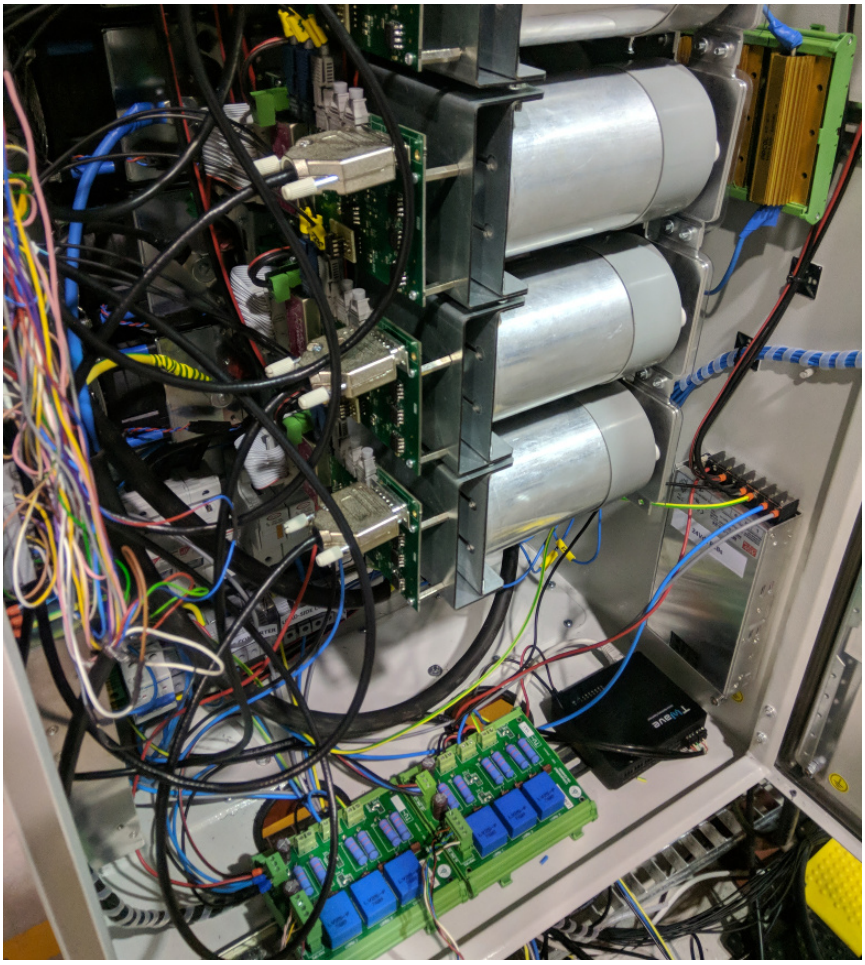

Figure 4.19: Experimental setup of a modular converter with a central controller and intelligent single-phase power cells.

The results of two reactive power compensation tests are shown in Fig. 4.20, Fig. 4.21, Fig. 4.22 and Fig. 4.23. In the first test, the reactive current is changed at 0.2 s from −10 A to +10 A, whereas, in the second test, it is changed from +10 A to −10 A. As can be seen, the dynamic response is quite good and there is not error at steady state.

Non-fundamental harmonics mitigation and negative sequence correction are shown in Fig. 4.24, Fig. 4.25, Fig. 4.26 and Fig. 4.27. As can be seen, the converter is able to

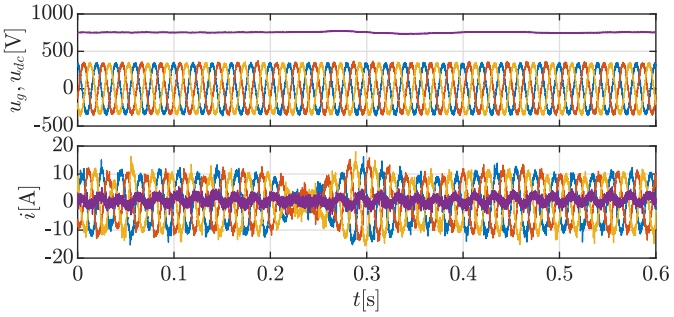

Figure 4.20: Experimental results for reactive power compensation (Test 1). Variables are shown in phase coordinates (abcn): blue, phase A; red, phase B; orange, phase C. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

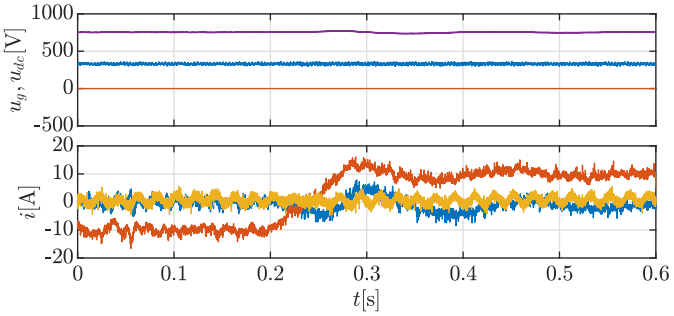

Figure 4.21: Experimental results for reactive power compensation (Test 1). Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

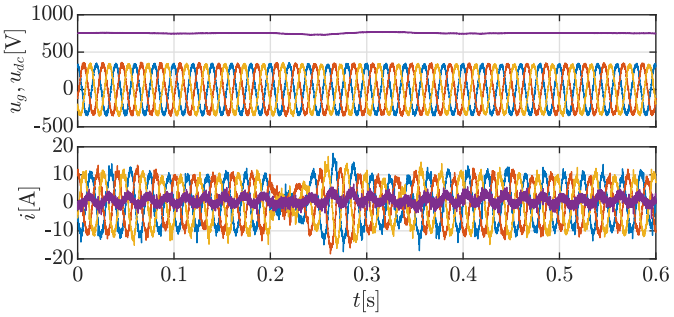

Figure 4.22: Experimental results for reactive power compensation (Test 2). Variables are shown in phase coordinates (abcn): blue, phase A; red, phase B; orange, phase C. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

inject current with non-fundamental harmonics and negative sequence to compensate the effect of non-linear/unbalanced loads connected to the grid.

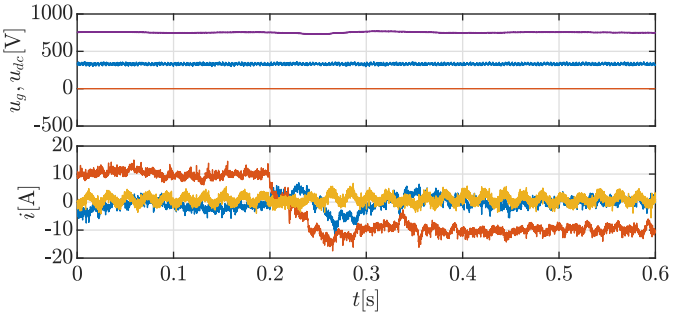

Figure 4.23: Experimental results for reactive power compensation (Test 2). Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

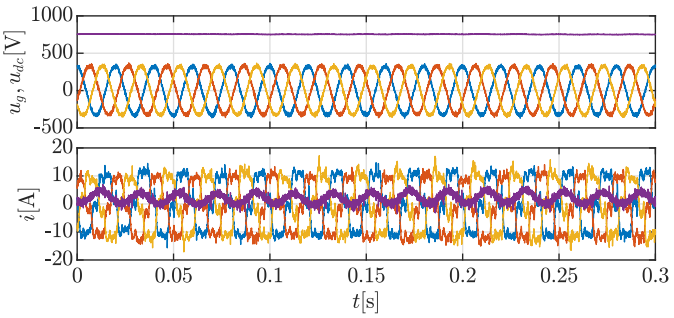

Figure 4.24: Experimental results for harmonics mitigation. Variables are shown in phase coordinates (abcn): blue, phase A; red, phase B; orange, phase C. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

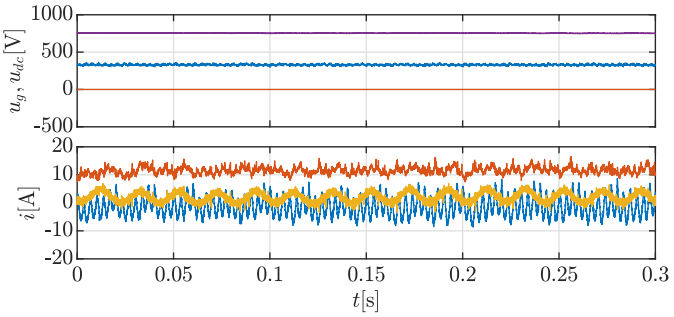

Figure 4.25: Experimental results for harmonics mitigation. Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

Finally, a THD comparative is done between the implemented modular single-phase control and a three-phase control in dq axis, which was previously implemented in the

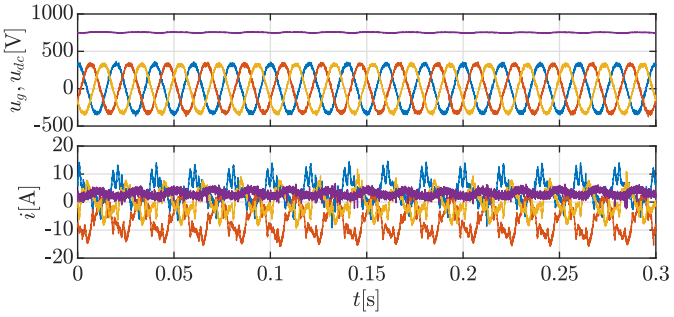

Figure 4.26: Experimental results for negative sequence mitigation. Variables are shown in phase coordinates (abcn): blue, phase A; red, phase B; orange, phase C. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

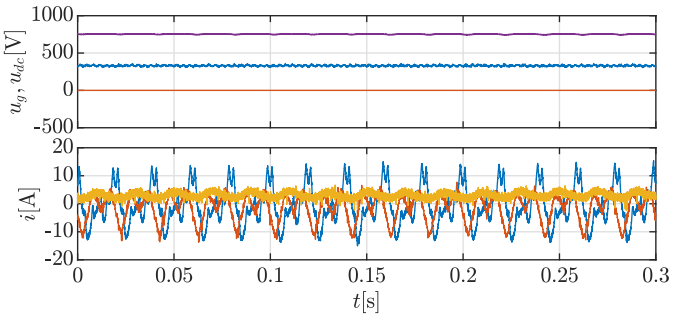

Figure 4.27: Experimental results for negative sequence mitigation.Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

experimental setup. The THD for the modular control is 5.02%, improving the THD for the three-phase which is 6.71%.

4.9 Conclusions

This chapter has presented a distributed control alternative based on DRC which can be applied to modular power converters. The proposed alternative was tested via simulations and experimentally, obtaining proper results in terms of steady-state error and transient behavior. Communication delays, frequency shifts and harmonic compensation are analyzed, and a reference extrapolator is proposed for mitigating its effects. Simulation and experimental results confirm the viability of the approach.

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Chapter 5

Distributed control deployment in a digital platform based on a μP under RTOS

5.1 Introduction

In Chapter 4, the analysis and development of a modular distributed digital control system platform, consisting of an arbitrary number of distributed controllers in charge of the operation of the iPEBBs and a central controller in charge of coordinating the operation of the converter from a global perspective, has been carried out. This platform has made it possible to realize the total control of the modular power converter to ensure the correct operation of the converter for its integration in various applications.

Nevertheless, the development of a distributed control system capable of managing a modular power converter based on iPEBBs requires the implementation of a central controller with sufficient computational power to perform those control tasks necessary to coordinate the operation of the distributed controllers for the different iPEBBs. While there are microcontrollers with sufficient performance for the implementation of the central controller to execute purely control tasks, they are more limited for the introduction of high-level programs for monitoring, supervision or data acquisition, or any HMI in general.

At this point, it is possible to use general-purpose microprocessors for the execution of high-level tasks, since they have a large support of libraries, packages and applications. This allows the development of high-level programs in a simpler and more flexible

way, or even the integration of software developed by third parties. In addition, the computational power and available memory (RAM and permanent storage) is usually high in a microprocessor to enable the execution of programs with high computational burden such as those requiring graphics processing.

Typically, microprocessor resource management is performed by an OS, which facilitates the execution of multiple tasks in parallel without user intervention through a scheduler, as well as organized access to hardware peripherals by different applications to avoid unwanted simultaneous use. This further expands the possibilities for high-level application integration, since the user does not have to deal with low-level programming for hardware management and the focus is only on the algorithm of the task to be performed.

That said, the fact that a scheduler is in charge of managing the CPU allocation when executing tasks implies delays that can be considered negligible for running auxiliary tasks but not for the execution of critical tasks that have to meet strict deadlines. While it is possible to set different priorities for the various tasks so that the OS scheduler prioritizes some tasks over others, deterministic operation cannot be guaranteed. This implies that, by default, standard OSes are not suitable for executing control tasks with RT constraints.

One option to overcome this problem is the use of OSes specifically designed for RT task execution, also known as RT OSes, which guarantee deterministic behavior to enable the execution of tasks with firm RT constraints. However, these OSes do not have the high support of standard OSes and are usually developed for integration on a specific set of microprocessors that are of interest to the RT OS developer.

Another option for the execution of RT tasks is the integration of a RT extension within a standard OS. In this way, the execution of tasks with firm RT constraints is enabled, while maintaining all the features of a highly supported OS. However, the resulting OS after the integration of the RT extension must be validated on the hardware platform where it is implemented, in order to ensure adequate behavior for the execution of RT tasks. Due to the versatility it provides, the standard OS option with RT extension is the one selected for the implementation of the digital central controller.

This chapter describes the hardware platform chosen for the implementation of the central controller and then describes the selected standard OS and the RT extension integrated in it. To validate its correct operation, a series of tests are performed on the resulting platform to determine the performance when executing tasks with firm RT constraints.

For this purpose, a program that executes a periodic task specifically designed to evaluate the existing delays after each iteration is implemented within the platform. This program is executed in two different operation modes, one managed by the RT extension and suitable for the execution of critical tasks, and the other managed by the standard OS and suitable for the execution of auxiliary tasks. The results of both cases are analyzed and compared with each other to demonstrate the suitability of the

RT extension for the execution of critical control tasks.

In addition, the architecture of the developed software is presented, in order to enable the integration of the central controller within the digital platform in a structured way, according to the requirements and characteristics of the different control tasks.

The work carried out in this chapter is derived from the development and subsequent intellectual property registration of the software known as "DECiSivE - Development of Energy Control SystEms", which is being exploited at the enterprise level through a software license agreement with the company Enfasys Ingeniería S.L, and hence based on contribution "Distributed Control Deployment in a Digital Platform based on a μP under RTOS [IPR1, SLA1]" shown in Chapter 1.

The analysis of the proposed control system starts from the power system used in Chapter 6, which consists of a multiport converter integrating a HESS,a bidirectional local load, and connected to the power grid, as shown in Fig. 5.1.

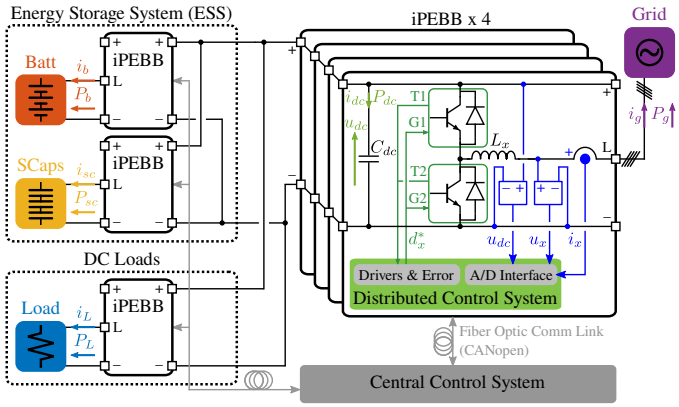

Figure 5.1: Electrical diagram of the multiport DC/DC/AC converter based on the use of Intelligent PEBBs (iPEBBs).

The proposed control system focuses on active power sharing and therefore consists of a central controller in charge of power sharing and DC-link voltage control, providing active power references to the distributed controllers of each iPEBB, which return DC-link voltage measurements. The block diagram of this control system is shown in Fig 5.2.

Starting from this proposed control system, a selection of the digital platform based on a general-purpose μP is carried out to provide extended capabilities to the control system.

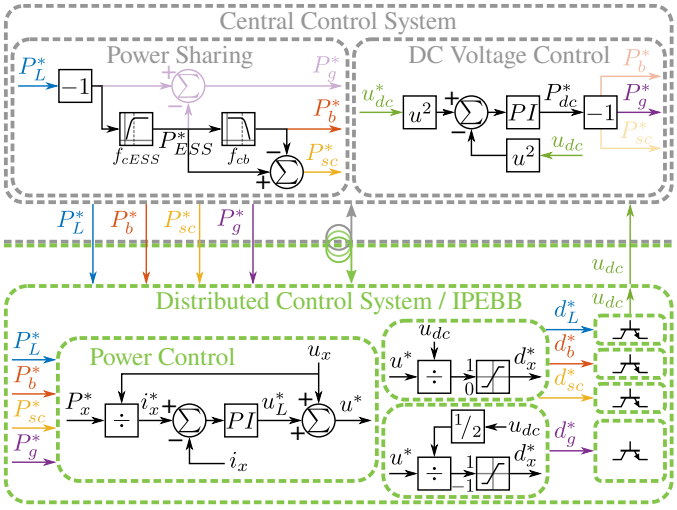

Figure 5.2: Distributed control.

5.2 Selection of the hardware and low-level software

In this section, the selection of those elements that are part of the digital control platform is carried out, in order to obtain a suitable solution for the implementation of the central controller in distributed control systems. First, the selection of the hardware device of the digital platform is carried out, in order to establish the basis for the integration of all the necessary software. Then, the selection of the most suitable OS together with the RT extension is carried out, in order to make the digital platform ready for the implementation of the central controller. Finally, the selected configuration for the digital platform is shown, in order to optimize the execution of RT tasks.

5.2.1 Hardware equipment

The main objective in the selection of hardware equipment is to maximize the performance and features of the digital platform and to have a great support to facilitate future upgrades and expansions, all while maintaining a reasonable cost.

The Raspberry Pi (RPi) is a device that meets these characteristics, as it has a moderately powerful CPU for the execution of computationally intensive tasks, a dedicated GPU for the development of GUI applications, and a reasonably large RAM and FLASH memory size to facilitate the execution of multiple tasks and the persistent storage of historical data generated by the applications.

In addition, it has integrated various hardware peripherals (e.g., HDMI, Ethernet, USB, UART, SPI, I^2C, PWM, clock generators) that provide connectivity with other

devices, a key feature for integrating the digital platform into a distributed control system. It is also worth mentioning the great support offered for this device, since it is being used in a large number of diverse applications.

Last but not least, RPi is marketed in a form factor suitable for embedded systems, known as Compute Module, which facilitates its integration in industrial applications. Moreover, this industrial form factor provides access to a larger number of pins compared to the traditional form factor, allowing the use of a larger number of hardware peripherals. All this at a cost of a few tens of euros.

For all the reasons stated above, the RPi will be used as the central element of the digital platform to be developed. The specific model selected will be the Compute Module 3+ (CM3+), based on the Raspberry Pi 3 Model B+, as it is sufficiently tested (released in January 2019), with long-term support (manufacturing until January 2026) and whose software is easily adaptable to the next model of the manufacturer (Compute Module 4).

While it is true that the RPi provides a number of peripherals that make it suitable for interfacing other devices, it is lacking in terms of connectivity with power systems, as it has no analog inputs and a reduced number of PWM outputs. To compensate for this problem, the DSP model TMS320F28335 manufactured by Texas Instruments will be included in the control platform. The interconnection between both control devices is done through a fast communications channel, so that the final implementation of the control is not affected. In this particular case, the SPI bus is used due to its full-duplex operation and high throughput.

5.2.2 Operating System

The number of OSes available for installation on the RPi is high, due to the great support provided to the device. There are general purpose OSes such as Raspberry Pi OS (formerly known as Raspbian), with official support from the manufacturer, and Ubuntu Desktop; OSes for multimedia applications such as LibreElec and OSMC; IoT OSes such as Ubuntu Core and Windows IoT Core; and even OSes for retrogaming such as RetroPie and Lakka.

However, the implementation of the digital platform requires an OS that meets a number of characteristics: suitable for embedded systems, lightweight and customizable, and with a framework that facilitates the development of UI applications. Therefore, an embedded Linux OS generated from the Qt for Device Creation product (formerly known as Boot2Qt), integrated in the Qt toolkit, is chosen. The Qt development framework is cross-platform and widely used in applications for embedded systems. This facilitates the development of monitoring, visualization, data storage and UI applications for the digital platform under development.

For the particular case of the CM3+ in the digital platform, an embedded Linux image based on Qt 5 is chosen, which is configured to have only those packages that are essential for proper operation.

However, even if a lightweight Linux distribution specially designed for embedded systems is being used, the system is not expressly prepared to guarantee adequate RT operation. As discussed in Section 2.4, the study of different schedulers could be considered in order to prioritize those tasks requiring RT behavior [5.1–5.12]. In any case, the final performance of the system would depend on the final design of the OS. Therefore, the solution adopted for the development of the digital platform consists in integrating into the OS a specific RT extension to enable the execution of tasks with firm RT constraints.

5.2.3 Real-Time extension

As discussed in Section 2.4.2, there are several options to enable a RT behavior into a Linux OS such as the one implemented in the digital platform.

RT_PREEMPT patch [5.13–5.15] enables a more aggressive preemption to minimize response time for RT tasks. In this way, the scheduler would have the ability to allocate hardware resources more aggressively to tasks with higher priority at the expense of those tasks with lower priority, in order to minimize delays in the most critical tasks. However, the performance of the system would still depend on the design of the OS, since the execution environment of both RT and non-RT tasks remains the same, and the hardware allocation mechanisms are common for both cases.

RTAI extension [5.15–5.19] is based on the introduction of a microkernel working in parallel to the standard Linux kernel following a dual kernel approach based on the HAL concept. The microkernel has direct access to the hardware and can catch IRQs without intervention from the Linux kernel. Therefore, the microkernel introduces a new execution environment into the OS isolated from the standard one. In this way, if the execution of RT tasks is redirected to the microkernel and hence to the new execution environment, RT and non-RT processes are executed separately. In addition, the lightweight implementation of the microkernel results in faster operation when allocating hardware resources to the various processes. By prioritizing the operation of the microkernel over the Linux kernel, the execution of critical (RT) tasks can be performed in the microkernel to improve response time, thus guaranteeing deterministic operation and firm RT behavior.

However, RTAI extension has a major disadvantage: it only allows executing RT tasks in kernel space, unlike RT_PREEMPT patch that allows executing them in user space. This hinders the development of RT applications, since most of the resources for application development are intended for user space, which is not accessible from kernel space. Xenomai extension [5.14, 5.17, 5.20–5.26] seeks to solve this problem since, following a similar idea to the RTAI extension, it provides the tools to enable the execution of RT applications in user space in C programming language. In fact, its development is still in progress with the aim of standardizing as much as possible the API at both user and system level to be POSIX-compliant. This facilitates the porting of libraries and resources developed for another digital platform, allowing their use in RT tasks running in the Xenomai environment.

Because of this, the RT extension known as Xenomai will be integrated to ensure adequate performance for those tasks that require at least firm RT conditions. The main concept of Xenomai in version 3 is to integrate a dual-kernel system in which the standard Linux kernel and a new kernel (Cobalt kernel) designed to manage RT tasks coexist. In this way, all RT tasks will run in the Cobalt kernel and will operate completely independently of the standard Linux kernel, so that the scheduler design becomes irrelevant in determining RT performance. In turn, all non-critical tasks and services can continue to run on the standard Linux kernel without having to be redesigned and without affecting the operation of the most critical tasks.

The dual kernel implementation requires the interception of interrupts, system calls and system events in order to decide whether they should be serviced by the RT kernel or the standard kernel. For this purpose, an interruption management mechanism based on Adeos and known as interrupt pipeline (I-pipe) will be integrated. Broadly speaking, I-pipe consists of a series of modifications made to the Linux kernel in order to add a higher layer of control that can intercept all interrupts before they reach the Linux kernel. Interrupts will be redirected to first be handled by the Cobalt kernel and then by the standard Linux kernel. In this way, the design of the Linux kernel would not affect the management of interrupts by the Cobalt kernel, guaranteeing a deterministic operation of the system when executing RT tasks.

However, although the behavior of the system becomes deterministic, the entire interrupt management mechanism involves a series of delays that must be taken into account for the correct operation of the system. In order to check the validity of this architecture, some tests will be carried out to analyze the delays produced when executing a periodic RT task.

5.2.4 Final implementation and software configuration

The flash memory of the CM3+ is programmed with an image based on Boot2Qt 5.14 with the version 4.19 of the Linux kernel for RPi. Version 3.1 of Xenomai with an I-pipe patch for ARM is applied into the image in order to integrate the RT extension in the final system. Kernel build configuration is tweaked in order to adapt kernel behavior to mitigate latencies and hence optimize RT operation:

- CPU frequency scaling (option: CPU Power Management/CPU Frequency scaling/CPU Frequency scaling) is disabled to remove latencies because of CPU frequency variations to save power.
- Memory compaction (option: Memory Management options/Allow for memory compaction) and contiguous memory allocation (option: Memory Management options/Contiguous Memory Allocator) are disabled to avoid page migration which can produce extra latencies.
- Kernel debugger (option: Kernel Hacking/KGDB: kernel debugger) is disabled since it is not compatible with I-pipe/Xenomai integration.

- Optionally, to maximize standard kernel time response, kernel is configured in low-latency mode (option: General setup/Preemption Model (Preemptible Kernel (Low-Latency Desktop)) and timer frequency is increased to 1000 Hz (option: Kernel Features/Timer frequency (1000 Hz)).

CM3+ has a 4-core CPU so, taking advantage of this feature and in order to determine the effect of the standard Linux kernel scheduler in high-priority tasks when executing non-critical background processes, CPU0 and CPU1 are isolated from the scheduler (isolcpus kernel parameter) to not be used during its operation. This way, only CPU2 and CPU3 are automatically managed by the scheduler when executing background processes.

5.3 Validation of the RT operation

The integration of the Xenomai RT extension within the OS would enable the execution of high-priority tasks with firm RT constraints. However, this statement has to be conveniently tested to confirm a correct performance of RT task execution on the proposed digital platform, in order to avoid undesired events when running any control algorithms that require responsive and deterministic behavior.

Therefore, in this section, a series of tests will be carried out to check the latency when executing high-priority tasks on the different CPUs, either managed by the standard Linux kernel (known as secondary mode in Xenomai) or by the Cobalt kernel (known as primary mode). For this purpose, a timed task tweaked for the computation of latency that computes a high-frequency algorithm with the highest possible priority is executed. Some timing variables are defined and analyzed to characterize the latency of the different tests and determine the performance of the whole system under different configurations, as shown in Fig. 5.3:

- Delay time: Difference between the theoretical programmed starting time of the timed task and the real starting time. It shows the reaction time of the system when the execution of a new task is triggered (asynchronous performance). In ideal conditions, its value is zero.
- Elapsed time: Difference between two consecutive iterations of the timed task. It shows the reliability of the system when executing periodic tasks with a fixed period (synchronous performance). In ideal conditions, its value is equal to the configured task period (T).
- Execution time: Time lasted during the active execution of a iteration of the timed task. It shows the computational capability of the system (throughput).

To ensure the validity of the results obtained from the tests, the source code in charge of computing the latency in the application running on the digital platform is

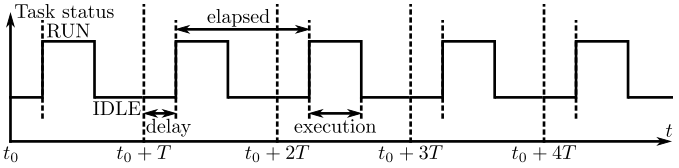

Figure 5.3: Time evolution of a timed task starting at time t_0 with a configured period of T. Some timing variables are included, such as elapsed, delay and execution time.

based on the source code of the application "latency" provided by the Xenomai API, with small tweaks to gather more information from the system.

At this point, it should be noted that, although the microkernel implementation is optimized to minimize delays, they cannot be completely eliminated. To mitigate this problem in the execution of periodic tasks, the Xenomai extension includes an automatic latency compensator responsible for tweaking without user intervention the timer configuration to anticipate its next firing the time necessary to compensate for the delays inherent in the system.

The timer correction value is user configurable and is known within the Xenomai extension as the gravity value. Depending on the hardware where the Xenomai extension is deployed, the gravity value takes a conservative default value to avoid overcorrections. This value can be subsequently tweaked by the user to further improve the performance of the latency compensator. However, in order not to distort the latency results under primary mode operation (Xenomai) for comparison with the results under secondary mode operation (standard Linux), the gravity value is set to zero only for testing purposes.

Back to the specific details of the test, the periodic task is executed with a period of 100 µs (10 kHz) to test the performance of the system for a high-frequency algorithm. A timer is configured to trigger the task with the selected period. Therefore, the difference between the actual timestamp read from the system when initiating the task and the expected one configured in the timer is computed to characterize the delay time for each iteration. In addition, the elapsed time is calculated as the difference between the actual timestamp obtained in the current iteration with respect to the previous one.

The algorithm computes the complex FFT of a rotating vector in alpha-beta coordinates formed from a full period of three sinusoidal signals sampled at 10 kHz, with a fundamental frequency of 50 Hz, out of phase $2\pi/3$ radians and with harmonic content in the 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonics. All this in order to emulate the harmonic analysis of a three-phase electrical system. The computation of the FFT is carried out using the FFTW v3 library, to demonstrate the integration capability of libraries and resources available for C language applications in RT applications in Xenomai.

Each test consists in executing the high-priority task during 5 minutes in one specific CPU, and hence producing 3000000 samples. There are 8 test cases in total, 1 case

per CPU for both standard Linux and Cobalt kernel management. Latency results in time domain of both delay and jitter are shown in Figs. 5.4-5.7 for standard Linux management, and Figs. 5.8-5.11 for Cobalt kernel management. In addition, in order to appreciate with more detail the differences between all cases, the corresponding heat maps for latency distribution are shown in Figs. 5.12-5.20.

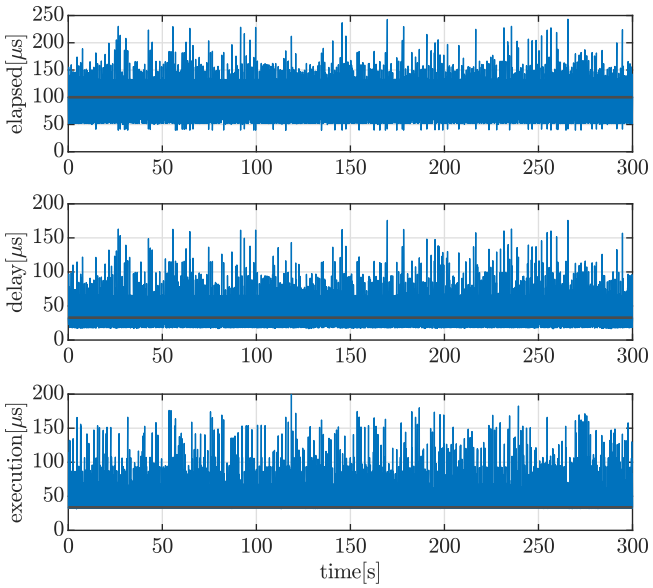

Figure 5.4: Latency results in time domain for a high-priority task with a period of 100 µs managed by standard Linux kernel in CPU0. Median of the data is shown with an horizontal black line.

The median value for the elapsed time of all cases is around 100 µs, which coincides with the period of the periodic task as would be expected. However, the deviations for the cases with standard Linux kernel management are much larger than the ones with Cobalt (Xenomai) kernel management.

Focusing on standard Linux kernel cases, CPU2 and CPU3 show the worst behavior because they occasionally reach a value of 1800 µs, 18 times more than the configured period, which is absolutely unacceptable for the execution of periodic tasks with firm RT constraints. This is due to the influence of the OS scheduler, which is responsible for managing the execution of background processes on these same two cores. Therefore, the scheduler occasionally ignores the timed task being executed, raising the elapsed time to an absurdly high value and provoking a high number of overruns.

CPU0 offers better results than previous cases but still fails to comply with firm RT constraints, since the elapsed time occasionally reaches values greater than 200 µs, 2 times the configured period. Although the result is not so catastrophic, it confirms the appearance of undesired overruns for the execution of periodic tasks.

CPU1 shows the best behavior of all cases, since its elapsed time is within a ±50%

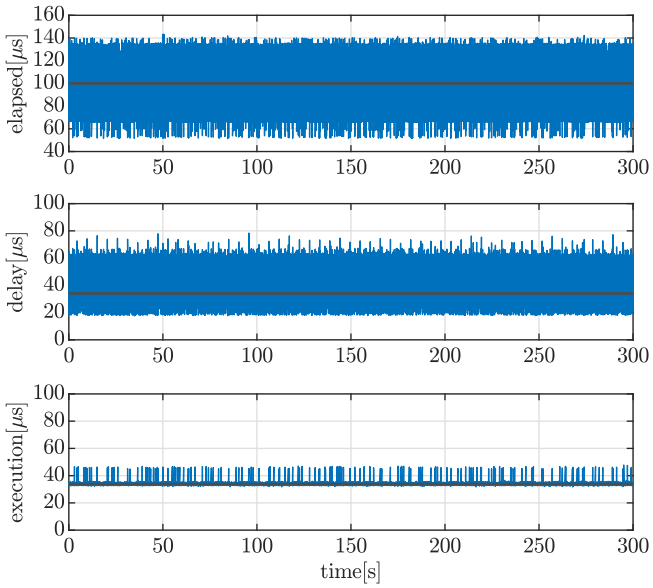

Figure 5.5: Latency results in time domain for a high-priority task with a period of 100 µs managed by standard Linux kernel in CPU1. Median of the data is shown with an horizontal black line.

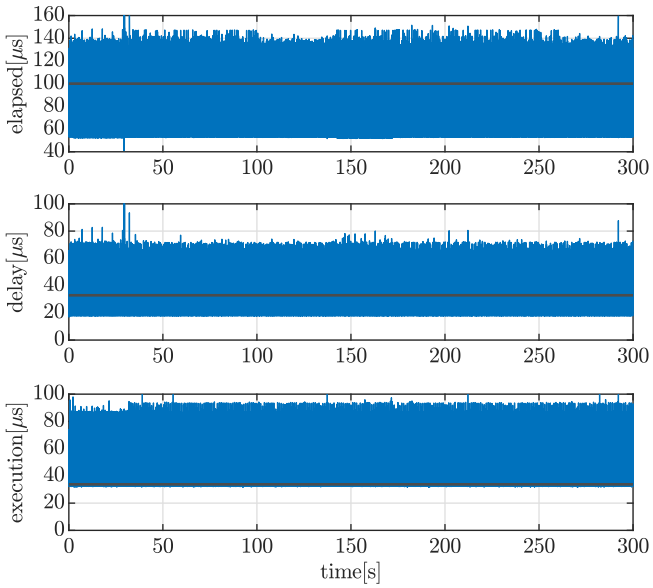

Figure 5.6: Latency results in time domain for a high-priority task with a period of 100 µs managed by standard Linux kernel in CPU2. Median of the data is shown with an horizontal black line.

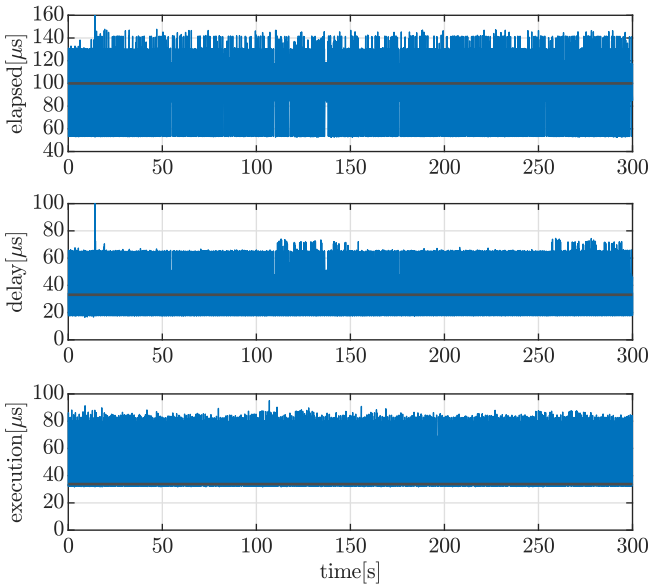

Figure 5.7: Latency results in time domain for a high-priority task with a period of 100 µs managed by standard Linux kernel in CPU3. Median of the data is shown with an horizontal black line.

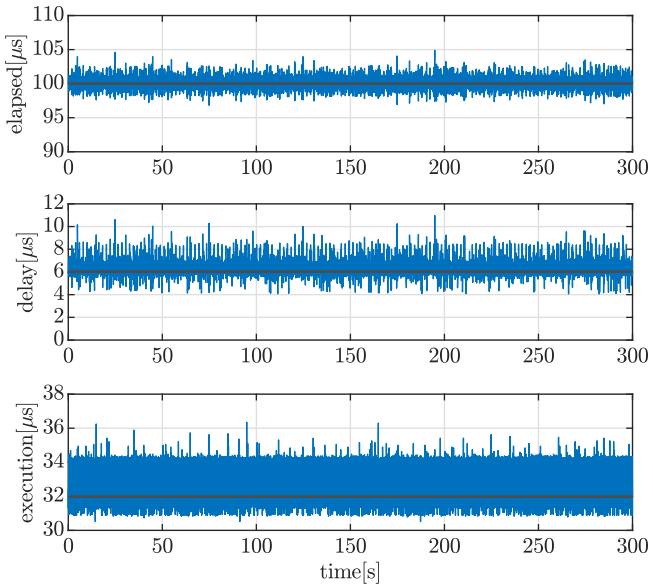

Figure 5.8: Latency results in time domain for a high-priority task with a period of 100 µs managed by Cobalt kernel in CPU0. Median of the data is shown with an horizontal black line.

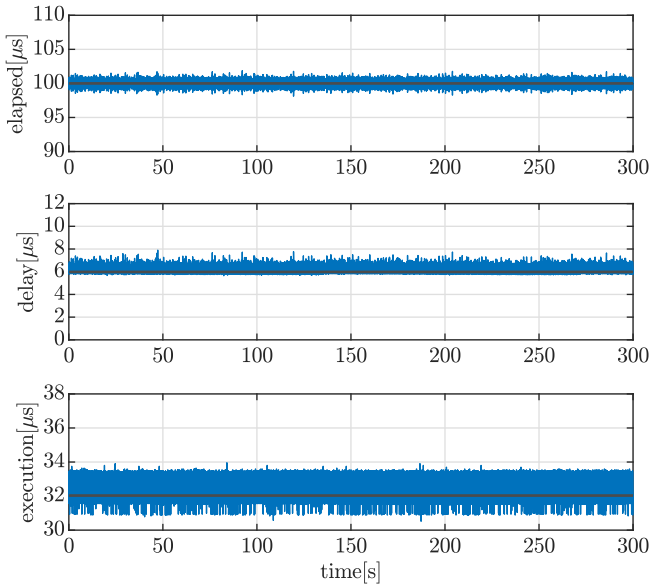

Figure 5.9: Latency results in time domain for a high-priority task with a period of 100 µs managed by Cobalt kernel in CPU1. Median of the data is shown with an horizontal black line.

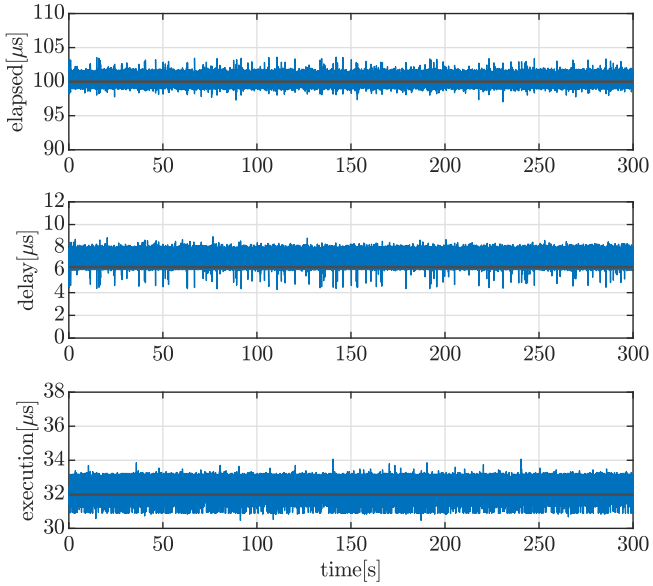

Figure 5.10: Latency results in time domain for a high-priority task with a period of 100 µs managed by Cobalt kernel in CPU2. Median of the data is shown with an horizontal black line.

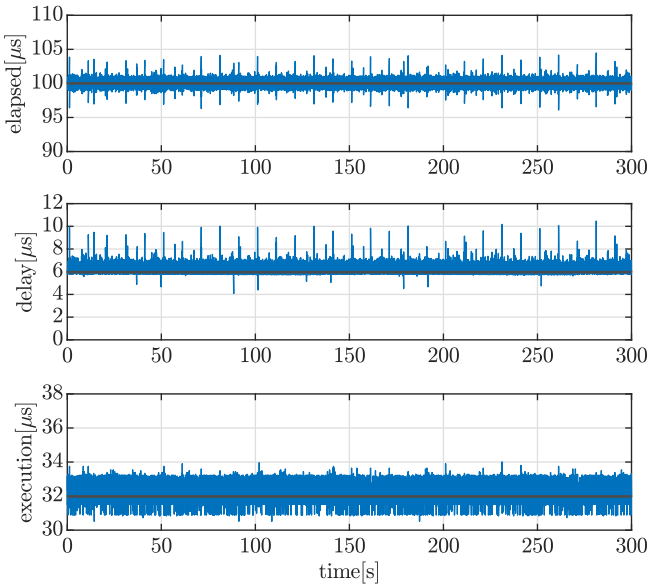

Figure 5.11: Latency results in time domain for a high-priority task with a period of 100 µs managed by Cobalt kernel in CPU3. Median of the data is shown with an horizontal black line.

range with respect to the configured period. The reason for CPU0 to show a worse performance than CPU1 is that, although the scheduler is not executed in either of the two cores, RPi handles all IRQs through CPU0. Servicing all these requests has a negative impact since it introduces latency and degrades performance on CPU0 when executing high-priority tasks.

In Cobalt kernel cases, the results obtained are much better than those seen for Linux kernel cases, showing variations from ±5% in CPU3 to ±2% in CPU1. The differences found for the various cases may be due to the operation of the scheduler for the standard Linux kernel on CPU1 and CPU2, and IRQs on CPU0, which slightly affect the behavior of the Cobalt kernel but with limited influence. Nevertheless, variations in all Cobalt kernel cases are much smaller than the configured period, guaranteeing a correct performance for executing periodic tasks with firm RT constraints in any of the CPUs.

The median value for the delay time is between 30 µs and 35 µs for standard Linux kernel cases and between 6 µs and 6.5 µs for Cobalt (Xenomai) kernel cases, showing a much better performance for asynchronous operation when using Xenomai RT extension.

The same pattern as for elapsed time is repeated for delay time, showing catastrophic results for CPU2 and CPU3 (maximum delay time around 1800 µs), inadequate results for CPU0 (maximum delay time around 200 µs) and alarming results for CPU1 (maximum delay time of 80 µs), referring to the standard Linux kernel management.

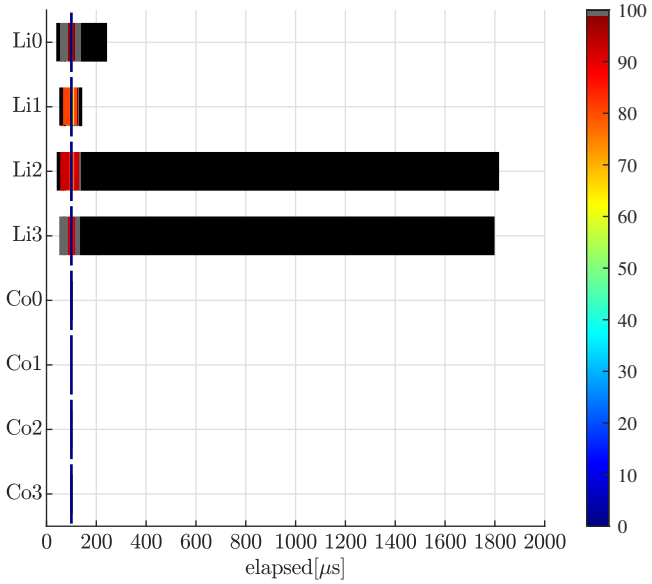

Figure 5.12: One-dimensional heat map of elapsed data distribution for all cases: LiX for standard Linux kernel management and CoX for Cobalt kernel management, where X represents the CPU number. Blue vertical line represents the median elapsed value for each case. Color map is defined depending on the cumulative percentage of data around the median elapsed value: grey color represents last 1% of data whereas black color represents last 0.1%

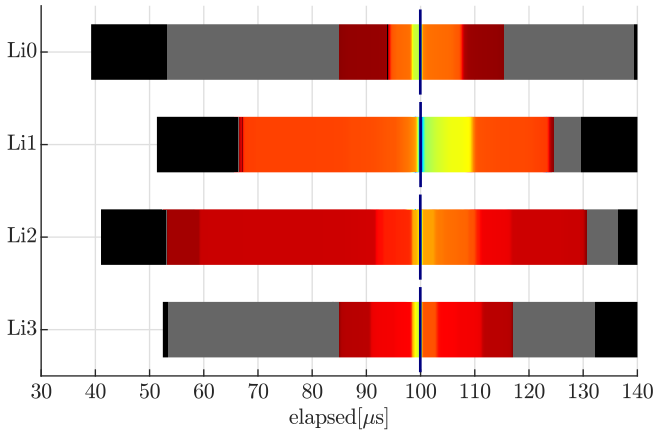

Figure 5.13: One-dimensional heat map of elapsed data distribution for standard Linux kernel cases (LiX, where X represents the CPU number). Blue vertical line represents the median elapsed value for each case. Color map is defined in Fig. 5.12.

For the Cobalt kernel management cases, much better results than those for standard Linux kernel management are observed, making them compatible with the execution

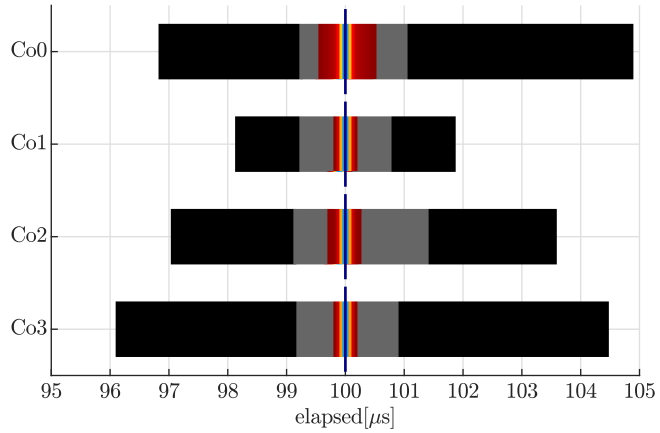

Figure 5.14: One-dimensional heat map of elapsed data distribution for Cobalt kernel cases (CoX, where X represents the CPU number). Blue vertical line represents the median elapsed value for each case. Color map is defined in Fig. 5.12.

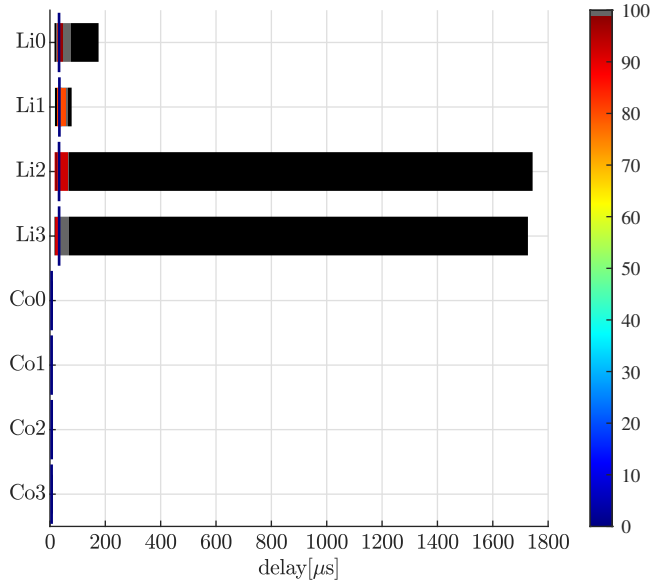

Figure 5.15: One-dimensional heat map of delay data distribution for all cases: LiX for standard Linux kernel management and CoX for Cobalt kernel management, where X represents the CPU number. Blue vertical line represents the median delay value for each case. Color map is defined depending on the cumulative percentage of data around the median delay value: grey color represents last 1% of data whereas black color represents last 0.1%

of asynchronous tasks with firm RT constraints. In particular, maximum delay time of 11 µs for CPU0, 10.5 µs for CPU3, 9 µs for CPU2 and 8 µs for CPU1 is observed.

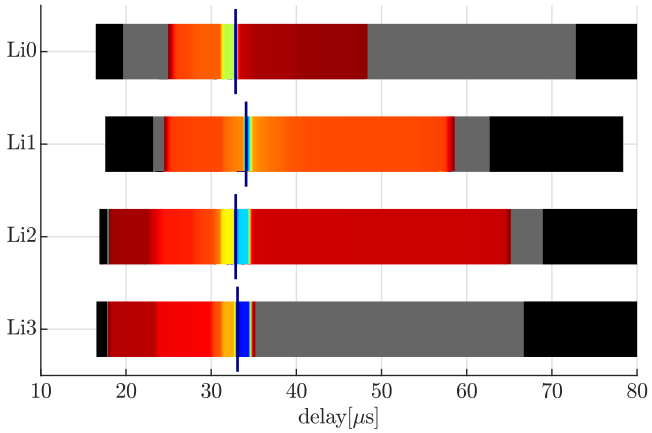

Figure 5.16: One-dimensional heat map of delay data distribution for standard Linux kernel cases (LiX, where X represents the CPU number). Blue vertical line represents the median delay value for each case. Color map is defined in Fig. 5.15.

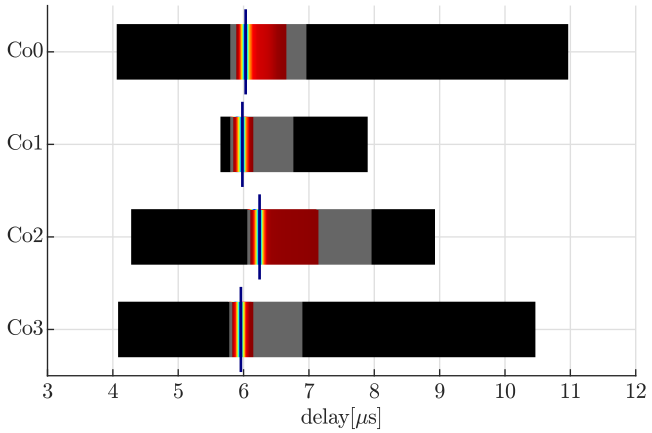

Figure 5.17: One-dimensional heat map of delay data distribution for Cobalt kernel cases (CoX, where X represents the CPU number). Blue vertical line represents the median delay value for each case. Color map is defined in Fig. 5.15.

The median value for the execution time is 34 µs for standard Linux kernel cases and 32 µs for Cobalt (Xenomai) kernel cases, showing a better performance for computational capability (throughput) when using Xenomai RT extension.

Focusing on standard Linux kernel management cases, CPU0 shows the worst results with a maximum execution time of 200 µs, followed by CPU2 with a maximum execution time of 140 µs, and CPU3 with a maximum execution time of 100 µs. Moreover, they often reach execution times of up to 65 µs, much higher than the median value (34 µs). In contrast, CPU1 shows a fairly consistent behavior in terms of execu-

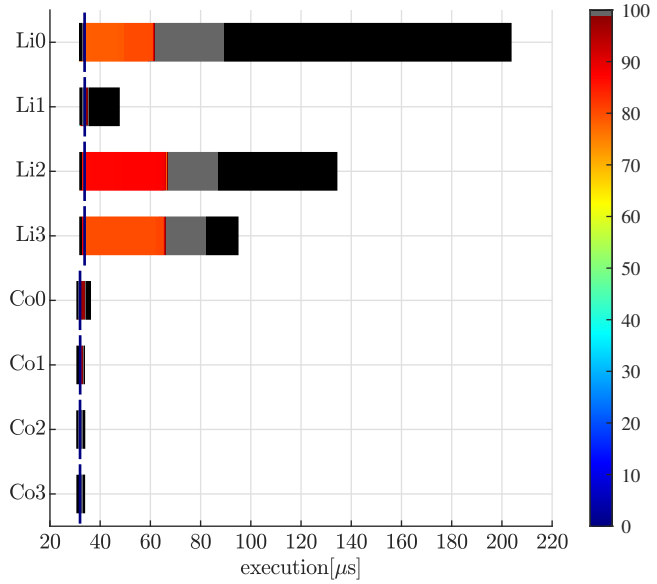

Figure 5.18: One-dimensional heat map of execution data distribution for all cases: LiX for standard Linux kernel management and CoX for Cobalt kernel management, where X represents the CPU number. Blue vertical line represents the median execution value for each case. Color map is defined depending on the cumulative percentage of data around the median execution value: grey color represents last 1% of data whereas black color represents last 0.1%

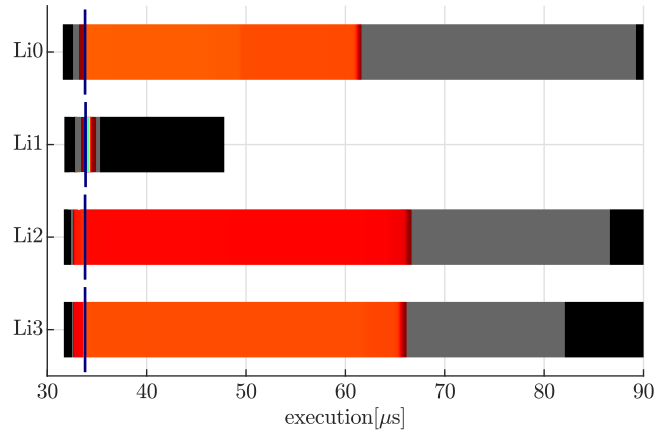

Figure 5.19: One-dimensional heat map of execution data distribution for standard Linux kernel cases (LiX, where X represents the CPU number). Blue vertical line represents the median execution value for each case. Color map is defined in Fig. 5.18.

tion time, with 99.9% of samples under 36 microseconds and a maximum time of 50 microseconds. Focusing on Cobalt kernel management cases, all CPUs show similar

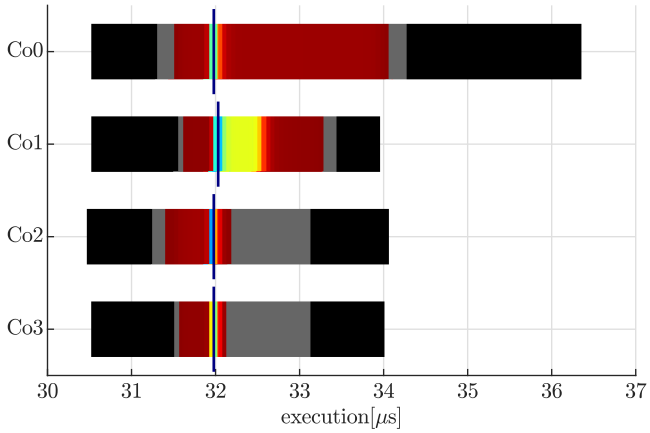

Figure 5.20: One-dimensional heat map of execution data distribution for Cobalt kernel cases (CoX, where X represents the CPU number). Blue vertical line represents the median execution value for each case. Color map is defined in Fig. 5.18.

results, with CPU0 showing the worst results with a maximum deviation of 4 µs and frequent deviations of up to 2 µs, followed by CPU1 with a maximum deviation of 2 µs and frequent deviations of up to 1 µs, and CPU2 and CPU3 with a maximum deviation of 2 µs and negligible frequent deviations.

To sum up, all the results obtained in this section indicate poor performance for the execution of RT tasks under the standard Linux kernel and demonstrate the correct performance of the Xenomai extension for the execution of RT periodic tasks with operating frequencies less than or equal to 100 kHz), which enables the digital platform for the implementation of the central controller in a distributed control system. All this, while maintaining all the features provided by an embedded Linux-based OS, allowing the integration of any type of applications necessary for the execution of auxiliary tasks in the control system. Timings when executing RT control tasks can be slightly improved by executing them on cores not handling IRQs and isolated from the OS scheduler management. However, regardless of the above, task execution under Cobalt kernel shows similar results for all cores, demonstrating the ability of the Xenomai extension to integrate a separate execution environment with deterministic behavior.

5.4 Architecture of the developed software

Once the validity of the digital platform for the execution of tasks with firm RT constraints has been proven, the architecture of the developed software is presented to lay the necessary foundations for the implementation of any application to be executed in the central controller, either for the execution of critical control tasks or for the execution of auxiliary HMI tasks.

The proposed software architecture consists of a series of libraries and executables for the development of control and monitoring systems for industrial processes and, more specifically, for energy conversion systems [5.27]. For this purpose, a modular software architecture has been developed to provide functionality to each of the layers of this type of systems, as shown in Fig. 5.21, and it is structured in the following parts:

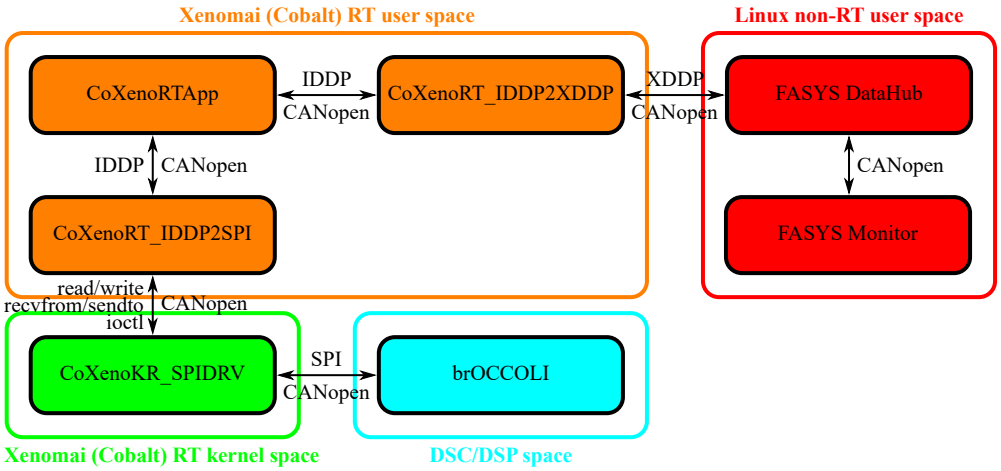

Figure 5.21: Architecture of the developed software in an embedded Linux-based OS with Xenomai RT extension.

- Internal control system (brOCCOLI). The internal control loops are implemented using the brOCCOLI library, which abstracts the hardware access and implementation of digital control systems on the Texas Instruments C2000 digital controllers. The library is based on the libraries provided by Texas Instruments under the name TI Control Suite. The deployment of this system is performed into the TMS320F28335 DSP, providing access to 16 A/D inputs for measurements, 12 PWM outputs for switching operation, 6 trip-zone inputs for switching protection, 8 digital inputs for on/off sensors and 8 digital outputs for on/off actuators.

- External control system (CoXenoRT). The external control system is implemented on the RPi CM3+. This control system obtains its RT characteristics through the Xenomai framework. All the tasks of this control system are executed in primary (RT) mode (Cobalt/Xenomai kernel) to meet firm RT constraints, and in user space to facilitate the access to external libraries and resources. In addition, launching these tasks in a separate execution environment helps to prevent them from interacting undesirably with non-RT resources, which would degrade their performance.

- Monitoring, visualization, data storage and UI system (FASYS). The outermost layer of the developed software implements the UI, the elements for data visualization, data storage and sending information to servers or remote users. This system is implemented on the Qt framework. All the tasks of this control system are executed in secondary (non-RT) mode (standard Linux kernel) because they do not need to meet firm RT constraints and do benefit from running in a more standardized and regular framework. Moreover, the effect that such tasks may have on RT critical tasks is mitigated by being launched in a separate execution environment.

- Communications system. The communications protocol between the different layers at application level is implemented using CANopen, due to the features it offers for the operation of multi-node systems and its easy applicability to various physical communication channels. For this purpose, the CANFestival library is used. The physical communications protocol between the external and internal control system is developed using the SPI protocol. By default, the embedded Linux OS provides drivers to enable applications to interact with the hardware peripherals through read, write, receive (recvfrom), send (sendto) and configure (ioctl) requests. However, these drivers are not ready for RT operation, since they are not managed by the Cobalt (Xenomai) kernel. Therefore, a specific RT driver (CoXenoKR) is developed to manage the SPI hardware peripheral through the Cobalt (Xenomai) kernel, in order to ensure firm RT operation. The exchange of information at the operating system level between the different processes integrated in the device is performed by IPC mechanisms. In particular, two mechanisms provided by the Xenomai extension are used: IDDP for information exchange between processes running in primary mode (RT) and XDDP for information exchange between a process in primary mode (RT) and another one in secondary mode (non-RT).

Regarding the control system proposed in the Fig. 5.21, all critical control tasks carried out by the central controller are integrated in the external control system (CoXenoRT), particularly in the CoXenoRTApp process. In this way, sufficient computational capacity is provided to the central controller to facilitate future upgrades of the control system involving management of a larger number of distributed controllers or integration of more complex algorithms.

The control tasks performed by the distributed controllers are integrated within the internal control system (brOCCOLI), providing direct access to the hardware peripherals in direct contact with the power stage and thus allowing fast operation under changing conditions or malfunction.

5.5 Conclusions

In this chapter, the implementation of a digital control platform on a general purpose μP has been shown. For this purpose, an embedded Linux operating system has been integrated on a RPi CM3+, with the introduction of a RT extension known as Xenomai. This RT extension provides a separate application execution environment with a responsive and deterministic behavior, allowing the execution of tasks with firm RT constraints to avoid missed deadlines.

The results obtained during the different tests demonstrate the unsuitability of executing high-priority tasks under the standard Linux kernel management and the suitability of executing RT tasks under the Cobalt kernel management provided by Xenomai. In this way, it is possible to develop a software architecture designed for the implementation of the central controller in a distributed control system allowing, on the one hand, the execution of critical control tasks mandatory for correct operation in a real-time execution environment and allowing, on the other hand, the execution of auxiliary tasks for monitoring, supervision and data collection in a standard execution environment with access to multiple libraries and resources.

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Chapter 6

Analysis of power sharing in multiport DC/DC/AC converters based on iPEBBs

6.1 Introduction

The work developed in Chapters 3-5 allows to have a distributed modular digital control system platform, composed of an arbitrary number of distributed controllers for the iPEBBs and a central controller programmed inside a general purpose microprocessor under a real-time operating system. In this way, the implementation of a modular multiport converter for the integration of distributed resources is enabled, particularized for the use of HESSs, supply of bidirectional local loads and integration with the power grid.

Regarding the above, local small-scale power systems are being developed to promote the introduction of renewable energies, since they are closely related to distributed generation unlike the conventional ones. The concept of microgrid appears in order to categorize this type of systems, which are evolving over time [6.1]. Microgrids usually have some energy storage units to support the renewable power generation, which is non-deterministic. Different kind of energy storage systems (ESS) can be installed, some of them being more dedicated to the energy needs (batteries), while others show their advantages in terms of power capability (supercapacitors) [6.2, 6.3]. In order to exploit the advantages of the different types of energy storage system, microgrids can use an hybrid implementation (e.g. batteries and supercapacitors), so that a flexible and reliable operation is achieved [6.4, 6.5].

Batteries have relatively high energy density but they are not suitable when suffering high variations of power. This is because the internal electrochemical reactions

inside the battery produce a process of degradation [6.6, 6.7]. To face this problem, supplementary supercapacitors can be used since they work properly under high variations of power [6.8–6.10], though they have low energy density. Therefore, it is necessary to perform a power sharing between the battery-based ESS and the supercapacitor ones [6.11–6.16].

However, any error in the calculation of the power sharing produces a mismatch, which may disturb the system performance. Errors in the sensors, in the estimation of the power load or in the control actions of the converters often appear during the operation of a power system. Thus, the influence of these mismatches should be analyzed to determine the resultant effects on the system under control.

The analyzed case is a multiport DC/DC/AC converter, as a simplification of a complete hybrid DC/AC microgrid, composed of a DC load, a battery and a supercapacitor. A schematic diagram, based on the concept of distributed intelligent Power Electronics Building Blocks (iPEBBs) [6.17], is shown in Fig. 6.1. As explained in [6.17], an iPEBB is a single-phase power cell (upper and lower power switches, parallel capacitor, and series inductor in mid-point) with built-in voltage and current sensors, and a digital control system which manages the power cell.

The power converters outputs are coupled to a DC bus. Additionally, an inverter is connected to exchange energy with the AC grid. Since the DC bus is the central element of the system and the common coupling point of all iPEBBs, the convention used in this chapter considers positive any power (either demanded by a load or given by a source) provided as an output by the DC bus.

The objective of this chapter is to analyze the power mismatch problem in the multiport DC/DC/AC converter when grid power is limited and to propose several compensation alternatives. For this purpose, control of the DC-link voltage in saturation conditions is carried out. Some references can be found in literature targeting the specific analysis of DC-link voltage control under saturation conditions for the current control [6.18–6.21].

The main contribution of this chapter is to propose different methods to compensate this power mismatch by directly using the information given by the DC-link voltage controller. This way, power mismatch is mitigated by the compensation methods without requiring the information from any of the sensors in the loads and sources connected to the DC bus. Operation in islanding mode is considered to demonstrate the robustness of the compensation techniques. Moreover, errors in sensors and communication delays are analyzed to validate the performance of the system.

The proposed target applications are hybrid microgrids or distribution systems in which multiple paths for the power flow could exist. In those applications, the limits for the power coming from the AC grid could lead to the very extreme situation in which there are DC-side loads with a power consumption (or generation) while the AC grid is disconnected. In those cases, the DC/AC converter is useless.

Regarding the standards, IEC 60038:2009 [6.22] states that low-voltage (LV) systems can withstand a steady-state voltage variation of $\pm 10\%$ in the supply terminals.

CENELEC EN 50160:2010 [6.23] also specifies a ±10% magnitude variation to be accomplished 95% of the time of the week for LV systems, allowing normal rapid voltage changes of 5% and infrequent rapid voltage changes of 10%. ANSI C84.1-2016 [6.24] shows that normal voltage fluctuations do not normally exceed ±5% of the nominal value. IEEE Std 1159-2019 [6.25] does not consider variations within ±10% of the nominal voltage as electromagnetic phenomena, whereas IEEE Std 1250-2018 [6.26] defines a voltage regulation of ±5% in normal conditions. IEEE Std 1547-2018 [6.27] specifies voltage ride-through requirements for distributed energy resources (DERs) connected to electric power systems (EPSs), so that continuous operation has to be guaranteed if voltage range is from 0.88 to 1.1 pu. Therefore, the boundary of working conditions is a maximum variation of ±5% in the DC nominal voltage.

IEEE Std 2030.7-2017 [6.28] states that microgrids are capable to operate in islanding mode and supply local loads, but also connected to the grid at the point of interconnection (POI). Thus, to limit the maximum power to be exchanged depending on grid state, a grid power limit is established. Whilst a conventional AC/DC converter would be suitable to meet the maximum DC voltage variation during normal conditions, it is prone to fail whenever grid power limit is reached. This can happen either when it is required to limit the maximum power exchanged with the grid or to operate in islanding mode due to a controlled disconnection from the grid or a blackout. Therefore, the introduction of an ESS in the DC grid with a multiport DC/DC/AC converter provides redundancy and thus improves the reliability of the DC grid, since local loads/sources can continue to operate regardless of the state of the main grid.

In addition, applications with regenerative electric motors or any DC-side generation may be suitable for this topology to limit the exchanged grid power. This way, fast power variations will be provided by the ESS whereas the grid only manages the base power and the energy demand to maintain the ESS conveniently charged, always guaranteeing that the total grid power is below the configured limit.

It has to be remarked that the proposals in this chapter do not need for the additional installation of ESS units but despite it uses the elements already available in the hybrid DC/AC grid, by implementing a collaborative control between all of them.

In addition, the use of the same power cell (iPEBB) for all power converters reduces costs and facilitates maintenance, since the hardware is common and only its programming varies depending on the application. It would also facilitate the integration of new power units with a similar nominal power without having to design a new specific power stage, providing flexibility to the system when introducing new loads/sources, a common case in distributed generation systems. In addition, several iPEBBs could be parallel combined to enable power units with higher nominal powers, providing scalability to the system.

This research is mainly based on the contributions presented in [6.29]. Past work is extended by a meaningful theoretical analysis of the system performance and compensation methods under saturation conditions derived from power limitations. New simulation and experimental results have been developed to consider islanding opera-

tion, thus demonstrating the robustness of the proposed control system under sudden AC grid disconnection. In addition, an analysis of the effect of power measurement (sensor) errors and communication delays in the performance of the compensation methods is performed.

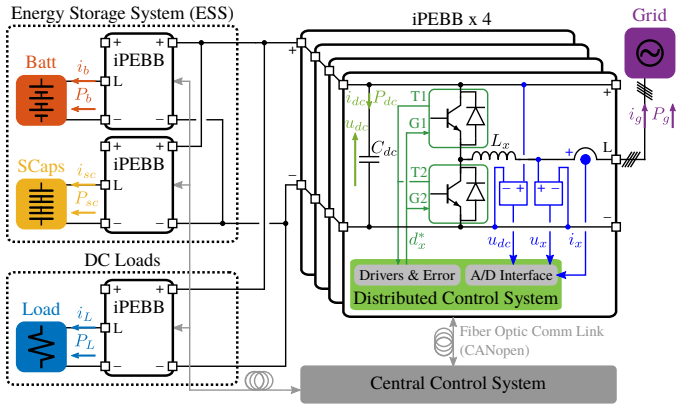

Figure 6.1: Electrical diagram of the multiport DC/DC/AC converter based on the use of Intelligent PEBBs (iPEBBs).

6.2 Power sharing issues

The multiport DC/DC/AC converter used in this work is made up of several power units interconnected through a dc-link capacitor. The considered units are an aggregated regenerative DC load, which represents the different loads connected to the DC grid; a Li-ion battery; a supercapacitor, and a grid-tied interlinking converter connected to the AC grid (Fig. 6.1). In order to supply the DC load, a power sharing between the different power converters is employed. Considering as the starting point an operational AC grid, the base load demand is provided by the AC connection, whereas the peak load demand is given by the ESS. Between the two available sources, the low frequency components are supplied by the battery (energy source) whereas the high frequency components are supplied by the supercapacitor (power source). By using two low-pass/high-pass filters with different cutoff frequencies, it is possible to tweak the power sharing as desired.

Fig. 6.2 shows the proposed control diagram to carry out the power sharing mechanism. The power sharing is computed by the central controller, which sends the power references (P^*_{x0}) to the power control of the different distributed control units, in order to manage the current/power of the different system power converters. This control system implementation requires to have an accurate measurement of the power by each of the converter units. However, sensor accuracy or saturation phenomena in the control action of any unit will induce differences in the real power sharing.

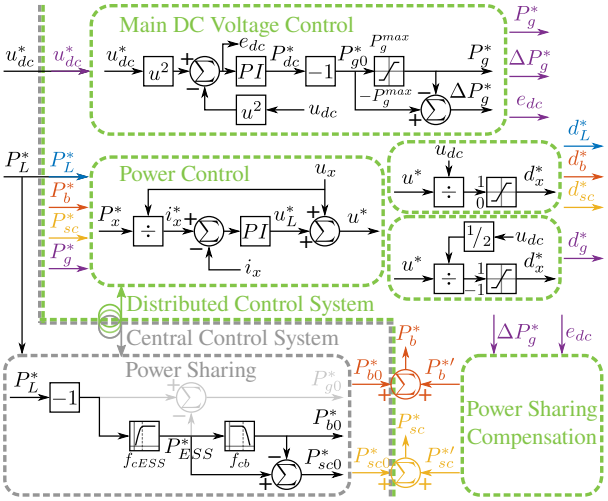

Figure 6.2: Control diagram of the multiport DC/DC/AC converter. Gray units are integrated in the central control system whereas green units are integrated in the distributed control units.

Focusing on the DC side of the multiport converter (Fig. 6.1), the power balance expression which links the different power units (load: P_L, battery: P_b, supercapacitor: P_{sc}, grid: P_g and DC bus capacitor: P_{dc}) is given by (6.1).

$$P_L + P_b + P_{sc} + P_g + P_{dc} = 0 \tag{6.1}$$

As it can be seen in Fig. 6.2, the power in the DC bus capacitor is not directly controlled, being dependent on the power mismatch (ΔP) among the different controlled power units. From (6.1), it is possible to obtain the magnitude of the DC bus capacitor power as given by (6.2).

$$P_{dc} = -\Delta P = -\left(P_L + P_b + P_{sc} + P_g\right) \tag{6.2}$$

For this purpose, it is necessary to calculate the power handled by the different units of the system using the expressions (6.3)-(6.6).

$$P_L = u_L i_L \tag{6.3}$$

$$P_b = u_b i_b \tag{6.4}$$

$$P_{sc} = u_{sc} i_{sc} \tag{6.5}$$

$$P_g = u_{ga} i_{ga} + u_{gb} i_{gb} + u_{gc} i_{gc} \tag{6.6}$$

Therefore, if the power sharing is perfectly done, the power mismatch is zero and the DC grid is balanced. Whenever a power mismatch occurs, (6.2) is not longer equal to zero and the power surplus or shortage has to be delivered/absorbed by the DC bus

capacitor in order to compensate for that difference, acting as a power buffer. The problem is that this variation of DC bus capacitor power because of the power mismatches produces variations in the DC-link voltage. These DC-link voltage deviations are undesirable and thus have to be kept under certain bounds in order to avoid the system to reach unstable conditions. The absolute minimum limit for the DC-link voltage is twice the peak value of the grid phase voltage, since it is the minimum value needed to maintain the controllability of the system in inverter mode. The absolute maximum limit is determined by the maximum operating voltage of the power devices to not deteriorate them. In order to avoid the operation close to the absolute limits, a 5% margin is introduced in the actual limits.

As shown in Fig. 6.2, the grid-tied DC/AC inverter controls the DC-link voltage, so its variation will depend on the stiffness of its control system. Additionally, the variations induced in the DC-link voltage because of the power mismatch are also affected by the maximum power that can be managed by the grid-tied DC/AC converter ($\pm P_g^{max}$). Operation under saturation conditions in the delivered/absorbed power has still to guarantee an stable and stiff DC-link voltage.

Note that the addition of new unpredictable energy loads or sources would affect the power sharing of the system. Power produced/consumed by new sources/loads shall be estimated to be considered by the central controller algorithm to generate a modified ESS power reference. Nevertheless, if new load/source power could not be properly estimated due to its unpredictability, DC voltage control would provide the corresponding power mismatch.

Assuming that the power control of all the power units is accurate and much faster than the DC-link voltage control, the power control loops are considered ideal (unitary gain) from the point of view of the DC-link voltage control. This way, the system behavior can be modeled with the diagram shown in Fig. 6.3. There is a limitation in the minimum/maximum grid power, which is represented by a saturation block. If this limitation is reached, the applied grid power into the system ($P_g = P_g^*$) cannot match anymore the required power by the controller (P_{g0}^*). This way, the DC-link voltage control enters in saturation and loses the ability to properly maintain the DC-link voltage.

The aforementioned problems are following illustrated. Fig. 6.4 shows the power sharing issues which appear when the grid power is limited, so that saturation in the grid DC-link voltage controller is produced. In normal conditions, the grid provides the base load demand, whereas short-term power variations are provided by the ESS and the DC bus, trying to keep grid power dynamics as slow as possible to not disturb the grid. Since the DC-link voltage is controlled by the grid converter, power mismatches are also supplied by the grid-side converter. When the grid power reaches the minimum/maximum limit, the DC-link voltage either drops to the rectifier level or rises to fault values.

Constant power loads are commonly used to validate the robustness of voltage control algorithms, since they put the system in a worst-case scenario. For the evaluation of

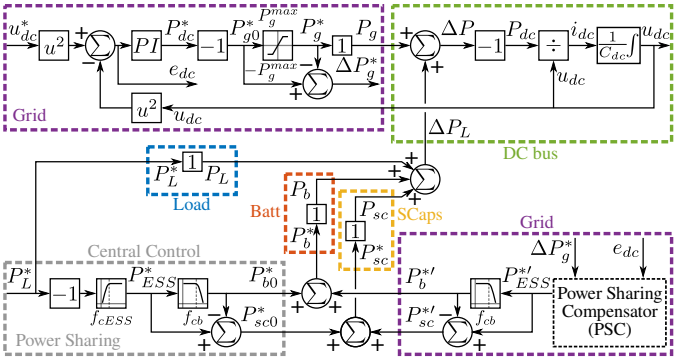

Figure 6.3: Model of the multiport DC/DC/AC converter with Power Sharing Compensator (PSC) from the point of view of the grid-side DC voltage control (ideal power control loops shown as unitary gain).

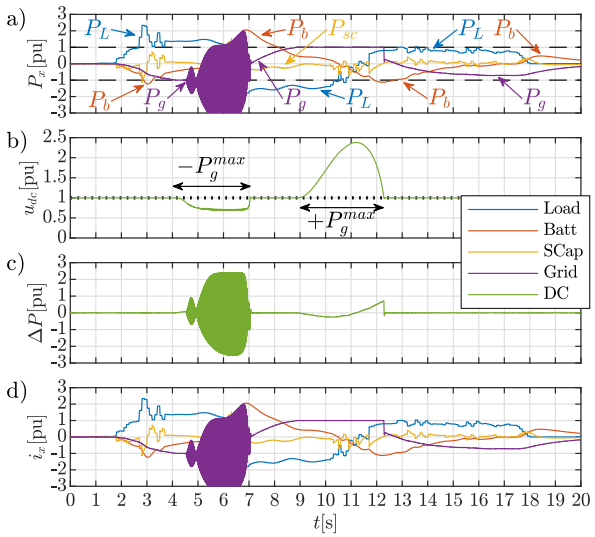

Figure 6.4: Power sharing issues when the grid power is limited (±1 pu). a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Current comsumption. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus. Dashed lines: grid power limits.

the system dynamics, a bidirectional electronic load able to generate rich time-varying profiles, either as a constant power or constant current load is used. The underpinning idea is to emulate the behaviour of high performance electrical drives.

At 4.1 s, the DC-link voltage starts dropping because of grid power reaching the minimum limit and thus the DC-link voltage control is saturated. At 4.5 s, the DC-link voltage reaches 400 V (0.8889 pu), which is twice the peak value of the grid phase voltage (200 V) and the minimum value that guarantees a stable system operation.

Operation under that limit causes system instability when the DC/AC converter work in inverter mode delivering power to the grid, hence the shown oscillating behavior of the grid power. At 7 s, the DC-link voltage raises above the minimum limit, resulting in the system to be stabilized. From 9 s to 12 s, the DC-link voltage starts increasing because the grid power reaching the maximum limit and the DC-link voltage control being also saturated. In this event, the DC-link voltage reaches values greater than twice the nominal value (2.38 pu), which can deteriorate the power devices. This way, the system operation is compromised and correction actions are required to take back DC-link voltage within safe values.

In order to solve this problem, it is necessary to dynamically correct power mismatches to ensure a suitable operation. Considering that power mismatches are normally a transient problem, often with fast dynamics, this chapter proposes several alternative compensation methods relaying on a modified operation of the ESS.

A new control module called Power Sharing Compensator (PSC) is introduced into the control diagram (Fig. 6.2 and Fig. 6.3) with a view to performing the power sharing compensation. Extra power references ($P_x^{*\prime}$) are computed by this module and commanded together with the initial power references (P_{x0}^{*}) to the power control loops. Since it is required to compensate the power mismatches rapidly, the power sharing compensation is internally performed by each distributed control unit.

6.3 Compensation techniques

As mentioned above, power mismatches in the power sharing produce a deviation of the DC-link voltage from the nominal value. Thus, some kind of correction has to be applied to mitigate the problem. Three different compensation techniques are proposed: 1) direct power reference compensation, 2) auxiliary DC voltage control and 3) enhanced power reference compensation.

The challenge in the compensation is to properly estimate the power mismatch. Ideally, it could be determined by measuring the power in all system units and computing the summation, as shown in (6.2)-(6.6). However, this requires good accuracy in all current/voltage sensors of the system and does not allow the addition of new power units that do not provide any feedback of the power consumption.

Alternatively, an estimation method for the compensation power can be done by analyzing the shape of the grid DC-link voltage controller. The grid-side DC voltage control is controlled by the grid-tied converter using a quadratic voltage control (QVC) [6.30] as shown in Fig. 6.2 and Fig. 6.3, so that the control action is expressed in terms of power. If saturation in the grid-tied converter is produced, the controller will not longer be able to apply the required power. The remaining grid power (ΔP_g^*) can be considered as the required extra power to counteract the power mismatch. This way, good accuracy is only required in the current/voltage sensors of the grid power units to compute the power mismatch, reducing the number of elements that can introduce errors in its calculation.

In order to determine the options to compensate this power mismatch, the control law of the discrete QVC based on a PI controller is discussed. Observing the system model (Fig. 6.3) and for a given proportional gain (K_p), integral gain (K_i) and sample period (T_s), the expression (ideal form) to calculate the control action (u) of the controller depending on the error (e) at any sample k is given by (6.7)-(6.9).

$$e_k = e_{dc} = \left(u_{dc}^*\right)^2 - \left(u_{dc}\right)^2 \tag{6.7}$$

$$u_k = u_k^0 = \underbrace{K_p e_k}_{\text{P action}} + \underbrace{K_p \left(K_i T_s - 1\right) e_{k-1} + u_{k-1}}_{\text{Integral action}} = P_{dc}^* \tag{6.8}$$

$$P_{g0}^* = -P_{dc}^* = -u_k;\ P_g^* = \text{sat}(P_{g0}^*);\ \Delta P_g^* = P_{g0}^* - P_g^* \tag{6.9}$$

Since the implemented controller provides integral action, an anti-windup mechanism that limits this action during saturation is required. In this case, the realizable references method is used due to its performance and simplicity in discrete systems [6.31] when the controller has the same number of poles than zeros. Considering a discrete PI controller implemented by the bilinear approximation, the calculations performed by the anti-windup method during saturation conditions to correct the actual control action (u_k) and error (e_k) with realizable values (u_k^r, e_k^r) for the next iteration (u_{k+1}, e_{k+1}) are given by (6.10) and (6.11) respectively.

$$u_k^r = -P_g^* = -\text{sat}(-u_k);\ u_{k+1} = u_k^r \tag{6.10}$$

$$e_k^r = \frac{u_k^r - K_p \left(K_i T_s - 1\right) e_{k-1} - u_{k-1}}{K_p};\ e_{k+1} = e_k^r \tag{6.11}$$

This way, when the DC-link voltage reaches steady state ($u_{dc} \approx u_{dc}^*$, $e_k \approx 0$, $e_{k-1} \approx 0$), the controller only applies the integral action. Once the system enters into saturation, the grid converter power is limited and the anti-windup mechanism starts actuating by limiting the integral action. If saturation is kept at least during two samples periods, both the previous (u_{k-1}) and the realizable action control (u_k^r) take the limited minimum/maximum value. This way, (6.11) can be simplified into the expression given by (6.12).

$$e_k^r = \left(1 - K_i T_s\right) e_{k-1};\ e_{k+1} = e_k^r \tag{6.12}$$

Assuming that $|1 - K_i T_s| < 1$, the realizable error (e_k^r) and hence the previous error (e_{k-1}) will converge to zero. In this case, from (6.7)-(6.10), it is possible to obtain the expression which defines the remaining grid power, as shown in (6.13) and (6.14).

$$\Delta P_g^* = -\left(u_k^0 - u_k^r\right) = -\left(u_k^0 - u_{k-1}\right) \tag{6.13}$$

$$\Delta P_g^* = -K_p e_{dc} = -K_p \left(\left(u_{dc}^*(t)\right)^2 - \left(u_{dc}(t)\right)^2\right) \tag{6.14}$$

Therefore, the applied grid power by the converter (P_g^*) will be dominated by the limited integral action ($\pm P_g^{max}$) whereas the remaining grid power (ΔP_g^*) will be

dominated by the proportional action which is not provided by the converter due to saturation. Taking all of this into account, the model in Fig. 6.3 can be simplified under saturation conditions, so that the model shown in Fig. 6.5 is obtained.

Since the applied grid power is limited during saturation, the power mismatch (ΔP) is no longer zero and a disturbance of the DC-link voltage is produced. Extra power has to be introduced into the system in order to minimize the mismatch, obtaining a corrected power mismatch ($\Delta P'$) as close as possible to zero and hence reducing the DC-link voltage deviation.

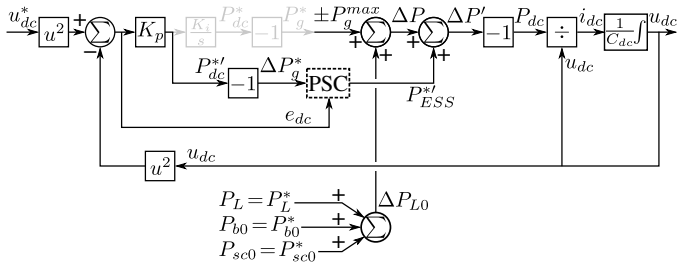

Figure 6.5: Simplified model under saturation conditions of the multiport DC/DC/AC converter with DC-link voltage control carried out by the grid and the Power Sharing Compensator (PSC).

Analyzing the simplified model for saturation (Fig. 6.5), a expression which relates the different variables of the system, including the Power Sharing Compensator (PSC), in the forward path is calculated, as given by (6.15).

$$\Delta P(t) + \underbrace{PSC \cdot \Delta P^*_g(t)}_{P^{*\prime}_{ESS}} + C_{dc} \cdot u_{dc}(t) \frac{\mathrm{d}u_{dc}(t)}{\mathrm{d}t} = 0 \tag{6.15}$$

If (6.14) and (6.15) are combined and then linearized for the equilibrium point (U_{dc0}, U^*_{dc0}, $\Delta P^*_g = 0$, $\Delta P = 0$) by using Taylor series [6.30], the expressions in (6.16) and (6.17) are obtained.

$$\begin{aligned} &\left(s\tfrac{C_{dc}}{2K_p} + PSC\right)\Delta P^*_g(s) \\ &\quad + \left(sC_{dc}\right)U^*_{dc0}\Delta u^*_{dc}(s) = -\Delta P(s) \end{aligned} \tag{6.16}$$

$$\begin{aligned} &\left(sC_{dc} + 2K_p PSC\right)U_{dc0}\Delta u_{dc}(s) \\ &\quad - \left(2K_p PSC\right)U^*_{dc0}\Delta u^*_{dc}(s) = -\Delta P(s) \end{aligned} \tag{6.17}$$

Assuming that the DC-link voltage reference does not vary ($\Delta u^*_{dc} = 0$, fixed DC-link voltage), it is possible to obtain from (6.16) and (6.17) the transfer functions which

define the model of the system, as given by (6.18)-(6.20).

$$\frac{\Delta P_g^*(s)}{\Delta P(s)} = \frac{-2K_p}{sC_{dc} + 2K_p PSC} \tag{6.18}$$

$$\frac{\Delta u_{dc}(s)}{\Delta P(s)} = \frac{-1/U_{dc0}}{sC_{dc} + 2K_p PSC} \tag{6.19}$$

$$\frac{\Delta u_{dc}(s)}{\Delta P_g^*(s)} = \frac{1}{2K_p U_{dc0}} \tag{6.20}$$

As it can be seen, the evolution of both the remaining grid power (ΔP_g^*) and the DC-link voltage deviation (Δu_{dc}) depends on the structure of the PSC, whereas the ratio between both variables is constant regardless of the PSC. Therefore, the PSC is able to mitigate them, so different alternatives for the PSC will be discussed below in order to analyze their performance.

6.3.1 Direct power reference compensation

The first compensation technique consists of tracking the remaining grid power ($\Delta P_g^* = -K_p\left(u_{dc}^*(t)^2 - u_{dc}(t)^2\right)$) and delivering an extra power with the same value, as shown in Fig. 6.6a. In this case, the PSC is simply a unitary gain.

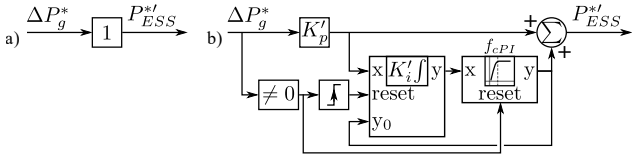

Figure 6.6: Model of Power Sharing Compensator (PSC): direct (a) and enhanced (b) power reference compensation.

This extra power will be provided by the ESS ($P_{ESS}^{*\prime}$) since the grid-tied converter is working under saturation conditions, as shown in Fig. 6.5. A low-pass filter is used to determine the battery and supercapacitor references ($P_b^{*\prime}$ and $P_{sc}^{*\prime}$).

The performance of the direct power reference compensation can be determined by computing (6.18) and (6.19) for the particular case of $PSC = 1$, obtaining the transfer functions shown in (6.21).

$$\frac{\Delta P_g^*(s)}{\Delta P(s)} = \frac{-2K_p}{sC_{dc} + 2K_p}; \quad \frac{\Delta u_{dc}(s)}{\Delta P(s)} = \frac{-1/U_{dc0}}{sC_{dc} + 2K_p} \tag{6.21}$$

The resultant transfer functions correspond to first order systems and hence there is not overshoot in the evolution of the remaining grid power and the DC-link voltage. Then, the maximum deviation of both variables (ΔP_g^{*max}, Δu_{dc}^{max}) can be obtained

with the maximum power mismatch ($|\Delta P^{max}|$) via the DC gain ($\lim_{s\to 0}$) of the transfer functions in (6.21), whose expressions are given by (6.22).

$$\Delta P_g^{*max} = |\Delta P^{max}|;\ \Delta u_{dc}^{max} = \frac{|\Delta P^{max}|}{2K_p U_{dc0}} \tag{6.22}$$

As it can be seen, the variations of both the remaining grid power and the DC-link voltage are not fully mitigated in the direct power reference compensation, so the power mismatch (ΔP) is not totally compensated. Following, alternative compensation techniques are discussed in order to improve the PSC performance.

6.3.2 Auxiliary DC voltage control

The second compensation technique consists on an auxiliary DC voltage control in the ESS to support the grid-side DC voltage control during saturation events. The proposed scheme is shown in Fig. 6.7. Under normal conditions, only the grid-side DC voltage control has to be active. Therefore, an enabling strategy which triggers the auxiliary DC voltage control needs to be considered. The enabling strategy is similar

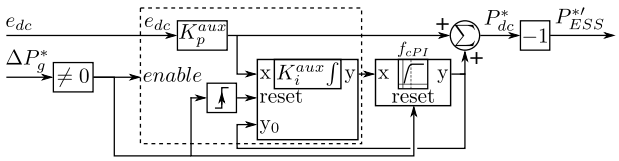

Figure 6.7: Model of Power Sharing Compensator (PSC): auxiliary DC voltage control.

to the one applied for the direct power reference compensation. The power mismatch resulting from the saturation condition in the grid-side DC voltage control provokes a non-zero remaining grid power ($\Delta P_g^* \neq 0$), which is used as the trigger event.

Same sharing method than the one in Subsection 6.3.1 is used for the computation of the extra reference of the battery ($P_b^{*\prime}$) and the supercapacitor ($P_{sc}^{*\prime}$).

Two different controller implementations will be studied for this compensation technique: P and PI controller. If zero steady-state errors are not required in the voltage value during the saturation event, a P controller is valid.

Unlike the direct power reference compensation, the input of the auxiliary DC voltage control is the error (e_{dc}) instead of the remaining grid power (ΔP_g^*). Thus, this compensation technique is not affected by the proportional gain of the grid-side DC voltage control (K_p). The corresponding PSC transfer function has to be computed in order to compare its performance with the previous method. Considering the transfer function of a PI controller in ideal form ($C(s) = K_p^{aux} + K_p^{aux} K_i^{aux}/s$), the equivalent

PSC is given by (6.23) and the corresponding transfer functions by (6.24) and (6.25).

$$PSC^{aux} = \frac{1}{K_p}\left(K_p^{aux} + \frac{K_p^{aux}K_i^{aux}}{s}\right) \tag{6.23}$$

$$\frac{\Delta P_g^*(s)}{\Delta P(s)} = \frac{-s2K_p}{s^2C_{dc} + s2K_p^{aux} + 2K_p^{aux}K_i^{aux}} \tag{6.24}$$

$$\frac{\Delta u_{dc}(s)}{\Delta P(s)} = \frac{-s/U_{dc0}}{s^2C_{dc} + s2K_p^{aux} + 2K_p^{aux}K_i^{aux}} \tag{6.25}$$

In the particular case of a pure proportional controller ($K_i^{aux}=0$), it is possible to calculate from (6.25) the optimal auxiliary proportional gain (K_p^{auxP}) depending on the desired maximum voltage deviation (Δu_{dc}^{max}) and the maximum power mismatch ($|\Delta P^{max}|$), with the expression given by (6.26).

$$K_p^{auxP} = \frac{|\Delta P^{max}|}{2U_{dc0}\Delta u_{dc}^{max}} \tag{6.26}$$

When a PI controller is used instead, the gains are selected to mimic the behavior of the grid-side DC voltage controller. Therefore, both the auxiliary proportional gain (K_p^{auxPI}) and the auxiliary integral gain (K_i^{auxPI}) are made equal to the original proportional and integral gains (K_p, K_i), as stated by (6.27).

$$K_p^{auxPI} = K_p;\ K_i^{auxPI} = K_i \tag{6.27}$$

Additionally, since the auxiliary DC voltage control is only required to work during saturation events, the effect of the integral action after the transient recovering has to be removed. This way, steady-state contribution of the battery power ($P_b^{*\prime}$) is avoided, thus improving its life usage. For that, a resettable high-pass filter (HPF) is placed in the output of the integrator, as shown in Fig. 6.7. This way, the HPF avoids steady-state contribution of the ESS in normal conditions, but it is bypassed (forced activation of reset) during the saturation condition in the DC voltage control ($\Delta P_g^* \neq 0$). In addition, it has to be remarked that, in order to avoid inconsistency between the value applied to the ESS by the HPF and the dictated integrator output value whenever saturation appears, it is necessary to modify the integrator state to be initialized with the HPF output value each time the saturation condition is reached.

6.3.3 Enhanced power reference compensation

As shown in the expressions given by (6.21) and (6.22), an increment in the proportional gain induces a reduction in the voltage deviation. Therefore, it is possible to implement an enhanced power reference compensation by managing the remaining grid power (ΔP_g^*) through an extra proportional gain (K_p'), which amplifies the effect of the original proportional gain of the grid-side DC voltage control (K_p). An extra integral

action (K_i') can also be added to completely eliminate the voltage deviation in steady state. According to that, an enhanced power reference compensation is proposed, as shown in Fig. 6.6b. As it can be seen in Fig. 6.6b, same sharing method than the one in Subsection 6.3.1 is used for the computation of the extra battery and supercapacitor references.

From (6.18) and (6.19), making a similar analysis to the one in Subsection 6.3.2 with $PSC = K_p' + K_p'K_i'/s$, it is possible to obtain the transfer functions in (6.28) and (6.29), and the optimal extra proportional gain for a P controller ($K_p'^P$) and the extra proportional ($K_p'^{PI}$) and integral ($K_i'^{PI}$) gain for a PI controller in (6.30).

$$\frac{\Delta P_g^*(s)}{\Delta P(s)} = \frac{-s2K_p}{s^2C_{dc} + s2K_pK_p' + 2K_pK_p'K_i'} \tag{6.28}$$

$$\frac{\Delta u_{dc}(s)}{\Delta P(s)} = \frac{-s/U_{dc0}}{s^2C_{dc} + s2K_pK_p' + 2K_pK_p'K_i'} \tag{6.29}$$

$$K_p'^P = \frac{|\Delta P^{max}|}{2K_pU_{dc0}\Delta u_{dc}^{max}};\ K_p'^{PI} = 1;\ K_i'^{PI} = K_i \tag{6.30}$$

Also as stated in Subsection 6.3.2, an additional high-pass filter can be put in the output of the controller, as shown in Fig. 6.6b, for avoiding any steady-state contribution of the PSC when system recovers from saturation.

6.3.4 Operation in islanding mode

All the analysis carried out so far in this section assumes an operating point in which the minimum/maximum grid power is varied with slower dynamics compared to the internal converter control, which is the case for normal system operation. However, in the event of grid disconnection, the system has to immediately enter in islanding mode. For that, the grid power limit (P_g^{max}) has to be reduced to 0. Fig. 6.3 shows that this will suddenly force zero grid power reference (P_g^*), creating a power mismatch (ΔP) that has to be dealt by the different compensation techniques.

Direct and enhanced power reference compensation control the remaining grid power (ΔP_g^*), while auxiliary DC voltage control manages the voltage error (e_{dc}). By looking at Fig. 6.3, the effect of a sudden reduction in the grid power (P_g^*) on the control variables can be determined.

In the case of using the remaining grid power (ΔP_g^*), a sudden reduction in the grid power limit would have a direct effect on it, as shown in the expression given by (6.31).

$$\Delta P_g^*(t) = P_{g0}^*(t) - P_g^*(t) \tag{6.31}$$

In the case of the voltage error (e_{dc}), the reaction is indirectly coupled through the DC-link voltage dynamics. This is shown in (6.32).

$$\Delta P(t) + C_{dc} u_{dc}(t) \frac{\mathrm{d}u_{dc}(t)}{\mathrm{d}t} = 0; \; e_{dc} = u_{dc}^{*2}(t) - u_{dc}^{2}(t) \tag{6.32}$$

Therefore, auxiliary DC voltage control has a certain delay in acting in the event of a sudden reduction in the grid power limit when entering islanding mode, whereas direct and enhanced power reference compensations react immediately.

6.3.5 Summary

Comparing the expressions which define the behavior of the different compensation techniques, (6.24), (6.25), (6.28) and (6.29), an equivalent behavior can be observed between the auxiliary DC voltage control and the enhanced power reference compensation. Nevertheless, controller gain selection is a little more straightforward in the enhanced power reference compensation since it does not depend on the proportional gain of the main DC voltage controller (K_p), as shown in (6.26), (6.27) and (6.30). In any case, either of the two methods could be used indistinctly in a first approximation.

However, as discussed in Subsection 6.3.4, since the control variable is not the same for both compensation techniques (voltage error e_{dc} vs remaining grid power ΔP_g^*), auxiliary DC voltage control would respond more slowly to the islanding mode condition. Due to this, the preferred compensation technique is the enhanced power reference compensation. This statement will be validated via simulations to certify the better performance of the enhanced power reference compensation during islanding operation.

Regarding the choice of a purely proportional controller or a PI controller, the latter allows to eliminate any voltage deviation in steady state. However, the implementation of the PI controller adds additional complexity to the system, since it requires a resettable integrator and high-pass filter, whereas only a simple gain is needed for the P controller. In the P controller options, the memory footprint is 2 floating variables (8 bytes) whereas the number of operations is 1 read, 1 multiplication and 1 write. Considering the PI controller alternatives, the memory footprint is 11 floating and 2 boolean variables (46 bytes) whereas the number of operations is 15 reads, 5 multiplications, 4 sums, 2 boolean comparisons and 10 writes.

Note that the power mismatch compensation is an extra addition to an already functional control in the iPEBB, which consists of power and DC voltage control loops in the case of the grid-side power branches, with all the communication protocol also integrated. Thus, since the digital signal processor of the iPEBB is optimized to reduce costs, both options (with P and PI controllers) are offered for cases where the digital processor is close to its limits. Both P and PI controllers will be tested during the simulations and experimental tests to determine their performance.

6.4 Simulation results

Several simulations for the validation of the proposed compensation techniques are carried out in MATLAB/Simulink with the parameters described in Table 6.1. A specific load power profile lasting 20 s has been selected to test saturation in the grid-side converter.

Table 6.1: System parameters.

Parameter	Value
Filter inductor inductance (L)	1.7 mH
Filter inductor resistance (R)	0.33 Ω
DC-link total capacitance (C_{dc})	750 μF
Nominal grid power (base power value)	1 kW
Nominal DC-link voltage (DC base voltage value)	450 V
Nominal grid line RMS voltage	245 V
Nominal grid frequency	50 Hz
Nominal load voltage	48 V
Nominal battery voltage	144 V
Nominal supercapacitor voltage	48 V
Current control loop bandwidth	300 Hz
Grid-side DC voltage control bandwidth	20 Hz
Grid-side DC voltage control proportional gain (K_p)	0.06664
Grid-side DC voltage control integral gain (K_i)	88.86
ESS HPF cutoff frequency (f_{cESS})	0.1 Hz
Battery LPF cutoff frequency (f_{cb})	0.5 Hz
Compensation PI HPF cutoff frequency (f_{cPI})	1 Hz
Central control system frequency	100 Hz
Distributed control system frequency	10 kHz

6.4.1 Ideal case

Results when neither grid power restriction nor compensation are shown in Fig. 6.8. Due to the limited bandwidth of the grid-side DC voltage control, some small DC voltage deviations are produced during the transients. Still, the system operation is nearly ideal. However, when the grid power exceeds the maximum power, the problem shown in Section 6.2 will arise. In the following discussion, grid power limits are set to ±1 pu for comparison of the proposed compensation mechanisms. Moreover, the grid power limits are forced to ±0 pu between 12 s and 15 s so compensation techniques under islanding can also be tested.

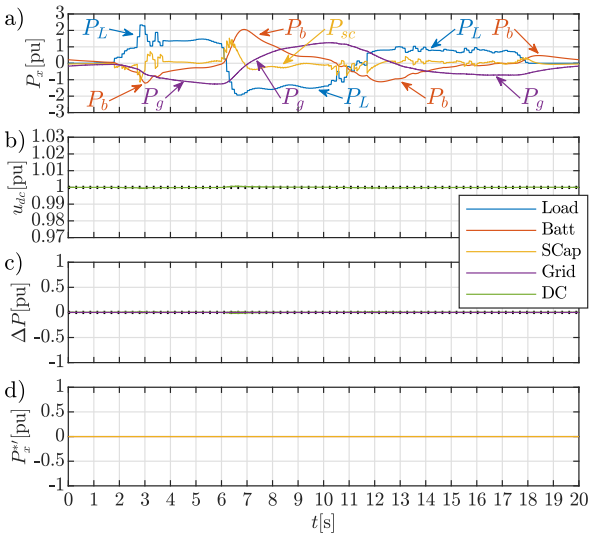

Figure 6.8: Simulation results: Ideal case. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus. Dashed lines: grid power limits. Dotted lines: theoretical model evolution.

6.4.2 Direct power reference compensation

Second simulation considers the direct power reference compensation presented in Subsection 6.3.1. Results are shown in Fig. 6.9. As it can be seen, the maximum grid power is accomplished so saturation conditions are considered. The DC-link voltage (u_{dc}) has a similar evolution than in the ideal case, except when saturation is produced. During these events, the power mismatch (ΔP) is not zero (Fig. 6.9c), so the remaining grid power (ΔP_g^*) takes a non-zero value and a DC-link voltage deviation is produced. For the compensation, the PSC generates an extra power reference for the ESS (Fig. 6.9d), which is shared between the battery and the supercapacitor. Thus, when comparing with the results shown in Fig, 6.4, the improved response is clearly visible.

Although the system continues operating within limits, there is a variation of about ± 0.02 pu in the DC-link voltage. As predicted by (6.22), this compensation method cannot totally compensate for the power mismatch. When the system enters in islanding, an expected larger variation can be easily seen.

6.4.3 Auxiliary DC voltage control

Third simulation is performed according to the discussion in Subsection 6.3.2 by enabling the auxiliary DC voltage control with a proportional controller. The propor-

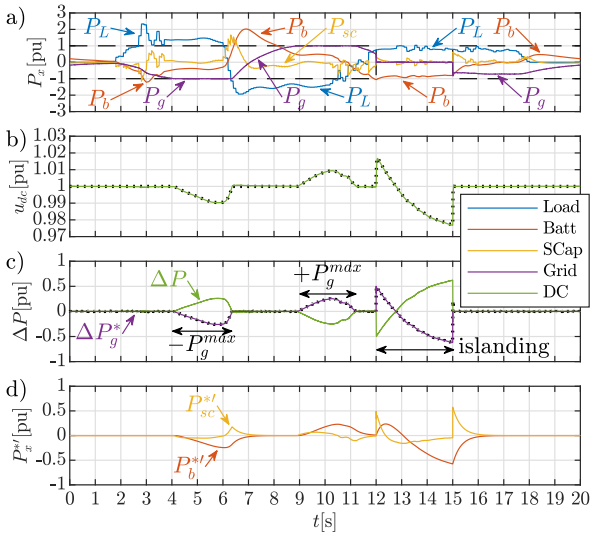

Figure 6.9: Simulation results: Direct power reference compensation. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus. Dashed lines: grid power limits. Dotted lines: theoretical model evolution.

tional gain of the auxiliary DC voltage control is set to twice the one of the grid-side DC voltage control. Results are shown in Fig. 6.10. In this case, voltage variations during saturation are improved compared to the direct power reference compensation due to the equivalent doubled proportional gain and, consequently, the voltage deviation are reduced by this amplification ratio.

Nevertheless, although the voltage variations are mitigated, the DC-link voltage is not completely compensated and some deviations are still present. Note that since there is not integral action, the proportional gain shall be tuned in order to fulfill the maximum DC-link voltage deviation requirements.

Fourth simulation relies on the use of a PI controller for the auxiliary DC voltage control. The addition of an integral action eliminates any voltage deviation in steady state, so it is not necessary to increase the proportional gain in order to reduce the deviation. Therefore, both proportional and integral gains of the auxiliary DC voltage control take the same values of those for the grid-side DC voltage control, allowing to replicate the same dynamics. Results are shown in Fig. 6.11. Now, it can be observed that the integral action is being applied whenever the auxiliary DC voltage control is enabled, so that the DC-link voltage error is completely canceled.

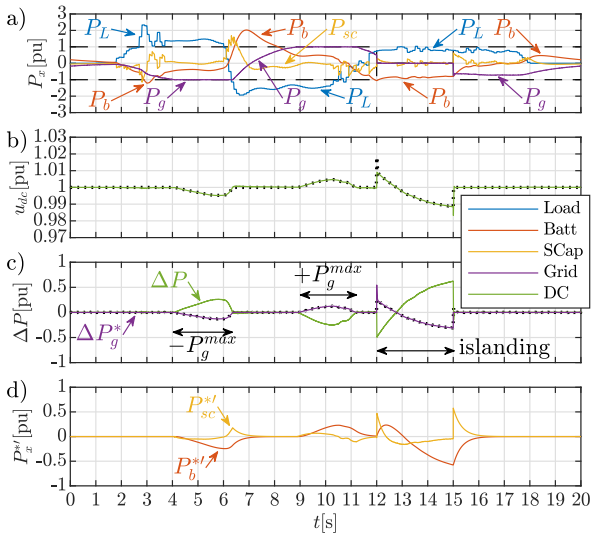

Figure 6.10: Simulation results: Auxiliary DC voltage control with P controller. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 6.9.

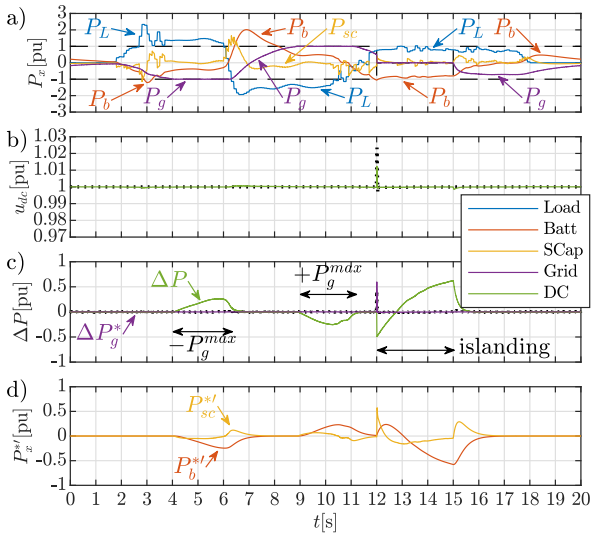

Figure 6.11: Simulation results: Auxiliary DC voltage control with PI controller. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 6.9.

6.4.4 Enhanced power reference compensation

In here, the enhanced reference compensation proposed in Subsection 6.3.3, both considering P and PI controllers, is taken into account.

Fifth simulation considers a proportional controller with a gain equal to 2. Results are shown in Fig. 6.12. As it can be seen, the results are similar to the ones obtained in Subsection 6.4.3 with the P controller (Fig. 6.10) since the DC-link voltage variations are practically the same. Note that the proportional gain in both cases has the same multiplication factor (2), which explains the similarities in their behavior. Nevertheless, the enhanced power reference compensation shall be chosen over the auxiliary DC voltage control since it is easier to implement.

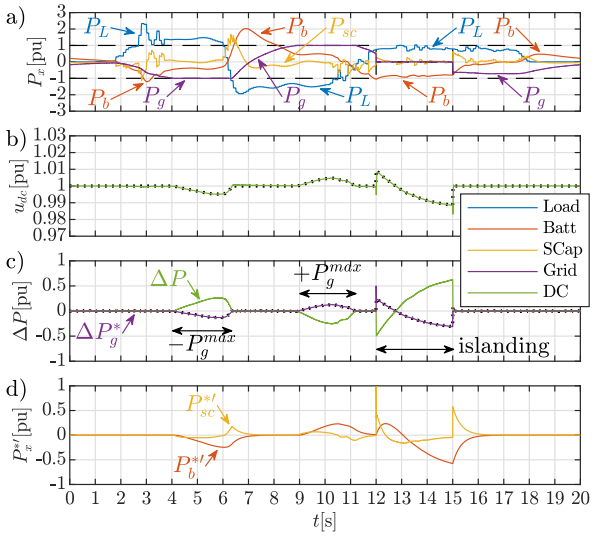

Figure 6.12: Simulation results: Enhanced power reference compensation with P controller. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 6.9.

Sixth simulation relies on the use of a PI controller for the enhanced power reference compensation. Results are shown in Fig. 6.13. The results are practically the same to the ones obtained in Subsection 6.4.3 with the PI controller (Fig. 6.11). However, when the system enters in islanding, the enhanced power reference compensation is able to maintain the DC-link voltage constant throughout the test, whereas the auxiliary DC voltage control suffers from a transient voltage deviation.

This is shown in detail in Fig. 6.14 and Fig. 6.15. As explained in Subsection 6.3.4, when grid power limit is suddenly reduced, remaining grid power (ΔP_g^*) instantaneously varies with a magnitude equivalent to the grid power reduction. Therefore, enhanced power reference compensation immediately reacts, generating an instantaneous extra power reference for the supercapacitor ($P_{sc}^{*\prime}$) to avoid voltage deviation. However, auxiliary DC voltage control depends on the DC bus capacitor dynamics when reacting, provoking a bandwidth-limited extra power reference for the supercapacitor and hence some voltage deviation.

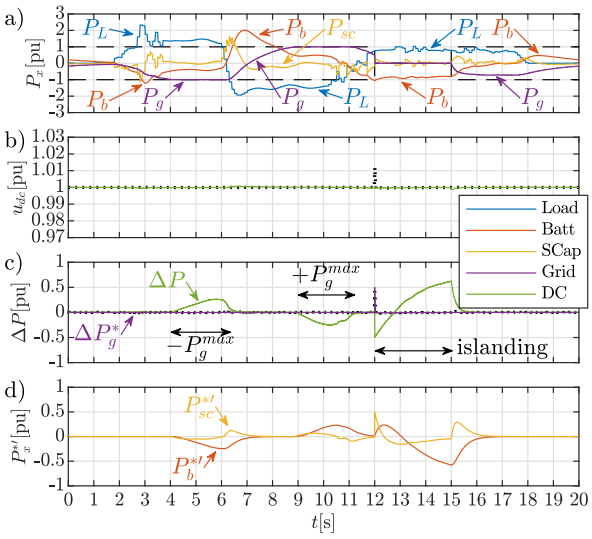

Figure 6.13: Simulation results: Enhanced power reference compensation with PI controller. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 6.9.

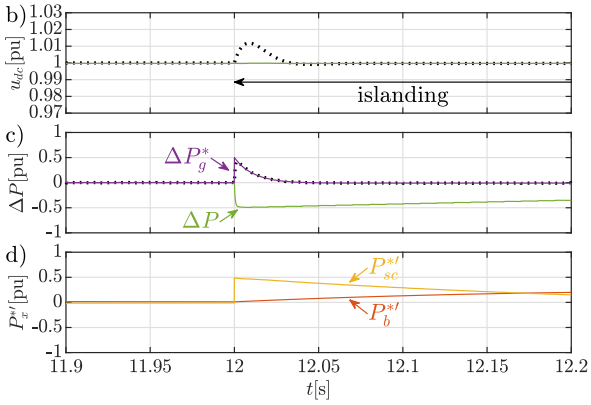

Figure 6.14: Detail of simulation results: Enhanced power reference compensation with PI controller when entering in islanding mode. b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 6.9.

6.4.5 Summary

An overview of the key results (maximum grid power, cumulative error, maximum error and DC voltage overshoot) for all the simulation cases is shown in Table 6.2. As it can be seen, in all the cases with compensation, the maximum grid power is within the expected limits.

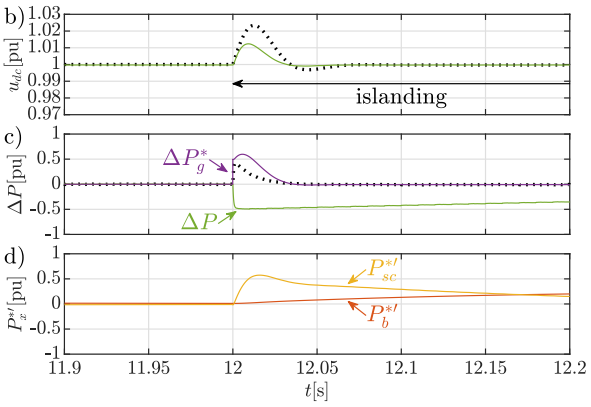

Figure 6.15: Detail of simulation results: Auxiliary DC voltage control with PI controller when entering in islanding mode. b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 6.9.

Table 6.2: Performance overview of the different simulation cases.

CASE	P_{grid}^{max} [pu]	$\int\lvert\text{error}\rvert$ u_{dc}[pu.s]	$\lvert\text{error}_{\max}\rvert$ u_{dc}[pu]	$\int\lvert\text{error}\rvert$ ΔP_g^*[pu.s]	$\lvert\text{error}_{\max}\rvert$ ΔP_g^*[pu]
A) Ideal grid	1.3	0.0029	0.0007	0	0
B) Direct pow	1.0	0.0686	0.0233	1.7869	0.6206
C1) Aux DC (P)	1.0	0.0353	0.0168	0.8945	0.5458
C2) Aux DC (PI)	1.0	0.0031	0.0124	0.0262	0.5972
D1) Enh pow (P)	1.0	0.0355	0.0168	0.8959	0.4999
D2) Enh pow (PI)	1.0	0.0030	0.0016	0.0239	0.4998

The direct power reference compensation is the worst method for all the metrics, followed by the auxiliary DC voltage control and the enhanced power reference compensation with P controller, whose cumulative errors are almost reduced by 2, since their equivalent proportional gain is twice the one for the direct power reference compensation. These compensation methods without integral action are able to reduce but not totally correct the power mismatch, as it can be seen by comparison with the ideal case.

The compensation methods including a PI controller have a better performance, since their cumulative errors are close to the ideal case. Particularly, the enhanced power reference compensation with PI controller gives the best results, providing a virtually perfect DC-link voltage regulation under saturation conditions. Therefore, the enhanced power reference compensation will be chosen over the auxiliary DC voltage control for the experimental validation.

The dotted lines from Figs. 6.8-6.13 show the theoretical model evolution of the DC-link voltage and the remaining grid power by using the simulated power mismatch

as input in the transfer functions, in order to compare them with the simulation results. As it can be seen, they virtually match except during large transients. The statistical analysis shown in Table 6.3 validates numerically these results, since both the mean and standard deviation of the modelling error are almost negligible.

Table 6.3: Statistical analysis (mean, standard deviation) of the error between theoretical model and simulation results.

CASE	mean u_{dc}[%]	SD u_{dc}[%]	mean ΔP_g^*[pu]	SD ΔP_g^*[pu]
B) Direct pow	0.0043	0.0301	0.1728	0.7079
C1) Aux DC (P)	0.0061	0.0439	0.1165	0.7809
C2) Aux DC (PI)	0.0076	0.0361	0.2068	0.9089
D1) Enh pow (P)	0.0061	0.0459	0.0775	0.4198
D2) Enh pow (PI)	0.0073	0.0325	0.1684	0.3561

Table 6.4 shows the total energy flowing through the different power devices, considering positive the energy that flows through the loads and negative the energy that flows through the sources (grid, battery and supercapacitor). By summing all these energies, the circulating energy is obtained. As shown in Table 6.4, the circulating energy is about 8 pu.s. Assuming an efficiency of 90% in the power converters, losses due to the circulating power are about 0.8 pu.s. Therefore, by comparing these losses with the energy needed by the load (about 17 pu.s), an increment of about 4.7% in the total energy is produced because of the circulating power. The authors consider that increment to be low compared to the benefits regarding the enhanced overall system stability and improved control margins.

Table 6.4: Total energy flowing through the different loads(+) and sources(−), and total circulating energy ($\sum$) in simulation results.

CASE	$+\int \lvert P_L \rvert$ [pu.s]	$-\int \lvert P_g \rvert$ [pu.s]	$-\int \lvert P_b \rvert$ [pu.s]	$-\int \lvert P_{sc} \rvert$ [pu.s]	$\sum \int \lvert P \rvert$ [pu.s]
A) Ideal grid	+17.04	−12.64	−9.91	−3.31	−8.82
B) Direct pow	+17.04	−10.85	−10.83	−3.39	−8.03
C1) Aux DC (P)	+17.05	−10.85	−10.84	−3.40	−8.04
C2) Aux DC (PI)	+17.04	−10.73	−10.92	−3.37	−7.99
D1) Enh pow (P)	+17.04	−10.85	−10.84	−3.40	−8.05
D2) Enh pow (PI)	+17.04	−10.73	−10.92	−3.37	−7.99

6.4.6 Effect of power measurement errors and communication delays

All simulations already performed in this section have considered ideal power measurements and no communication delays when sending power references to the ESS

(battery + supercapacitor). However, in a more realistic approach, errors in the sensors will distort the power measurements, and delays will affect the references sent from the central controller or the Power Sharing Compensator (PSC) to the battery and supercapacitor interface converters, as shown in Fig. 6.2. Therefore, additional simulations are conducted with the enhanced power reference compensation to test these phenomena.

Fig. 6.16 and Fig. 6.17 show the effect of having a 10% error in the grid power measurement, a 15% error in the battery power measurement and a 25% error in the supercapacitor measurement. Comparing these results to the ones with ideal sensor (Fig. 6.12 and Fig. 6.13), it can be seen that additional power mismatches appear in the system. In the case of using a P controller, the magnitude of the voltage deviation will be slightly amplified, but the DC-link voltage will remain almost constant in the case of using a PI controller.

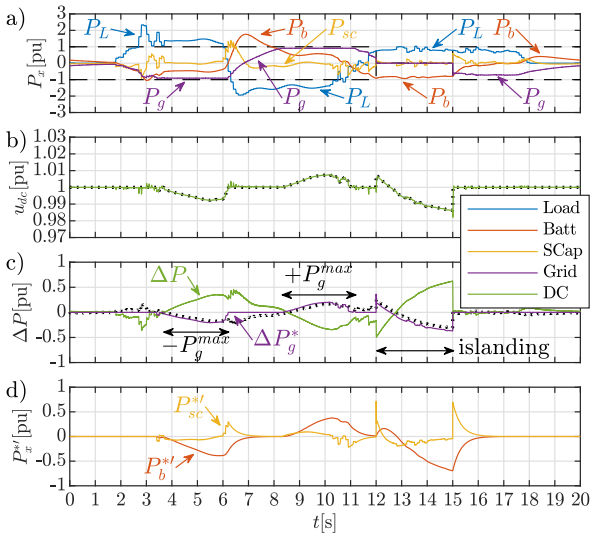

Figure 6.16: Simulation results: Enhanced power reference compensation with P controller with power measurement errors: grid, 10%; battery, 15%; supercapacitor, 25%. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 6.9.

Fig. 6.18, Fig. 6.19 and Fig. 6.20 show the effect of adding a communication delay of 2 ms, 5 ms and 10 ms when sending the power references to the battery and the supercapacitor. A communication delay of 2 ms (Fig. 6.18) does not provoke any noticeable change in the performance of the system, as can be shown by comparing it to the case with no delays (Fig. 6.13). However, a delay of 5 ms (Fig. 6.19) does affect the behavior of the system, deteriorating its performance, as can be seen in the deviation produced in the bus voltage when entering in islanding at 12 s. Finally, a delay of 10 ms (Fig. 6.20) makes the system unstable. Therefore, the maximum

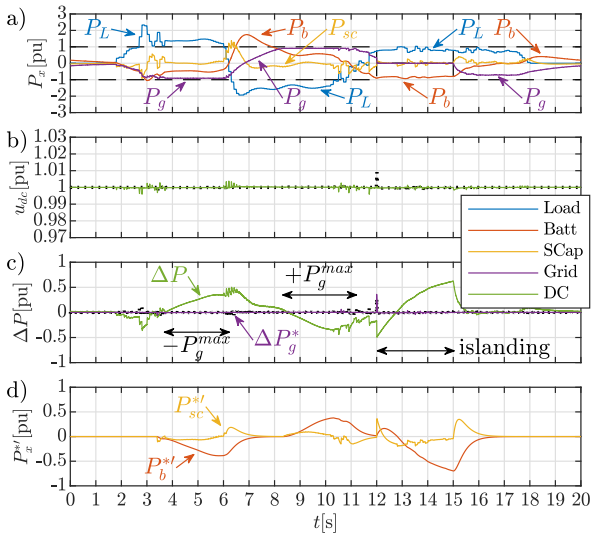

Figure 6.17: Simulation results: Enhanced power reference compensation with PI controller with power measurement errors: grid, 10%; battery, 15%; supercapacitor, 25%. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 6.9.

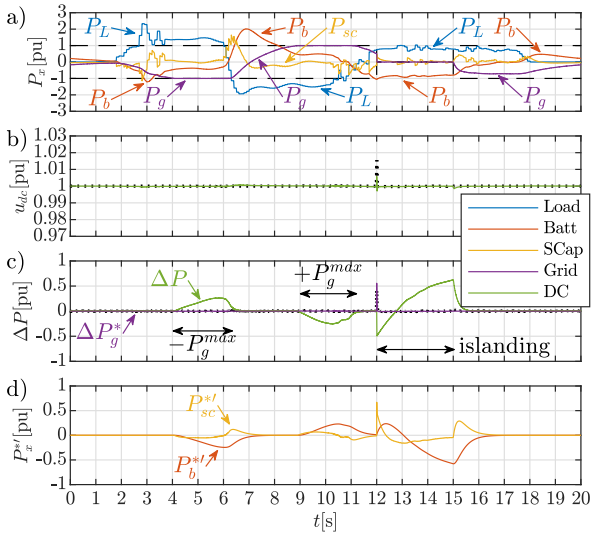

Figure 6.18: Simulation results: Enhanced power reference compensation with PI controller with a communication delay of 2 ms when sending power references to battery and supercapacitor. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 6.9.

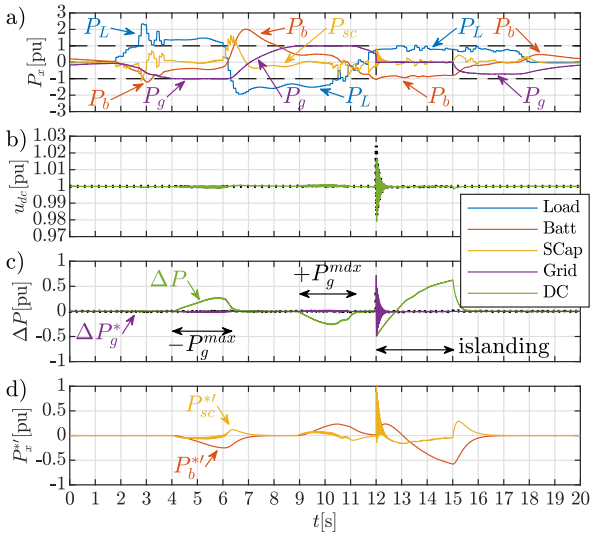

Figure 6.19: Simulation results: Enhanced power reference compensation with PI controller with a communication delay of 5 ms when sending power references to battery and supercapacitor. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 6.9.

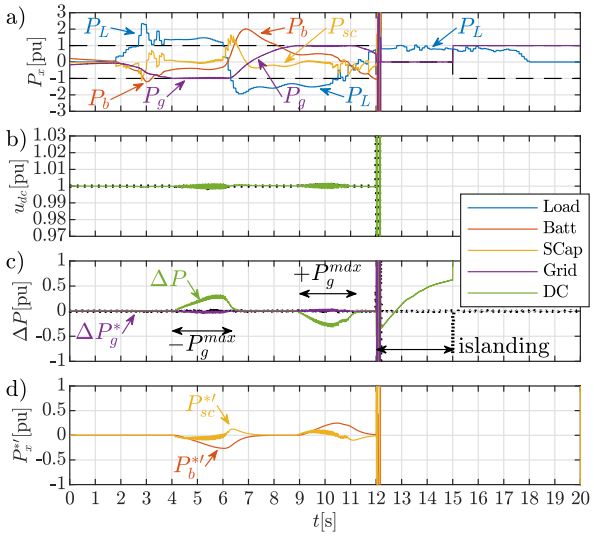

Figure 6.20: Simulation results: Enhanced power reference compensation with PI controller with a communication delay of 10 ms when sending power references to battery and supercapacitor. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 6.9.

communication delay can be up between 2 ms and 5 ms to not alter the performance of the system. The utilization of industrial communication networks (e.g. Modbus [6.32], CAN [6.33], Ethercat [6.34]...) within that delay range and a distributed control system execution period of $(10\ \text{kHz})^{-1} = 0.1$ ms (Table 6.1), 20 times faster than the maximum communication delay, guarantees a proper operation of the system.

6.5 Experimental results

Experimental validation is carried out using the setup shown in Fig. 6.21 for the different tests. The same load power profile and system parameters used in the simulation section are here considered.

The setup consists on two three-phase converters connected through the DC link (back-to-back) and two 4-wire 3-phase inductor filters, which allow the interconnection of the different power units: AC grid, battery, supercapacitor and bidirectional load. The parameters are listed in Table 6.1. The implementation of the control system is carried out by using two different control units: a Texas Instruments TMS320F28335 DSC at the distributed control system and a single-board computed (SBC) Raspberry Pi at the central control system.

Various experimental tests are carried out to demonstrate the suitability of the different compensation techniques and to address some problems that may appear during the real implementation: ideal grid, direct power reference compensation and enhanced power reference compensation.

First experimental test verifies the results shown in Section 6.2 (Fig. 6.4), in which grid power restrictions are applied without compensation. Results are shown in Fig. 6.22. As it can be seen, the DC-link voltage either drops to the rectifier level or rises to fault values when the grid power reach the limits.

Second experimental test is related to the simulation performed in Subsection 6.4.1, in which there is neither grid power restriction nor compensation. Results are shown in Fig. 6.23. As expected and in agreement with the simulation results, the DC-link voltage remains almost unchanged, while the grid power exceeds the considered power limit.

Third experimental test verifies the simulation conducted in Subsection 6.4.2, in which the direct power reference compensation is applied. Results are shown in Fig. 6.24. As it can be seen, the grid power is now limited to the maximum one. When the grid control reaches saturation, the DC-link voltage varies but its deviation is mitigated by applying some extra power via the energy storage system.

Fourth experimental test replicates the simulation in Subsection 6.4.4, in which the enhanced power reference compensation with a P controller is applied. Results are shown in Fig. 6.25. As expected, this compensation method improves the performance of the direct power reference compensation, with a reduction to a half in the DC-link voltage variations.

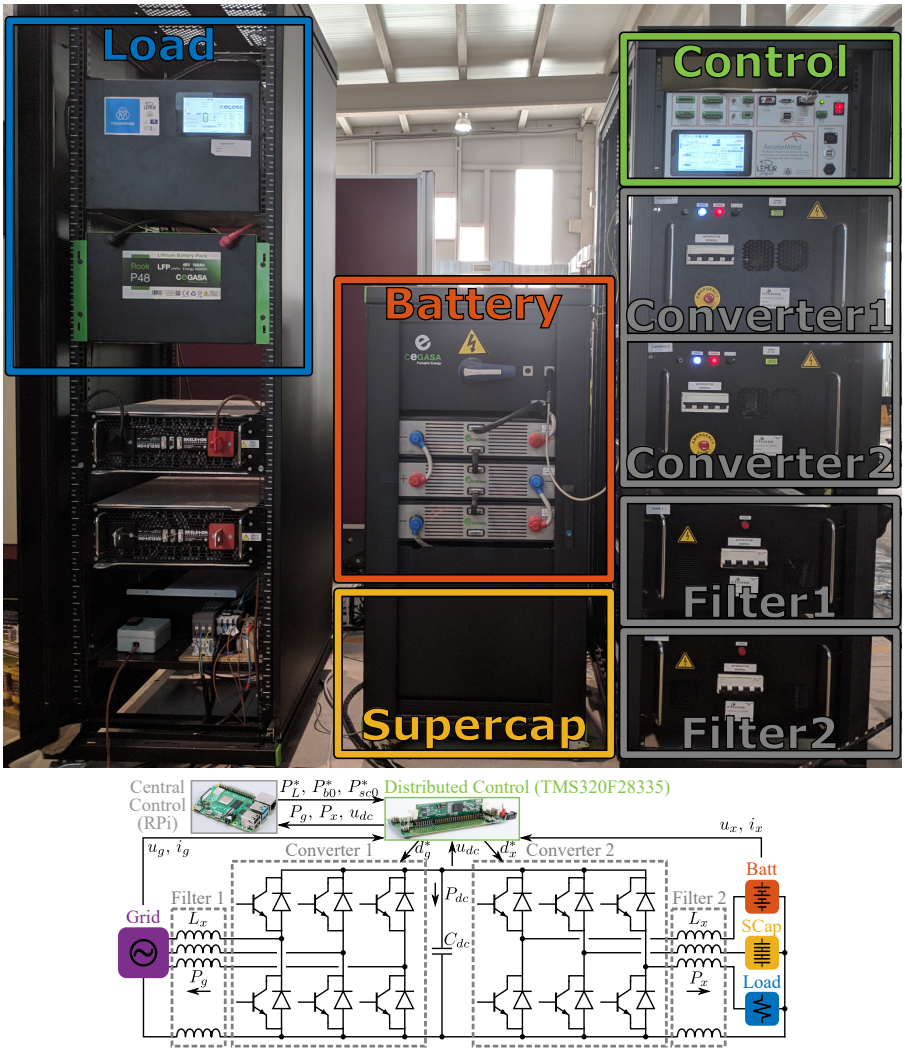

Figure 6.21: Experimental setup: Front side and electrical diagram.

Last experimental test follows the enhanced power reference compensation with a PI controller discussed in Subsection 6.4.4. Results are shown in Fig. 6.26. It is clear from the results that this compensation technique is the best one, since the DC-link voltage deviation is nearly zero, obtaining a result which is equivalent to the ideal case.

All the experimental tests show similar results (Table 6.5) to those of the simulation. Direct power reference compensation is the worst method for all the metrics, followed by enhanced power reference compensation with P controller, whose cumulative errors are almost reduced by 2, since their equivalent proportional gain is twice the one for the

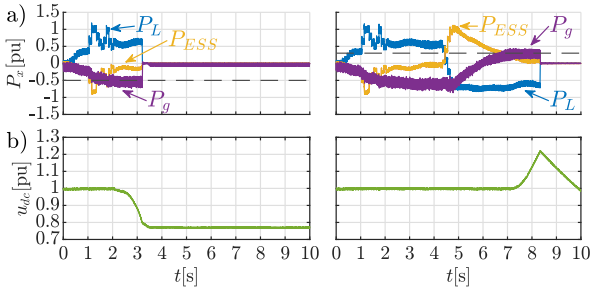

Figure 6.22: Experimental results: Power sharing issues when the grid power is limited (left, −0.5 pu; right, +0.3 pu). a) Power consumption; b) DC-link voltage. Color legend: blue, load; orange, ESS; purple, grid; green, DC bus. Dashed lines: grid power limits.

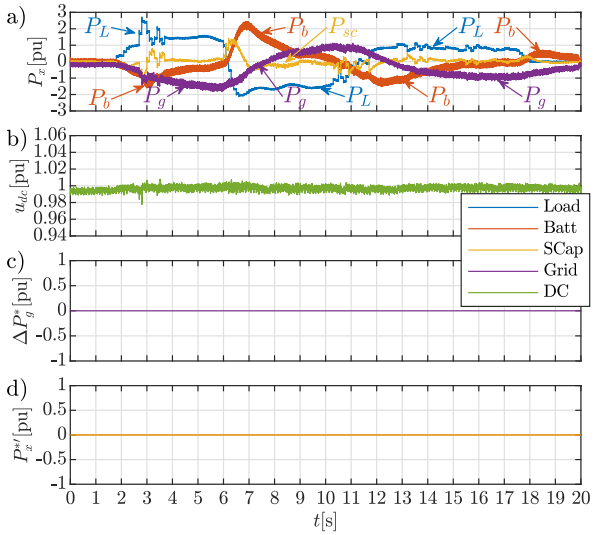

Figure 6.23: Experimental results: Ideal case. a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Extra power reference. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus. Dashed lines: grid power limits.

direct power reference compensation. Enhanced power reference compensation with PI controller gives the best results. Therefore, the feasibility of the real implementation of the power mismatch compensation techniques discussed throughout the chapter is demonstrated.

Table 6.6 shows the total energy flowing through the different power devices using the same sign convention than in the simulation results. Results are shown in Table 6.6. The circulating energy is about 9.5 pu.s. Assuming an efficiency of 90% in the power converters, losses due to the circulating power are about 0.95 pu.s. Therefore, by comparing these losses with the energy needed by the load (about 17.7 pu.s), an increment

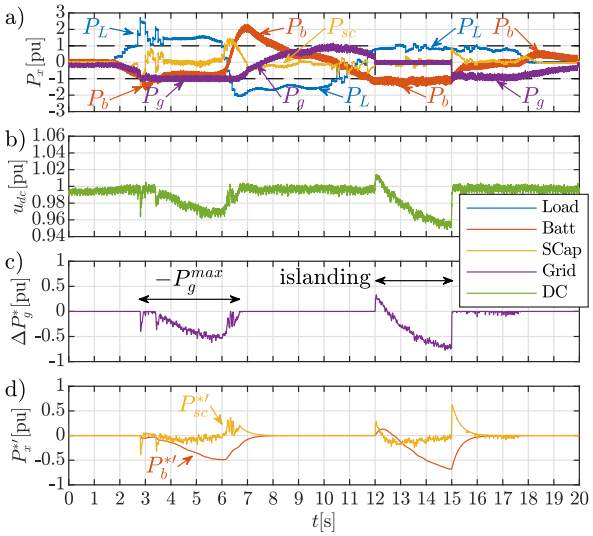

Figure 6.24: Experimental results: Direct power reference compensation. a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Extra power reference. Legend is the same as Fig. 6.23.

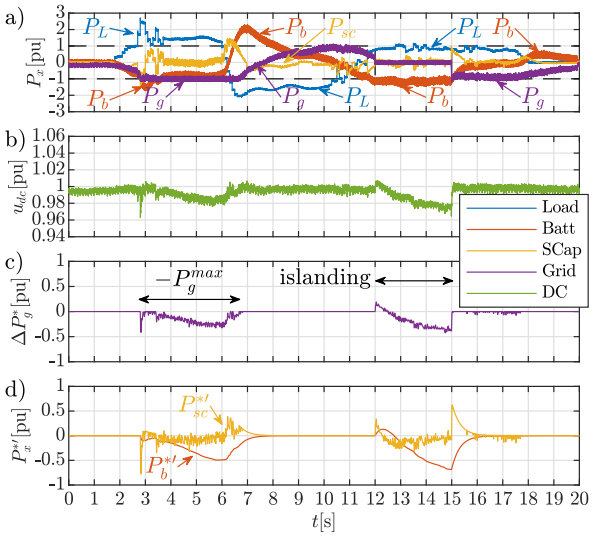

Figure 6.25: Experimental results: Enhanced power reference compensation with P controller. a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Extra power reference. Legend is the same as Fig. 6.23.

of about 5.4% in the total energy is produced because of the circulating power.

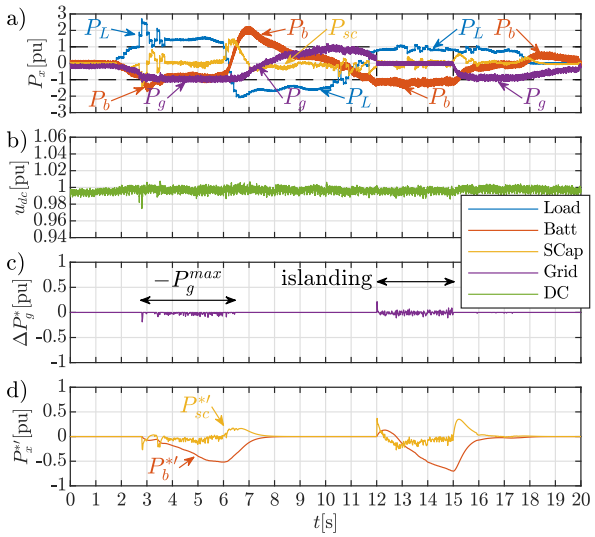

Figure 6.26: Experimental results: Enhanced power reference compensation with PI controller. a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Extra power reference. Legend is the same as Fig. 6.23.

Table 6.5: Performance overview of the different experimental tests.

CASE	P_{grid}^{max} [pu]	$\int\|\text{error}\|$ u_{dc}[pu.s]	$\|\text{error}_{\max}\|$ u_{dc}[pu]	$\int\|\text{error}\|$ ΔP_g^*[pu.s]	$\|\text{error}_{\max}\|$ ΔP_g^*[pu]
A) Ideal grid	1.6	0.0299	0.0081	0	0
B) Direct pow	1.0	0.1537	0.0440	2.4027	0.7715
D1) Enh pow (P)	1.0	0.0872	0.0254	1.2513	0.4244
D2) Enh pow (PI)	1.0	0.0299	0.0094	0.1444	0.2154

Table 6.6: Total energy flowing through the different loads(+) and sources(−), and total circulating energy ($\sum$) in experimental tests.

CASE	$+\int\|P_L\|$ [pu.s]	$-\int\|P_g\|$ [pu.s]	$-\int\|P_b\|$ [pu.s]	$-\int\|P_{sc}\|$ [pu.s]	$\sum\int\|P\|$ [pu.s]
A) Ideal grid	+17.70	−14.06	−10.87	−2.96	−10.19
B) Direct pow	+17.67	−11.45	−12.81	−2.94	−9.54
D1) Enh pow (P)	+17.66	−11.41	−12.88	−2.97	−9.59
D2) Enh pow (PI)	+17.66	−11.07	−13.05	−2.96	−9.43

6.6 Conclusions

This chapter has presented some compensation techniques of power sharing error affecting the DC-link voltage regulation in a multiport DC/DC/AC converter. The

proposed alternatives have been analytically discussed and firstly validated by numerical simulations, considering saturation events, transient behavior and operation under islanding mode. Among the presented alternatives, the enhanced power reference compensation with a PI controller shows the best trade-off between implementation complexity and performance. The proposed methods have been also validated by experimental results with a close match between the simulation and the real implementation.

Studied power mismatch compensation techniques are designed to be used regardless of the system nominal power, as shown in (6.22), (6.26), (6.27) and (6.30). Therefore, these compensation techniques can be applied to utility-scale power systems by resizing the power cells (iPEBBs) to withstand the required voltages and currents. Few tweaks will be needed in the proposed compensation methodology, regarding the voltage/current limits and the tuning of the control gains to adequate to the new values for the physical components.

Moreover, the influence of communication delays is critical on the system performance, making the system unstable if a certain threshold is exceeded. Future work for precisely characterizing these delays and analyzing different compensation techniques, such as the Smith predictor [6.35], to mitigate the influence of delays and improve the dynamic response of the system.

Lastly, it is worth mentioning that harmonics or unbalances in the grid would provoke undesired variations in the DC-link voltage introduced by the grid power control. In particular, unbalances in the grid will cause DC-link voltage variations at twice the fundamental frequency, whereas $6n \pm 1$ harmonics in the three-phase grid will induce $6n$ harmonics. These considerations are focus of future works.

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Chapter 7

Conclusions and future work

7.1 Conclusiones

Todo el trabajo realizado a largo del desarrollo de la tesis doctoral habilita al cumplimiento del objetivo principal de la tesis, que consiste en el modelado y diseño de un sistema de control distribuido basado en celdas de potencia adecuado para su implementación en convertidores de potencia multipuerto para la integración de recursos distribuidos.

Inicialmente, se plantea el modelado y análisis dinámico de una celda de potencia con inteligencia integrada, conocida como bloque de potencia inteligente. Para ello, se realiza el modelado del modelo promediado de señal grande en el espacio de estados de diferentes configuraciones que pueden ser formadas a partir del bloque de potencia. De esta manera, se consigue obtener el modelo genérico de un convertidor formado por un número arbitario de fases y el modelo genérico de un convertidor multipuerto formado por una combinación de topologías half-bridge, full-bridge y trifásica. La obtención de este modelo habilita el análisis dinámico del convertidor, permitiendo entender el comportamiento del convertidor en función de magnitudes impuestas por el resto del sistemas de potencia.

Posteriormente, se muestra el desarrollo del sistema de control distribuido para su implementación en convertidor basado en celdas de potencia. El diseño de los controladores distribuidos en la celdas de potencia es llevado a cabo con un enfoque versátil y genérico, de manera que las celdas de potencia sean capaces de realizar sus tareas de control independientemente de la naturaleza de la unidad de potencia que esté conectada a las mismas. El controlador central se diseña para llevar a cabo la gestión a nivel de sistema y aplicación del convertidor, configurándolo atendiendo a las diferentes unidades de potencia conectadas al convertidor multipuerto para determinar las referencias enviadas a los controladores distribuidos en todo momento, con el fin de obtener el comportamiento global deseado. La validez del sistema de control distribuido

para el manejo de un convertidor de potencia es confirmado mediante la ejecución de diversas simulaciones y tests experimentales.

A continuación, se expone el desarrollo de una plataforma digital sobre un microprocesador de propósito general, con el fin de integrar el controlador central del sistema de control distribuido para se ejecución tanto de tareas críticas de control con restricciones firmes de tiempo real como de tareas auxiliares de control que doten al controlador central de funcionalidades extendidas de supervisión, monitorización, registro de históricos e interfaces humano-máquina. Para ello, se propone la integración de un sistema operativo Linux embebido estándar junto con la extensión de tiempo real Xenomai, habilitando la ejecución de tareas críticas de alta prioridad con un comportamiento responsivo y determinista, y la ejecución de tareas auxiliares de baja prioridad con acceso a múltiples recursos y librerías ofrecidos por el sistema operativo. El correcto desempeño de la plataforma digital para la ejecución de tareas en tiempo real es demostrado ejecutando una tarea periódica de alta prioridad que computa un algoritmo matemático, validando la ejecución de tareas con restricciones firmes de tiempo real bajo la gestión del kernel Cobalt ofrecido por la extensión Xenomai.

Finalmente, se implementa el sistema de control distribuido para el control de un convertidor multipuerto conectado a red basado en celdas de potencia y encargado de integrar diversos recursos distribuidos. En esta aplicación particular se integran una carga bidireccional y un sistema híbrido de almacenamiento formado por una batería (unidad de energía) y un supercondensador (unidad de potencia). La red eléctrica principal a la que está conectado el convertidor impone restricciones en el intercambio de potencia, estableciéndose un flujo de potencia máximo entre convertidor y red que no debe ser sobrepasado. Por tanto, el sistema híbrido de almacenamiento es utilizado para suavizar el perfil de potencia transferida por la red a la hora de alimentar a la carga local. Para ello, se integra un algoritmo de reparto de potencia en el controlador central para maximiza las características de los dispositivos que forman parte del sistema híbrido de almacenamiento. La correcta operación del sistema cuando se alcanza la potencia máxima de red se garantiza mediante el desarrollo de varios métodos de compensación de errores en el reparto de potencia, de manera que el sistema sea capaz de funcionar en condiciones de saturación incluso en condiciones de aislamiento de red. El correcto desempeño de estos métodos de compensación es comprobado mediante diversas simulaciones y tests experimentales.

7.2 Conclusions

All the work done throughout the development of the doctoral thesis enables the fulfillment of the main objective of the thesis, which is the modeling and design of a distributed control system based on power cells suitable for implementation in multiport power converters for the integration of distributed resources.

Initially, the modeling and dynamic analysis of a power cell with integrated intelligence, known as intelligent power block, is proposed. For this purpose, the modeling of

the large signal averaged model in the state space of different configurations that can be formed from the power block is performed. In this way, it is possible to obtain the generic model of a converter formed by an arbitrary number of phases and the generic model of a multiport converter formed by a combination of half-bridge, full-bridge and three-phase topologies. Obtaining this model enables the dynamic analysis of the converter, allowing to understand the converter behavior as a function of magnitudes imposed by the rest of the power system.

Subsequently, the development of the distributed control system for its implementation in a power cell based converter is shown. The design of the distributed controllers in the power cells is carried out with a versatile and generic approach, so that the power cells are able to perform their control tasks regardless of the nature of the power unit that is connected to them. The central controller is designed to carry out the system and application level management of the converter, configuring it according to the different power units connected to the multiport converter to determine the references sent to the distributed controllers at all times, in order to obtain the desired global behavior. The validity of the distributed control system for the management of a power converter is confirmed by performing various simulations and experimental tests.

Next, the development of a digital platform on a general purpose microprocessor is presented, in order to integrate the central controller of the distributed control system for the execution of both critical control tasks with firm real-time constraints and auxiliary control tasks that provide the central controller with extended functionalities of supervision, monitoring, history logging and human-machine interfaces. For this purpose, we propose the integration of a standard embedded Linux operating system together with the Xenomai real-time extension, enabling the execution of high priority critical tasks with responsive and deterministic behavior, and the execution of low priority auxiliary tasks with access to multiple resources and libraries offered by the operating system. The correct performance of the digital platform for real-time task execution is demonstrated by executing a high-priority periodic task that computes a mathematical algorithm, validating the execution of tasks with firm real-time constraints under the management of the Cobalt kernel offered by the Xenomai extension.

Finally, the distributed control system is implemented for the control of a grid-connected multiport converter based on power cells and in charge of integrating several distributed resources. In this particular application, a bidirectional load and a hybrid storage system consisting of a battery (energy unit) and a supercapacitor (power unit) are integrated. The main electrical grid to which the converter is connected imposes restrictions on power exchange, establishing a maximum power flow between converter and grid that must not be exceeded. Therefore, the hybrid storage system is used to smooth the power profile transferred by the grid when feeding the local load. For this purpose, a power sharing algorithm is integrated in the central controller to maximize the characteristics of the devices that are part of the hybrid storage system. The correct operation of the system when the maximum grid power is reached is ensured by the development of several methods of power sharing error compensation, so that the

system is able to operate under saturation conditions even in grid islanding conditions. The correct performance of these compensation methods is verified through various simulations and experimental tests.

7.3 Future work

Derived from the knowledge acquired during the development of the thesis, future work can be carried out in the following lines of research:

- Construction of the power cell based on commercial solutions to carry out the physical implementation of the multiport converter in a modular way in order to integrate the final distributed control system solution. In this way, it would be possible to test the distributed control system with the real final implementation to validate its exploitation in industrial applications outside a laboratory environment.

- Improvements in the dynamic modeling of the different power cell configurations to consider the effect on the power converter behavior of the control loops integrated in the distributed control system. Taking into account that the final operation of the converter is conditioned by the performance of the implemented control loops, the introduction of the effect of these loops in the mathematical model would allow to determine the final model in the state space of the whole power and control system, in order to perform the dynamic analysis of the final system for reference tracking and disturbance rejection. This analysis would facilitate the development of more advanced control loops to improve system performance, such as model predictive control. Moreover, a non-ideal behavior for internal control loops could be considered to determine their effect on the final performance of the system.

- Extension of the distributed control system structure for power plant level applications. The development of the distributed control structure proposed in this thesis is intended for integration at the power converter level. However, such structure could be extended for its integration in applications operating at a power plant level, enabling a coordinated operation between different power plants and industrial facilities. The effect of delays inherent to the communications system becomes very relevant in these cases and must be conveniently studied, since the communications protocols for these applications may have a non-deterministic behavior and the physical layer usually covers long distances.

Appendix A

Journal publications

A.1 Compensation Alternatives for Power Sharing Mismatch in Multi-Port DC/DC/AC Converters

Compensation Alternatives for Power Sharing Mismatch in Multi-Port DC/DC/AC Converters

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***Abstract*—This paper proposes several alternatives for the compensation of power sharing errors in the coupling DC bus of multi-port DC/DC/AC converters. The case of study consists in a multi-port converter used for the interconnection of an AC grid-tied converter, a battery, a supercapacitor and a regenerative DC load. A distributed control system, where the central controller computes the load power sharing between the battery and the supercapacitor modules and local controllers for the power control at each converter port is implemented. The sharing mechanism requires a precise measurement or estimation for the required load and ports power. However, due to measurements errors or control actions deviations, the real power share can differ from the estimated one and hence a power mismatch is produced. Those mismatches are absorbed by the DC-link voltage, which is assumed to be controlled by the grid-tied converter. However, considering power restrictions in the grid-tied converter, the differences in the power sharing can compromise the system operation and stability. The paper includes an analytical study for the converter operation under saturation conditions and proposes three compensation methods which are compared by simulation and experimental results. The proposed methods allow for the stable operation of the system, even when large errors in the power sharing are considered.**

NOMENCLATURE

Acronyms

Batt	Batteries.
ESS	Energy storage system.
HPF	High-pass filter.
iPEBB	Intelligent Power Electronics Building Block.
LPF	Low-pass filter.
PSC	Power Sharing Compensator.
SCaps	Supercapacitors.

Subscripts

0	Initial value of a variable.
b	Battery variable.
dc	DC bus variable.
ESS	Energy storage system variable.
g	Grid variable.
L	Load variable.
sc	Supercapacitor variable.
x	Unspecified device variable.

Superscripts

$*$	Reference value (setpoint) of a variable.
$\prime$	Additional/extra value of a variable.

Variables

d	Duty cycle.
e_{dc}	DC voltage error.
f	Frequency.
i	Current.
K_i	Integral gain.
K_p	Proportional gain.
P	Power.
T_s	Sample period.
u	Voltage.
ΔP	Power mismatch.
ΔP_g	Remaining grid power.

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I. INTRODUCTION

LOCAL small-scale power systems are being developed to promote the introduction of renewable energies, since they are closely related to distributed generation unlike the conventional ones. The concept of microgrid appears in order to categorize this type of systems, which are evolving over time [1]. Microgrids usually have some energy storage units to support the renewable power generation, which is non-deterministic. Different kind of energy storage systems (ESS) can be installed, some of them being more dedicated to the energy needs (batteries), while others show their advantages in terms of power capability (supercapacitors) [2], [3]. In order to exploit the advantages of the different types of energy storage system, microgrids can use an hybrid implementation (e.g. batteries and supercapacitors), so that a flexible and reliable operation is achieved [4], [5].

Batteries have relatively high energy density but they are not suitable when suffering high variations of power. This is because the internal electrochemical reactions inside the battery produce a process of degradation [6], [7]. To face this problem, supplementary supercapacitors can be used since they work properly under high variations of power [8]–[10], though they have low energy density. Therefore, it is necessary to perform a power sharing between the battery-based ESS and the supercapacitor ones [11]–[16].

However, any error in the calculation of the power sharing produces a mismatch, which may disturb the system performance. Errors in the sensors, in the estimation of the power load or in the control actions of the converters often appear during the operation of a power system. Thus, the influence of these mismatches should be analyzed to determine the resultant effects on the system under control.

The analyzed case is a multi-port DC/DC/AC converter, as a simplification of a complete hybrid DC/AC microgrid, composed of a DC load, a battery and a supercapacitor. A schematic diagram, based on the concept of distributed intelligent Power Electronics Building Blocks (iPEBBs) [17], is shown in Fig. 1. As explained in [17], an iPEBB is a single-phase power cell (upper and lower power switches, parallel capacitor, and series inductor in mid-point) with built-in voltage and current sensors, and a digital control system which manages the power cell.

The power converters outputs are coupled to a DC bus. Additionally, an inverter is connected to exchange energy with the AC grid. Since the DC bus is the central element of the system and the common coupling point of all iPEBBs, the convention used in this paper considers positive any power (either demanded by a load or given by a source) provided as an output by the DC bus.

The objective of this paper is to analyze the power mismatch problem in the multi-port DC/DC/AC converter when grid power is limited and to propose several compensation alternatives. For this purpose, control of the DC-link voltage in saturation conditions is carried out. Some references can be found in literature targeting the specific analysis of DC-link voltage control under saturation conditions for the current control [18]–[21].

The main contribution of this paper is to propose different methods to compensate this power mismatch by directly using the information given by the DC-link voltage controller. This way, power mismatch is mitigated by the compensation methods without requiring the information from any of the sensors in the loads and sources connected to the DC bus. Operation in islanding mode is considered to demonstrate the robustness of the compensation techniques. Moreover, errors in sensors and communication delays are analyzed to validate the performance of the system.

The proposed target applications are hybrid microgrids or distribution systems in which multiple paths for the power flow could exist. In those applications, the limits for the power coming from the AC grid could lead to the very extreme situation in which there are DC-side loads with a power consumption (or generation) while the AC grid is disconnected. In those cases, the DC/AC converter is useless.

Regarding the standards, IEC 60038:2009 [22] states that low-voltage (LV) systems can withstand a steady-state voltage variation of ±10% in the supply terminals. CENELEC EN 50160:2010 [23] also specifies a ±10% magnitude variation to be accomplished 95% of the time of the week for LV systems, allowing normal rapid voltage changes of 5% and infrequent rapid voltage changes of 10%. ANSI C84.1-2016 [24] shows that normal voltage fluctuations do not normally exceed ±5% of the nominal value. IEEE Std 1159-2019 [25] does not consider variations within ±10% of the nominal voltage as electromagnetic phenomena, whereas IEEE Std 1250-2018 [26] defines a voltage regulation of ±5% in normal conditions. IEEE Std 1547-2018 [27] specifies voltage ride-through requirements for distributed energy resources (DERs) connected to electric power systems (EPSs), so that continuous operation has to be guaranteed if voltage range is from 0.88 to 1.1 pu. Therefore, the boundary of working conditions is a maximum variation of ±5% in the DC nominal voltage.

IEEE Std 2030.7-2017 [28] states that microgrids are capable to operate in islanding mode and supply local loads, but also connected to the grid at the point of interconnection (POI). Thus, to limit the maximum power to be exchanged depending on grid state, a grid power limit is established. Whilst a conventional AC/DC converter would be suitable to meet the maximum DC voltage variation during normal conditions, it is prone to fail whenever grid power limit is reached. This can happen either when it is required to limit the maximum power exchanged with the grid or to operate in islanding mode due to a controlled disconnection from the grid or a blackout. Therefore, the introduction of an ESS in the DC grid with a multi-port DC/DC/AC converter provides redundancy and thus improves the reliability of the DC grid, since local loads/sources can continue to operate regardless of the state of the main grid.

In addition, applications with regenerative electric motors or any DC-side generation may be suitable for this topology to limit the exchanged grid power. This way, fast power variations will be provided by the ESS whereas the grid only manages the base power and the energy demand to maintain the ESS conveniently charged, always guaranteeing that the total grid power is below the configured limit.

It has to be remarked that the proposals in this paper do not need for the additional installation of ESS units but despite it uses the elements already available in the hybrid DC/AC grid, by implementing a collaborative control between all of them.

In addition, the use of the same power cell (iPEBB) for all power converters reduces costs and facilitates maintenance, since the hardware is common and only its programming varies depending on the application. It would also facilitate the integration of new power units with a similar nominal power without having to design a new specific power stage, providing flexibility to the system when introducing new loads/sources, a common case in distributed generation systems. In addition, several iPEBBs could be parallel combined to enable power units with higher nominal powers, providing scalability to the system.

This research is mainly based on the contributions presented in [29]. Past work is extended by a meaningful theoretical

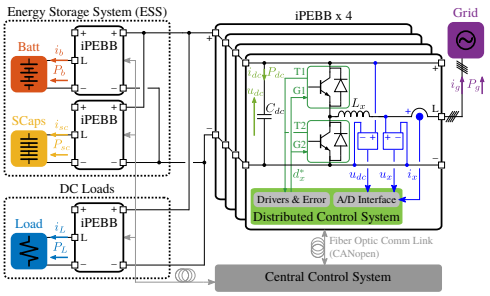

Fig. 1. Electrical diagram of the multi-port DC/DC/AC converter based on the use of intelligent Power Electronics Building Blocks (iPEBBs).

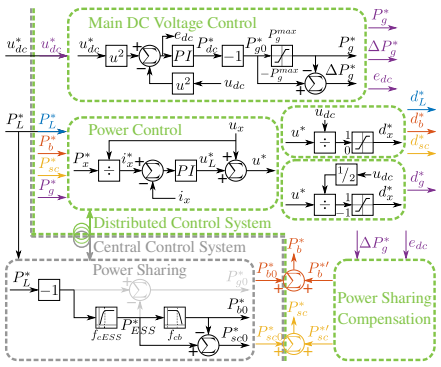

Fig. 2. Control diagram of the multi-port DC/DC/AC converter. Gray units are integrated in the central control system whereas green units are integrated in the distributed control units.

analysis of the system performance and compensation methods under saturation conditions derived from power limitations. New simulation and experimental results have been developed to consider islanding operation, thus demonstrating the robustness of the proposed control system under sudden AC grid disconnection. In addition, an analysis of the effect of power measurement (sensor) errors and communication delays in the performance of the compensation methods is performed.

This paper is organized as follows. In Section II, an explanation of the power sharing hurdles in the multi-port DC/DC/AC converter is introduced. In Section III, an analysis of the different compensation techniques for tackling the power sharing mismatch is discussed. In Section IV and Section V, simulation and experimental results are obtained for the control system validation. Finally, in Section VI, conclusions about the accomplished work are discussed.

II. Power Sharing Issues

The multi-port DC/DC/AC converter used in this work is made up of several power units interconnected through a dc-link capacitor. The considered units are an aggregated regenerative DC load, which represents the different loads connected to the DC grid; a Li-ion battery; a supercapacitor, and a grid-tied interlinking converter connected to the AC grid (Fig. 1). In order to supply the DC load, a power sharing between the different power converters is employed. Considering as the starting point an operational AC grid, the base load demand is provided by the AC connection, whereas the peak load demand is given by the ESS. Between the two available sources, the low frequency components are supplied by the battery (energy source) whereas the high frequency components are supplied by the supercapacitor (power source). By using two low-pass/high-pass filters with different cutoff frequencies, it is possible to tweak the power sharing as desired.

Fig. 2 shows the proposed control diagram to carry out the power sharing mechanism. The power sharing is computed by the central controller, which sends the power references (P^*_{x0}) to the power control of the different distributed control units, in order to manage the current/power of the different system power converters. This control system implementation requires to have an accurate measurement of the power by each of the converter units. However, sensor accuracy or saturation phenomena in the control action of any unit will induce differences in the real power sharing.

Focusing on the DC side of the multi-port converter (Fig. 1), the power balance expression which links the different power units (load: P_L, battery: P_b, supercapacitor: P_{sc}, grid: P_g and DC bus capacitor: P_{dc}) is given by (1).

$$P_L + P_b + P_{sc} + P_g + P_{dc} = 0 \tag{1}$$

As it can be seen in Fig. 2, the power in the DC bus capacitor is not directly controlled, being dependent on the power mismatch (ΔP) among the different controlled power units. From (1), it is possible to obtain the magnitude of the DC bus capacitor power as given by (2).

$$P_{dc} = -\Delta P = -\left(P_L + P_b + P_{sc} + P_g\right) \tag{2}$$

For this purpose, it is necessary to calculate the power handled by the different units of the system using the expressions (3)-(6).

$$P_L = u_L i_L \tag{3}$$

$$P_b = u_b i_b \tag{4}$$

$$P_{sc} = u_{sc} i_{sc} \tag{5}$$

$$P_g = u_{ga} i_{ga} + u_{gb} i_{gb} + u_{gc} i_{gc} \tag{6}$$

Therefore, if the power sharing is perfectly done, the power mismatch is zero and the DC grid is balanced. Whenever a power mismatch occurs, (2) is not longer equal to zero and the power surplus or shortage has to be delivered/absorbed by the DC bus capacitor in order to compensate for that difference, acting as a power buffer. The problem is that this variation of DC bus capacitor power because of the power mismatches produces variations in the DC-link voltage. These DC-link voltage deviations are undesirable and thus have to be kept under certain bounds in order to avoid the system to reach unstable conditions. The absolute minimum limit for the DC-link voltage is twice the peak value of the grid phase

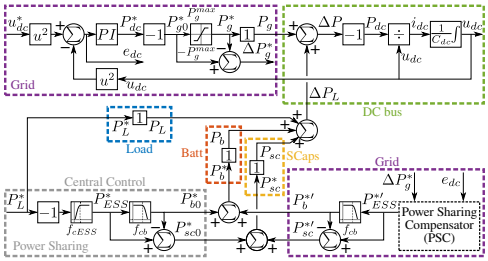

Fig. 3. Model of the multi-port DC/DC/AC converter with Power Sharing Compensator (PSC) from the point of view of the grid-side DC voltage control (ideal power control loops shown as unitary gain).

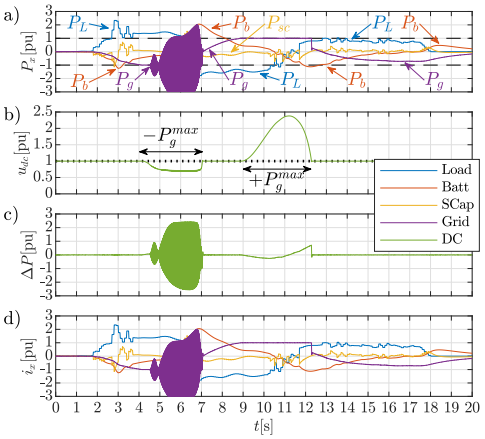

Fig. 4. Power sharing issues when the grid power is limited (±1 pu). a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Current comsumption. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus. Dashed lines: grid power limits.

voltage, since it is the minimum value needed to maintain the controllability of the system in inverter mode. The absolute maximum limit is determined by the maximum operating voltage of the power devices to not deteriorate them. In order to avoid the operation close to the absolute limits, a 5% margin is introduced in the actual limits.

As shown in Fig. 2, the grid-tied DC/AC inverter controls the DC-link voltage, so its variation will depend on the stiffness of its control system. Additionally, the variations induced in the DC-link voltage because of the power mismatch are also affected by the maximum power that can be managed by the grid-tied DC/AC converter ($\pm P_g^{max}$). Operation under saturation conditions in the delivered/absorbed power has still to guarantee an stable and stiff DC-link voltage.

Note that the addition of new unpredictable energy loads or sources would affect the power sharing of the system. Power produced/consumed by new sources/loads shall be estimated to be considered by the central controller algorithm to generate a modified ESS power reference. Nevertheless, if new load/source power could not be properly estimated due to its unpredictability, DC voltage control would provide the corresponding power mismatch.

Assuming that the power control of all the power units is accurate and much faster than the DC-link voltage control, the power control loops are considered ideal (unitary gain) from the point of view of the DC-link voltage control. This way, the system behavior can be modeled with the diagram shown in Fig. 3. There is a limitation in the minimum/maximum grid power, which is represented by a saturation block. If this limitation is reached, the applied grid power into the system ($P_g = P_g^*$) cannot match anymore the required power by the controller (P_{g0}^*). This way, the DC-link voltage control enters in saturation and loses the ability to properly maintain the DC-link voltage.

The aforementioned problems are following illustrated. Fig. 4 shows the power sharing issues which appear when the grid power is limited, so that saturation in the grid DC-link voltage controller is produced. In normal conditions, the grid provides the base load demand, whereas short-term power variations are provided by the ESS and the DC bus, trying to keep grid power dynamics as slow as possible to not disturb the grid. Since the DC-link voltage is controlled by the grid converter, power mismatches are also supplied by the grid-side converter. When the grid power reaches the minimum/maximum limit, the DC-link voltage either drops to the rectifier level or rises to fault values.

Constant power loads are commonly used to validate the robustness of voltage control algorithms, since they put the system in a worst-case scenario. For the evaluation of the system dynamics, a bidirectional electronic load able to generate rich time-varying profiles, either as a constant power or constant current load is used. The underpinning idea is to emulate the behaviour of high performance electrical drives.

At 4.1 s, the DC-link voltage starts dropping because of grid power reaching the minimum limit and thus the DC-link voltage control is saturated. At 4.5 s, the DC-link voltage reaches 400 V (0.8889 pu), which is twice the peak value of the grid phase voltage (200 V) and the minimum value that guarantees a stable system operation. Operation under that limit causes system instability when the DC/AC converter work in inverter mode delivering power to the grid, hence the shown oscillating behavior of the grid power. At 7 s, the DC-link voltage raises above the minimum limit, resulting in the system to be stabilized. From 9 s to 12 s, the DC-link voltage starts increasing because the grid power reaching the maximum limit and the DC-link voltage control being also saturated. In this event, the DC-link voltage reaches values greater than twice the nominal value (2.38 pu), which can deteriorate the power devices. This way, the system operation is compromised and correction actions are required to take back DC-link voltage within safe values.

In order to solve this problem, it is necessary to dynamically correct power mismatches to ensure a suitable operation. Considering that power mismatches are normally a transient problem, often with fast dynamics, this paper proposes several

alternative compensation methods relaying on a modified operation of the ESS.

A new control module called Power Sharing Compensator (PSC) is introduced into the control diagram (Fig. 2 and Fig. 3) with a view to performing the power sharing compensation. Extra power references ($P_x^{*\prime}$) are computed by this module and commanded together with the initial power references (P_{x0}^*) to the power control loops. Since it is required to compensate the power mismatches rapidly, the power sharing compensation is internally performed by each distributed control unit.

III. Compensation techniques

As mentioned above, power mismatches in the power sharing produce a deviation of the DC-link voltage from the nominal value. Thus, some kind of correction has to be applied to mitigate the problem. Three different compensation techniques are proposed: 1) direct power reference compensation, 2) auxiliary DC voltage control and 3) enhanced power reference compensation.

The challenge in the compensation is to properly estimate the power mismatch. Ideally, it could be determined by measuring the power in all system units and computing the summation, as shown in (2)-(6). However, this requires good accuracy in all current/voltage sensors of the system and does not allow the addition of new power units that do not provide any feedback of the power consumption.

Alternatively, an estimation method for the compensation power can be done by analyzing the shape of the grid DC-link voltage controller. The grid-side DC voltage control is controlled by the grid-tied converter using a quadratic voltage control (QVC) [30] as shown in Fig. 2 and Fig. 3, so that the control action is expressed in terms of power. If saturation in the grid-tied converter is produced, the controller will not longer be able to apply the required power. The remaining grid power (ΔP_g^*) can be considered as the required extra power to counteract the power mismatch. This way, good accuracy is only required in the current/voltage sensors of the grid power units to compute the power mismatch, reducing the number of elements that can introduce errors in its calculation.

In order to determine the options to compensate this power mismatch, the control law of the discrete QVC based on a PI controller is discussed. Observing the system model (Fig. 3) and for a given proportional gain (K_p), integral gain (K_i) and sample period (T_s), the expression (ideal form) to calculate the control action (u) of the controller depending on the error (e) at any sample k is given by (7)-(9).

$$e_k = e_{dc} = \left(u_{dc}^*\right)^2 - \left(u_{dc}\right)^2 \tag{7}$$

$$u_k = u_k^0 = \underbrace{K_p e_k}_{\text{P action}} + \underbrace{K_p\left(K_i T_s - 1\right) e_{k-1} + u_{k-1}}_{\text{Integral action}} = P_{dc}^* \tag{8}$$

$$P_{g0}^* = -P_{dc}^* = -u_k;\ P_g^* = \mathrm{sat}(P_{g0}^*);\ \Delta P_g^* = P_{g0}^* - P_g^* \tag{9}$$

Since the implemented controller provides integral action, an anti-windup mechanism that limits this action during saturation is required. In this case, the realizable references method is used due to its performance and simplicity in discrete systems [31] when the controller has the same number of poles than zeros. Considering a discrete PI controller implemented

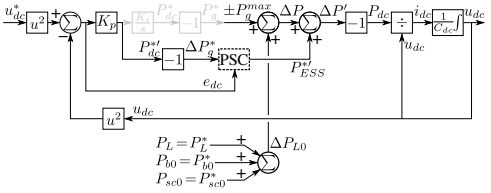

Fig. 5. Simplified model under saturation conditions of the multi-port DC/DC/AC converter with DC-link voltage control carried out by the grid and the Power Sharing Compensator (PSC).

by the bilinear approximation, the calculations performed by the anti-windup method during saturation conditions to correct the actual control action (u_k) and error (e_k) with realizable values (u_k^r, e_k^r) for the next iteration (u_{k+1}, e_{k+1}) are given by (10) and (11) respectively.

$$u_k^r = -P_g^* = -\mathrm{sat}(-u_k);\ u_{k+1} = u_k^r \tag{10}$$

$$e_k^r = \frac{u_k^r - K_p\left(K_i T_s - 1\right) e_{k-1} - u_{k-1}}{K_p};\ e_{k+1} = e_k^r \tag{11}$$

This way, when the DC-link voltage reaches steady state ($u_{dc} \approx u_{dc}^*$, $e_k \approx 0$, $e_{k-1} \approx 0$), the controller only applies the integral action. Once the system enters into saturation, the grid converter power is limited and the anti-windup mechanism starts actuating by limiting the integral action. If saturation is kept at least during two samples periods, both the previous (u_{k-1}) and the realizable action control (u_k^r) take the limited minimum/maximum value. This way, (11) can be simplified into the expression given by (12).

$$e_k^r = \left(1 - K_i T_s\right) e_{k-1};\ e_{k+1} = e_k^r \tag{12}$$

Assuming that $|1 - K_i T_s| < 1$, the realizable error (e_k^r) and hence the previous error (e_{k-1}) will converge to zero. In this case, from (7)-(10), it is possible to obtain the expression which defines the remaining grid power, as shown in (13) and (14).

$$\Delta P_g^* = -\left(u_k^0 - u_k^r\right) = -\left(u_k^0 - u_{k-1}\right) \tag{13}$$

$$\Delta P_g^* = -K_p e_{dc} = -K_p\left(\left(u_{dc}^*(t)\right)^2 - \left(u_{dc}(t)\right)^2\right) \tag{14}$$

Therefore, the applied grid power by the converter (P_g^*) will be dominated by the limited integral action ($\pm P_g^{max}$) whereas the remaining grid power (ΔP_g^*) will be dominated by the proportional action which is not provided by the converter due to saturation. Taking all of this into account, the model in Fig. 3 can be simplified under saturation conditions, so that the model shown in Fig. 5 is obtained.

Since the applied grid power is limited during saturation, the power mismatch (ΔP) is no longer zero and a disturbance of the DC-link voltage is produced. Extra power has to be introduced into the system in order to minimize the mismatch, obtaining a corrected power mismatch ($\Delta P'$) as close as possible to zero and hence reducing the DC-link voltage deviation.

Analyzing the simplified model for saturation (Fig. 5), a expression which relates the different variables of the system,

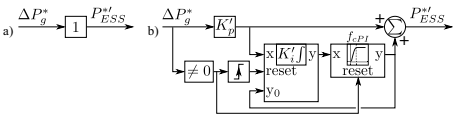

Fig. 6. Model of Power Sharing Compensator (PSC): direct (a) and enhanced (b) power reference compensation.

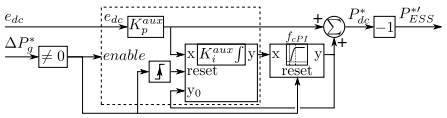

Fig. 7. Model of Power Sharing Compensator (PSC): auxiliary DC voltage control.

including the Power Sharing Compensator (PSC), in the forward path is calculated, as given by (15).

$$\Delta P(t) + \underbrace{PSC \cdot \Delta P_g^*(t)}_{P_{ESS}^{*\prime}} + C_{dc} \cdot u_{dc}(t) \frac{\mathrm{d}u_{dc}(t)}{\mathrm{d}t} = 0 \quad (15)$$

If (14) and (15) are combined and then linearized for the equilibrium point (U_{dc0}, U_{dc0}^*, $\Delta P_g^* = 0$, $\Delta P = 0$) by using Taylor series [30], the expressions in (16) and (17) are obtained.

$$\left(s\frac{C_{dc}}{2K_p} + PSC\right)\Delta P_g^*(s) + (sC_{dc})\, U_{dc0}^* \Delta u_{dc}^*(s) = -\Delta P(s) \quad (16)$$

$$(sC_{dc} + 2K_p PSC)\, U_{dc0} \Delta u_{dc}(s) - (2K_p PSC)\, U_{dc0}^* \Delta u_{dc}^*(s) = -\Delta P(s) \quad (17)$$

Assuming that the DC-link voltage reference does not vary ($\Delta u_{dc}^* = 0$, fixed DC-link voltage), it is possible to obtain from (16) and (17) the transfer functions which define the model of the system, as given by (18)-(20).

$$\frac{\Delta P_g^*(s)}{\Delta P(s)} = \frac{-2K_p}{sC_{dc} + 2K_p PSC} \quad (18)$$

$$\frac{\Delta u_{dc}(s)}{\Delta P(s)} = \frac{-1/U_{dc0}}{sC_{dc} + 2K_p PSC} \quad (19)$$

$$\frac{\Delta u_{dc}(s)}{\Delta P_g^*(s)} = \frac{1}{2K_p U_{dc0}} \quad (20)$$

As it can be seen, the evolution of both the remaining grid power (ΔP_g^*) and the DC-link voltage deviation (Δu_{dc}) depends on the structure of the PSC, whereas the ratio between both variables is constant regardless of the PSC. Therefore, the PSC is able to mitigate them, so different alternatives for the PSC will be discussed below in order to analyze their performance.

A. Direct power reference compensation

The first compensation technique consists of tracking the remaining grid power ($\Delta P_g^* = -K_p\left(u_{dc}^*(t)^2 - u_{dc}(t)^2\right)$) and delivering an extra power with the same value, as shown in Fig. 6a. In this case, the PSC is simply a unitary gain.

This extra power will be provided by the ESS ($P_{ESS}^{*\prime}$) since the grid-tied converter is working under saturation conditions, as shown in Fig. 5. A low-pass filter is used to determine the battery and supercapacitor references ($P_b^{*\prime}$ and $P_{sc}^{*\prime}$).

The performance of the direct power reference compensation can be determined by computing (18) and (19) for the particular case of $PSC = 1$, obtaining the transfer functions shown in (21).

$$\frac{\Delta P_g^*(s)}{\Delta P(s)} = \frac{-2K_p}{sC_{dc} + 2K_p};\ \frac{\Delta u_{dc}(s)}{\Delta P(s)} = \frac{-1/U_{dc0}}{sC_{dc} + 2K_p} \quad (21)$$

The resultant transfer functions correspond to first order systems and hence there is not overshoot in the evolution of the remaining grid power and the DC-link voltage. Then, the maximum deviation of both variables (ΔP_g^{*max}, Δu_{dc}^{max}) can be obtained with the maximum power mismatch ($|\Delta P^{max}|$) via the DC gain ($\lim_{s\to 0}$) of the transfer functions in (21), whose expressions are given by (22).

$$\Delta P_g^{*max} = |\Delta P^{max}|;\ \Delta u_{dc}^{max} = \frac{|\Delta P^{max}|}{2K_p U_{dc0}} \quad (22)$$

As it can be seen, the variations of both the remaining grid power and the DC-link voltage are not fully mitigated in the direct power reference compensation, so the power mismatch (ΔP) is not totally compensated. Following, alternative compensation techniques are discussed in order to improve the PSC performance.

B. Auxiliary DC voltage control

The second compensation technique consists on an auxiliary DC voltage control in the ESS to support the grid-side DC voltage control during saturation events. The proposed scheme is shown in Fig. 7. Under normal conditions, only the grid-side DC voltage control has to be active. Therefore, an enabling strategy which triggers the auxiliary DC voltage control needs to be considered. The enabling strategy is similar to the one applied for the direct power reference compensation. The power mismatch resulting from the saturation condition in the grid-side DC voltage control provokes a non-zero remaining grid power ($\Delta P_g^* \neq 0$), which is used as the trigger event.

Same sharing method than the one in Subsection III-A is used for the computation of the extra reference of the battery ($P_b^{*\prime}$) and the supercapacitor ($P_{sc}^{*\prime}$).

Two different controller implementations will be studied for this compensation technique: P and PI controller. If zero steady-state errors are not required in the voltage value during the saturation event, a P controller is valid.

Unlike the direct power reference compensation, the input of the auxiliary DC voltage control is the error (e_{dc}) instead of the remaining grid power (ΔP_g^*). Thus, this compensation technique is not affected by the proportional gain of the grid-side DC voltage control (K_p). The corresponding PSC transfer function has to be computed in order to compare its performance with the previous method. Considering the transfer function of a PI controller in ideal form ($C(s) =$

$K_p^{aux} + K_p^{aux}K_i^{aux}/s$), the equivalent PSC is given by (23) and the corresponding transfer functions by (24) and (25).

$$PSC^{aux} = \frac{1}{K_p}\left(K_p^{aux} + \frac{K_p^{aux}K_i^{aux}}{s}\right) \quad (23)$$

$$\frac{\Delta P_g^*(s)}{\Delta P(s)} = \frac{-s2K_p}{s^2C_{dc} + s2K_p^{aux} + 2K_p^{aux}K_i^{aux}} \quad (24)$$

$$\frac{\Delta u_{dc}(s)}{\Delta P(s)} = \frac{-s/U_{dc0}}{s^2C_{dc} + s2K_p^{aux} + 2K_p^{aux}K_i^{aux}} \quad (25)$$

In the particular case of a pure proportional controller ($K_i^{aux} = 0$), it is possible to calculate from (25) the optimal auxiliary proportional gain (K_p^{auxP}) depending on the desired maximum voltage deviation (Δu_{dc}^{max}) and the maximum power mismatch ($|\Delta P^{max}|$), with the expression given by (26).

$$K_p^{auxP} = \frac{|\Delta P^{max}|}{2U_{dc0}\Delta u_{dc}^{max}} \quad (26)$$

When a PI controller is used instead, the gains are selected to mimic the behavior of the grid-side DC voltage controller. Therefore, both the auxiliary proportional gain (K_p^{auxPI}) and the auxiliary integral gain (K_i^{auxPI}) are made equal to the original proportional and integral gains (K_p, K_i), as stated by (27).

$$K_p^{auxPI} = K_p;\ K_i^{auxPI} = K_i \quad (27)$$

Additionally, since the auxiliary DC voltage control is only required to work during saturation events, the effect of the integral action after the transient recovering has to be removed. This way, steady-state contribution of the battery power ($P_b^{*\prime}$) is avoided, thus improving its life usage. For that, a resettable high-pass filter (HPF) is placed in the output of the integrator, as shown in Fig. 7. This way, the HPF avoids steady-state contribution of the ESS in normal conditions, but it is bypassed (forced activation of reset) during the saturation condition in the DC voltage control ($\Delta P_g^* \neq 0$). In addition, it has to be remarked that, in order to avoid inconsistency between the value applied to the ESS by the HPF and the dictated integrator output value whenever saturation appears, it is necessary to modify the integrator state to be initialized with the HPF output value each time the saturation condition is reached.

C. Enhanced power reference compensation

As shown in the expressions given by (21) and (22), an increment in the proportional gain induces a reduction in the voltage deviation. Therefore, it is possible to implement an enhanced power reference compensation by managing the remaining grid power (ΔP_g^*) through an extra proportional gain (K_p'), which amplifies the effect of the original proportional gain of the grid-side DC voltage control (K_p). An extra integral action (K_i') can also be added to completely eliminate the voltage deviation in steady state. According to that, an enhanced power reference compensation is proposed, as shown in Fig. 6b. As it can be seen in Fig. 6b, same sharing method than the one in Subsection III-A is used for the computation of the extra battery and supercapacitor references.

From (18) and (19), making a similar analysis to the one in Subsection III-B with $PSC = K_p' + K_p'K_i'/s$, it is possible to obtain the transfer functions in (28) and (29), and the optimal extra proportional gain for a P controller ($K_p'^P$) and the extra proportional ($K_p'^{PI}$) and integral ($K_i'^{PI}$) gain for a PI controller in (30).

$$\frac{\Delta P_g^*(s)}{\Delta P(s)} = \frac{-s2K_p}{s^2C_{dc} + s2K_pK_p' + 2K_pK_p'K_i'} \quad (28)$$

$$\frac{\Delta u_{dc}(s)}{\Delta P(s)} = \frac{-s/U_{dc0}}{s^2C_{dc} + s2K_pK_p' + 2K_pK_p'K_i'} \quad (29)$$

$$K_p'^P = \frac{|\Delta P^{max}|}{2K_pU_{dc0}\Delta u_{dc}^{max}};\ K_p'^{PI} = 1;\ K_i'^{PI} = K_i \quad (30)$$

Also as stated in Subsection III-B, an additional high-pass filter can be put in the output of the controller, as shown in Fig. 6b, for avoiding any steady-state contribution of the PSC when system recovers from saturation.

D. Operation in islanding mode

All the analysis carried out so far in this section assumes an operating point in which the minimum/maximum grid power is varied with slower dynamics compared to the internal converter control, which is the case for normal system operation. However, in the event of grid disconnection, the system has to immediately enter in islanding mode. For that, the grid power limit (P_g^{max}) has to be reduced to 0. Fig. 3 shows that this will suddenly force zero grid power reference (P_g^*), creating a power mismatch (ΔP) that has to be dealt by the different compensation techniques.

Direct and enhanced power reference compensation control the remaining grid power (ΔP_g^*), while auxiliary DC voltage control manages the voltage error (e_{dc}). By looking at Fig. 3, the effect of a sudden reduction in the grid power (P_g^*) on the control variables can be determined.

In the case of using the remaining grid power (ΔP_g^*), a sudden reduction in the grid power limit would have a direct effect on it, as shown in the expression given by (31).

$$\Delta P_g^*(t) = P_{g0}^*(t) - P_g^*(t) \quad (31)$$

In the case of the voltage error (e_{dc}), the reaction is indirectly coupled through the DC-link voltage dynamics. This is shown in (32).

$$\Delta P(t) + C_{dc}u_{dc}(t)\frac{\mathrm{d}u_{dc}(t)}{\mathrm{d}t} = 0;\ e_{dc} = u_{dc}^{*2}(t) - u_{dc}^2(t) \quad (32)$$

Therefore, auxiliary DC voltage control has a certain delay in acting in the event of a sudden reduction in the grid power limit when entering islanding mode, whereas direct and enhanced power reference compensations react immediately.

E. Summary

Comparing the expressions which define the behavior of the different compensation techniques, (24), (25), (28) and (29), an equivalent behavior can be observed between the auxiliary DC voltage control and the enhanced power reference compensation. Nevertheless, controller gain selection is a

little more straightforward in the enhanced power reference compensation since it does not depend on the proportional gain of the main DC voltage controller (K_p), as shown in (26), (27) and (30). In any case, either of the two methods could be used indistinctly in a first approximation.

However, as discussed in Subsection III-D, since the control variable is not the same for both compensation techniques (voltage error e_{dc} vs remaining grid power ΔP_g^*), auxiliary DC voltage control would respond more slowly to the islanding mode condition. Due to this, the preferred compensation technique is the enhanced power reference compensation. This statement will be validated via simulations to certify the better performance of the enhanced power reference compensation during islanding operation.

Regarding the choice of a purely proportional controller or a PI controller, the latter allows to eliminate any voltage deviation in steady state. However, the implementation of the PI controller adds additional complexity to the system, since it requires a resettable integrator and high-pass filter, whereas only a simple gain is needed for the P controller. In the P controller options, the memory footprint is 2 floating variables (8 bytes) whereas the number of operations is 1 read, 1 multiplication and 1 write. Considering the PI controller alternatives, the memory footprint is 11 floating and 2 boolean variables (46 bytes) whereas the number of operations is 15 reads, 5 multiplications, 4 sums, 2 boolean comparisons and 10 writes.

Note that the power mismatch compensation is an extra addition to an already functional control in the iPEBB, which consists of power and DC voltage control loops in the case of the grid-side power branches, with all the communication protocol also integrated. Thus, since the digital signal processor of the iPEBB is optimized to reduce costs, both options (with P and PI controllers) are offered for cases where the digital processor is close to its limits. Both P and PI controllers will be tested during the simulations and experimental tests to determine their performance.

IV. Simulation results

Several simulations for the validation of the proposed compensation techniques are carried out in MATLAB/Simulink with the parameters described in Table I. A specific load power profile lasting 20 s has been selected to test saturation in the grid-side converter.

A. Ideal case

Results when neither grid power restriction nor compensation are shown in Fig. 8. Due to the limited bandwidth of the grid-side DC voltage control, some small DC voltage deviations are produced during the transients. Still, the system operation is nearly ideal. However, when the grid power exceeds the maximum power, the problem shown in Section II will arise. In the following discussion, grid power limits are set to ± 1 pu for comparison of the proposed compensation mechanisms. Moreover, the grid power limits are forced to ± 0 pu between 12 s and 15 s so compensation techniques under islanding can also be tested.

TABLE I
System parameters.

Parameter	Value
Filter inductor inductance (L)	1.7 mH
Filter inductor resistance (R)	0.33 Ω
DC-link total capacitance (C_{dc})	750 μF
Nominal grid power (base power value)	1 kW
Nominal DC-link voltage (DC base voltage value)	450 V
Nominal grid line RMS voltage	245 V
Nominal grid frequency	50 Hz
Nominal load voltage	48 V
Nominal battery voltage	144 V
Nominal supercapacitor voltage	48 V
Current control loop bandwidth	300 Hz
Grid-side DC voltage control bandwidth	20 Hz
Grid-side DC voltage control proportional gain (K_p)	0.06664
Grid-side DC voltage control integral gain (K_i)	88.86
ESS HPF cutoff frequency (f_{cESS})	0.1 Hz
Battery LPF cutoff frequency (f_{cb})	0.5 Hz
Compensation PI HPF cutoff frequency (f_{cPI})	1 Hz
Central control system frequency	100 Hz
Distributed control system frequency	10 kHz

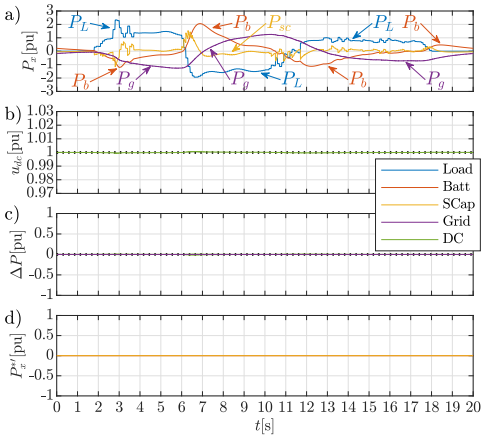

Fig. 8. Simulation results: Ideal case. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus. Dashed lines: grid power limits. Dotted lines: theoretical model evolution.

B. Direct power reference compensation

Second simulation considers the direct power reference compensation presented in Subsection III-A. Results are shown in Fig. 9. As it can be seen, the maximum grid power is accomplished so saturation conditions are considered. The DC-link voltage (u_{dc}) has a similar evolution than in the ideal case, except when saturation is produced. During these events, the power mismatch (ΔP) is not zero (Fig. 9c), so the remaining grid power (ΔP_g^*) takes a non-zero value and a DC-link voltage deviation is produced. For the compensation, the PSC generates an extra power reference for the ESS (Fig. 9d), which is shared between the battery and the supercapacitor. Thus, when comparing with the results shown in Fig, 4, the

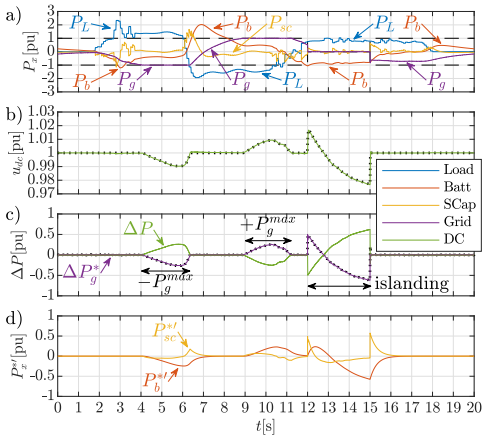

Fig. 9. Simulation results: Direct power reference compensation. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus. Dashed lines: grid power limits. Dotted lines: theoretical model evolution.

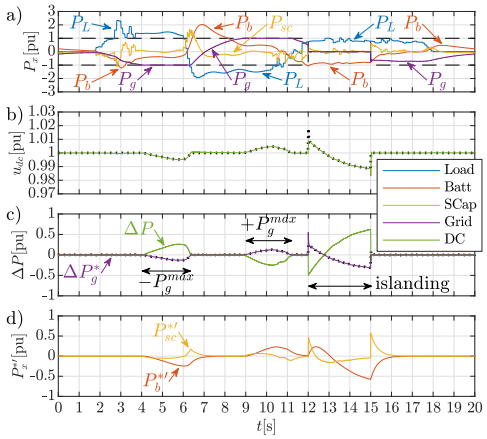

Fig. 10. Simulation results: Auxiliary DC voltage control with P controller. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

improved response is clearly visible.

Although the system continues operating within limits, there is a variation of about ± 0.02 pu in the DC-link voltage. As predicted by (22), this compensation method cannot totally compensate for the power mismatch. When the system enters in islanding, an expected larger variation can be easily seen.

C. Auxiliary DC voltage control

Third simulation is performed according to the discussion in Subsection III-B by enabling the auxiliary DC voltage control with a proportional controller. The proportional gain of the auxiliary DC voltage control is set to twice the one of the grid-side DC voltage control. Results are shown in Fig. 10. In this case, voltage variations during saturation are improved compared to the direct power reference compensation due to the equivalent doubled proportional gain and, consequently, the voltage deviation are reduced by this amplification ratio.

Nevertheless, although the voltage variations are mitigated, the DC-link voltage is not completely compensated and some deviations are still present. Note that since there is not integral action, the proportional gain shall be tuned in order to fulfill the maximum DC-link voltage deviation requirements.

Fourth simulation relies on the use of a PI controller for the auxiliary DC voltage control. The addition of an integral action eliminates any voltage deviation in steady state, so it is not necessary to increase the proportional gain in order to reduce the deviation. Therefore, both proportional and integral gains of the auxiliary DC voltage control take the same values of those for the grid-side DC voltage control, allowing to replicate the same dynamics. Results are shown in Fig. 11. Now, it can be observed that the integral action is being applied

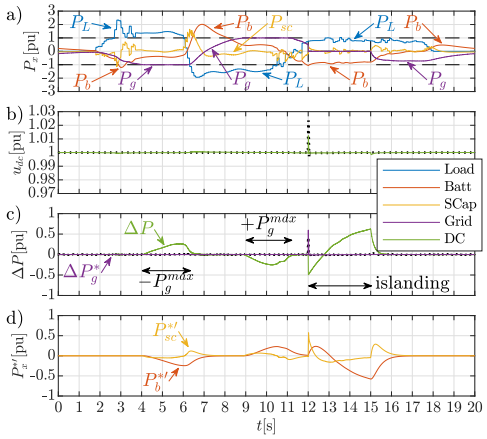

Fig. 11. Simulation results: Auxiliary DC voltage control with PI controller. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

whenever the auxiliary DC voltage control is enabled, so that the DC-link voltage error is completely canceled.

D. Enhanced power reference compensation

In here, the enhanced reference compensation proposed in Subsection III-C, both considering P and PI controllers, is taken into account.

Fifth simulation considers a proportional controller with a gain equal to 2. Results are shown in Fig. 12. As it can be seen,

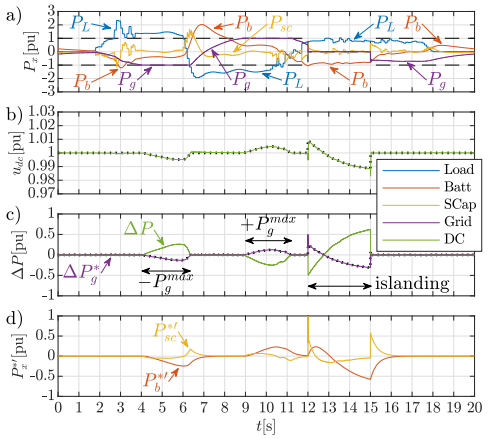

Fig. 12. Simulation results: Enhanced power reference compensation with P controller. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

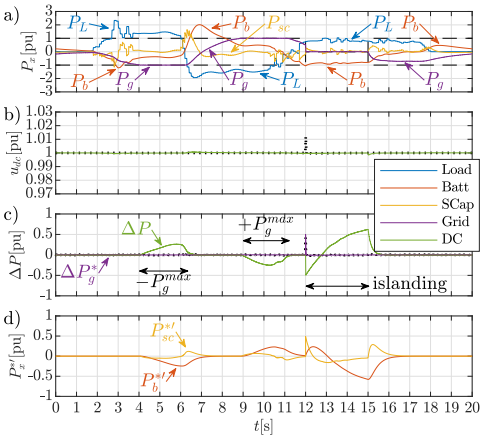

Fig. 13. Simulation results: Enhanced power reference compensation with PI controller. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

the results are similar to the ones obtained in Subsection IV-C with the P controller (Fig. 10) since the DC-link voltage variations are practically the same. Note that the proportional gain in both cases has the same multiplication factor (2), which explains the similarities in their behavior. Nevertheless, the enhanced power reference compensation shall be chosen over the auxiliary DC voltage control since it is easier to implement.

Sixth simulation relies on the use of a PI controller for the enhanced power reference compensation. Results are shown in Fig. 13. The results are practically the same to the ones obtained in Subsection IV-C with the PI controller (Fig. 11). However, when the system enters in islanding, the enhanced power reference compensation is able to maintain the DC-link voltage constant throughout the test, whereas the auxiliary DC voltage control suffers from a transient voltage deviation.

This is shown in detail in Fig. 14 and Fig. 15. As explained in Subsection III-D, when grid power limit is suddenly reduced, remaining grid power (ΔP_g^*) instantaneously varies with a magnitude equivalent to the grid power reduction. Therefore, enhanced power reference compensation immediately reacts, generating an instantaneous extra power reference for the supercapacitor ($P_{sc}^{*\prime}$) to avoid voltage deviation. However, auxiliary DC voltage control depends on the DC bus capacitor dynamics when reacting, provoking a bandwidth-limited extra power reference for the supercapacitor and hence some voltage deviation.

E. Summary

An overview of the key results (maximum grid power, cumulative error, maximum error and DC voltage overshoot) for all the simulation cases is shown in Table II. As it can be seen, in all the cases with compensation, the maximum grid power is within the expected limits.

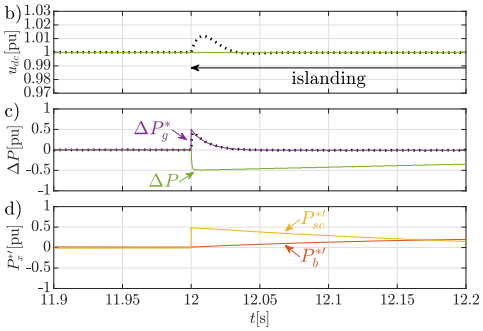

Fig. 14. Detail of simulation results: Enhanced power reference compensation with PI controller when entering in islanding mode. b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

TABLE II
PERFORMANCE OVERVIEW OF THE DIFFERENT SIMULATION CASES.

CASE	P_{grid}^{max} [pu]	$\int\lvert\text{error}\rvert$ u_{dc}[pu.s]	$\lvert\text{error}_{\max}\rvert$ u_{dc}[pu]	$\int\lvert\text{error}\rvert$ ΔP_g^*[pu.s]	$\lvert\text{error}_{\max}\rvert$ ΔP_g^*[pu]
A) Ideal grid	1.3	0.0029	0.0007	0	0
B) Direct pow	1.0	0.0686	0.0233	1.7869	0.6206
C1) Aux DC (P)	1.0	0.0353	0.0168	0.8945	0.5458
C2) Aux DC (PI)	1.0	0.0031	0.0124	0.0262	0.5972
D1) Enh pow (P)	1.0	0.0355	0.0168	0.8959	0.4999
D2) Enh pow (PI)	1.0	0.0030	0.0016	0.0239	0.4998

The direct power reference compensation is the worst method for all the metrics, followed by the auxiliary DC voltage control and the enhanced power reference compensation with P controller, whose cumulative errors are almost

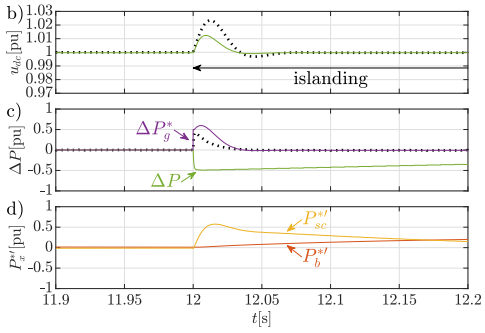

Fig. 15. Detail of simulation results: Auxiliary DC voltage control with PI controller when entering in islanding mode. b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

TABLE III
STATISTICAL ANALYSIS (MEAN, STANDARD DEVIATION) OF THE ERROR BETWEEN THEORETICAL MODEL AND SIMULATION RESULTS.

CASE	mean u_{dc}[%]	SD u_{dc}[%]	mean ΔP_g^*[pu]	SD ΔP_g^*[pu]
B) Direct pow	0.0043	0.0301	0.1728	0.7079
C1) Aux DC (P)	0.0061	0.0439	0.1165	0.7809
C2) Aux DC (PI)	0.0076	0.0361	0.2068	0.9089
D1) Enh pow (P)	0.0061	0.0459	0.0775	0.4198
D2) Enh pow (PI)	0.0073	0.0325	0.1684	0.3561

reduced by 2, since their equivalent proportional gain is twice the one for the direct power reference compensation. These compensation methods without integral action are able to reduce but not totally correct the power mismatch, as it can be seen by comparison with the ideal case.

The compensation methods including a PI controller have a better performance, since their cumulative errors are close to the ideal case. Particularly, the enhanced power reference compensation with PI controller gives the best results, providing a virtually perfect DC-link voltage regulation under saturation conditions. Therefore, the enhanced power reference compensation will be chosen over the auxiliary DC voltage control for the experimental validation.

The dotted lines from Figs. 8-13 show the theoretical model evolution of the DC-link voltage and the remaining grid power by using the simulated power mismatch as input in the transfer functions, in order to compare them with the simulation results. As it can be seen, they virtually match except during large transients. The statistical analysis shown in Table III validates numerically these results, since both the mean and standard deviation of the modelling error are almost negligible.

Table IV shows the total energy flowing through the different power devices, considering positive the energy that flows through the loads and negative the energy that flows through the sources (grid, battery and supercapacitor). By summing all these energies, the circulating energy is obtained. As shown in Table IV, the circulating energy is about 8 pu.s. Assuming an efficiency of 90% in the power converters, losses due

TABLE IV
TOTAL ENERGY FLOWING THROUGH THE DIFFERENT LOADS(+) AND SOURCES(−), AND TOTAL CIRCULATING ENERGY ($\sum$) IN SIMULATION RESULTS.

CASE	$+\int\lvert P_L\rvert$ [pu.s]	$-\int\lvert P_g\rvert$ [pu.s]	$-\int\lvert P_b\rvert$ [pu.s]	$-\int\lvert P_{sc}\rvert$ [pu.s]	$\sum\int\lvert P\rvert$ [pu.s]
A) Ideal grid	+17.04	−12.64	−9.91	−3.31	−8.82
B) Direct pow	+17.04	−10.85	−10.83	−3.39	−8.03
C1) Aux DC (P)	+17.05	−10.85	−10.84	−3.40	−8.04
C2) Aux DC (PI)	+17.04	−10.73	−10.92	−3.37	−7.99
D1) Enh pow (P)	+17.04	−10.85	−10.84	−3.40	−8.05
D2) Enh pow (PI)	+17.04	−10.73	−10.92	−3.37	−7.99

to the circulating power are about 0.8 pu.s. Therefore, by comparing these losses with the energy needed by the load (about 17 pu.s), an increment of about 4.7% in the total energy is produced because of the circulating power. The authors consider that increment to be low compared to the benefits regarding the enhanced overall system stability and improved control margins.

F. Effect of power measurement errors and communication delays

All simulations already performed in this section have considered ideal power measurements and no communication delays when sending power references to the ESS (battery + supercapacitor). However, in a more realistic approach, errors in the sensors will distort the power measurements, and delays will affect the references sent from the central controller or the Power Sharing Compensator (PSC) to the battery and supercapacitor interface converters, as shown in Fig. 2. Therefore, additional simulations are conducted with the enhanced power reference compensation to test these phenomena.

Fig. 16 and Fig. 17 show the effect of having a 10% error in the grid power measurement, a 15% error in the battery power measurement and a 25% error in the supercapacitor measurement. Comparing these results to the ones with ideal sensor (Fig. 12 and Fig. 13), it can be seen that additional power mismatches appear in the system. In the case of using a P controller, the magnitude of the voltage deviation will be slightly amplified, but the DC-link voltage will remain almost constant in the case of using a PI controller.

Fig. 18, Fig. 19 and Fig. 20 show the effect of adding a communication delay of 2 ms, 5 ms and 10 ms when sending the power references to the battery and the supercapacitor. A communication delay of 2 ms (Fig. 18) does not provoke any noticeable change in the performance of the system, as can be shown by comparing it to the case with no delays (Fig. 13). However, a delay of 5 ms (Fig. 19) does affect the behavior of the system, deteriorating its performance, as can be seen in the deviation produced in the bus voltage when entering in islanding at 12 s. Finally, a delay of 10 ms (Fig. 20) makes the system unstable. Therefore, the maximum communication delay can be up between 2 ms and 5 ms to not alter the performance of the system. The utilization of industrial communication networks (e.g. Modbus [32], CAN [33], Ethercat [34]...) within that delay range and a distributed control system execution period of $(10\text{ kHz})^{-1} = 0.1$ ms

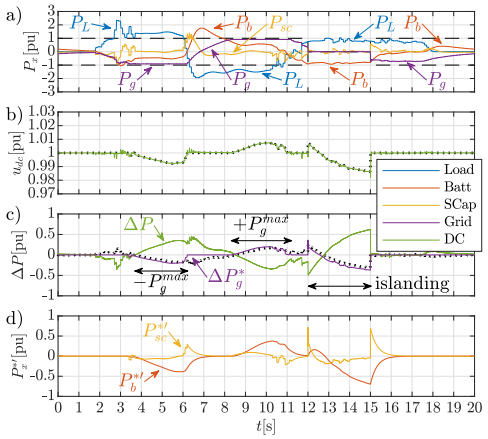

Fig. 16. Simulation results: Enhanced power reference compensation with P controller with power measurement errors: grid, 10%; battery, 15%; supercapacitor, 25%. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

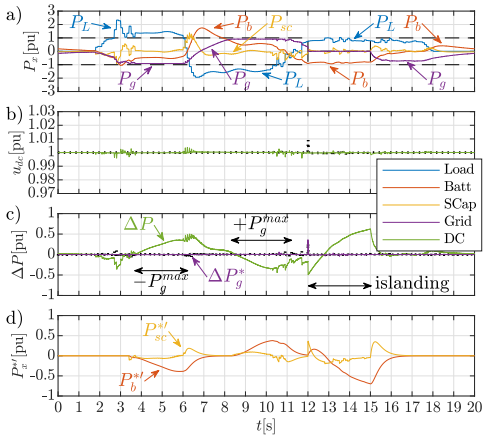

Fig. 17. Simulation results: Enhanced power reference compensation with PI controller with power measurement errors: grid, 10%; battery, 15%; supercapacitor, 25%. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

(Table I), 20 times faster than the maximum communication delay, guarantees a proper operation of the system.

V. Experimental results

Experimental validation is carried out using the setup shown in Fig. 21 for the different tests. The same load power profile and system parameters used in the simulation section are here considered.

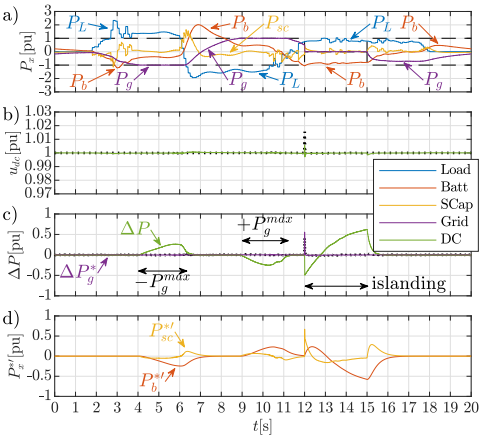

Fig. 18. Simulation results: Enhanced power reference compensation with PI controller with a communication delay of 2 ms when sending power references to battery and supercapacitor. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

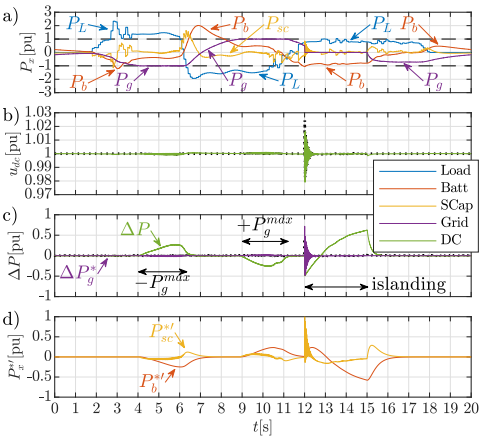

Fig. 19. Simulation results: Enhanced power reference compensation with PI controller with a communication delay of 5 ms when sending power references to battery and supercapacitor. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

The setup consists on two three-phase converters connected through the DC link (back-to-back) and two 4-wire 3-phase inductor filters, which allow the interconnection of the different power units: AC grid, battery, supercapacitor and bidirectional load. The parameters are listed in Table I. The implementation of the control system is carried out by using two different control units: a Texas Instruments TMS320F28335 DSC at

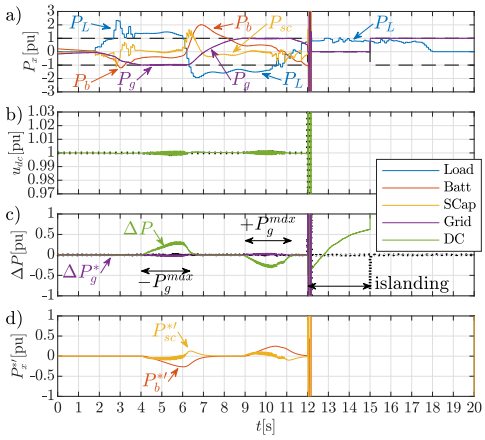

Fig. 20. Simulation results: Enhanced power reference compensation with PI controller with a communication delay of 10 ms when sending power references to battery and supercapacitor. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

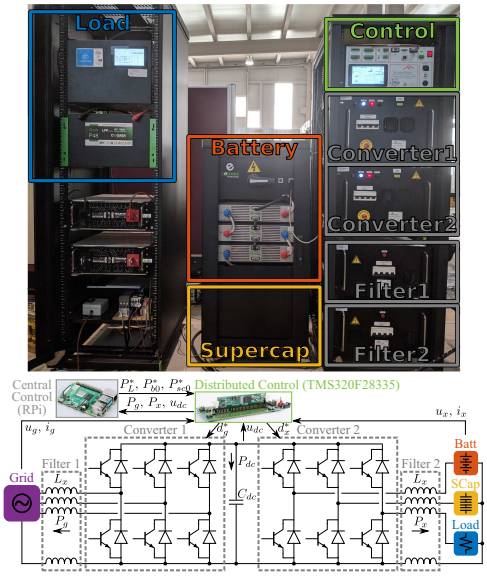

Fig. 21. Experimental setup: Front side and electrical diagram.

the distributed control system and a single-board computed (SBC) Raspberry Pi at the central control system.

Various experimental tests are carried out to demonstrate the suitability of the different compensation techniques and to address some problems that may appear during the real implementation: ideal grid, direct power reference compensation and enhanced power reference compensation.

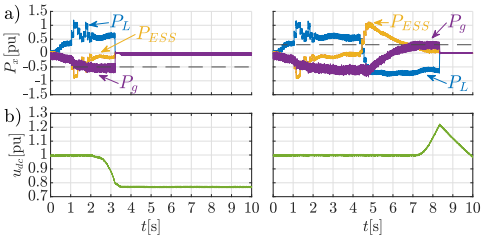

Fig. 22. Experimental results: Power sharing issues when the grid power is limited (left, −0.5 pu; right, +0.3 pu). a) Power consumption; b) DC-link voltage. Color legend: blue, load; orange, ESS; purple, grid; green, DC bus. Dashed lines: grid power limits.

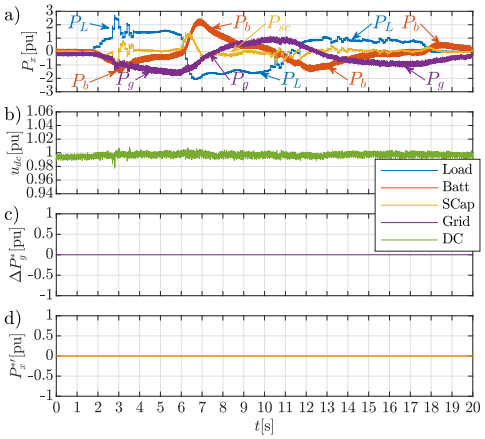

Fig. 23. Experimental results: Ideal case. a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Extra power reference. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus. Dashed lines: grid power limits.

First experimental test verifies the results shown in Section II (Fig. 4), in which grid power restrictions are applied without compensation. Results are shown in Fig. 22. As it can be seen, the DC-link voltage either drops to the rectifier level or rises to fault values when the grid power reach the limits.

Second experimental test is related to the simulation performed in Subsection IV-A, in which there is neither grid power restriction nor compensation. Results are shown in Fig. 23. As expected and in agreement with the simulation results, the DC-link voltage remains almost unchanged, while the grid power exceeds the considered power limit.

Third experimental test verifies the simulation conducted in Subsection IV-B, in which the direct power reference compensation is applied. Results are shown in Fig. 24. As it can be seen, the grid power is now limited to the maximum one. When the grid control reaches saturation, the DC-link

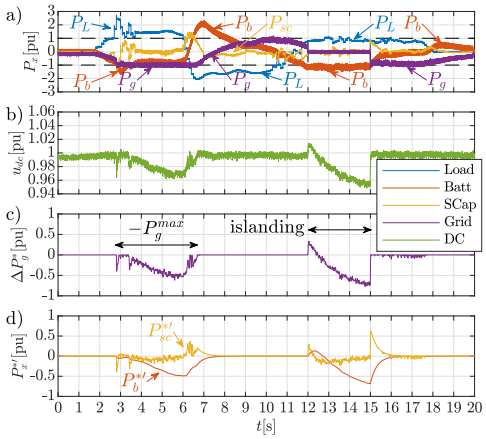

Fig. 24. Experimental results: Direct power reference compensation. a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Extra power reference. Legend is the same as Fig. 23.

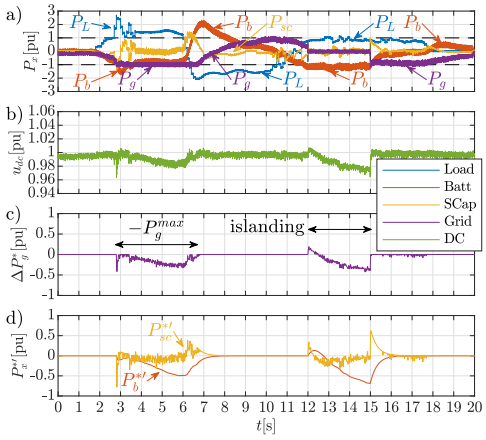

Fig. 25. Experimental results: Enhanced power reference compensation with P controller. a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Extra power reference. Legend is the same as Fig. 23.

voltage varies but its deviation is mitigated by applying some extra power via the energy storage system.

Fourth experimental test replicates the simulation in Subsection IV-D, in which the enhanced power reference compensation with a P controller is applied. Results are shown in Fig. 25. As expected, this compensation method improves the performance of the direct power reference compensation, with a reduction to a half in the DC-link voltage variations.

Last experimental test follows the enhanced power reference compensation with a PI controller discussed in Subsection IV-D. Results are shown in Fig. 26. It is clear from the results that this compensation technique is the best one, since the DC-link voltage deviation is nearly zero, obtaining a result which is equivalent to the ideal case.

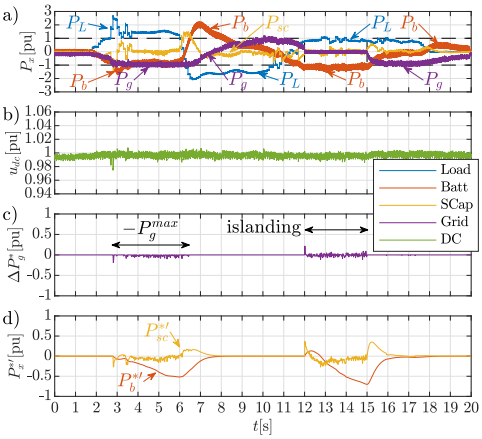

Fig. 26. Experimental results: Enhanced power reference compensation with PI controller. a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Extra power reference. Legend is the same as Fig. 23.

TABLE V
PERFORMANCE OVERVIEW OF THE DIFFERENT EXPERIMENTAL TESTS.

CASE	P_{grid}^{max} [pu]	$\int$|error| u_{dc}[pu.s]	|error$_{max}$| u_{dc}[pu]	$\int$|error| ΔP_g^*[pu.s]	|error$_{max}$| ΔP_g^*[pu]
A) Ideal grid	1.6	0.0299	0.0081	0	0
B) Direct pow	1.0	0.1537	0.0440	2.4027	0.7715
D1) Enh pow (P)	1.0	0.0872	0.0254	1.2513	0.4244
D2) Enh pow (PI)	1.0	0.0299	0.0094	0.1444	0.2154

All the experimental tests show similar results (Table V) to those of the simulation. Direct power reference compensation is the worst method for all the metrics, followed by enhanced power reference compensation with P controller, whose cumulative errors are almost reduced by 2, since their equivalent proportional gain is twice the one for the direct power reference compensation. Enhanced power reference compensation with PI controller gives the best results. Therefore, the feasibility of the real implementation of the power mismatch compensation techniques discussed throughout the paper is demonstrated.

Table VI shows the total energy flowing through the different power devices using the same sign convention than in the simulation results. Results are shown in Table VI. The circulating energy is about 9.5 pu.s. Assuming an efficiency of 90% in the power converters, losses due to the circulating power are about 0.95 pu.s. Therefore, by comparing these losses with the energy needed by the load (about 17.7 pu.s), an increment of about 5.4% in the total energy is produced because of the circulating power.

TABLE VI
TOTAL ENERGY FLOWING THROUGH THE DIFFERENT LOADS(+) AND SOURCES(−), AND TOTAL CIRCULATING ENERGY ($\sum$) IN EXPERIMENTAL TESTS.

CASE	$+\int\lvert P_L\rvert$ [pu.s]	$-\int\lvert P_g\rvert$ [pu.s]	$-\int\lvert P_b\rvert$ [pu.s]	$-\int\lvert P_{sc}\rvert$ [pu.s]	$\sum\int\lvert P\rvert$ [pu.s]
A) Ideal grid	$+17.70$	-14.06	-10.87	-2.96	-10.19
B) Direct pow	$+17.67$	-11.45	-12.81	-2.94	-9.54
D1) Enh pow (P)	$+17.66$	-11.41	-12.88	-2.97	-9.59
D2) Enh pow (PI)	$+17.66$	-11.07	-13.05	-2.96	-9.43

VI. CONCLUSIONS

This paper has presented some compensation techniques of power sharing error affecting the DC-link voltage regulation in a multi-port DC/DC/AC converter. The proposed alternatives have been analytically discussed and firstly validated by numerical simulations, considering saturation events, transient behavior and operation under islanding mode. Among the presented alternatives, the enhanced power reference compensation with a PI controller shows the best trade-off between implementation complexity and performance. The proposed methods have been also validated by experimental results with a close match between the simulation and the real implementation.

Studied power mismatch compensation techniques are designed to be used regardless of the system nominal power, as shown in (22), (26), (27) and (30). Therefore, these compensation techniques can be applied to utility-scale power systems by resizing the power cells (iPEBBs) to withstand the required voltages and currents. Few tweaks will be needed in the proposed compensation methodology, regarding the voltage/current limits and the tuning of the control gains to adequate to the new values for the physical components.

Moreover, the influence of communication delays is critical on the system performance, making the system unstable if a certain threshold is exceeded. Future work for precisely characterizing these delays and analyzing different compensation techniques, such as the Smith predictor [35], to mitigate the influence of delays and improve the dynamic response of the system.

Lastly, it is worth mentioning that harmonics or unbalances in the grid would provoke undesired variations in the DC-link voltage introduced by the grid power control. In particular, unbalances in the grid will cause DC-link voltage variations at twice the fundamental frequency, whereas $6n\pm1$ harmonics in the three-phase grid will induce $6n$ harmonics. These considerations are focus of future works.

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Appendix B

Conference publications

B.1 Distributed Control Alternatives of Modular Power Converters for Hybrid DC/AC Microgrids

Distributed Control Alternatives of Modular Power Converters for Hybrid DC/AC Microgrids

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***Abstract*—This paper proposes a distributed control alternative for modular power converters. The focus is on the use of single-phase power units with embedded control capabilities, namely intelligent Power Electronics Building Block (iPEBB) for power conversion in hybrid DC/AC microgrids. The distributed control is achieved by the use of a versatile controller inside each iPEBB, so that they can operate independently by controlling their own voltage(s)/current(s). For the management of the entire system, a central controller is integrated into the control scheme. The central controller is in charge of the application-level control of the modular power converter, so that it determines the role of each iPEBB and commands the references to achieve the control goals. As a demonstration of the proposed approach, the control of a 4-wire 4-leg STATCOM using 4 independent power units is shown in this paper. For the implementation of the iPEBB control system, two different approaches are evaluated: Proportional-Resonant (PR) and Repetitive Control (RC) alternatives. Analysis is done using direct discrete design. Different simulations as well as experimental results are performed in order to validate the proposed system. The study considers communication delays between the central controller and the iPEBB as well as internal reconstruction of the reference from the central controller command.**

I. Introduction

Nowadays, the penetration of renewable energy generation is encouraging an evolution towards distributed generation systems, with the appearance of local small-scale power systems known as microgrids [1]. Microgrids opt for implementing hybrid generation using batteries, supercapacitors and flywheels [2], [3] to have a flexible and reliable operation. The increasing requirements regarding the number of switches, the switching frequency and the communication needs are driving the change of the control systems, moving from the central DSP/DSC based architecture to decentralized architectures [4]. The benefits of this approach can be summarized as: 1) scalability in terms of the needed inputs (A/D) and outputs (PWM), 2) flexibility and 3) reliability. However, there are some drawbacks that make the implementation more difficult than the one based on a central controller. In particular, the need of synchronization and communications as well as a change in the control design.

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In order to accomplish a modular power converter, different proposals can be found in the literature using basic power cells [4], [5] to interface with the power system. This power cell is known as Power Electronics Building Block (PEBB) [5] and has to be controlled according to the desired power converter topology. Therefore, a distributed control system has to be developed in order to achieve a proper behavior of the modular power converter. This control consists of an individual autonomous control for each of the power blocks (inner current and voltage control loops), and a central controller to coordinate all the power blocks and provide a specific function to the whole power converter (application-level control loops).

In a generic application-agnostic approach, the inner control loop of each power cell has to be capable of tracking references and rejecting disturbances of different polynomial order. In this paper, the analysis is restricted to AC/DC and DC/AC power conversion, in which references and disturbances are expected at the fundamental harmonic frequency and its multiples. Based on the internal mode principle [6], the controllers need an internal harmonic generator model to properly manage harmonic references/disturbances. In this way, a theoretical zero steady-state error is achieved at the harmonic frequencies. Control techniques which meet this requirement are Proportional-Resonant (PR) controllers [7]–[9] and Repetitive Controllers (RC) [10]–[12].

The outer control loop of the central controller shall provide the control goals, i.e. references to the PEBB and receive the feedback signals for the control of the complete power converter through a communication channel, which implies the appearance of pure delays. The impact on the performance of these intrinsic pure delays have to be considered during the control system design.

The objective of this paper is to tackle the control issues for the system explained above. The studied case will be a 4-wire 4-leg grid-tied inverter. Particular emphasis will be placed in the reference tracking and disturbance rejection of fundamental and non-fundamental harmonics. The behavior under changes in the fundamental frequency will be analyzed. Communication delays will also be taken into account.

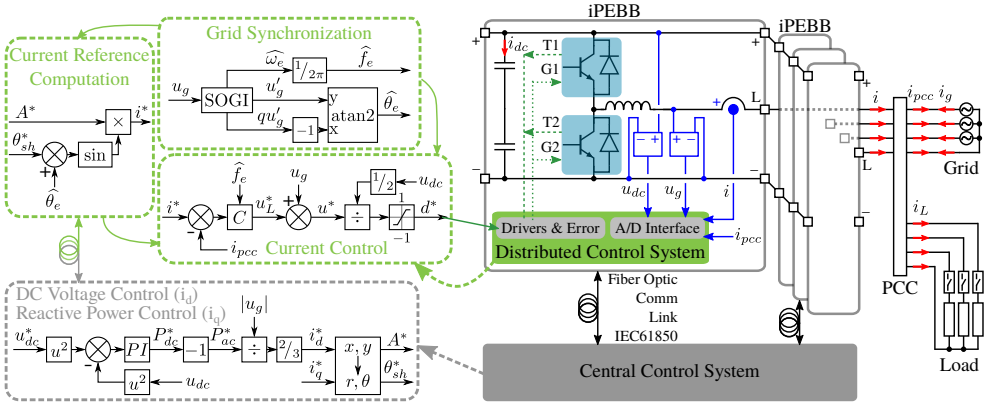

Fig. 1. Proposed architecture for a modular power converter based on iPEBB. The application is for a 4-wire 4-leg STATCOM connected to the grid.

This paper is organized as follows. In Section II, an explanation of the proposed system architecture is addressed. In Section III, an analysis of the different control alternatives suited for managing periodic signals is discussed. In Section IV, several control issues related to the studied case are analyzed. In Section V and Section VI, simulation and experimental results are obtained in order to validate the proposed system. Finally, in Section VII, conclusions about the accomplished work are discussed.

II. System Architecture

The proposed solution consists of several single-phase power cells (upper and lower power switches, parallel capacitor, and series inductor in mid-point) with built-in voltage and current sensors, and a digital control system which manages the power cell; thus creating an intelligent PEBB (iPEBB). On top of them, a central controller, based on a generic microprocessor with real-time capabilities and a fast communication channel, coordinates all the system.

The iPEBBs provide the interface with the global power system and hence their objective is to measure the electric variables (voltages and currents) and give the switching command to the drivers turning on/off the switches according to the desired control action. The central controller determines the application of the whole system by sending messages to the power cells with information about the operating point. An schematic of the proposed architecture for the power converter is shown in Fig. 1. Integration with the system operator, even if not analyzed in the present paper, is proposed to be implemented using the IEC61850 standard.

In order to validate the proposed architecture, the modular converter will behave as a 4-wire 4-leg STATCOM connected to the grid. Therefore, the main objective of the test application is to compensate reactive power and mitigate unbalances and harmonics produced by the connection of local loads, so that the current at the PCC is balanced and does not contain any non-fundamental harmonics. Four iPEBBs are used to carry out the current control of the three active phases and the neutral phase (homopolar injection), whereas the central controller is in charge of the DC link voltage control (i_d^*) and the reactive power compensation (i_q^*). The DC link voltage control uses a quadratic implementation to obtain directly the required power as control action.

The central controller sends messages with references of current magnitude (A^*) and phase shift (θ_{sh}^*) to the iPEBBs in charge of the active phases. Note that the homopolar current controller (neutral phase) does not receive any references from the central controller since its reference is zero (local control).

Since the system is connected to the grid and is working with resonant single-phase controllers, a SOGI is implemented for each iPEBB to carry out the grid synchronization. This way, each iPEBB is capable of estimating the grid frequency ($\widehat{f}_e$) and the grid voltage phase ($\widehat{\theta}_e$), and thus it can tune properly its resonant controller (C) and compute the current reference (i^*).

Note that the current control has to manage currents at the fundamental grid frequency and corresponding harmonics, so the selection of the single-phase controller (C) topology is not straightforward. An analysis of the different control alternatives is going to be done in the next section.

III. Analysis of Control Alternatives

The control of single-phase signals at a nominal frequency and multiples is analyzed in this section. The analysis is focused on the study of resonant controllers, particularly the proportional-resonant (PR) controller and the repetitive controller (RC).

A. Proportional-resonant controller

1) Continuous domain: The PR controller is a generalization of a proportional-integral (PI) controller centered at an

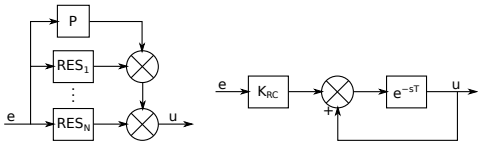

Fig. 2. Proportional-resonant (a) and repetitive (b) controller.

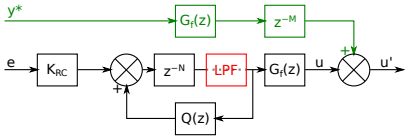

Fig. 3. Direct repetitive controller with feed-forward term (green path) and optional low-pass filter in direct path (red block).

arbitrary frequency. The PI controller is capable of achieve zero steady-state error for DC references (0Hz) whereas the PR controller has to be capable of achieve zero steady-state error at the central frequency. The continuous transfer function of the PR controller is given by [7].

The implementation of a PR controller in discrete domain can be achieved both by discretization methods (often Tustin with pre-warping is used) or by direct-discrete design techniques. The first approach is easier to implement, but tracking of higher harmonics becomes difficult if the sample-time delay is not considered. In this paper, direct-discrete design is used in order to extend the controller capabilities.

2) Discrete domain: The derivation of the PR controller in discrete domain is obtained from the discrete PI expression shown at (1).

$$C_{PI}(z) = C_P(z) + C_I(z) = K_p + \frac{K_i T_s}{z-1} \tag{1}$$

Applying the same derivation as in [7] to (1) as shown in (2), the discrete PR controller is obtained. This PR controller has infinite gain at the resonance frequency (ω), and thus zero steady-state error at that frequency. When considering multiple harmonics, the expressions in (3) and (4) are obtained, which is related to the block diagram shown in Fig. 2a.

$$C_{RES}(z) = C_{PI}(ze^{+j\omega T_s}) + C_{PI}(ze^{-j\omega T_s}) \tag{2}$$

$$C_{PR}(z) = C_P(z) + \sum C_{RES}(z) \tag{3}$$

$$C_{PR}(z) = K_p + \sum_{h\in\mathbb{Z}^*} \frac{2K_{ih}T_s\left[\cos(h\omega T_s)z - 1\right]}{z^2 - 2\cos(h\omega T_s)z + 1} \tag{4}$$

As it can be observed, the coefficients of the PR controller have to be calculated using the fundamental frequency of the system, and the number of resonant controllers in parallel depends on the number of harmonics which is going to be taken into account. This makes this multiple-parallel-connected PR approach tedious to implement [9].

B. Repetitive controller

1) Continuous domain: The RC is mainly based on the concept that it is possible to generate a periodic signal with a fixed period by means of a system with a pure time delay equal to the signal period (T) and a unitary positive feedback around this delay [10]. Applying the internal model principle [6], it is possible to design a controller capable of tracking a periodic variable by including the model inside its scheme. The resultant controller is shown in (5) and Fig. 2b.

$$C_{RC}(s) = K_{RC}\frac{e^{-sT}}{1-e^{-sT}} \tag{5}$$

The implementation of the RC into a digital control system is straightforward since the pure time delay is transformed into a number of control periods delay depending on the sampling frequency.

2) Discrete domain: As stated before, the RC digital implementation offers simplicity as a main advantage. Nevertheless, the stability of this controller is compromised since the RC introduces a unitary positive feedback. Therefore, the final scheme of the RC has to be tweaked a little bit. The presented discrete RC is known as direct repetitive controller (DRC) [11], [12]. The delay is now determined by an integer number of samples (N) and its expression is shown at (6) and Fig. 3.

$$C_{DRC}(s) = K_{RC}\frac{z^{-N}}{1-Q(z)z^{-N}}G_f(z) \tag{6}$$

Compared to Fig. 2b, in Fig. 3 there are two additional blocks, the robustness filter $Q(z)$ and the stability filter $G_f(z)$. The robustness filter is used to avoid a perfect positive feedback which could lead to an unstable system. There are several options for the robustness filter: constant value slightly lower than one, low-pass filter, moving average filter, etc. The stability filter is computed in order to achieve a zero-phase-shift (ZPS) compensator [12], so that the dynamics of the power converter filter are compensated and its influence is attenuated: $G_f(z) = \hat{G}_{OL}^{-1}(z)$.

Compared to the multiple-parallel-connected PR, the DRC is easier to implement since it provides an infinite number of resonances at multiples of the fundamental frequency without need of parallelization. However, this behavior implies that the repetitive controller reacts to high-frequency harmonics, which can lead to an unstable behavior due to high-frequency noise. In order to avoid this behavior, two different topologies are accounted: 1) Robustness filter $Q(z)$ with constant value slightly lower than one and without low-pass-filter (LPF) $\Rightarrow$ DRC; 2) $Q(z) = 1$ and low-pass filter (LPF) after the pure delay z^{-N} (Fig. 3 with red block) $\Rightarrow$ DRC_LPF.

Additionally, the RC has a drawback in the form of one fundamental period delay in order to track references (learning period). In order to reduce this effect, a feed-forward component of the reference through the block $G_f(z)$ is added to the action control of the controller as shown in Fig. 3 [13]. Note

that $G_f(z)$ is not a proper system in this case, so an additional pure delay (z^{-M}) is included in the feed-forward path to make the resultant system biproper.

The iPEBBs of the modular converter are not computationally very powerful, so that the control topology is focused on the use of repetitive controllers to reduce the complexity of the computations as stated in Subsection III-A. In particular, the DRC with LPF will be used to limit the bandwidth of the system.

IV. Control issues

The modular implementation approach used in this paper, together with the use of resonant controllers for the current control loop, implies the appeareance of some control issues, which are discussed hereunder: frequency shifts, communication channel and reference reconstruction.

A. Frequency shifts

The main problem of resonant controllers appears when the fundamental frequency is shifted with regard to the nominal frequency. In order to solve this problem, an adaptive frequency-dependent version of the resonant controllers has to be implemented.

Similarly, operation under variable frequency for the DRC case requires to adapt the delay value, as it depends on the ratio between the sampling frequency and the fundamental frequency. However, an integer relationship has to be kept according to the controller expression. Therefore, variations of the fundamental frequency cannot be fully compensated in a first approach (non-integer ratio). There are two options to solve this problem: 1) modifying the sampling frequency to achieve an integer delay or 2) implementing a fractional delay (z^{-F}) computation. The chosen option is the second one since the first would increase the complexity and the cost of the system. It is possible to halve the minimum delay of the controller as stated in [14] ($\omega_1 = 2$ and $\omega_2 = -1$ for even and odd harmonic compensation) but a better solution is addressed in [15], which is capable of compensating any kind of fractional delay by using a Lagrange-interpolating-polynomial-based fractional delay filter. A cubic interpolating polynomial is used: $z^{-F} \approx H_0 + H_1 z^{-1} + H_2 z^{-2} + H_3 z^{-3}$. The z^{-F} estimation block is placed just after the integer delay block (z^{-N}).

In this way, under frequency shifts, the integer part of the new ratio between sampling frequency and fundamental frequency will be considered by shifting the coefficients of the DRC (pure delay variation) whereas the non-integer part will be considered by changing the coefficients of the fractional delay filter.

B. Communication channel

A communication channel is required in order to connect the central controller and the power cells. This implies an additional problem in comparison to conventional control schemes, which is the appearance of stochastic pure delays between the outer and the inner control loop. In the analyzed case, the central controller sends references to the power cells (current magnitude and phase shift) and receives measurements from them (DC link voltage). In order to reduce the cost and the complexity of the system, a common communication channel is used for the entire system. Two operation modes are considered in relation to the communication channel:

- Asynchronous mode. Each power cell updates the reference value and the central controller updates the corresponding measurement asynchronously once the communication is carried out. Accumulative delays take place between power cell variables, so that virtual unbalances appear.
- Synchronous mode. A synchronization message is added to the communication protocol in order to synchronize the different elements of the system. In this case, the synchronization message is sent after all the references/measurements sequence. Only after this message, the elements of the system update their references/measurements, so that the accumulative delay effect disappears.

In this paper, the asynchronous mode is considered in order to avoid the need of synchronization among the different cells. This operation mode will be analyzed, and its effect over the error of the generated current will be considered as the figure of merit.

C. Reference reconstruction

The central controller is in charge of sending references to the individual iPEBBs. Since the control loop frequency of the power cells is higher than the control loop frequency of the central controller (a ratio of 10 for this research), the iPEBBs have a constant value for the reference between external loop iterations, thus leading to step-wise reference changes that cause additional distortion in the system, as shown in Fig. 4 (Initial Case).

To mitigate this problem, a linear extrapolation process at the iPEBB is proposed in this research in order to obtain a reference with a smoother shape for the intermediate iterations of the distributed current control with regard to the centralized voltage control, as shown in Fig. 5. The numerical expression is shown in (7).

$$x_k = \frac{x_{k'} - x_{(k-1)'}}{k_0 - k_{-1}} (k - k_0) + x_{k'} \tag{7}$$

After applying the linear extrapolation to the received reference, the results shown in Fig.4 (Reconstructed Ref. Case) are obtained. As can be seen, the spikes in the converter voltage because of sharp reference changes are mitigated, and thus the converter current is smoother. Note that, the extrapolation used in this case is linear but higher order extrapolation algorithms can be used in order to improve slightly the performance.

This algorithm is applied in the iPEBB to the magnitude reference (A^*) but not to the phase shift (θ^*_{sh}) in order to avoid an overcorrection of the whole reference.

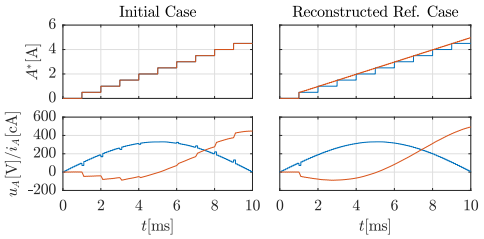

Fig. 4. Comparison between the initial case (left figures) and the reconstructed reference case (right figures) for one phase of the converter. Top figures: blue, reference sent by the central controller; orange, reference built by the single-phase controller via extrapolation. Bottom figures: blue, converter voltage; orange, converter current.

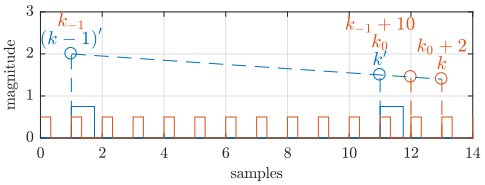

Fig. 5. Graphical representation of the linear extrapolation process used to generate a smooth reference for the intermediate iterations of the distributed current control. Circular marks represent the samples of the control loops and square signals represent the control loop periods. Blue variables are related to the centralized voltage control whereas orange variables are related to the distributed current control.

TABLE I
SYSTEM PARAMETERS.

Parameter	Value
Active phase filter inductance (L)	7 mH
Active phase filter resistance (R)	0.3 Ω
Neutral phase filter inductance (L_n)	3 mH
Neutral phase filter resistance (R_n)	0.06 Ω
DC link total capacitance (C_{dc})	5.04 mF
Nominal DC link voltage (U_{dc})	750 V
Sampling/PWM frequency	10 kHz
Current (iPEBB) control loop frequency	10 kHz
DC link voltage (central) control loop frequency	1 kHz
Nominal grid line RMS voltage	400 V
Nominal grid frequency	50 Hz

V. SIMULATION RESULTS

The simulation results are based on the system architecture shown in Fig. 1. The parameters are detailed in Table I.

In order to determine the system performance, four different tests will be conducted: 1) Reactive power management and frequency shifts, 2) Connection of local linear loads, 3) Connection of local non-linear loads, and 4) Error from communication delays. The complete simulation profile is shown in Fig. 6. For the subsequent analysis, the three-phase variables will be shown in a theoretical synchronous reference frame (dq0) in order to ease the understanding of the results.

As shown in Fig. 6, different operating conditions are

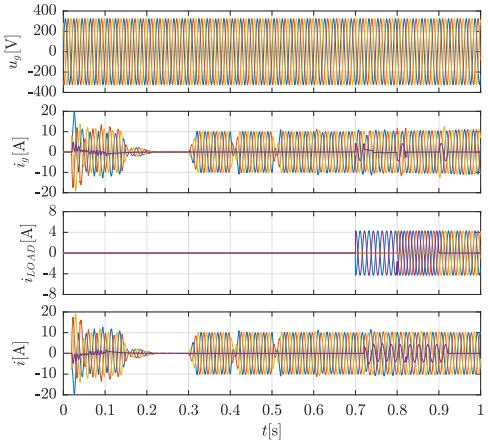

Fig. 6. Global simulation results. Variables are shown in phase coordinates (abcn): blue, phase A; red, phase B; orange, phase C; purple, phase N. 1) Grid voltage, 2) Grid current, 3) Load current, 4) Converter current.

evaluated: 1) At 0.02 s, the control is enabled; 2) From 0.3 s to 0.32 s, the reactive current reference (i_q^*) is changed from 0 A to −10 A by using a ramp; 3) From 0.4 s to 0.42 s, the reference is changed from −10 A to +10 A by using a ramp; 4) From 0.5 s to 0.52 s, the reference is changed from +10 A to −10 A by using a ramp; 5) At 0.6 s, the grid frequency is changed from 50 Hz to 47.2 Hz; 6) At 0.7 s, a resistive load of 700 W is connected between phase A and neutral phase; 7) At 0.8 s, a resistive load of 700 W is connected between phase B and neutral phase; 8) At 0.9 s, a resistive load of 700 W is connected between phase C and neutral phase.

A. Reactive power management and frequency shifts

The initial test consists in managing the reactive power which is injected/consumed into/from the grid by following the reference profile which was previously defined.

The results are shown in Fig. 7, Fig. 8 and Fig. 9. As can be seen, the DC link voltage reaches its nominal value at 0.3 s, which is maintained almost constant under changes in the reactive current. In addition, the reactive current management is properly done since the actual current follows the reference quickly and without steady-state error.

In addition, the grid frequency change is properly compensated in about 2 fundamental periods (40 ms). Note that, a huge step change in the grid frequency is tested (50 Hz to 47.2 Hz) whereas the grid frequency variations are much slower in a real application. The selection of the simulation final frequency value is not arbitrary, since it gives $(10000/47.2)$ an integer delay of 211 samples and a fractional delay of 0.8644. This way, the fractional delay is quite high and its compensation is also tested.

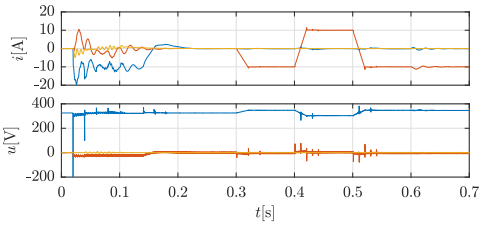

Fig. 7. Simulation results for reactive power management. Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. Top, converter current in synchronous reference frame. Bottom, current controller control action in synchronous reference frame.

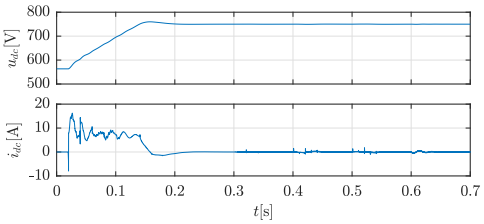

Fig. 8. Simulation results for reactive power management. Top, converter DC link voltage. Bottom, converter total DC link current.

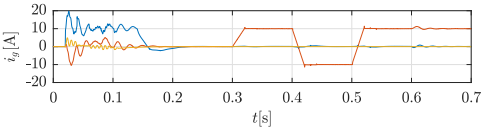

Fig. 9. Simulation results for reactive power management. Grid current in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis.

B. Connection of local linear loads

Disturbance rejection capabilities are demonstrated with a set of single-phase linear loads which are connected to the grid at different times. With the proposed control scheme, both negative sequence and homopolar currents are supplied by the converter, making the grid isolated from the disturbances in steady state, only supplying balanced currents.

The results of this test are shown in Fig. 10 and Fig. 11. As can be seen, the converter reacts to the local load connection after one fundamental period (20 ms) due to the inherent learning period of the repetitive controller. Note that the feed-forward term is only applied to the current reference and a disturbance is introduced into the system in this case. Nevertheless, the unbalances are compensated in steady state by the converter by injecting negative sequence and homopolar current into the local grid. The main grid only supplies the needed balanced power.

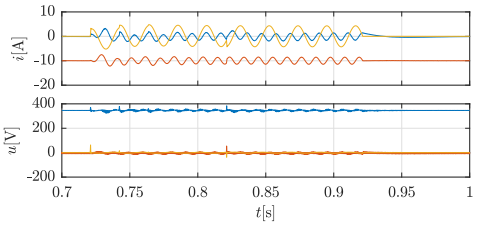

Fig. 10. Simulation results for local linear load connection. Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. Top, converter current in synchronous reference frame. Bottom, current controller control action in synchronous reference frame.

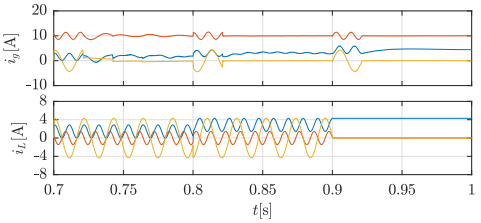

Fig. 11. Simulation results for local linear load connection. Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. Top, grid current in synchronous reference frame. Bottom, load current in synchronous reference frame.

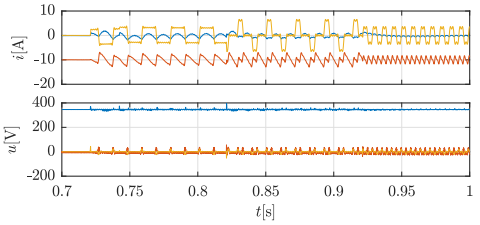

Fig. 12. Simulation results for local non-linear load connection. Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. Top, converter current in synchronous reference frame. Bottom, current controller control action in synchronous reference frame.

C. Connection of local non-linear loads

In order to see the disturbance rejection against non-fundamental harmonics, a set of non-linear loads is now connected instead of the linear loads of Subsection V-B. The non-linear loads absorb a power equivalent to the linear loads (same RMS current) but the current shape is now almost square (full-wave rectifier connected to an inductive load).

The results of this test are shown in Fig. 12 and Fig. 13. Similar performance when compared to the linear load case is obtained. The harmonics are absorbed by the power converter in steady state with a transient response lasting 20 ms.

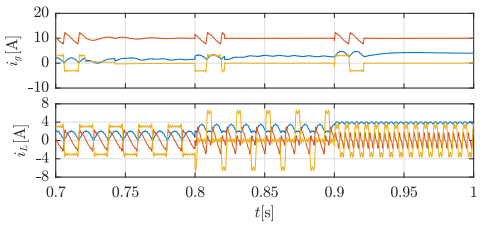

Fig. 13. Simulation results for local non-linear load connection. Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. Top, grid current in synchronous reference frame. Bottom, load current in synchronous reference frame.

D. Error from communication delays

As stated in Subsection IV-B, communication delays can affect the error of the resultant current since the output current reference is affected by the delay in the communication channel. Several cases are analyzed in order to detail the effect of this phenomenon.

In Case 1, both the central and the single-phase controllers work at the maximum frequency (10 kHz) without any delays (ideal case). This case is used as reference. In Case 2, the central and the single-phase controllers work at the nominal frequency (1 kHz and 10 kHz) without any delays (perfect real case). In Case 3, the central and the single-phase controllers work at the nominal frequency with the same random communication delay for all the single-phase controllers (quasi-random real case), using a normal distribution with a mean value of 0 (no delay) and a variance of 2% of the nominal communication period. In Case 4, the central and the single-phase controllers work at the nominal frequency with different random communication delay for each single-phase controller (random real case), using the same distribution as in Case 3.

To determine the effect of communication delays, a cumulative trapezoidal integration of the absolute value of the error is performed. This way, the area between the actual value and the reference value is calculated, so that the deviation from the reference value is obtained. Results from Case 1 are used as the reference value for the rest of the cases.

Applying the described cases to the first reactive current reference change, the results of Table II are obtained. As can be seen, the error results get worse if communication delays are considered. Nevertheless, the reference reconstruction implementation reduces the effect of delays into the system, regardless of the analyzed case.

VI. Experimental results

The modular power converter proposed during this paper is also tested experimentally. For that purpose, the experimental setup shown in Fig. 14 is used. The experimental tests analyzes four features of the modular converter: DC link voltage control, reactive power compensation, non-fundamental harmonics mitigation and negative sequence correction.

TABLE II
Cumulative error [A.ms] results from communication delays. Case 1 is used as a reference for the rest of the cases. A) Without reference reconstruction; B) With reference reconstruction.

	CASE2		CASE3		CASE4	
TIME [s]	A)	B)	A)	B)	A)	B)
0.30÷0.40	7.0	0.7	18.0	12.7	18.0	12.5
0.30÷0.32	5.9	0.4	16.3	11.1	16.5	11.2
0.32÷0.34	0.9	0.2	1.4	1.3	1.0	0.9
0.34÷0.36	0.2	0.2	0.3	0.2	0.3	0.3
0.36÷0.38	0.0	0.0	0.1	0.1	0.1	0.1
0.38÷0.40	0.0	0.0	0.0	0.0	0.0	0.0

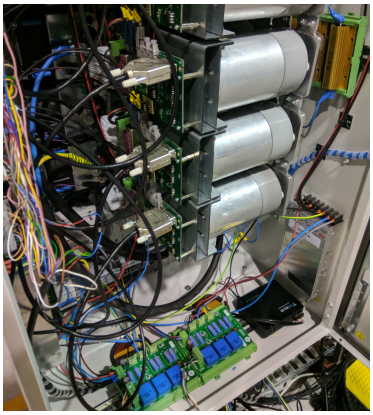

Fig. 14. Experimental setup of a modular converter with a central controller and intelligent single-phase power cells.

The DC link voltage control test is shown in Fig. 15. The reference for the DC voltage is a ramp of 1 s with a final value of 450 V (note that the grid line RMS voltage is 230 V for the experimental tests). As can be seen, the converter current phase is in reversed with respect to the grid voltage, so that active power is absorbed by the converter to charge the DC link.

The reactive power compensation test is shown in Fig. 16. The reference profile for the reactive current consists of a step from 0 A to -10 A and, after 0.4 s, another step from -10 A to $+10$ A. As can be seen, the dynamic response is quite good and there is not error at steady state.

Non-fundamental harmonics mitigation and negative sequence correction are shown in Fig. 17 and Fig. 18. As can be seen, the converter is able to inject current with non-fundamental harmonics and negative sequence to compensate the effect of non-linear/unbalanced loads connected to the grid.

Finally, a THD comparative is done between the implemented modular single-phase control and a three-phase control in dq axis, which was previously implemented in the experimental setup. The THD for the modular control is 5.02%, improving the THD for the three-phase which is 6.71%.

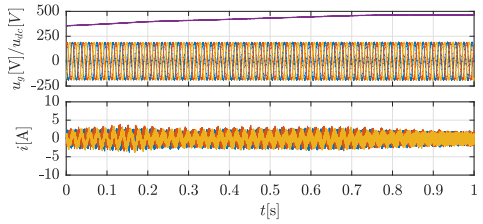

Fig. 15. Experimental results for DC link voltage control. Variables are shown in phase coordinates (abcn): blue, phase A; red, phase B; orange, phase C. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

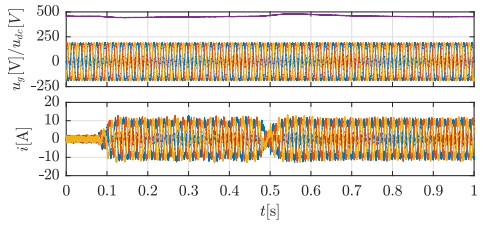

Fig. 16. Experimental results for reactive power compensation. Variables are shown in phase coordinates (abcn): blue, phase A; red, phase B; orange, phase C. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

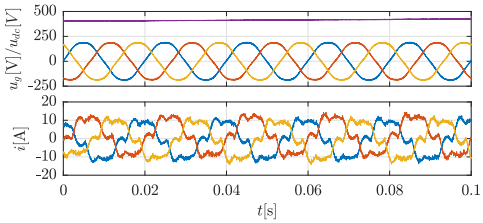

Fig. 17. Experimental results for harmonics mitigation. Variables are shown in phase coordinates (abcn): blue, phase A; red, phase B; orange, phase C. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

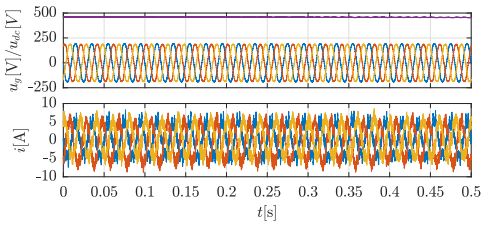

Fig. 18. Experimental results for negative sequence mitigation. Variables are shown in phase coordinates (abcn): blue, phase A; red, phase B; orange, phase C. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

VII. Conclusions

This paper has presented a distributed control alternative based on DRC which can be applied to modular power converters. The proposed alternative was tested via simulations and experimentally, obtaining proper results in terms of steady-state error and transient behavior. Communication delays, frequency shifts and harmonic compensation are analyzed, and a reference interpolator is proposed for mitigating its effects. Simulation and experimental results confirm the viability of the approach.

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B.2 Compensation Alternatives for Power Sharing Errors in Multi-Port Converters for Hybrid DC/AC Microgrids

Compensation Alternatives for Power Sharing Errors in Multi-Port Converters for Hybrid DC/AC Microgrids

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***Abstract*—This paper proposes several alternatives for the compensation of power sharing errors in the DC bus of hybrid DC/AC microgrids. The case of study consists in a multi-port converter used for the interconnection of a AC grid-tied converter, a battery, a supercapacitor and a regenerative DC load that has to be supplied. The storage elements and the load are connected by means of DC/DC converters. The power sharing between the battery and the supercapacitor is determined by using an estimation of the load power. However, due to errors in sensors or control actions of the converters, the real load power is not exactly equal to the estimated one and hence a power mismatch is produced. Those mismatches are absorbed by the DC-link voltage, which is controlled by the grid-tied converter. However, considering restrictions in the grid-tied converter, the differences in the power sharing can compromise the operation and the stability of the system. In this paper, three compensation methods are proposed and compared. The proposed methods allow for the stable operation of the system, even with noticeable errors in the power sharing.**

I. Introduction

Local small-scale power systems are being developed to promote the introduction of renewable energies, since they are closely related to distributed generation unlike the conventional ones. The concept of microgrid appears in order to categorize this type of systems, which are evolving over time [1]. Microgrids usually have some energy storage units to support the renewable power generation, which is nondeterministic. Different kind of energy storage systems can be installed, some of them being more dedicated to the energy needs (batteries), while others show their advantages in terms of power capability (supercapacitors) [2], [3]. In order to exploit the advantages of the different types of energy storage system, microgrids can use an hybrid implementation (e.g. battery and supercapacitor), so that a flexible and reliable operation is achieved [4], [5].

Batteries have relatively high energy density but they are not suitable when suffering high variations of power. This is because the internal electrochemical reactions inside the battery produce a process of degradation [6]. To face this problem, supplementary supercapacitors can be used since they work properly under high variations of power [7]–[9], though they have low energy density. Therefore, it is necessary to perform a power sharing between battery and supercapacitor [10], [11], so that the battery manages the main power exchanges (energy source) whereas the supercapacitor is in charge of the transient power variations (power source) [12]–[15].

However, any error in the calculation of the power sharing produces a mismatch, which may disturb the performance of the system. Errors in the sensors, in the estimation of the power load or in the control actions of the converters often appear during the operation of a power system. Thus, the influence of these mismatches should be analyzed in order to determine the resultant effects, which might affect the integrity of the system.

The analyzed case is a hybrid DC/AC microgrid which is composed of a DC load, a battery and a supercapacitor. The electrical diagram, which is based on the use of intelligent Power Electronics Building Blocks (iPEBB) [16], is shown in Fig. 1. An extra capacitor is connected to the DC grid to create a DC bus with an established DC voltage. Additionally, an inverter is connected to exchange energy with the AC grid. The objective of this paper is to analyze the power mismatches problem in the DC/AC microgrid and to propose several compensation alternatives.

This paper is organized as follows. In Section II, an explanation of the problems that can arise when power sharing is applied to the DC/AC microgrid is addressed. In Section III, an analysis of the different compensation techniques suited for mitigating the different issues is discussed. In Section IV and Section V, simulation and experimental results are obtained in order to validate the proposed system. Finally, in Section VI, conclusions about the accomplished work are discussed.

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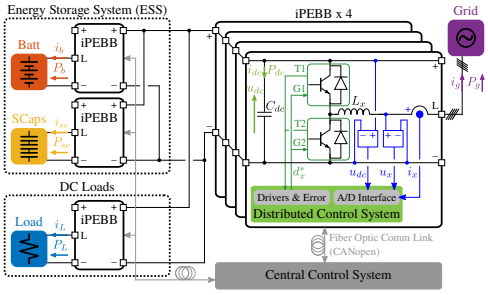

Fig. 1. Electrical diagram of the hybrid DC/AC microgrid based on the use of intelligent Power Electronics Building Blocks (iPEBB).

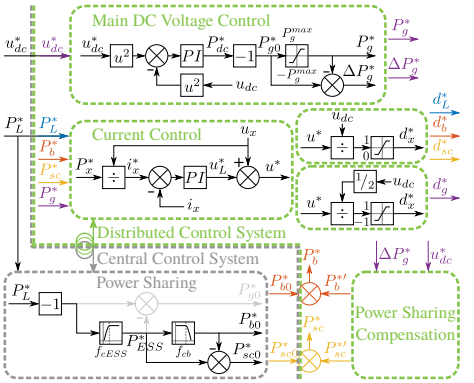

Fig. 2. Control diagram of the hybrid DC/AC microgrid. Gray units are integrated in the central control system whereas green units are integrated in the distributed control units.

II. Power Sharing Issues

The simplified DC/AC microgrid is made up of several power units interconnected by a multi-port power converter through a capacitor which creates a DC bus. The considered units are an aggregated regenerative DC load, which represents the different loads connected to the DC grid; a Li-ion battery; a supercapacitor, and a grid-tied interlinking converter connected to the AC grid (Fig. 1). In order to supply the DC load, a power sharing between the different devices of the system is done. The base load demand is provided by the AC grid, whereas the peak load demand is provided by the energy storage system (ESS): low frequency components are supplied by the battery (energy source) whereas the high frequency components are supplied by the supercapacitor (power source). By using two low-pass/high-pass filters with different cutoff frequencies, it is possible to tweak the power sharing as desired.

Fig. 2 shows the proposed control diagram to carry out the power sharing mechanism. The power sharing is computed by the central controller, which sent the initial power references (P^*_{x0}) to the current control of the different distributed control units, in order to manage the power of the different devices in the system. Still, it requires to have an accurate measurement of the power by each of the converter units. However, accuracy of the sensors or saturation phenomena in the control action of any unit will induce differences in the real power sharing.

Focusing on the DC side of the system, the power balance expression which links the different power units (load: P_L, battery: P_b, supercapacitor: P_{sc}, grid: P_g and DC bus capacitor: P_{dc}) is given by (1).

$$P_L + P_b + P_{sc} + P_g + P_{dc} = 0 \tag{1}$$

When a power mismatch occurs, (1) is not longer equal to zero. In that case, the power surplus or shortage has to be delivered/absorbed by some power units to compensate for the difference. In the present application, the DC-link capacitor acts as the buffer for it and hence the power mismatches produces a variation in the DC-link voltage. Considering the grid-tied DC/AC inverter is controlling the DC-link voltage, the variation will depend on the stiffness of that control. The variations induced in the DC-link voltage because of the power mismatch are also affected by the maximum power that can be managed by the grid DC/AC converter, since the converter can reach saturation and therefore not be able to provide the required power to maintain the DC-link voltage at an appropriate level.

Fig. 3 shows the power sharing issues which appear when the grid power is limited, so that saturation in the grid DC-link voltage controller is produced. When the grid power reaches the minimum/maximum limit, the DC-link voltage either drops to the rectifier level or rises to fault values. This way, the system operation is compromised and correction actions are required to take back DC voltages within safe values.

In order to solve this problem, it is necessary to dynamically correct power mismatches to ensure a suitable operation. Considering that power mismatches are normally a transient problem, often with fast dynamics, this paper proposes several alternative compensation methods relaying on a modified operation of the ESS.

A new control module is introduced into the control diagram (Fig. 2) with a view to performing the power sharing compensation. Extra power references ($P^{*\prime}_x$) are computed by this module and commanded together with the initial power references (P^*_{x0}) to the current control loop. Since it is required to compensate the power mismatches rapidly, the power sharing compensation is internally performed by each distributed control unit.

III. Compensation Techniques

As mentioned above, power mismatches in the power sharing produce a deviation of the DC bus voltage from the nominal value. Thus, some kind of correction has to be applied to mitigate the problem. Three different compensation techniques are proposed: 1) open loop power reference compensation,

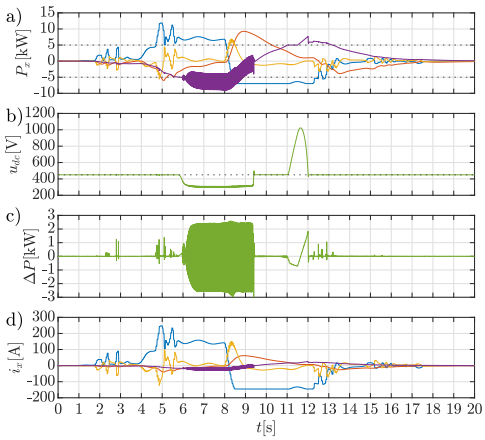

Fig. 3. Power sharing issues when the grid power is limited (−5 to 5 kW). a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Current comsumption. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus.

2) auxiliary DC voltage control and 3) closed loop power reference compensation.

The big challenge is to estimate properly the power mismatch. It would be necessary to measure the power of every unit which comprise the whole system, but this would require the installation of an extra current sensor for the load (the power generation units are already controlled so they need a current sensor) and the cost would increase. Moreover, errors in the calibration of the sensors will produce additional power mismatches since the measurements of the different variables will not be completely accurate.

Alternatively, an estimation method for the compensation power can be done by analyzing the shape of the grid DC-link voltage controller. The main (grid) DC voltage control is controlled by the grid-tied converter using a quadratic voltage control (QVC) [17] as shown in Fig. 2, so that the control action is expressed in terms of power. If saturation in the grid-tied converter is produced, the controller will not longer be able to apply the required power. The remaining power (ΔP_g^*) can be considered as the power mismatch and, under the presented control structure, is assigned to the grid-tied converter.

A. Open loop power reference compensation

The first compensation technique consists of tracking the power mismatch and trying to introduce into the system the opposite power.

The power mismatch has to be provided by the ESS since the grid-tied converter is working under saturation conditions. Since the supercapacitor is the device in charge of managing fast power variations and the battery is responsible for giving/absorbing energy, a low-pass filter is used to determine the extra references of both devices ($P_b^{*\prime}$ and $P_{sc}^{*\prime}$), using the power mismatch as an input, as shown in Fig. 4.

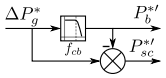

Fig. 4. Open loop power sharing compensation.

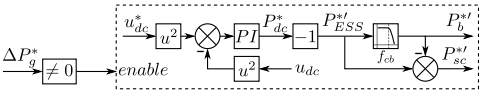

Fig. 5. Auxiliary DC voltage control.

This way, the power mismatch is mitigated and hence the DC bus voltage deviation is reduced, so that the system is kept in safe conditions.

B. Auxiliary DC voltage control

The second compensation technique consists of implementing an auxiliary DC voltage control in the ESS to support the main (grid) DC voltage control during saturation events. The proposed scheme is shown in Fig. 5. Under normal conditions, only the main DC voltage control has to be active. Therefore, it is necessary to determine the enabling strategy which triggers the auxiliary DC voltage control.

The enabling strategy is similar to the one applied for the open loop power reference compensation. When saturation is produced in the main DC voltage control, there is a power mismatch which needs to be corrected. Thus, the auxiliary DC voltage control can be enabled when saturation is detected (grid power mismatch is not zero).

The resultant control action of the auxiliar DC voltage control is the extra ESS power reference ($P_{ESS}^{*\prime}$), so a low-pass filter is used to determine the extra reference of the battery ($P_b^{*\prime}$) and the extra reference of the supercapacitor ($P_{sc}^{*\prime}$).

Two different implementations of the controller will be studied for this compensation technique: pure P controller and PI controller. The reasoning behind analyzing both controllers is that the auxilary DC voltage control is only enabled from time to time. Therefore, an integral action can be clampled to a non-zero value whenever the control is disabled, so that the performance of the PI controller could be affected.

C. Closed loop power reference compensation

Analyzing in detail the main DC voltage control, which is shown in Fig. 2, it can be observed that the grid power reference mismatch (ΔP_g^*) corresponds to the error between the desired grid power reference and the applied one.

Therefore, it is possible to implement a closed loop power reference compensation by managing this error through a PI controller, as shown in Fig. 6. This way, it is expected to improve the results obtained from the open loop power reference compensation if the controller is tuned properly.

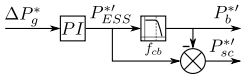

Fig. 6. Closed loop power sharing compensation.

TABLE I
SYSTEM PARAMETERS.

Parameter	Value
Filter inductor inductance (L)	1.7 mH
Filter inductor resistance (R)	0.33 Ω
DC-link total capacitance (C_{dc})	750 μF
Nominal DC-link voltage	450 V
Nominal grid line RMS voltage	245 V
Nominal grid frequency	50 Hz
Nominal grid power	5 kW
Nominal load voltage	48 V
Nominal battery voltage	150 V
Nominal supercapacitor voltage	48 V
Current control loop bandwidth	300 Hz
Main DC voltage control bandwidth	20 Hz
Auxiliary DC voltage control bandwidth	20 Hz
ESS HPF cutoff frequency (f_{cESS})	0.1 Hz
Battery LPF cutoff frequency (f_{cb})	0.5 Hz
Central control system frequency	100 Hz
Distributed control system frequency	10 kHz

The resultant control action of the closed loop power reference compensation is the extra ESS power reference ($P_{ESS}^{*\prime}$). As in the previous cases, a low-pass filter is used to determine the extra reference of the battery ($P_b^{*\prime}$) and the extra reference of the supercapacitor ($P_{sc}^{*\prime}$).

As in the case stated in Subsection III-B, a pure P controller and a PI controller will be implemented in order to perform the analysis of the closed loop power reference compensation. This way, it will be possible to observe the effects of applying an integral action in this compensation method.

IV. Simulation Results

In order to validate the different compensation techniques, several simulations are carried out in MATLAB/Simulink with the parameters described in Table I: ideal case, open loop power reference compensation, auxiliary DC voltage control and closed loop power reference compensation.

A. Ideal case

First simulation (ideal case) has neither grid power restriction nor compensation. The results are shown in Fig. 7. Due to the limited bandwidth of the main DC voltage control, there are some small DC voltage deviations during the transients. Still, the system operation is nearly ideal. However, when the grid power exceeds the maximum power, the highlighted problem shown in Section II and Fig. 3 would arise. In the following discussion, limits to the grid power are set to ± 5 kW and the proposed compensation mechanisms are analyzed and compared.

B. Open loop power reference compensation

Second simulation case is performed by enabling the open loop power reference compensation presented in Subsection III-A. Results are shown in Fig. 8. As it can be seen, now the maximum grid power is accomplished. The DC voltage has a similar evolution than in the ideal case, except when saturation is produced. In that case, the DC-link voltage variations reflect the power mismatch problem. During saturation, the main DC voltage control loop generates the estimated power mismatch which is compensated by the ESS. When comparing

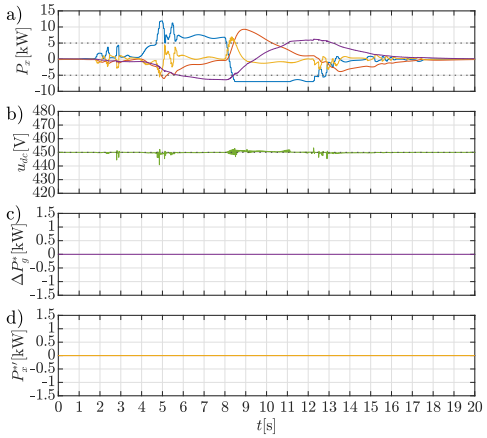

Fig. 7. Simulation results: Ideal case. a) Power consumption; b) DC-link voltage; c) Power mismatch given by grid controller; d) Extra power reference. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus.

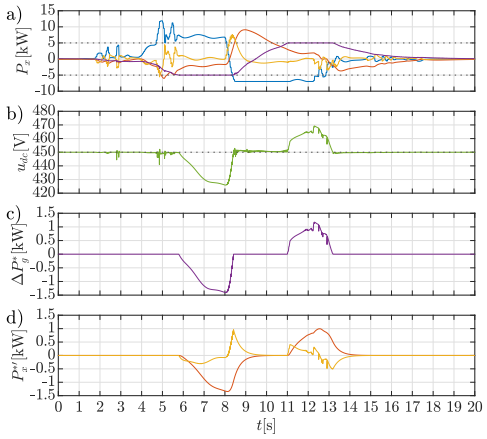

Fig. 8. Simulation results: Open loop power reference compensation. a) Power consumption; b) DC-link voltage; c) Power mismatch given by grid controller; d) Extra power reference. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus.

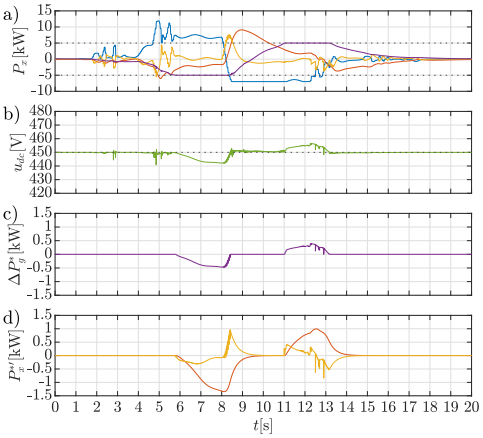

Fig. 9. Simulation results: Auxiliary DC voltage control with P controller. a) Power consumption; b) DC-link voltage; c) Power mismatch given by grid controller; d) Extra power reference. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus.

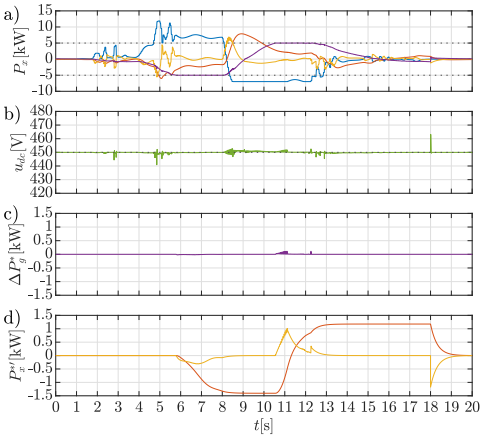

Fig. 10. Simulation results: Auxiliary DC voltage control with PI controller. a) Power consumption; b) DC-link voltage; c) Power mismatch given by grid controller; d) Extra power reference. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus.

the DC-link voltage profile with the results shown in Fig, 3, the enhanced response is quite visible.

However, although the system continues operating within proper values, there is a noticeable variation of about ± 20 V in the DC-link voltage. This is produced because this compensation method does not take into account any feedback from the system (open loop), so any parameter deviation in the system will not be mitigated.

C. Auxiliary DC voltage control

Under this compensation method presented in Subsection III-B, two controllers are considered: P and PI structures.

Third simulation is performed by enabling the auxiliary DC voltage control with a proportional controller. Results are shown in Fig. 9. In this case, voltage variations during saturation are greatly improved compared to the open-loop compensation. This is because the analyzed compensation method is now using a closed control loop with the feedback signal of the DC-link voltage, which allows a better performance of the power sharing compensation.

Nevertheless, although the voltage variations are mitigated, the DC-link voltage is not completely corrected and some error is still present. Note that since there is not integral action, the proportional gain has to be tuned in order to fulfill the maximum DC-link voltage deviation requirements. In this case, it is 3 times the gain of the main DC voltage control.

Fourth simulation relies on the use of a PI controller for the auxiliary DC voltage control with a view to reduce the maximum error in the DC-link voltage during grid saturation events. Results are shown in Fig. 10. Now, it can be observed that the integral action is being applied whenever the auxiliary DC voltage control is enabled, so that the DC-link voltage error is completely canceled. The controller gains are equal to the ones of the main DC voltage control.

However, in this case, once the grid converter comes out of saturation, the auxiliary DC voltage control is disabled and hence the integral action is fixed to a constant value. This implies that the extra power references ($P_x^{*\prime}$) sent to both the battery and the supercapacitor may be stuck to a non-zero magnitude (Fig. 10), which is undesirable in the long run.

A possible solution is to reset the integral action whenever the auxiliary DC voltage control is disabled, but this causes a deterioration in the performance of the compensation method. The implemented solution also consists in resetting the integral action, but with a delay (some seconds) after disabling the auxiliary DC voltage control. In the simulated case, the reset of the integral action is produced at 18 s (5 s after coming out of saturation, which corresponds to 500 times the integral time) so that both extra power references evolve to zero at the expense of having a short DC-link variation during this time.

D. Closed loop power reference compensation

For the closed loop reference compensation proposed in Subsection III-C, also P and PI controllers are considered. The differences between the two approaches are here compared.

Fifth simulation is performed by enabling the closed loop power reference compensation with a proportional controller with a gain of 3. Results are shown in Fig. 11. As it can be seen, the results are similar to the ones obtained in Subsection IV-C with the P controller (Fig. 9) since the DC-link voltage variations are practically the same. Note that the proportional gain in both cases has the same multiplication fac-

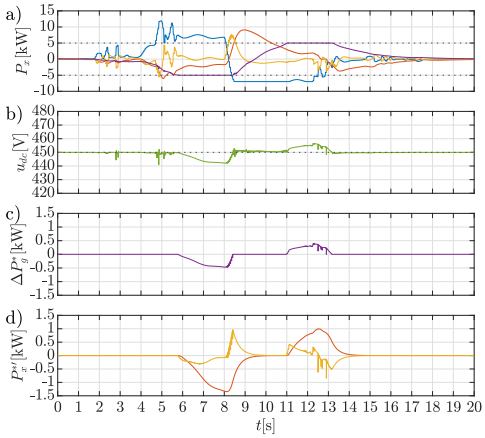

Fig. 11. Simulation results: Closed loop power reference compensation with P controller. a) Power consumption; b) DC-link voltage; c) Power mismatch given by grid controller; d) Extra power reference. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus.

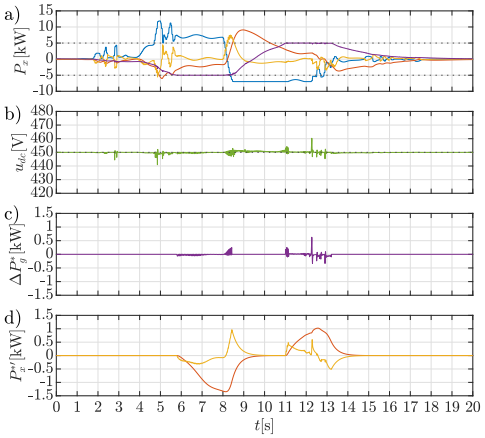

Fig. 12. Simulation results: Closed loop power reference compensation with PI controller. a) Power consumption; b) DC-link voltage; c) Power mismatch given by grid controller; d) Extra power reference. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus.

tor (3), which could explain the similarities in their behavior. Nevertheless, if using a P controller, the closed loop power reference compensation would be chosen over the auxiliary DC voltage control since it is easier to implement.

That said, the proportional gain has to be tuned in order to fulfill the maximum DC-link voltage deviation requirements since no integral action is applied in this case.

Sixth simulation relies on the use of a PI controller for the closed loop power reference compensation with a view to reduce the maximum error in the DC-link voltage during grid saturation events. Results are shown in Fig. 12. At first glance, the results seems to be similar to the ones obtained in Subsection IV-C with the PI controller (Fig. 10) if the focus is on the variation of the DC-link voltage.

However, there are noticeable differences in the extra power reference ($P_x^{*\prime}$) commands. In contrast to the case of the auxiliary DC voltage control with PI controller, the control loop power reference compensation is operating continuously and hence the extra power references of both the battery and the supercapacitor automatically recover a zero value when the grid converter comes out of saturation. This way, the ESS is not forced to give extra power when the system is not in saturation for this compensation technique. This feature together with the fact that its implementation is easier makes the closed loop power reference compensation more suitable for this system than the auxiliary DC voltage control approach.

E. Summary

An overview of the key results (maximum grid power, integral of DC voltage error, maximum DC voltage error and DC voltage overshoot) for all the simulation cases is shown in Table II. As it can be seen, in all the cases with compensation, the maximum grid power is within the expected limits.

TABLE II
OVERVIEW FOR THE DIFFERENT SIMULATION CASES.

CASE	P_{grid}^{max} [kW]	$\int$|error| u_{dc}[V.s]	|error$_{max}$| u_{dc}[V]	overshoot u_{dc}[%]
A) Ideal grid	6.4	5.3	9.1	1.2
B) OL pow ref comp	5.0	71.7	24.1	3.2
C1) Aux DC volt cont (P)	5.0	26.5	9.1	1.2
C2) Aux DC volt cont (PI)	5.0	5.5	13.2	1.8
D1) CL pow ref comp (P)	5.0	26.5	9.1	1.2
D2) CL pow ref comp (PI)	5.0	6.0	10.3	1.4

The open loop power reference compensation is the worst method for all the metrics, whereas the auxiliary DC voltage control and the closed loop power reference compensation achieve similar results. Overall, the implementations with PI controller obtain better results but their maximum voltage error (overshoot) is slightly worse when using a P controller.

Considering the integration of the auxiliary DC voltage control is more complex than the integration of the closed loop power reference, the last solution is the chosen one for the experimental validation.

V. EXPERIMENTAL RESULTS

In order to validate that the simulated results can be applied to a real system, the experimental setup shown in Fig. 13 is available for performing different tests.

The setup consists of two three-phase converters connected through the DC link (back-to-back configuration) and two inductor filters, which allow the interconnection of the different power units: AC grid, battery, supercapacitor and bidirectional load. The parameters of the experimental setup are the same

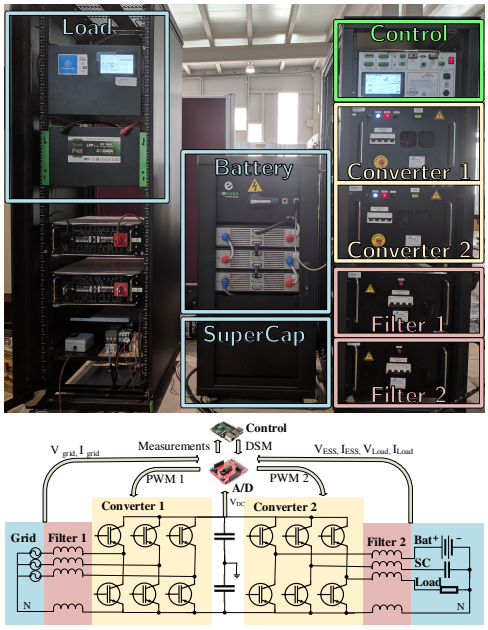

Fig. 13. Experimental setup: Front side and diagram.

as in the simulation (Table I) except the powers managed by the different power units, which are 10 times lower due to the current limitation of the converters.

The implementation of the control scheme is carried out by using two different control units: the microcontroller TMS320F28335 of Texas Instruments as the core of the distributed control system, and the single-board computed (SBC) Raspberry Pi as the core of the central control system.

Various experimental tests are carried out to demonstrate the suitability of the different compensation techniques and to address some problems that may appear during the real implementation: ideal grid, open loop power reference compensation and closed loop power reference compensation.

First experimental test verifies the results shown in Section II (Fig. 3), in which there is grid power restriction but no compensation. Results are shown in Fig. 14. As it can be seen, the DC-link voltage either drops to the rectifier level or rises to fault values when the grid power reaches the negative or positive limit.

Second experimental test is related to the simulation performed in Subsection IV-A, in which there is neither grid power restriction nor compensation. Results are shown in Fig. 15. As it can be seen, the DC-link voltage remains almost unchanged but the grid power exceeds the maximum power, so this case is not suitable for the requirements of the system.

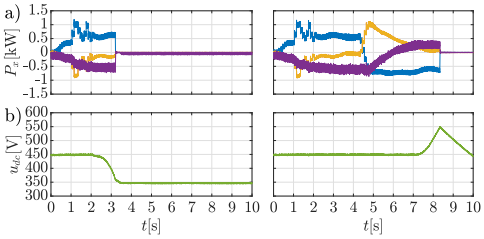

Fig. 14. Experimental results: Power sharing issues when the grid power is limited (left, negative; right, positive). a) Power consumption; b) DC-link voltage. Color legend: blue, load; orange, ESS; purple, grid; green, DC bus.

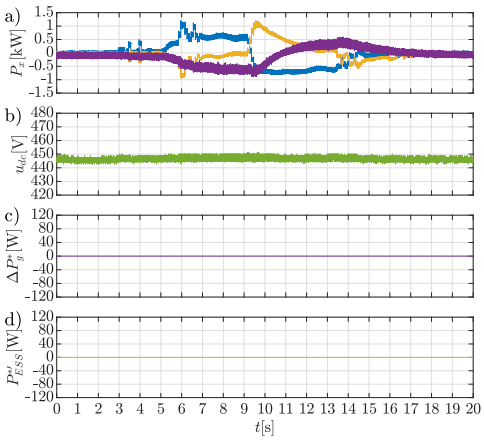

Fig. 15. Experimental results: Ideal case. a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Extra power reference. Color legend: blue, load; orange, ESS; purple, grid; green, DC bus.

Third experimental test is related to the simulation performed in Subsection IV-B, in which the open loop power reference compensation is applied. Results are shown in Fig. 16. As it can be seen, the grid power is now limited to the maximum one. When the grid control reaches saturation, the DC-link voltage varies but its reference value is recovered by applying some extra power via the energy storage system.

Fourth experimental test is related to the simulation performed in Subsection IV-D, in which the closed loop power reference compensation with a P controller is applied. Results are shown in Fig. 17. As expected, this compensation method improves the performance of the open loop power reference compensation, with a noticeable reduction in the DC-link voltage variations.

VI. Conclusions

This paper has presented some compensation techniques of power sharing error, which can be applied to the DC

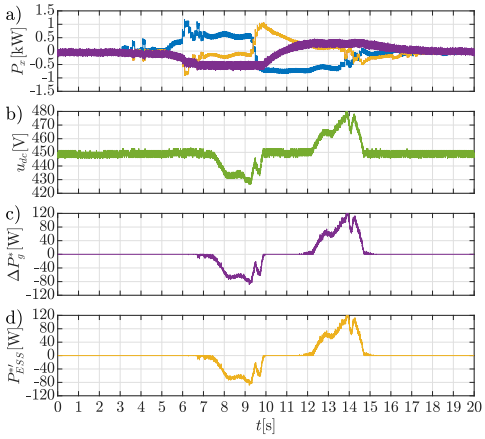

Fig. 16. Experimental results: Open loop power reference compensation. a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Extra power reference. Color legend: blue, load; orange, ESS; purple, grid; green, DC bus.

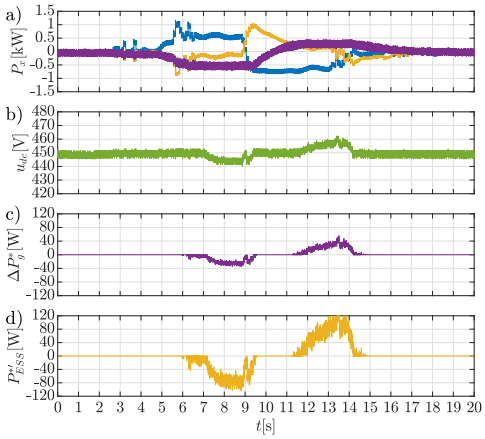

Fig. 17. Experimental results: Closed loop power reference compensation. a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Extra power reference. Color legend: blue, load; orange, ESS; purple, grid; green, DC bus.

bus of hybrid microgrids. The proposed alternatives have been tested via simulations, obtaining proper results during saturation events and transient changes. Among the presented alternatives, the closed loop power reference compensation has the best tradeoff between implementation complexity and performance. Additionally, some experimental tests have been performed to verify that the system operates properly in a real situation.

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