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Frequency-based Active Ripple Compensation Technique to Reduce Bulk Capacitance in Integrated Off-line LED Drivers

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***Abstract*—In order to increase the power density and the lifespan of LED drivers, several studies have proposed Active Ripple Compensation (ARC) techniques for minimizing the converter bulk capacitance. However, a common side-effect of the ARC method is the increase in the Total Harmonic Distortion (THD) of the converter input current. In this context, a frequency-based ARC technique is proposed as an alternative to the conventional ARC methodology, in which the duty-cycle is modulated. The analyses presented in this paper show that the frequency-based ARC approach applied to resonant converters has a better performance than the one used in hard-switching converters, since it allows for a huge capacitance reduction with a small THD increase. Furthermore, this paper presents a generalized analysis of ARC techniques applied to integrated off-line LED drivers, which reduce the number of components and the overall LED driver cost. The input current harmonic content and the output ripple reduction have been theoretically predicted for several converters. Experimental results gathered from a 96-W laboratory prototype supplied from a 127-V 60-Hz grid attested the superior performance of the frequency-based active ripple compensation, since a capacitance reduction of 66.6% has been obtained with an increase of only 0.9% in the THD.**

***Index Terms*—Active ripple compensation, capacitance reduction, high power factor, light-emitting diode (LED) drivers, resonant converter.**

I. Introduction

LIGHT emitting diodes (LEDs) have becoming the main source of artificial lighting. Features such as high luminous efficacy, h igh c olor r endering i ndex, l ow operating temperature, ability to emit white light, small size and long life make them advantageous in lighting, especially because of their potential of reducing energy consumption [1]–[4].

In order to maximize the benefits o f t he t echnology, the LED must be properly driven by an electronic circuit. This device must control the average value and ripple level of the LED current, which can significantly a ffect t he photometric performance of the LEDs [5]. Furthermore, the current ripple can cause stroboscopic and flickering e ffects, w hich c ould be noticeable to the human eye in some circumstances [6]. Thus, this undesirable low frequency (LF) ripple in the LED current is a limiting factor for solid-state lighting systems [7], [8].

The subject of LF ripple is especially important in off-line LED power supplies, since the pulsating single-phase power at the input produces a low-frequency voltage ripple at its output at a frequency twice that of line frequency. These instantaneous power oscillations are typically filtered out by electrolytic capacitors, which are known to reduce the circuit lifespan, or alternatively by using a bank of metalized film capacitors, which have better lifespan, but decrease the power density of the drivers [9], [10].

In order to mitigate these problems and to attenuate the output current ripple, some studies have proposed techniques based on alternative topologies [11], [12], on design procedures [13]–[15] or on control techniques [16]–[25]. Among the aforementioned alternatives, two-stage LED drivers, which are composed of a power control (PC) stage connected at the output of the power factor correction (PFC) stage, have been used to reduce the LF ripple. In order to reduce the component count and the driver cost, some works have proposed the use of integrated topologies, which are based on the integration of the PFC and the PC stages [15], [24].

Regarding the alternatives based on control methods, some studies rely on the reduction of the instantaneous power unbalance between the input and the output of the converter [19]–[21], [23]–[25]. This approach for capacitance minimization, also called active ripple compensation (ARC), is implemented by a large-signal modulation of the control variables of the LED driver. Although this technique usually provides good results in terms of capacitance reduction, it has the drawback of increasing the input current distortion, mainly when it is employed in pulse width modulation (PWM) converters. Thus, most of the ARC techniques proposed in the literature allows for reducing the output current ripple at the cost of an increase in the input current total harmonic distortion (THD).

In this context, this work proposes an alternative that allows for output ripple compensation with a lesser negative impact on THD: the switching frequency modulation, which can be applied to resonant power control stages, thus improving the overall LED driver efficiency by employing soft-switching [15]. Furthermore, this paper presents a more complete and generalized analysis of the active ripple compensation technique based on this large-signal modulation of the control variable in integrated off-line converters. In this way, as will be shown, the strategy of the switching frequency modulation has several advantages and can be used to design LED drivers with high efficiency and very low capacitance.

The remainder of this paper is organized as follows. Section II presents the generalized analysis of the ARC technique

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based on the large-signal modulation of the control variable. Section III addresses the design example of an integrated off-line LED driver associated to the switching frequency-based ARC technique. Section IV presents the experimental results from a laboratory prototype. Finally, the conclusions of this work are detailed in Section V.

II. Active Ripple Compensation Techniques

This section presents the study of the ARC technique based on the large-signal modulation of the control variable in integrated off-line LED drivers, comparing duty-cycle versus switching frequency modulation. The analysis carried out in this section considers that the driver is based on integrated topologies whose first stage (PFC) operates in discontinuous conduction mode (DCM), since it allows the converter to achieve a high power factor without using a loop for controlling the input current.

The effectiveness of the ARC technique when applied to integrated converters is related with the frequency response characteristic of such converters. As shown in [26], the output-to-control transfer function of an integrated converter depends only on the output stage. In addition, the operating principles of each stage are preserved although they share switches. Therefore, both stages can be discussed separately in order to simplify the analysis. First, the PFC stage with duty cycle or frequency modulation will be considered to calculate the THD. Thereafter, the values of the ARC parameters required to reduce the LF ripple in the LED current will be evaluated in the PC stage.

The line voltage can be defined by its RMS value V_G and angular frequency ω_L, as described by (1). In off-line converters, it is well-known that the main variables (*e.g.*, the output current) oscillate at twice the line frequency. Similarly to what was presented in [25], an extra control parcel at twice the line frequency has been added, thus allowing it to influence the large-signal behavior of the converter. In this way, the duty cycle and the switching frequency functions used in the analysis of this section may well be represented by (2) and (3) respectively.

$$v_g(t) = \sqrt{2}V_G \sin(\omega_L t). \tag{1}$$

$$d(t) = d_0[1 + k_d \sin(2\omega_L t + \varphi_d)], \tag{2}$$

where d_0 is the dc component, k_d the relative amplitude and φ_d is the modulation phase of duty cycle modulation.

$$f(t) = f_0[1 + k_f \sin(2\omega_L t + \varphi_f)], \tag{3}$$

in which f_0 is the dc component and k_f the relative amplitude and φ_f is the modulation phase of switching frequency modulation.

A. PFC Stage Analysis

The analysis outlined in this subsection aims to present the main topologies applied to a single-phase voltage-mode controlled power factor pre-regulators, addressing the ARC characteristics regarding each one. It is important to highlight that although uncommon, the analysis of the ARC technique presented here also considers PFC pre-regulators with variable frequency, thus allowing a comparison with duty cycle modulation. The PFC pre-regulators that operate in DCM behave like voltage-followers, which allows them to achieve a high power factor at their input. However, depending on the converter, it is not possible to have an ideal sinusoidal current at the converter input, being that non-sinusoidal current condition the case of buck and boost-type topologies. On the other hand, the buck-boost type topologies can achieve a unity power factor when operating in DCM.

Some considerations are made to simplify the analysis as follows. All input current harmonics are suppressed by the EMI filter. The modulations of duty cycle and of switching frequency are not introduced simultaneously. The dc-linked capacitor (*i.e.*, output capacitor of the PFC stage) is large enough so that the bus voltage $v_B(t)$ can be treated as a constant value, and therefore does not interfere in the THD analysis of the converter with ARC technique.

The harmonic content of the input current can be obtained by using the Fourier series. The amplitude of the h-th order harmonic component of the converter input current can be calculated by (4). In this work, the THD of the input current was chosen to evaluate the power quality of the converter, as shown in (5).

$$I_h = \frac{2}{T_L}\int_0^{T_L} \sin(h\omega_L t) i_g(t) \mathrm{d}t, \tag{4}$$

in which T_L is the line period and h is the harmonics order of the line frequency.

$$\text{THD} = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \tag{5}$$

Furthermore, the deviation of THD of PFC pre-regulators, which is calculated according to (6), represents an interesting parameter for the generalized analysis of the ARC technique.

$$\Delta\text{THD} = \text{THD}_m - \text{THD}_o, \tag{6}$$

in which THD_m is the THD of the pre-regulator with ARC technique and THD_o is the THD of the pre-regulator when the ARC technique is not used.

Table I shows the input current equations for buck, boost and buck-boost pre-regulators according to [27]. The input current of the converter with ARC technique is also affected by LF large-signal modulation of the control variable, so that the power processed by the converter is also modified according to the values of such parameters. Therefore, the PFC stage inductance, whose value can be obtained by using the third column equation of Table I, can be calculated by means of the power balance between the input and the output of the converter, as stated in (7), by considering the control variable modulation.

$$\frac{1}{T_L}\int_0^{T_L} v_g(t) i_g(t) \mathrm{d}t = \frac{P_o}{\eta}, \tag{7}$$

in which P_o is the output power and η is the global efficiency of the integrated converter.

TABLE I
EQUATIONS OF PFC PRE-REGULATORS OPERATING IN DCM

Topology	Input current of the PFC stage: i_g	PFC stage inductance design equation
buck PFC pre-regulator	$\begin{cases} \frac{d^2(\lvert v_g\rvert - v_B)}{2fL_{bu}}, & \text{if } \lvert v_g\rvert > v_B \text{ and } v_g > 0 \\ -\frac{d^2(\lvert v_g\rvert - v_B)}{2fL_{bu}}, & \text{if } \lvert v_g\rvert > v_B \text{ and } v_g < 0 \\ 0, & \text{if } \lvert v_g\rvert \le v_B \end{cases}$ (8)	$L_{bu} = \frac{\eta}{T_L P_o}\int_{t_1}^{\frac{T_L}{2}-t_1} \frac{v_g(\lvert v_g\rvert - v_B)d^2}{f}\mathrm{d}t,$ (9) in which t_1 is the instant of time given by: $t_1 = \frac{T_L}{2\pi}\sin^{-1}\left(\frac{V_B}{\sqrt{2}V_G}\right).$ (10)
boost PFC pre-regulator	$\frac{d^2}{2fL_{bo}}\left(\frac{v_g v_B}{v_B - \lvert v_g\rvert}\right).$ (11)	$L_{bo} = \frac{\eta}{T_L P_o}\int_0^{T_L} \frac{v_B d^2 v_g^2}{f(v_B - \lvert v_g\rvert)}\mathrm{d}t.$ (12)
buck-boost PFC pre-regulator	$\frac{d^2}{2fL_{bb}}v_g.$ (13)	$L_{bb} = \frac{\eta}{T_L P_o}\int_0^{T_L} \frac{d^2 v_g^2}{f}\mathrm{d}t.$ (14)

1) Buck PFC pre-regulator: The input current is proportional to the input voltage, but only within the time interval in which the rectified line voltage is higher than the bus voltage. When $|v_g(t)|$ falls below the bus voltage, the input current is zero. The period in which the input current is not zero was named as conduction angle θ. The higher the conduction angle, the closest the input current to a perfect sine waveform, and the lower the harmonic content. According to [28], a minimum conduction angle of 130^o is necessary in order to ensure the compliance with the IEC 61000-3-2 class C standard.

Fig. 1 shows the deviation of THD, defined in (6), of buck PFC pre-regulator for two values of θ. For each conduction angle, a set of curves was generated, being each one characterized by a certain value of modulation angle and plotted for several values of relative amplitude modulation (k_d and k_f). In order to ensure the average power balance of the converter, for each point on the graph a new value of the buck inductance must be calculated so that the power delivered to the load remains constant.

As can be noted in Fig. 1, the cases that presented the harmonic components of the input current above the limits of the IEC 61000-3-2 standard were highlighted in red. The ARC technique has little influence on the value of the THD when the relative amplitude of the modulation (k_d and k_f) is low, especially for modulation angles of 0^o and 180^o. On the other hand, the control variable modulation can be used to reduce the input current distortion. The highest THD reduction occurs when φ_d = 90^o in $d(t)$ modulation and when φ_f = 270^o in $f(t)$ modulation. In general, the THD of the converter is less sensitive to k_f when compared to k_d, thus allowing a larger $f(t)$ modulation. For example, with θ=150^o and φ_d=φ_f=0^o, ΔTHD=4% (*i.e.*, THD=20%) is obtained when k_d=11% or k_f =25%. As mentioned before, a minimum conduction angle of 130^o is necessary for the conventional buck PFC pre-regulator in order to ensure the compliance with the IEC 61000-3-2 class C standard. However, the value of this angle can be reduced with the ARC technique, i.e., the buck PFC pre-regulator with ARC can be used in applications that demand higher output voltages.

2) Boost PFC pre-regulator: The input current of the PFC boost operating in DCM depends on the value of the bus

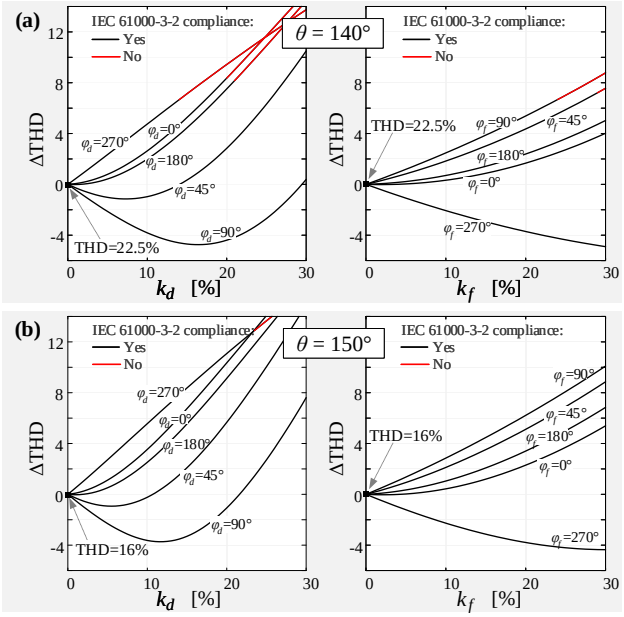


Fig. 1. Deviation of THD for buck PFC pre-regulator operating in DCM with ARC technique modulating duty-cycle or switching frequency, considering a conduction angle of (a) θ = 140^o and (b) θ = 150^o.

voltage and therefore of the dc static gain (V_B/V_G). According to [15], the converter only meets the requirements of the IEC 61000-3-2 class C standard if the dc static gain is larger than 1.27. Similar to the buck converter analysis, the ΔTHD of boost pre-regulator with ARC technique for some values of V_B/V_G was presented in Fig. 2. For each dc static gain, a set of curves was generated, being each one characterized by a certain value of modulation phase and plotted for several value of relative amplitude modulation. For each case in the graph the boost inductance is recalculated by (12) to keep the output power constant.

As verified in the buck converter, the input current distortion can be reduced by the control variable modulation, especially when φ_d = 90^o in $d(t)$ modulation and when φ_f = 270^o in $f(t)$ modulation. The results show that the deviation of the THD of boost pre-regulator can increase as the relative amplitude of

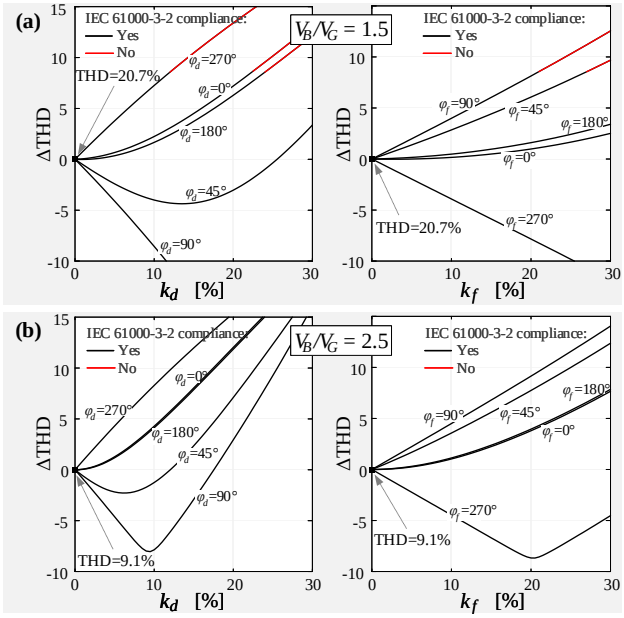


Fig. 2. Deviation of THD for boost PFC pre-regulator operating in DCM with ARC technique modulating duty-cycle or switching frequency, considering a dc static gain of (a) V_B/V_G = 1.5 and (b) V_B/V_G = 2.5.

modulation grows. However, this variation is smaller for $f(t)$ modulation when compared to $d(t)$ modulation. It is important to highlight that boost PFC pre-regulator with ARC technique can also meet the requirements of the IEC 61000-3-2 class C standard with the dc static gain less than 1.27 if the purpose is not capacitance reduction.

3) Buck-boost PFC pre-regulator: Differing from the buck- and boost-type pre-regulators, the input current shape of the buck-boost PFC operating in DCM does not depend on the bus voltage. Therefore, the input current waveform is ideally sinusoidal if the duty cycle and the switching frequency are kept within a half line cycle.

Fig. 3 shows the ΔTHD of buck-boost pre-regulator with ARC technique for several values of k_d and k_f, keeping the output power constant. Since the input current waveform is assumed sinusoidal, the deviation on THD for buck-boost pre-regulator always increases as the relative amplitude of large-signal modulation from ARC grows. The figure s hows that the input current distortion does not depend significantly on the modulation angle when a large-signal modulation of the switching frequency is used. In addition, k_d has a greater influence t han k_f o n ΔTHD.

This subsection compared the more conventional and known ARC approach of duty-cycle large-signal modulation with a novel ARC technique based on the switching frequency large signal modulation, both applied to the three basic PFC pre-regulator topologies operated in DCM. The analyses showed that the $f(t)$ modulation has a lower impact on the power quality when compared with the duty cycle modulation. Furthermore, the large-signal modulation of the switching frequency can be used for the purpose of power quality improvement, which allows for the use of buck and boost topologies in compliance with the IEC 61000-3-2 class C standard over

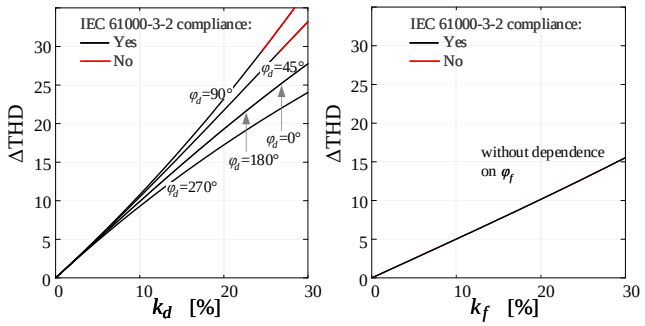


Fig. 3. Deviation of THD for buck-boost PFC pre-regulator operating in DCM with ARC technique modulating duty-cycle or switching frequency.

a wide voltage gain range (V_B/V_G), or, as proposed in this paper, aiming the capacitance reduction in order to increase the power density and the lifespan of LED drivers. Regarding capacitance reduction, the LF ripple transmission must also be analyzed, thus the ART technique can be evaluated according to the input current distortion and to the LF output current ripple in integrated off-line LED drivers.

B. PC Stage Analysis

This subsection presents how the deliberate modulation of the control variable impact the LF ripple transmission of the converters used as a PC stage. First, a converter sensitivity analysis will be presented in order to show the behavior of the converters with the control variable modulation. Thereafter, the values of the ARC parameters required to reduce the LF ripple will be measured and related to the THD analysis shown in the previous subsection.

Because in many drivers the bus voltage is significantly larger than the output voltage, step-down converters are tipically employed as the second stage in off-line LED drivers. Three topologies are studied in this section: buck and buck-boost operating in DCM, as well as LLC resonant converter with frequency modulation, which is a converter fairly common in off-line medium- and high-power LED drivers and has become an industry standard in these off-line applications. In order to produce more generalized results, some parameters of the LLC converter were normalized as follows:

- Q is the normalized AC-side load resistance;
- λ is the inductance ratio, which can be found by dividing the series inductance by the magnetizing inductance;
- ω_n is the normalized design switching frequency;

In order to investigate the behavior of the output voltage of the converters, the normalized output voltage was evaluated for variations of the control variable, as shown in Fig. 4. The ARC technique was disregarded in this analysis (k_d=k_f=0). In addition, the normalized control variables were defined as $c_d = D/D_{nom}$ and $c_f = f/f_{nom}$ for variations in the duty cycle and switching frequency, respectively. Fig. 4(a) presents the behavior of the normalized output voltage V_o/V_{nom} of the buck and buck-boost converter designed for the same operating point (nominal duty cycle D_{nom} and nominal output voltage V_{nom}). Both converters present a quasi-linear behavior and have very similar curves and sensitivities.

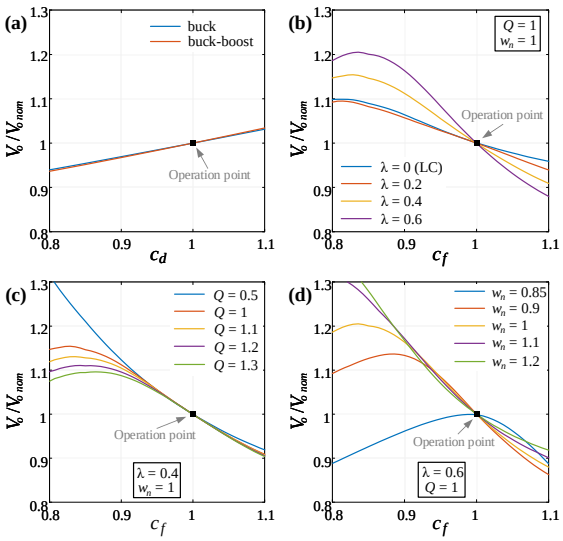


Fig. 4. Normalized output voltage of converters as PC stage. (a) buck and buck-boost converters; (b) LLC resonant converter for variations of λ; (c) LLC resonant converter for variations of Q and (d) LLC resonant converter for variations of ω_n.

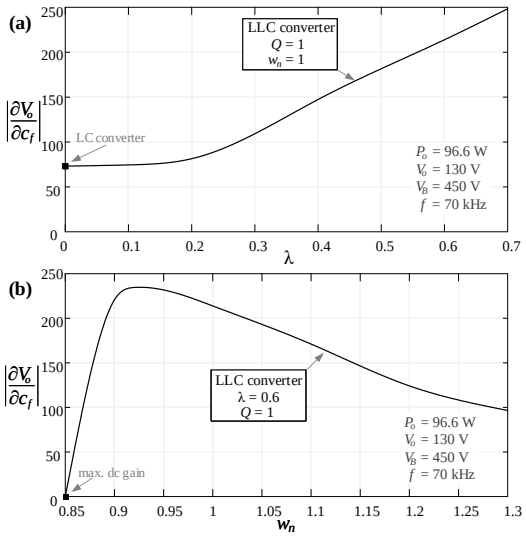


Fig. 5. Sensitivity analysis of the LLC converter used as the PC stage for several values of (a) λ and (b) ω_n.

Fig. 4(b) shows the normalized output voltage of the LLC converter according to variations in the switching frequency for several values of λ. The results show that at the operating point the curve slope (*i.e.*, parametric sensitivity) increases as the inductance ratio grows. The lowest output voltage sensitivity occurs when $\lambda = 0$, which is a specific case of the LLC converter known as LC series resonant converter. It is important to highlight that the curves were obtained from the design methodology and the accurate modeling for an LLC resonant converter proposed in [29], which is able to accurately predict the LED current.

Fig. 4(c) depicts the normalized output voltage for several values of Q. As can be seen, the impact of the quality factor becomes negligible around the operating point. Fig. 4(d) presents the normalized output voltage according to variations in the switching frequency for several values of normalized design switching frequency. As expected, the LLC converter operates very close to the maximum dc gain as ω_n reduces, a case that should be avoided to ensure operation under zero voltage switching (ZVS) conditions (inductive tank characteristic). On the other hand, the LLC converter is typically designed to operate at the series resonant frequency (ω_n=1), thus obtaining greater efficiency and better power quality. This case allows a wide variation of the switching frequency value while preserving the ZVS operation. In this sense, Fig. 4 shows that the inductance ratio has a major influence on the LLC converter sensitivity.

In order to quantify the sensitivity related to converters used as PC stage, a case with P_o = 96.6 W, V_o = 138 V, V_B = 450 V and $f(t)$ = 70 kHz was investigated considering the converters evaluated in Fig. 4. The sensitivity can be calculated as the partial derivative of the LLC average output voltage with respect to the normalized switching frequency, which is denoted as $\partial V_o/\partial c_f$. Fig. 5(a) shows the sensitivity analysis in absolute values for several values of inductance ratio. As can be seen, the sensitivity of the LLC converter increases as λ grows. Fig. 5(b) shows the sensitivity analysis in absolute values for several values of ω_n. When the LLC converter is operating close to the maximum dc gain, the sensitivity increases as ω_n grows. However, in the region in which the converter is usually designed to operate, this sensitivity reduces with increasing normalized frequency.

Regarding the hard-switching dc-dc converters, the sensitivity to duty cycle can be obtained by the partial derivative of the output voltage with respect to the normalized duty cycle ($\partial V_o/\partial c_d$). In this way, the sensitivity to duty cycle of the buck and buck-boost converter are constant and equal to 43 V and 46 V, respectively. Although uncommon, the $f(t)$ modulation was also evaluated in the hard-switching topologies ($i.e.$, buck and buck-boost). In these examples, $|\partial V_o/\partial c_f|$ of the buck and buck-boost converter are equal to 22.1 V and 23.5 V, respectively. Therefore, these hard-switching converters have a sensitivity to $d(t)$ modulation approximately twice that to $f(t)$ modulation. On the other hand, load-resonant converters can be considered more sensitive than hard-switching converters, thus requiring a lower relative amplitude modulation - thus a lower control effort - for achieving the same ripple reduction.

Finally, the previously studied converters were evaluated with the ARC technique in order to show the effect of large-signal modulation on the output ripple reduction. Table II shows k_d and k_f modulation amplitudes required to reduce the LF ripple in the LED current for several cases of dc-dc converters used as a PC stage. These converters are supplying an LED lamp with dynamic resistance r_d = 12 Ω and nominal threshold voltage V_t = 129.6 V. The values of the average output current and the output current ripple were 700 mA for this analysis when k_d and k_f are equal to zero, thus obtaining a LF current ripple of 100%. The value of the bus ripple that ensures the low-frequency ripple criterion was chosen for each converter. In order to obtain the maximum ripple reduction, the modulation phase was chosen so that $d(t)$ is completely out of phase with the ac portion of the bus voltage of the

TABLE II
PARAMETERS OF ARC TECHNIQUE (k_d OR k_f) FOR OUTPUT RIPPLE REDUCTION

relative amplitude of the modulation (%)		PC stages	$\Delta I_{o\%}$ 100%	75%	50%	25%
	k_d see (2)	buck	0%	7%	13%	20%
		buck-boost	0%	6.7%	13.5%	20.5%
	k_f see (3)	buck	0%	14%	27.5%	40%
		buck-boost	0%	14%	27.5%	39.8%
		LC (λ = 0)	0%	2%	4.2%	6.8%
		LLC (λ = 0.2)	0%	1.5%	2.5%	4%
		LLC (λ = 0.4)	0%	0.75%	1.5%	2.2%
		LLC (λ = 0.6)	0%	0.5%	1%	1.5%

TABLE III
ΔTHD OF INTEGRATED CONVERTERS WITH ARC TECHNIQUE FOR $\Delta I_{o\%}$=50%

PC stages	control variable	ΔTHD - see (6) buck PFC	boost PFC	buck-boost PFC
buck	duty cycle	5.4%	6.5%	12.8%
buck-boost		5.7%	6.9%	13.3%
buck	frequency	5.9%	6.8%	13.9%
buck-boost		5.9%	6.8%	13.9%
LC (λ = 0)		0.26%	0.22%	2.1%
LLC (λ = 0.2)		0.13%	0.08%	1.25%
LLC (λ = 0.4)		0.06%	0.03%	0.75%
LLC (λ = 0.6)		0.04%	0.02%	0.5%

hard-switching dc-dc converters. In other words, φ_d = 0% since the phase of the ac portion of the bus voltage is equal to 180^o. Regarding the switching frequency modulation, the modulation phase was chosen so that $f(t)$ is in phase with the ac portion of the bus voltage, *i.e.*, φ_f = 180^o.

The results show that ARC technique has a better performance in terms of ripple reduction in converters with higher sensitivity. For example, the output current ripple of 50% is obtained when k_d = 13% for the buck converter and k_f = 1% for the LLC resonant converter with λ = 0.6. For the same output current ripple, load-resonant converters with frequency modulation require a lower relative modulation amplitude when compared to conventional converters.

In order to show the behavior of the THD of integrated converters with PC stages listed in Table II, the parameters of ARC technique for an output ripple of 50% were evaluated according to subsection II-A and the values of ΔTHD are given in Table III for each combination of PFC and PC stages. For example, by considering the PFC buck-boost integrated with the buck, the output current ripple of 50 % is obtained with a duty cycle modulation that generates a THD increase of 12.8%. On the other hand, the same output ripple is obtained with ΔTHD of only 0.5% if the LLC resonant converter with λ = 0.6 is used as PC stage with frequency-based ARC. Regarding the hard-switching converters, although k_f is higher than k_d, the values of ΔTHD are similar since the $f(t)$ modulation has a lower impact on the THD when compared with the $d(t)$ modulation. Thus, the ARC technique applied to the switching frequency is also an alternative for the evaluated non-resonant converters, although the design of such topologies with a large frequency modulation can be somewhat difficult and can actually increase the volume of some passive elements. On the other hand, when a load-resonant PC stage is used, the frequency-based ARC is an excellent alternative, since it allows for a large capacitance reduction with a very small impact on the THD. This occurs owing to the high modulation sensitivity of those topologies. Furthermore, these converters have higher efficiency when compared to hard-switching converters.

In low-power applications, when the designer pursues simpler topologies composed of only one stage, the duty cycle modulation can be more interesting. On the other hand, the proposed frequency-based ARC yields better results when two-stage converters are needed since it allows for a huge capacitance reduction while maintaining a low input current distortion and a high overall efficiency.

III. CASE STUDY OF AN OFF-LINE LED DRIVER WITH ARC TECHNIQUE IN THE SWITCHING FREQUENCY

This section presents a design example of an integrated off-line LED driver with frequency-based ARC. The topology chosen in this work was obtained by integrating a totem-pole bridgeless boost PFC and a half-bridge LC series resonant converter, as illustrated in Fig. 6, which is referred by BBLC in this paper. It is worth noting that the topology chosen for the PC stage is the one with the lowest sensitivity among the LLC converters evaluated in the previous section, being considered the worst case of load-resonant converters, which have high efficiency. In other words, this topology needs a higher modulation amplitude for capacitance reduction, thus resulting in higher input current distortion. Therefore, this converter was chosen in order to show the higher influence of the frequency modulation on the input current of the integrated off-line LED drivers based on load-resonant converters.

The PFC stage was devised to operate in DCM, since in this condition, the circuit achieves a high power factor (PF) at the driver ac input. The duty cycle of this converter is 0.5 in order to obtain a symmetrical switching in the second stage. Moreover, the average bus voltage must be chosen in compliance with the condition given by (15) to ensure the DCM operation in the PFC stage.

$$v_B(t) > \frac{\sqrt{2}V_G}{1-D}. \tag{15}$$

The PC stage operates above the series resonant frequency, thus resulting in ZVS and high efficiency. As can be seen in Fig. 6, the ARC approach requires an additional compensator branch, C_{bp}, and one voltage sensor for its proper operation as compared to a typical control technique. The compensator C_{av} is used to synthesize the value of f_0 while the block C_{bp} generates the oscillating portion of $f(t)$ in phase with the ac portion of the bus voltage.

The design of the BBLC converter using the ARC technique must be performed in three steps. First, the passive elements of the PC stage (L_s and C_s) and the parameters of the switching frequency function (f_0 and k_f) must be obtained. Thereafter, the PFC stage design must be carried out. Finally, the control loop is designed so that $f(t)$ assumes the desired profile.

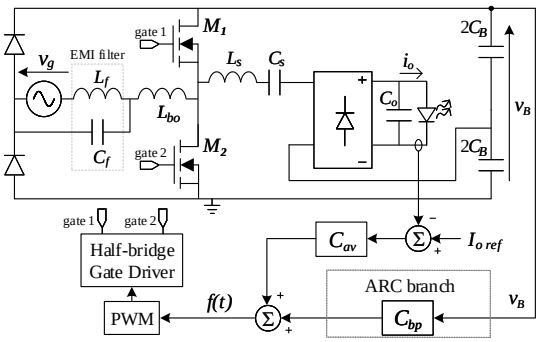


Fig. 6. Integrated Off-line LED driver based on the LC resonant converter with ARC technique in the switching frequency.

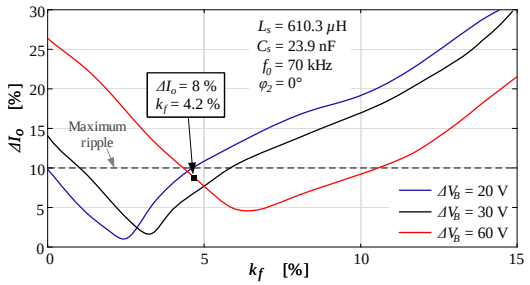


Fig. 7. Behavior of the peak-to-peak output current ripple according to k_f for several values of ΔV_B.

A. Design of the PC stage and the Frequency Modulation

Table IV shows the design parameters of the example converter. The design of the PC stage's elements is done by following the procedure outlined in [29] and by considering a design switching frequency f_d. Since the LC series converter is a specific case of the LLC converter, the mathematical model presented in [29] can be used considering the turns ratio equal to 1 and the inductance ratio equal to 0. Therefore, by using the design parameters of the converter listed in Table IV, the values of C_s = 23.9 nF, L_s = 610.3 μH, f_0 = 70 kHz and bus voltage ripple ΔV_B = 20 V can be found.

Since the capacitance reduction is associated with an increase in the bus voltage ripple, the relative amplitude of the modulation can be designed by adopting a graphical evaluation of the output current behaviors according to variations of ΔV_B and k_f. Fig. 7 shows the behavior of the relative output current ripple generated and plotted as a function of k_f for several values of ΔV_B. The graphs were obtained by solving the accurate modeling proposed in [29] using the values of C_s, L_s, ΔV_B as well as the parameters of the frequency modulation. As can be noted in Fig. 7, if the ARC technique was not used (k_f = 0), bus ripples higher than 20 V would be insufficient for meeting the design requirement of maximum ripple. In other words, lower capacitances can be employed only by using the $f(t)$ modulation. Thus, by choosing k_f = 4.2%, the desired ripple criterion is achieved for a bus ripple of ΔV_B = 60 V, which yields an output current ripple of 8% (56 mA peak-to-peak).

TABLE IV
DESIGN PARAMETERS BASED ON AN LLC TOPOLOGY [29]

Symbol	Description	Value
V_G	line voltage	127 V
ω_L	Angular line frequency	2π60 rad/s
V_B	Average bus voltage	450 V
Q	Normalized ac-side load resistance	1
λ	Inductance ratio	0
ω_n	Normalized switching frequency	1.2
f_d	Design switching frequency	50 kHz
V_t	Nominal threshold voltage of the LED lamp	129.6 V
r_d	Dynamic resistance of the LED lamp	12 Ω
I_o	Average output current	700 mA
V_o	Average output voltage	138 V
P_o	Output power	96.6 W
ΔI_o	Maximum LF LEDs current ripple	70 mA (10%)
η	Estimated efficiency	92 %

B. Design of the PFC stage

As long as the switching frequency function has been defined, the PFC stage can now be designed. According to [15], the PFC stage can be treated as a conventional boost DCM PFC for each line half-cycle, which simplifies the analysis and design of the converter. Therefore, the input current of the off-line converter is given by (11), in which $d(t)$ is equal to the duty cycle constant value, also denoted by D. In order to ensure the average power balance of the converter, L_{bo} can be calculated by (12), which yields a boost inductance of 413 μH.

The bus capacitance C_B can be calculated as outlined in [15]. According to this work, the bus capacitance can be written as:

$$C_B = \frac{\Delta Q_{CB}}{\Delta V_B}, \tag{16}$$

where ΔQ_{CB} is the amount of charge injected in (or extracted from) the bus capacitance during each quarter of line cycle.

By considering that the input is a 127-VAC/60-Hz mains and by using the design parameters of the converter listed in Table IV, the bus capacitance can be calculated as 11 μF. It is important to highlight that, if the ARCT was not used (*i.e.,* k_f = 0), a capacitance of ca. 33 μF should be used for achieving a similar ripple at the output. Therefore, the modulation of the switching frequency allowed for a capacitance reduction of 66.6 % when compared to the conventional approach without modulation. In addition, for the chosen operating point, the total harmonic distortion of 9.15% was increased by only 0.25%, yielding a theoretical THD of 9.4% in accordance with Fig. 2(b).

C. Design of the Control Loop

Since the passive elements and the switching frequency function have been defined, the control circuit can be designed. The transfer function of C_{av} is shown in (17). As it can be noted, this compensator is an integrator, which ensures that the system will have null steady-state error under constant current reference. Furthermore, the crossover frequency (f_{co}) of this transfer function must be tuned so that the output of the C_{av} block does not present any a.c. component in steady-state, *i.e.*,

C_{av} must attenuate all the oscillating components of the error signal. In addition, the negative signal is used here since, in the case of resonant converters, the circuit gain reduces as long as the amplitude of the control variable, which is the switching frequency, increases.

$$C_{av}(s) = -\frac{K_a}{s}. \tag{17}$$

In order to ensure a good attenuation at 120 Hz, a K_a = 8.17 Hz was chosen, resulting in a crossover frequency of ca. 1.3 Hz, which is two decades below $2\omega_L$.

The expression for C_{bp} was obtained based on a narrow-band second-order band-pass filter, as shown in [25]. This element was tuned with a center angular frequency of $2\omega_L$, which ensures that the oscillating component of $f(t)$ is tracked at the desired frequency. In addition, the desired phase of the modulation signal is also ensured, since the filter phase at the tuned angular frequency is null. Therefore, the transfer function of C_{bp} is given by (18), in which K_{bp} is the gain at center frequency and B is the filter bandwidth. The gain K_{bp} must be calculated by considering the amplitude of the bus voltage at the frequency of interest ($2\omega_L$). Thus, the desired oscillating portion of $f(t)$ can be obtained by (19), which was derived from the analysis of the control diagram of Fig. 6.

$$C_{bp}(s) = K_{bp}\frac{Bs}{s^2 + Bs + 4\omega_L^2}. \tag{18}$$

$$K_{bp} = \frac{2f_0 k_f}{\Delta V_B}. \tag{19}$$

Therefore, by replacing the design results obtained in (19), the calculated value of K_{bp} is equal to 101.5 Hz/V. Finally, the filter bandwidth was chosen as 20 rad/s in order to obtain a proper attenuation of the undesired frequencies.

It is important to highlight that owing to the simplicity of the control structure used in the ARC approach (see Fig. 6), its implementation could be performed by using a simple microcontroller or even by means of analog filters and control circuitry. In order to enable an easier tuning of parameters for the lab prototype, the control system of this work was implemented digitally.

IV. Experimental Results

In order to verify the theoretical analysis, a laboratory prototype was built, which is shown in Fig. 8. Table V presents the main elements used in the prototype.

Fig. 9 presents some experimental waveforms from the off-line LED driver based on the LC resonant converter employing the frequency-based ARC technique with C_B = 11 μF / 480V (Fig. 9a) compared with the same circuit without the large-signal modulation of the switching frequency (Fig. 9b), and also with the conventional approach (no active compensation) with a bus capacitance of 33 μF / 460V (Fig. 9c). The low-frequency output current ripple obtained from this experiment was 58 mA, which is quite close to the 54 mA from theoretical prediction. In addition, Fig. 9b depicts a larger ripple when the ARC technique is not used with the same bus capacitance of 11 μF, being necessary an additional value of 22 μF (Fig. 9c) to decrease the output current ripple to a similar level to the one obtained when the ARC technique is employed. The experimental results of the LED driver without ARC were obtained by using only the pure integrator shown in (17), which ensures that the system will have null steady-state error under constant current reference.

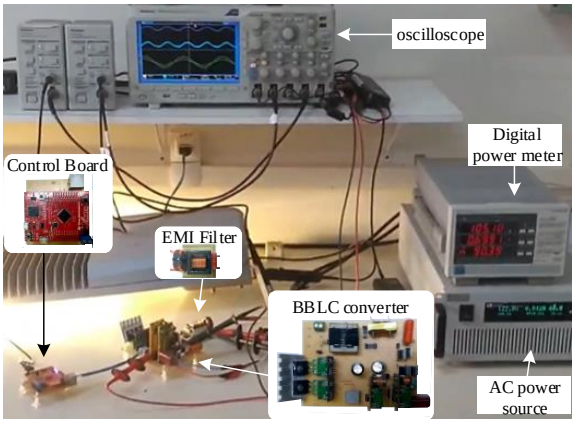


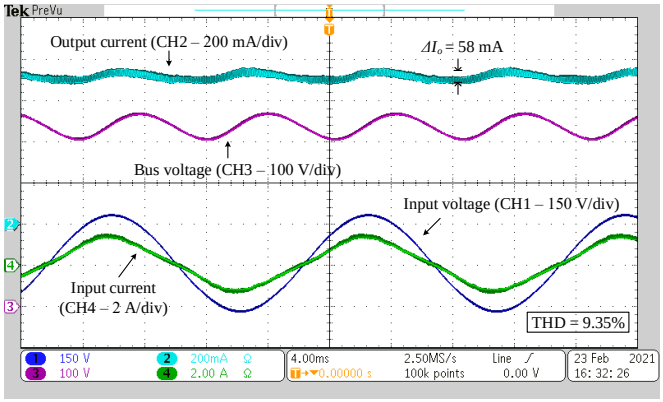
Fig. 8. Photograph of the experimental setup, showing each part of the prototype and the corresponding boards and components.

TABLE V
Main Parameters of Prototypes

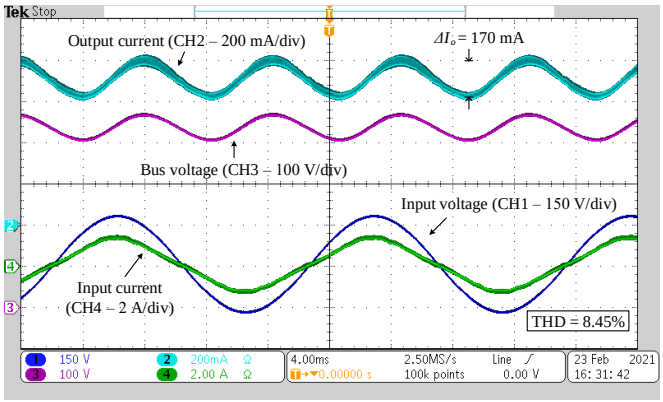
Item	Value
Half-bridge switches	2 x IRFP460 (500V / 0.25Ω)
Boost diodes	2 x MUR360S / (600V / 3A)
Boost inductor L_b	413 μH / NEE 30-15-14 / 53T gap = 0.48 mm / 4xAWG 28
Bus capacitors	22 μF / 400V Electrolytic capacitor equivalent C_B = 11 μF
Resonant inductor L_s	610.2 μH / NEE 30-15-7 / 53T gap = 0.16 mm / 3xAWG 28
Resonant capacitor C_s	22 nF / 250V Ceramic capacitor
Diode Bridge	4 x IDT02S60C (600V / 2A)
Output capacitor C_o	4.4 μF / 250 V Ceramic capacitor
EMI Filter	CM:5 mH / DM: 470μH / 220nF
Microcontroller	TI TM4C123G

It is important to highlight that, as shown in Fig. 9, the output current ripple of the circuit with low-frequency large-signal modulation of the switching frequency is lower than the conventional approach (i.e, without ARC) imposing little increase of the input current distortion. As it can be seen, experimental results showed that ARC technique increased only 0.9% the total harmonic distortion of the input current, when compared with the conventional approach. In addition, this distortion was predicted during the design procedure so that the harmonic content of the input current remains in compliance with the IEC-61000-3-2 standard, as presented in Fig. 10. The other harmonics were not depicted in Fig. 10 because their values were negligible. As can be noted, the experimental results of the input current are also close to the values obtained in the theoretical analysis. The measured THD was 9.35%, which is very close to the 9.4% predicted by the analysis. The measured PF of the BBLC with ARC technique was 0.986.

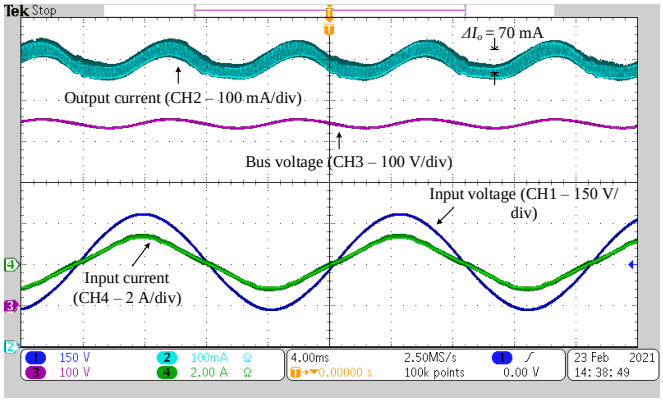
Fig. 11 presents experimental waveforms of the current and



(a) C_B = 11 µF with ARC



(b) C_B = 11 µF without ARC



(c) C_B = 33 µF without ARC

Fig. 9. Experimental waveforms obtained (a) with ARC and C_B = 11 μF; (b) without ARC and C_B = 11 μF; (c) without ARC and C_B = 33 μF.

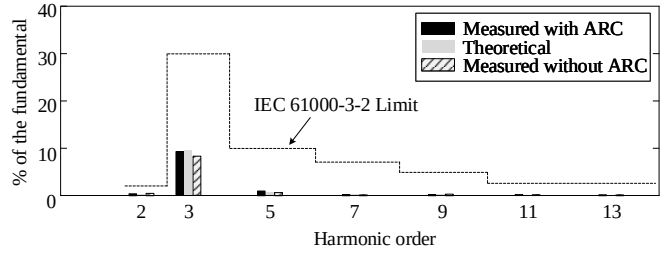
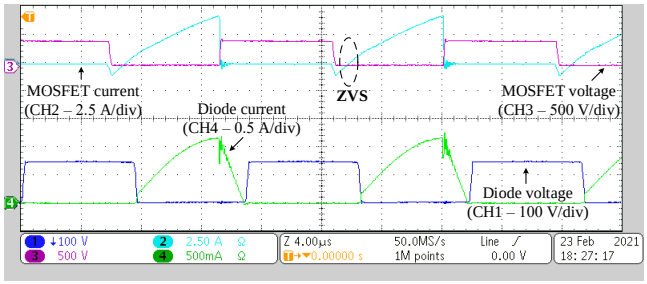
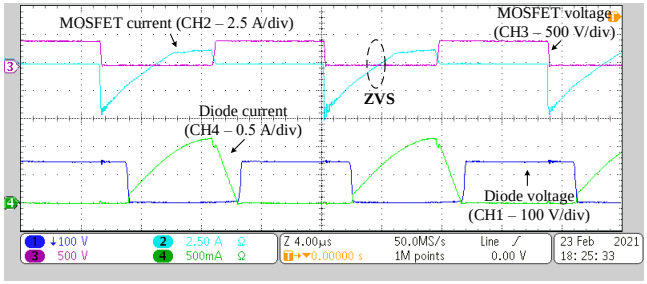


Fig. 10. Harmonic content of the input current compared with IEC limits

voltage of the MOSFET M_1 and the output rectifier diode at the positive (Fig. 11a) and negative (Fig. 11b) peak of line



(a)



(b)

Fig. 11. Waveforms measured at the (a) positive and (b) negative peak of line voltage. Diode voltage (CH1 - 100V/div), MOSFET M1 current (CH2 - 2.5A/div), MOSFET voltage (CH3 - 500V/div) and diode current (CH4 - 500mA/div). Horiz. scale: 4 μs/div.

TABLE VI
MEASURED LOSS DISTRIBUTION

Components	Values
EMI filter	0.32 W
MOSFETs switching loss	0.94 W
MOSFETs conduction loss	0.76 W
Input diodes	2 W
L_{bo}	1.3 W
C_B	0.46 W
C_s	0.8 W
L_s	1.6 W
Output diode bridge	1.8 W
C_o	0.2 W
Total	10.18 W

voltage. These waveforms show that the converter operates above series resonant frequency and with ZVS. Table VI shows the measured loss distribution in the prototype, which was obtained at nominal input voltage and rated load. Furthermore, those measurements did not take into account the consumption of the control board.

Fig. 12 presents the output current ripple, THD, and efficiency of the converter according to variations in the input voltage. The results show that the output ripple (Fig. 12a) of the driver with frequency-based ARC technique was much smaller over the entire range, with a small increment of THD (Fig. 12b). It is important to highlight that the influence of the frequency modulation upon the efficiency (Fig. 12c) is negligible for variations in the input voltage.

The behavior of the output current ripple, THD and efficiency owing to variations in the output power is presented in Fig. 13. The results showed that the converter with frequency modulation ensured a small current ripple for all the analyzed

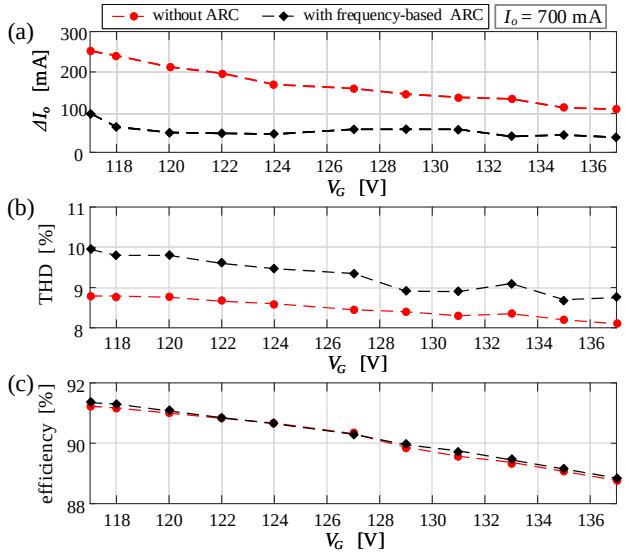


Fig. 12. Output ripple, THD and efficiency of the converter according to variations in the input voltage.

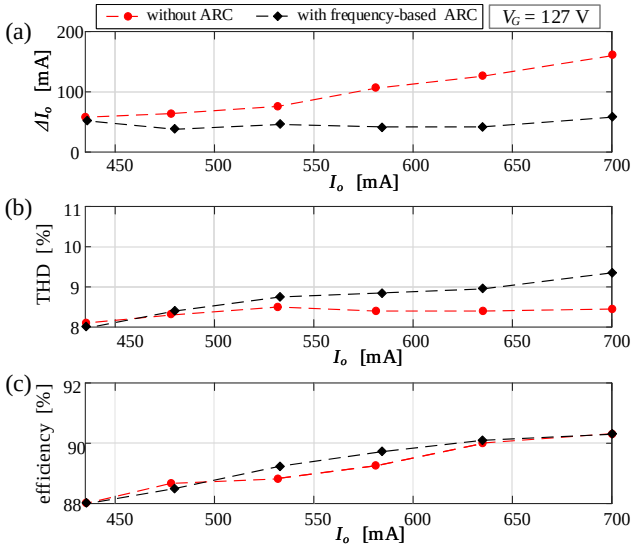


Fig. 13. Output ripple, THD and efficiency of the converter according to variations in the output power.

levels. In addition, the influence of the frequency-based ARC upon the THD and efficiency can be considered negligible for variations in the output power.

Table VII shows a brief comparison among the proposed frequency-based ARC and control techniques devised to reduce bulk capacitance in off-line LED drivers, highlighting deviation of THD and capacitance reduction. Overall efficiency, power, total harmonic distortion, and other performance parameters also were analyzed for each topology whose techniques were applied. Unlike the other techniques presented in the literature, the proposed frequency-based ARC can be applied to converters with resonant stages, which allows for the design of high-efficiency low-capacitance LED drivers. A good performance in terms of efficiency was also achieved in [22] and [25], since the converters presented in these papers are composed of only one stage. However, the aforementioned approaches yielded a moderate capacitance reduction with a high increase in the input current distortion. In the integrated off-line LED driver based on hard-switching topologies proposed in [23] and [24], the obtained capacitance reduction was improved, mainly in [23], but still resulting in a high input current distortion. Moreover, the overall efficiency of these converters is low. It is important to highlight that the proposed frequency-based ARC allows for a large capacitance reduction without affecting the THD significantly. Therefore, the proposed approach is a great alternative concerning reduction of bulk capacitance, improving the driver lifetime while still maintaining a low output ripple and preventing flickering.

One of the drawbacks of the evaluated topology is that the PFC stage operates with a duty cycle of 0.5 and, therefore, the bus voltage has to be at least twice the peak value of the input voltage. Hence, it poses some difficult to operate in universal-input voltage condition with the 650 V/700 V voltage rating power devices. However, this disadvantage can be solved by using one of the buck-boost type topologies instead of boost-based topologies. Regarding the PC stage, the series resonant converter adds no galvanic isolation and has a relatively low efficiency. These drawbacks can be mitigated by employing the LLC converter and performing the design procedure proposed in this paper.

TABLE VII
COMPARISON AMONG CONTROL TECHNIQUES TO REDUCE BULK CAPACITANCE IN OFF-LINE LED DRIVERS.

	Proposed frequency-based ARC	Conventional ARC [23]	Conventional ARC [24]	Conventional ARC [25]	3rd harmonic injection [22]
Topology	BBLC	double buck-boost	double buck-boost	PFC flyback	PFC boost
ΔTHD	0.9 %	17.2 %	12.71 %	24.5 %	$>$ 40 %
Capacitance reduction	66.6 %	85 %	46.3 %	24.2 %	33 %
			Performance Parameters of the Topology		
Efficiency	90.3 %	84 %	85 %	90.1 %	91 %
Output power	96.6 W	75 W	70 W	50 W	20 W
Output current ripple	58 mA (8.3 %)	50 mA (10 %)	220 mA (44 %)	36 mA (10.3 %)	14 mA (29.7 %)
PFC stage output capacitance	11 μF	22 μF	40 μF	470 μF	8.8 μF
PFC stage output voltage	450 V	160 V	180 V	144 V	420 V
FP	0.986	0.982	0.991	0.969	0.91
THD	9.35 %	18.2 %	13.5 %	25.3 %	-

V. Conclusion

This paper presented the generalized analysis of the active ripple compensation approach at the control variable of integrated off-line LED drivers. The theoretical analysis described the operation of several topologies under the modulation of switching frequency and duty cycle. The duty cycle modulation, which has been explored in some works, was analyzed for several topologies showing that it has a good capacitance reduction potential. However, all of them presenting a relevant drawback: the significant increase in the THD. The low sensitivity of the LF ripple to duty cycle modulation implies that to achieve a good ripple reduction, a significant modulation in the control variable must be employed, causing a large distortion in the input current. On the contrary, this paper proposed an alternative approach based on the modulation of the switching frequency, which allows for a large capacitance reduction without affecting the THD significantly when applied to converters with a load-resonant PC stage. This alternative also increases the overall LED driver efficiency when compared to integrated converters in which both stages operate under hard-switching condition. Experimental results verified the theoretical analysis, showing that the ARC technique in the switching frequency allowed for a capacitance reduction of 66.6%, while increasing only in 0.9% the input current THD.

Acknowledgments

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