Passive and online DC bus Status Monitoring for Back-to-Back Converters applied to Doubly-Fed Induction Machines

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***Abstract*—This paper proposes a passive and an online estimator of the DC Bus parameters (series resistance R_s, inductance L_s, and capacitance C) used in Doubly-Fed Induction Machines (DFIM) for wind applications. These kinds of machines are widely adopted as generators for wind applications, where predictive maintenance is an important cost-reduction driver. Two implementations are described, plug-in or parallel, depending on whether the algorithm runs in the application digital control platform (DCP) or as a standalone diagnostic device. Neither requires maintenance shutdown or DC current measurements to estimate bus parameters. In the plug-in operation, the proposed method relies only on the electrical quantities required by the control system, i.e., stator-side and rotor-side voltages and currents. Conversely, in parallel mode, dedicated external voltage and current sensors are used. In both cases, the series RLC estimation is based on a recursive least squares (RLS) algorithm that works for the full speed range of regular operation required in wind energy applications. In this way, the replacement of deteriorated capacitors can be performed by monitoring the estimated parameters. The validity of the proposal is discussed based on a theoretical analysis, simulation results, and experimental validations.**

***Index Terms*—Bus bar, Diagnostics, Doubly fed induction machine, Parameter estimate, Impedance measurement, Predictive maintenance**

I. Introduction

DISTRIBUTED power generation (DPG) based on wind is a mature technology. The EU strives to account for 20% of its final energy consumption coming from renewables by 2021 [1]. At the same time, renewables covered 34% of gross electricity consumption in the EU-27 in 2019 [1]. Finally, wind and hydropower accounted for two-thirds of the total renewable energy generation (35% each) [1]. Talking about the future wind installations in Europe (2021-2025) [2], it is expected that onshore installations will represent the 72% of new installations over the five years, averaging about 15 GW/year. Offshore new installations will average 6 GW/year, representing about 28% of the total market across 2021-2025. Regarding drive train configuration in onshore installations, geared wind turbines with Doubly Fed Induction Machines (DFIMs) are the most popular in the actual market [3].

Fig. 1 shows a diagram of a wind turbine generator based on a DFIM. The stator is directly connected to the grid in this configuration, whereas the rotor winding is connected to the grid via a three-phase back-to-back converter. The rotor-side converter (RSC) regulates the power factor, the torque and the rotor speed. At the same time, the grid-side converter (GSC) maintains the DC bus voltage constant independent of the magnitude and direction of the rotor power [4], allowing active and reactive power to be controlled separately.

Two of the most critical aspects of the DPG scenario are the maintenance and fault-detection tasks. According to [5], capacitors and semiconductors have the most significant failure rate of all components. The DC bus is responsible for up to 30% of wind turbine failures, while semiconductor failures account for roughly 20% of the overall [6], [7]. The deterioration estimation of the DC bus capacitors present in DFIMs is investigated in this work. The primary purpose here is to save money by replacing the capacitor bank in scheduled maintenance events before a failure occurs, avoiding the negative consequences.

Finding a monitoring method for the DC bus capacitor has been the focus of research efforts in previous years. A deep review of the state of the art of these techniques can be found in [8]–[13]. Two main categories are commonly used in the literature to group the methods according to their characteristics. The first one refers to the converter topology: DC-DC [10]–[19] and DC-AC [20]–[26] power converters. The second category groups the methods according to their ability to operate in real time. In this way, methods can be classified as offline, online and quasi-online. An offline method [27], [28] usually requires to stop the power converter, perform some measurements and restart it. They provide good accuracy at the cost of stopping converter operation. Conversely, online methods [10], [12], [13], [15], [17], [19], [20], [23], [25], [26] estimate the aging of the capacitor in the standard operating mode of the converter. Finally, quasi-online techniques [13], [21], [22], [24] work in a similar way to the online ones. The main difference lies in the fact that the estimation can only be performed during non-standard operating conditions of the system, for example, during the night hours of operation of solar inverters or in the regenerative mode of power converters for electrical machines.

A set of extended categories is proposed in this review. The first one groups the methods into active and passive. An active method [8], [9], [12], [14], [21], [22], [24], [25], [27], [28] requires to inject a perturbation to estimate the capacitor health state. In contrast, passive methods [10], [11], [15]–[17], [19], [20], [23], [26] work as an observer. Injection of a disturbance (usually a small sinusoidal signal or pulse train) can affect system losses and capacitor life, so passive methods are preferred. If an active method is at the same time online, special care should be taken not to affect the control of the power converter.

The second category groups the methods according to their estimation technology. Thus, temporal modeling techniques [10], [14] performs a parametric identification based on the

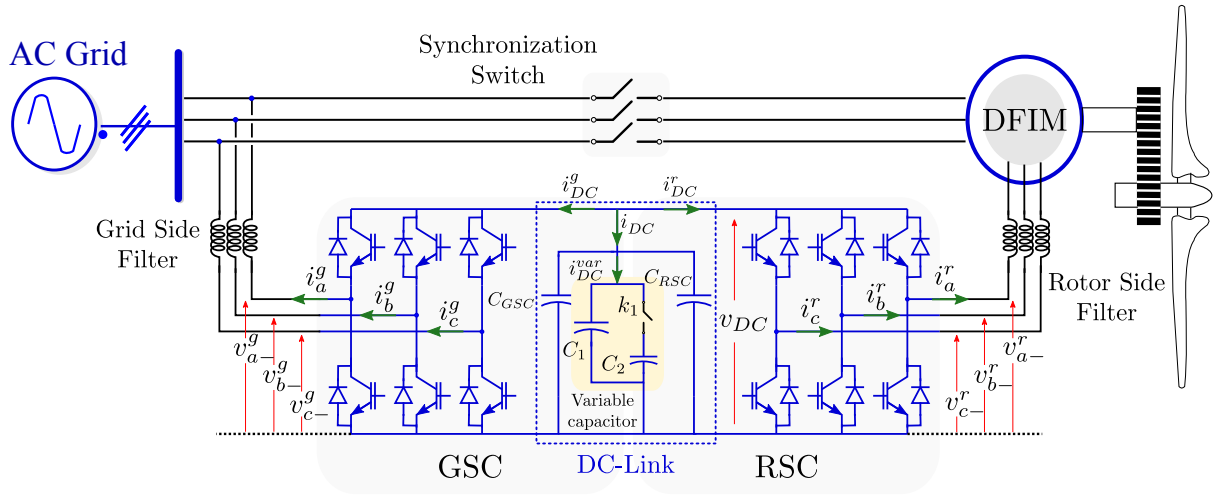

Fig. 1: Block diagram of a grid-connected DFIM. A variable DC capacitor is used for simulation and experimental verification.

transient response of the DC bus. These techniques require the converter to operate in a particular operation mode (continuous or discontinuous conduction mode), to deactivate the converter control to cause a change in the bus voltage or to induce a large transient in which the DC bus outweighs the converter control. Techniques based on adaptive filters [15], [16], [18], [21], [22], [24], [25] model the DC bus, use algorithms that minimize the estimation error and estimate the capacitor parameters. They provide high parameter accuracy but are very sensitive to system modeling. A third group is based on the estimation of the capacitor impedance at one or more frequencies of interest (switching frequency of the converter, or the second and sixth harmonics of the mains frequency). To isolate the desired components, bandpass filters can be used [12], [17], [23] or the impedance can be extracted using FFT/DFT-based techniques [19], [20], [27] or Goertzel's algorithm [26]. Some of these methods require tracking the voltage and current components at the switching frequency, which may require high sampling rates to ensure good accuracy.

Finally, the methods can be grouped depending on which parameters are used as metrics for estimation. Equivalent series resistance (ESR) has traditionally been used as a metric [11], [15]–[19], [21], [23], although some techniques use either only the capacitance [14], [22], [25] or both ESR and capacitance [10], [13], [20], [26], [27]. Special care must be taken in this regard when more than one capacitor is present in the DC bus. If only the ESR is used as a metric, the failure of one capacitor (or a small group of them) may be hidden in the estimation due to the greater weight of small series impedances (capacitors in good condition) over larger ones (faulty ones) in the parallel equivalent impedance calculation. Methods involving more than one parameter are preferred. Table I summarizes the best performing methods in each of the categories described above.

In order to associate the advantages of the methods described above (and curtail their disadvantages), a method for estimating the health status of the capacitors connected to the DC bus is proposed in this paper. The proposed method is valid for back-to-back power converters applied to DFIM, although it can be applied to any back-to-back configuration where the currents on both sides of the converter are controlled. Its main characteristics are: it can be implemented online and does not require any signal injection (passive implementation) since it takes advantage of the variable speed inherent to the functioning of the DFIM. Another advantage is that it does not require a high sampling frequency, allowing it to be easily integrated into standard control platforms. The method is based on modeling by means of adaptive filters (Recursive Least Squares, RLS). Lastly, and as a novel contribution, the method is able to extract not only the ESR and the DC bus capacitance, but also an estimate of the equivalent series inductance (ESL). Inputs to the algorithm are the measured DC link voltage and the measured or estimated capacitor current, that can be reconstructed from the AC currents and voltages at the output of the two converters (no DC bus current sensor is needed). This work generalizes the results of the conference paper [29]. Extended theoretical discussion regarding the estimator as well as experimental validation by using a laboratory-scale setup with a variable capacitor are considered in here. Additionally, the extension of the proposed method to be used in a standalone device is also added.

The following sections comprise this paper: The capacitor modeling is evaluated in Section II. The RLS algorithm is used to estimate the capacitor bank parameters in Section III. Section IV provides a system evaluation based on simulation results. The methods experimental results are presented in Section V, while the conclusions are summarized in Section VI.

II. Capacitor Modeling

Aluminum electrolytic, metalized polypropylene film, and multi-layer ceramic are the three types of capacitors often used in DFIMs. Because of its high energy density and low cost per joule, the aluminum electrolytic capacitor is the preferable alternative, according to [30].

The capacitor model used in this work is shown in Fig. 2. A series connection of a ESR (R_s), a ESL (L_s), and a capacitance (C) makes up it. As a result, (1) determines the voltage in the DC bus.

$$\frac{\mathrm{d}v_{DC}}{\mathrm{d}t} = L_s \frac{\mathrm{d}^2 i_{DC}}{\mathrm{d}t^2} + R_s \frac{\mathrm{d}i_{DC}}{\mathrm{d}t} + \frac{1}{C} i_{DC} \tag{1}$$

The performance and working life of the electrolytic capacitors found on DFIMs are heavily influenced by operating circumstances such as temperature, voltage, and current.

TABLE I: Comparison of methods for monitoring the DC bus health status.

Technology	Description and Converter Topology	Real Time	Active Passive	Metric	Pros and Cons
Temporal Modelling	[10] - DC-DC - Detects variations in the DC-DC dynamical response.	Yes	Passive	ESR+C	Pros: No current sensor required. Cons: The sensitivity depends on the size of the capacitor.
	[14] - DC-DC - Detects variations in the converter transient response.	Yes	Active	C	Pros: Ease of implementation Cons: Requires to disable the converter control.
Adaptive Filtering	[25] - AC-DC-AC - Uses a regression method and a 30 Hz voltage injection.	Yes	Active	C	Cons (1): Needs training data. Cons(2): Perturbs the DC voltage.
	[21] - AC-DC-AC - Based on RLS.	Yes	Active	ESR	Pros: Easy to implement. Cons: Temperature dependence.
	[24] - Single-phase DC-AC - Based on RLS.	No	Active	C	Cons (1): Requires to inject a perturbation. Cons (2): Requires no load condition.
Impedance estimation	[26] - Rectifier-fed three-phase DC-AC - Uses Goertzel algorithm to obtain the impedance at low and high frequencies.	Yes	Passive	ESR+C	Pros: Temperature estimation. Con: Requires high-frequency sampling for ESR estimation.
	[23] - Three-phase DC-AC - Uses switching harmonics to detect capacitor ESR.	Yes	Passive	ESR	Cons(1): Requires current sensor. Cons(2): Requires high-frequency sampling for ESR estimation.
	[12] - DC-DC - Low frequency injection to estimate impedance by using band-pass filters.	Yes	Active	C	Pros: Good accuracy. Cons: Disturbance injection.

Working outside of the operational limitations accelerates the degradation process by evaporating the electrolytic liquid, lowering its useful life. The combination of resistance and/or capacitance values is a helpful figure of merit to check capacitor aging [10], [11], [13]–[23], [25]–[27]. Capacitor aging results in an increase in the capacitor ESR and a decrease in the capacitance. Under nominal conditions, capacitors approach the end of their life when their ESR value exceeds 2.8 times the rated ESR value and capacitance declines by 20 percent of the rated value, as shown in prior works [31] and industry standards [32], [33].

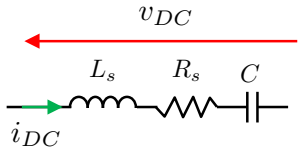

Fig. 2: Capacitor Model.

III. Parameter estimation using Recursive Least Squares Algorithm

The estimation process for the DC bus parameters is described in this section. The detailed block diagram of a DFIM back-to-back converter is shown in Fig. 1, which includes the voltages and currents on both the DC and AC sides (grid and rotor). It also has a variable capacitor attached to the DC bus for simulation and experimental validation. The RLS method is used for system identification in the proposed strategy, as shown in Fig. 3. The DC-link capacitor parameters are calculated using a variable filter driven by the error signal obtained by measuring and estimating the DC-link voltage. The RLS seeks to reduce the estimation error by adjusting the filter parameters in each iteration. Low data storage and computational effort are two advantages of the RLS method.

The RLS operates in the discrete domain [34]. Three different discrete approximation methods are here compared: forward Euler, backward Euler and Bilinear (Tustin), where their discrete approximations are gathered in the first row of Table II, being T the sampling period. The discrete version

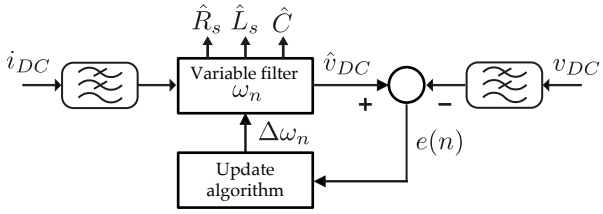

Fig. 3: RLS Algorithm.

TABLE II: Transfer function coefficients

	Forward Euler	Backward Euler	Tustin
$s \leftarrow z$ [35]	$\frac{z-1}{T}$	$\frac{z-1}{Tz}$	$\frac{2}{T}\frac{z-1}{z+1}$
b_0	$\frac{L}{T}$	$\frac{T^2+CR_sT+CL_s}{CT}$	$\frac{T^2+2CR_sT+4CL_s}{2CT}$
b_1	$\frac{-(2L-R_sT)}{T}$	$\frac{-(2L_s+R_sT}{T}$	$\frac{T^2-4CL_s}{CT}$
b_2	$\frac{T^2-CR_sT+CL}{CT}$	$\frac{L}{T}$	$\frac{T^2-2CR_sT+4CL_s}{2CT}$
a_0	0	1	1
a_1	1	−1	0
a_2	−1	0	−1

of the capacitor model in (2) is derived using the three alternatives, where the coefficients, b_0, b_1, b_2, a_0, a_1 and a_2, are related to the system parameters as presented in Table II.

$$TF_{Cap}(z) = \frac{v_{DC}(z)}{i_{DC}(z)} = \frac{b_0 z^2 + b_1 z + b_2}{a_0 z^2 + a_1 z + a_2} \tag{2}$$

Fig. 4 represents the Bode diagram for the continuous system and the discrete approximations. It can be observed that the magnitude of the module for the discrete approximations closely resembles the continuous domain value, although at frequencies close to Nyquist the Tustin method is slightly divergent (Fig. 4a). On the contrary, the Forward and Backward Euler methods present relevant phase errors, whereas the Tustin approach achieves better results up to the Nyquist frequency range (Fig. 4b). Considering this analysis, Tustin method is selected as the discretization method for the online estimation.

Once the system parameters are estimated, the n^{th} sample

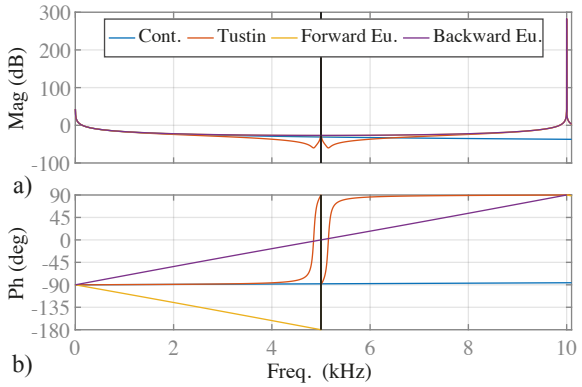

Fig. 4: Discretization process (10 kHz): Continuous function, Tustin, Forward Euler and Backward Euler discrete approximations. a) Magnitude, b) Phase. The vertical black line marks the Nyquist frequency.

Algorithm 1 DC Bus identification using RLS algorithm.

$\omega_n = zeros(1,4)$
$P_n = identity(4) \cdot 10^{10}$
$g_n = zeros(4,1)$;
$\alpha_n = 0$
while true **do**
  $X_n = [i_{DCn}, i_{DCn-1}, i_{DCn-2}, v_{DCn-2}]$
  $\alpha_n = v_{DCn} - X'_n \cdot \omega'_n$
  $g_n = \frac{P_n \cdot X_n}{\lambda + X'_n \cdot P_n \cdot X_n}$
  $P_n = \frac{1}{\lambda} \cdot \frac{P_n - (P_n \cdot (X_n \cdot X'_n) \cdot P_n}{\lambda + X'_n \cdot P_n \cdot X_n}$
  $\Delta\omega = (\alpha_n g_n)'$
  $\omega_n = \omega_n + \Delta\omega$
end while

of the predicted capacitor voltage is given by the difference equation in (3). After the state variable estimation is computed, the RLS algorithm can be executed recursively, as shown in *Algorithm* 1.

$$\hat{v}_{DC}^{[n]} = b_0 \cdot i_{DC}^{[n]} + b_1 \cdot i_{DC}^{[n-1]} + b_2 \cdot i_{DC}^{[n-2]} - (a_1 \cdot v_{DC}^{[n-1]} + a_2 \cdot v_{DC}^{[n-2]}) \quad (3)$$

The implementation is explained as follows: $zeros(r, c)$ sets a matrix with r rows and c columns, $identity(b)$ generates an identity square matrix with b rows and columns and λ parameter sets the forgetting factor (typically $0.9 < \lambda < 1$). In each iteration, the ω_n (4) array will contain an estimation of the filter coefficients of the discrete transfer function (2), where the actual and the last samples of the capacitor voltage and current are inputs to the RLS algorithm (see Fig. 3).

$$\omega_n = [\hat{b_0}, \hat{b_1}, \hat{b_2}] \quad (4)$$

Thus, the capacitor bank predicted values can be obtained for the different discrete approximation methods following the relation gathered in Table III.

Estimation of these parameters requires the use of capacitor voltage and current [11], [15]–[17], [21], [23], [25]. In general, DC current is not measured (although DC-link current sensor can be used for protection [36]–[39]), so an estimation method is required [10], [22], [24]. The capacitor current, assuming

TABLE III: DC bus parameter values

	Forward Euler	Backward Euler	Tustin
R_s	$2\hat{b_0} + \hat{b_1}$	$-\hat{b_1} - 2\hat{b_2}$	$\frac{\hat{b_0} - \hat{b_2}}{2}$
L_s	$T\hat{b_0}$	$T\hat{b_2}$	$\frac{T\,(\hat{b_0} - \hat{b_1} + \hat{b_2})}{8}$
C	$\frac{T}{\hat{b_0} + \hat{b_1} + \hat{b_2}}$	$\frac{T}{\hat{b_0} + \hat{b_1} + \hat{b_2}}$	$\frac{2T}{\hat{b_0} + \hat{b_1} + \hat{b_2}}$

the outgoing current in RSC and GSC converters (Fig. 1), can be determined from (5).

$$\hat{i}_{DC} = -(\hat{i}_{DC}^{g} + \hat{i}_{DC}^{r}) \quad (5)$$

The DC current at each of the bridges can, in turn, be obtained from the AC currents and the corresponding switching function (6), where $i_{abc,g/r}$ and $S_{abc,g/r}$ are the currents and switching functions for the grid-side (g) or rotor-side (r).

$$\hat{i}_{DC}^{g/r} = S_a^{g/r}\, i_a^{g/r} + S_b^{g/r}\, i_b^{g/r} + S_c^{g/r}\, i_c^{g/r} \quad (6)$$

The RLS algorithm requires some variation in the measured variables for correct operation. The DC bus current distribution for the case of a back-to-back converter was previously studied in the literature [40]–[42]. In this way, the frequency components depend on both the switching frequency of the RSC (f_{c_r}) and GSC (f_{c_s}), the fundamental frequency of the rotor (slip frequency, f_{slip}) and stator (grid frequency, f_e) side currents and the induced components among the rotor and stator [43]. It can be concluded that there are well-defined bands of interest in the DC bus current, and thus voltage, spectrums: a low frequency band (from zero to few hundreds of Hertzs depending on the natural system frequencies and close-loop bandwidths) and several high frequency bands (in the vicinity of the switching frequency and the resulting switching harmonics).

The low frequency zone may contain harmonics of frequency $6nf_{slip}$, $6nf_e$ and intermodulation harmonics due to the interaction between the rotor and the stator ($2f_e$, $3(f_e \pm f_{slip})$) [43]. The magnitude of these harmonic components depends on the DFIM load level, the RSC/GSC switching frequency, the DFIM control bandwidth and grid unbalanced conditions [40]–[43].

At the same time, the high-frequency components depend both on the switching frequencies on both sides of the converter (f_{c_r}, f_{c_s}) and on the frequencies of the rotor (f_{slip}) and stator (f_e). Thus, the following components are found in practice around the switching frequency [40]–[42]: $f_{c_r} \pm 3f_{slip}$ and $f_{c_s} \pm 3f_e$.

In order to verify this issue, Fig. 5 shows the simulation results including the DC current and voltage spectrums at the low and high frequency bands. In this case, the DFIM is operating at a 0.2 slip (super synchronous mode). Thus, the rotor currents have a frequency of $f_{slip} = 10\ Hz$, the stator currents having a $f_e = 50\ Hz$. As predicted by the theoretical analysis, the DC bus current (Fig. 5a) and voltage (Fig. 5c) include a component at $6f_{slip} = 60\ Hz$, a smaller component at $6f_e = 300\ Hz$ and a set of harmonics located at $2 \cdot 6f_{slip} = 120\ Hz$, $3 \cdot 6f_{slip} = 180\ Hz$. At the same time, the same components defined in the theoretical analysis are found in the upper band of the spectrum: $f_{c_r} \pm 3f_{slip} =$

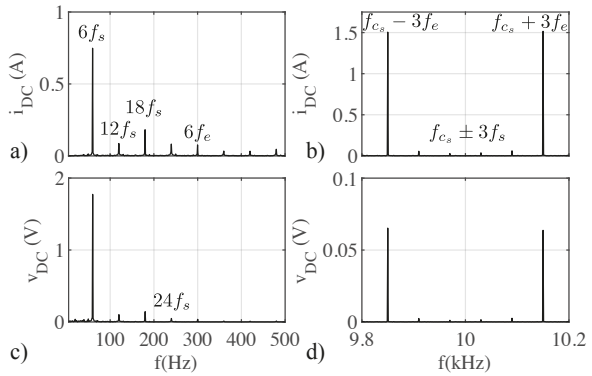

Fig. 5: Simulation results. Low and high frequency band spectrums of the DC bus current and voltage (0.2 slip) (to shorten, f_s stands for slip frequency): a) current, low band. b) Current, high band. c) Voltage, low band. d) Current, high band.

$10 \cdot 10^3\ Hz \pm 3 \cdot 10\ Hz = [9970, 10030]\ Hz$ and $f_{c_s} \pm 3f_e = 10 \cdot 10^3\ Hz \pm 3 \cdot 50\ Hz = [9850, 10150]\ Hz$.

Whenever the DFIM is handling power, both low and high frequency components will be present in the DC bus. In order to use the same sampling frequency as the switching frequency of either GSC/RSC, it is proposed to use the low frequency information to feed the RLS algorithm. For this purpose, both current and voltage RLS inputs (see Fig. 3 are filtered by a low-pass filter. A cutoff frequency of $500\ Hz$ is proposed. Note that, since both current and voltage are equally filtered, the impedance estimation is not affected. Also, at that frequency range, it is expected the Tustin discretization will be the least affected by the discrete approximation following Fig. 4 and it is expected to obtain the best estimation.

Two implementations are proposed in this paper depending on whether the algorithm runs: in a stand-alone device connected in parallel with the power converter (parallel mode) or in the DCP that controls the DFIM (plug-in mode). In the case where the algorithm runs on the DCP controlling the DFIM, no additional voltage or current measurements are required. In contrast, if the method is implemented in an independent monitoring device, both rotor-side and stator-side voltages and currents are measured.

In both techniques, the monitoring of the DC bus health status can be performed at any desired time, since under normal conditions it is not necessary to implement it on a continuous basis. This is because the degradation of the bus capacitors has a rather slow behavior, so the method can run continuously on the control system, or it can be scheduled to run several times per day/per hour.

A. Parallel mode.

In this operation mode, switching functions are evaluated as 1 or 0 depending on when an upper switch turns *ON* or *OFF* and they are estimated from the measured three-phase (inverter-side) phase voltages referred to the negative point of the DC bus ($v_{abc\,n,g/r}$ in Fig. 1). These voltages are compared with a threshold (e.g. 50% of the nominal DC bus voltage) to determine the value for the switching function.

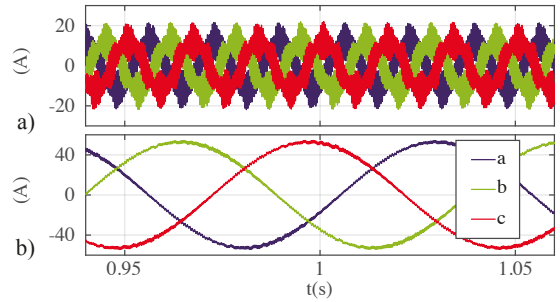

Fig. 6: i_{DC} Estimation input signals: a) i^g_{abc}, b) i^r_{abc}.

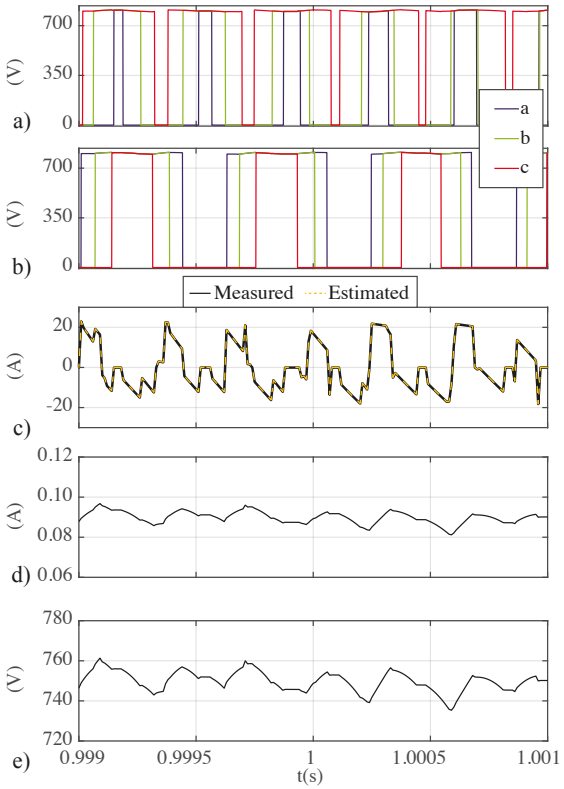

Fig. 7: i_{DC} Estimation results: a) v^g_{abc-}, b) v^r_{abc-} c) Measured and estimated DC current, d) Estimation error, d) DC bus voltage (v_{DC})

Figs. 6 and 7 show a simulation example of the proposed current estimation method in the parallel operating mode. Fig. 6 shows the input estimation currents while Fig. 7 shows the estimation results. As shown in Figs. 7c and Fig. 7d, the proposed estimation technique throws an excellent performance, showing a small DC estimation error lower than 0.4%.

B. Plug-in mode.

As said before, estimation of the DC-link capacitance requires to know the DC-link capacitor current. In parallel mode, where a dedicated system and sensors are used, the estimation of the DC-link current can be done by a rather straightforward approach. The output converter voltages are measured with respect to the DC-link negative rail and compared with a threshold value that determines whenever the state of each leg up-side or the low-side switches.

However, in plug-in mode, non dedicated sensors are used. For the control of the power converter, voltages are only measured in the grid-side converter after the filter for grid synchronization purposes. This makes the estimation method used in parallel mode not applicable in this case.

The DC-link current can be reconstructed by considering each switch and anti-parallel diode currents according to expression (7), where $\hat{i}^{g/r}_{DCx}$ represents the contribution to the DC-link current from phase x, $S^{g/r}_{x+}$ is the switching function state for the up-side switch in phase x that can be obtained from (8), $i^{g/r}_{x+}$ is the output current of phase x and $D^{g/r}_{x-}$ represents the switching function for the up-side diode in phase x, given by (9).

$$\hat{i}^{g/r}_{DCx} = S^{g/r}_{x+}, i^{g/r}_{x+} - D^{g/r}_{x-}, i^{g/r}_{x+} \tag{7}$$

$$S^{g/r}_{x+} = (d_x >= c_x)[i^{g/r}_{x+} >= 0] \tag{8}$$

$$D^{g/r}_{x-} = (d_x >= c_x)[i^{g/r}_{x+} < 0] \tag{9}$$

In (8) and (9), d_x and c_x are the duty cycle and the value of the carrier signal used for the PWM modulation for phase x. Finally, the total DC-link current can be simply obtained from (10).

$$\hat{i}^{g/r}_{DC} = \sum_{x=a}^{c} \hat{i}^{g/r}_{DCx} \tag{10}$$

As it can be seen, the contribution of each phase to the overall DC-link current can be determined only by knowing d_x, c_x and the sign of the phase current. The duty cycle and the sign of the phase current can be obtained directly from the control signal and the feedback current measurement within the digital control system. Determining the value of the carrier signal is not direct. Commonly, it is implemented by a timer in the digital control system that runs at much higher frequencies than the sample time used for control purposes and thus can not be known. However, most of the modern digital control systems used in power-conversion applications allow for generating an interrupt whenever the comparison register meets the value of the carrier signal, as well as in zero and period for the carrier signal. Using that enhanced hardware capability, the DC-link current can be estimated at these three points. The estimated current is shown in Fig. 8. As it can be seen, a very good agreement is obtained between the resulting current from the electrical circuit simulation (idc_{sim}) and the synthetic one (idc_{synth}).

IV. Simulation Results

The simulation evaluation of the proposed method is shown in this section. It was performed in Matlab/Simulink, following the configuration of Fig. 1. A DFIM model using the properties listed in Table IV was used. The DFIM is controlled by the RSC/conventional GSC's control architectures.

To implement the RLS method, two basic parameters must first be chosen: the sampling frequency f_{RLS} and the forgetting factor λ. Since the frequencies of interest of the voltage and current spectrums are bounded by a low-pass filter (Fig. 3), a value of $f_{RLS} = 10\,kHz$ was chosen which ensures a good sampling rate of the desired components.

At the same time, the forgetting factor λ determines how noisy the estimated filter coefficients are: a smaller λ reduces

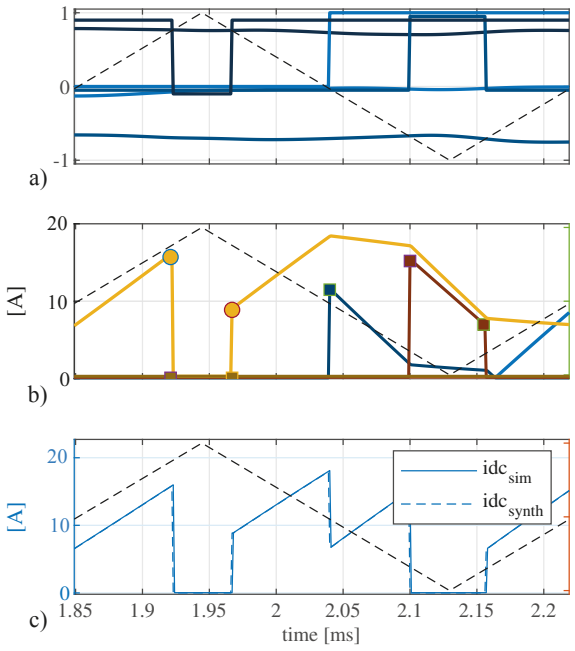

Fig. 8: Simulation results. i_{DC} current estimation under the plug-in mode. a) carrier signal, duties for the three phases and corresponding comparison; b) estimated switches and diodes currents. The sample times for the respective switches are marked with the same color than the respective phase; c) estimated i_{DC} current.

TABLE IV: Setup Parameters

Parameter	Value
Rated Power	$S_G = 15\,kVA$
GSC/RSC switching frequency	$f = 10\,kHz$
C_{GSC} and C_{RSC} Capacitances	$C_{(G/R)SC} = 350\ \mu F$
C_1 Capacitance	$C_1 = 420\ \mu F$
C_2 Capacitance	$C_2 = 120\ \mu F$
RLS sampling frequency	$f_{RLS} = 10\ kHz$
RLS forgetting factor	$\lambda_{RLS} = 0.997$

the memory capabilities of the RLS and leads to filter coefficients with noticeable noise. Therefore, $\lambda_{RLS} = 0.997$ was chosen in this work to obtain a clear and stable estimate. Finally, it should be noted that the plug-in mode was used to estimate the DC bus current.

Fig. 9 shows the simulation results of the proposed estimation technique using the Tustin coefficients found in Table II. The results are obtained for a different rotor speeds between 1200 and 1800 rpm ($slip = \pm 0.2$). Figs. 9a, b and c show the estimated DC bus resistance R_s, inductance L_s and capacitance C values respectively. Figs. 9d and e show a zoom around the time instant at which the change occurs.

At the beginning of the simulation, $t < 0.5\ s$, the nominal DC-bus parameters were used ($L_s = 0\,\mu H$, $R_s = 1\,m\Omega$ and the C_1, C_{GSC} and C_{RSC} capacitances shown in Table IV). This results in a total capacitance on the DC bus of $1120\,\mu F$. To test the transient response of the proposed technique, a second resistor of $1\,m\Omega$ is connected in parallel with the previous ESR in $t = 0.5\ s$. This leads to an equivalent ESR of $0.5\,m\Omega$. The same procedure was performed with the external

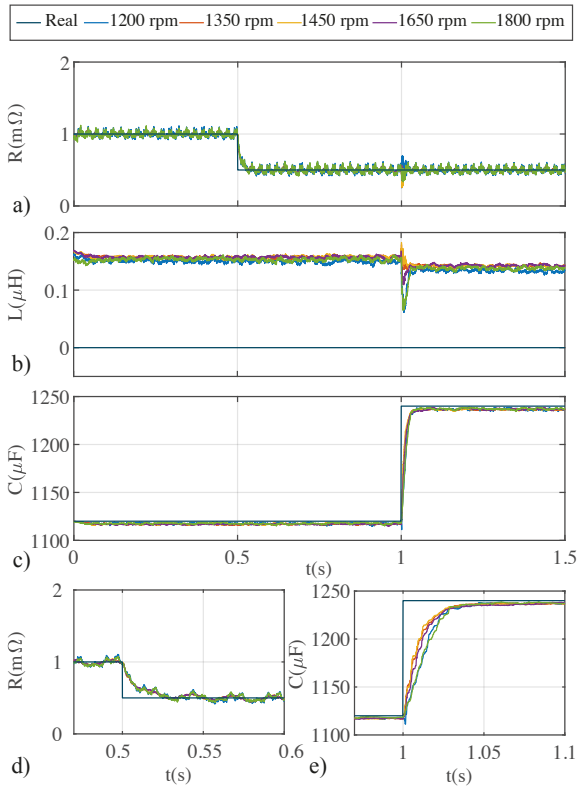

Fig. 9: System evaluation: simulation results. a) Estimated R_s, b) Estimated L_s, c) Estimated C, d) Estimated R_s (zoom) and e) Estimated C(zoom).

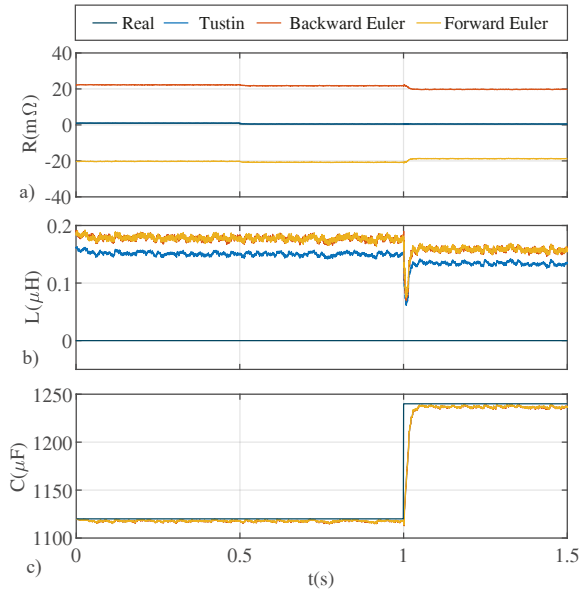

Fig. 10: System evaluation: simulation results. Effect of the discretization method on the proposed technique performance. a) Estimated R_s, b) Estimated L_s, c) Estimated C.

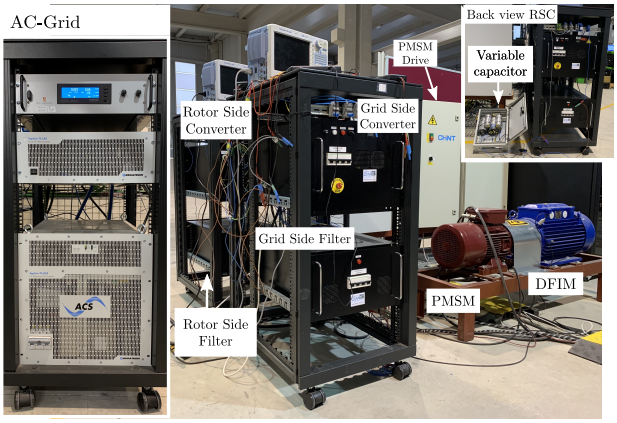

Fig. 11: Experimental Setup.

capacitance C_2 ($120\,\mu F$, see TableIV) that is connected in parallel with the previous DC bus capacitance in $t = 1\ s$. This implies that the capacitance of the bus is increased to $1240\,\mu F$. The proposed technique tracks with excellent performance both changes in the DC bus as shown in Fig. 9. An important result here is that the estimate is independent of the DFIM speed, while the proposed technique demonstrates an excellent accuracy and transient behavior. It shows a settling time of 50 ms to achieve the steady-state.

The effects of the discretization in the parameter estimation are gathered in Fig. 10. As it was expected, the best estimation is obtained with the Tustin transform due to the closest similarity to the continuous-time system, previously shown in Fig. 4. However, the phase error presented in the Forward and Backward Euler method (Fig. 4b) leads to a wrong estimation reflected in the R_s value: the Forward approximation has a phase lower than $-90°$ and results in negative estimated value, whereas, on the contrary, the Backward method has a positive error in the phase and provokes a positive error in the estimated R_s.

V. Experimental Verification

Experimental verification has been carried out by using the laboratory setup shown in Fig. 11 and Table IV. A four-quadrant programmable voltage source (2210 TC-ACS-50-480-400 from Regatron) was used as an AC grid emulator, while a pair of DC-AC voltage source inverters in back-to-back configuration were used to connect the DFIM to the grid.

A Texas Instruments F28335 DSP was used to implement the RSC/GSC controls. A permanent magnet synchronous motor (PMSM) was used to emulate the behaviour of a wind turbine in the variable speed range of 1200-1800 rpm ($0.2 > slip > -0.2$). This allows testing the estimation accuracy under sub and hypersynchronous modes. Since the plug-in mode was used in the simulation verification, the parallel mode was used in the experimental verification.

A variable capacitor was connected to the DC bus (Figs. 1 and 11): each VSC contains a 350 μF capacitor connected directly to the DC busbar. In addition, an external capacitor (connected in parallel with the DC busbar by means of a cable) was introduced in order to change the overall DC bus capacitance. It consists of a 420 μF fixed capacitor connected in parallel with a 120 μF switchable capacitor. This results in a fixed capacitor value of 1120 μF and a switchable capacitance of 120 μF.

The first experimental test evaluates the performance of the proposed method with DC-bus measurements. The voltage and

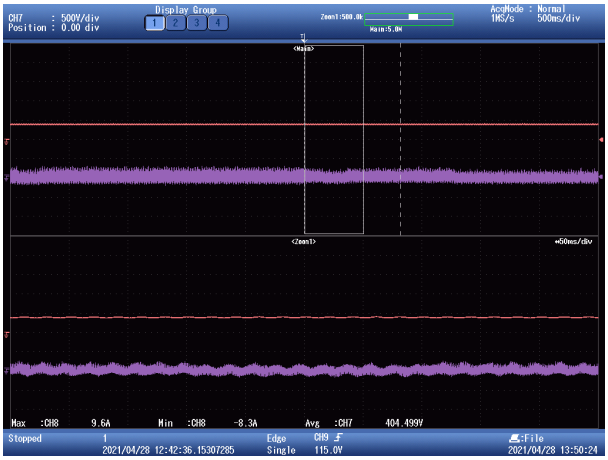

Fig. 12: Experimental results. Oscilloscope snapshot containing measurements of the external variable capacitor (Fig. 1). Red channel shows the DC bus voltage (v_{DC}) while purple channel shows the DC bus current (i_{DC}).

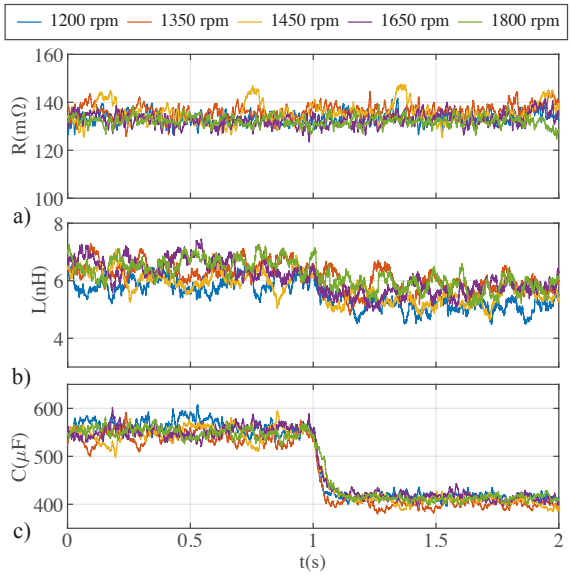

Fig. 13: Experimental results in parallel mode. Parameter estimation with voltage and current measurements (only the variable capacitor is estimated, see Fig. 1). a) Estimated R_s, b) Estimated L_s, and d) Estimated C.

current of the external capacitor were measured (see oscilloscope snapshot in Fig. 12) and fed to the proposed method to estimate its parameters (see Fig. 1). A $f_{RLS} = 10\,kHz$ was used. The RLS forgetting factor was set to $\lambda_{RLS} = 0.997$.

Fig. 13 shows the experimental results with DC-bus measurements and under different DFIM speeds (1200-1800 rpm). The switchable capacitor remains connected from the beginning of the experiment and it is disconnected from the DC bus at $t = 1\ s$. Note that the estimation of the DC bus parameters is independent of the DFIM speed. The proposed methodology clearly detects the capacitor disconnection after a few ms. Note that the equivalent series resistance and inductance are slightly modified by the capacitor disconnection since a cable was used to connect the external capacitor to the DC bus (see Fig. 11) to use a DC current probe. The resistance and

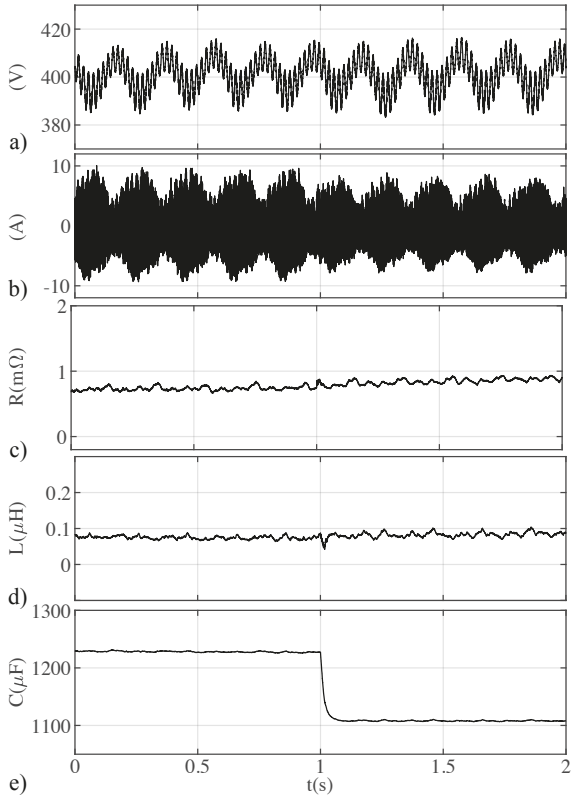

Fig. 14: Experimental results in parallel mode for ω_r=1350 rpm. DC bus current estimation was performed (the complete DC bus is estimated, see Fig. 1). a) Measured bus voltage, b) Estimated DC current, c) Estimated R_s, d) Estimated L_s, and e) Estimated C.

inductance of the connecting cable have a greater influence on the total impedance (cable plus capacitor) than that of the capacitor.

Fig. 14 shows the experimental results for parallel operation and DC bus current estimation. In this case, the DFIM speed remains constant at 1350 rpm, the DC bus voltage is measured (Fig. 14a), and the DC current is estimated by using (5) and (6) (Fig. 14b). As in the previous test, the switchable capacitor is connected from the beginning of the test and it is disconnected at $t = 1\ s$. Throughout the test, the ESR (R_s, Fig. 14c) rounds by 0.8-1 $m\Omega$ while the ESL (L_s, Fig. 14d) remains constant at a mean value of 0.1 μH. As mentioned earlier, when several capacitors are connected in parallel with the DC bus, the smaller ESRs dominate the parallel ESR. Therefore, monitoring the DC bus health state by using ESR as a metric can potentially lead to errors. Finally, Fig. 14e shows the estimated DC bus capacitance. As can be seen, the capacitor disconnection is clearly detected, showing a smooth transient and steady-state response.

To illustrate the influence of the switching threshold on the parameter estimation (6), Fig. 15 shows a scatter plot with the estimated mean values (R_s, L_s and C) in the range of $1-2\ s$ of the previous test (Fig. 14). A threshold sweep was set in the range of 10% to 90% of the DC bus voltage. Black dots show the mean value of the estimated resistance; orange dots show the inductance estimate, and black dots show the capacitance

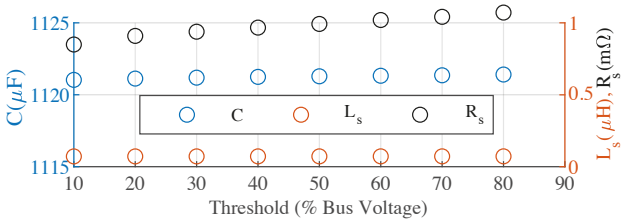

Fig. 15: Scatter plot containing a threshold sweep in the range of 10% to 90% of the DC bus voltage.

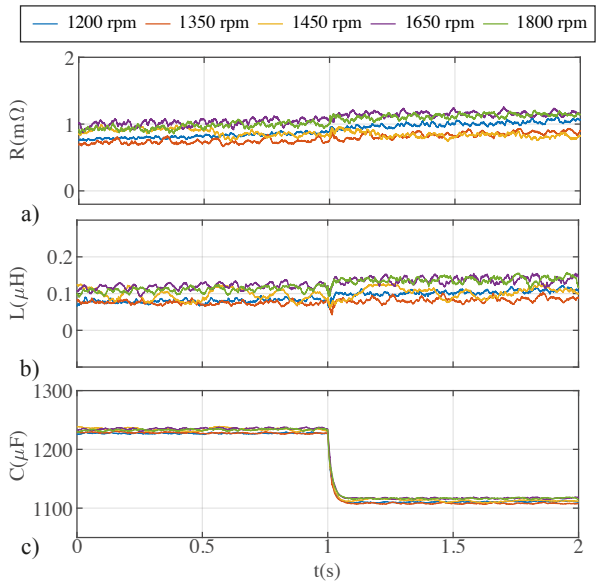

Fig. 16: Experimental results in parallel mode for different rotor speeds. DC bus current estimation was performed (the complete DC bus is estimated, see Fig. 1). a) Estimated R_s, b) Estimated L_s, and d) Estimated C.

estimate. The estimated parameters are fairly constant over the range tested so the choice of threshold has no noticeable effect on the parameter estimate. A threshold of 50% can be safely set to deal with the noise of voltage sensors.

The parameter estimate with DC current estimation test was repeated for the different DFIM speeds to test the accuracy of the method under different working conditions (from 1200 to 1800 rpm). The estimated values for resistance (Fig. 16a), inductance (Fig. 16b) and capacitance (Fig. 16c) vary slightly across DFIM operating speeds. In all tests, the proposed technique was able to detect the capacitor disconnection with similar transient and steady-state behavior.

VI. Conclusions

This paper proposed a technique to estimate the DC bus parameters of DFIMs using a back-to-back converter. This allows monitoring the aging of the DC bus capacitor, reducing, the number of unwanted shutdowns and their undesirable effects. First, the RLC series bus modeling was performed. The RLS algorithm for system identification was then used to estimate the parameters of the DC bus. A theoretical and numerical analysis of the DC bus components has been carried out. A band with frequencies of interest has been identified that allows the RLS to converge in a fast and accurate way. Two different implementation modes were proposed: the plug-in mode, where the algorithm resides in the DCP that controls the machine, and the parallel mode where the technique is implemented in a maintenance device that takes measurements from the DFIM. In the system evaluation sections, it has been proved that it is possible to estimate the DC bus parameters (series resistance, inductance, and capacitance) online without disturbing the operation of the DFIM operation. At the same time, the proposed method works with or without DC bus current measurement, since it can estimate the DC bus current using the three-phase voltages and currents. Another advantage of the method is that it can be implemented at low sampling frequencies, since it does not need to track any components at the switching frequency. The method was validated in simulations and experimental tests and showed high accuracy and good transient and steady-state performance.

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