Circuit proposal of a latching current limiter for space applications based on a SiC N-MOSFET

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Abstract: **Latching Current Limiters (LCLs) provide individual over-current protection to payloads protecting the satellite power bus. Under an overload, they limit the maximum current for a certain time. After this time, if the failure persists, the LCL isolate it from the power bus. The keystone of the LCLs is the current-limiting transistor. In traditional LCL designs, P-MOSFETs are used as the main current limiting device. However, in this work a complete LCL based on N-MOSFETs is presented. This change involves a complete redesign of the control circuitry. of the LCL architecture. The use of Silicon Carbide (SiC) is explored to assess the possibility of operating at higher voltages and potentially at higher temperatures. The paper shows a complete LCL design based on a SiC N-MOSFET. The design is tested implementing a class 10 LCL (10 A as nominal current) for a bus voltage of 100 V, a limitation current of 12 A, and for a limitation time (trip-off time) of 1.5 ms.**

Keywords: **LCL, satellite, SiC N-MOSFET, current protection, wide bandgap devices.**

I. Introduction

European satellites usually perform power distribution tasks using Latching Current Limiters (LCLs). The LCLs provide reliable connection and controlled disconnection of loads. LCLs also limit the load current demand to a predefined value, protecting the spacecraft bus against overloads or short-circuits. Fig. 1 shows the schematic of a regulated power bus in a satellite, where the distribution system is made up of LCLs. The ECSS standards and guidelines [1]-[3] are the main references for the design of these solid-state current limiters. The traditional structure of an LCL is shown in

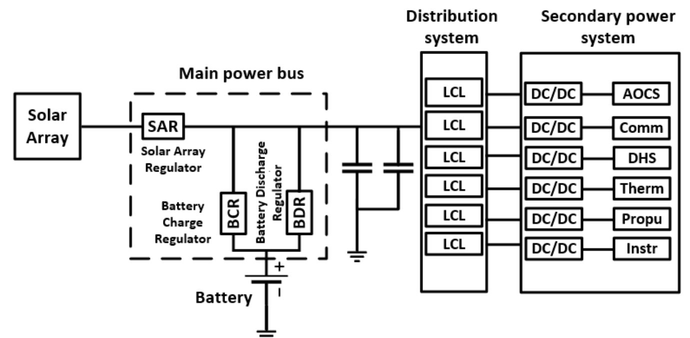


Fig. 1. Situation of the distribution system on a satellite

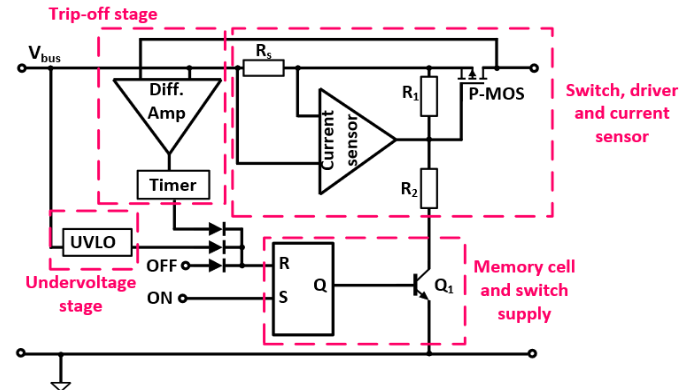


Fig. 2. Traditional LCL architecture based on a P-MOSFET

Fig. 2, it is based on a P-MOSFET [4]-[10] as the main limiting device, connected in series with the load. While the current through the P-MOSFET is lower than the desired limitation value, the transistor is fully ON in ohmic mode, thus the current demanded by the load flows without limitation. However, if the current demanded is higher than the limitation value, the control circuitry will force the MOSFET to operate in a linear zone regulating the current to the LCL limit value. As shown in [5] the current sensor also incorporates current regulation capabilities. In linear mode, the P-MOSFET will be withstanding a significant voltage level, being the worst case the bus voltage. Under these conditions the transistor is dissipating a significant power, then its temperature will increase very rapidly. As this situation cannot continue indefinitely, as soon as the P-MOSFET enters in linear mode, a timer circuit is started. If the current sensed by the LCL is still higher than the reference value after a predefined time (trip-off time), the control circuit of the LCL will turn off the MOSFET disconnecting the load from the satellite power bus. This load can be reconnected again later, by remote command.

According to [1], LCLs are classified in terms of its maximum current (Table 3.1 in [1]) only for bus voltages between 28 V and 50 V. The main reason for not using these LCL protections for higher bus voltages (i.e. 100 V and 120 V) is the difficulty of obtaining space-grade qualified P-MOSFETs capable of withstanding these voltages, with channel resistance (R_{DS}) values that will not imply high conduction losses without paralleling multiple devices, which can be problematic in terms of current sharing.

With the goal to improve the efficiency of the system, the main idea is to replace P-MOSFETs with N-MOSFETs, which for the same voltage and current capabilities usually present lower R_{DS} values. In this N-MOSFET-based LCL design, the drain and source terminals will be connected reversed than in the traditional P-MOS design, in which the source of the transistor is connected to the bus. With N-MOSFETs, the drain is connected to the bus. This forces a complete redesign of the control stage,

which must include some way to drive the current limiting MOSFET between gate and source. Unlike DC-DC converters in which the gate-source voltage of the transistor only takes two values to turn on and off the transistor, in LCLs the transistor gate to source voltage can take any value between the maximum gate-source voltage and the voltage to turn it. This guarantees a precise control of the current through the transistor. With P-MOSFETs, as the source is connected to the stable bus voltage, the control stage will impose a voltage in the gate lower than the bus, thus setting a negative gate-source which is what is needed to properly control P-MOSFETs. However, with N-MOSFETs the control signal needs to be translated to a positive gate-source voltage, thus a higher voltage in the gate than in the source must be imposed. As the source is connected to the load, its voltage can vary during LCL operation, i.e., if a short-circuit happens at the output of the LCL the source voltage would be 0 V.

The use of transistors based on wide bandgap materials (WBG) as the LCL main current limiting transistor, would enable working at higher voltages and, allegedly, higher temperatures. Some studies [11][12] about using SiC N-MOSFETs have been presented in the literature, showing some key points related to the driving circuitry, transistor selection, and power supply. The main objective of the present paper is to present a complete LCL design based on a SiC N-MOSFET for bus voltages between 100 V and 120 V. The proposed architecture has an auxiliary power supply, an analog isolator stage (DCX), which will provide the gate-source voltage level to the N-MOSFET, a timer stage to turn off the LCL when the limitation time has passed, and finally an undervoltage lockout stage (UVLO) in order to prevent the LCL turn ON process for a low bus voltage level.

This paper expands the one published in [13]. The paper is organized as follows: Section II details the process for choosing the limiting semiconductor devices. Section III. describes the stages of the proposed LCL architecture. Experimental results for a class 10 LCL, using the SiC N-MOSFET architecture, are presented in Section IV. Finally, the main conclusions are presented in Section V.

II. TRANSISTOR SELECTION

This section details the SiC transistor selection process, MOSFET or JFET, to be used in the LCL as current limiting devices under the requirements for use in space described in [1] and [2]. Due to the high dissipation of the transistors under LCL operation the junction temperature is used as a selection criterion. Several SiC transistors were selected and evaluated using theoretical models for estimating the junction temperature. It is possible to evaluate whether this junction temperature is keep under the device limits, regarding the margins established in [2] for the different LCL classes in [1]. LCLs for bus voltages of 28 V and 50 V are divided in classes according to the nominal current they can drive, and their current limit. For instance, a class 10 LCL has a nominal current of 10 A. The current limit for each LCL class is between 110% and 140% of the nominal current according to [1]. An LCL design will meet the current regulation requirements if the current is regulated between those limits in case of an overload. Fig. 3 shows the LCL current profile used for thermal simulation, assuming the worst case from the junction temperature point of view. At the first point, the LCL carries the nominal current, which is also the class current. When the short circuit takes place, there is an overshoot due to the reaction time of the LCL circuit, which cannot be larger than 50 A regardless of class, as defined in [1]. Finally, the maximum limitation current depends on the maximum trip-off time, which is different depending on the LCL class. As mentioned above, the bus voltage for these LCL designs is 100 V.

Transistors were selected considering both, availability and power dissipation. The most commonly available SiC transistors have a breakdown voltage of 1200 V and a nominal current rating, much larger than the voltages and currents in standard aerospace applications. Nonetheless, the LCL transistor will be operating in linear mode (with very high losses) in the milliseconds time range. Therefore, transistors with the highest power dissipation were selected. This means that SiC transistors are preferred for this type of work, rather than GaN transistors. SiC transistors are offered in packages which present better performances working at higher power levels than GaN [14]-[17]. There has been some research in the literature regarding radiation hardness of SiC devices. The wider bandgap makes them more robust than Silicon devices. However, there are no specified rad-hard tolerant devices. Commercial devices have been tested in various radiation environments. Degradation effects are similar to those experienced by Silicon MOSFETs, including threshold voltage (V_{th}) degradation and single events, which may be destructive [18]-[22]. None of the selected SiC devices were found in the literature. However, some degree of radiation tolerance is expected in the selected devices, especially since they will be operated well below their voltage and current limits.

Regarding maximum junction temperature, most of the devices are rated for 150ºC, but some of them are rated for 175ºC and 200ºC. Some other semiconductors devices as JFETs, can be another good option in order to work in the LCL application [23]. However, as they are normally on devices, they could compromise the LCL behaviour at start-up. Without applied voltage at the gate of the JFET the different loads will demand power.

Two criteria were considered in selecting from the different transistors. The first criterion was already highlighted. It is the junction temperature reached at the end of the trip-off time under the worst-case scenario. This maximum junction temperature depends on the dissipated power in linear mode and on the transient thermal impedance. The second criterion is based on the limiting devices dissipation while working in ohmic mode, thus carrying currents equal or below to the nominal current. Therefore, the best device would present the lowest losses under nominal operation and would not reach the junction temperature limit of the device while limiting the current. Worst scenario would be the one due to a short-circuit, making that the N-MOS will be withstanding the bus voltage level. From the current profile described in Fig. 3, the power dissipation profile was calculated using the following procedure:

1. Prior to the short-circuit, the device is in ohmic mode driving the nominal current. The power dissipated by the transistor is the one determined by (1), where R_{ON} is the device channel resistance, and I_N is the nominal current. This dissipation determines the initial temperature of the junction T_{j_start}.

$$P_{dis_nom} = R_{ON} \cdot I_N^2 \tag{1}$$

2. During the first overload event, the switch will be carrying 50 A [1]; therefore, the dissipated power is determined by (2).

$$P_{dis_overshoot} = R_{ON} \cdot 50^2 \quad (2)$$

3. During the limitation time, the device will be in linear mode withstanding the full bus voltage. Hence, the dissipated power is the one described in (3), where I_{lim} is the maximum limitation current.

$$P_{dis_linear} = V_{bus} \cdot I_{lim} \quad (3)$$

Fig. 4 shows the dissipated power profile, according to the behaviour, previously described.

The transient thermal responses are represented by graphs shown in the datasheet from all the selected SiC transistors. All these graphs were analysed approximating the transient thermal impedance by a 4th order Foster network. This Foster network was then transformed into a Cauer network using impedance synthesis techniques [24] and mathematical approximations. This transformation from Foster to Cauer network allows easy incorporation of other thermal impedances, such as R_{trp} in Fig. 5, between the thermal reference point and the device. According to [24]-[27], these Foster and Cauer networks are very accurate for evaluating the thermal behaviour of the selected SiC semiconductors.

The response of the Cauer network to the dissipated power represented in Fig. 4 was simulated to estimate the final temperature rise of the junction, T_{j_rise}. Using T_{j_start} and T_{j_rise} it is the value of the maximum junction temperature (T_{j_max}) can be calculated using (4):

$$T_{j_max} = T_{j_start} + T_{j_rise} \quad (4)$$

According to the LCL classes described in [1], the worst cases will be LCL classes 8 and 10 as they have the highest-nominal currents (8 A and 10 A, respectively) and the highest maximum limitation currents (11.2 A and 14 A, respectively). Junction temperature limits for transistors operating in space conditions are fixed as 110ºC or the maximum temperature specified on the semiconductor device minus 40ºC, whichever is lower [2]. It is considered that the LCL is going to be working once. This allows us to consider the SiC advantages of higher temperature devices. Therefore, the device limit in this work is set as the maximum device temperature minus 40ºC as a safety margin.

To choose the best device, a dissipation analysis, in nominal operation, has been carried out. The devices with the lowest power dissipation under nominal conditions were SCT3022AL, SCTW90N65G2V, C2M0040120D, and C2M0045170P. These devices dissipated about 3 W, while they are working in a class 10 LCL, carrying 10 A. Considering junction temperature during a failure, the transient thermal response of devices with a 150ºC limit (device limit) are shown in Fig. 6a), devices with a 175ºC limit (device limit) are shown in Fig. 6b), and devices with a 200ºC limit are shown in Fig. 6c). The safety temperature limit ($T_{junction}$ - 40ºC) is also shown for all cases (device limit with margin). For each case, the device limit represents the maximum junction temperature of the selected SiC devices.

It is important to note that the temperature limit (device limit with margin) cannot be exceeded during the trip-off time, depending on the LCL class. Considering a class 10 LCL, only the SCTW90N65G2V [28] complies with the correct trip-off times. The SCT3022AL [29] complies also with the safety times and exhibited the lowest dissipation losses (i.e. 2.2 W). For those reasons, the experimental results were produced for two different prototypes, with the same architecture but these two different SiC N-MOSFETs.

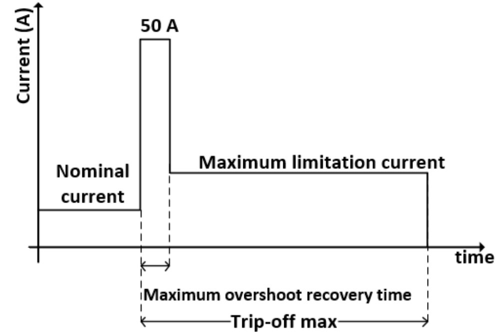


Fig. 3. Current behavior under short circuit

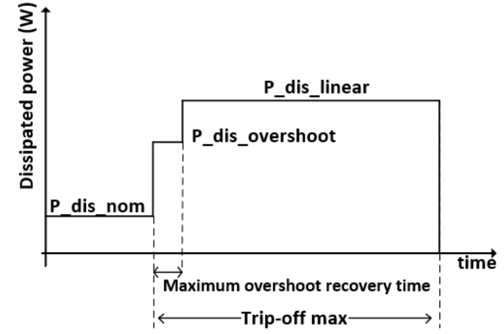


Fig. 4. Dissipated power under short circuit

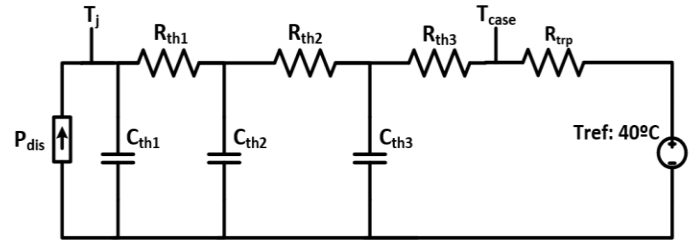
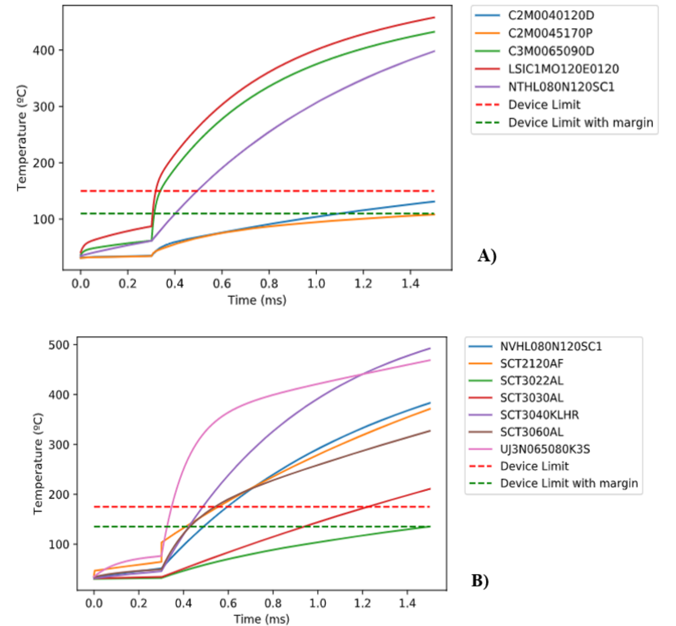


Fig. 5. Cauer network with the extra resistor R_{trp}



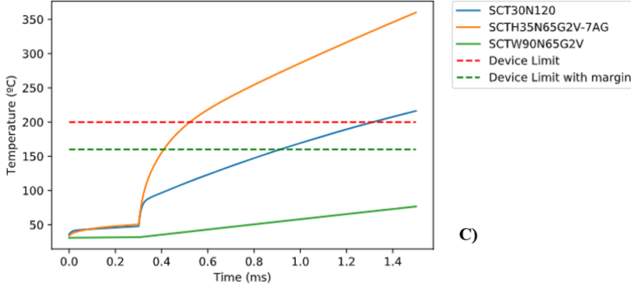


Fig. 6. Thermal impedance a) 150ºC, b)175ºC and c) 200ºC

III. PROPOSED SIC LCL DESIGN

The complete LCL design using a N-channel MOSFET is shown in Fig. 7. Being a space application, all the stages have been analog implemented using discrete components with space grade equivalents. All the LCL stages (auxiliary power supply, current sensor, current control loop, analog isolator, the control cell, timer, and the undervoltage lockout) are supplied using a voltage level, which will act as the voltage reference for the control circuitry. This voltage level between the bus voltage and the additional reference is V_{supply} (see Fig. 7). In this way, it is possible to comply with the requirements of the current sensor [32] regarding the maximum allowed voltage difference between power and sensing terminals. This architecture is based on [12] and [34], and the main disadvantage is that the reference voltage is the source terminal of a P-MOSFET in the auxiliary power supply.

A. Auxiliary power supply

All the circuitry for driving the N-MOSFET is supplied through an auxiliary power supply. This power supply is composed by a P-MOSFET, a TL431 circuit and a resistor (see Fig. 7). The V_{supply} level is fixed by the TL431 circuit which controls the gate-source voltage level of the P-MOSFET. This MOSFET drives all the current demanded by the control circuitry of the LCL architecture, withstanding the difference between the bus voltage (V_{bus}) and V_{supply}. Special care must be taken in the selection of this P-MOSFET because an increase of the bus voltage level generates higher power dissipation in the P-MOSFET. In this work, the dissipated power in the P-MOS is about 0.5 W.

B. Analog isolator (DCX)

The DCX (DC/DC Transformer) is the stage that communicates the current control loop to the SiC N-MOSFET gate-source voltage (each referring to a different voltage reference). It is worth noting that this control signal determines the operating point of the MOSFET, not only in ohmic and cut-off regions, but also in the active region. This analog isolator is based on a DC/DC isolated converter working in an open loop. This DC/DC converter is designed so its dynamic response does not affect significantly the dynamic of the current control loop. Therefore, it operates at a switching frequency of 4 MHz.

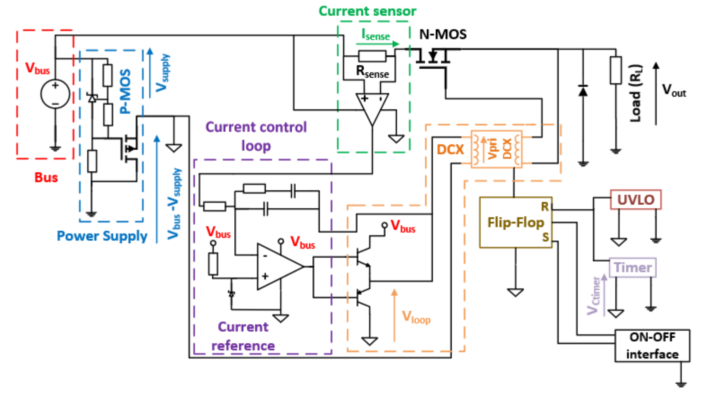


Fig. 7.SiC N-MOS LCL design

The DCX stage is based on an LLC topology (LLC-DCX). Fig. 8 shows the LLC-DCX schematic formed by a half-bridge inverter and a full wave rectifier. A detailed design guideline is provided in [33].

The DCX stages were designed using the First Harmonic Approximation (FHA) [35]. The half bridge output voltage (V_{bridge}) presents a square waveform with a duty cycle D close to 0.5, with a low level of 0 V and a high level of V_{in}. Hence, the Fourier series expression for the V_{bridge} is the one shown in (5).

$$V_{BRIDGE} = V_{in} \cdot D + \sum_{k=1}^{\infty} \frac{2}{k \cdot \pi} \cdot V_{in} \cdot sin(k\pi D) \cdot cos(kD\omega_s t) \quad (5)$$

The first harmonic amplitude (A_{FH}) is described in (6), with a maximum for a D of 0.5 being (7):

$$A_{FH} = \frac{2}{\pi} V_{in} \cdot sin(\pi D) \quad (6)$$

$$A_{FH} = \frac{2}{\pi} V_{in} \quad (7)$$

Fig. 9 shows the equivalent circuit diagram of the LLC-DCX converter under the FHA approximation. This approximation is used to analyze the resonant network behavior (Z_{tank}) when a sinusoidal input voltage is applied at its input. Resistors R_{p1} and R_{p2} model the resistive losses in both transformer windings. The design process is based on choosing the resonant frequency of the network formed by C_{tank} and L_{lk1}.

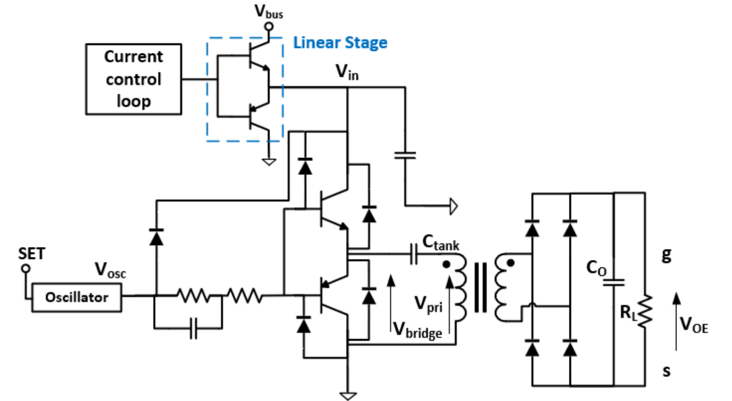


Fig. 8. LLC-DCX stage circuit

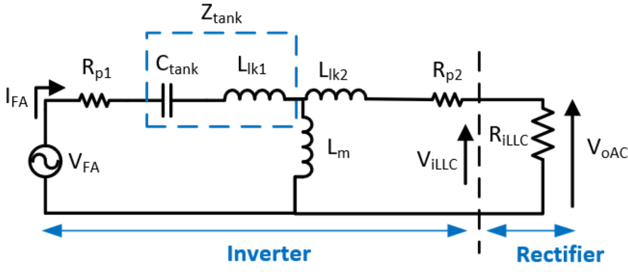


Fig. 9.DCX stage for the FHA analysis

Expression (8) shows the equivalent impedance (Z_{tank}) of the resonant network.

$$Z_{tank} = j \cdot \left(\omega_S \cdot L_{lk1} - \frac{1}{\omega_S \cdot C_{tank}} \right) \quad (8)$$

Where $\omega_s = 2\pi \cdot F_{sw}$ is the angular frequency for the switching frequency (F_{SW}). Regarding the full wave rectifier, the input equivalent impedance is described in [36], and its use is described in the literature [36],[37]. This full wave rectifier behaves as a resistor (R_{iLLC}) described in (9).

$$R_{iLLC} = \frac{8}{\pi^2} \cdot R_L \quad (9)$$

Where R_L is the load resistor in LLC-DCX topology. The voltage gain pf this stage is defined by the resonant network voltage gain ($G_{tankLLC}$). This R_{iLLC} determines the quality factor (Q_{tank}) of the resonant network at the switching frequency. The expression is described in (10).

$$Q_{tank} = \frac{\left(\frac{F_R}{F_{SW}}\right) \cdot \omega_s \cdot L_{lk1}}{R_e} \quad (10)$$

$$R_e = R_{iLLC} + Rp_2 + Rp_1$$

Where F_R/F_{SW} is the ratio between the resonant frequency for the resonant tank, and the switching frequency. The $G_{tankLLC}$ is defined with (11)-(13):

$$Z_1 = R_{iLLC} + Rp_2 + (j \cdot \omega_s \cdot L_{lk2}) \quad (11)$$

$$Z_{eq} = \frac{j \cdot \omega_s \cdot Lm \cdot Z_1}{j \cdot \omega_s \cdot Lm + Z_1} \quad (12)$$

$$Gtank_{LLC} = \frac{V_{iLLC}}{V_{FA}} = \left| \frac{Z_{eq}}{Rp_1 + Z_{tank} + Z_{eq}} \cdot \frac{R_{iLLC}}{Z_1} \right| \quad (13)$$

Therefore, with the $G_{tankLLC}$ value, it is possible to obtain the LLC-DCX stage gain (see (14)), which depends on $G_{tankLLC}$, the gain of the resonant tank and the amplitude of the first harmonic, A_{FH}:

$$G_{aisolatorLLC} = \frac{V_o}{V_{in}} = \frac{2}{\pi} \cdot sin(\pi \cdot D) \cdot Gtank_{LLC} \quad (14)$$

Apart from the value of the voltage at the gate, the other key factor that must be considered in the LLC-DCX design process is its audio-susceptibility bandwidth. Audio-susceptibility relates voltage variations between the input and the output voltage, which is precisely how the DCX translates the control loop voltage to the gate-source voltage of the transistor. The bandwidth value must be so that the overall current regulator complies with the European Cooperation for Space Standardization (ECSS) [1] requirements regarding the control loop speed to regulate the current. The bandwidth achieved is in the range of hundreds of kHz, offering a voltage gain wide enough to comply with these requirements. In this work, it is possible to establish a relationship between DCX bandwidth, Q_{tank}, and the F_R/F_{SW} ratio. Therefore, it is possible to analyze the bandwidth variation for a fixed Q_{tank} or a fixed F_R/F_{SW} ratio.

This analysis is performed though a series of PSIM circuit simulations. As a simplification, ideal MOSFETs are considered as the switching elements. The first analysis consists of a fixed Q_{tank} value modifying the F_R/F_{SW} ratio. Hence, it is possible to obtain the Bode diagrams that relate V_{OLLC} with V_{in} in the LLC-DCX stage.

The main steps for this analysis are:

1. For a fixed Q_{tank} value it is possible to establish a range of values for the resonant inductance (L_{lk1}).

2. For each L_{lk1} value the F_R/F_{SW} ratio can be obtained using expression (10), as shown in (15):

$$\frac{F_R}{F_{SW}} = \frac{Q_{tank} \cdot R_e}{\omega_s \cdot L_{lk1}} \quad (15)$$

3. With the L_{lk1} range of values and the F_R/F_{SW} ratios, it is possible to obtain the values for the resonant capacitors (C_{tank}), using expression (16):

$$C_{tank} = \frac{1}{\left[\left(\frac{F_R}{F_{SW}}\right) \cdot \omega_s\right]^2 \cdot L_{lk1}} \quad (16)$$

Therefore, for each F_R/F_{SW} ratio there are pairs of values for the L_{lk1} and C_{tank} parameters. Through these simulations it is possible to obtain the Bode diagram for each G_{tank}. Fig. 10 shows the different Bode diagrams, without the DC gain, for a fixed Q_{tank} value of 0.1818 and for a F_R/F_{SW} ratio variation between 0.63 and 2.53. The discontinuous line in Fig. 10 represents the -3dB gain drop. The highest bandwidth appears when the F_R/F_{SW} ratio tends to 1. However, if the ratio is higher than one, the bandwidth starts to drop. In this example, the highest bandwidth is 224.57 kHz for a F_R/F_{SW} ratio of 1.27, and the lowest bandwidth is 73.26 kHz for a F_R/F_{SW} ratio of 2.53.

The second analysis consists of having a fixed F_R/F_{SW} ratio while varying the Q_{tank} value. Again, the main idea is to analyze the bandwidth achieved following the variations of Q_{tank}. The steps are very similar to the previous analysis.

1. For a fixed F_R/F_{SW} ratio it is possible to establish a range of values for the resonant inductance (L_{lk1}).

2. For each L_{lk1} value, and using the fixed F_R/F_{SW} ratio, each C_{tank} value can be obtained using expression (16). Using expression (10) it is also possible to obtain the range of values for the Q_{tank} parameter.

3. Finally, for each Q_{tank} parameter it is possible to calculate a pair of values for the L_{lk1} and C_{tank} parameters. In this way, it is possible to produce the Bode diagram for each G_{tank}.

Fig. 11 shows the different Bode diagrams, without the DC gain, for a fixed F_R/F_{SW} ratio of 1.27 and for a Q_{tank} variation between 0.0912 and 0.3650. The discontinuous line in Fig. 11 represents the -3dB gain drop. The highest bandwidth appears for the lowest Q_{tank} parameter. In this example, the highest bandwidth is 224.57 kHz for a Q_{tank} of 0.0912, and the lowest bandwidth is 186.32 kHz for a Q_{tank} of 0.3650.

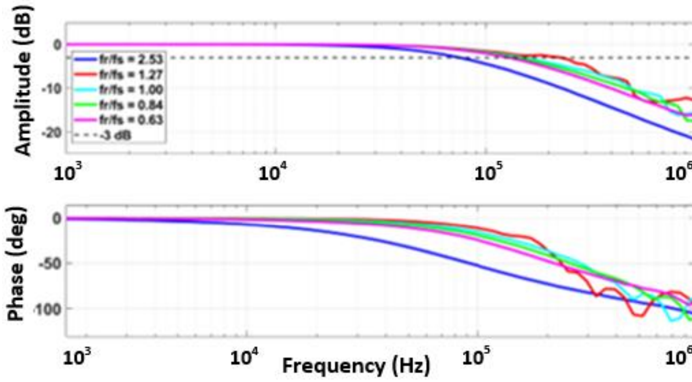


Fig. 10. Bode diagrams for a fixed Q_{tank} of 0.1818 changing the F_R/F_{SW} ratio

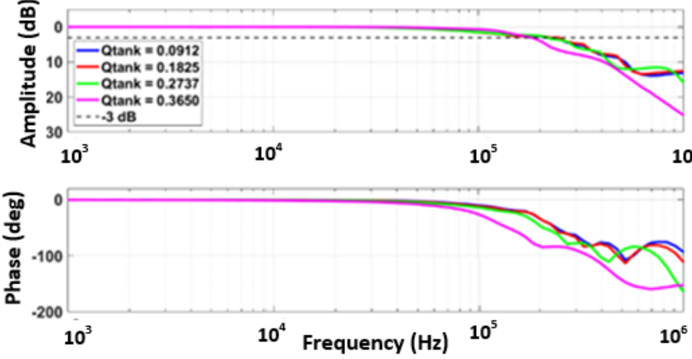


Fig. 11. Bode diagrams for a fixed F_R/F_{SW} ratio of 1.27 changing the Q_{tank} parameter

The analysis shows that for this DCX design it is possible to establish a connection between the F_R/F_{SW} ratio, the Q_{tank} parameter, G_{tank}, and the 3dB bandwidth. The highest Q_{tank}, implies the lowest 3dB bandwidth and the lowest G_{tank}. Therefore, in order to achieve high bandwidth combined with high gain, it is necessary to design the DCX stage with an F_R/F_{SW} ratio close to 1 and a low value of the Q_{tank} parameter. In the LLC-DCX implemented in this work, the Q_{tank} parameter is 0.092 and the F_R/F_{SW} ratio is 0.896, making it possible to achieve a G_{tank} of 1.53.

C. Current control loop

The current control loop design process is in explained in this section. This current loop is in charge of regulating the current to the reference value. This control loop is based on a type II regulator. When the current sensed in the LCL is lower than the reference, the integrator saturates to positive, having the maximum V_{GS} value in N-MOSFET, thus giving the lowest R_{DS} value. If the current measured by the sensor is above the limit, the value of the current loop control signal will fall reducing the V_{GS} voltage value of the N-MOSFET. This forces the MOSFET to operate in linear mode regulating the current and making it equal to the reference current. A proper tuning of the regulator must consider the dynamic of the current sensor, the current source defined by the current limiting MOSFET and the DCX audio-susceptibility.

The LT6105 [32] current sensor was used in this work. Its dynamic response was obtained using a SPICE AC analysis for frequencies up to 1 MHz, using the vendor provided SPICE simulation model. The result of the analysis was then approximated using a transfer function (G_{sensor}) composed of 3 poles and 2 zeros. The audio-susceptibility of the DCX (G_{uc_uciso}) was obtained by direct measurement of the prototypes using a frequency response analyzer [38].

These measurements were approximated by a transfer function. Fig. 12 shows the approximation of the experimental results for frequencies up to 100 kHz, with a 3 dB bandwidth of 145 kHz. This result is in line with the bandwidth predicted by the simulation shown in Fig. 10, according to the green trace for a F_R/F_{SW} ratio of 0.84. In the current design the F_R/F_{SW} ratio is 0.896.

Finally, the behaviour of the N-MOSFET in limitation mode, must be considered in order to model the transfer function (G_{i_uc}) between the DCX output voltage (u_c) and the sensed current (i). Fig. 13 shows the equivalent circuit diagram for the LCL small signal model and Fig. 14 shows the small signal model circuit between the DCX output and the N-MOSFET from Fig. 13. This transistor is modelled by its parasitic capacitances, its transconductance value (g_m), and the influence of the drain-source voltage (u_{ds}). The sensed current can be expressed as (17).

$$\hat{\imath} = g_m \cdot \widehat{ugs} + \widehat{uds} \cdot (1/R_{ds} + s \cdot C_{ds}) \tag{17}$$

As the V_{bus} level in the small signal model can be considered a short-circuit, the u_{ds} voltage can be expressed as (18).

$$\widehat{uds} = -\hat{\imath} \cdot (R_{sense} + Z_{load}) \tag{18}$$

Where Z_{load} models the impedance that the LCL sees as a load. In case of a short-circuit, this Z_{load} parameter will be zero. The gate-source voltage of the N-MOSFET (u_{gs}) can be expressed as (19), where $C_{in} = C_{dg} + C_{gs}$.

$$\widehat{ugs} = \widehat{uc} \cdot \left[\frac{1}{(Zo_{DCX} + R_{gate}) \cdot C_{in} \cdot s + 1}\right] + \widehat{uds} \cdot \left(\frac{Zo_{DCX} \cdot C_{dg} \cdot s}{Zo_{DCX} \cdot C_{dg} \cdot s + 1}\right) \tag{19}$$

Using (17), (18), (19) and dividing by u_c, it is possible to get the expression for the G_{i_uc} transfer function (20).

$$G_{i_uc} = \frac{g_m}{(Zo_{DCX} + R_{gate}) \cdot C_{in} \cdot s + 1} + \frac{1}{\frac{1}{(R_{sense} + Z_{load})} \cdot \frac{gm \cdot Zo_{DCX} \cdot C_{dg} \cdot s}{Zo_{DCX} \cdot C_{dg} \cdot s + 1} + \frac{R_{ds} \cdot C_{gd} \cdot s + 1}{R_{ds}}} \tag{20}$$

Hence, considering G_{sensor}, the audio-susceptibility G_{uc_uciso}, and G_{i_uc}, the current control loop plant is described in (21), which can be used to tune the regulator.

$$G_{LCL} = G_{sensor} \cdot G_{uc_uciso} \cdot G_{i_uc} \tag{21}$$

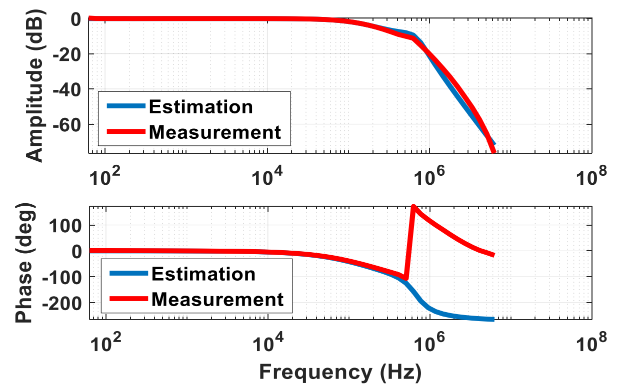


Fig. 12. LLC-DCX audio-susceptibility for an input voltage of 10 V

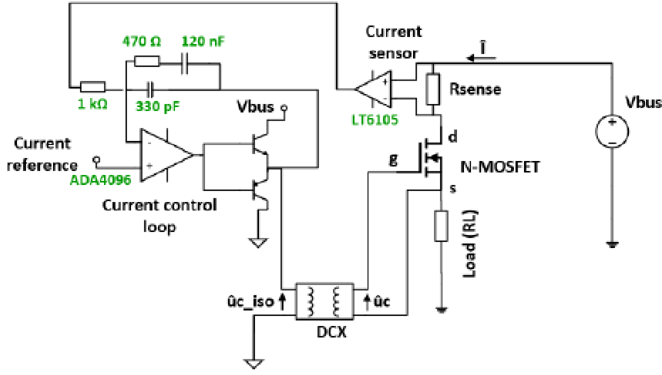


Fig. 13. LCL circuit for the small signal model

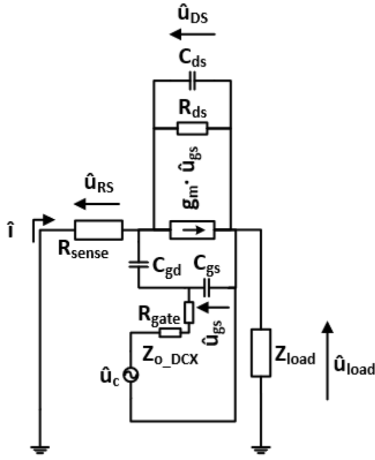


Fig. 14. Small signal model between the DCX output and the N-MOSFET

According to (20) the G_{i_uc} depends on the load impedance of the LCL (i.e. Z_{load}). The higher Z_{load} values, the worse dynamic response of the LCL. Therefore, different values for $Z_{load,}$ were included in the model to define worst cases:

1. A pure short-circuit
2. A resistor selected to get the I_{lim} value (Max resistance)
3. A pure inductance (Inductive)
4. An inductance in series with the resistor (L_R)
5. A LC filter with a short-circuit at its output (Filter)
6. The same LC filter with the resistor (Filter+R)

The LC filter represents the input filter of a DC/DC converter. The filter design process was adapted from [39], and was implemented following the schematic in Fig. 15, with L_f = 150 µH, C_f = 150 µF, C_b = 300 µF and R_f = 1.2 Ω.

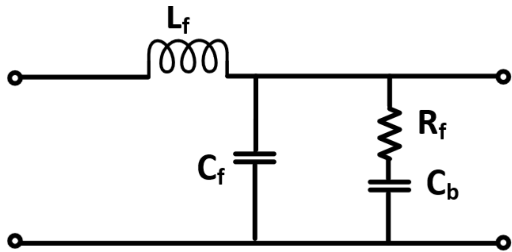


Fig. 15. LC filter design

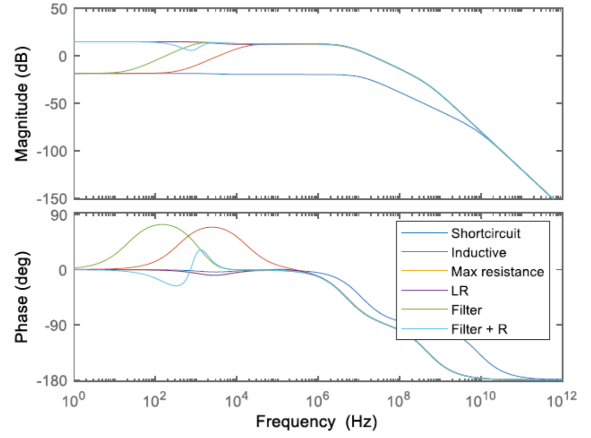


Fig. 16. Bode diagram of the G_{i_uc} transfer function for different Z_{loads}

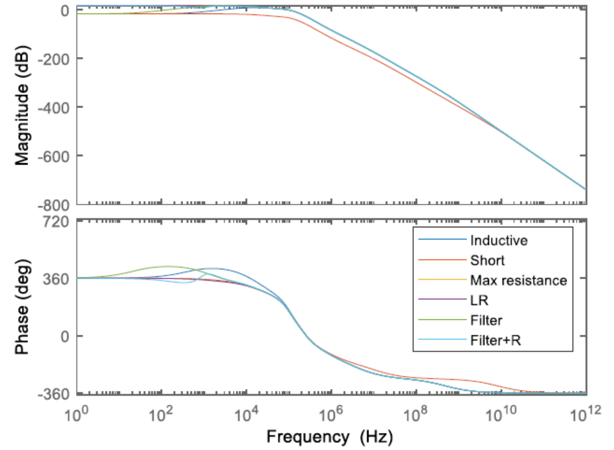


Fig. 17. Bode diagram of the G_{LCL} transfer function for different Z_{loads}

Fig. 16 shows the Bode diagram of the G_{iu_uc}. The worst case occurs in the "filter + resistor" case, due to the maximum load at the output of the LCL. Fig. 17 shows the Bode diagram for the G_{LCL} transfer function in (21).

D. Undervoltage Lockout stage (UVLO)

The undervoltage lockout stage automatically disconnects the load for a low bus voltage value. According to [1] a hysteresis system was implemented. Special care must be taken with the bus voltage measurement. The UVLO section needs to sense the bus voltage between its hot terminal and the bus reference. This information must be translated referred to the control reference, so the LCL disconnects the load.

To sense the bus voltage a current mirror was used. Fig. 18 shows the implemented UVLO circuit. The PNP I transistor is connected between V_{bus} and the bus reference through the R_{mirror_UVLO} resistor, generating the $I_{ref_mirror_UVLO}$ current. This current, related with the bus voltage level, is mirrored with the PNP II generating the $I_{_UVLO}$ current. This $I_{_UVLO}$ current will flow through the R_1 resistor or through the parallel between the R_1 and R_2 resistors. This pair of resistors stablished the reference of a TL431 [40] comparator. This implementation allows hysteresis in the UVLO. When the TL431 input voltage is higher than its reference voltage level (i.e. 2.5 V), its output voltage saturates to low, turning off the NPN_{set} bipolar transistor, connected to the SET terminal of the RS flip-flop. However, if the input voltage level in the TL431 is lower than 2.5 V, the SET terminal is connected to the control reference. This SET signal activates the DCX oscillator and, hence controls the LCL activation. When this SET signal is in the low level, the DCX will turn off, the same as the current limiting N-MOSFET.

E. Timer stage

As soon as the LCL starts limiting the current a timer must start. Once the trip-off time has elapsed, the LCL must be turned off if the MOSFET is still limiting the current. This trip-off time is selected so the transistor does not exceed its maximum junction temperature. Traditional LCL architectures have fixed times independent of the V_{DS} level. In the present work, the timer implementation is dependent on the V_{diff} level. V_{diff} is composed by the V_{DS} in the N-MOSFET plus the voltage drop in resistor R_{sense}. Fig. 19 shows the circuit diagram for the implemented timer stage. The V_{diff} voltage is sensed though a current mirror. The PNP_{tempI} transistor is connected between the bus voltage, through the R_{g1} resistor, and the N-MOSFET source terminal, using R_{mirror}. When V_{diff} voltage is higher than the base-emitter drop voltage, the PNP_{tempI} transistor is in ON-state, conducting the I_{ref_mirror} current. This current is mirrored using PNP_{tempII} and generating the I_{timer} current.

This current, I_{timer}, will be integrated through the RC network formed by C_{timer}, R_1 and R_2. The resistive divider formed by R_1 and R_2 is connected to the reference input of a TL431. In this way, when the voltage at the reference input of the TL431 is higher than its internal voltage reference, it saturates to low level, activating the PNP_{set} transistor, which connects the SET terminal to the control reference. When this happens, the DCX stage is turned off, thus turning off the LCL clearing the overcurrent. Once the LCL is turned off the NPN_{reset} transistor, which is connected in parallel with $C_{timer,}$ is turned on, discharging C_{timer}. This PNP_{reset} transistor short-circuits the C_{timer} capacitor until the LCL is in the ON-state, allowing for a new temporization to start when an overload occurs. As I_{ref_mirror} current is proportional to the V_{diff} voltage level, the C_{timer} charging time (i.e. the trip-off time) is proportional to the N-MOSFET V_{diff} voltage value.

F. Soft-start stage

During the current limiting process of the LCL, especially when the LCL tries to limit the current starting directly to a short-circuit, a high overshoot appears in the I_{sense} current. This can be alleviated by introducing a soft-start (SS) circuit. This circuit is connected directly in the current reference circuit. Fig. 20 shows the normal circuit for the current reference in black, and the additional soft start circuitry in red. There is a TL431 circuit in charge of establishing the reference value for the current, which is used in the current control loop. Using the PNP_{SS} transistor it is possible to control the current reference value using the SET terminal. When the SET signal is at a low level, the C_{SS} capacitor is short-circuited by PNP_{SS}, so the current reference is fixed to zero in the current control loop. But when the SET terminal turns to high level (i.e. when the DCX stage is working), the current reference for the control loop will rise to its final value mainly following the dynamics of the RC circuit comprising the C_{SS} capacitor and R_{bias}. Therefore, it is possible to reduce current overshoot when the LCL starts directly to a short-circuit.

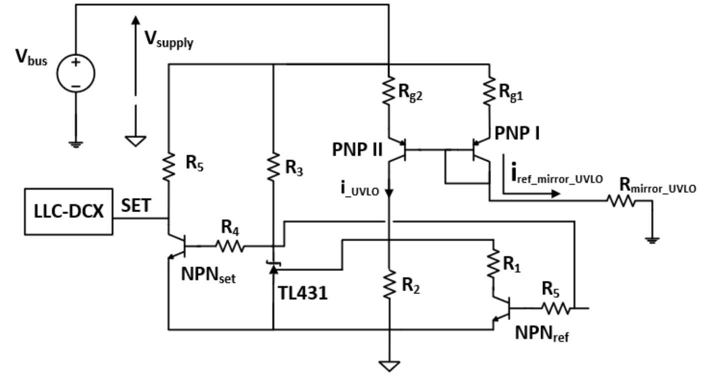


Fig. 18. Schematic of the proposed UVLO stage

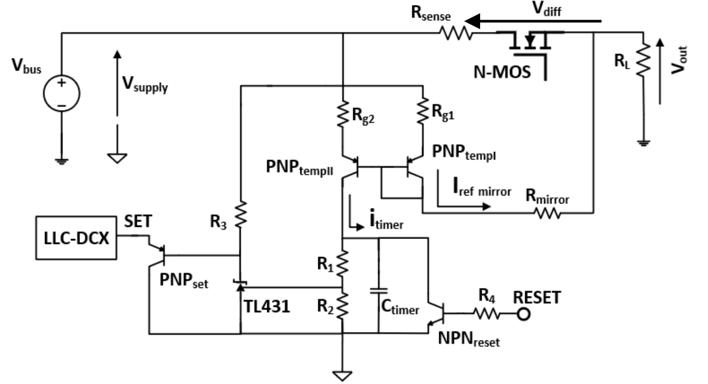


Fig. 19. Schematic of the proposed timer stage

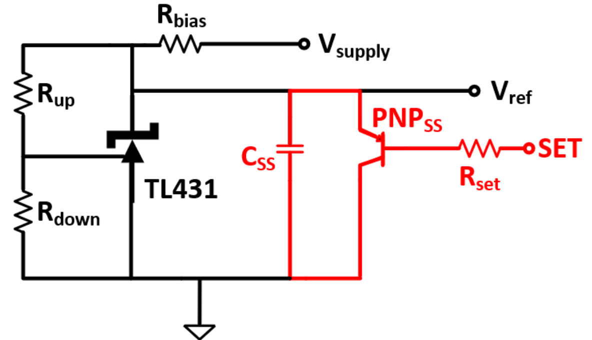
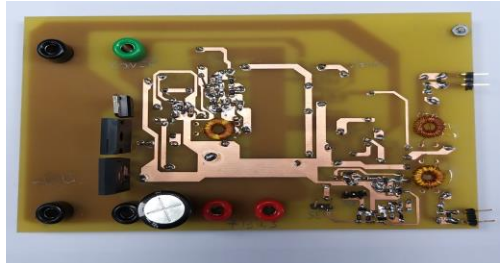


Fig. 20. Soft-start circuitry in the current reference stage

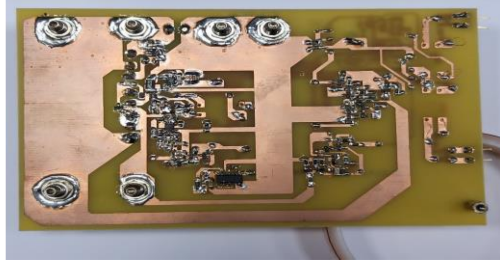
IV. EXPERIMENTAL RESULTS

Two prototypes were made according to the LCL design described in Section III, for the two selected SiC transistors (see Fig. 21). Fig. 22 shows the main waveforms for a class 10 LCL under a short-circuit at its output for a V_{bus} of 100 V. The LCL carries the nominal current (I_N), and the voltage level in the loop (V_{loop}) is driving to its highest value. Therefore, the V_{GS} voltage level is on its maximum value at the gate-source terminals of the N-MOS. V_{bridge} denotes the voltage level at the output of the half-bridge structure in the DCX. During the overload, there is an overshoot, and then, the LCL limits the sensed current, according to its reference level.

This is achieved by the current control loop, regulating the current through the V_{loop} and V_{GS} values. After the overload event, the timer stage starts working, turning off the LCL, according to the trip-off times of each LCL class. The V_{bridge}, and then V_{GS} goes to zero, turning-off the N-MOSFET. Consequently, the I_{sense} current turns off.



a)



b)

Fig. 21. LCL designed prototype, a) top layer, b) bottom layer

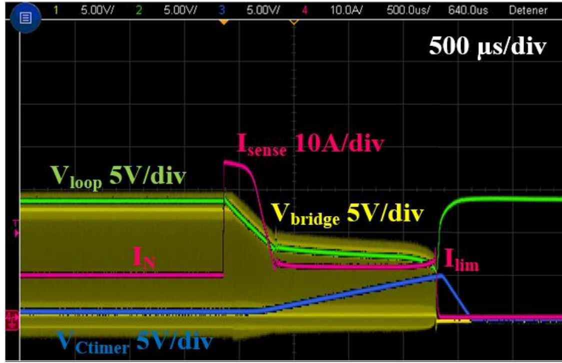


Fig. 22. LCL behavior with a short-circuit

The second test proofs the LCL activation directly to a short-circuit (the nominal current is zero). It is possible to see how the LCL regulates the current, through the control stage, to the reference value. After this activation, the timer section turns off the LCL, once the fixed time is elapsed. Fig. 23 shows the activation of the LCL directly to a short circuit without the soft-start circuit. Different trip-off times between Fig. 22 and Fig. 23 are due to the change in the C_{timer} value in the timer section. The highest overshoot value appears in the I_{sense} current, which is near 70 A. This situation is corrected by the implementation of the soft-start circuitry explained in Section III. Thus, Fig. 24 represents LCL working behaviour starting to a short-circuit, using the SS circuit. Comparing Fig. 23 with Fig. 24 it is clear that the current overshoot is lower than when no SS circuitry is used, and the sensed current increases until it reaches the limiting value set in the current control loop.

The third test shows the effect of the impedance placed at the output of the LCL. According to Section III, high values of Z_{load} on the LCL could generate an undesired dynamic behaviour, due to the dependency of the G_{i_uc} transfer function on the Z_{load} parameter. Fig. 25 shows the LCL operation with a LC filter connected at the LCL output. In this case, prior to the overload the LCL is carrying about 2.3 A, the reference current (I_{lim}) is 12 A, and V_{bus} is about 100 V. Fig. 25 shows that the LCL works correctly, regulating the current to the desired value. However, there are some initial oscillations, that do not affect the LCL operation, and the current is regulated correctly. Hence, the LCL behaviour for the worst Z_{load} case is properly verified.

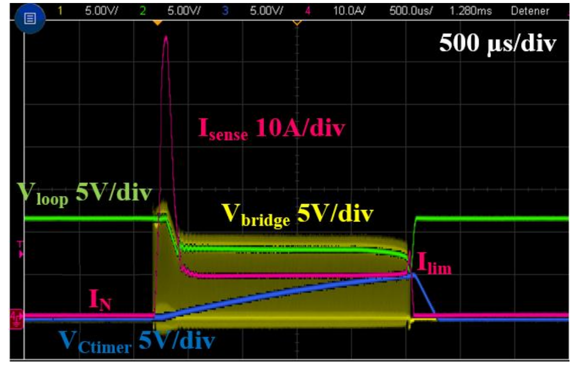


Fig. 23. LCL working behavior under a short-circuit test

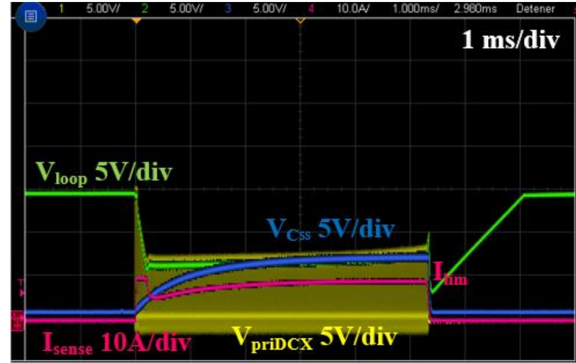


Fig. 24. LCL working behavior under a short-circuit test, using the SS circuit

The last test performed in this study presents a capacitor connection at the LCL output. This way, we can simulate the charging process of a converter supplied by the LCL. Fig. 26 shows the charging process of a 470 µF capacitor by depicting its voltage V_c, for a V_{bus} level of 100 V. The time to complete the charging process is 5 ms and the R_{sense} value was 0.02 Ω. Thus, the proposed LCL architecture has been tested in different situations, and in all the cases, this N-MOS LCL topology worked correctly, regulating the current in the fixed time and reliably turning-off the LCL after the trip-off time.

Finally, Fig. 27 shows a losses analysis for the SiC based LCL design, compared with a Hi-Rel P-MOS which could be used in a traditional LCL design. This analysis assumes that the LCL is not limiting the current and carrying 10 A, the class current. Regarding Fig. 27, the losses of the proposed SiC LCL design are about 5 W. On the other hand, considering only the ohmic losses of the IRHNA5S97260 [41] space qualified P-MOS 10 W are dissipated. This illustrates the power saving achieved by using the proposed LCL SiC design, in comparison with the classical P-MOS LCL architectures. In terms of efficiencies, and considering that most of the time, the LCL will be working in ohmic mode, driving the class current (I_N), it is possible to establish an efficiency level (η) according to expression (22):

$$\eta = 1 - \frac{I_N^2 \cdot R_{DS}}{P_{in}} \tag{22}$$

Considering (22), working in the same conditions for a bus voltage of 100 V and an I_N current of 10 A (same input power, P_{in}), the efficiency of the LCL based on a SiC N-MOS is about 99.78%, while the efficiency considering the IRHNA5S97260 Hi-Rel, space qualified P-MOS is about 98.98%. In terms of saved power, the loss breakdown in Fig. 27 shows a significant reduction of losses by using the LCL based on a SiC N-MOS device.

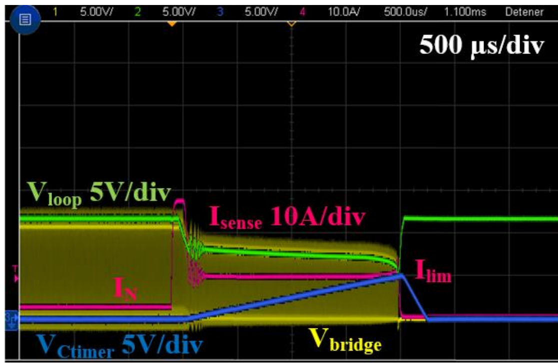


Fig. 25. LCL working behavior under a short-circuit test using an LC filter

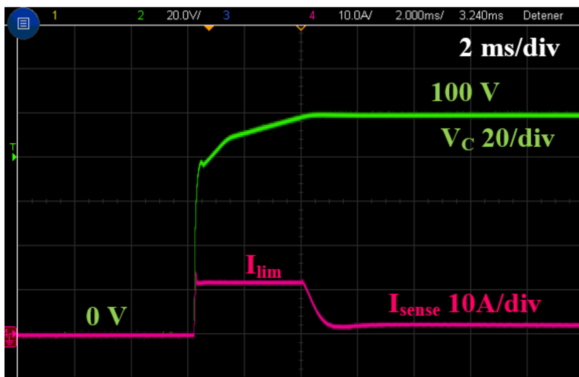


Fig. 26. Charging process of a capacitor at the LCL output

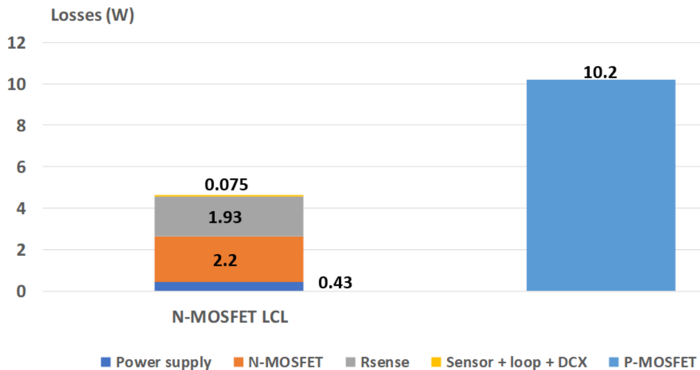


Fig. 27. Losses comparison between the SiC N-MOS LCL and a space qualified P-MOS, for a class 10 LCL using a V_{bus} of 100 V

For these working conditions, the conduction losses alone using the SiC N-MOS are about 2.2 W, while the same losses using the Hi-Rel space qualified P-MOS are about 10 W. This reduction of power losses, and the suggested capacity of the SiC based transistors to work at higher temperatures, are the key points in working with these SiC channel N devices in the LCL context.

V. CONCLUSIONS

This work presents an LCL design using a SiC N-MOS as the main switch. This design also includes some guidelines for the DCX stage in charge of controlling the N-MOSFET, in terms of how the bandwidth for the application can be controlled.

A class 10 LCL has been designed following the guidelines of the proposed architecture for a bus voltage of 100 V. A class 10 LCL bases on the presented design has been tested, proving its correct working behaviour limiting the current to the reference level. The dynamic of the LCL can be easily tuned, according to the analysis presented, making possible to adapt this design for higher bus voltage levels. Regarding dissipation, this SiC based LCL architecture brings a significant reduction of power losses, which also brings the possibility to reduce the overall losses in the satellite distribution system. Whilst no specific radiation tests were performed over the selected SiC transistors, the presented design could be used for any forthcoming Rad-Hard SiC device.

ACKNOWLEDGEMENTS

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