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High-Efficient Electrolytic-Capacitor-less Off-Line LED Driver with Reduced Power Processing

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***Abstract*— In this paper, an integrated parallel buck-boost and boost converter (IPB^{3}C) is proposed as an electrolytic-capacitor-less light-emitting diode (LED) driver. The IPB^{3}C provides a high power factor (PF) and low total harmonic distortion (THD). The driver is composed of two converters that are connected in parallel, using just one controlled switch. The buck-boost duty is to deliver constant power to the LED, while ensuring a good PF. The boost converter is employed to cancel the low-frequency ripple at the LED. In return, this decreases the flicker effect and only a relatively small capacitance is needed to fulfill the standard requirements. The buck-boost converter handles the full power of the LED, while the boost converter handles only a portion of the LED power. Thus, better efficiency is ensured by this parallel configuration compared to conventional cascaded integrated converters. Moreover, the voltage across the switch is low, as it is the higher, whether buck-boost or boost converter, but not the addition of both. In this paper, the IPB^{3}C is analyzed, and its design methodology is presented. A universal input voltage range prototype of the proposed converter supplying an LED lamp of 108 V/ 0.35 A is presented. The prototype shows high PF, nearly equal to one, very small THD, nearly zero, output voltage ripple of 4.5 %, output current ripple of 19 %, and high efficiency, equal to 92.4 %. Moreover, the converter requires the use of a bulk capacitance of only 68 μF, while the required output capacitance is just 1 μF.**

Keywords—electrolytic-capacitor-less LED driver, integrated converters; integrated parallel buck-boost and boost converter; high efficiency LED driver; Off-line LED driver; power factor correction; high power factor, low current THD.

I. INTRODUCTION

Since the 1960s, when light-emitting-diodes (LEDs) were first developed [1-3], they have been replacing little by little the conventional sources of light, until they have become the most popular lighting source in a wide variety of applications. This has been possible owing to their long lifetime, which is usually quoted as 25,000 to 50,000 h, as declared by the LED manufacturers and standard organizations [4]-[6]. Besides, they present higher efficacy compared to other light sources [7], [8]. Besides, they provide other features like smaller size, fast response, robustness, reliability, and good color rendering index [9]-[15]. However, LEDs cannot be connected directly to the mains due to their low internal impedance; thus making it necessary for their driving through a current-controlled power supply [3], [7], [16]-[19].

To assure the advantages offered by this new technology, an electronic converter to drive the LEDs should be well designed to fulfill all required standards. Working with a luminaire load, fulfilling the IEC 61000-3-2 Class C standard [20] concerning the harmonic content of the input current becomes a must [21]. Besides, the PF must be higher than the level specified by the U.S. Energy Star program [22].

Traditionally, a single-stage driver is used to operate as a power factor correction (PFC) stage and as a constant output current source, simultaneously. Both, the buck and flyback converters are the most used topologies to implement single-stage LED drivers. Both converters show accurate output current control and acceptable power quality figures, such as good PF and low THD, for low and medium power applications [23]-[24]. To ensure high PF, the loss-free resistance characteristic of the buck-boost operating in discontinuous conduction mode (DCM) is used. However, the operation in DCM increases electrical stress over the converter components. Thus, when operating with a single-stage driver, a compromise needs to be made to choose between attaining high power quality or high efficiency.

To fulfill the standards and regulations, the two-stage LED driver configuration has been proposed. Two-stage drivers are composed of a PFC stage and a Power Control (PC) stage in cascade [25]. However, although two-stage converters show a significant good operation, this structure shows some drawbacks as well. Such as a higher number of components; having at least two active switches, which means two gate drivers and associated circuitry, thus producing bigger size and higher cost [17], [26]-[27].

A promising solution to overcome the above-mentioned drawbacks is given by integrated converters, which are two-stage converters implemented sharing a single active switch, which usually provides lower switching losses and requires only one gate driving circuit. Therefore, they keep the good

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operation of the two-stage while they retain some of the advantages of single-stage converters [11][12], [28]-[36].

Conventional integrated converters solve the power quality regulations and standards, such as power factor and total harmonic distortion. However, in order to fulfill the flicker standard, they require the presence of a bulk ripple filter capacitance. Thus, a novel structure is proposed to fulfill both power quality and flicker standards and regulation, the parallel two-stage converters. It consists of a PC stage operating as a PFC stage and a second stage operates as a Ripple Reduction (RR) stage [37]-[47]. The following converters were found in the literature: flyback operating as PFC and a bidirectional buck/boost parallel stage [37]-[39], flyback operating as PFC and a buck parallel stage [40]-[41], buck-boost operating as PFC and a buck parallel stage with power flow control switch [42], active clamp flyback PFC stage and floating capacitor full-bridge [43]-[44], buck-boost operating as PFC and a buck parallel stage [45], and buck-boost operating as PFC and a flyback parallel stage [47]. The proposed converter is a novel combination, where the PFC stage consists of a buck-boost converter and the RR stage consists of a boost converter. Moreover, the proposed solutions in [37]-[47] use two or more controlled switches, which in return require additional control and sensing circuitry. However, the proposed technique is an integrated parallel converter that eliminates the LED ripple using a parallel RR stage, using just one controlled switch.

This paper is an improved version of the conference paper in [48], which proposes a fully functioning electrolytic-capacitor-less LED driver based on the integrated parallel buck-boost and boost converter (IPB^{3}C) supplying an LED luminaire load of 38 W. In comparison with the conference paper, additional information has been added regarding the efficiency analysis and the operation of the converter, the design and prototype implementation, as well as the experimental verification of the proposed converter. The proposed driver features high PF, low THD, low current ripple, high efficiency, and compact design. Moreover, this version of the paper provides a mathematical analysis of the efficiency comparison between the conventional cascaded integrated converters and the proposed parallel integrated converter. The conventional two-stage driver operates in cascaded mode, which means that the power is handled by the first stage, later the second stage, and then finally goes to the LED. However, the proposed converter implements a Power Control (PC) stage, whose main duty is to deliver the necessary power to the output LED. Also, it uses a Ripple Reduction (RR) stage, whose main duty is to eliminate the output LED ripple, but this stage only processes a part of the output power. Thus, there is no need for a bulky capacitor, and in return, an electrolytic-capacitor-less driver can be implemented. The proposed driver presents a ripple reduction technique through energy processing similar to that presented in [49], [50], but using only one single controlled switch. Furthermore, the proposed driver ensures a higher overall efficiency compared to the conventional integrated converter.

Fig. 1 shows the block diagram of the proposed converter, which is implemented using a buck-boost converter in the PC stage, and a boost converter in the RR stage. The reason for choosing the buck-boost converter in the PC stage is its high PF operating in DCM. Thus, the driver does not require any complex control or regulation circuitry to fulfill all requirements and standards.

In order to reduce the output ripple, the output LED voltage is generated from the PC stage output voltage subtracting from it the RR stage input voltage. The RR stage input voltage will be in reverse polarity of that of the PC stage. Thus, the low-frequency ripple will be subtracted so that only the average value will be applied to the output.

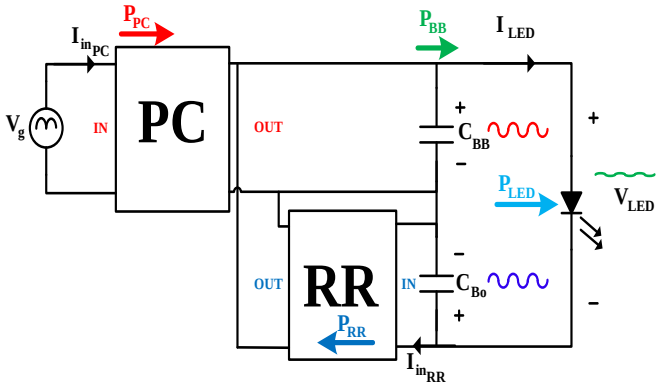


Fig. 1. Block diagram of the proposed ripple reduction technique.

This paper is organized as the following: in Section II the IPB^{3}C is presented. Section III shows the operation principles of the proposed IPB^{3}C, as well as the converter analysis, the efficiency estimation, and the average model. The design procedure is illustrated in section IV, while the experimental results are shown in section V. Finally, a brief conclusion about the contribution of this paper is presented in Section VI.

II. Derivation of the Proposed IPB^{3}C

Fig. 2 shows the electric schematic of the two converters before integration. The buck-boost converter's role is to operate as a PC stage while keeping a high PF similar to single-stage LED drivers. Thus, it will be operating in DCM to behave as a resistive load for the line. The boost converter's role is to operate as a RR stage, in order to decrease the required capacitance to fulfill the IEEE flicker standards. The benefits gained from this structure are the following:

- No bulk capacitor is needed; thus, it offers a long lifetime, compact, and low-cost LED driver.
- The driver process less power compared to conventional cascaded integrated converters; thus, higher efficiency is obtained.
- The control can be implemented using a conventional output current controller; thus, no extra complex control is needed.

In conclusion, it is a more compact and lower cost solution compared to the existing in the literature, featuring higher efficiency and longer lifetime, while no extra complex circuitry is needed. However, the main disadvantage of this topology in the version illustrated in Fig. 2 is the necessity of two active switches with two gate driving circuits and two controllers.

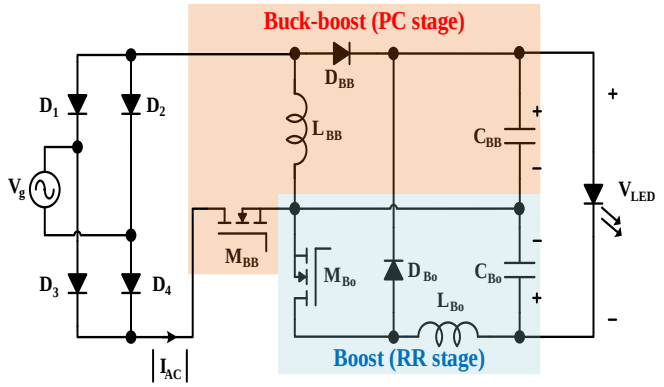


Fig. 2. Structure of the electrolytic-capacitor-less parallel buck-boost and boost converter.

III. Operational Principles of the Proposed IPB^{3}C

The integration of the two converters can be performed to keep the same operating behavior and features while simultaneously eliminating one of the two active switches. Fig. 3 shows the electric diagram of the integration of the buck-boost and boost converters, namely integrated parallel buck-boost and boost converter (IPB^{3}C). The PC stage buck-boost converter is made up by L_{BB}, D_{BB}, C_{BB}, and M_I, while the RR stage boost converter is formed by L_{Bo}, D_{Bo}, D_I, C_{Bo}, and M_I.

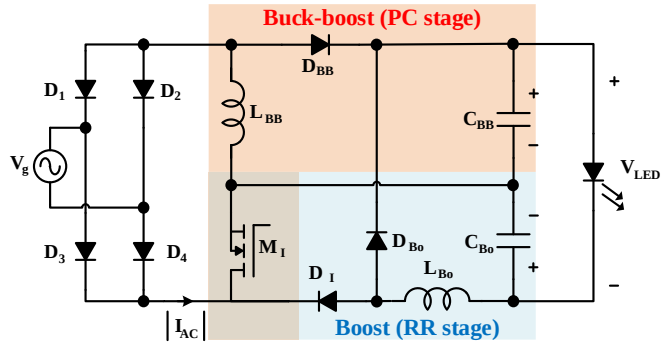


Fig. 3. Schematic of the electrolytic-capacitor-less integrated parallel buck-boost and boost converter.

A. Operation Principle

Since the proposed topology is a single controlled switch converter, there are only two main states: on-state and off-state. However, the DCM operation of the buck-boost and boost converters splits the off-state into three intervals. Fig. 4 and Fig. 5 illustrate the main current waveforms within a high-frequency switching period and the equivalent circuits, respectively.

In the following, a concise explanation for each interval is given:

- Interval I

During this interval, the main switch M_I is turned on. While the switch is on, both inductors are energizing. Thus, a current i_{BB} flows in the buck-boost input loop, coming from the AC grid to energize the buck-boost inductance. Meanwhile, a current i_{Bo} flows in the boost input loop, coming from the boost capacitor, and energizing the boost inductor. The current is increasing linearly in both inductors.

- Interval II

This interval starts with the turn-off of the main switch M_I. During this interval, both buck-boost and boost converters

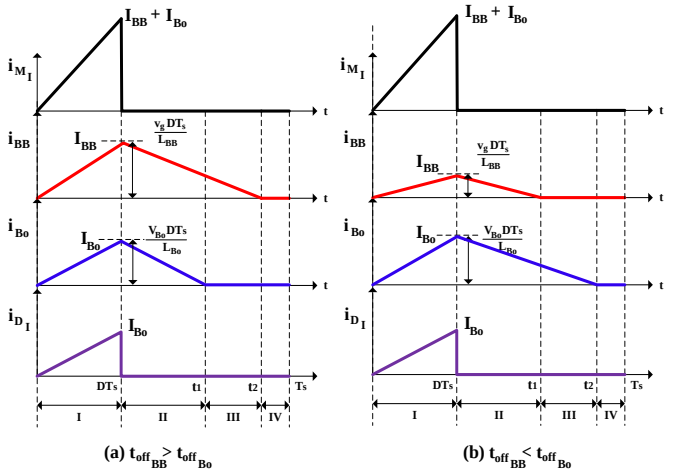


Fig. 4. Main current waveforms of the IPB^{3}C operating in DCM, within a high-frequency switching period; (a) when $t_{off_{BB}} > t_{off_{Bo}}$ around the peak line voltage, (b) when $t_{off_{BB}} < t_{off_{Bo}}$ for low values of the line voltage.

inductors are de-energizing. The buck-boost inductor is de-energizing, sending the power to the buck-boost capacitor through the buck-boost diode D_{BB}. Meanwhile, the boost inductor is de-energizing delivering the power to the buck-boost capacitor. Concerning, the output LED current, it is continuously delivered by the output buck-boost capacitor.

- Interval III

Interval III starts when one of the two inductors' current reaches zero so that it is entirely de-energized. Fig. 5 (c) and Fig. 4 (a) show interval III for the case where the boost inductor current reaches zero, while the buck-boost inductor current is still conducting. Concerning Fig. 4 (b), it shows the case when the buck-boost inductor current reaches zero and the boost inductor current is still conducting.

- Interval IV

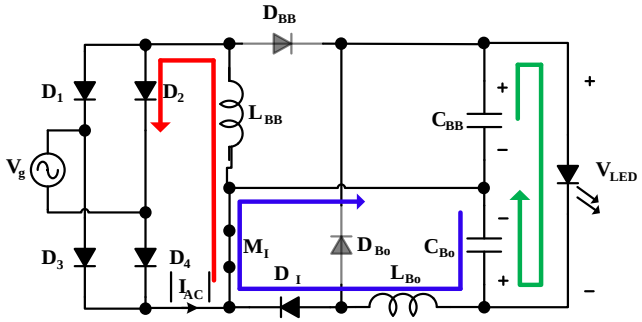
Finally, interval IV represents the period where both inductors are fully discharged. However, concerning the current going to the LED, it is continuous owing to the output capacitor presence.

This integration is an over-current integration, which means that the current of the integrated switch will be the addition of both converters' currents. However, the voltage across the switch will not be the addition of the voltage across each switch in the converter before integration, but it will be the highest of them. The voltage across the switch in buck-boost operating in DCM is the addition of input and output voltages when the inductor is de-energizing, while it will be equal to input voltage in the idle interval. Conversely, the voltage across the switch in the boost operating in DCM is the output voltage when the inductor is de-energizing, while it will be equal to the input voltage in the idle interval.

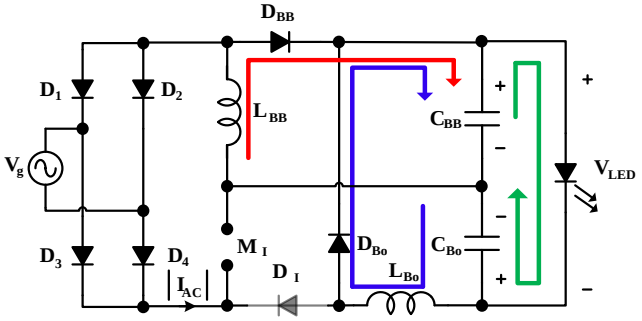
B. Mathematical Analysis

This section presents the operation equations. Their detailed derivation is presented in [48]. For the sake of simplicity, the analysis will consider the converter in its ideal state. An ideally sinusoidal line voltage waveform will be considered as input voltage, expressed as $v_g(t) = V_g \sin(2\pi f_l t)$.

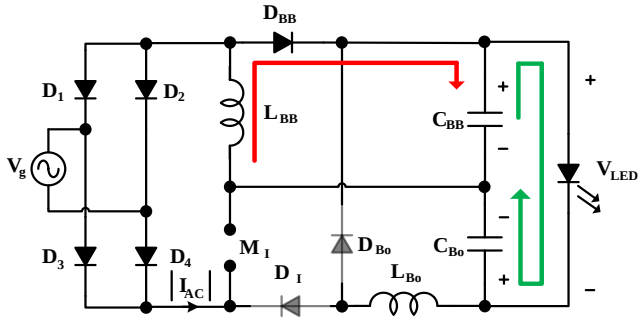
The converter contains three main power flows, which can be listed as the following:



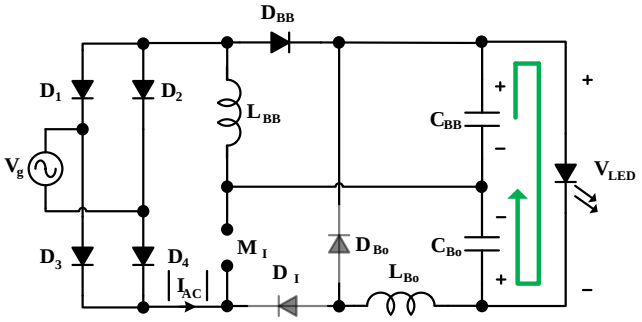
(a) Interval I : 0 < t < DTs



(b) Interval II : DTs < t < t1



(c) Interval III : t1 < t < t2



(d) Interval IV : t2 < t < Ts

Fig. 5. Equivalent circuits of the IPB[3]C operating in DCM.

- Average input power

It is the power coming from the grid; it is expressed by the following:

$$P_{PC} = \frac{V_g^2 D^2}{4 L_{BB} f_s} \quad (1)$$

Where P_{PC} is the power of AC main, V_g is the grid peak voltage, D is the main switch duty cycle, L_{BB} is the buck-boost inductance, and f_s is the switching frequency.

- Average RR stage power

It is the power handled by the RR stage, and it is expressed by the following:

$$P_{RR} = \frac{V_{Bo}^2 D^2}{2 L_{Bo} f_s} \left(\frac{V_{BB}}{V_{BB} - V_{Bo}} \right) \quad (2)$$

Where V_{Bo} is the boost input voltage, L_{Bo} is the boost inductance, and V_{BB} is the buck-boost output voltage.

- Output power

It represents the power going from the buck-boost output to the LED plus the power going to the boost converter. Considering the converter in ideal conditions, the following relations are found:

$$P_{BB} = I_{LED} * V_{BB} = I_{LED} * V_{Bo} + I_{LED} * V_{LED} = P_{RR} + P_{LED} \quad (3)$$

$$P_{LED} = P_{BB} - P_{RR} = P_{PC} \quad (4)$$

Thus, the input power and RR stage power can be expressed as the following:

$$P_{RR} = I_{LED} * V_{Bo} \qquad P_{PC} = I_{LED} * V_{LED} \quad (5)$$

Using (1), (2), and (5) a relation between the buck-boost output voltage and the boost input voltage is found:

$$V_{BB} V_{Bo} = \frac{V_g^2 L_{Bo}}{2 L_{BB}} \quad (6)$$

An additional relation between the buck-boost output voltage and the boost input voltage is found from the output loop, as follows:

$$V_{BB} = V_{Bo} + V_{LED} \quad (7)$$

C. Efficiency estimation

Concerning the conventional cascaded converter, the efficiency of the power flow considering losses can be expressed as:

$$\eta_{PC} = P_{LED} / P_{PFC} \quad (8)$$

$$\eta_{PFC} = P_{PFC} / P_{PC} \quad (9)$$

Where P_{PFC} is the power handled by the PFC stage, η_{PFC} is the efficiency of the power factor correction (PFC) stage, and η_{PC} is the efficiency of the PC stage.

Thus, the total efficiency of the driver is expressed as the following:

$$\eta_{total} = \frac{P_{LED}}{P_{PC}} = \eta_{PFC} * \eta_{PC} \quad (10)$$

Concerning the parallel integrated converter, the power handled by the RR stage is not the full power of the LED load. The ideal power flow equations are illustrated in (1)-(4); however, if the losses are considered, the equations are as follows:

$$P_{BB} = \eta_{PC} * P_{PC} + \eta_{RR} * P_{RR} \quad (11)$$

$$P_{LED} = P_{BB} - P_{RR} = \eta_{PC} * P_g - (1 - \eta_{RR}) * P_{RR} \quad (12)$$

The power processed by the RR stage is a function of the LED power. This factor is a function of the converter

inductances. Thus, the RR stage power can be expressed as the following:

$$P_{RR} = k * P_{LED} \tag{13}$$

Where k is the RR stage power-sharing factor. The relation between the inductance ratio and k can be expressed as the following:

$$\frac{L_{Bo}}{L_{BB}} = \frac{2V_{LED}^2}{V_g^2} k(k+1) \tag{14}$$

Using both (12) and (13) an expression for the total efficiency of the parallel integrated converter is found:

$$\eta_{total} = \frac{P_{LED}}{P_{PC}} = \frac{\eta_{PC}}{1 + k * (1 - \eta_{RR})} \tag{15}$$

To better illustrate the idea of the parallel integration and its effect on the efficiency, an example is studied. Estimating the efficiency of the PFC buck-boost is equal to 94 %, and the efficiency of the boost is equal to 96 %, the efficiency of the conventional integrated converter will be equal to the product of both efficiencies, which is 90.2 %, as shown in Fig. 6. For a fair comparison, the conventional cascaded converter is considered operating in DCM and using a simple control strategy. However, concerning the parallel integration, the efficiency depends on the RR stage power-sharing factor. The power circulating into the RR stage depends on the inductance ratio and, in return, on the factor k. Fig. 6 shows the efficiency of the parallel integration in terms of the inductance ratio L_{Bo}/L_{BB} as well as the k factor. Fig. 6 is drawn using the equations presented in (14) and (15). Fig. 6 also shows the ripple attenuation obtained by simulation as a function of the inductance ratio. The ripple attenuation is the percentage of ripple decrease compared to the ripple in the case that the RR stage is not active. If an example is taken for an inductance ratio below 2, for instance, at an inductance ratio equal to 1, the efficiency of the parallel integration is nearly 91.5 % compared to the 90.2 % shown by the conventional cascaded parallel integration; moreover, a ripple reduction of 90 % is attained. However, if the ripple reduction is desired to be boosted up to 95 %, it would require an inductance ratio equal to 4, which will decrease the efficiency to 88.5 %.

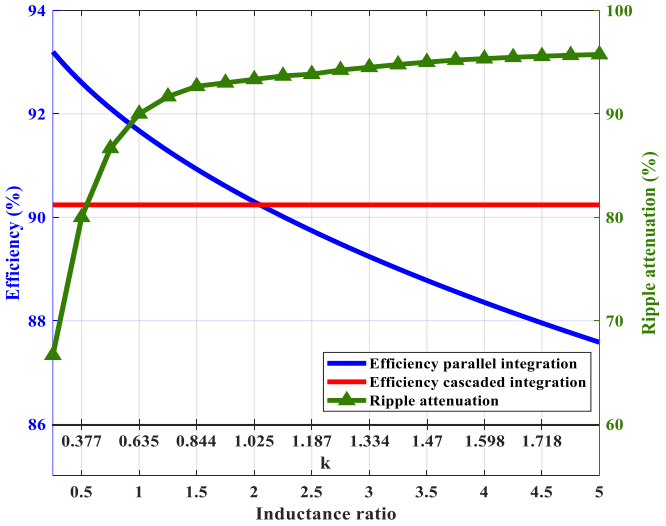


Fig. 6. The efficiency of both integration methodologies as well as the ripple attenuation percentage with respect to the inductance ratio (boost inductance over buck-boost inductance L_{Bo}/L_{BB}), V_{LED} equal to 108 V and line voltage is equal to 110 V_{rms}.

D. *Averaged Model*

For a better illustration of the converter's operation, an averaged model has been developed as shown in Fig. 7. The averaged model is helpful in terms of understanding the power flow in the converter. As well as it is a faster way to check, by simulation, the magnitude of the voltages and currents in all elements without considering the high-frequency switching effect. The values of the buck-boost and boost resistances used in the model are given by [19]:

$$R_{BB} = \frac{2L_{BB}f_s}{D^2} \tag{16}$$

$$R_{Bo} = \frac{2L_{Bo}f_s}{D^2}\left(\frac{V_{BB} - V_{Bo}}{V_{BB}}\right) \tag{17}$$

An approximation in the boost equivalent resistance can be considered if $V_{BB} >> V_{Bo}$, then the boost behaves almost as a pure resistance of the following value:

$$R_{Bo} \approx \frac{2L_{Bo}f_s}{D^2} \tag{18}$$

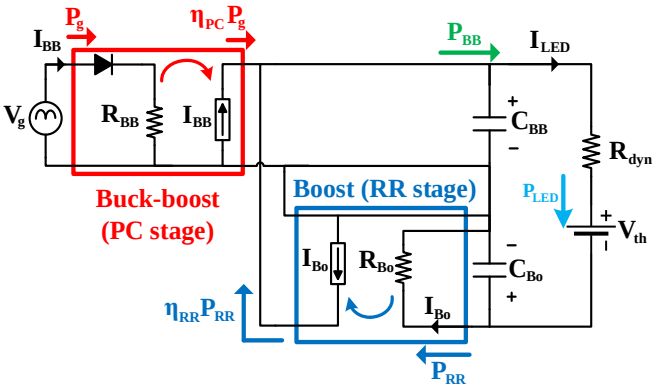


Fig. 7. Averaged model of the proposed IPB^{3}C LED driver.

IV. Design Procedure of the Laboratory Prototype

Using the previously determined equations and the averaged model illustrated in Fig. 7, a design is made to supply an LED luminaire of 108 V/ 350 mA, resulting in 38 W of output power. The line voltage and frequency are 110 V_{rms} and 60 Hz. The switching frequency selected for this driver is 40 kHz. Both buck-boost and boost inductances are selected in order to have a full DCM operation for the converter and to ensure a low circulating power in the driver.

The design of the prototype starts by selecting the inductance ratio, as a trade-off between the efficiency and the percentage of ripple reduction must be taken. The first step is to set the value of the buck-boost inductance. This selection aims to decrease the peak current as much as possible, while keeping the DCM operation. The suitable value based on this methodology and found from (1) is equal to 500 µH. Later, a selection of the k factor is done, in order to decrease the ripple as much as possible while keeping the required efficiency. The value of k is selected to produce a circulating power equal to 40 % of the LED power ($k = 0.4$), which will make a significate reduction in the ripple of the LED current of almost 80 %, keeping the efficiency higher than in the conventional cascaded circuit estimated to be 92.7 %. Finally, from (14) and Fig. 6, the inductance ratio is equal to 0.5, and in return, the boost inductance is equal to 250 µH.

Later, after selecting the values of the inductances, the effect of the input voltage variation needs to be studied. (14) shows that for fixed values for the inductances and LED voltage, the change in input voltage will change the k constant value. Thus, the change in the k factor will affect the operating point and, in return, the efficiency and LED current ripple. The increase in the input voltage will increase the percentage of circulating power in the parallel RR stage. Fig. 8 shows the efficiency and LED current percentage with respect to input voltage variation from 90 V to 250 V. The efficiency is calculated by calculating the value of k from (14) then obtaining the efficiency from (15). The ripple percentage is found from the simulation by changing the input voltage value and check the effect on the LED current. The increase in input voltage will lead to an increase in the k factor and, in return, to a decrease in both the LED current ripple percentage and converter efficiency.

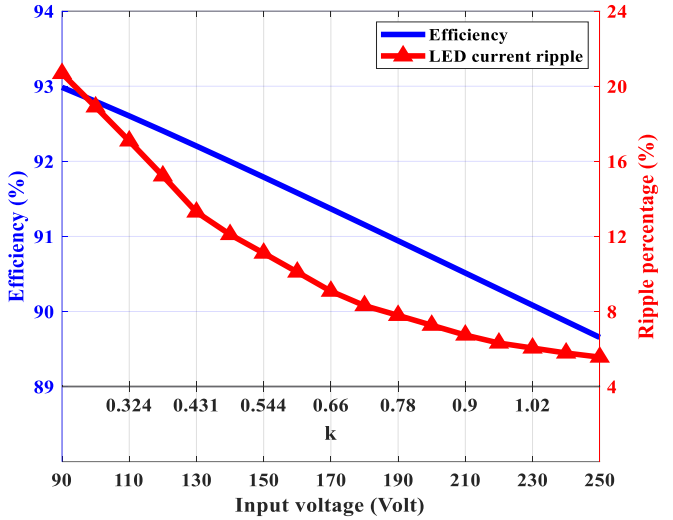


Fig. 8. Efficiency and ripple percentage with respect to the input voltage.

The LED chosen for the testing is an LW W5SG Golden Dragon, while the luminaire load is composed of a series of 30 LEDs. The capacitance selection is made after estimating the linear model of the LEDs to keep the ripple of the LED current lower than the recommendation given by IEEE Std. 1789-2015 [51]. The I-V characteristic was experimentally obtained in the laboratory to find the actual values of the dynamic resistance and the threshold voltage. Thus, the threshold voltage is found to be equal to 94 V and the dynamic resistance is equal to 40 Ω.

Table I shows the values of the parameters selected for the driver components. As can be seen, low-value capacitances are used, while the output current ripple is kept low and within the required limits.

TABLE I
COMPONENTS OF THE PROPOSED PROTOTYPE

Component	Value
EMI Filter Inductor	*560 μH*
EMI Filter Capacitors	*2*68 nF*
Buck-boost Inductance	L_{BB} = 500 *μH* / ETD34
Boost Inductance	L_{Bo} = 250 *μH* / ETD29
Output buck-boost Capacitor C_{BB} *Kyocera FTFM4F0686*025*	68 μF, 160 V
Input Capacitor C_{Bo} *Kyocera FTA14S0155*025*	1 μF, 63 V
M_1	*SPA07N60C3*
Bridge Diodes & D_1 *&* D_{BO} *&* D_{BB}	*MUR840*

V. EXPERIMENTAL VERIFICATION

This section presents the experimental results obtained from the laboratory prototype. The line voltage and current waveforms are shown in Fig. 9. As shown in this figure, the current waveform is almost a pure sinusoidal waveform, which demonstrates that the proposed technique ensures that the PF and THD will satisfy IEC 61000-3-2 regulation. Analyzing the measured input voltage and current waveforms at full load, the PF is equal to 0.996. Concerning the THD, it is equal to 7% and the breakdown of the harmonic content is illustrated in Fig. 10. As shown in Fig. 10 the converter meets the IEC 61000-3-2 Class C limit [20].

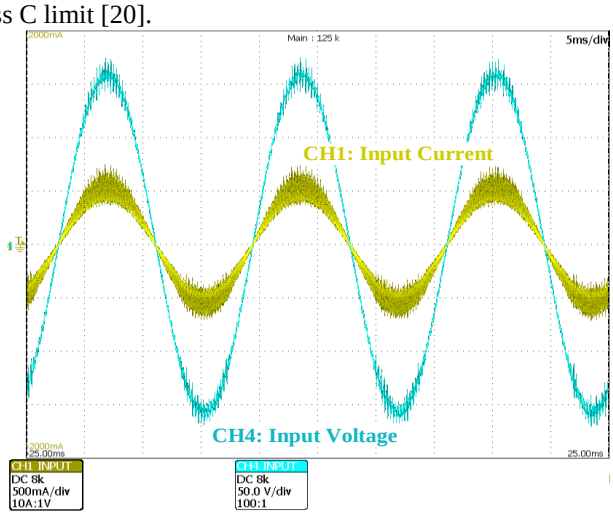


Fig. 9. AC main voltage (CH4), AC main current (CH1) at full load at RMS input voltage 110 V.

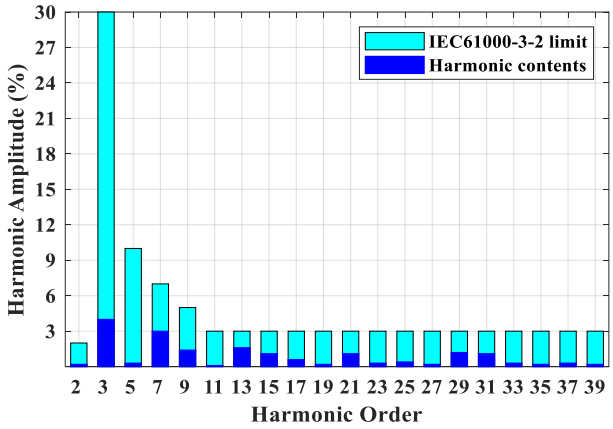


Fig. 10. Input current harmonic contents compared to IEC 61000-3-2 limit at RMS input voltage 110 V.

Fig. 11 shows the output voltage and current of the LED at full load. As shown in the figure, the ripple in the voltage is equal to 5.3 V, which is equivalent to 5 %. The current ripple is equal to 68 mA, which is 19 %. Thus, it operates below the IEEE Std. 1789-2015 recommendations. The experimental results show that the efficiency of the converter at full load is equal to 92.4 %. Thus, the driver provides the low current ripple as well as the high efficiency using relatively low capacitance for both capacitors, 1 μF and 68 μF for output and bulk capacitors, respectively.

Fig. 12 shows the three voltages of the output loop, the output buck-boost voltage (CH4), the LED voltage (CH3), and the boost input voltage (CH1). As can be seen, the LED voltage

has the lowest ripple, as the ripples are subtracted from each other. The ripple in the buck-boost output voltage is equal to 9.6 V, while the ripple of the input boost voltage is equal to 6.4 V, leading to a 4.8 V of ripple in the LED voltage approximately.

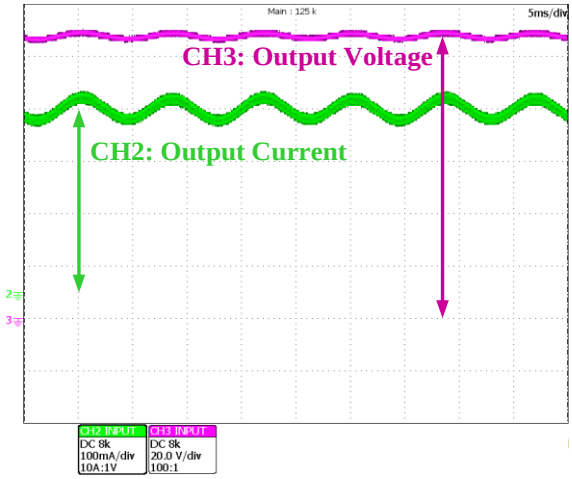


Fig. 11. LED voltage (CH3) and LED current (CH2) at full load.

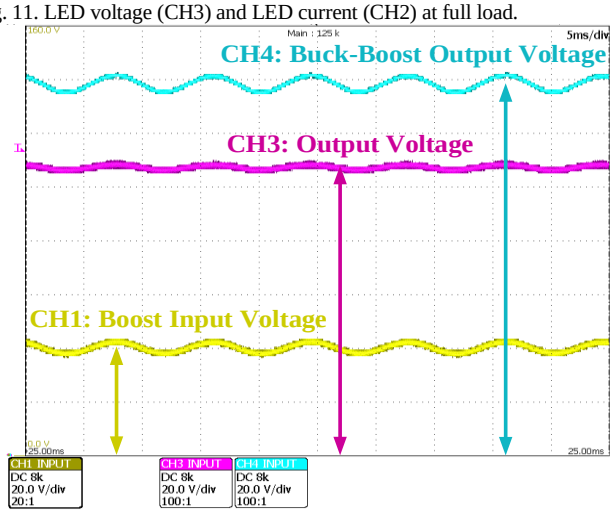


Fig. 12. Buck-boost output voltage (CH4), LED voltage (CH3) and boost input voltage (CH1) at full load.

For a better illustration of the subtraction process of the voltage ripples, Fig. 13 shows the three voltage ripples of the output loop. The figure shows the voltages without the DC component, in order to highlight only the low-frequency ripple.

Fig. 14 shows the MOSFET drain to source voltage as well as the MOSFET gate to source voltage. The upper plot shows the experimental results at low-frequency, while the lower plot shows a zoom of the upper plot to illustrate the high-frequency behavior. As illustrated in the figure, the driver is able to drive the MOSFET perfectly; it appears some resonance in the drain to source voltage, which corresponds to the idle interval of DCM operation.

In order to verify the operation of the converter, the currents in both inductors are measured. Fig. 15 shows the current of the buck-boost inductor in CH2 and the boost inductor in CH3. The top plot shows the currents in the low-frequency range (5 ms/div) and the bottom plot in the switching frequency range (20 µs/div). The currents shown in the results are perfectly matching the expected operation of the converter; moreover, the current range is within the expected values of 2.6 A for the buck-boost current and 1.25 A for the boost current.

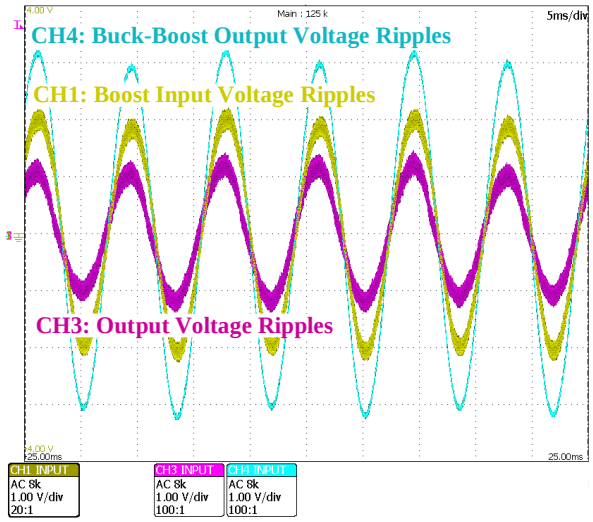


Fig. 13. Buck-boost output voltage ripple (CH4), LED voltage (CH3) and boost input voltage (CH1) at full load.

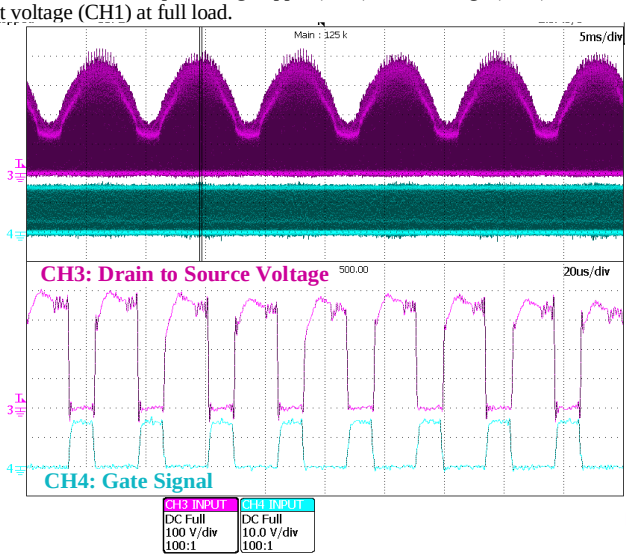


Fig. 14. Gate-to-source signal (CH4) and drain-to-source voltage across of the MOSFET (CH3).

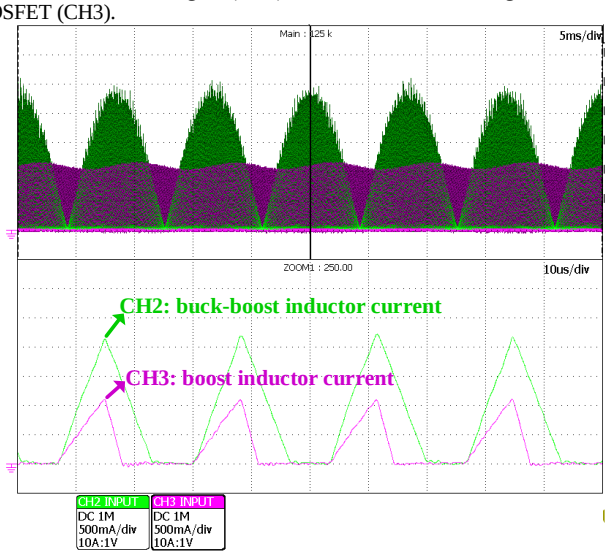


Fig. 15. Buck-boost inductor current (CH2) and the boost inductor current (CH3). The upper plot shows the waveforms in the low-frequency range (5 ms/div), and the lower plot shows the waveforms in the switching frequency range (20 µs/div).

The performance of the driver has also been tested in the universal input voltage range (90-250 V_{rms}). Fig. 16 shows the operation of the driver under input voltage 230 V. As shown in the figure, the operation principles remain the same; however, the operating point changes, which makes the efficiency drop to 88.33%, and the power factor to 0.97. As previously analyzed, the increase in the input voltage will decrease the efficiency but also the LED current ripple decreases. Fig. 16 shows the ripple of the LED current equal to 5 %, which is much lower than the value of 19 % obtained at 110 V line voltage.

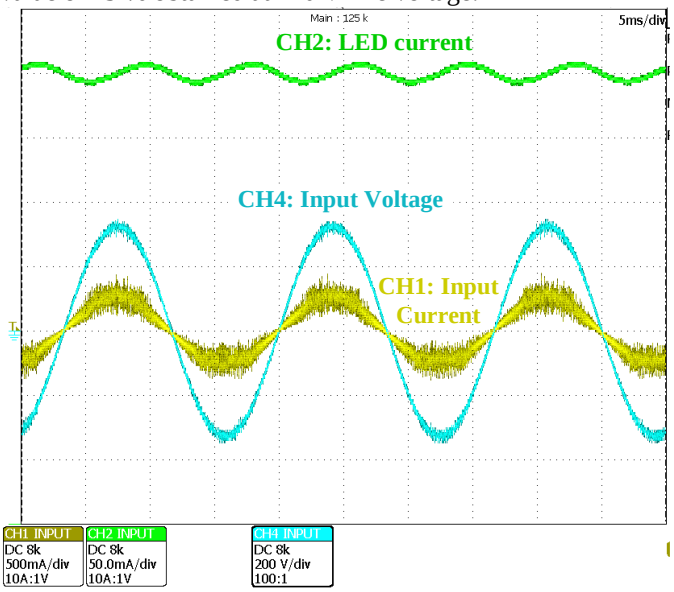


Fig. 16. AC main voltage (CH4), AC main current (CH1) and LED current (CH2) at RMS input voltage 230 V.

Fig. 17 shows the efficiency as well as the power factor with respect to the input voltage variation. The figure shows the experimental points and the fitting curve using the fitting tool of Matlab. As can be seen, the fitting curve of the efficiency is a linear function that validates the theoretical analysis previously illustrated in Fig. 8. Concerning the power factor, it drops with the increase of the input voltage showing a lower value of 0.95, which is above all limitations and standards.

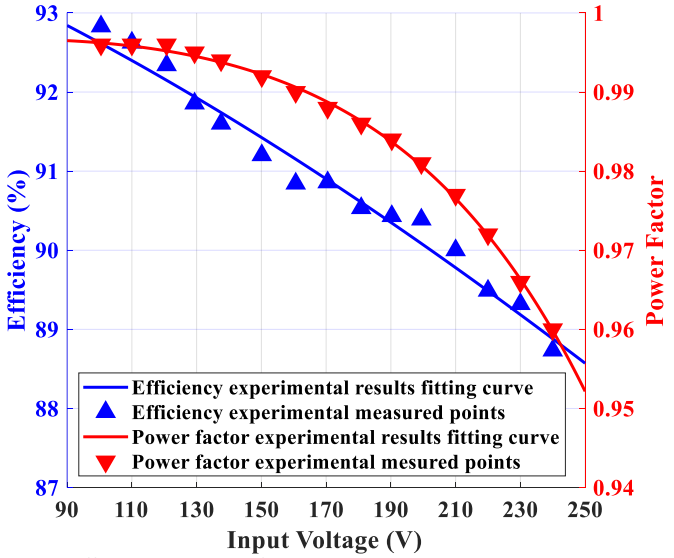


Fig. 17. Efficiency and Power factor with respect to the input voltage variation.

Fig. 18 shows the input voltage and current as well as the output voltage and current, at output power equal to 3.6 W which is approximately 10 % of the rated power. This figure shows a great advantage of the proposed converter, which corresponds to its operation at this low power with an efficiency of 74 % and input PF of 0.975. Therefore, it is proven that the converter operates correctly within the whole dimming range.

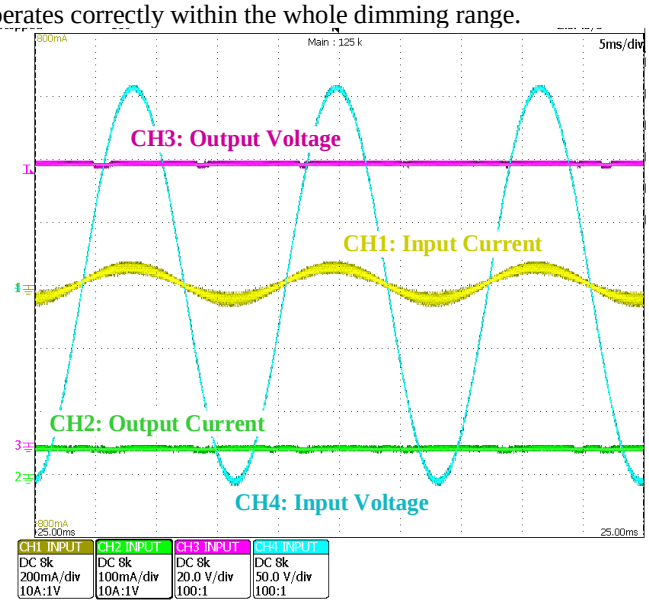


Fig. 18. AC main voltage (CH4), AC main current (CH1), LED voltage (CH3) and LED current (CH2) at 10% of rated power.

Fig. 19 shows the efficiency and the PF versus the output power, extracted from the experimental results. Analyzing the PF of the converter, it is above 0.97 in all output power range. Concerning the efficiency, it varies between 74 % at 10 % output power to 92.4 % at rated power.

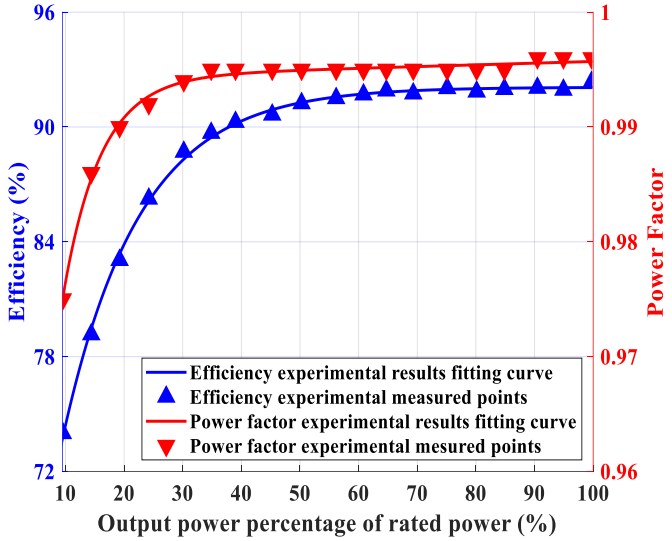


Fig. 19. Efficiency and Power factor with respect to the output power percentage of the rated power.

In order to verify the effectiveness of the proposed converter, the laboratory prototype is tested when deactivating the RR stage. Thus, a buck-boost single-stage converter is configured. Keeping the same parameters, the efficiency of the driver 94%, which is 2% higher than the parallel converter, as it should be expected by the fact that there is only one stage processing the

energy. However, the ripple is increased from 68 mA (19%) to 186 mA (53%), as shown in Fig. 20. Thus, the converter fails to meet the IEEE Std. 1789-2015 recommendations, and the output capacitance must be increased to fulfill this goal. A second experiment is repeated with the RR stage deactivated but now using a higher capacitance to meet the IEEE Std. 1789-2015 recommendations with the same ripple level as in the parallel converter, as shown in Fig. 21. It is found that a capacitance of 390 µF is needed to fulfill the IEEE recommendations, which is more than five times the required capacitance of the proposed converter. Fig. 21 shows the input and output voltages and current of the buck-boost single-stage at full load using an output capacitance of 390 µF. Using the bulk capacitor of 390 µF, the voltage ripple decreases to 5 %, and the current ripple decreases to 19%.

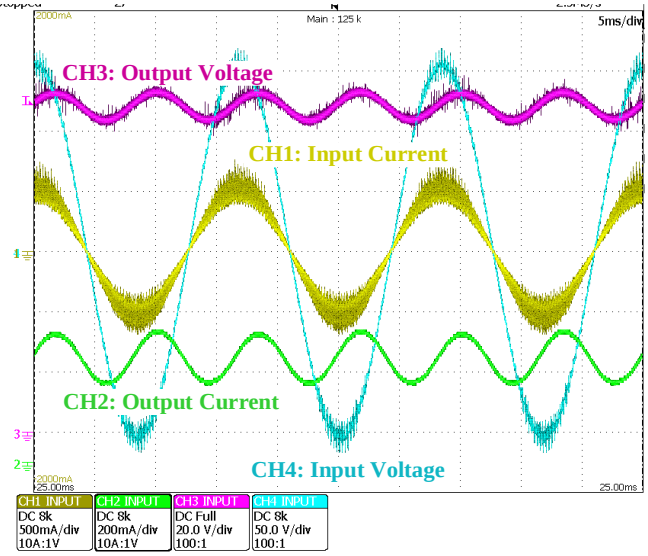


Fig. 20. AC main voltage (CH4), AC main current (CH1), LED voltage (CH3) and LED current (CH2), from the stand-alone buck-boost converter at full load, using output capacitor 68 µF.

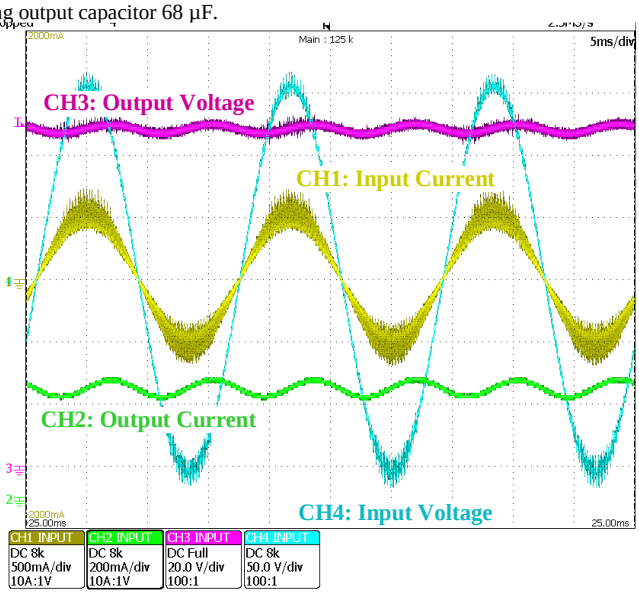


Fig. 21. AC main voltage (CH4), AC main current (CH1), LED voltage (CH3) and LED current (CH2), from the stand-alone buck-boost converter at full load, using output capacitor 390 µF.

For the sake of a better understanding of the power distribution in the converter and allocation of the losses, Table II shows the power entering and going out from each stage as well as the losses and efficiency of each stage for the converter operating at the rated power. Moreover, the final row shows the same information for the proposed topology IPB3C.

TABLE II
POWER AND EFFICIENCY OF THE CONVERTER STAGES

Stage	Efficiency	Input Power	Output Power	Losses
Buck-boost (PC stage)	*94 %*	*40.7 W*	*38.2 W*	*2.5 W*
boost (RR stage)	*96 %*	*14.1 W*	*13.5 W*	*0.6 W*
IPB3C (total)	*92.4 %*	*40.7 W*	*37.6 W*	*3.1 W*

Fig. 22 shows the laboratory prototype photograph. The prototype shows that even using film capacitors that are known for their bulky size, the driver is compact and its size is comparable to normal electrolytic capacitor conventional drivers. The driver dimensions are 80 mm by 80 mm and the height of the longest component is 40 mm.

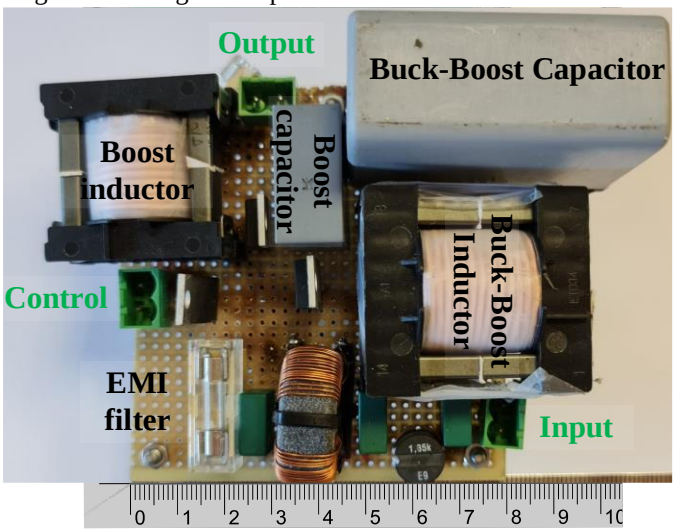


Fig. 22. Prototype photograph.

Finally, a comprehensive comparison with the parallel converters found in the literature is shown in Table III. The following converters were found: flyback operating as PFC and a bidirectional buck-boost parallel stage [37], flyback operating as PFC and a buck parallel stage [40], buck-boost operating as PFC and a buck parallel stage with power flow control switch [42], active clamp flyback PFC stage & floating capacitor full-bridge [43-44], buck-boost operating as PFC and a buck parallel stage [45], and buck-boost operating as PFC and a flyback parallel stage [47]. As shown in Table III, the proposed driver is the only driver that is using just one single controlled switch, which means that only one control circuitry and one single driver are needed. Concerning the capacitance required by the proposed driver, it is an intermediate value among all proposed electrolytic-capacitor-less LED drivers. The efficiency of the proposed driver is the highest compared to found in the literature. The only drawback is that the proposed driver does not offer electric isolation, while some other techniques do. Nevertheless, isolation is not considered a mandatory requirement in lighting applications.

TABLE III
COMPARISON AMONG THE PROPOSED CONVERTER AND THE FOUND-IN-LITERATURE INTEGRATED CONVERTER [37], [40], [42]-[45], [47]

Flyback PFC & buck/boost parallel stage [37]	**Flyback PFC & buck parallel stage [40]**	**Buck-boost PFC & buck parallel stage & power flow control [42]**	**Active clamp flyback PFC stage & floating capacitor full-bridge [43-44]**	**Buck-boost PFC & buck parallel stage [45]**	**Buck-boost PFC & flyback parallel stage [47]**	**Proposed buck-boost PFC & boost parallel stage**
3 Switches	*2 Switches*	*3 Switches*	*6 Switches*	*2 Switches*	*2 Switch*	*1 Switch*
2 inductors	*1 inductor*	*2 inductors*	*2 inductors*	*2 inductors*	*1 coupled inductor*	*2 inductors*
1 transformer	*1 transformer*	*No transformer*	*1 transformer*	*No transformer*	*1 transformer*	*No transformer*
1 diode	*3 diodes*	*3 diodes*	*1 diode*	*2 diodes*	*2 diodes*	*3 diodes*
2 capacitors 0.47 µF & 20 µF	*2 capacitors 2*10 µF & 2*5.6 µF*	*2 capacitors 3*2.2 µF & 3*2.2 µF*	*3 capacitors 0.47 µF & 4.7 µF & 12*10 µF*	*2 capacitors 67 µF & 6.8 µF*	*2 capacitors 130 µF & 20 µF*	*2 capacitors 68 µF & 1 µF*
2 Control circuitries	*2 Control circuitries*	*3 Control circuitries*	*2 Control circuitries*	*2 Control circuitries*	*2 Control circuitries*	*1 Control circuitry*
3 driver circuitries	*2 driver circuitries*	*3 driver circuitries*	*6 driver circuitries*	*2 driver circuitries*	*2 driver circuitries*	*1 driver circuitry*
Electric isolation	*Electric isolation*	*No Electric isolation*	*Electric isolation*	*No Electric isolation*	*No electric isolation.*	*No electric isolation.*
Universal operation can be achieved.	*Universal operation can be achieved.*	*Universal operation can be achieved.*	*Universal operation can be achieved*	*No Universal operation tested*	*Universal operation can be achieved.*	*Universal operation can be achieved*
Efficiency of 88 % at rated power 33.6 W	*Efficiency of 84 % at rated power 20 W*	*Efficiency of 89.69%, at rated power 16 W*	*Efficiency of 91%, at rated power 100 W*	*Efficiency of 91 %, at rated power 75 W*	*Efficiency of 85 %, at rated power 9 W*	*Efficiency of 92.4 %, at rated power 37.6 W*
Theoretical unity power factor.	*High power factor of 0.98*	*High power factor of 0.99*	*High power factor of 0.99*	*High power factor of 0.98*	*High power factor of 0.97*	*High power factor of 0.996*

VI. CONCLUSION

This paper presents a new highly efficient converter for LED driver applications, which ensures high PF and low THD to be far below the limitation specified by IEC 61000-3-2 standard. Moreover, the converter ensures a low LED current ripple using small capacitances, which can lead to an electrolytic-capacitor-less driver. This is done by parallel integrating a buck-boost converter operating as a PC stage and PFC stage simultaneously, with a boost converter operating as an RR stage. Furthermore, the proposed topology does not require any coupled inductors nor transformers, which means that a spike-less operation is ensured, and winding losses can be minimized. Additionally, the proposed technique avoids requiring any complex circuitry or any advanced sensors other than the normal ones used in dc-dc converters. Regarding the power component, the proposed topology offers all these features by using only one controlled power switch. Lastly, the parallel integration provides the ability to control the percentage of the circulating power in the RR stage, allowing for improved efficiency compared with the conventional cascade structure.

A prototype operating at 110 V, 60 Hz line input, and 108 V output, driving an LED luminaire of 38 W, has been designed to illustrate the application of the derived characteristics. The experimental results have proven that the harmonic content of the input current is low, with nearly unity PF, so that the converter meets the IEC-61000-3-2 standard and U.S. Energy Star program requirements. Concerning the efficiency of the proposed driver, it is higher than the conventional cascaded converters as it gives a 92.4 % efficiency at rated power. Moreover, the efficiency of the prototype is equal to 74 % at 3.6 W, which is relatively high efficiency at this low power. Furthermore, the prototype is operating with no electrolytic capacitor, which means a longer lifetime driver.

Comparing the obtained results with a conventional buck-boost single-stage converter, it is found that the proposed technique offers the usage of a five times smaller capacitance keeping the same operating conditions. The proposed converter offers higher power density, price reduction, and longer lifetime as it is an electrolytic-capacitor-less driver. The proposed converter requires the addition of two diodes, one capacitor of 1 µF / 63 V, and an inductor of 250 µH / ETD29.

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