Compensation Alternatives for Power Sharing Mismatch in Multi-Port DC/DC/AC Converters

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Abstract—This paper proposes several alternatives for the compensation of power sharing errors in the coupling DC bus of multi-port DC/DC/AC converters. The case of study consists in a multi-port converter used for the interconnection of an AC grid-tied converter, a battery, a supercapacitor and a regenerative DC load. A distributed control system, where the central controller computes the load power sharing between the battery and the supercapacitor modules and local controllers for the power control at each converter port is implemented. The sharing mechanism requires a precise measurement or estimation for the required load and ports power. However, due to measurements errors or control actions deviations, the real power share can differ from the estimated one and hence a power mismatch is produced. Those mismatches are absorbed by the DC-link voltage, which is assumed to be controlled by the grid-tied converter. However, considering power restrictions in the grid-tied converter, the differences in the power sharing can compromise the system operation and stability. The paper includes an analytical study for the converter operation under saturation conditions and proposes three compensation methods which are compared by simulation and experimental results. The proposed methods allow for the stable operation of the system, even when large errors in the power sharing are considered.

NOMENCLATURE

Acronyms

Batt	Batteries.
ESS	Energy storage system.
HPF	High-pass filter.
iPEBB	Intelligent Power Electronics Building Block.
LPF	Low-pass filter.
PSC	Power Sharing Compensator.
SCaps	Supercapacitors.

Subscripts

0	Initial value of a variable.

b	Battery variable.
dc	DC bus variable.
ESS	Energy storage system variable.
g	Grid variable.
L	Load variable.
sc	Supercapacitor variable.
x	Unspecified device variable.

Superscripts

$*$	Reference value (setpoint) of a variable.
$\prime$	Additional/extra value of a variable.

Variables

d	Duty cycle.
e_{dc}	DC voltage error.
f	Frequency.
i	Current.
K_i	Integral gain.
K_p	Proportional gain.
P	Power.
T_s	Sample period.
u	Voltage.
ΔP	Power mismatch.
ΔP_g	Remaining grid power.

I. INTRODUCTION

LOCAL small-scale power systems are being developed to promote the introduction of renewable energies, since they are closely related to distributed generation unlike the conventional ones. The concept of microgrid appears in order to categorize this type of systems, which are evolving over time [1]. Microgrids usually have some energy storage units to support the renewable power generation, which is non-deterministic. Different kind of energy storage systems (ESS) can be installed, some of them being more dedicated to the energy needs (batteries), while others show their advantages in terms of power capability (supercapacitors) [2], [3]. In order to exploit the advantages of the different types of energy storage system, microgrids can use an hybrid implementation (e.g. batteries and supercapacitors), so that a flexible and reliable operation is achieved [4], [5].

Batteries have relatively high energy density but they are not suitable when suffering high variations of power. This is because the internal electrochemical reactions inside the battery produce a process of degradation [6], [7]. To face this problem, supplementary supercapacitors can be used since they work properly under high variations of power [8]–[10], though they have low energy density. Therefore, it is necessary to perform a power sharing between the battery-based ESS and the supercapacitor ones [11]–[16].

However, any error in the calculation of the power sharing produces a mismatch, which may disturb the system performance. Errors in the sensors, in the estimation of the power load or in the control actions of the converters often appear during the operation of a power system. Thus, the influence of these mismatches should be analyzed to determine the resultant effects on the system under control.

The analyzed case is a multi-port DC/DC/AC converter, as a simplification of a complete hybrid DC/AC microgrid, composed of a DC load, a battery and a supercapacitor. A schematic diagram, based on the concept of distributed intelligent Power Electronics Building Blocks (iPEBBs) [17], is shown in Fig. 1. As explained in [17], an iPEBB is a single-phase power cell (upper and lower power switches, parallel capacitor, and series inductor in mid-point) with built-in voltage and current sensors, and a digital control system which manages the power cell.

The power converters outputs are coupled to a DC bus. Additionally, an inverter is connected to exchange energy with the AC grid. Since the DC bus is the central element of the system and the common coupling point of all iPEBBs, the convention used in this paper considers positive any power (either demanded by a load or given by a source) provided as an output by the DC bus.

The objective of this paper is to analyze the power mismatch problem in the multi-port DC/DC/AC converter when grid power is limited and to propose several compensation alternatives. For this purpose, control of the DC-link voltage in saturation conditions is carried out. Some references can be found in literature targeting the specific analysis of DC-link voltage control under saturation conditions for the current control [18]–[21].

The main contribution of this paper is to propose different methods to compensate this power mismatch by directly using the information given by the DC-link voltage controller. This way, power mismatch is mitigated by the compensation methods without requiring the information from any of the sensors in the loads and sources connected to the DC bus. Operation in islanding mode is considered to demonstrate the robustness of the compensation techniques. Moreover, errors in sensors and communication delays are analyzed to validate the performance of the system.

The proposed target applications are hybrid microgrids or distribution systems in which multiple paths for the power flow could exist. In those applications, the limits for the power coming from the AC grid could lead to the very extreme situation in which there are DC-side loads with a power consumption (or generation) while the AC grid is disconnected. In those cases, the DC/AC converter is useless.

Regarding the standards, IEC 60038:2009 [22] states that low-voltage (LV) systems can withstand a steady-state voltage variation of ±10% in the supply terminals. CENELEC EN 50160:2010 [23] also specifies a ±10% magnitude variation to be accomplished 95% of the time of the week for LV systems, allowing normal rapid voltage changes of 5% and infrequent rapid voltage changes of 10%. ANSI C84.1-2016 [24] shows that normal voltage fluctuations do not normally exceed ±5% of the nominal value. IEEE Std 1159-2019 [25] does not consider variations within ±10% of the nominal voltage as electromagnetic phenomena, whereas IEEE Std 1250-2018 [26] defines a voltage regulation of ±5% in normal conditions. IEEE Std 1547-2018 [27] specifies voltage ride-through requirements for distributed energy resources (DERs) connected to electric power systems (EPSs), so that continuous operation has to be guaranteed if voltage range is from 0.88 to 1.1 pu. Therefore, the boundary of working conditions is a maximum variation of ±5% in the DC nominal voltage.

IEEE Std 2030.7-2017 [28] states that microgrids are capable to operate in islanding mode and supply local loads, but also connected to the grid at the point of interconnection (POI). Thus, to limit the maximum power to be exchanged depending on grid state, a grid power limit is established. Whilst a conventional AC/DC converter would be suitable to meet the maximum DC voltage variation during normal conditions, it is prone to fail whenever grid power limit is reached. This can happen either when it is required to limit the maximum power exchanged with the grid or to operate in islanding mode due to a controlled disconnection from the grid or a blackout. Therefore, the introduction of an ESS in the DC grid with a multi-port DC/DC/AC converter provides redundancy and thus improves the reliability of the DC grid, since local loads/sources can continue to operate regardless of the state of the main grid.

In addition, applications with regenerative electric motors or any DC-side generation may be suitable for this topology to limit the exchanged grid power. This way, fast power variations will be provided by the ESS whereas the grid only manages the base power and the energy demand to maintain the ESS conveniently charged, always guaranteeing that the total grid power is below the configured limit.

It has to be remarked that the proposals in this paper do not need for the additional installation of ESS units but despite it uses the elements already available in the hybrid DC/AC grid, by implementing a collaborative control between all of them.

In addition, the use of the same power cell (iPEBB) for all power converters reduces costs and facilitates maintenance, since the hardware is common and only its programming varies depending on the application. It would also facilitate the integration of new power units with a similar nominal power without having to design a new specific power stage, providing flexibility to the system when introducing new loads/sources, a common case in distributed generation systems. In addition, several iPEBBs could be parallel combined to enable power units with higher nominal powers, providing scalability to the system.

This research is mainly based on the contributions presented in [29]. Past work is extended by a meaningful theoretical
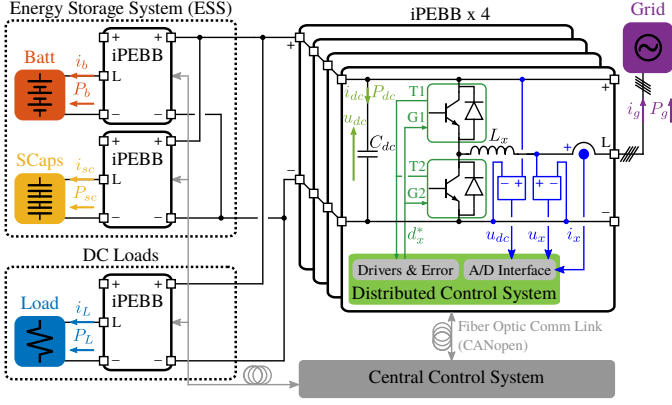
Fig. 1. Electrical diagram of the multi-port DC/DC/AC converter based on the use of intelligent Power Electronics Building Blocks (iPEBBs).
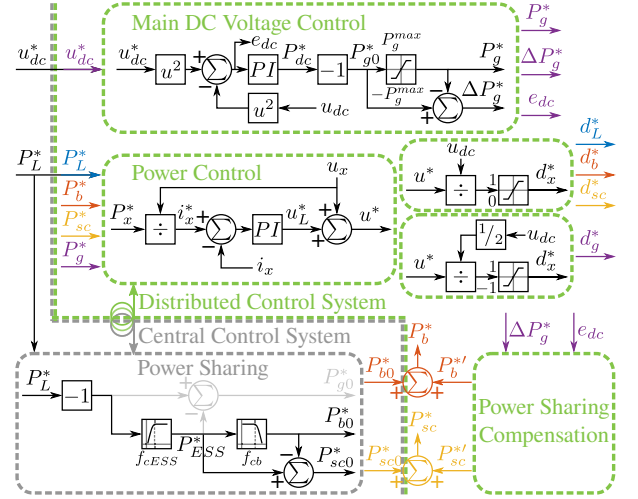

Fig. 2. Control diagram of the multi-port DC/DC/AC converter. Gray units are integrated in the central control system whereas green units are integrated in the distributed control units.

analysis of the system performance and compensation methods under saturation conditions derived from power limitations. New simulation and experimental results have been developed to consider islanding operation, thus demonstrating the robustness of the proposed control system under sudden AC grid disconnection. In addition, an analysis of the effect of power measurement (sensor) errors and communication delays in the performance of the compensation methods is performed.

This paper is organized as follows. In Section II, an explanation of the power sharing hurdles in the multi-port DC/DC/AC converter is introduced. In Section III, an analysis of the different compensation techniques for tackling the power sharing mismatch is discussed. In Section IV and Section V, simulation and experimental results are obtained for the control system validation. Finally, in Section VI, conclusions about the accomplished work are discussed.

II. POWER SHARING ISSUES

The multi-port DC/DC/AC converter used in this work is made up of several power units interconnected through a dc-link capacitor. The considered units are an aggregated regenerative DC load, which represents the different loads connected to the DC grid; a Li-ion battery; a supercapacitor, and a grid-tied interlinking converter connected to the AC grid (Fig. 1). In order to supply the DC load, a power sharing between the different power converters is employed. Considering as the starting point an operational AC grid, the base load demand is provided by the AC connection, whereas the peak load demand is given by the ESS. Between the two available sources, the low frequency components are supplied by the battery (energy source) whereas the high frequency components are supplied by the supercapacitor (power source). By using two low-pass/high-pass filters with different cutoff frequencies, it is possible to tweak the power sharing as desired.

Fig. 2 shows the proposed control diagram to carry out the power sharing mechanism. The power sharing is computed by the central controller, which sends the power references (P_{x0}^*) to the power control of the different distributed control units, in order to manage the current/power of the different system power converters. This control system implementation requires to have an accurate measurement of the power by

each of the converter units. However, sensor accuracy or saturation phenomena in the control action of any unit will induce differences in the real power sharing.

Focusing on the DC side of the multi-port converter (Fig. 1), the power balance expression which links the different power units (load: P_L, battery: P_b, supercapacitor: P_{sc}, grid: P_g and DC bus capacitor: P_{dc}) is given by (1).

$$P_L + P_b + P_{sc} + P_g + P_{dc} = 0 \qquad (1)$$

As it can be seen in Fig. 2, the power in the DC bus capacitor is not directly controlled, being dependent on the power mismatch (ΔP) among the different controlled power units. From (1), it is possible to obtain the magnitude of the DC bus capacitor power as given by (2).

$$P_{dc} = -\Delta P = -(P_L + P_b + P_{sc} + P_g) \qquad (2)$$

For this purpose, it is necessary to calculate the power handled by the different units of the system using the expressions (3)-(6).

$$P_L = u_L i_L \qquad (3)$$
$$P_b = u_b i_b \qquad (4)$$
$$P_{sc} = u_{sc} i_{sc} \qquad (5)$$
$$P_g = u_{ga} i_{ga} + u_{gb} i_{gb} + u_{gc} i_{gc} \qquad (6)$$

Therefore, if the power sharing is perfectly done, the power mismatch is zero and the DC grid is balanced. Whenever a power mismatch occurs, (2) is not longer equal to zero and the power surplus or shortage has to be delivered/absorbed by the DC bus capacitor in order to compensate for that difference, acting as a power buffer. The problem is that this variation of DC bus capacitor power because of the power mismatches produces variations in the DC-link voltage. These DC-link voltage deviations are undesirable and thus have to be kept under certain bounds in order to avoid the system to reach unstable conditions. The absolute minimum limit for the DC-link voltage is twice the peak value of the grid phase
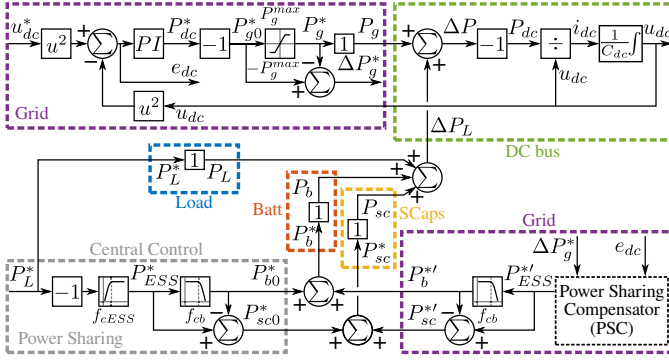
Fig. 3. Model of the multi-port DC/DC/AC converter with Power Sharing Compensator (PSC) from the point of view of the grid-side DC voltage control (ideal power control loops shown as unitary gain).

Fig. 4. Power sharing issues when the grid power is limited (± 1 pu). a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Current comsumption. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus. Dashed lines: grid power limits.

voltage, since it is the minimum value needed to maintain the controllability of the system in inverter mode. The absolute maximum limit is determined by the maximum operating voltage of the power devices to not deteriorate them. In order to avoid the operation close to the absolute limits, a 5% margin is introduced in the actual limits.

As shown in Fig. 2, the grid-tied DC/AC inverter controls the DC-link voltage, so its variation will depend on the stiffness of its control system. Additionally, the variations induced in the DC-link voltage because of the power mismatch are also affected by the maximum power that can be managed by the grid-tied DC/AC converter ($\pm P_g^{max}$). Operation under saturation conditions in the delivered/absorbed power has still to guarantee an stable and stiff DC-link voltage.

Note that the addition of new unpredictable energy loads or sources would affect the power sharing of the system. Power produced/consumed by new sources/loads shall be estimated to be considered by the central controller algorithm to generate a modified ESS power reference. Nevertheless, if new load/source power could not be properly estimated due to its unpredictability, DC voltage control would provide the corresponding power mismatch.

Assuming that the power control of all the power units is accurate and much faster than the DC-link voltage control, the power control loops are considered ideal (unitary gain) from the point of view of the DC-link voltage control. This way, the system behavior can be modeled with the diagram shown in Fig. 3. There is a limitation in the minimum/maximum grid power, which is represented by a saturation block. If this limitation is reached, the applied grid power into the system ($P_g = P_g^*$) cannot match anymore the required power by the controller (P_{g0}^*). This way, the DC-link voltage control enters in saturation and loses the ability to properly maintain the DC-link voltage.

The aforementioned problems are following illustrated. Fig. 4 shows the power sharing issues which appear when the grid power is limited, so that saturation in the grid DC-link voltage controller is produced. In normal conditions, the grid provides the base load demand, whereas short-term power variations are provided by the ESS and the DC bus, trying to keep grid power dynamics as slow as possible to not disturb the grid. Since the DC-link voltage is controlled
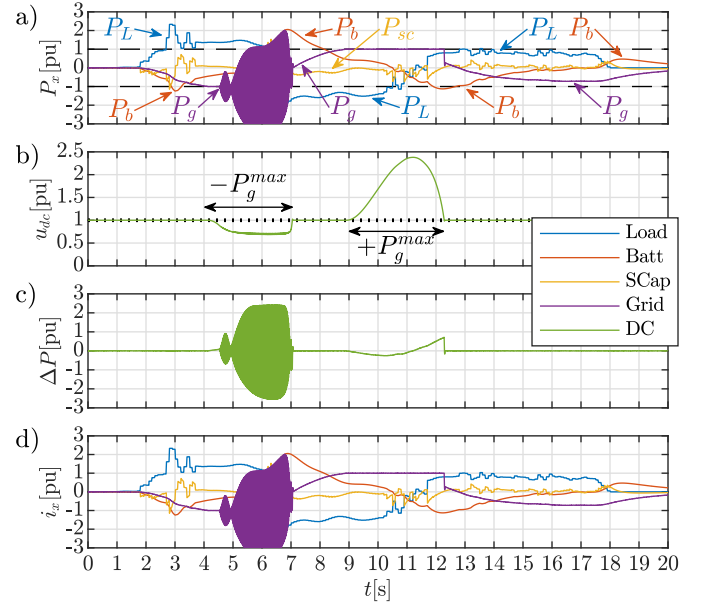
by the grid converter, power mismatches are also supplied by the grid-side converter. When the grid power reaches the minimum/maximum limit, the DC-link voltage either drops to the rectifier level or rises to fault values.

Constant power loads are commonly used to validate the robustness of voltage control algorithms, since they put the system in a worst-case scenario. For the evaluation of the system dynamics, a bidirectional electronic load able to generate rich time-varying profiles, either as a constant power or constant current load is used. The underpinning idea is to emulate the behaviour of high performance electrical drives.

At 4.1 s, the DC-link voltage starts dropping because of grid power reaching the minimum limit and thus the DC-link voltage control is saturated. At 4.5 s, the DC-link voltage reaches 400 V (0.8889 pu), which is twice the peak value of the grid phase voltage (200 V) and the minimum value that guarantees a stable system operation. Operation under that limit causes system instability when the DC/AC converter work in inverter mode delivering power to the grid, hence the shown oscillating behavior of the grid power. At 7 s, the DC-link voltage raises above the minimum limit, resulting in the system to be stabilized. From 9 s to 12 s, the DC-link voltage starts increasing because the grid power reaching the maximum limit and the DC-link voltage control being also saturated. In this event, the DC-link voltage reaches values greater than twice the nominal value (2.38 pu), which can deteriorate the power devices. This way, the system operation is compromised and correction actions are required to take back DC-link voltage within safe values.

In order to solve this problem, it is necessary to dynamically correct power mismatches to ensure a suitable operation. Considering that power mismatches are normally a transient problem, often with fast dynamics, this paper proposes several

alternative compensation methods relaying on a modified operation of the ESS.

A new control module called Power Sharing Compensator (PSC) is introduced into the control diagram (Fig. 2 and Fig. 3) with a view to performing the power sharing compensation. Extra power references ($P_x^{*\prime}$) are computed by this module and commanded together with the initial power references (P_{x0}^*) to the power control loops. Since it is required to compensate the power mismatches rapidly, the power sharing compensation is internally performed by each distributed control unit.

III. COMPENSATION TECHNIQUES

As mentioned above, power mismatches in the power sharing produce a deviation of the DC-link voltage from the nominal value. Thus, some kind of correction has to be applied to mitigate the problem. Three different compensation techniques are proposed: 1) direct power reference compensation, 2) auxiliary DC voltage control and 3) enhanced power reference compensation.

The challenge in the compensation is to properly estimate the power mismatch. Ideally, it could be determined by measuring the power in all system units and computing the summation, as shown in (2)-(6). However, this requires good accuracy in all current/voltage sensors of the system and does not allow the addition of new power units that do not provide any feedback of the power consumption.

Alternatively, an estimation method for the compensation power can be done by analyzing the shape of the grid DC-link voltage controller. The grid-side DC voltage control is controlled by the grid-tied converter using a quadratic voltage control (QVC) [30] as shown in Fig. 2 and Fig. 3, so that the control action is expressed in terms of power. If saturation in the grid-tied converter is produced, the controller will not longer be able to apply the required power. The remaining grid power (ΔP_g^*) can be considered as the required extra power to counteract the power mismatch. This way, good accuracy is only required in the current/voltage sensors of the grid power units to compute the power mismatch, reducing the number of elements that can introduce errors in its calculation.

In order to determine the options to compensate this power mismatch, the control law of the discrete QVC based on a PI controller is discussed. Observing the system model (Fig. 3) and for a given proportional gain (K_p), integral gain (K_i) and sample period (T_s), the expression (ideal form) to calculate the control action (u) of the controller depending on the error (e) at any sample k is given by (7)-(9).

$$e_k = e_{dc} = (u_{dc}^*)^2 - (u_{dc})^2 \tag{7}$$

$$u_k = u_k^0 = \underbrace{K_p e_k}_{\text{P action}} + \underbrace{K_p(K_i T_s - 1)e_{k-1} + u_{k-1}}_{\text{Integral action}} = P_{dc}^* \tag{8}$$

$$P_{g0}^* = -P_{dc}^* = -u_k; \; P_g^* = \text{sat}(P_{g0}^*); \; \Delta P_g^* = P_{g0}^* - P_g^* \tag{9}$$

Since the implemented controller provides integral action, an anti-windup mechanism that limits this action during saturation is required. In this case, the realizable references method is used due to its performance and simplicity in discrete systems [31] when the controller has the same number of poles than zeros. Considering a discrete PI controller implemented
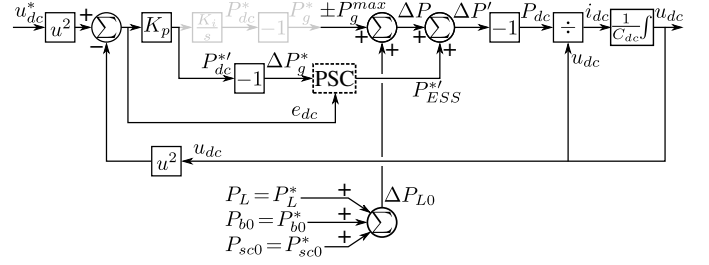

Fig. 5. Simplified model under saturation conditions of the multi-port DC/DC/AC converter with DC-link voltage control carried out by the grid and the Power Sharing Compensator (PSC).

by the bilinear approximation, the calculations performed by the anti-windup method during saturation conditions to correct the actual control action (u_k) and error (e_k) with realizable values (u_k^r, e_k^r) for the next iteration (u_{k+1}, e_{k+1}) are given by (10) and (11) respectively.

$$u_k^r = -P_g^* = -\text{sat}(-u_k); \; u_{k+1} = u_k^r \tag{10}$$

$$e_k^r = \frac{u_k^r - K_p(K_i T_s - 1)e_{k-1} - u_{k-1}}{K_p}; \; e_{k+1} = e_k^r \tag{11}$$

This way, when the DC-link voltage reaches steady state ($u_{dc} \approx u_{dc}^*$, $e_k \approx 0$, $e_{k-1} \approx 0$), the controller only applies the integral action. Once the system enters into saturation, the grid converter power is limited and the anti-windup mechanism starts actuating by limiting the integral action. If saturation is kept at least during two samples periods, both the previous (u_{k-1}) and the realizable action control (u_k^r) take the limited minimum/maximum value. This way, (11) can be simplified into the expression given by (12).

$$e_k^r = (1 - K_i T_s)e_{k-1}; \; e_{k+1} = e_k^r \tag{12}$$

Assuming that $|1 - K_i T_s| < 1$, the realizable error (e_k^r) and hence the previous error (e_{k-1}) will converge to zero. In this case, from (7)-(10), it is possible to obtain the expression which defines the remaining grid power, as shown in (13) and (14).

$$\Delta P_g^* = -\left(u_k^0 - u_k^r\right) = -\left(u_k^0 - u_{k-1}\right) \tag{13}$$

$$\Delta P_g^* = -K_p e_{dc} = -K_p\left((u_{dc}^*(t))^2 - (u_{dc}(t))^2\right) \tag{14}$$

Therefore, the applied grid power by the converter (P_g^*) will be dominated by the limited integral action ($\pm P_g^{max}$) whereas the remaining grid power (ΔP_g^*) will be dominated by the proportional action which is not provided by the converter due to saturation. Taking all of this into account, the model in Fig. 3 can be simplified under saturation conditions, so that the model shown in Fig. 5 is obtained.

Since the applied grid power is limited during saturation, the power mismatch (ΔP) is no longer zero and a disturbance of the DC-link voltage is produced. Extra power has to be introduced into the system in order to minimize the mismatch, obtaining a corrected power mismatch ($\Delta P'$) as close as possible to zero and hence reducing the DC-link voltage deviation.

Analyzing the simplified model for saturation (Fig. 5), a expression which relates the different variables of the system,
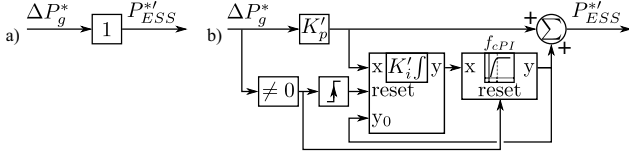
Fig. 6. Model of Power Sharing Compensator (PSC): direct (a) and enhanced (b) power reference compensation.

Fig. 7. Model of Power Sharing Compensator (PSC): auxiliary DC voltage control.

including the Power Sharing Compensator (PSC), in the forward path is calculated, as given by (15).

$$\Delta P(t) + \underbrace{PSC \cdot \Delta P_g^*(t)}_{P_{ESS}^{*\prime}} + C_{dc} \cdot u_{dc}(t)\frac{\mathrm{d}u_{dc}(t)}{\mathrm{d}t} = 0 \quad (15)$$

If (14) and (15) are combined and then linearized for the equilibrium point (U_{dc0}, U_{dc0}^*, $\Delta P_g^* = 0$, $\Delta P = 0$) by using Taylor series [30], the expressions in (16) and (17) are obtained.

$$\left(s\frac{C_{dc}}{2K_p} + PSC\right)\Delta P_g^*(s)$$
$$+ (sC_{dc})U_{dc0}^*\Delta u_{dc}^*(s) = -\Delta P(s) \quad (16)$$

$$(sC_{dc} + 2K_p PSC)U_{dc0}\Delta u_{dc}(s)$$
$$- (2K_p PSC)U_{dc0}^*\Delta u_{dc}^*(s) = -\Delta P(s) \quad (17)$$

Assuming that the DC-link voltage reference does not vary ($\Delta u_{dc}^* = 0$, fixed DC-link voltage), it is possible to obtain from (16) and (17) the transfer functions which define the model of the system, as given by (18)-(20).

$$\frac{\Delta P_g^*(s)}{\Delta P(s)} = \frac{-2K_p}{sC_{dc} + 2K_p PSC} \quad (18)$$

$$\frac{\Delta u_{dc}(s)}{\Delta P(s)} = \frac{-1/U_{dc0}}{sC_{dc} + 2K_p PSC} \quad (19)$$

$$\frac{\Delta u_{dc}(s)}{\Delta P_g^*(s)} = \frac{1}{2K_p U_{dc0}} \quad (20)$$

As it can be seen, the evolution of both the remaining grid power (ΔP_g^*) and the DC-link voltage deviation (Δu_{dc}) depends on the structure of the PSC, whereas the ratio between both variables is constant regardless of the PSC. Therefore, the PSC is able to mitigate them, so different alternatives for the PSC will be discussed below in order to analyze their performance.

A. Direct power reference compensation

The first compensation technique consists of tracking the remaining grid power ($\Delta P_g^* = -K_p\left(u_{dc}^*(t)^2 - u_{dc}(t)^2\right)$) and delivering an extra power with the same value, as shown in Fig. 6a. In this case, the PSC is simply a unitary gain.

This extra power will be provided by the ESS ($P_{ESS}^{*\prime}$) since the grid-tied converter is working under saturation conditions, as shown in Fig. 5. A low-pass filter is used to determine the battery and supercapacitor references ($P_b^{*\prime}$ and $P_{sc}^{*\prime}$).

The performance of the direct power reference compensation can be determined by computing (18) and (19) for the

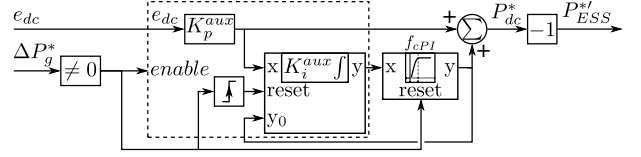particular case of $PSC = 1$, obtaining the transfer functions shown in (21).

$$\frac{\Delta P_g^*(s)}{\Delta P(s)} = \frac{-2K_p}{sC_{dc} + 2K_p}; \; \frac{\Delta u_{dc}(s)}{\Delta P(s)} = \frac{-1/U_{dc0}}{sC_{dc} + 2K_p} \quad (21)$$

The resultant transfer functions correspond to first order systems and hence there is not overshoot in the evolution of the remaining grid power and the DC-link voltage. Then, the maximum deviation of both variables (ΔP_g^{*max}, Δu_{dc}^{max}) can be obtained with the maximum power mismatch ($|\Delta P^{max}|$) via the DC gain ($\lim_{s\to 0}$) of the transfer functions in (21), whose expressions are given by (22).

$$\Delta P_g^{*max} = |\Delta P^{max}|; \; \Delta u_{dc}^{max} = \frac{|\Delta P^{max}|}{2K_p U_{dc0}} \quad (22)$$

As it can be seen, the variations of both the remaining grid power and the DC-link voltage are not fully mitigated in the direct power reference compensation, so the power mismatch (ΔP) is not totally compensated. Following, alternative compensation techniques are discussed in order to improve the PSC performance.

B. Auxiliary DC voltage control

The second compensation technique consists on an auxiliary DC voltage control in the ESS to support the grid-side DC voltage control during saturation events. The proposed scheme is shown in Fig. 7. Under normal conditions, only the grid-side DC voltage control has to be active. Therefore, an enabling strategy which triggers the auxiliary DC voltage control needs to be considered. The enabling strategy is similar to the one applied for the direct power reference compensation. The power mismatch resulting from the saturation condition in the grid-side DC voltage control provokes a non-zero remaining grid power ($\Delta P_g^* \neq 0$), which is used as the trigger event.

Same sharing method than the one in Subsection III-A is used for the computation of the extra reference of the battery ($P_b^{*\prime}$) and the supercapacitor ($P_{sc}^{*\prime}$).

Two different controller implementations will be studied for this compensation technique: P and PI controller. If zero steady-state errors are not required in the voltage value during the saturation event, a P controller is valid.

Unlike the direct power reference compensation, the input of the auxiliary DC voltage control is the error (e_{dc}) instead of the remaining grid power (ΔP_g^*). Thus, this compensation technique is not affected by the proportional gain of the grid-side DC voltage control (K_p). The corresponding PSC transfer function has to be computed in order to compare its performance with the previous method. Considering the transfer function of a PI controller in ideal form ($C(s) =$

$K_p^{aux} + K_p^{aux} K_i^{aux}/s)$, the equivalent PSC is given by (23) and the corresponding transfer functions by (24) and (25).

$$PSC^{aux} = \frac{1}{K_p} \left(K_p^{aux} + \frac{K_p^{aux} K_i^{aux}}{s} \right) \tag{23}$$

$$\frac{\Delta P_g^*(s)}{\Delta P(s)} = \frac{-s2K_p}{s^2 C_{dc} + s2K_p^{aux} + 2K_p^{aux} K_i^{aux}} \tag{24}$$

$$\frac{\Delta u_{dc}(s)}{\Delta P(s)} = \frac{-s/U_{dc0}}{s^2 C_{dc} + s2K_p^{aux} + 2K_p^{aux} K_i^{aux}} \tag{25}$$

In the particular case of a pure proportional controller ($K_i^{aux} = 0$), it is possible to calculate from (25) the optimal auxiliary proportional gain (K_p^{auxP}) depending on the desired maximum voltage deviation (Δu_{dc}^{max}) and the maximum power mismatch ($|\Delta P^{max}|$), with the expression given by (26).

$$K_p^{auxP} = \frac{|\Delta P^{max}|}{2U_{dc0}\Delta u_{dc}^{max}} \tag{26}$$

When a PI controller is used instead, the gains are selected to mimic the behavior of the grid-side DC voltage controller. Therefore, both the auxiliary proportional gain (K_p^{auxPI}) and the auxiliary integral gain (K_i^{auxPI}) are made equal to the original proportional and integral gains (K_p, K_i), as stated by (27).

$$K_p^{auxPI} = K_p; \; K_i^{auxPI} = K_i \tag{27}$$

Additionally, since the auxiliary DC voltage control is only required to work during saturation events, the effect of the integral action after the transient recovering has to be removed. This way, steady-state contribution of the battery power ($P_b^{*\prime}$) is avoided, thus improving its life usage. For that, a resettable high-pass filter (HPF) is placed in the output of the integrator, as shown in Fig. 7. This way, the HPF avoids steady-state contribution of the ESS in normal conditions, but it is bypassed (forced activation of reset) during the saturation condition in the DC voltage control ($\Delta P_g^* \neq 0$). In addition, it has to be remarked that, in order to avoid inconsistency between the value applied to the ESS by the HPF and the dictated integrator output value whenever saturation appears, it is necessary to modify the integrator state to be initialized with the HPF output value each time the saturation condition is reached.

C. Enhanced power reference compensation

As shown in the expressions given by (21) and (22), an increment in the proportional gain induces a reduction in the voltage deviation. Therefore, it is possible to implement an enhanced power reference compensation by managing the remaining grid power (ΔP_g^*) through an extra proportional gain (K_p'), which amplifies the effect of the original proportional gain of the grid-side DC voltage control (K_p). An extra integral action (K_i') can also be added to completely eliminate the voltage deviation in steady state. According to that, an enhanced power reference compensation is proposed, as shown in Fig. 6b. As it can be seen in Fig. 6b, same sharing method than the one in Subsection III-A is used for the computation of the extra battery and supercapacitor references.

From (18) and (19), making a similar analysis to the one in Subsection III-B with $PSC = K_p' + K_p' K_i'/s$, it is possible to obtain the transfer functions in (28) and (29), and the optimal extra proportional gain for a P controller ($K_p'^P$) and the extra proportional ($K_p'^{PI}$) and integral ($K_i'^{PI}$) gain for a PI controller in (30).

$$\frac{\Delta P_g^*(s)}{\Delta P(s)} = \frac{-s2K_p}{s^2 C_{dc} + s2K_p K_p' + 2K_p K_p' K_i'} \tag{28}$$

$$\frac{\Delta u_{dc}(s)}{\Delta P(s)} = \frac{-s/U_{dc0}}{s^2 C_{dc} + s2K_p K_p' + 2K_p K_p' K_i'} \tag{29}$$

$$K_p'^P = \frac{|\Delta P^{max}|}{2K_p U_{dc0}\Delta u_{dc}^{max}}; \; K_p'^{PI} = 1; \; K_i'^{PI} = K_i \tag{30}$$

Also as stated in Subsection III-B, an additional high-pass filter can be put in the output of the controller, as shown in Fig. 6b, for avoiding any steady-state contribution of the PSC when system recovers from saturation.

D. Operation in islanding mode

All the analysis carried out so far in this section assumes an operating point in which the minimum/maximum grid power is varied with slower dynamics compared to the internal converter control, which is the case for normal system operation. However, in the event of grid disconnection, the system has to immediately enter in islanding mode. For that, the grid power limit (P_g^{max}) has to be reduced to 0. Fig. 3 shows that this will suddenly force zero grid power reference (P_g^*), creating a power mismatch (ΔP) that has to be dealt by the different compensation techniques.

Direct and enhanced power reference compensation control the remaining grid power (ΔP_g^*), while auxiliary DC voltage control manages the voltage error (e_{dc}). By looking at Fig. 3, the effect of a sudden reduction in the grid power (P_g^*) on the control variables can be determined.

In the case of using the remaining grid power (ΔP_g^*), a sudden reduction in the grid power limit would have a direct effect on it, as shown in the expression given by (31).

$$\Delta P_g^*(t) = P_{g0}^*(t) - P_g^*(t) \tag{31}$$

In the case of the voltage error (e_{dc}), the reaction is indirectly coupled through the DC-link voltage dynamics. This is shown in (32).

$$\Delta P(t) + C_{dc}u_{dc}(t)\frac{\mathrm{d}u_{dc}(t)}{\mathrm{d}t} = 0; \; e_{dc} = u_{dc}^{*2}(t) - u_{dc}^2(t) \tag{32}$$

Therefore, auxiliary DC voltage control has a certain delay in acting in the event of a sudden reduction in the grid power limit when entering islanding mode, whereas direct and enhanced power reference compensations react immediately.

E. Summary

Comparing the expressions which define the behavior of the different compensation techniques, (24), (25), (28) and (29), an equivalent behavior can be observed between the auxiliary DC voltage control and the enhanced power reference compensation. Nevertheless, controller gain selection is a

little more straightforward in the enhanced power reference compensation since it does not depend on the proportional gain of the main DC voltage controller (K_p), as shown in (26), (27) and (30). In any case, either of the two methods could be used indistinctly in a first approximation.

However, as discussed in Subsection III-D, since the control variable is not the same for both compensation techniques (voltage error e_{dc} vs remaining grid power ΔP_g^*), auxiliary DC voltage control would respond more slowly to the islanding mode condition. Due to this, the preferred compensation technique is the enhanced power reference compensation. This statement will be validated via simulations to certify the better performance of the enhanced power reference compensation during islanding operation.

Regarding the choice of a purely proportional controller or a PI controller, the latter allows to eliminate any voltage deviation in steady state. However, the implementation of the PI controller adds additional complexity to the system, since it requires a resettable integrator and high-pass filter, whereas only a simple gain is needed for the P controller. In the P controller options, the memory footprint is 2 floating variables (8 bytes) whereas the number of operations is 1 read, 1 multiplication and 1 write. Considering the PI controller alternatives, the memory footprint is 11 floating and 2 boolean variables (46 bytes) whereas the number of operations is 15 reads, 5 multiplications, 4 sums, 2 boolean comparisons and 10 writes.

Note that the power mismatch compensation is an extra addition to an already functional control in the iPEBB, which consists of power and DC voltage control loops in the case of the grid-side power branches, with all the communication protocol also integrated. Thus, since the digital signal processor of the iPEBB is optimized to reduce costs, both options (with P and PI controllers) are offered for cases where the digital processor is close to its limits. Both P and PI controllers will be tested during the simulations and experimental tests to determine their performance.

IV. SIMULATION RESULTS

Several simulations for the validation of the proposed compensation techniques are carried out in MATLAB/Simulink with the parameters described in Table I. A specific load power profile lasting 20 s has been selected to test saturation in the grid-side converter.

A. Ideal case

Results when neither grid power restriction nor compensation are shown in Fig. 8. Due to the limited bandwidth of the grid-side DC voltage control, some small DC voltage deviations are produced during the transients. Still, the system operation is nearly ideal. However, when the grid power exceeds the maximum power, the problem shown in Section II will arise. In the following discussion, grid power limits are set to ± 1 pu for comparison of the proposed compensation mechanisms. Moreover, the grid power limits are forced to ± 0 pu between 12 s and 15 s so compensation techniques under islanding can also be tested.

TABLE I
SYSTEM PARAMETERS.

| Parameter	Value
Filter inductor inductance (L)	1.7 mH
Filter inductor resistance (R)	0.33 Ω
DC-link total capacitance (C_{dc})	750 μF
Nominal grid power (base power value)	1 kW
Nominal DC-link voltage (DC base voltage value)	450 V
Nominal grid line RMS voltage	245 V
Nominal grid frequency	50 Hz
Nominal load voltage	48 V
Nominal battery voltage	144 V
Nominal supercapacitor voltage	48 V
Current control loop bandwidth	300 Hz
Grid-side DC voltage control bandwidth	20 Hz
Grid-side DC voltage control proportional gain (K_p)	0.06664
Grid-side DC voltage control integral gain (K_i)	88.86
ESS HPF cutoff frequency (f_{cESS})	0.1 Hz
Battery LPF cutoff frequency (f_{cb})	0.5 Hz
Compensation PI HPF cutoff frequency (f_{cPI})	1 Hz
Central control system frequency	100 Hz
Distributed control system frequency	10 kHz
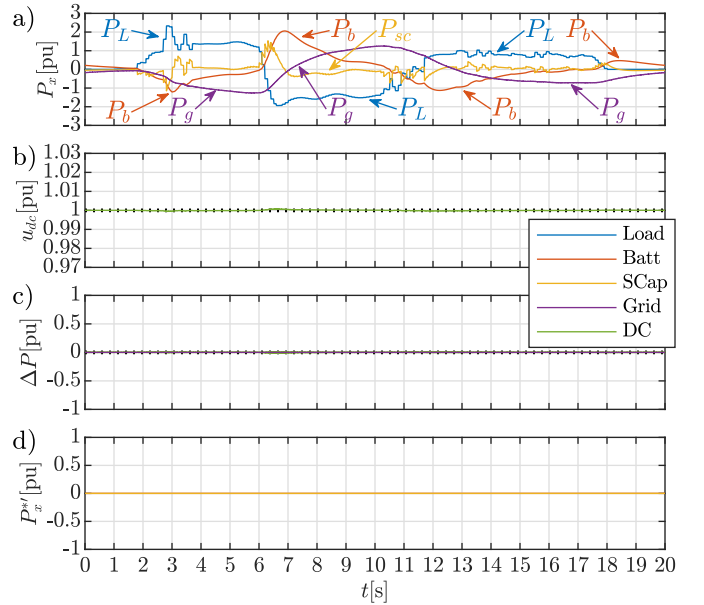
Fig. 8. Simulation results: Ideal case. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus. Dashed lines: grid power limits. Dotted lines: theoretical model evolution.

B. Direct power reference compensation

Second simulation considers the direct power reference compensation presented in Subsection III-A. Results are shown in Fig. 9. As it can be seen, the maximum grid power is accomplished so saturation conditions are considered. The DC-link voltage (u_{dc}) has a similar evolution than in the ideal case, except when saturation is produced. During these events, the power mismatch (ΔP) is not zero (Fig. 9c), so the remaining grid power (ΔP_g^*) takes a non-zero value and a DC-link voltage deviation is produced. For the compensation, the PSC generates an extra power reference for the ESS (Fig. 9d), which is shared between the battery and the supercapacitor. Thus, when comparing with the results shown in Fig. 4, the
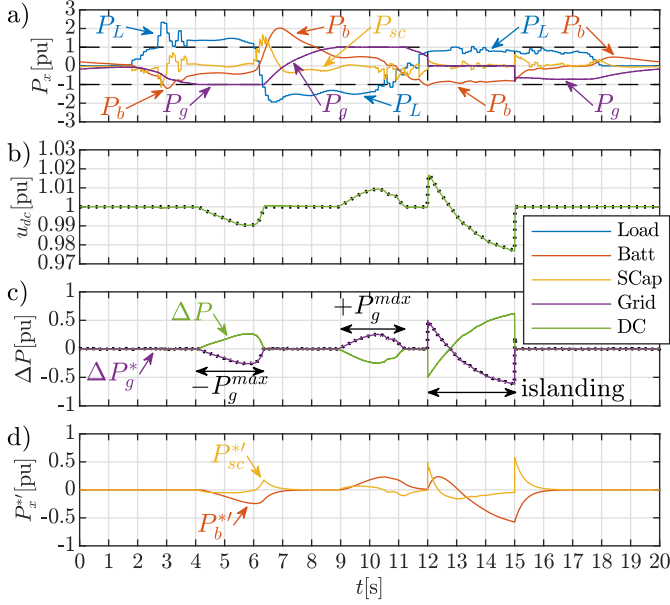
Fig. 9. Simulation results: Direct power reference compensation. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus. Dashed lines: grid power limits. Dotted lines: theoretical model evolution.

improved response is clearly visible.

Although the system continues operating within limits, there is a variation of about ± 0.02 pu in the DC-link voltage. As predicted by (22), this compensation method cannot totally compensate for the power mismatch. When the system enters in islanding, an expected larger variation can be easily seen.

C. Auxiliary DC voltage control

Third simulation is performed according to the discussion in Subsection III-B by enabling the auxiliary DC voltage control with a proportional controller. The proportional gain of the auxiliary DC voltage control is set to twice the one of the grid-side DC voltage control. Results are shown in Fig. 10. In this case, voltage variations during saturation are improved compared to the direct power reference compensation due to the equivalent doubled proportional gain and, consequently, the voltage deviation are reduced by this amplification ratio.

Nevertheless, although the voltage variations are mitigated, the DC-link voltage is not completely compensated and some deviations are still present. Note that since there is not integral action, the proportional gain shall be tuned in order to fulfill the maximum DC-link voltage deviation requirements.

Fourth simulation relies on the use of a PI controller for the auxiliary DC voltage control. The addition of an integral action eliminates any voltage deviation in steady state, so it is not necessary to increase the proportional gain in order to reduce the deviation. Therefore, both proportional and integral gains of the auxiliary DC voltage control take the same values of those for the grid-side DC voltage control, allowing to replicate the same dynamics. Results are shown in Fig. 11. Now, it can be observed that the integral action is being applied
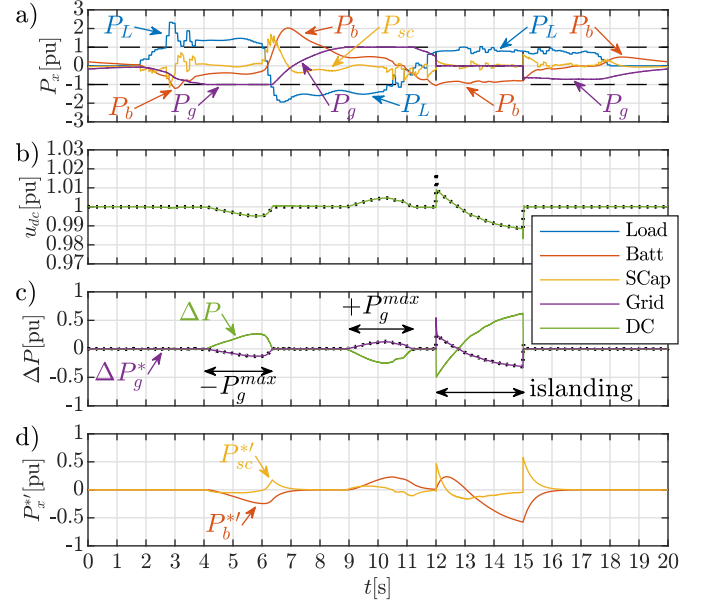

Fig. 10. Simulation results: Auxiliary DC voltage control with P controller. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.
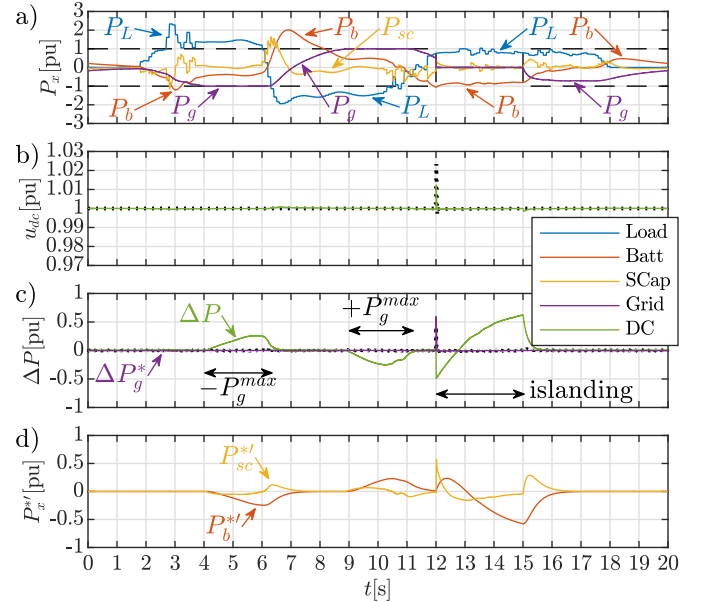

Fig. 11. Simulation results: Auxiliary DC voltage control with PI controller. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

whenever the auxiliary DC voltage control is enabled, so that the DC-link voltage error is completely canceled.

D. Enhanced power reference compensation

In here, the enhanced reference compensation proposed in Subsection III-C, both considering P and PI controllers, is taken into account.

Fifth simulation considers a proportional controller with a gain equal to 2. Results are shown in Fig. 12. As it can be seen,
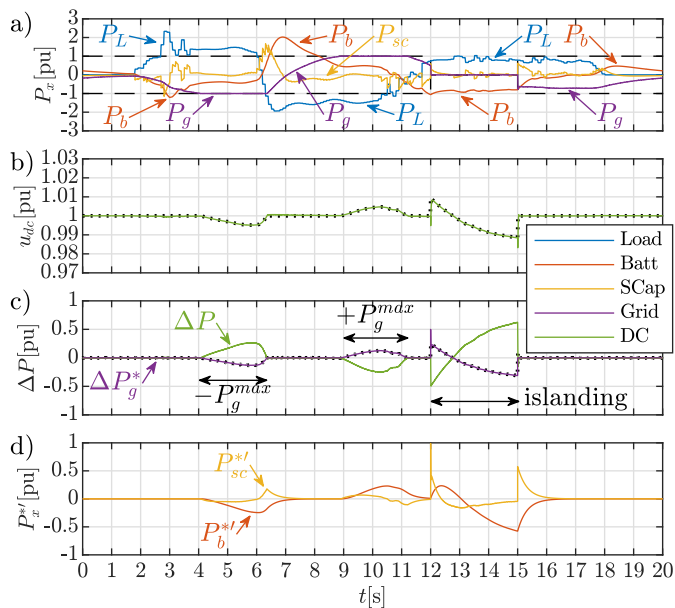
Fig. 12. Simulation results: Enhanced power reference compensation with P controller. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.
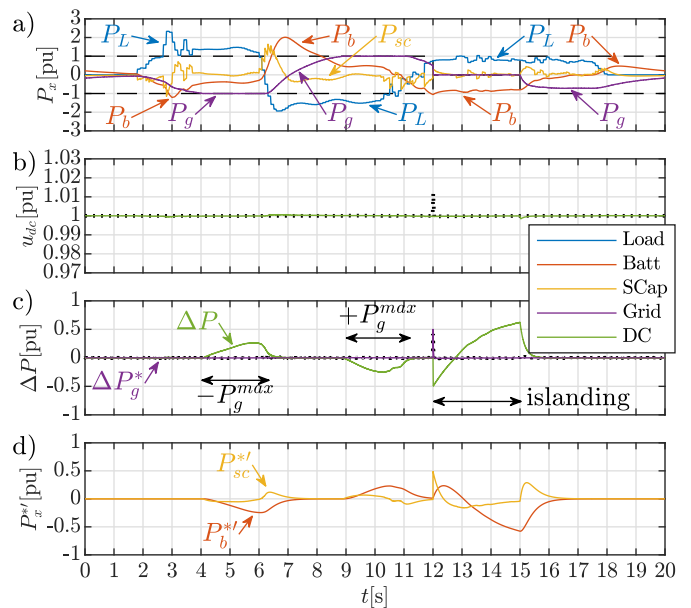

Fig. 13. Simulation results: Enhanced power reference compensation with PI controller. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.
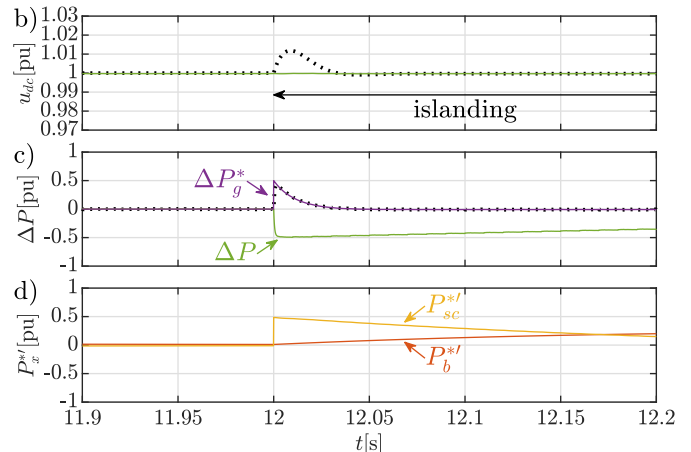

Fig. 14. Detail of simulation results: Enhanced power reference compensation with PI controller when entering in islanding mode. b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

the results are similar to the ones obtained in Subsection IV-C with the P controller (Fig. 10) since the DC-link voltage variations are practically the same. Note that the proportional gain in both cases has the same multiplication factor (2), which explains the similarities in their behavior. Nevertheless, the enhanced power reference compensation shall be chosen over the auxiliary DC voltage control since it is easier to implement.

Sixth simulation relies on the use of a PI controller for the enhanced power reference compensation. Results are shown in Fig. 13. The results are practically the same to the ones obtained in Subsection IV-C with the PI controller (Fig. 11). However, when the system enters in islanding, the enhanced power reference compensation is able to maintain the DC-link voltage constant throughout the test, whereas the auxiliary DC voltage control suffers from a transient voltage deviation.

This is shown in detail in Fig. 14 and Fig. 15. As explained in Subsection III-D, when grid power limit is suddenly reduced, remaining grid power (ΔP_g^*) instantaneously varies with a magnitude equivalent to the grid power reduction. Therefore, enhanced power reference compensation immediately reacts, generating an instantaneous extra power reference for the supercapacitor ($P_{sc}^{*\prime}$) to avoid voltage deviation. However, auxiliary DC voltage control depends on the DC bus capacitor dynamics when reacting, provoking a bandwidth-limited extra power reference for the supercapacitor and hence some voltage deviation.

E. Summary

An overview of the key results (maximum grid power, cumulative error, maximum error and DC voltage overshoot) for all the simulation cases is shown in Table II. As it can be seen, in all the cases with compensation, the maximum grid power is within the expected limits.

TABLE II
PERFORMANCE OVERVIEW OF THE DIFFERENT SIMULATION CASES.

CASE	P_{grid}^{max} [pu]	$\int\|error\|$ u_{dc}[pu.s]	$\|error_{max}\|$ u_{dc}[pu]	$\int\|error\|$ ΔP_g^*[pu.s]	$\|error_{max}\|$ ΔP_g^*[pu]
A) Ideal grid	1.3	0.0029	0.0007	0	0
B) Direct pow	1.0	0.0686	0.0233	1.7869	0.6206
C1) Aux DC (P)	1.0	0.0353	0.0168	0.8945	0.5458
C2) Aux DC (PI)	1.0	0.0031	0.0124	0.0262	0.5972
D1) Enh pow (P)	1.0	0.0355	0.0168	0.8959	0.4999
D2) Enh pow (PI)	1.0	0.0030	0.0016	0.0239	0.4998

The direct power reference compensation is the worst method for all the metrics, followed by the auxiliary DC voltage control and the enhanced power reference compensation with P controller, whose cumulative errors are almost
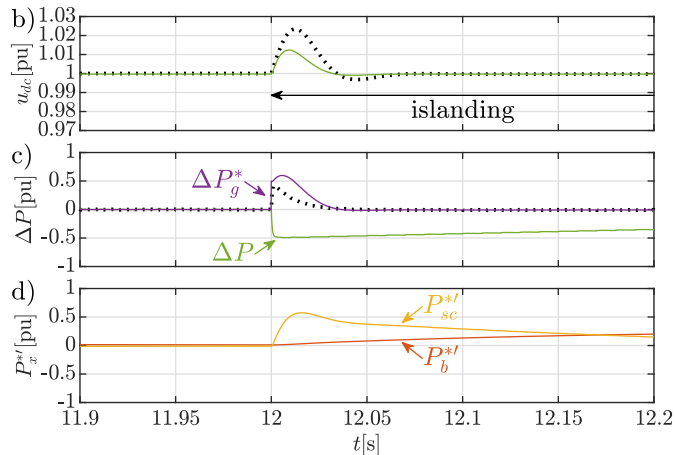
Fig. 15. Detail of simulation results: Auxiliary DC voltage control with PI controller when entering in islanding mode. b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

TABLE III
STATISTICAL ANALYSIS (MEAN, STANDARD DEVIATION) OF THE ERROR BETWEEN THEORETICAL MODEL AND SIMULATION RESULTS.

CASE	mean $u_{dc}[\%]$	SD $u_{dc}[\%]$	mean $\Delta P_g^*[pu]$	SD $\Delta P_g^*[pu]$
B) Direct pow	0.0043	0.0301	0.1728	0.7079
C1) Aux DC (P)	0.0061	0.0439	0.1165	0.7809
C2) Aux DC (PI)	0.0076	0.0361	0.2068	0.9089
D1) Enh pow (P)	0.0061	0.0459	0.0775	0.4198
D2) Enh pow (PI)	0.0073	0.0325	0.1684	0.3561

reduced by 2, since their equivalent proportional gain is twice the one for the direct power reference compensation. These compensation methods without integral action are able to reduce but not totally correct the power mismatch, as it can be seen by comparison with the ideal case.

The compensation methods including a PI controller have a better performance, since their cumulative errors are close to the ideal case. Particularly, the enhanced power reference compensation with PI controller gives the best results, providing a virtually perfect DC-link voltage regulation under saturation conditions. Therefore, the enhanced power reference compensation will be chosen over the auxiliary DC voltage control for the experimental validation.

The dotted lines from Figs. 8-13 show the theoretical model evolution of the DC-link voltage and the remaining grid power by using the simulated power mismatch as input in the transfer functions, in order to compare them with the simulation results. As it can be seen, they virtually match except during large transients. The statistical analysis shown in Table III validates numerically these results, since both the mean and standard deviation of the modelling error are almost negligible.

Table IV shows the total energy flowing through the different power devices, considering positive the energy that flows through the loads and negative the energy that flows through the sources (grid, battery and supercapacitor). By summing all these energies, the circulating energy is obtained. As shown in Table IV, the circulating energy is about 8 pu.s. Assuming an efficiency of 90% in the power converters, losses due

TABLE IV
TOTAL ENERGY FLOWING THROUGH THE DIFFERENT LOADS($+$) AND SOURCES($-$), AND TOTAL CIRCULATING ENERGY ($\sum$) IN SIMULATION RESULTS.

CASE	$+\int|P_L|$ [pu.s]	$-\int|P_g|$ [pu.s]	$-\int|P_b|$ [pu.s]	$-\int|P_{sc}|$ [pu.s]	$\sum\int|P|$ [pu.s]
A) Ideal grid	$+17.04$	-12.64	-9.91	-3.31	-8.82
B) Direct pow	$+17.04$	-10.85	-10.83	-3.39	-8.03
C1) Aux DC (P)	$+17.05$	-10.85	-10.84	-3.40	-8.04
C2) Aux DC (PI)	$+17.04$	-10.73	-10.92	-3.37	-7.99
D1) Enh pow (P)	$+17.04$	-10.85	-10.84	-3.40	-8.05
D2) Enh pow (PI)	$+17.04$	-10.73	-10.92	-3.37	-7.99

to the circulating power are about 0.8 pu.s. Therefore, by comparing these losses with the energy needed by the load (about 17 pu.s), an increment of about 4.7% in the total energy is produced because of the circulating power. The authors consider that increment to be low compared to the benefits regarding the enhanced overall system stability and improved control margins.

F. Effect of power measurement errors and communication delays

All simulations already performed in this section have considered ideal power measurements and no communication delays when sending power references to the ESS (battery + supercapacitor). However, in a more realistic approach, errors in the sensors will distort the power measurements, and delays will affect the references sent from the central controller or the Power Sharing Compensator (PSC) to the battery and supercapacitor interface converters, as shown in Fig. 2. Therefore, additional simulations are conducted with the enhanced power reference compensation to test these phenomena.

Fig. 16 and Fig. 17 show the effect of having a 10% error in the grid power measurement, a 15% error in the battery power measurement and a 25% error in the supercapacitor measurement. Comparing these results to the ones with ideal sensor (Fig. 12 and Fig. 13), it can be seen that additional power mismatches appear in the system. In the case of using a P controller, the magnitude of the voltage deviation will be slightly amplified, but the DC-link voltage will remain almost constant in the case of using a PI controller.

Fig. 18, Fig. 19 and Fig. 20 show the effect of adding a communication delay of 2 ms, 5 ms and 10 ms when sending the power references to the battery and the supercapacitor. A communication delay of 2 ms (Fig. 18) does not provoke any noticeable change in the performance of the system, as can be shown by comparing it to the case with no delays (Fig. 13). However, a delay of 5 ms (Fig. 19) does affect the behavior of the system, deteriorating its performance, as can be seen in the deviation produced in the bus voltage when entering in islanding at 12 s. Finally, a delay of 10 ms (Fig. 20) makes the system unstable. Therefore, the maximum communication delay can be up between 2 ms and 5 ms to not alter the performance of the system. The utilization of industrial communication networks (e.g. Modbus [32], CAN [33], Ethercat [34]...) within that delay range and a distributed control system execution period of $(10\ kHz)^{-1} = 0.1\ ms$
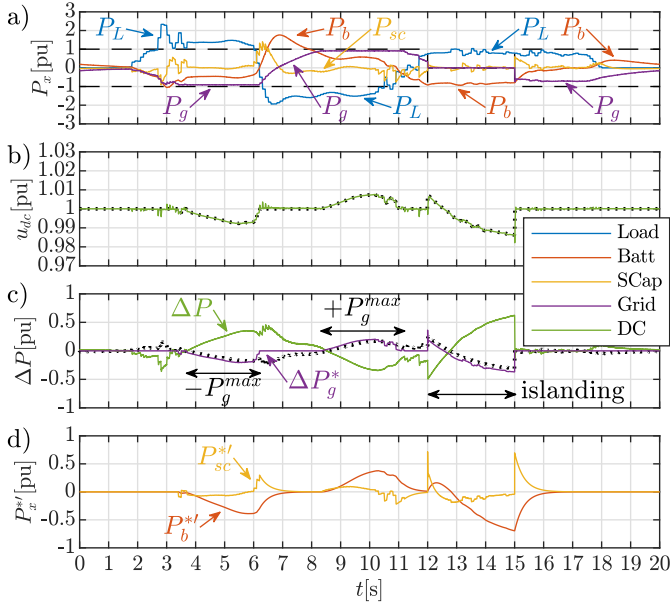
Fig. 16. Simulation results: Enhanced power reference compensation with P controller with power measurement errors: grid, 10%; battery, 15%; supercapacitor, 25%. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.
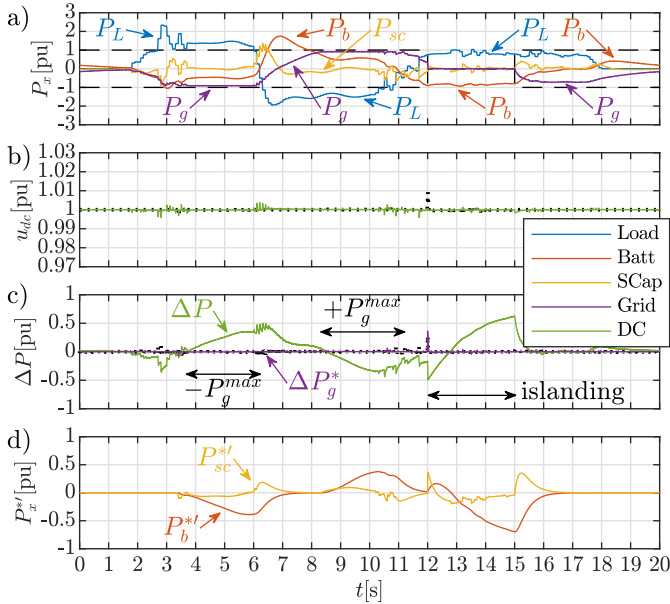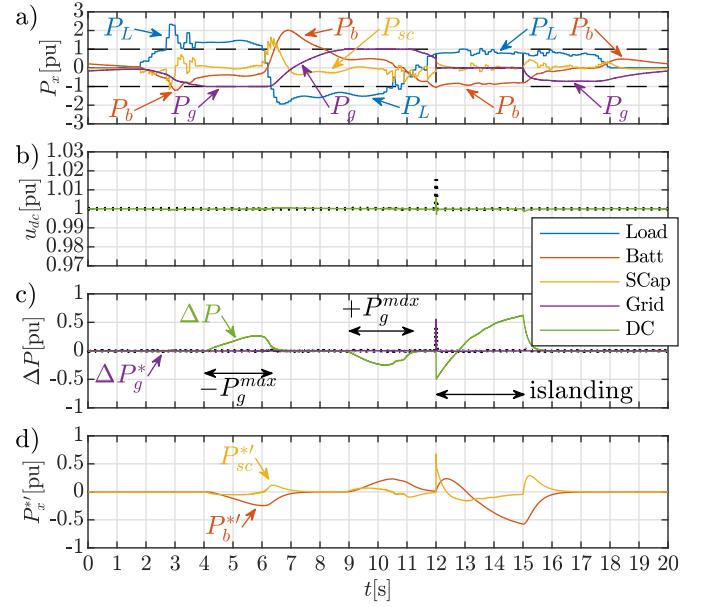

Fig. 18. Simulation results: Enhanced power reference compensation with PI controller with a communication delay of 2 ms when sending power references to battery and supercapacitor. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

Fig. 17. Simulation results: Enhanced power reference compensation with PI controller with power measurement errors: grid, 10%; battery, 15%; supercapacitor, 25%. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.
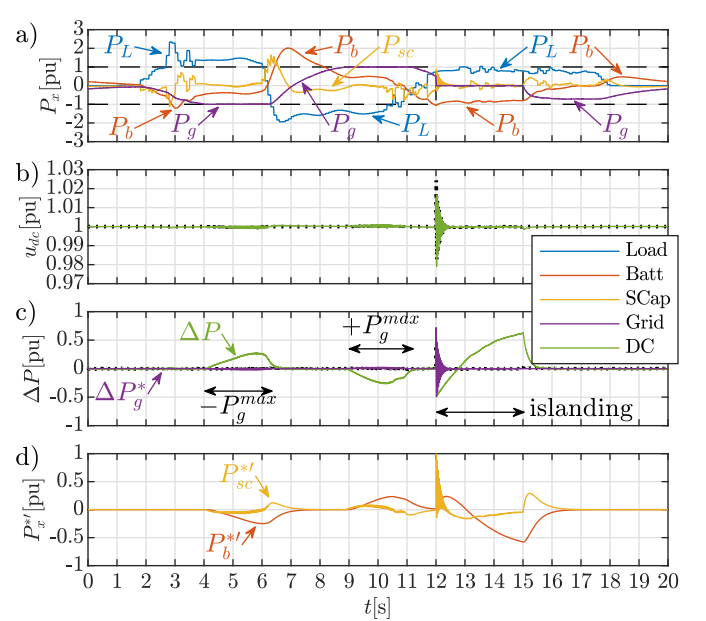

Fig. 19. Simulation results: Enhanced power reference compensation with PI controller with a communication delay of 5 ms when sending power references to battery and supercapacitor. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.

(Table I), 20 times faster than the maximum communication delay, guarantees a proper operation of the system.

V. EXPERIMENTAL RESULTS

Experimental validation is carried out using the setup shown in Fig. 21 for the different tests. The same load power profile and system parameters used in the simulation section are here considered.

The setup consists on two three-phase converters connected through the DC link (back-to-back) and two 4-wire 3-phase inductor filters, which allow the interconnection of the different power units: AC grid, battery, supercapacitor and bidirectional load. The parameters are listed in Table I. The implementation of the control system is carried out by using two different control units: a Texas Instruments TMS320F28335 DSC at
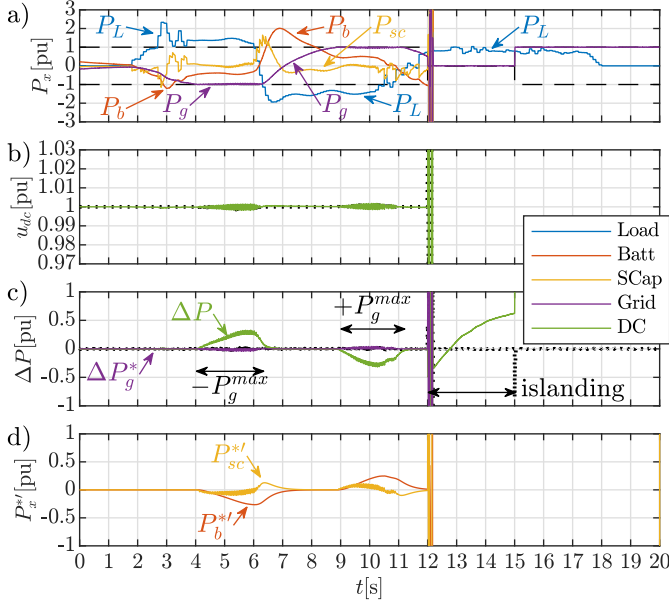
Fig. 20. Simulation results: Enhanced power reference compensation with PI controller with a communication delay of 10 ms when sending power references to battery and supercapacitor. a) Power consumption; b) DC-link voltage; c) Power mismatch (green) and remaining grid power (purple); d) Extra power reference. Legend is the same as Fig. 9.
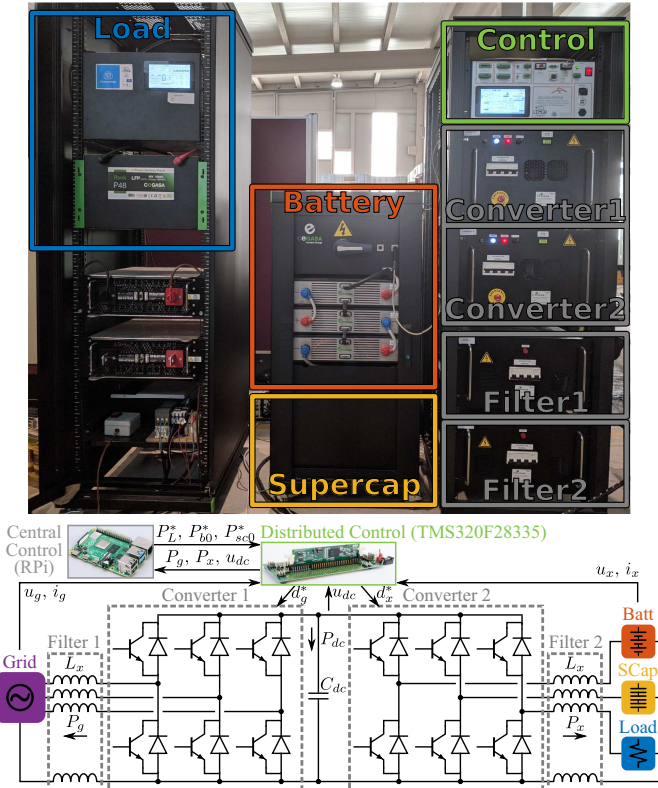

Fig. 21. Experimental setup: Front side and electrical diagram.

Fig. 22. Experimental results: Power sharing issues when the grid power is limited (left, -0.5 pu; right, $+0.3$ pu). a) Power consumption; b) DC-link voltage. Color legend: blue, load; orange, ESS; purple, grid; green, DC bus. Dashed lines: grid power limits.

Fig. 23. Experimental results: Ideal case. a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Extra power reference. Color legend: blue, load; red, battery; orange, supercapacitor; purple, grid; green, DC bus. Dashed lines: grid power limits.

the distributed control system and a single-board computed (SBC) Raspberry Pi at the central control system.

Various experimental tests are carried out to demonstrate the suitability of the different compensation techniques and to address some problems that may appear during the real im-
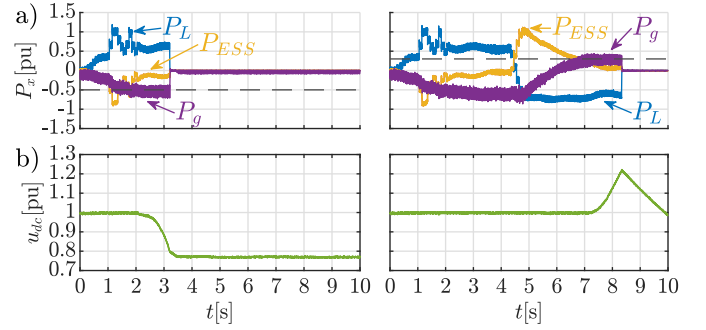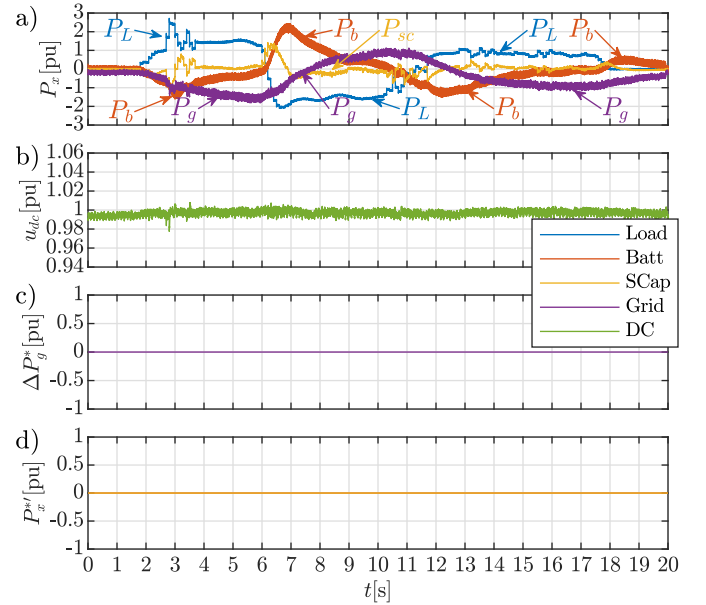
plementation: ideal grid, direct power reference compensation and enhanced power reference compensation.

First experimental test verifies the results shown in Section II (Fig. 4), in which grid power restrictions are applied without compensation. Results are shown in Fig. 22. As it can be seen, the DC-link voltage either drops to the rectifier level or rises to fault values when the grid power reach the limits.

Second experimental test is related to the simulation performed in Subsection IV-A, in which there is neither grid power restriction nor compensation. Results are shown in Fig. 23. As expected and in agreement with the simulation results, the DC-link voltage remains almost unchanged, while the grid power exceeds the considered power limit.

Third experimental test verifies the simulation conducted in Subsection IV-B, in which the direct power reference compensation is applied. Results are shown in Fig. 24. As it can be seen, the grid power is now limited to the maximum one. When the grid control reaches saturation, the DC-link
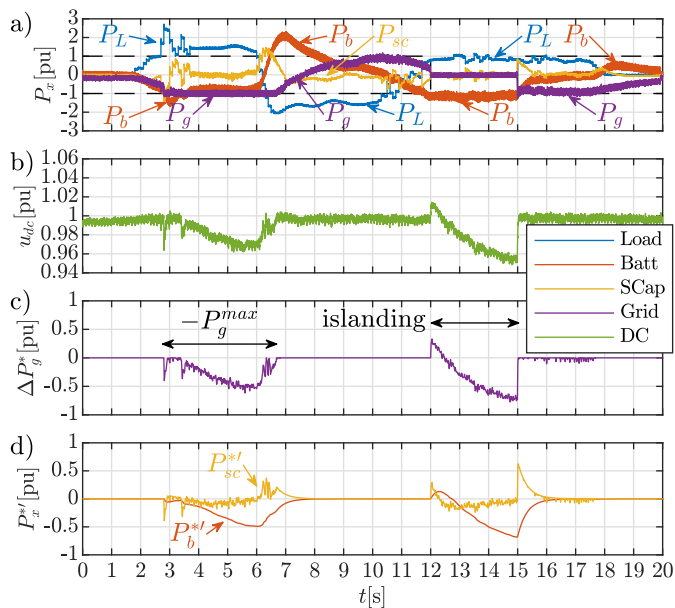
Fig. 24. Experimental results: Direct power reference compensation. a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Extra power reference. Legend is the same as Fig. 23.

Fig. 25. Experimental results: Enhanced power reference compensation with P controller. a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Extra power reference. Legend is the same as Fig. 23.
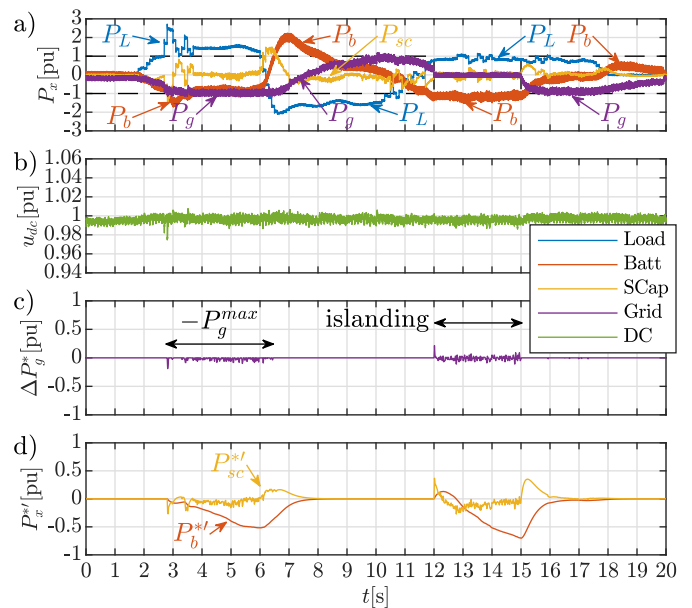

Fig. 26. Experimental results: Enhanced power reference compensation with PI controller. a) Power consumption; b) DC-link voltage; c) Power mismatch; d) Extra power reference. Legend is the same as Fig. 23.
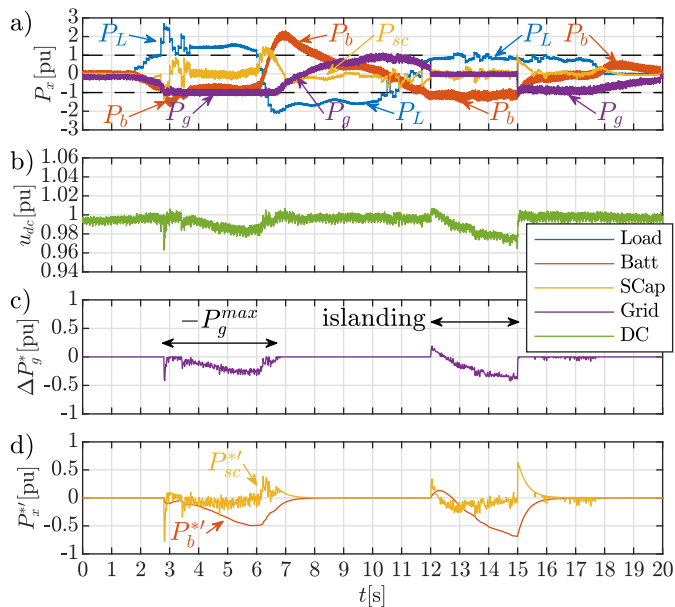
TABLE V
PERFORMANCE OVERVIEW OF THE DIFFERENT EXPERIMENTAL TESTS.

CASE	P_{grid}^{max} [pu]	$\int |\text{error}|$ u_{dc}[pu.s]	$|\text{error}_{max}|$ u_{dc}[pu]	$\int |\text{error}|$ ΔP_g^*[pu.s]	$|\text{error}_{max}|$ ΔP_g^*[pu]
A) Ideal grid	1.6	0.0299	0.0081	0	0
B) Direct pow	1.0	0.1537	0.0440	2.4027	0.7715
D1) Enh pow (P)	1.0	0.0872	0.0254	1.2513	0.4244
D2) Enh pow (PI)	1.0	0.0299	0.0094	0.1444	0.2154

tion IV-D. Results are shown in Fig. 26. It is clear from the results that this compensation technique is the best one, since the DC-link voltage deviation is nearly zero, obtaining a result which is equivalent to the ideal case.

All the experimental tests show similar results (Table V) to those of the simulation. Direct power reference compensation is the worst method for all the metrics, followed by enhanced power reference compensation with P controller, whose cumulative errors are almost reduced by 2, since their equivalent proportional gain is twice the one for the direct power reference compensation. Enhanced power reference compensation with PI controller gives the best results. Therefore, the feasibility of the real implementation of the power mismatch compensation techniques discussed throughout the paper is demonstrated.

Table VI shows the total energy flowing through the different power devices using the same sign convention than in the simulation results. Results are shown in Table VI. The circulating energy is about 9.5 pu.s. Assuming an efficiency of 90% in the power converters, losses due to the circulating power are about 0.95 pu.s. Therefore, by comparing these losses with the energy needed by the load (about 17.7 pu.s), an increment of about 5.4% in the total energy is produced because of the circulating power.

voltage varies but its deviation is mitigated by applying some extra power via the energy storage system.

Fourth experimental test replicates the simulation in Subsection IV-D, in which the enhanced power reference compensation with a P controller is applied. Results are shown in Fig. 25. As expected, this compensation method improves the performance of the direct power reference compensation, with a reduction to a half in the DC-link voltage variations.

Last experimental test follows the enhanced power reference compensation with a PI controller discussed in Subsec-

TABLE VI
TOTAL ENERGY FLOWING THROUGH THE DIFFERENT LOADS($+$) AND
SOURCES($-$), AND TOTAL CIRCULATING ENERGY ($\sum$) IN EXPERIMENTAL
TESTS.

CASE	$+\int |P_L|$ [pu.s]	$-\int |P_g|$ [pu.s]	$-\int |P_b|$ [pu.s]	$-\int |P_{sc}|$ [pu.s]	$\sum \int |P|$ [pu.s]
A) Ideal grid	$+17.70$	-14.06	-10.87	-2.96	-10.19
B) Direct pow	$+17.67$	-11.45	-12.81	-2.94	-9.54
D1) Enh pow (P)	$+17.66$	-11.41	-12.88	-2.97	-9.59
D2) Enh pow (PI)	$+17.66$	-11.07	-13.05	-2.96	-9.43

VI. CONCLUSIONS

This paper has presented some compensation techniques of power sharing error affecting the DC-link voltage regulation in a multi-port DC/DC/AC converter. The proposed alternatives have been analytically discussed and firstly validated by numerical simulations, considering saturation events, transient behavior and operation under islanding mode. Among the presented alternatives, the enhanced power reference compensation with a PI controller shows the best trade-off between implementation complexity and performance. The proposed methods have been also validated by experimental results with a close match between the simulation and the real implementation.

Studied power mismatch compensation techniques are designed to be used regardless of the system nominal power, as shown in (22), (26), (27) and (30). Therefore, these compensation techniques can be applied to utility-scale power systems by resizing the power cells (iPEBBs) to withstand the required voltages and currents. Few tweaks will be needed in the proposed compensation methodology, regarding the voltage/current limits and the tuning of the control gains to adequate to the new values for the physical components.

Moreover, the influence of communication delays is critical on the system performance, making the system unstable if a certain threshold is exceeded. Future work for precisely characterizing these delays and analyzing different compensation techniques, such as the Smith predictor [35], to mitigate the influence of delays and improve the dynamic response of the system.

Lastly, it is worth mentioning that harmonics or unbalances in the grid would provoke undesired variations in the DC-link voltage introduced by the grid power control. In particular, unbalances in the grid will cause DC-link voltage variations at twice the fundamental frequency, whereas $6n{\pm}1$ harmonics in the three-phase grid will induce $6n$ harmonics. These considerations are focus of future works.

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