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A Simple Resonant Switched Capacitor LED Driver Employed as a Fast Pulse-Based Transmitter for VLC Applications

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***Abstract*—This paper presents a Resonant Switched Capacitor (RSC) dc-dc converter for Visible Light Communications (VLC) applications operating as both high efficiency power converter and fast-response data transmitter. By operating under soft-switching, the topology allows for higher switching frequency and higher slew rate, so that the VLC functionality can be embedded into the power stage without an auxiliary switch. In the literature, this additional switch has been presented as a viable implementation of On-Off-Keying (OOK) and Variable Pulse Position Modulation (VPPM) for data transmission, yet at the same time, is a major efficiency bottleneck for higher transmission rates due to its inherent hard-switching operation, justifying efforts in enabling Pulse-Based Transmission (PBT) without this additional switch. A $10\,\mathrm{W}$ prototype was built to demonstrate such feasibility, operating at a switching frequency of $500\,\mathrm{kHz}$, resulting in nominal efficiency of $85\,\%$ during data transmission under VPPM scheme, achieving up to $100\,\mathrm{kpbs}$ for various brightness levels, over a distance up to $1\,\mathrm{m}$.**

***Index Terms*—Resonant Switched Capacitor, dc-dc Converters, Visible Light. Communication.**

I. Introduction

OVER the last years Light-Emitting Diodes (LEDs) technology has been steadily increasing its market penetration by excelling over traditional lighting methods in energy consumption and lifespan, becoming a more viable alternative as production costs falls. More recently, such technology has not only become a major contender in financial viability but also presenting new applications for light emission. In these vanguard fields, applications in communications have been showing a promising prospect for widening wireless bandwidth, previously contained mostly in the Radio Frequency spectrum. By making use of this so far underused spectrum comprised in Visible Light for Communication (hence the common abbreviation VLC) a form of relief for the overgrowing congestion on RF spectrum as technologies become increasingly connected [1] is expected. Additionally, the use of VLC takes advantage of installations already in place, as VLC transmitters can occupy with virtually no change the space of traditional lamps. All of these prospects are made available by the fast dynamic response of LEDs whose switching frequency is able to reach up to 10's of MHz [2] [3] given appropriate equalization techniques and proper filtering of blue light at the receiver.

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The workings of sending information through visible light are based on a modulation scheme that comprises a dc level, essential to perform the LED's dc bias and the illumination aspect of the lamp, and an ac level at a high frequency, imperceptible to the human eye, responsible for the information content [4] [5]. The light signal $s(t)$ can be as described by

$$s(t) = s_{dc} + s_{ac}(t). \tag{1}$$

The different possible modulations strategies are mainly comprised in single-carrier modulated transmission (SCMT), multiple-carrier modulated transmission (MCMT) and pulse-based transmission (PBT) [6]. The SCMT contains modulations inspired by traditional methods of information transmission that uses a usually pure sine carrier waveform as the oscillating part of the signal, where digital information (bits) are coded by either amplitude (ASK), phase (PSK) or frequency (FSK) keying. Furthermore, simultaneously keying both amplitude and phase allows for the more complex Quadrature Amplitude Modulation (QAM) method [4]. In addition to the single-carrier options, the MCMT uses a combination of two or several carriers transmitting multiple sequences of bits instead of a single stream, presenting better response in transmission with multipaths which introduces otherwise the major problem of signal attenuation [5] [7].

For the SCMT and MSMT transmissions, the sinusoidal waveform presents null average by definition, demanding a mandatory sum of a dc, usually provided by a slow-response dc-dc converter with a low-pass filter, while the alternating parcel is provided to the LEDs through a power amplifier (usually linear) that presents faster response but lower efficiency. An alternative to the aforementioned scheme is using a single fast-response converter for providing both alternating and constant aspects of the current, a challenging task that demands more intricate converter capabilities [6].

In contrast to carrier-based philosophies, the PBT method uses current pulses of sufficiently high frequency in order to transmit data. PBT method can also be achieved by either a slow-response converter for the dc bias, with an amplifier adding the square waveform, or by a fast-response converter that performs both functions simultaneously. Once again, the

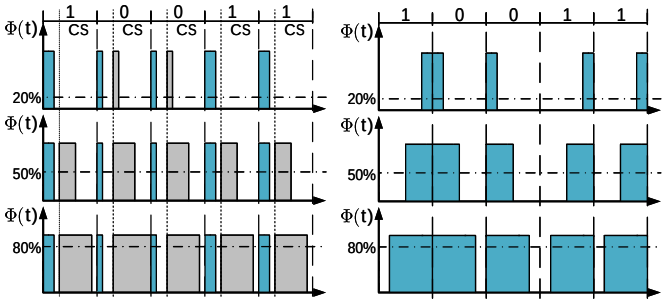

Fig. 1. Example for PBT modulations for (a) OOK and (b) VPPM 1b given three different brightness levels.

former alternative requires fast-response converters that are usually complex and costly alternatives.

Pulse-based transmission opens a third possibility due to the capacity of pulse width variation, which allows for the lighting level modulation. Considering this adding of dimming to the VLC modulation, the IEEE standard 802.15.7 [8] describes three modulation schemes that allows data transmission at different light levels, On-Off-Keying (OOK), Variable Pulse Position Modulation (VPPM) and Color-shift Keying (CSK), characterized as the physical layer (PHY) of the VLC system. Each of the three physical layers describes the application and expected data rate. While layers PHY I and II both allow for OOK and VPPM modulations and differentiate among them in frequency range, PHY III exclusively comprises CSK modulation for high data-rate applications. Since CSK requires RGB LEDs and multiple light detectors, it is beyond the scope of this paper, which aims at high-brightness LEDs (HB-LEDs) that are usually a single blue-LED covered with a yellow phosphor layer, such modulation will not be covered.

As presented in [8], the OOK modulation differentiate the logical high and low bits by means of the pulse width whereas the VPPM technique uses the pulse position for this purpose. The operations of these PBT modulations are highlighted in Fig. 1, which shows that the OOK strategy demands a compensation symbol (CS) for ensuring the desired lighting level. It is worth mentioning that the dc level doesn't need to be supplied by a separate converter. Rather, it is a consequence of the pulse width of the data signal.

Regarding the implementation of the OOK and VPPM modulations in real applications, some works have proposed the use of auxiliary switches in series [9] [10] or in parallel [11] with the LED string. The use of the VLC switch simplifies the transmitter topology to such a degree that even resonant LLC converters were shown to employ it [12]. Although the simplicity of this strategy must be highlighted as a remarkable advantage, the hard-switching operation of this auxiliary switch makes this mechanism not ideal for high data transmission rates. For example, [10] reported an efficiency drop of almost $10\,\%$ when the switching frequency of the auxiliary switch is increased from $50\,kHz$ to $1\,MHz$.

This work proposes a new resonant switched capacitor (RSC), whose fast-response allows embedding of the VLC data transmission in its inner workings. By operating under soft-switching and discontinuous inductor current, it allows for higher switching frequencies without excessive diode and MOSFET losses, enabling data transfer purely through burst-mode operation without an additional VLC switch.

II. RSC Converter

The proposed topology at first resembles the structure of a three-level flying capacitor buck converter, a circuit employed in envelope-tracking applications [13], as shown in Fig. 2. However, such topology employs a large capacitor behaving as a voltage source, whereas in this topology the capacitance is small, to be operated as an energy processing and storage device. The capacitor will act as a switched capacitor once its charge and discharge will be controlled by the active switches and its communion with the inductor will transform the circuit in a resonant topology, yielding its name Resonant Switched-Capacitor (RSC) buck-type converter.

The capacitor and inductor form a resonant network, with its resonance angular frequency ω_o defined by to $\omega_o = 1/\sqrt{L\,C_s}$. In order to simplify the analysis, the output capacitance will be considered high enough in order to keep output voltage relatively constant during continuous operation, a fair approximation given the LEDs threshold voltage doesn't allow the capacitor from significantly discharging. The static voltage gain G of the converter is then defined by $G = V_o/V_{in}$. At the end, the output capacitor's dynamics will be considered in order to calculate rise and fall times of the LED current.

A. Operation of the RSC Buck-type Converter

The six stages for the RSC buck-type converter are shown in Fig. 3. Every stage begins and ends with the switched capacitor either fully charged or fully discharged. Therefore, in order to begin the operational analysis, the initial conditions for the stages must be found and hence the voltages at the resonant capacitor while fully charged and discharged must be determined. It is then necessary to calculate the voltage at the resonant capacitor capable of forward biasing the blocking diodes in stages 1 and 3 which results in the maximum and minimum voltages at the resonant capacitor respectively. Doing so through the analysis of the $[V_{in} - C_s - D_2]$ loop in Fig. 3a and the $[C_s - D_1]$ loop in Fig. 3d, one must find that for the RSC Buck converter, the charged and discharged conditions of the resonant capacitor are given by:

$$V_{max} = V_{in}\ ;\ V_{min} = 0 \tag{2}$$

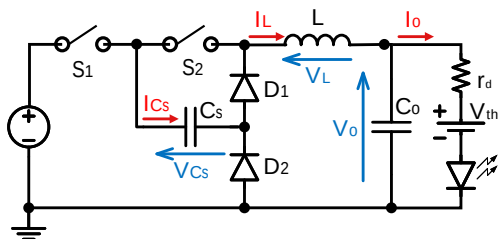

Fig. 2. RSC Buck-type Converter.

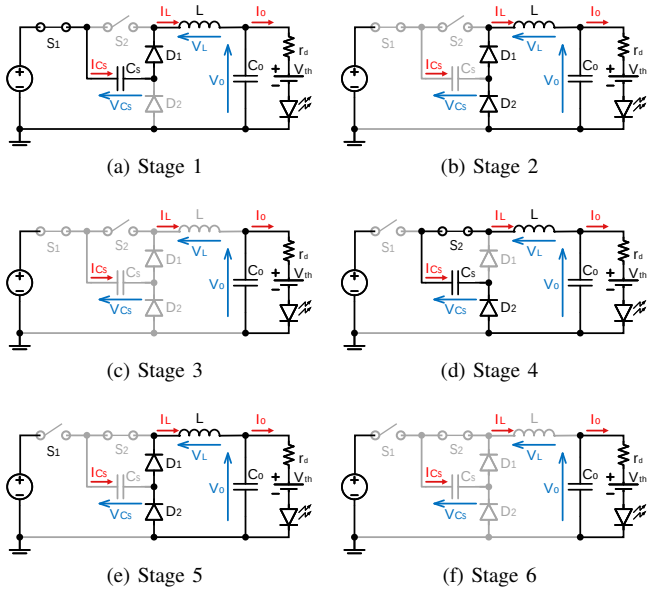

Fig. 3. Stages of operation of the RSC Buck converter.

With the initial conditions of stages 2 and 4 determined above, the operational analysis of each of the states are drawn in the following.

1) Stage 1 [t_0,t_1] - Fig. 3a: The voltage source supplies energy to the circuit, both by charging the capacitor and by supplying the load through the $[V_{in} - S_1 - C_s - D_1 - L - V_o]$ loop. Describing the states $v_{Cs}(t)$ and $i_L(t)$ through the loop and node equations and substituting one in another, the voltage at the switched capacitor and the current through the diode can be found as:

$$\begin{cases} v_{Cs}(t) = (V_{in} - V_o)\,(1 - \cos(\omega_0)\,(t - t_0)) \\ i_L(t) = C_s\,\omega_0\,(V_{in} - V_o)\,sin(\omega_0\,(t - t_0)) \end{cases} \tag{3}$$

This stage lasts until the capacitor is charged to the point where D_2 no longer is reverse biased, which occurs at $t = t_1$ where $v_{Cs}(t_1) = V_{in}$. By replacing this value at the first part of (3) the time delay of the first stage is found as:

$$\Delta t_1 = t_1 - t_0 = \frac{1}{\omega_0}\,acos\left(\frac{G}{G-1}\right) \tag{4}$$

Finally, by using (4) in the second part of (3), the residual current at the inductor at the end of stage 1 can be found by:

$$i_L(t_1) = C_s\,V_{in}\,\omega_0\,\sqrt{1 - 2\,G} \tag{5}$$

The above equation yields a real value if the converter operates according to the constraint $G \leq 1/2$, which limits the voltage range for the application.

2) Stage 2 [t_1,t_2] - Fig. 3b: Once the diode D_2 is forward biased, the capacitor has its voltage clamped at V_{in}. The inductor, however, still presents residual energy and forces current through the closed loop. Analyzing the loop created by the diodes, the state-variables can be found through:

$$\begin{cases} v_{Cs}(t) = V_{in} \\ i_L(t) = C_s\,V_{in}\,\omega_0\,\sqrt{1 - 2\,G} - \frac{V_o}{L}\,(t - t_1) \end{cases} \tag{6}$$

This state ends at $t = t_2$ with the inductor current reaching zero, allowing the timespan of this stage to be calculated through:

$$\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_0\,G}\,\sqrt{1 - 2\,G} \tag{7}$$

3) Stage 3 [t_2,t_3] - Fig. 3c: During this stage neither the inductor nor the capacitor absorbs or supply energy, such that:

$$\begin{cases} v_{Cs}(t) = V_{in} \\ i_L(t) = 0 \end{cases} \tag{8}$$

The end of this stage happens when the control signal changes, turning off switch S_1 and turning on switch S_2, which occurs at the half of the switching period. Therefore:

$$t_3 = \frac{T_s}{2} = \frac{1}{2\,f_s} \tag{9}$$

Once DCM operation is required for zero-current turn-on of the MOSFETs, the sum of the timespan required for stages 1 and 2 must be lower than the end of stage 3, that is,

$$\Delta t_1 + \Delta t_2 < t_3. \tag{10}$$

This constraint allows for defining the a relationship between the resonant and the switching frequencies:

$$\omega_0 > 2\,f_s\,\left(acos\left(\frac{G}{G-1}\right) + \frac{1}{G}\sqrt{1 - 2\,G}\right) \tag{11}$$

4) Stage 4 [t_3,t_4] - Fig. 3d: The second half of the switching period is marked by the switch S_1 being in blocking condition while the switch S_2 is active. During stage 4 the capacitor can finally discharge, releasing its stored energy from stage 1, magnetizing the inductor. Through the analysis of the loop and node present at the active circuit the state-variables can be described as:

$$\begin{cases} v_{Cs}(t) = V_o + (V_{in} - V_o)\,\cos(\omega_0\,(t - t_3)\,) \\ i_L(t) = C_s\,\omega_0\,(V_{in} - V_o)\,sin(\omega_0\,(t - t_3)) \end{cases} \tag{12}$$

The end of this stage occurs at $t = t_4$, marked by the complete depletion of energy at the capacitor until the forward biasing of diode D_1, which then stops the capacitor in decreasing its voltage. The duration of this stage is the same as stage 1, which can be found by (4). Therefore, the residual energy at the inductor by the end of state 4 is the same as state 1, and its current can also be described through (5).

5) Stage 5 [t_4,t_5] - Fig. 3e: Once more, stage 5 is a reflection of stage 2, where the capacitor maintain its voltage while the inductor returns its stored energy. The state-variables during this time period can be descried through:

$$\begin{cases} v_{Cs}(t) = 0 \\ i_L(t) = C_s\,V_{in}\,\omega_0\,\sqrt{1 - 2\,G} - \frac{V_o}{L}\,(t - t_4) \end{cases} \tag{13}$$

The duration of time of stage 5 can also be found by (7).

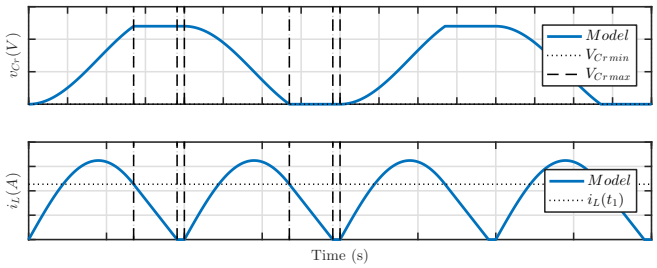

Fig. 4. Comparison between simulation and theoretical predictions of the state variables waveforms derived.

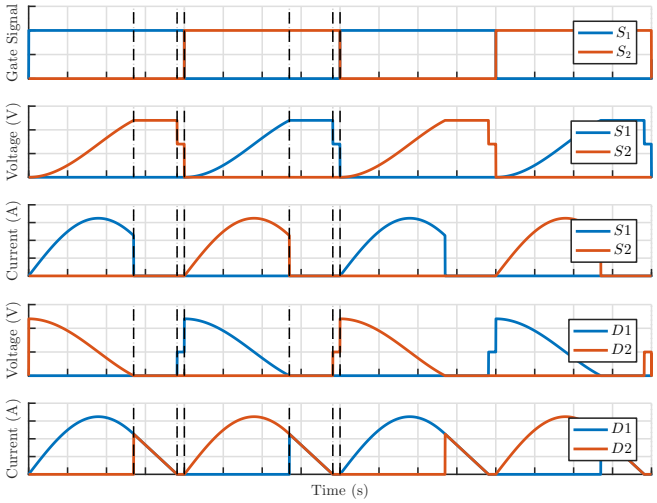

Fig. 5. Soft-switching evaluation for the proposed example.

6) Stage 6 [t_5,t_6] - Fig. 3f: Finally, Stage 6 is marked by both state-variables remaining constant values once again, with the elements capable of storing energy unable to charge or discharge.

$$\begin{cases} v_{Cs}(t) = 0 \\ i_L(t) = 0 \end{cases} \tag{14}$$

The theoretical waveforms are plotted in as previously derived. Figure 4 describes the switched capacitor voltage and inductor current, while Figure 5 highlights voltage and current at the semiconductors, proving operation under soft-switching.

B. Turn-on and turn-off dynamics

With the absence of a VLC switch, the output loop will always form a closed path for circulating current. In steady state, this shouldn't be a problem once stages 3 and 6 are ideally much shorter than their predecessors in order to ensure smallest inductor current peaks. However, for VLC applications through pulse-based modulations, this outer loop must be taken into account, once the required off-times of the burst mode will lead to possible significant discharge of the output capacitor. As a result, the pulses will suffer delays during both turn on and turn off, which can affect how the signal is interpreted in the receptor if not properly into account.

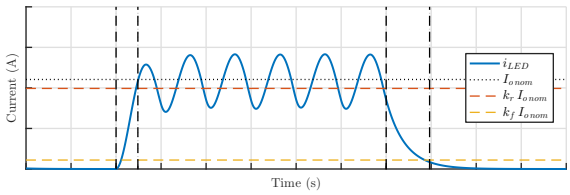

Fig. 6. LED Turn-on and turn-off times.

1) turn-off: The turn off of the converter will ideally occur alongside stage 6, assuming DCM operation for maximum efficiency. The output active loop is composed by the output capacitor and the LED. The current waveform during turn off is found through (15).

$$i_o(t)_{off} = I_{o\,nom}\, e^{-t/\tau_o} \tag{15}$$

Where τ_o is defined as described through (16).

$$\tau_o = r_d\, C_o \tag{16}$$

Considering $t = t_{fall}$ where current falls to an arbitrary factor k_f of the output average current ($i_o(t_{fall}) = k_f\, I_{o\,nom}$), the time delay can be found through (17).

$$t_{fall} = \tau_o\, ln(1/k_f) \tag{17}$$

2) turn-on: Equivalently, the turn on dynamics will occur during stage 1, where the analyzed current path contains the switched capacitor and the inductor in parallel to the output loop. The initial output voltage for this loop must also be considered as the minimum capacitor voltage, i.e., the LED threshold voltage V_t. The description of the current behavior during this timespan in given through

$$i_o(t)_{on} = \frac{V_{in} - V_t}{r_d + \dfrac{Z_o\,(\tau_o^2\,\omega_o^2 + 1)}{sin(\omega_o\, t) + \tau_o\,\omega_o(e^{-t/\tau_o} - cos(\omega_o\, t))}} \tag{18}$$

where Z_o is defined as $Z_o = \sqrt{L/C_s}$.

Such transcendental equation must be solved numerically in order to find the required time $t = t_{on}$ for the output current to reach an arbitrary k_r factor of the average output current.

The theoretical turn-on and turn-off LED waveforms are displayed in Fig. 6, where the definitions of k_r and k_f can be visually described.

III. VLC-oriented Design Example

In order to demonstrate the capabilities of the RSC Buck converter to be designed in the light of the VLC requirements, this section will discuss the step-by-step design process for a $10\,W$ LED converter fed by a $48 - V$ power source. Other significant data are highlighted in Table I.

A. Data transmission and power requirements

The average value of the inductor current, presented in (19), can be calculated by means of its waveforms presented in previous section. This result can be used together with the definition of the average output power $P_o = V_o\, I_o$ to yield (20). This equation relates the equivalence between output power, switched capacitor's capacitance and switching frequency.

$$I_L = C_s\, f_s\, \frac{V_{in}}{G} \tag{19}$$

$$P_o = C_s\, f_s\, V_{in}^2 \tag{20}$$

Once the output power is is predetermined by load and capacitance values must follow commercial availability, the frequency is used as the main design variable. Once a finite integer number of high-frequency pulses are allowed in data period, the transmission rate f_d is a multiple of the switching frequency f_s. So as it can be seen, the process of choosing data transmission rate is tied to the load power and the design must be made somewhat iterative, rather than in closed form. This first part of the design process can be divided as follows.

1) Step 1 - VLC requirements: The relation between data frequency and converter switching frequency describes an integer value that represents the amount of high-frequency pulses fitting a single data period. This factor represents the inverse of the dimming resolution ($\Delta_{dim} = f_d/f_s$) achieved by the transmitter while still preserving DCM.

A dimming resolution of up to $20\,\%$ was chosen, allowing data transmission at a rate of 5 times the switching frequency. With switching frequency reaching up to $500\,kHz$, a transmission rate of $100kbps$ is expected. However, it is also possible to reduce dimming resolution with a data transmission rate trade-off, such that transmissions of $50kpbs$ are possible for intermediate brightness levels intervals of $10\,\%$.

2) Step 2 - Power corrections: In order to ensure data transmission at the LED's nominal power, a power correction is required for the converter design such that nominal LED conditions are achieved for minimum dimming. This corrections are shown in (21) assuming the LED's nominal power must be processed for the converter operating at 90$ of its maximum power.

TABLE I
SOURCE AND LOAD VALUES.

LED		
Dynamic Resistance	r_d	$6.16\,\Omega$
Threshold Voltage	V_t	$17.24\,V$
Nominal Current	I_s	$0.5\,A$
Output Power	P_o	$10\,W$
Nominal Output Voltage	$V_{o\,nom}$	$20.32\,V$
Input Voltage	V_{in}	$48\,V$

$$\begin{cases} I_o = \frac{0.5\,A}{0.9} & \rightarrow I_o = 0.556\,A \\ V_o = V_t + r_d\, I_o & \rightarrow V_o = 20.662\,V \\ P_{max} = I_o\, V_o & \rightarrow P_{max} = 11.476\,W \\ G = \frac{V_o}{V_{in}} & \rightarrow G = 0.43 \end{cases} \tag{21}$$

3) Step 3 - Capacitor selection: With switching frequency set as $f_s = 500\,kHz$ and output power set at $P_{max} = 11.476\,W$, (20) can be used in order to find the required capacitance of the switched capacitor C_s through (22).

$$C_s = \frac{P_{max}}{f_s\, V_{in}^2} = \frac{11.476\,W}{500\,kHz\,(48\,V)^2} \rightarrow C_s = 9.964nF \tag{22}$$

An arrangement of three $3.3\,nF$ parallel-connected capacitors is then chosen in order to properly divide circulating current and reduce possible heating of the switched capacitor. It must be remarked that when no commercial value of capacitance is found, switching frequency cannot be changed without altering the data rate transmission, and these three initial steps must be simultaneously fine-tuned. Having found a relatively acceptable capacitance value through commercial capacitor arrangements, the design can be proceeded.

4) Step 4 - Output Capacitor: The selection of the output capacitor will directly affect the fall time of the VPPM modulation, which should be observed according to (15). The worst-case scenario occurs while sending the two subsequent $1's$ during minimum dimming, where a larger fall time of the first bit could cause the erroneous detection of the second bit as a zero. During minimum dimming, a delay of one switching period is expected between the ending of stage 6 of the first bit and the beginning of stage 1 for the second. Therefore, it is reasonable to expect a detector that samples around the data period edge at a distance of half a switching cycle, which would be an appropriate delay time for the converter to turn off. With that assumption, the output capacitor can be chosen by selecting the capacitance value that causes the current to reach a factor k_f of its nominal value at the required time. This capacitance is described as

$$C_o = \frac{1}{2\, f_s\, r_d}\, \frac{-1}{ln(k_f)}. \tag{23}$$

However, the output capacitance will also directly affect the output voltage and current ripple, such that blindly selecting a capacitor for a given fall time without considering these effects can be detrimental to the LED's photometrical performance. In order to calculate the output voltage ripple it is required an integration of the output capacitor current waveform in order to estimate charge accumulation at the output capacitor according to (24).

$$Q_o = \int_{\alpha_1}^{t_1} [\, i_{L\,stage1}(t) - I_L\,]\, dt + \int_{t_1}^{\alpha_2} [\, i_{L\,stage2}(t) - I_L\,]\, dt \tag{24}$$

Where α_1 and α_2 are the crossing points where the output capacitor current waveform touches zero, given by (25).

$$\begin{cases} \alpha_1 = \dfrac{1}{\omega_o}\, asin\left[\dfrac{f_s}{\omega_o}\dfrac{1}{G\,(G-1)}\right] \\ \alpha_2 = \dfrac{1}{\omega_o}\, acos\left(\dfrac{G}{G-1}\right) - \dfrac{f_s}{\omega_o^2\, G} + \dfrac{\sqrt{1-2\,G}}{\omega_o\, G} \end{cases} \tag{25}$$

As can be seen, a value for resonant frequency ω_o is required for these calculations, which can't be determined once the inductor was not selected at that point. However, it will be desired to select an inductance value such that the converter operates near the DCM limits in order to reduce the maximum current peak value. Therefore, a fair estimation is to use the limit resonant frequency value given in (11).

Once the output capacitor charge has been calculated, the LED current ripple can be given by (26).

$$\Delta I_o = \frac{Q_o}{r_d\, C_o} \tag{26}$$

The relation between output capacitor, current ripple and fall-time are graphically shown in Fig. 7. The time delay is calculated considering the time that the voltage reaches $k_f = 0.1$ times its nominal value. As can be seen, smaller values of capacitance lead to shorter fall times, at the cost of increased current ripple. Using the parameter of t_{fall} as half the switching period and choosing the next commercially available caacitor ($C_o = 68\,nF$) lead to a current ripple of $\Delta I_o = 361mA$ with a fall time of $t_{fall} = 964\,ns$.

It is important to remember that although output current ripple seems excessive (around $65\,\%$ of the nominal current), the light modulation standard for this order of frequency is rather broad [14]. For instance, a light modulation of $100\,\%$ is allowed by around $1.2\,kHz$, enabling the PBT modulations with embedded dimming for higher frequencies. For instance, in this example VPPM is achieved at $f_d = 100\,kHz$ and $f_d = 50\,kHz$, far above the limit. Around the switching frequency of $f_s = 500\,kHz$, not only the limit would be higher, but also the light modulation is smaller, meaning that for the output capacitor itself, a design focused on response time is adequate.

5) Step 5 - Inductor: The inductance selection must be trifold: it must consider the inductor effect on the rising time, on the inductor current ripple and must be limited to a maximum value in order to assure DCM operation.

Once again, these relations can be displayed graphically. In order to describe the effect of the inductance at the rising time, the calculation provided in (18) must be solved numerically for t_{rise} such that $i_o(t_{rise}) = k_r\, I_o$. This relation shows that the rising time is affected by every single reactive element in the circuit. However, once both capacitors are more closely related to different variables, it is desired to considered them constants, while inductance value can be chosen in order to tune rise time.

In the meantime, the relation between inductance and peak inductor current can be found at time instant t where current value in (3) reaches maximum value. This calculation can be described by

$$\Delta I_L = \frac{\sqrt{L\, C_s}}{L_s}\,(V_{in} - V_t). \tag{27}$$

Finally, the maximum limit of inductance is described according to the definition of ω_0 and (11), resulting in

$$L_{max} = \frac{1}{\omega_0^2\, C_s} \rightarrow L_{max} = 9.31\,\mu H. \tag{28}$$

The comparison between the three relations are displayed in Fig. 8, where the rise time is calculated as the delay it takes the current to reach $k_r = 0.9$ times the nominal current. As can be seen, the calculation of rise time fails for smaller ranges, but is still valid for a significant range. Nevertheless, it can be seen that just by the DCM limitation, the choice of the inductor already produces rise time significantly smaller than fall times and should not produce any sampling problem even in worst case scenario. Finally, the inductor of choice is $L = 8.2\mu\, H$, the next commercially available inductor smaller than the DCM limit (28). The rise time expected is $t_{rise} = 484\,ns$ whereas the inductor peak current is $\Delta I_L = 0.968\,A$.

IV. Experimental Results

In order to evaluate experimentally the operation of the converter, a prototype was built. This section describes the experiment set up and results. The results of the design process are summarized in Table II, detailing the passive and components used.

A. Transmitter

The transmitter is composed by the RSC buck converter and an optical isolator that decouples the high-power circuit to the

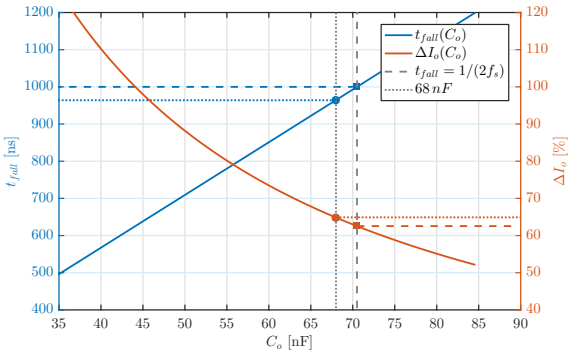

Fig. 7. Output capacitor influence in t_{fall} and ΔI_o.

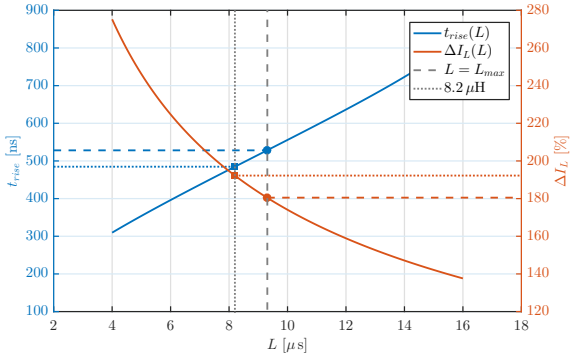

Fig. 8. Inductor influence in t_{rise} and ΔI_L.

TABLE II
SIMULATION VALUES OF RSC BUCK CONVERTER.

Source and Load		
Input Voltage	V_{in}	$48\,V$
Output Voltage	V_o	$20.662\,nF$
Output Current	I_s	$0.552\,A$
Output Power	P_o	$11.405\,W$
Converter Design		
Switched Capacitance	C_s	$3 \cdot 3.3\,nF$
Inductance	L	$8.2\,\mu H$
Output Capacitance	C_o	$68\,nF$
Switching Frequency	f_s	$500.000\,kHz$
Active Switch (GaN-FET)	$S_1; s_2$	$LMG5200$
Diodes (Schottky)	$D_1; D_2$	$PMEG6010$
Delay times		
Rise Time	t_r	$484.322\,ns$
Fall Time	t_f	$964.507\,ns$
Current Variations		
Inductor Peak Current	ΔI_L	$0.968\,A$
LED Current Ripple	ΔI_{led}	$0.361\,A$

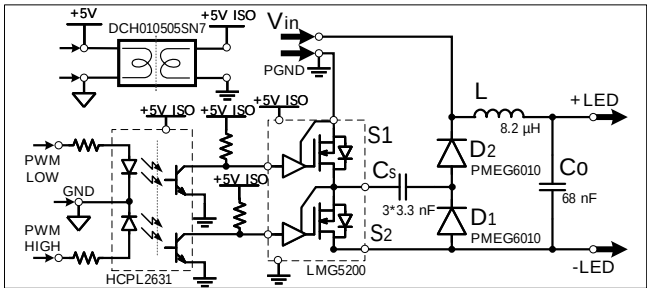

Fig. 9. VLC transmitter schematics based on RSC buck converter.

microcontroller. A TIVA C Series TM4C123G was used in order to synthesize the required PWM signals. The simplified schematics of the transmitter circuit is shown in Fig. 9. The prototypes are shown in Fig. IV-A. The transmitter circuit presents dimensions of $(23mm \cdot 16mm \cdot 19mm)$, and power density of $0.0014\,W/ml$.

B. Receiver

The receiver is composed by a BPW34 photodiode and dual operational amplifier OPA2350 which implements a TIA and a regenerator. The TIA will convert the photocurrent into a voltage signal, adding an offset V_{off} controlled by a potentiometer. This offset regulates the voltage signal in order to compensate for ambient light, allowing a positioning of the

Fig. 10. Transmitter prototype: passive board (top view), GaN-FET board (top view) and passive board (bottom view).

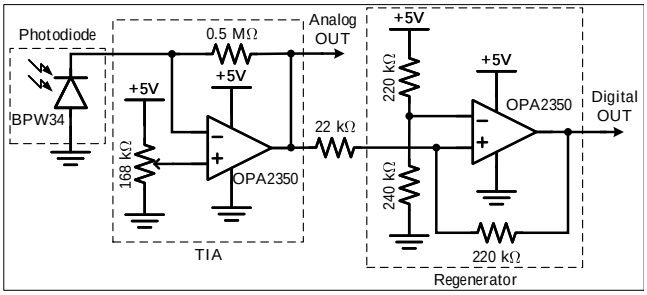

Fig. 11. VLC receiver schematics.

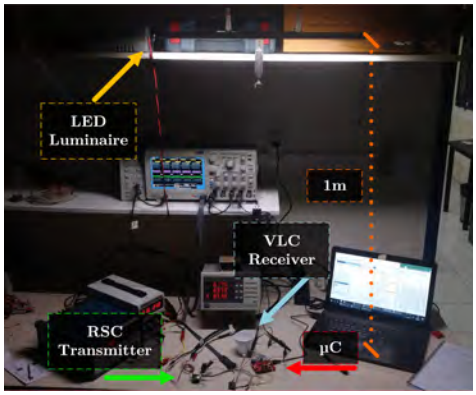

Fig. 12. Experiment setup.

analog output at an appropriate position for the regenerator (which is a non-inverting comparator with hysteresis). As a result, the VLC receiver presents an intermediate analog output, which is proportional to the received light and a final digital output that describes the received light in states of 'on' and 'off' depending on the instantaneous amplitude. The simplified schematics is shown in Fig. 11.

C. Experimental Data

The experiment was set up with the luminaire at a distance of $1\,m$ above the receiver. A picture of the set up can be seen in Fig. 12.

1) Components waveform: Figure 13 displays the main waveforms during steady state, where Fig. 13a highlights current at the inductor and voltage across the switched capacitor. Current and voltage at the active switch S_1 and at the diode D_1 are displayed in Fig. 13b and Fig. 13c respectively. Finally, Fig. 13d displays the output current during burst mode.

The inductor current and switched capacitor voltage waveforms displayed expected behavior albeit non-idealities of the semiconductors plays the minor role of stopping the inductor current to cap at $0\,A$ instantly. The output waveform during burst mode highlights both turn-on and turn-off times as perceived by the light load. The converter takes around $500\,ns$ to reach $90\,\%$ of its nominal value, a time slightly higher than calculated possibly due to the parasitic load capacitance, and around $960\,ns$ to turn-off to $10\,\%$ of its nominal value.

2) Data Transfer: The data transfer at $100\,kbps$ is then evaluated in Fig. 14 for the appropriate allowed light levels. A bit stream of $[01010011]$ is sent repetitively. One can note that

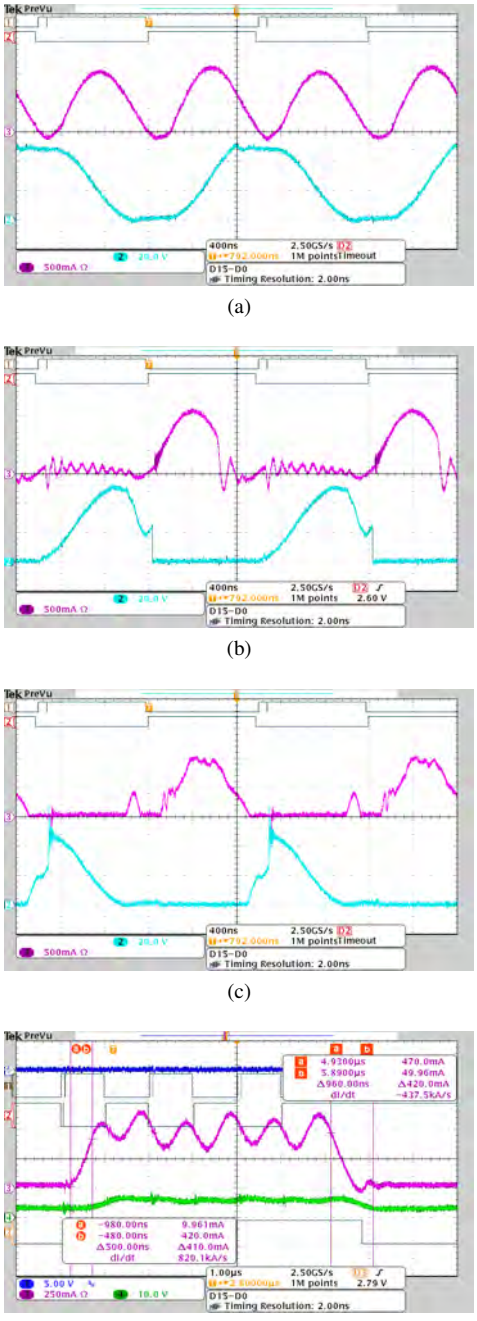

Fig. 13. Voltage and current waveforms at (a) inductor and switched capacitor, (b) active switch, (c) diode and (d) output. Analog channels: CH1 - data, CH2 - Current, CH3 - Voltage, CH4 - Analog output of VLC receiver.

for all cases, the coded bit stream is available at the receiver-side, showing that the proposed converter is able to transmit the desired data.

Both transmitter and receiver operate according to expected, with the system appropriately aligning the light pulse at the beginning of the data period for 0 bit and at the end of the data period for the 1 bit. Finally, the system under duty cycle variation is highlighted in Fig. 15.

3) Efficiency Analysis: In order to analyze the converter's efficiency, power measurements were performed for different light levels while switching frequency is kept constant at $f_s =$

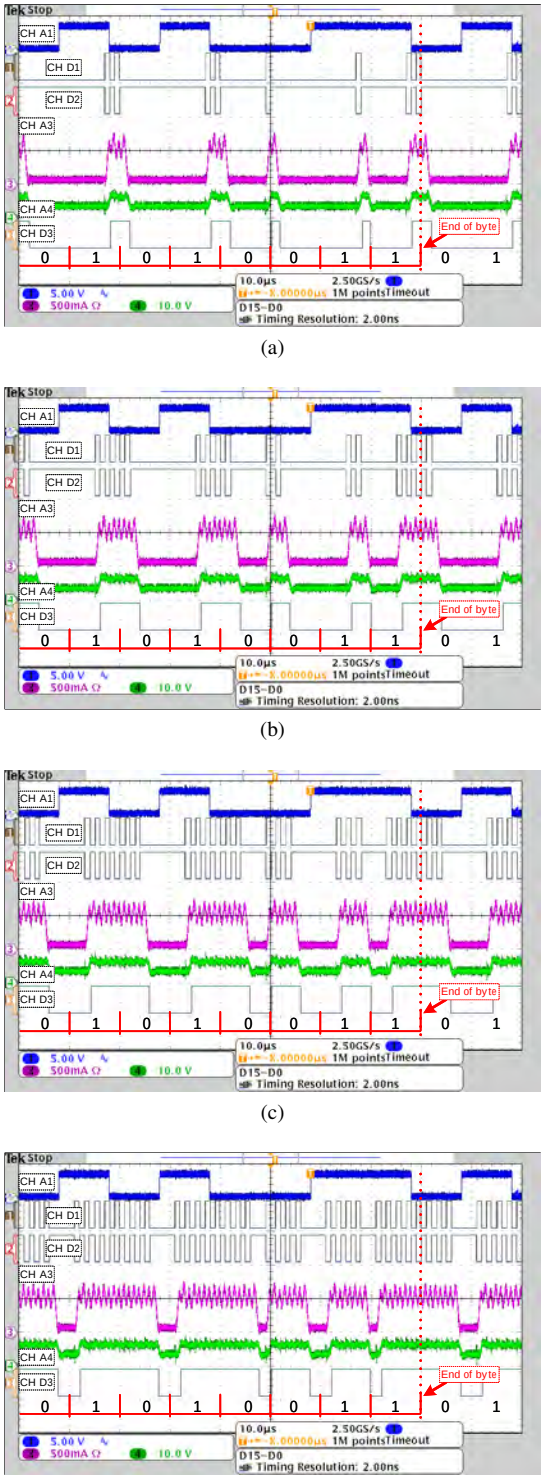

Fig. 14. Data transmission of bit [01010011] at light levels of (a) 20 %, (b) 40 %, (c) 60 % and (d) 80 %. Analog channels: CH A1 (5 V/div) - DATA, CH A3 (500 mA/div) - Output Current, CH A4 (10 V/div) - Analog output of VLC receiver. Digital channels: CH D1 - PWM at switch S_1, CH D2 = PWM at switch S_2, CH D3 = Digital output at VLC receiver. Horizontal scale: $10\,\mu s/div$.

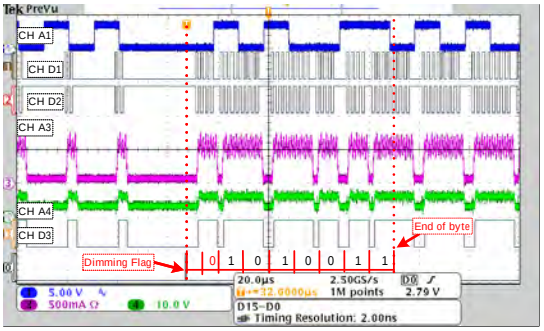

Fig. 15. Data transmission of bit [01010011] at variating light level of 20 % to 80 %. Analog channels: CH A1 (5 V/div) - DATA, CH A3 (500 mA/div) - Output Current, CH A4 (10 V/div) - Analog output of VLC receiver. Digital channels: CH D1 - PWM at switch S_1, CH D2 = PWM at switch S_2, CH D3 = Digital output at VLC receiver. Horizontal scale: $20\,\mu s/div$.

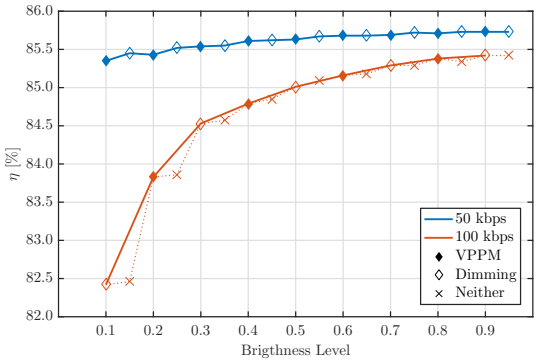

Fig. 16. Efficiency analysis for given brightness levels (constant switching frequency f_s).

$0.5\,MHz$. The results are presented in Fig. 16. On the other hand, efficiency can also be analyzed through the lenses of constant output power by performing variations in both light level and switching frequency, as shown in Fig. 17.

Converter losses are less significant for higher power as the converter reaches efficiencies of up to 85.73 % for transmission rates of $100\,kbps$ and up to 85.42 for transmission rates od $50\,kbps$. The efficiency levels found for the RSC buck converter match efficiency levels found in literature for the same power level. For instance, [15] uses a similar structure

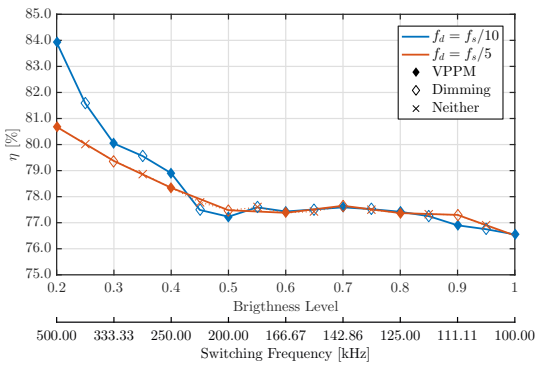

Fig. 17. Efficiency analysis for given switching frequencies (constant output power P_o).

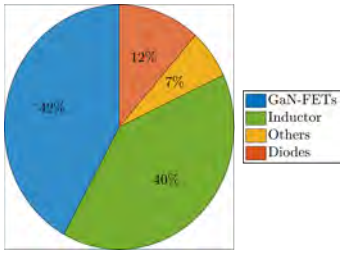

Fig. 18. Power loss breakdown for the main components of the RSC converter.

on a CMOS LED driver for up to $700\,mA$, reaching 83.1 % efficiency in nominal operation. In [16], a power delivery of $10\,W$ can be achieved by a $2V : 5A$ setup or by a $8V : 1.25A$ setup, with respective efficiencies of around 85 % and 80.0 %.

Furthermore, the relation between efficiency and switching frequency was shown to be almost constant at around 77.5 % for lower frequencies, but once again surpassing the 80 % mark for nominal switching frequency.

In order to investigate power loss, a power breakdown for the three major components can be performed by measuring both current and voltage at a finite and integer number of cycles for each component. Figure 18 displays the relative consumption of the GaN-FETs, diodes and inductor. The measurement was performed with burst mode disabled.

It can be noted that the inductor alone is the major loss-causing element with a power loss, close to being equal to the two GaN-FETs combined, indicating necessity of further investigation on the employment of high-frequency cores. Additionally, corrections on the prototype PCB towards reducing current loops are required for a better switching characteristics of the GaN-FETs as well as fewer associated losses.

V. Conclusion

This paper presented a resonant switched capacitor buck-type converter in which burst-mode was used to allow VPPM transmission in VLC applications. The increase of slew rate has becoming a requirement for emerging VLC systems as an alternative to the low efficiency VLC switch currently applied to traditional slow-response converters. The exclusion of the auxiliary switch, however, introduces load dynamics that must be considered in the converter design.

The high-frequency behavior of the converter was analyzed, comparing theoretical waveforms with simulated results. A design methodology was proposed for VLC-oriented converters considering output dynamics. Finally, a prototype was built capable of both data transmission and power processing of $10\,W$. The compact prototype, with dimensions of $(23mm \cdot 16mm \cdot 19mm)$, presented power density of $0.0014\,W/ml$.

Additionally, a VLC receptor was built in order to evaluate data recognition. The system has proven VLC applicability with appropriate burst operation as VPPM transmitter. The receptor was able to correctly recognize bits for several brightness levels.

Finally, a transmission rate of $100\,kbps$ was achieved over a distance of $1\,m$ with a overall efficiency of 85.4 %.

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