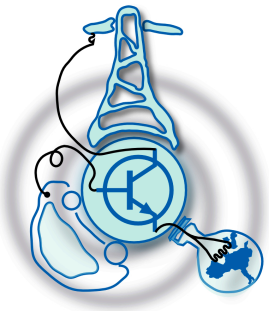
Optimization of the Design of a Half-Bridge LLC Resonant Converter for Fast Charging of Storage in Electric Vehicles

by

Maria-Ruxandra Luca



Submitted to the Department of Electrical Engineering, Electronics, Computers and Systems

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Abstract

This thesis proposes a method for the optimization of a LLC resonant converter in order to achieve maximum efficiency for a desired load. The novelty of this converter is the usage of GaN switching devices instead of Si MOSFETs. The prototype is converting 600 V from the input to a nominal output voltage of 75.6 V, with a maximum output power of 5.2 kW.

First, an initial design is made without using any optimization process to calculate its efficiency. The losses taken into consideration are the core and copper losses generated by the inductors, the switching and conduction losses coming from the GaN switches, plus the losses generated by the rectifier diodes. Afterwards, an optimization algorithm is implemented, which consists of an iterative solver, to determine the optimal design of the inductors which were causing the majority of the losses in the initial design. Maximum efficiency value of 98.6% has been achieved for the optimized converter.

Thesis Supervisor: Jorge García García
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Title: Associate Professor

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Special thanks to my parents who have always supported me though this journey and last, but definitely not least, I express my gratitude towards my friends: Marcos, Mohammad, Konstantin, Matias, and many others with whom I share so many fond memories. With you, my life throughout this master has been anything but monotonous.

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Chapter 1

Introduction

1.1 Background

In the fast evolving world of power electronics, the objective of every designer is to create a highly efficient, reliable and qualitative product. In the case of DC-DC converters, there are many topologies available such as the flyback converter, forward converter, full bridge converter, resonant converter, etc. According to the requirements of the system, one configuration or another can be more suitable.

The commercial success of pulse-width modulation DC-DC converters is mainly due to the fact that they have fixed frequency operation and variable input duty cycle, making the control very easy. However, the switching operation of those converters is highly inefficient, causing overall big losses. Because of the hard switching phenomenon, the converters present electromagnetic interferences issues. Moreover, they are not suitable for high switching frequencies because along with its increase, the stress of the components increases as well, shortening their lifetime. With the implementation of soft switching techniques, the overall performance of the DC-DC converters is improved, by making possible the transitions at turn on or turn off of the switches theoretically with no power losses.

Resonant converters on the other hand are capable of performing soft-switching, this being one of the reasons for gaining attention in recent years. There are two cases in which soft-switching is achieved: Zero Voltage Switching and Zero Current

Switching. By performing the switching operation when the voltage or current is zero, the losses decrease substantially, thus making the overall efficiency of the converter higher.

The category of resonant converters can be also divided further into: LC series resonant, LC parallel resonant, and different combinations of series-parallel configurations such as LLC or LCC. In the case of charging electric vehicles, there is one topology which stands out and is gaining popularity in industrial applications and that topology is the LLC resonant converter. Some of its advantages include high efficiency, reduced power loss, low EMI and high power density, all of which will be discussed in the following chapters.

A few disadvantages worth mentioning would be that the converter achieves the power conversion by using frequency modulation, not PWM. For this reason it may present some difficulties in the design and optimization process as there are multiple modes of operation, each with their own different resonant characteristics. Secondly, it is necessary to include an optimization of the magnetic components. By omitting this step, the efficiency could be lower than expected. A more detailed analysis of the LLC converter can be read in Chapter 2.

The physical system under study in this thesis consists of a 6 kW half-bridge module equipped with GS66516T switches from GaN Systems, the resonant tank inductances which are manually built after completing the optimization process, a series resonant capacitor, a full bridge rectifier consisting of STPS160H100TV Schottky diodes from STMicroelectronics and an CL filter at the output. More in-depth information about the physical system is revealed in the coming chapters [1] [2] [3].

1.2 Objectives

As part of this thesis, the design and optimization of a half-bridge GaN based converter with resonant LLC configuration will be performed. This topic was chosen in order to respond to the request of the Wolfast MotoStudent Team for designing a charger that corresponds to the specifications of their electrical motorcycle battery.

The objectives are as follow:

- Analysis and design of a half-bridge LLC converter.
- Analysis and design of magnetic components.
  - Determining the optimal diameter of the conductor, the number of turns, core size and material, etc.
  - Calculating the magnetic losses of the circuit.
- Simulations to understand and calculate the switching losses and conduction losses of GaN switches.
- Development and implementation of an optimization algorithm for the LLC circuit.
  - Finding the optimal switching frequency in order to achieve the highest efficiency of the converter.
  - Choosing the configuration of the magnetic components that generate the lowest losses.
- Efficiency calculation at different operating frequencies.

It should be noted that, initially, among the objectives of this thesis, the development of the designed prototype was included in order to verify the results obtained from the simulation. However, due to the circumstances taking place in the summer of 2020, this objective could not be completed.

1.3 Thesis Structure

Chapter 2 presents in-depth particularities of the LLC resonant topology along with the steps to design the resonant tank. Moreover, it includes the basic structure of a GaN switch and a comparison between Si and SiC MOSFETs. Finally the chapter ends with a brief overview on the magnetic components present in the circuit, their

losses, and how to start their design by choosing the right magnetic material and core size.

In Chapter 3, the proposed converter is designed. The role of this chapter is to provide an initial design, or a starting point, for its later optimization, that takes place in Chapter 5. A series of simulations have been performed in this sense using MATLAB, datasheets and application notes to determine the value of the resonant tank, and the currents that flow into it. Moreover, the design of the magnetic components is carried out. The core material and type, the diameter of the conductor, the number of turns and the airgap are all parameters that not only influence the value of the losses, but are also needed to build the said inductors.

Chapter 4 deals with the analysis of the results coming from the simulation of the losses. First, an LTSpice model of the proposed circuit is presented. Furthermore, the simulation validates the design developed in the previous chapter. Next, the losses of the switching and magnetic components are calculated. In the case of the GaN devices, a mathematical model that calculates the switching times is developed in MATLAB, which is later checked against the LTSpice simulation. Finally, all the losses are summed and analyzed, and the efficiency of the converter in the initial design is calculated.

The optimization algorithm is presented in Chapter 5, along with the vector that defines all the variables used for the optimization, the objective function and the inequality constraints. In addition, the losses of all the elements from the new circuit are calculated. Moreover, the inductances belonging to the resonant tank are built according to the parameters that result from the said optimization process and their inductance is measured as a function of frequency. Furthermore, a comparison between the initial design and the optimized design is made, with an accent on the power losses and efficiency. Finally, Chapter 6 presents the conclusions withdrawn from conducting the thesis and the possible future work.

Chapter 2

Literature Review and State of the Art

The objective of this chapter is to set a base in order to answer the requirements of the application under study. As a result, this chapter is structured as follows: the first subsection presents a general overview of the LLC converter topology and the design steps, followed by a comparison between GaN switching devices and Si/SiC MOSFETS, with an accent on their structure, existing capacitances and reverse recovery behaviour. The second part of this chapter focuses on an overview of the magnetic components with its afferent literature review on how to choose the right magnetic material and core size.

2.1 LLC Converter Topology

Fig. 2-1 presents the LLC converter topology consisting of an input DC voltage source, a half-bridge power stage drive formed by Q1 and Q2, and driven by an LLC controller. This converter uses a transformer to either step up or down the DC input voltage and to achieve galvanic isolation. This design also requires output

rectifiers consisting of 4 diodes (D1, D2, D3, D4) and an output filter capacitor, C_f and inductance L_f. To control the output voltage, (V_o), Q1 and Q2 are operated at 50% duty cycle. This will put a square wave across an LLC resonant tank consisting of a resonant inductor (Lr), the transformers primary magnetizing inductance (Lm), and a resonant capacitor(Cr).

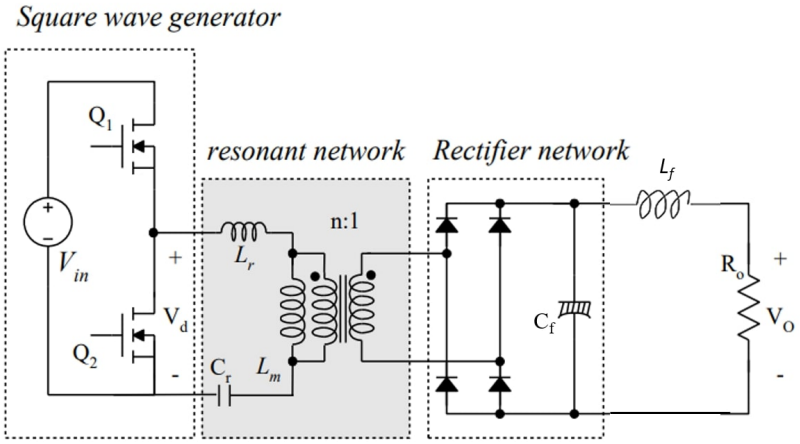


Figure 2-1: Half-bridge LLC converter topology [4].

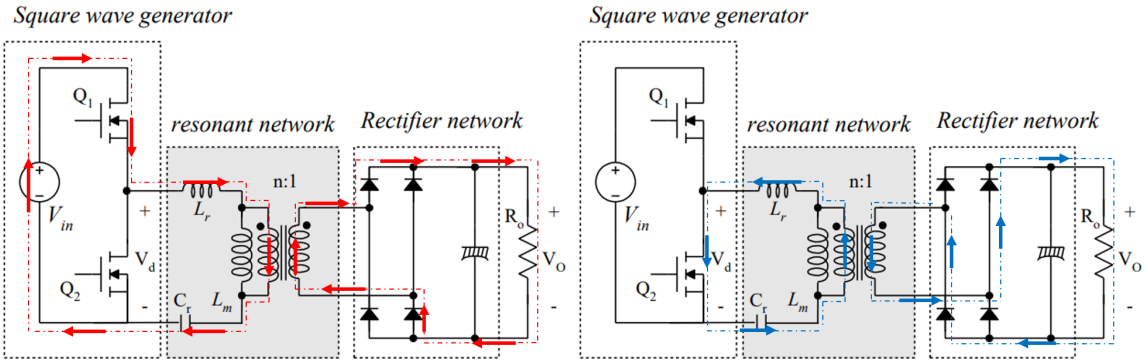
There are two resonant frequencies associated with this resonant topology. The first one appears when the secondary winding is conducting, thus when the output diode bridge is turned on. The magnetizing inductance, L_m, withstands a DC voltage and, as a result, it is not taken into account. The effective resonant frequency is given only by the series inductance, L_r and by the resonant capacitor, C_r. This is the frequency which is normally referred to as the true frequency of the circuit and such a converter is designed to operate in its vicinity. It can be expressed in the following way [5]:

$$f_0 = \frac{1}{2\pi\sqrt{L_r \cdot C_r}} \tag{2.1}$$

The other resonant frequency appears when the power is not delivered to the load and the magnetizing inductance withstands a sinusoidal voltage. Under these conditions, the resonant frequency is given by L_m, L_r and C_r with the following formula:

$$f_p = \frac{1}{2\pi\sqrt{(L_r + L_m) \cdot C_r}} \tag{2.2}$$

f_0 is greater than f_p and the separation between them depends on the ratio between the two inductances L_m and L_r. As it will further be described, in the design of the resonant tank, the ratio between these two inductances is an important parameter.



(a) Positive voltage applied to the resonant tank. (b) Negative voltage applied to the resonant tank.

Figure 2-2: Current flow in the resonant circuit [4].

The power delivery transmission occurs two times in a switching cycle, and can be observed in Fig. 2-2. Figure 2-2a represents the case when Q_1 is on and Q_2 is off. During this period, the resonant tank is excited with positive voltage, thus the power is transmitted to the load, while the capacitor C_r starts to charge. The current flows through the circuit as shown by the red arrows.

In the second half of the cycle, the circuit is excited by negative voltage, resulting in a current that resonates negatively. The equivalent circuit of this condition is shown in Figure 2-2b. The power is still transmitted to the load, this time via Q_2. Moreover, the input DC source is dismissed, and the current flows because of the power charged in C_r in the previous half of the cycle.

Between these two half-cycles, a dead time is necessary. If both switches are on at the same time, massive currents could flow through them, leading to their destruction. Moreover, the dead time provides the condition for the power switches, such as GaN or MOSFETs, to be turned on with zero-voltage switching (ZVS), when operating in the inductive region. In the case of switching frequency lower than the resonant frequency, the rectifier diodes are off with zero-current switching (ZCS).

Depending on the load conditions of the converter, there are three possible oper-

ation modes:

- Below the resonant frequency, f_0;
- At the resonant frequency, f_0;
- Above the resonant frequency, f_0.

For operation at the resonant frequency, the power is delivered to the load throughout the cycles, meaning that the output diode bridge is always on. The current that flows through the resonant inductor, I_{L_r} reaches the value of the current flowing though the magnetizing inductor, I_{L_m}, as seen in Fig. 2-3a. The current transmitted to the secondary becomes zero at the end of the first half-cycle. Under this condition, the switching losses are minimized and the converter circulating currents come down. This property is only achieved in one operating point. In practice, input voltage and load vary such that the converter operates at frequencies either higher or lower than the resonant frequency.

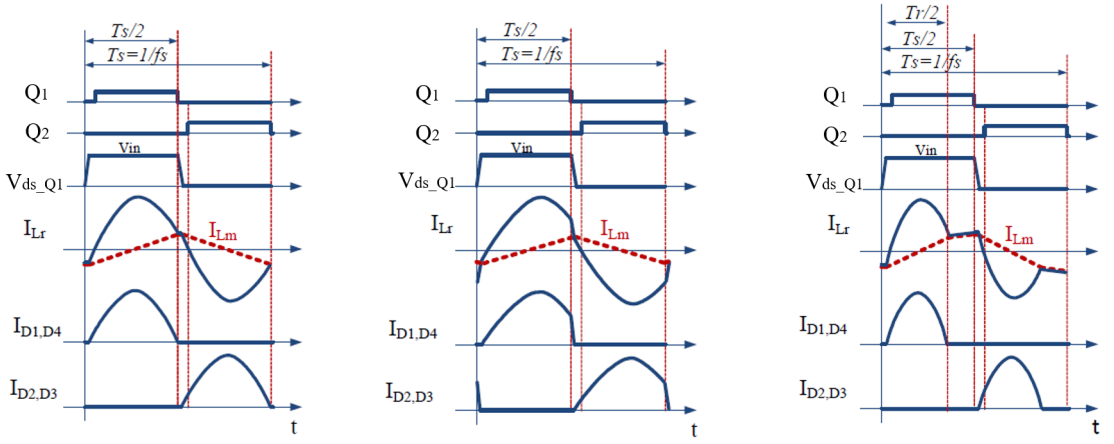
Fig. 2-3b shows the converter operation above the resonant frequency. Although similar to the operation at resonant frequency, half of the cycle is not totally completed. The load current reaches zero after the switching period, which accounts for the lack of ZVS for the output diode bridge.

Finally, at operation below the resonant frequency, current I_{L_r} reaches I_{L_m} before the end of the first half-cycle. As a result, the load current is equal to zero before the switching period, and the output diode bridge can turn off naturally. This behaviour can be observed in Fig.2-3c.

2.1.1 Bridge and Rectifier Selection

There are two bridge switching circuits that are suitable for this application, both of which influence the value of the losses: full bridge configuration and half bridge configuration. While it is true that a half bridge configuration has twice the current of a full bridge configuration, the number of FETs required is half [6].

In the case of the rectifier, the designer can choose to use either a full bridge rectifier or a full wave rectifier with a center tapped transformer. The full bridge



(a) Operation at resonant frequency.

(b) Operation above the resonant frequency.

(c) Operation below the resonant frequency.

Figure 2-3: Modes of operation of LLC converter at different frequencies [6].

rectifier uses 4 diodes, while the full wave uses just two. Because the full-wave rectifier needs a center tapped transformer, it will have two secondary windings, thus the resistance is doubled and as a result the copper losses of the full-wave are double than the losses of the full bridge rectifier. In addition to this, the diodes from the full-wave configuration require double voltage rating compared to the full-bridge configuration.

2.1.2 Design Procedure

Power losses of the LLC resonant converter are related to the design of the resonant tank mainly. Efficiency oriented optimal design is based on the relationships between L-C parameters and power losses. However, the operation modes of resonant converters depend on switching frequency and load conditions. It is hard to estimate the conduction, switching and magnetic losses precisely and simply. To derive an analytic expression of the losses, consumption of each component must be considered and the circuit must analyzed.

The main objectives of the given design procedure are determining the appropriate values for the transformer turn ratio and its magnetizing inductance, the resonant inductance and capacitance values, and a minimum switching frequency variation

range to reduce the components voltage and current stresses and to make the converter volume and cost as reduced as possible. It should be noted that minimum switching frequency variation range is desired for output voltage regulation against the other parameters changes. Having an broad frequency range to control can be treated as a disadvantage because of increase of the driving and magnetic losses, thus the objective of achieving maximum efficiency at a predetermined load value is hindered. Moreover, it could create interferences with the other parts of the converter [7].

The first step in the design should be to establish the electrical specifications of the converter, such as the minimum, maximum, nominal input voltage, output voltage and current and rated output power.

Choosing the switching frequency of the DC/DC converter is one important step in the design procedure and needs to be carefully determined by the designer. Depending on each application, one value of the switching frequency could be more suitable than the other. As a rule of thumb, the lower the frequency, the more voluminous the converter will be, and the conduction losses become more prominent in the circuit. On the other case, if the frequency is too high, other losses could increase, such as magnetic core losses. Moreover, the availability of the components which withstand high frequencies could be low. However, operating at high frequencies is advantageous for LLC converters, due to their decreased switching losses [5].

Converters are usually non-linear and time-variant structures and the LLC topology is not an exception to that. By using the first harmonic approximation (FHA) the model becomes linear and time-invariant as illustrated in Fig. 2-4.

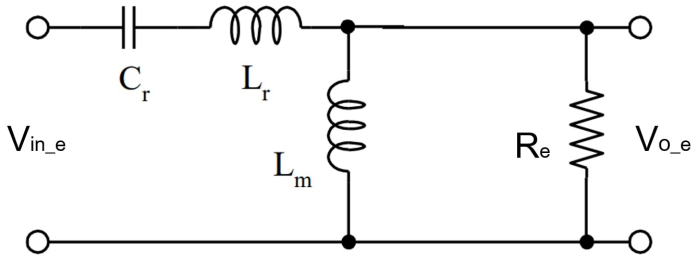


Figure 2-4: FHA equivalent circuit [4].

V_{in_e} represents the fundamental component of V_{in} and V_{o_e} is the fundamental

component of V_O. The input voltage source for this circuit is sinusoidal, and drives an equivalent resistor, R_e, which can be calculated in the following way [5]:

$$R_e = \frac{8 \cdot n^2}{\pi^2} \cdot R_O \tag{2.3}$$

Some important parameters need to be defined, such as the ratio between the two inductances.

$$L_n = \frac{L_m}{L_r} \tag{2.4}$$

When choosing this value, a trade-off has to be done. When L_n is high, the magnetizing inductance becomes high, while the magnetizing currents are low. The frequency range is also spread over a big interval and the efficiency increases. On the other hand, when L_n is small, the regulation is more flexible, the frequency spectrum is reduced, and the efficiency is lower.

The transfer function that makes the connection between the input and output voltage is called voltage gain, M_g.

$$M_g = \frac{n \cdot V_O}{V_{in}/2} \tag{2.5}$$

n is the transformers turns ratio, $n = N_p/N_s$, where N_p and N_s are the number of turns at the primary and secondary sides of the transformer, respectively. f_n is the normalized frequency and is dimensionless, whereas f_{sw} represents the switching frequency of the converter, and f_r is the resonant frequency of the resonant tank.

$$f_n = \frac{f_{sw}}{f_r} \tag{2.6}$$

Moreover, the quality factor of the resonant circuit can be defined as:

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_e} \tag{2.7}$$

Using equations 2.4, 2.6 and 2.7, the gain function can be normalized and written as such [5]:

$$M_g = \left| \frac{L_n \cdot f_n^2}{[(L_n + 1) \cdot f_n^2 - 1] + j[(f_n^2 - 1) \cdot f_n \cdot Q_e \cdot L_n]} \right| \tag{2.8}$$

The starting point for selecting the turns ratio is initially setting M_g at unity (M_g=1). This ensures that the the output voltage is at the middle between minimum output voltage, V_{O_min} and maximum output voltage, V_{O_max}. This value can be called V_{O_nom}.

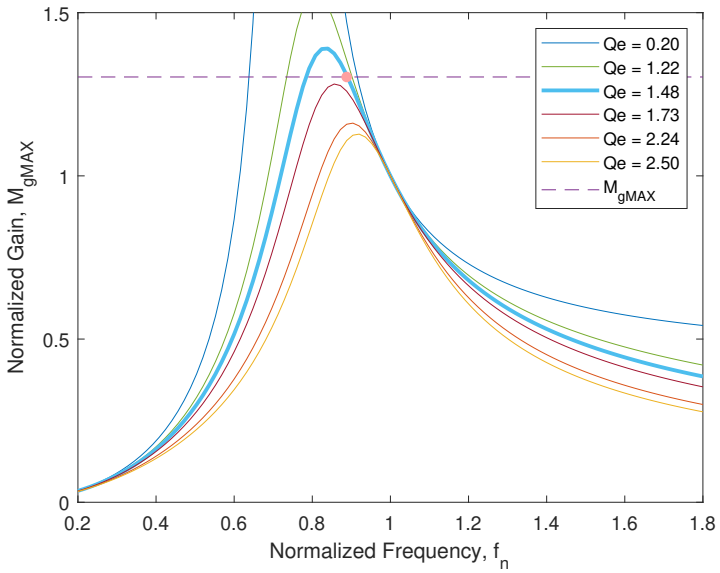


Figure 2-5: Voltage Gain vs. Normalized Frequency for Varying Quality Factor.

Normally, the converter's application purpose is to deliver a fixed output voltage under a range of input voltage and load current [8]. Voltage V_{O_max} from Figure 2-5 is achieved by carrying out the line regulation of the circuit. That is, the maximum output voltage possible to obtain from a variation of the input voltage, at a certain output current. [5]

Based on equation (2.5), the transformer turns ratio can be calculated as follows, taking into account that M_g=1:

$$n = M_g \cdot \frac{V_{in}/2}{V_O} \tag{2.9}$$

Choosing the quality factor, Q_e and ratio between L_m and L_r can be a challenging task and can take a few trial and error efforts.

By fixing the value of L_n, Figure 2-5 can be plotted for various values of Q_e. Choosing the appropriate curve of operation is called load regulation: the variation of the output voltage caused by the variation of the load current, from light load to full load [5]. The curve associated with $Q_e = 0.2$ corresponds to low-load condition, while the curve associated with $Q_e = 2.5$ corresponds to the full-load condition. The intersection between M_{gMAX} and the peak of the curve that comes just above the M_{gMAX} line is the maximum quality factor that yields an appropriate gain curve. Going further on the same curve could mean operating in the capacitive region, operation which should be avoided. For a better understanding, in the case of Fig. 2-5, the appropriate value of Q_e is 1.48. Since Q_e is associated with the load current, it can be noted that if the load is increased more, then the curve would go toward the one corresponding to $Q_e = 1.73$, which would not cross over with M_{gMAX} line, thus making it inadmissible.

The last step in the design of the converter is to calculate the value of the reactive components, using equations (2.7), (2.1) and (2.4):

$$C_r = \frac{1}{2\pi f_{sw} R_e Q_e} \tag{2.10}$$

$$L_r = \frac{1}{(2\pi f_{sw})^2 C_r} \tag{2.11}$$

$$L_m = L_n \cdot L_r \tag{2.12}$$

Finally, the selection of the output filter values is very straightforward.

$$C_f \geq \frac{I_O}{8 \cdot f_{sw} \cdot V_O \cdot \frac{\Delta V_O}{100}} \tag{2.13}$$

$$L_f \geq \frac{\Delta V_O \cdot V_O}{\Delta I_O \cdot I_O \cdot 4 \cdot \pi \cdot f_{sw}} \tag{2.14}$$

where ΔV_O represents the battery voltage ripple, and ΔI_O is the battery current ripple, both measured in percentages.

2.2 GaN Technology Overview

For many decades, silicon has been the base material for transistors. It is still widely used because of two main reasons: first, silicon has the property of being a semiconductor, while the second reason would be that it is an abundant element in the world which makes it very affordable and appealing for producers. However, it is not the only element used in the manufacturing of switching devices. One of its successors is another semiconductor material, gallium nitride. One utilization that is very interesting from the point of view of power application is the gallium nitride high electron mobility transistor, or GaN HEMT, which is one of the switching devices produced with this semiconductor material. Right now, GaN HEMT transistors are the direct competitors of the silicon carbide, SiC, wide-band gap transistors.

If the comparison is made between Si and SiC MOSFETs, then SiC have a higher switching speed. Furthermore, GaN switching devices have a significantly faster switching speed even than SiC. They are suited for applications that require very fast switching frequencies and can support higher voltages while also withstanding operation at higher temperatures. Many of these advantages come from the fact it is a wide band semiconductor.

By observing the energy level diagram of a semiconductor, it is clear that there exists a difference in energy between the valence band and the conduction band, otherwise called band gap. It can be interpreted as the amount of energy an electron needs to jump from the valence band to the conduction band. Generally, wide-band semiconductors have a band gap of over 3 eV.

By comparison, Si has a band gap of 1.12 eV, while SiC (silicon carbide) and GaN have a band gap of 3.26 eV, respectively of 3.39 eV [9].

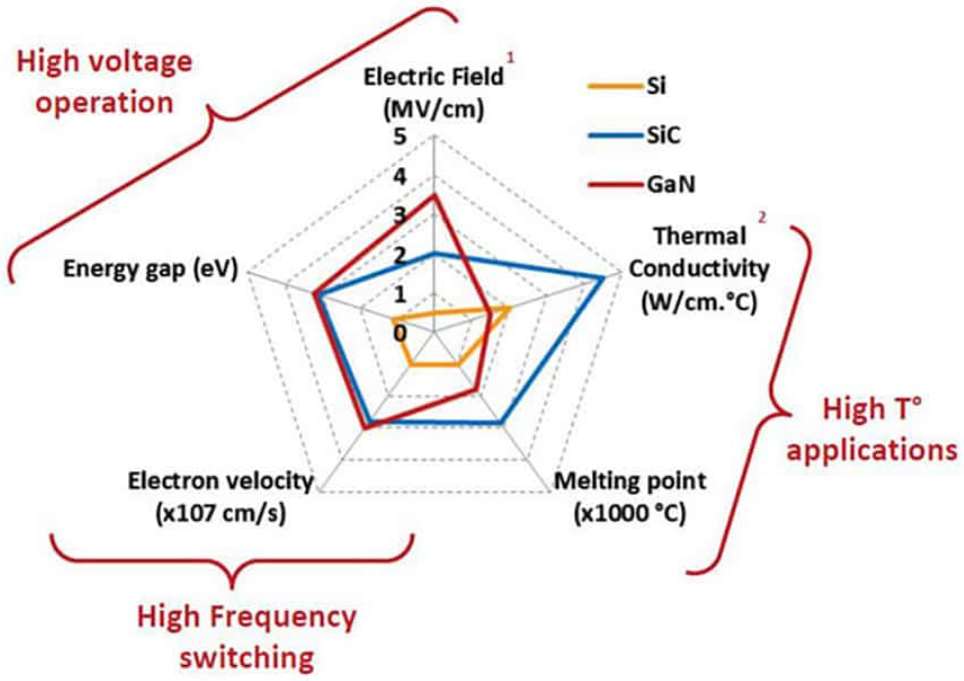


Figure 2-6: Key characteristics of Silicon, Silicon Carbide and Gallium Nitride [10].

Figure 2-6 shows very clearly the differences between the three semiconductor materials. First of all, it is clear that Si devices are running behind in terms of capabilities. While SiC is preferred for high temperature applications, GaN switching devices are more suitable for high voltage operations or where a high switching frequency is needed [10].

Even though GaN is still young in its life cycle and as a result the technology is not yet as mature as silicon, it's worth observing it's evolution in time. Surely it will undergo many improvements in the years to come and will become a powerful competitor to silicon.

2.2.1 Basic GaN structure

Just like their silicon counterparts, GaN transistors have the same nomenclature: gain, drain and source as seen in Figure 2-7, with the mention that there is no body diode. They are naturally capable of reverse conduction and as a consequence, their

reverse recovery charge is zero, something that will be discussed more in detail later in this chapter. Also their important parameters are on-resistance and breakdown voltage.

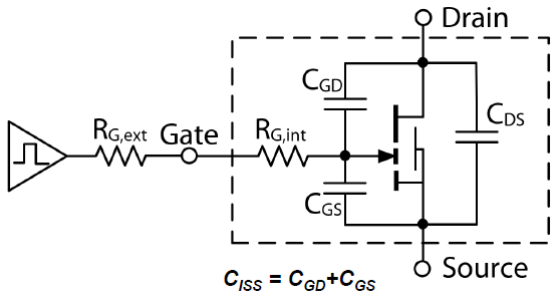


Figure 2-7: Real model of GaN transistor including intrinsic and external parasitic components [11].

There are two types of GaN devices:

- Depletion mode type, otherwise known as d-mode HEMT, where the state of the transistor is normally on and it requires a negative voltage in order to be turned off. This type was the first to be developed, but it was not attractive to designers. In order not to have a short circuit, at start-up, a negative bias must be applied to make sure that the transistor is turned off.

- Enhancement mode type, otherwise knows as e-mode HEMT, where the transistor is normally off and turns on when it has a positive gate voltage applied, just like the Si MOSFET technology. This document will focus more on this type as it is the one later used for the development of the LLC resonant converter circuit.

One similarity with Si MOSFETs regarding the working principle is that it is voltage driven, meaning that the driver charges and discharges C_{ISS}, otherwise known as the input capacitance which is the sum between gate-drain capacitance, C_{GD} and gate-source capacitance, C_{GS}. Moreover, the slew rate can be easily controlled by R_G, gate resistor.

In contrast with Si MOSFETs, GaN technology has a much lower gate charge which significantly lowers the power losses and allows for a faster switching. The

typical gate bias level is around -3 V or 0 V for turn off and between +5 to 6 V for turn on, whereas for a Si MOSFET the gate bias to turn on is much higher, around +10 to 12 V. Furthermore the typical threshold voltage is 1.5 V, which is lower than its Si counterpart.

Gate Bias Level	GaN Sys.	Si MOSFET	SiC MOSFET	IGBT
Maximum rating	-20/+10V	-/+20V	-/+20V	-8/+20V
Typ. gate bias val.	0 or -3/+5-6V	0/10-12V	0 or -9/+15V	-4/+15-20V

Table 2.1: Gate Bias Level for different transistors [9].

2.2.2 Reverse conduction

Although these devices do not have a body diode, it is not necessary to add an external anti-parallel diode in order to obtain a reverse conduction state when V_{GS} is off. This can be attained thanks to their internal structure.

Without going too much into detail with the chemical structure, within a GaN E-HEMT there is a lateral two-dimensional electron gas called 2DEG which forms a channel between a layer of GaN and AlGaN. This gas has very high charge density and mobility. By implanting fluorine atoms in the AlGaN layer, it is possible to trap negative charges in the same layer depleting the 2DEG. By adding a Schottky gate on top, an enhancement mode type transistor is formed.

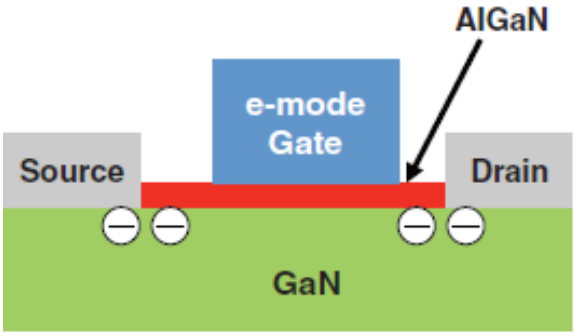


Figure 2-8: Structure of an e-mode GaN HEMT [9].

When the switching device is conducting forward, it behaves like a typical MOSFET, only with better performance. However, when the gate signal is off, it starts to

behave differently. The gas, 2DEG, starts to operate as a diode.

Cutting out the body diode has its advantages and disadvantages. First of all, there are no minority carriers involved in the conduction process in an e-mode GaN HEMT. For this reason, the reverse recovery charge Q_{RR} is reduced to zero, making GaN switching devices suitable for half-bridge applications with hard switching. No longer will the switching losses account for the losses of the diode reverse recovery. Moreover, the absence of the body diode, means less EMI problems because of the lack of noise produced by the diode when it turns on. As a result, circuits can become even more compact and power conversion and signal processing could be included in the same PCB.

On the other hand, the main disadvantage of not having a body diode is having a higher reverse voltage drop than most MOSFETs. This could lead to higher losses in the dead-time of a typical half-bridge circuit. Fortunately, this can be fixed by reducing the dead time.

2.2.3 Capacitance and Charge

One big factor in the process of assessing the switching losses of the transistor is knowing the capacitances. In a FET there are three main capacitances that should be acknowledged: gate-to-source capacitance (C_{GS}), gate-to-drain capacitance (C_{GD}) and drain-to-source capacitance (C_{DS}). All of these can be observed in Fig. 2-7. In practical applications, the designer should look at the total capacitance seen at the input terminals, represented by equation (2.15), at the output terminals, defined by equation (2.16), respectively at the at the reverse transfer capacitance which is equal to C_{GD}. All three of them influence greatly the switching performance of the FET.

$$C_{ISS} = C_{GD} + C_{GS} \tag{2.15}$$

$$C_{OSS} = C_{GD} + C_{DS} \tag{2.16}$$

Knowing this parameters, the amount of charge (Q) could be determined by integrating the capacitance between two terminals across the voltage applied to the same terminals. It is useful to know how much charge should be applied in order to achieve a change in the voltage. At the same time, the integration of current over time equals charge, which thus making the usage of charge very intuitive [9].

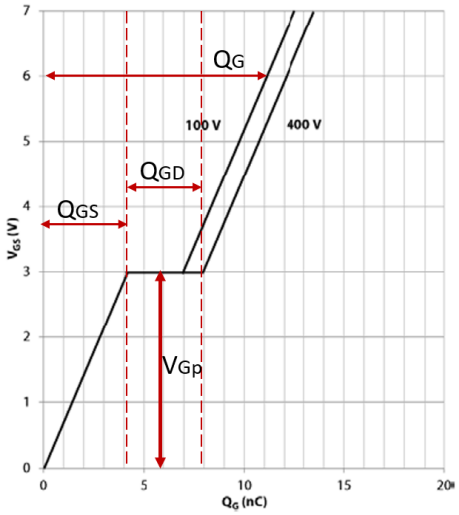


Figure 2-9: GS66516T Gate Charge, Q_G Characteristic @ V_{DS} = 100, 400 V [1].

For example, Fig. 2-9 shows the amount of gate charge Q_G that is needed in order to achieve the wanted gate-source voltage. Here, Q_G represents the integrated value of the C_{ISS} capacitance. For a V_{DS} of 400 V, around 11 nC are needed to reach a V_{GS} of 6V, to ensure a fully turned on transistor. If the gate drive can supply 1 A, then it will take 10 ns to reach that voltage.

Another perspective over Fig.2-9 would be to define Q_{GS} from the origin to the plateau voltage, V_{Gp}. When V_{GS} starts to increase, capacitances C_{GS} and C_{GD} start to charge as well, while C_{DS} stays relatively constant. However, because C_{GS} is larger than C_{GD}, the gate charge is assumed to be equal to the gate-source charge. Throughout the Miller plateau, the gate-drain charge is defined, Q_{GD}. This is true if the slope of the voltage is zero. If the slope is different from zero, then some current might charge C_{GS}. Once the Miller plateau ends, C_{GD} becomes constant again. Finally, Q_G is defined as the charge from the origin to the value of the voltage that keeps the transistor fully on [12].

Parameter	Sym.	Typ.	Units	Test Conditions
Input Capacitance	C_{iss}	520	pF	$V_{DS} = 400V$
Output Capacitance	C_{oss}	130	pF	$V_{GS} = 0$
Reverse Transfer Capacitance	C_{rss}	4	pF	f=1 MHz
Total Gate Charge	Q_G	12.1	nC	V_{GS}=0 to 6, V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}	4.4	nC	
Gate-to-Drain Charge	Q_{GD}	3.4	nC	
Output Charge	Q_{OSS}	113	nC	V_{GS} = 0 V, V_{DS} = 400 V
Reverse Recovery Charge	Q_{RR}	0	nC	

Table 2.2: Data from GS66516T datasheet showing the section relating to capacitance and charge [1].

The capacitances and charges for GaN Systems GS66516T 650 V E-mode transistor are shown in Table 2.2.

2.3 Magnetic Components Overview

The LLC resonant circuit is composed of three magnetic components: the magnetizing inductance, L_m, the series inductance, L_r, and the output filter inductance, L_f. They transform electrical energy into magnetic energy in an intermediate stage of the power converter and store it until it is needed later. Designing the magnetic components can affect in a great measure the performance of the converter and the size, so a great deal of attention should be paid to them. It is very rare that the design of the converter uses off-the-shelf magnetic components that meet all the requirements of the project. For this reason, it is advised to design them, even though the process might be lengthy and iterative.

The primary-side and secondary-side currents of the converter, such as the load current, the magnetizing current and the total load current referred from the primary-side to the secondary side can be determined in the stage of the design of the LLC topology. By knowing the current that flows through a magnetic component, the frequency and the value of the inductances, the objective is to design and construct the reactive components by minimizing physical size and losses. The parameters that need to be established are, among others: the core material, the core size, the airgap

length, the numbers of turns, the diameter of the wire and the number of wires per turn.

2.3.1 Types of Losses

There are two types of losses that need to be taken into account when estimating and optimizing a power inductor of a converter. The first one refers to core losses. They are divided into three categories: hysteresis losses, eddy current losses and ferriresonance losses. The hysteresis losses can be modeled by the the Steinmetz equation [13], outlined below:

$$P_{HYST} = K_C \cdot f^{\alpha} \cdot \hat{B}^{\beta} \tag{2.17}$$

where f is the operating frequency (Hz), $\hat{B}$ is the peak magnetic flux density in (T), and α, β and K_C are Steinmetz coefficients. As it can be observed, the losses are greatly influenced by the switching frequency.

Eddy losses are due to the induced current loops in the dipoles of the material. They can be modeled with the following formula:

$$P_{EDDY} = C_b \cdot f^2 \cdot \hat{B}^2 \cdot \frac{A_e}{\rho_{NU}} \tag{2.18}$$

where A_e is the effective cross-sectional area of the core (m^2) and ρ_{NU} is the resistivity of the material ($\Omega \cdot m$).

However, in the development of this application, the empirical formula for determining the total copper losses will be used:

$$P_{CORE} = c \cdot f^x \cdot {B_{ac|HF}}^y \cdot V_e \tag{2.19}$$

where c, x, y are Steinmetz coefficients, $B_{ac|HF}$ is the AC magnetic flux density

in Teslas and can be calculated with equation (2.20).

$$B_{ac|HF} = \frac{L \cdot I_{ac|HF}}{A_e \cdot N} \tag{2.20}$$

At the same time, the designer has to take into account that the maximum magnetic flux density should not be above the saturation value of the material.

The second factor refers to the copper losses. Those are the losses produced by the flowing current through the windings and they dissipate in the form of heat. The major causes of copper losses are DC and AC losses. The DC losses are due to the DC resistance of the wire, while the AC losses are generated by skin and proximity effects in the winding conductors. Under high frequency conditions AC copper losses increase [14].

2.3.2 Choice of Magnetic Material and Core Size

Because it is an iterative process, as said in the previous paragraphs, the designer should make a good initial guess in order to arrive to an optimum result.

The material and the size of the core should be chosen accordingly to the requirements of the circuits. There are many different materials to choose from, such as silicon steel, iron powder, or ferrites, each with their properties.

Specifically for the requirements of this application, ferrites are the most recommendable. This material has high magnetic permeability and high resistivity. Moreover, it has reduced Eddy currents in comparison to the other materials and is suitable for high-frequency applications. They are composed out of metal combinations between manganese and zinc (MnZn), and nickel and zinc (NiZn) [15].

When it comes to the choice of the size of the core, as in the case of the material, there are different types: E, I, ETD, EFD, EC, to name a few. According to the power range of the application and the switching frequency, the designer can choose the appropriate type and size.

Chapter 3

Design and Implemetation

3.1 Charger Specifications

The design of the whole circuit starts from knowing the parameters of the battery that the Wolfast MotoStudent Team is going to use in the construction of their motorcycle prototype. A charger with a maximum output power of 5.2 kW is needed and by studying the commercial alternatives, there are not many options for such a charger. For more information about the battery, all of its key parameters can be seen in Table 3.1.

Symbol	Quantity	Value
V_{DC}	Input Voltage	600 V_{dc}
VB_{min}	Minimum Battery Voltage	52.5 V_{dc}
VB_{nom}	Nominal Battery Voltage	75.6 V_{dc}
VB_{max}	Maximum Battery Voltage	88.2 V_{dc}
I_O	Maximum Output Current	60 A
PB_{max}	Maximum Output Power	5.2 kW
Cap	Battery Capacity	55 Ah (at 1C)

Table 3.1: Key parameters of the battery.

There are many charging curves that can be applied to this battery, however the main charging scheme that will be used is a CCCV (Constant Current, Constant

Voltage) strategy where the battery is charged with a constant current of 55A over the period of time F1. When the battery reaches the threshold voltage of 75.6 V, the voltage becomes constant, while the current decreases exponentially until the battery reaches full charge at F2. This method prevents overcharging and is suitable for Li-ion batteries.

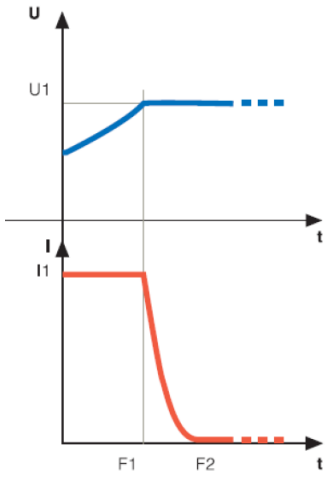


Figure 3-1: Desired charger scheme, U1=75.6V, I1=55.

3.2 Design Steps of the LLC Converter

Symbol	Quantity	Value
f_s	Switching Frequency	150 kHz
P_{nom}	Charger Nominal Power	4.2 kW
V_{DCmin}	Minimum Charger input DC link	590 V_{dc}
V_{DC}	Nominal Charger input DC link	600 V_{dc}
V_{DCmax}	Maximum Charger input DC link	610 V_{dc}
ΔI	Battery Current Ripple	$\leq$ 5.5 A
ΔV	Battery Voltage Ripple	$\leq$ 0.5 V
V_f	Forward voltage of output rectifier diodes	0.875 V

Table 3.2: Key parameters of the designed charger.

As said in the previous chapter, in order to calculate the elements of the resonant circuit, there are some parameters which need to be established at the beginning of

the design. Table 3.2 illustrates the initial parameters that have been used for the charger.

3.2.1 Selection of the switching frequency, f_{sw}

For the initial design, a switching frequency of 150 kHz was chosen. By utilizing a high switching frequency, the size of the magnetic parts is decreased. Moreover, the half bridge configuration of the LLC will contain GaN switching devices which have a maximum switching frequency well over 150 kHz, so they can easily withstand the proposed frequency. Also, for AC-DC applications, usually the upper limit in terms of frequency is 150 kHz. At this frequency, the EMI testing begins, and setting the switching frequency equal or lower than this, helps to pass the test without great difficulties [5].

Following the design procedure from the previous chapter, the components of the resonant tank can be determined. Using equation (2.9) and assuming M_g is equal to 1, the turns ratio of the converter can be calculated.

$$n_{exact} = M_g \times \frac{V_{DC}/2}{VB_{nom} + V_f} = 1 \times \frac{600/2}{75.5 + 0.875} = 3.93 \tag{3.1}$$

Taking into consideration the transformer coupling, TC=0.99, the final turns ratio becomes equal to 3.9.

$$n = \sqrt{TC} \times n_{exact} = \sqrt{0.99} \times 3.3 = 3.9 \tag{3.2}$$

By using equation (2.5), the minimum and maximum gains can be calculated.

$$M_{gMIN} = \frac{n \times (VB_{min} + V_f)}{V_{DCmax}/2} = \frac{3.9 \times (52.5 + 0.875)}{610/2} = 0.68 \tag{3.3}$$

$$M_{gMAX} = \frac{n \times (VB_{max} + V_f)}{V_{DCmin}/2} = \frac{3.9 \times (88.2 + 0.875)}{590/2} = 1.18 \tag{3.4}$$

3.2.2 Selection of L_n and Q_e

The selection of the ratio between L_r and L_m and the selection of the quality factor is very important, and as discussed in the previous chapter, will determine the behaviour of the circuit.

For this circuit, the value of L_n was fixed to 0.8 to achieve both a flexible regulation plus good efficiency. Furthermore, by fixing the value of L_n, Fig. 3-2 was plotted for several values of the quality factor. It should be noted that the value of the maximum gain includes a 10% factor of safety margin.

Choosing a quality factor of Q_e=0.2 up to 1.4, provides a higher boost gain, but at the same time is less sensitive in the region above resonant frequency. On the other hand, choosing a higher value, above 1.8, reaches the minimum gain, but does not reach the maximum. As a result, the moderate value is to choose Q_e=1.6.

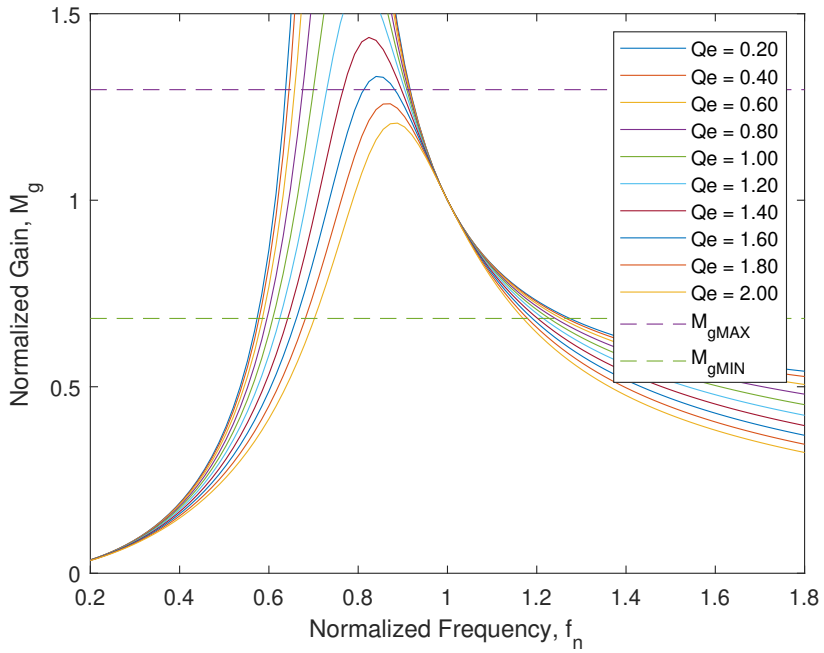


Figure 3-2: Voltage Gain vs. Normalized Frequency for Varying Quality Factor.

Now that the maximum and minimum gains are known, and that L_n and the quality factor, Q_e have also been chosen, the full range of operation of the converter can be determined. As a result, the minimum switching frequency admissible for operation is $f_{swMIN} = 140kHz$, while the maximum frequency is equal to $f_{swMAX} = 180kHz$.

3.2.3 Resonant Tank Parameters Calculation

After setting the previous parameters, the resonant tank parameters can be calculated using equations (2.10), (2.11), (2.12). Equivalent Load Resistance at primary side, R_e is determined in conditions of nominal load.

$$R_{eNOM} = \frac{8 \cdot n^2}{\pi^2} \times \frac{VB_{nom}}{I_O} = \frac{8 \cdot 3.9032^2}{\pi^2} \times \frac{75.7}{55} = 17\Omega \tag{3.5}$$

$$C_r = \frac{1}{2\pi \cdot Q_e \cdot f_{sw} \cdot R_{eNOM}} = \frac{1}{2\pi \cdot 1.48 \cdot 150kHz \cdot 17\Omega} = 41.82nF \tag{3.6}$$

$$L_r = \frac{1}{(2\pi f_{sw})^2 C_r} = \frac{1}{(2\pi 150kHz)^2 \cdot 41.8152nF} = 26.7\mu H \tag{3.7}$$

$$L_m = L_n \cdot L_r = 0.83 \cdot 26.6960\mu H = 22.66\mu H \tag{3.8}$$

3.3 Magnetic Components Design

There are three magnetic components in the circuit, two of which are part of the resonant tank and have already been determined. The current that flows through the series resonant inductance is sinusoidal and is the squared sum of the primary-side RMS load current and the RMS mangetizing inductance current.

$$I_{oe} = \frac{I_O \cdot 1.1 \cdot \pi}{2 \cdot \sqrt{2} \cdot n} = \frac{55 \cdot 1.1 \cdot \pi}{2 \cdot \sqrt{2} \cdot 3.9} = 17.2A; \tag{3.9}$$

$$I_m = \frac{2 \cdot \sqrt{2}}{\pi} \times \frac{n \cdot VB_{nom}}{2 \cdot \pi \cdot f_{sw} \cdot L_m} = \frac{2 \cdot \sqrt{2}}{\pi} \times \frac{3.9 \cdot 75.6}{2 \cdot \pi \cdot 150kHz \cdot 22.6625\mu H} = 12.44A; \tag{3.10}$$

$$I_r = \sqrt{I_m^2 + I_{oe}^2} = 21.24A \tag{3.11}$$

For the calculation of the primary-side current, a 10% over current was assumed in equation (3.9), and the magnetizing current is calculated at the resonant switching frequency.

The third magnetic component is filter inductance, L_f, situated after the full-bridge rectifier. It's value and the current flowing through it can be calculated using equations (3.12) and (3.13).

$$L_f = \frac{VB_{nom} \cdot \Delta V}{I_O \cdot 4 \cdot pi \cdot f_{sw}} = 0.7292\mu H; \tag{3.12}$$

$$I_{oes} = n * I_{oe} = 67.2A; \tag{3.13}$$

Now that the current waveforms and their values are known, each inductance will be designed one by one, starting with the series resonant inductor, L_r. The inductors of the circuit will be designed using the Equivalent Toroid Method. This method considers the magnetic circuit as a toroid with an equivalent length, l_e, and an equivalent area, A_e.

The first step is to choose one suitable core size and a material from the available ones. In this case, the available cores are from the ETD range. Taking into account the frequency and the magnitude of the current flowing through L_r, the core size chosen is ETD59 and the chosen ferrite material is 3C81. The physical properties of the available cores and the Steinmetz coefficients of the available materials are illustrated in Tables A.1 and A.2 from Appendix A.

For the initialization, the core and copper losses are assumed to be equal. Their

summation is also assumed to be 1% out of the total power output of the converter.

$$\frac{P_{CORE} + P_{CU}}{P_{CONVERTER}} = 1\% \tag{3.14}$$

Therefore, for nominal conditions and under the previously made assumptions, the losses are equal to 20.8 W. The core losses are a function of the AC component of the magnetic density. By calculating the specific power loss as the ratio between the core losses and the core volume, $P_v = \frac{P_{CORE}}{V_e}$, $\widehat{B}$ can be determined by looking at Figure 3-3.

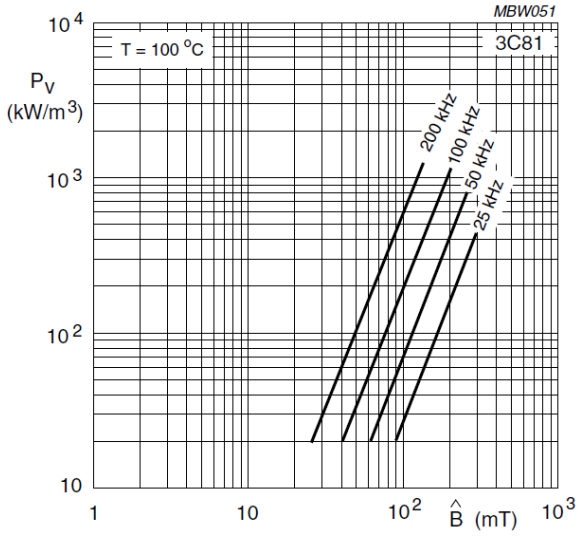


Figure 3-3: Specific power loss as a function of peak flux density with frequency as a parameter for material 3C81 [16].

In this case, $P_v = 403.69 kW/m^3$, and at a switching frequency of 150 kHz, $\widehat{B}$ is equal to approximately 110 mT. If the core ETD59 is transposed into an equivalent toroid, then the reluctance is equal to the ratio between the magnetomotive force and the flux. Moreover, because the magnetic circuit of the toroid is uniform, the equivalent reluctance can be defined as the sum of the reluctance of the airgap and the reluctance of the core, as in equation (3.15).

$$\mathfrak{R}_{eq} = \mathfrak{R}_{ag} + \mathfrak{R}_c = \frac{g}{\mu_0 \cdot A_e} + \frac{l_e}{\mu \cdot A_e} \tag{3.15}$$

Furthermore, according to Faraday's Law illustrated in equation (3.16) and Ampere's Law from equation (3.17), the magnetic flux is the energy stored in a volume, while the magnetomotive force is the amount of current multiplied by the number of turns in the magnetic circuit.

$$\phi = B \cdot A \tag{3.16}$$

$$mmf = \mathfrak{R} \cdot \phi = N \cdot i \tag{3.17}$$

Inductance, as well, can be defined as the ratio of the magnetic flux over the current in the circuit. Combining all of this information, a different formula for the inductance is derived that contains both the number of turns and the airgap as variables, as seen in equation (3.18).

$$L = \frac{\mu_0 \cdot A_e \cdot N^2}{\frac{l_e}{\mu_r} + g} \tag{3.18}$$

Finally, the formula for calculating the number of turns and for calculating the airgap is determined by further substituting the above formulas. Equations (3.19) and (3.20) are calculated for the case of the series resonant inductor, L_r.

$$N = \frac{L \cdot \widehat{i}}{A_e \cdot \widehat{B}} = \frac{26.696\mu H \cdot 21.24 \cdot \sqrt{2}}{3.68 \cdot 10^{-4} \cdot 110mT} = 20 \tag{3.19}$$

$$g = \frac{N \cdot \mu_0 \cdot \widehat{i}}{\widehat{B}} - \frac{l_e}{\mu_r} = \frac{20 \cdot 4\pi \cdot 10^{-7} \cdot 21.24 \cdot \sqrt{2}}{110mT} - \frac{139 \cdot 10^{-3}}{4000} = 6.83mm \tag{3.20}$$

With this, the design of the physical properties of the series inductor is almost complete. The only thing that is left to determine is the diameter of the conductor. To find out the optimum value in this design, the variation of the AC, or high frequency, power losses should be checked against different diameters. It is worth noting that the wire diameter has discrete values, ranging from 0.05 mm to 1 mm in steps of 0.05 mm.

Higher diameters are not practical and need to be implemented with several wires per turn. Due to the symmetry of the core geometry and to simplify the calculations, the round profile of the conductor is transformed into a square wire profile of the same area. This method allows calculating the winding dimensions, without changing the copper area.

$$h = D\sqrt{\frac{\pi}{4}}; \tag{3.21}$$

The maximum number of turns per layer is determined by multiplying the effective width of the window with the linear window factor and then divided by the equivalent area of the conductor, as illustrated in equation (3.22).

$$N_{tl} = \frac{w_e \cdot Lwf}{h} \tag{3.22}$$

Some more attention should be given to the linear window factor, Lwf. Unlike the DC, also called low frequency losses, the AC losses take into account the skin and proximity effects, which greatly influence the power loss. The skin depth, δ_{SKIN}, represents the distance from the surface of the conductor to where the current density increases with 1/e times the density from the surface, where e is the natural log base. In certain conditions, at a temperature of 100° and μ=μ_0, the skin depth can be approximated to equation (3.23) [17].

$$\delta_{SKIN} = \frac{7.5}{\sqrt{f_{sw}}} \tag{3.23}$$

Knowing the skin depth according to the frequency, the diameter of the wire should not be higher than twice the skin depth. One solution is to use litz-wire for the winding. They reduce the copper losses by using multiple small diameter wires so that each of them fulfills the skin-depth condition.

$$Lwfs = 1 - \frac{1 - Lwf_0}{1 + e^{(-a \cdot D - b)}}; \tag{3.24}$$

The final linear window factor, Lwf, is the multiplication of the calculated $Lwfs$

and Lwf_0, where Lwf_0 is the initial linear window factor which is 0.7. As seen in equation (3.24), $Lwfs$ depends on some other factors, such as a and b. They depend on the diameter of the wire, which as stated earlier, cannot be higher than twice the skin depth.

Figure 3-4 is the result of computing multiple iterations at the resonant frequency of 150 kHz, where the diameter takes values between 0.05 to 1.1 mm. It is a sigmoid curve that represents the different values of the linear window factor at different diameters and varying frequencies. For diameters up to 0.3 mm, Lwf is equal to 0.7 and no litz wire is required, because there is no skin effect present. However, for diameters of 0.3 mm and higher, because the curve is dependent of frequency, and the "corner" of the sigmoid corresponds to twice the skin depth, it is necessary the use of litz wire. At higher frequencies Lwf is equal to 0.56.

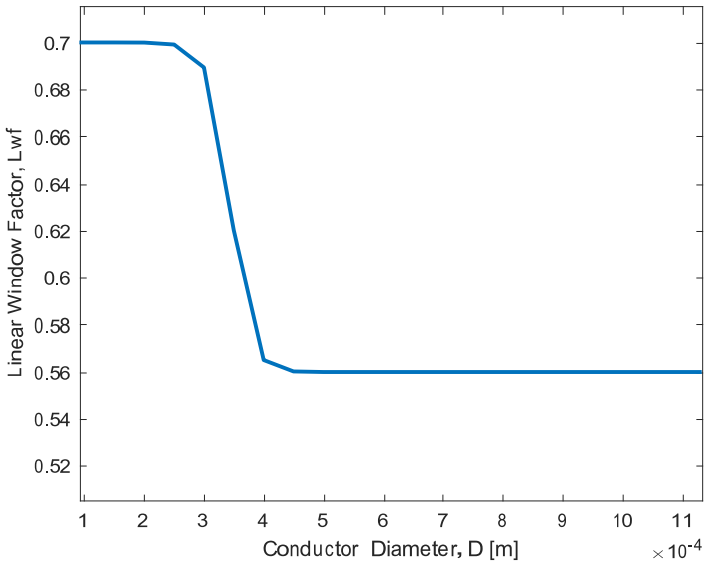


Figure 3-4: Sigmoid curve showing the dependency of the linear window factor to the frequency and wire diameter.

Now, by knowing how many turns it takes to complete a layer, the number of layers can be calculated, by dividing the actual number of turns obtained in equation (3.19) to the maximum turns per layer. The ratio of the total winding width to the

window width, also known as η, is calculated in equation (3.26).

$$m = \frac{N}{N_{tl}} \tag{3.25}$$

$$\eta = \frac{h \cdot N_{tl}}{w_e} \tag{3.26}$$

Finally, the formula used to calculate the Dowell resistance is illustrated in equation (3.27). Generally, Dowell resistance is used for the calculation of the low frequency losses, but also the corresponding AC values can be obtained by multiplication of appropriate factors, as shown in equation (3.28) [14].

$$R_{DC_{Dowell}} = \frac{m \cdot \rho_{Cu} \cdot L_{turn} \cdot N_{tl}^2}{\eta \cdot w_e \cdot h} \tag{3.27}$$

$$R_{AC} = R_{DC_{Dowell}} \cdot (real(M_{coef}) + \frac{(m^2 - 1) \cdot real(D_{coef})}{3}) \tag{3.28}$$

where M_{coef} and D_{coef} are expressed as follows:

$$M_{coef} = \alpha \cdot h \cdot coth(\alpha \cdot h) \tag{3.29}$$

$$D_{coef} = 2 \cdot \alpha \cdot h \cdot tanh(2 \cdot \alpha \cdot h) \tag{3.30}$$

where α can be written as:

$$\alpha = \sqrt{\frac{2\pi \cdot f_{sw} \cdot j \cdot \mu_0 \cdot \eta}{\rho_{Cu}}}; \tag{3.31}$$

As stated earlier, the diameter of the conductor could take values from 0.05 to 10 mm in steps of 0.05 mm. The process of choosing the optimal diameter is iterative and for each value of the diameter, the AC losses are calculated. To calculate the losses, simply multiply the high frequency RMS current flowing through the inductor with

the AC resistance. The variation of these losses with the diameter of the resonant inductor is shown in Figure 3-5.

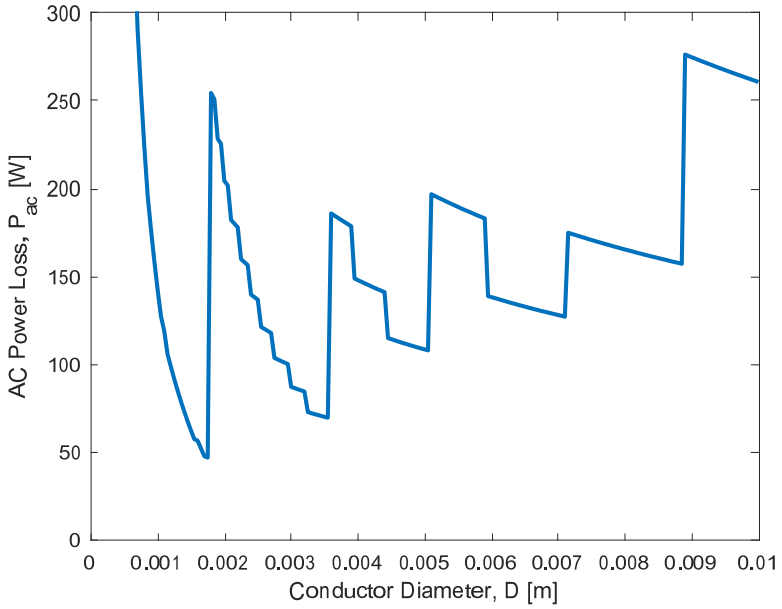


Figure 3-5: Variation of AC power losses with the diameter calculated for the series resonant inductor.

Each saw-tooth from Figure 3-5 represents a complete layer wounded on the core. As the number of layers increases, the losses increase as well. Therefore, the lowest HF losses are registered when wounding one layer with a conductor diameter of approximately 1.75 mm. By using this configuration, the losses of the resonant inductor are equal to 46.28 W. The variation of AC losses with the diameter for the other two magnetic components can be seen in Fig. B-4, in Annex B.

The same method was applied to the magnetizing inductor and filter inductance in order to find out their physical properties and calculate the losses. Without repeating the algorithm two more times, Table 3.3 summarizes all the required parameters.

The magnetizing inductance uses the ETD54 core type in this initial design, and material 3C90. The diameter of the conductor used for the magnetizing inductance is almost double than the diameter of the series inductance, L_r. From the calculations result 10 turns and an airgap of 1.44 mm. The filter inductance withstands a DC current, so a ETD34 core should be sufficient. The diameter of the conductor however

	Value $[\mu H]$	**Core Material**	**Core Type**	**Diameter of conductor [mm]**	**Turns**	**Airgap [mm]**
L_r	26.7	3C81	ETD59	1.75	20	6.83
L_m	22.66	3C90	ETD54	3.15	10	1.44
L_f	0.7292	3C95	ETD34	6.2	3	1.31

Table 3.3: Data for designing the inductances of the resonant converter.

is the biggest and requires only 3 turns. With this, the design of the magnetic components is complete, even though from the point of view of the losses it might not be the optimal design. More information about the optimization process and the chosen approach will be discussed in Chapter 5.

Chapter 4

Simulation Results

4.1 LTSpice Simulation

Everything that was designed in the previous chapter needs to be tested to verify that the output corresponds to the requirements of the charger. The full circuit is illustrated in Figure 4-1. It contains the driver of the two switches, the model of

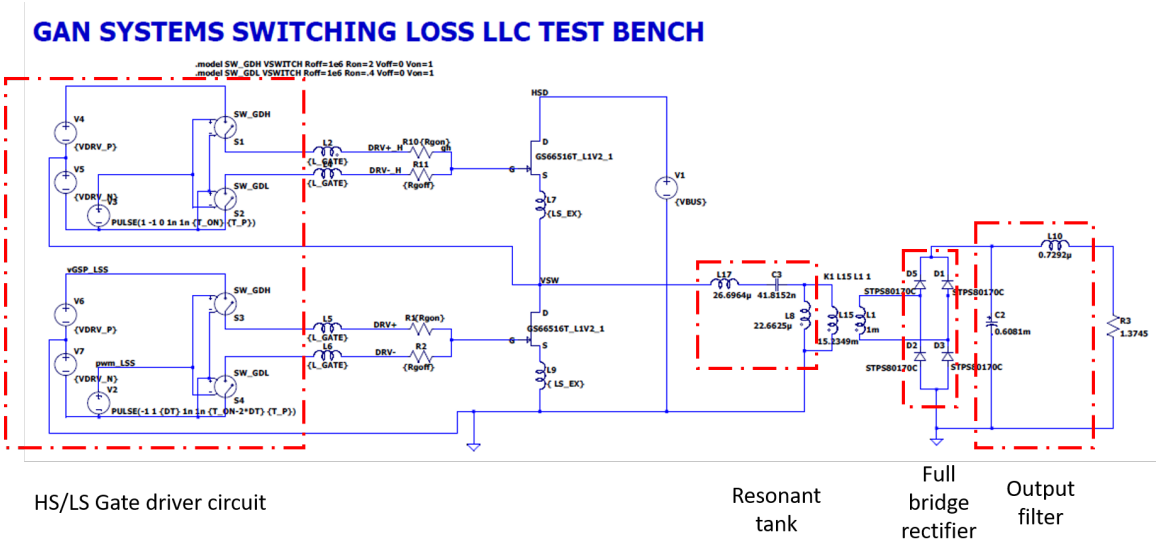


Figure 4-1: Schematic circuit of the resonant charger in LTSpice.

GaN GS66516T switching device, the DC-link voltage, the resonant tank, full bridge

rectifier, the output filter and finally the load which is treated as a resistor in this case. For the purpose of this simulation, a complete model of the switch provided by GaN Systems was used. Even though the manufacturer provides three models of GaN transistors, in the present simulation only the level one type was used. This model targets general electrical simulations, with a focus on simulation speed.

Table 4.1 shows the switching test parameters and the parasitic inductances. Most of the parameters are straight forward and easy to understand what they represent. A dead time of 100ns is applied in order to have a big enough interval for ZVS, in addition to following the recommendations of GaN systems documentation. The duty cycle is set to 0.5. To have exact results of the simulation, the parasitic inductances should not be approximated, however without any real measurements, the gate inductance, external source inductance and power loop inductance have default values.

	Parameter	**Symbol**	**Value**
Switching Test Parameters	DC bus voltage	V_{DC}	600 V
	Turn On Gate Resistor	$R_{G(ON)}$	20Ω
	Turn Off Gate Resistor	$R_{G(OFF)}$	4Ω
	Turn On Gate Voltage	$V_{G(ON)}$	6 V
	Turn Off Gate Voltage	$V_{G(OFF)}$	3 V
	Dead Time	DT	100 ns
	Total Period	T_P	6.67μs
	Turn On Period	T_ON	3.33μs
Parasitic Inductances	Gate Inductance	L_{GATE}	2.5 nH
	External Source Inductance	L_{EX}	10 pH
	Power Loop Inductance	L_{DS}	2 nH

Table 4.1: Set up of the simulation parameters.

Maybe one of the most influential choice of variables in terms of performance is the choice of the turn-on gate resistor and turn-off gate resistor. By varying the gate resistors, the speed of GaN HEMT can be easily controlled. Moreover, it is critical to choose the right resistors for good performance and driver stability. It is recommended to choose the ratio $R_{G(ON)}/\ R_{G(OFF)}$ between 5-10 for controlling the Miller effect [18]. If the chosen $R_{G(ON)}$ is too high, then the switching slows down

and the losses increase. Losses can also increase if $R_{G(ON)}$ is too small since the gate could potentially oscillate. For the purpose of this project, $R_{G(ON)}$ was chosen to be 20Ω, and $R_{G(OFF)}$ was chosen to be 4Ω.

As it can be observed from Figure 4-2, when the switching frequency, f_{sw} is equal to the resonant frequency, the output voltage reaches the nominal output voltage with an acceptable error of 3.1%. The average value of the voltage is 73.2 V instead of 75.6 V. The same is applied for the output power. At moment of time 0.03, the switching frequency is increased by 1%, and as a result, the output voltage and power decrease accordingly. In the same figure, the magnetizing current and the resonant current can be observed at resonant frequency. The calculated RMS values of the currents are 15 A for I_m and 21.85 A for I_r, very close results to the values calculated in equations (3.11) and (3.10).

4.2 GaN Power Loss Calculation

There are two aspects that influence the losses: switching and conduction losses. Because GaN technology is not mature yet, estimating the switching losses can be a difficult task, not attempted by many before. One approach is to observe the switches behaviour in the proposed circuit by means of an LTSpice simulation, using the model provided by the manufacturer. Then, the already known switching performance of MOSFETS can be adapted to match as much as possible the behaviour of the GaN switches. To accomplish this, the switching losses can be either calculated with the use of the capacitances, or with the use of a combination between gate charge of the device and its capacitances. In the case of this project, the second approach will be implemented, that is, by using the combined method. The gate charge of the used devices is illustrated in Figure 2-9 in Chapter 2.

The drain-source voltage and the drain-source current were plotted in Figure 4-3. The multiplication of these two values represents the power loss of the devices, while their integration over time gives the energy loss. Moreover, the third subplot

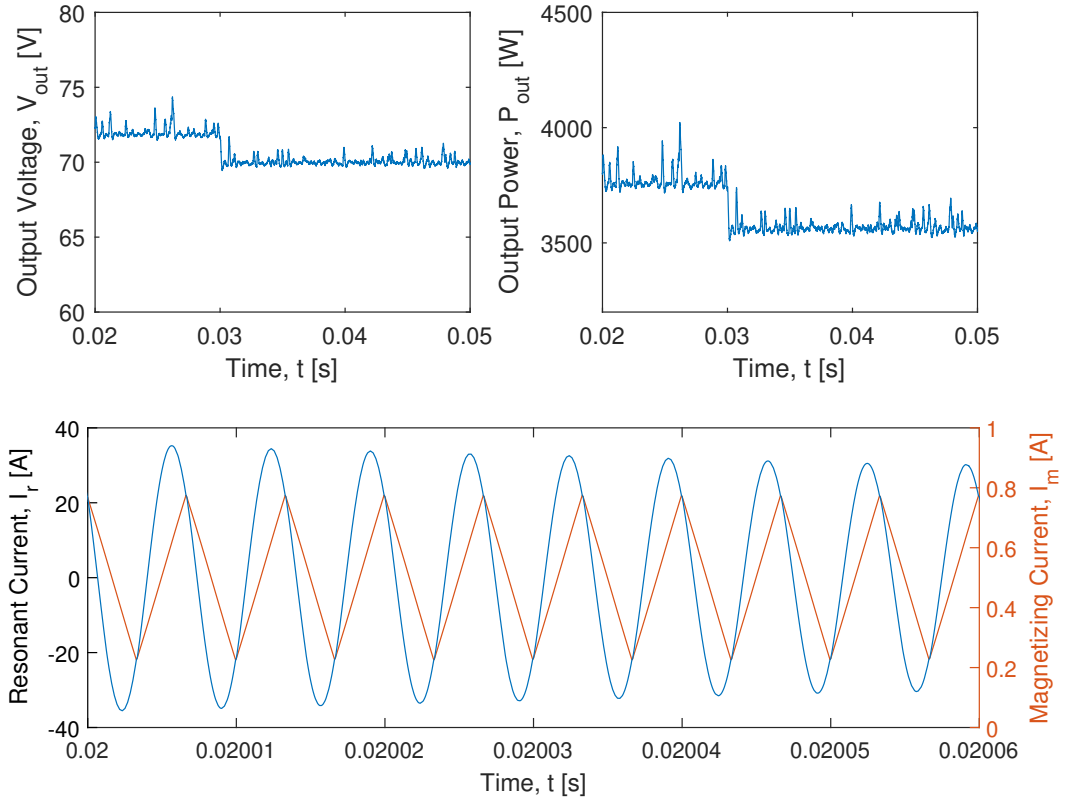


Figure 4-2: Step in the output voltage and power of the converter at the resonant frequency $fsw = 150kHz$, followed by 1% increase of f_{sw}; waveforms of the magnetizing, I_m, and resonant current, I_r.

in Figure 4-3 represents the gate-source voltage, which as stated earlier, at turn on is 6 V and at turn off is -3 V. This value also influences the power losses.

4.2.1 GaN Switching Losses

Switching losses are divided in two: turn-on losses and turn-off losses. The objective is to use the data provided by the datasheet of the device to estimate these losses. This estimation will then be compared to the results obtained from the simulation in LTSpice to verify their accuracy.

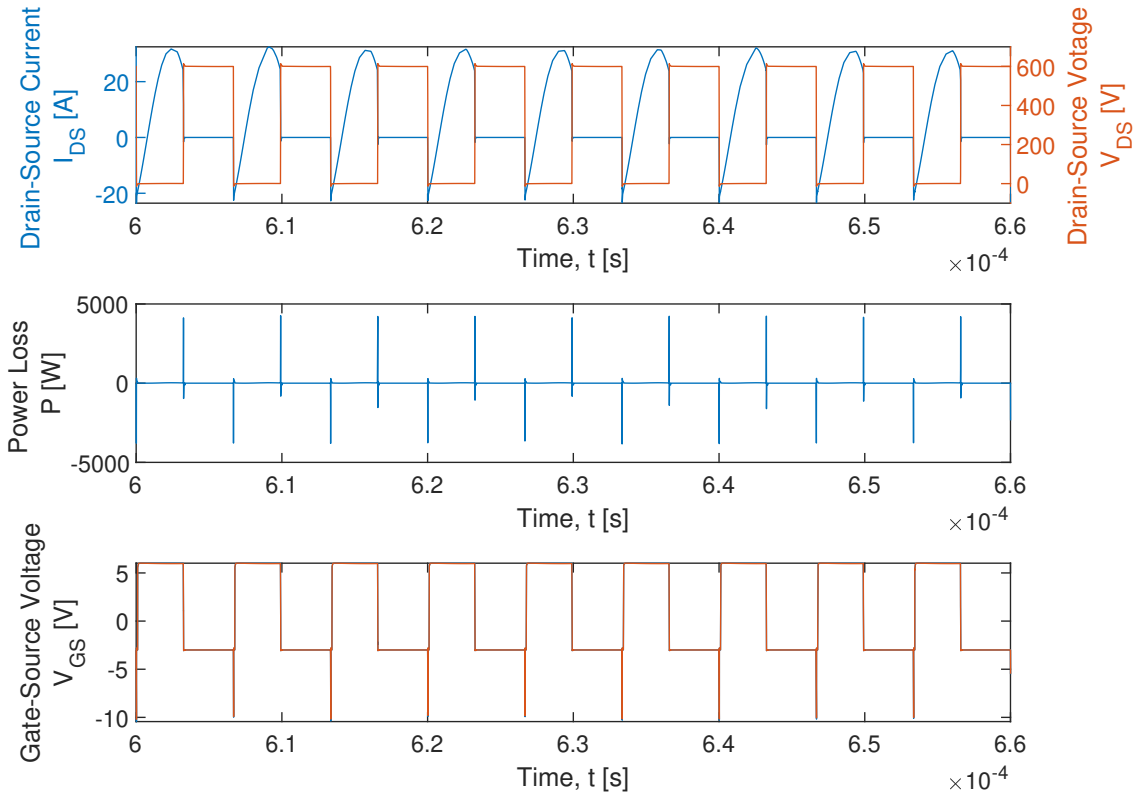


Figure 4-3: Full waveform at turn-on and turn-off of GaN switch.

4.2.2 Turn-on Losses

Although the turn-on losses have been put equal to zero in this work, thanks to the zero voltage switching phenomenon that is present at turn-on in the LLC converters, it is interesting to know the loss model of a GaN HEMT device during this operation [19] [20]. For this purpose, Figure 4-4 illustrates all of the stages involved. S_1 and S_2 are the two transistors in half-bridge configuration, while C_1 and C_2 represent the sum of the parasitic and external capacitances of the two switches. In the first stage, V_{GS} is higher than the threshold voltage, thus switch S1 is fully conducting. In Figure 4-4b the switch-off losses appear. The process is very similar to the MOSFET turn-off, and the Miller plateau can be observed. During the state (c), the reverse conduction of the switch S1 is taking place. Because the body diode is missing in GaN HEMT devices, the reverse conduction is different than it would be in a conventional

MOSFET. The process is explained more in detail in Chapter 1. Finally, the last stage consists of the switch S1 fully conducting [19].

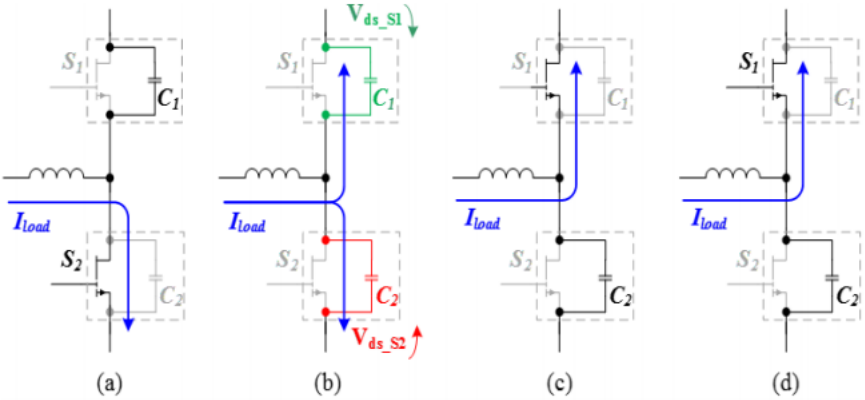


Figure 4-4: Zero voltage switching of a half bridge circuit, (a) S2 is conducting, (b) S2 is switching off, (c) S1 is reverse conducting, (d) S1 is conducting [19].

4.2.3 Turn-off Losses

The turn-off losses will be analyzed in this section. Figure 4-5 presents the turn-off waveforms captured from the simulation. The first noticeable thing is that although the load of the converter is inductive, the switching corresponds to a resistive switching. Unlike the inductive switching, where the current remains constant while the voltage changes and vice-versa, in the proposed circuit both current and voltage change simultaneously during the crossover interval [21]. By referring to Fig. 4-4, when transistor S2 is switching off, the voltage increases gradually. However, the slope of this voltage is depended on the capacitance C_2. The higher the value of C_2, the more shallow the slope of the voltage becomes. In addition to this, the magnitude of the switching losses also decreases [22].

There are five distinctive moments that define the turn-off process. Time moment t_0 represents the moment when the switching begins. For the development of the model, t_0 will be considered equal to 0. Just like in the case of inductive switching, time t_1 represents the starting point of the Miller plateau. After this moment, the behaviour of the curves starts to resemble the resistive switching.

Instant t_D is the point in time when V_{DS} reaches 15% of the final value. The end of the Miller plateau is marked by t_2, and finally, t_3 represents the moment when the drain current reaches 0. All these instants of time are defined for the turn-off process, and have to be manually identified for a given switch model. By estimating their position, the losses can be calculated. On the other hand, the already presented time instants have to be compared to the calculated ones. These time instants can be determined through the use of mathematical equations and by using the data provided in the datasheet.

The turn-off power losses generated by the switch are determined by calculating the area under the power loss curve from Figure 4-5 between time interval t_D and t_3. As a result, the power loss displayed by the simulation is equal to $P_{offS} = 4.55W$.

Before building the mathematical model, some parameters of the switching device must be extracted from the datasheet, such as the input, output and reverse trans-

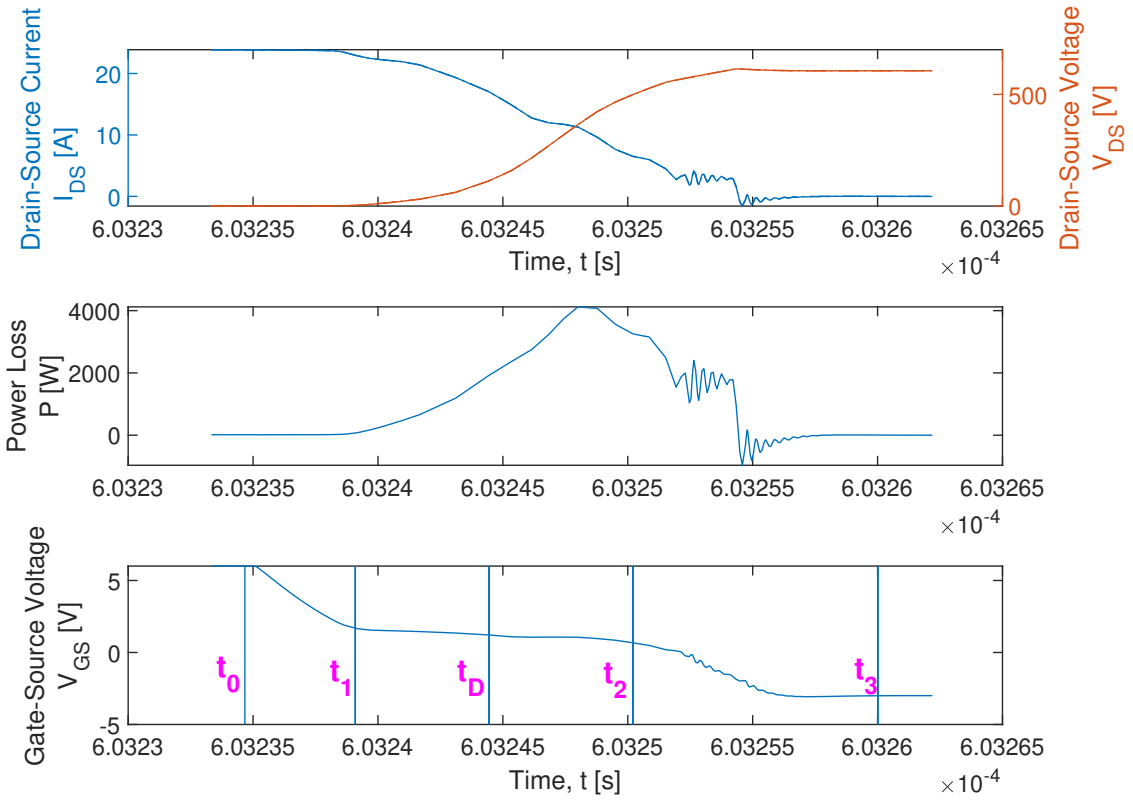


Figure 4-5: Waveforms of GaN device at turn-off under the simulation parameters.

fer capacitances, the threshold voltage, internal gate resistor. For a more concise understanding, all the needed parameters are listed in Table 4.2.

By using equations (2.15) and (2.16), the junction capacitances can be calculated at different voltages. As a result, the gate-source capacitance at 600V is $C_{GSHV} = 516pF$, respectively at low voltage, $C_{GSLV} = 480pF$. The drain-source capacitance at high voltage is $C_{DSHV} = 136pF$, while at low voltage is $C_{DSLV} = 880pF$. Finally, as stated earlier, the reverse transfer capacitance is equal to C_{GD}, which at high voltage is 4pF and at low voltage is 120 pF.

Moreover, the total resistance at turn-on and turn-off is a combination between the internal resistor, R_{gint} and external resistors $R_{G(ON)}$ and $R_{G(OFF)}$, such that R_{ON} and R_{OFF} have the following values:

$$R_{ON} = R_{gint} + R_{G(ON)} = 0.34 + 20 = 20.34\Omega \tag{4.1}$$

$$R_{OFF} = R_{gint} + R_{G(OFF)} = 0.34 + 4 = 4.34\Omega \tag{4.2}$$

To calculate the moment in time when V_{GS} reaches the Miller plateau voltage, equation (4.3) is used.

$$t_1 = t_0 - R_{G(OFF)} \cdot (C_{GDLV} + C_{GSLV}) \cdot log\frac{V_{G(ON)} - Vmiller}{V_{G(ON)} - V_{G(OFF)}} \tag{4.3}$$

$$t_2 = t_1 + \frac{Q_{GD} \cdot V_{DC} \cdot R_{OFF}}{V_{DSdata} \cdot (V_{G(ON)} - Vmiller)} \tag{4.4}$$

$$t_{D1} = \frac{(C_{GDHV} \cdot depth) \cdot V_{DC}}{I_{GDoff}} \tag{4.5}$$

$$t_{D2} = \frac{C_{GD} \cdot (1 - depth) \cdot V_{DC}}{I_{GDoff}} \tag{4.6}$$

where C_{GD} is equal to the value of $Crss$ at 25 V and I_{GDoff} is calculated with

equation (4.7).

$$I_{GDoff} = \frac{V_{miller} - V_{G(OFF)}}{R_{OFF}} \tag{4.7}$$

Moment of time t_D is equal to the sum of t_{D1} and t_{D2}. Finally, time t_3 is calculated with equation (4.9), where I_{Loff} is equal to the drain current of the GaN switch during the switching interval and it is assumed to have the same value for the turn-on and turn-off.

$$t_D = t_2 - (t_{D1} + t_{D2}) \tag{4.8}$$

$$t_3 = t_2 + R_{OFF} \cdot (C_{GDHV} + C_{GSHV}) \cdot \frac{I_{nom}}{I_{Loff}} \tag{4.9}$$

Although t_4 does not have any influence on the final value of the loss, it can be calculated, and represents the point where the switching has ended completely. Thus in the case of turn off, where current fully becomes zero, and drain-source voltage is equal to V_{DC}.

$$t_4 = t_3 + R_{OFF} \cdot (C_{GDHV} + C_{GSHV}) \cdot log\frac{V_{gsth} - V_{G(OFF)}}{0.9 \cdot V_{gsth} - V_{G(OFF)}} \tag{4.10}$$

As a way of displaying the obtained results, different intervals of time have been considered and are described in Table 4.3. The first column of the table represents the chosen intervals, the second column represents the value of the said interval obtained from the mathematical model developed in MATLAB, while the third column displays the results obtained from the LTSpice simulation. Finally, the last column represents the difference between the model and simulation. As illustrated in the table, the differences are very small and do not exceed 1.4 ns, meaning the constructed model is valid and can be used to calculate the switching losses for turn-off operation.

The formula to calculate the turn-off losses is described in equation (4.11), and as stated earlier, takes into account the interval between t_D and t_3, because that is the interval in which the voltage and current crossover. It is worth noting that k_{off} is a

GaN Datasheet Parameters	Value	Unit
C_{issLV}	600	pF
C_{ossLV}	1000	
C_{rssLV}	120	
C_{issHV}	520	
C_{ossHV}	140	
C_{rssHV}	4	
V_{gsth}	2.6	V
V_{miller}	3	
R_{gint}	0.34	Ω
Q_{GD}	5.4	nC

Table 4.2: Datasheet parameters GaN GS66516T.

Intervals	Model	Simulation	Diff.
$t_1 - t_0[ns]$	2.8608	3.3395	-0.4787
$t_D - t_1[ns]$	7.1176	6.0410	1.0766
$t_2 - t_D[ns]$	4.6004	6.0038	-1.4034
$t_2 - t_1[ns]$	11.7180	12.0448	-0.3268
$t_3 - t_2[ns]$	13.5560	14.5794	-1.0234

Table 4.3: Determined time intervals at turn-off switching in the LTSpice simulation, MATLAB model and their difference.

factor equal to 0.35. It is used to adjust the value of the drain current.

$$P_{offM} = (V_{DC} \cdot I_{Loff} \cdot k_{off} \cdot \frac{t_2 - t_D}{2} + V_{DC} \cdot I_{Loff} \cdot k_{off} \cdot \frac{t_3 - t_2}{2}) \cdot f_{sw} = 3.75W \quad (4.11)$$

The difference between the power obtained in the LTSpice simulation and MATLAB model is approximately 0.8 W since $P_{offS} = 4.55W$ and $P_{offM} = 3.75W$.

4.2.4 GaN Conduction Losses

The conduction losses of the GaN switches can be estimated in the same manner as with a regular Si MOSFET. The device can be modelled with a pure resistor, $R_{DS(ON)}$. In this case, by looking into the datasheet, the typical value of the internal resistor is 0.025Ω, at 25°C. This value multiplied by the square of the switching current represents the conduction losses of the device.

The switching current that flows though the transistor can be expressed as in equation 4.12.

$$I_{DS(RMS)} = \frac{I_{DS} \cdot \sqrt{\delta}}{\sqrt{2}} = \frac{23 \cdot \sqrt{0.5}}{2} = 11.5A \tag{4.12}$$

$$P_{COND_M} = R_{DS(ON)} \cdot I^2_{DS(RMS)} = 0.025 \cdot 11.5^2 = 3.31W \tag{4.13}$$

Therefore, the losses estimated by the model are equal to 3.31 W as seen in equation 4.13. Calculating the conduction losses obtained from the simulation of LTSpice consists of simply subtracting the switching losses calculated earlier from the total value of losses.

$$P_{COND_S} = P_{TOT} - P_{SWITCH_S} = 6.75 - 4.45 = 2.17W \tag{4.14}$$

Finally, the total losses derived from the MATLAB model of the GaN switches is equal to $P_{TOTAL_M} = 7.1W$, while the total losses extracted from the LTSPice simulation are equal to $P_{TOTAL_S} = 6.75W$.

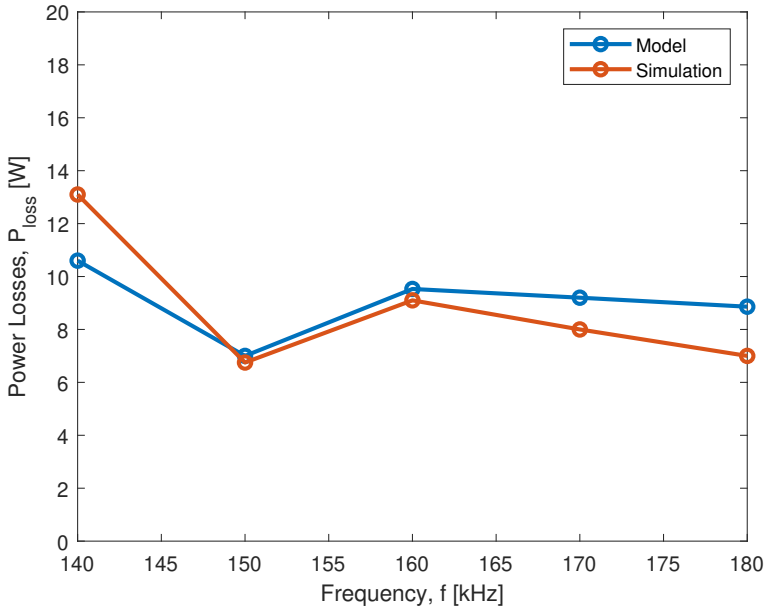


Figure 4-6: Comparison between GaN power losses obtained from the simulation vs. obtained from the model at different frequencies.

As seen in Figure 4-6, for switching frequencies raging from 140 kHz to 180 kHz,

and output power varying from 1.5 kW to 5.2 kW, the losses obtained from the simulation are compared to the ones obtained from the model. It is worth noting that in the case of changing the parameters of the simulation, the model of the losses changes accordingly, with a certain degree of error. The highest errors were registered at 140 kHz and at 180 kHz. However, they don't exceed a difference 2.5 W and the trend is consistent, therefore it can be used for the optimization process.

4.3 Magnetic Components Loss Calculation

Chapter 3 overlaps with the topic of this section. The reason for this is that the design of the three magnetic components implies the calculation of copper power loss. In order to calculate the optimum diameter for the chosen core material and type, the variation of the copper losses was observed. Finally, the diameter that generates the minimum losses is elected. Therefore, the process of calculating the AC power losses will not be repeated in this chapter, but the methodology for determining the core losses will be explained and the results of the calculations will be commented.

4.3.1 Series Resonant Inductance

In the case of the series inductance, the designed conductor diameter is 1.75 mm. This generates copper losses of $P_{CU} = 46.3W$.

To determine the core losses, the high frequency magnetic flux density has to be calculated using equation (2.20), which is then introduced into equation (2.19) to obtain the value of P_{CORE}.

$$B_{ac|HF} = \frac{Lr \cdot I_{ac|HF}}{A_e \cdot N} = \frac{26.7 \cdot 10^{-6} \cdot 21.24}{3.68 \cdot 10^{-4} \cdot 20} = 109mT \tag{4.15}$$

$$
\begin{aligned}
P_{CORE} &= c \cdot f^x \cdot {B_{ac|HF}}^y \cdot V_e \\
&= 5.4 \cdot 10^{-8} \cdot (150 \cdot 10^3)^{1.59} \cdot (109 \cdot 10^{-3})^{2.32} \cdot 51500 \cdot 10^{-9} \\
&= 2.76 \cdot 10^{-6} W
\end{aligned} \tag{4.16}
$$

The core losses are truly negligible in the case of this resonant converter. By summing the copper and core losses, the result of the total losses still adds up to 46.3 W.

4.3.2 Magnetizing Inductance

The copper losses in the case of L_m are equal to $P_{CU} = 16.5W$ in the configuration developed in Chapter 3. Moreover, the core losses of the magnetizing inductance is done in a similar way, using equations (2.20) and (2.19). Just like in the previous case, the core losses are negligible.

$$
B_{ac|HF} = \frac{L_m \cdot I_{ac|HF}}{A_e \cdot N} = \frac{22.66 \cdot 10^{-6} \cdot 12.44}{2.8 \cdot 10^{-4} \cdot 10} = 143mT \tag{4.17}
$$

$$
\begin{aligned}
P_{CORE} &= c \cdot f^x \cdot {B_{ac|HF}}^y \cdot V_e \\
&= 1.966 \cdot 10^{-10} \cdot (150 \cdot 10^3)^{1.84} \cdot (143 \cdot 10^{-3})^{2.68} \cdot 35500 \cdot 10^{-9} \\
&= 1.26 \cdot 10^{-7} W
\end{aligned} \tag{4.18}
$$

4.3.3 Filter Inductance

Lastly, the copper losses generated by the filter inductance, L_f are equal to $P_{CU} = 22.8W$. For the calculation of the core losses, the same formulas and algorithm were used, the result being similar to the other two inductances. The core losses are equal

to $P_{CORE} = 8.79 \cdot 10^{-9} W$, which is a negligible quantity.

$$B_{ac|HF} = \frac{L_f \cdot I_{ac|HF}}{A_e \cdot N} = \frac{0.7292 \cdot 10^{-6} \cdot 55}{9.71 \cdot 10^{-5} \cdot 10} = 194.7mT \tag{4.19}$$

$$\begin{aligned} P_{CORE} &= c \cdot f^x \cdot {B_{ac|HF}}^y \cdot V_e \\ &= 1.79 \cdot 10^{-11} \cdot (150 \cdot 10^3)^{1.91} \cdot (194.7 \cdot 10^{-3})^{2.91} \cdot 7460 \cdot 10^{-9} \\ &= 8.79 \cdot 10^{-9} W \end{aligned} \tag{4.20}$$

4.4 Rectifier Diode Loss Calculation

So far there were no discussions about the choice of the rectifier diodes, although they also have an impact in the generation of losses. The circuit adopted in this project is a full bridge rectifier for the following reasons: to minimize the copper losses of the transformer and to be able to use diodes with lower voltage rating than in the case of the full wave rectifier.

In order to choose the appropriate diodes for the circuit, three possible commercial choices are presented: a dual diode with common cathode Schottky rectifier suited for high frequency operations, model STPS80170C from STMicroelectronics; a dual Schottky doide package, APT2X101S20J from Microsemi; and a Schottky rectifier, STPS160H100TV, also from STMicroelectronics. All of them are designed for high frequency operation and provide low switching losses and low noise.

Just like the GaN switching devices, they have two types of power losses: switching and conduction.

$$P_{DIODE} = P_{COND} + P_{SWITCH} \tag{4.21}$$

4.4.1 Conduction Losses

Conduction losses represent the average dissipated power during the forward conduction. Normally, the expression for this losses can be written like in equation (4.22).

$$P_{COND} = I^2_{F(RMS)} \cdot R_d + V_F \cdot I_{F(AV)} \tag{4.22}$$

where R_d is the dynamic resistance and V_F is the forward voltage. R_d can be calculated by carrying out a linear interpolation from the "Forward Voltage vs Forward Current" characteristic from the datasteet of the diode.

However, in the case of rectifier diode STPS160H100TV from STMicroelectronics, equation (4.23) should be used to evaluate the losses. This equation is provided in the datasheet of the device [23] [3].

$$P_{COND} = 0.56 \cdot I_{F(AV)} + 0.0015 \cdot I^2_{F(RMS)} \tag{4.23}$$

where $I_{F(AV)}$ is the average forward current and $I_{F(RMS)}$ is the forward RMS current.

The waveform of the current that flows into the diodes is half period sinusoidal and the average value is half the output current. A rough estimation is presented in equation (4.25).

$$I_{F(AV)} = \frac{2 \cdot I_{MAX}}{\pi} \cdot \delta = \frac{2 \cdot 67.2 \cdot \sqrt{2}}{\pi} \cdot 0.5 = 30.25A \tag{4.24}$$

$$I_{F(RMS)} = I_{MAX} \cdot \sqrt{\frac{\delta}{2}} = 67.2 \cdot \sqrt{2} \cdot \sqrt{\frac{0.5}{2}} = 47.52A \tag{4.25}$$

By replacing the values in equation (4.23), the obtained conduction losses are equal to $P_{COND_{1D}} = 20.3W$ for each diode. Taking into account that two diodes conduct at the same time, the final losses are double $P_{COND} = 40.6W$.

4.4.2 Switching Losses

The switching losses refer to the average power dissipated in the diode during the turn off process. They generally also include the reverse recovery losses [24]. However, since Schottky diodes are not minority carrier rectifiers, their reverse recovery time is zero, and as a result, the second bracket from equation (4.26) becomes zero as well. V_R represents the reverse voltage, while C_r is the junction capacitance, which can be determined from its variation versus the reverse voltage applied, according to the datasheet. C_r in this case of STPS160H100TV is equal to 1 nF [3].

$$\begin{aligned} P_{SWITCH} &= [(\frac{1}{2} \cdot C_r \cdot V_R^2 \cdot f_{sw}) + (\frac{1}{6} \cdot I_{RR} \cdot V_R \cdot t_b \cdot f_{sw})] \\ &= (\frac{1}{2} \cdot 1 \cdot 10^{-9} \cdot 52.5^2 \cdot 150 \cdot 10^3) \cdot 2 = 0.85W \end{aligned} \tag{4.26}$$

Finally, the sum of the switching and conducting losses generated by the diodes are equal to $P_{TOTAL} = 42.3W$.

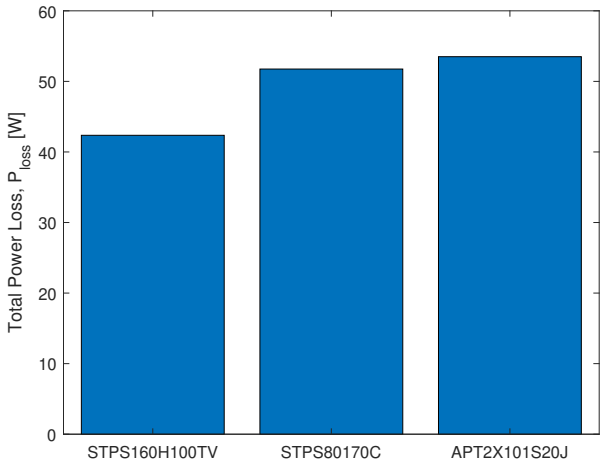


Figure 4-7: Total power losses of the rectifier diodes proposed at $f_{sw} = 150kHz$.

Figure 4-7 represents the total losses of the three sets of diodes that were taken into consideration. STPS160H100TV registers the lowest losses compared to the other two options, and as a result, it is the one used in the further analysis.

4.5 Total Loss Estimation

The summation of all the losses calculated in the sections above represents the total losses generated by the switching and magnetic components at the resonant frequency. They reach a total of $P_{loss@fsw} = 135W$.

A visual representation of these losses is done in Figure 5-5a. It can be observed that the resonant inductance, L_r, and the rectifier diodes produce the majority of the losses, summing a total of 65% of the total amount. This means that although the circuit outputs nominal power, its efficiency would be of 96.8%., calculated with equation (4.27). The lowest amount of losses belong to the magnetizing inductance and GaN switching devices. Through the optimization algorithm presented in Chapter 5, the efficiency of the converter can be raised.

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \tag{4.27}$$

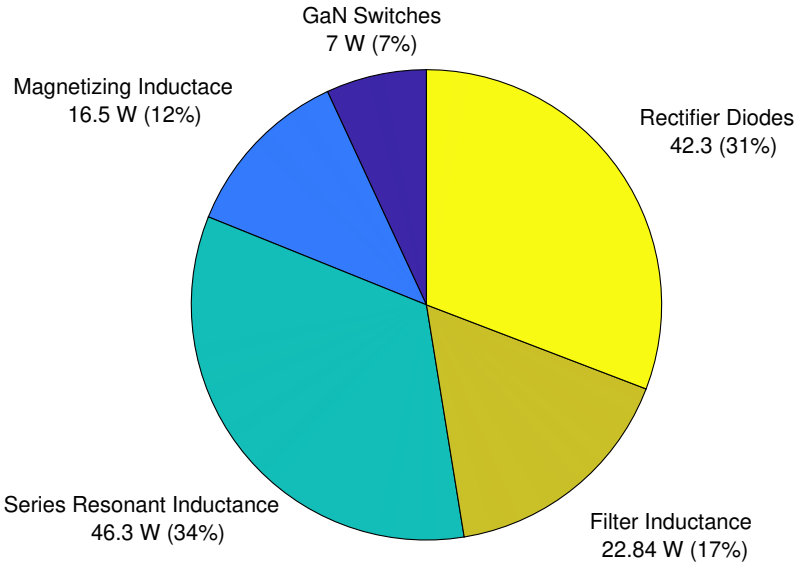
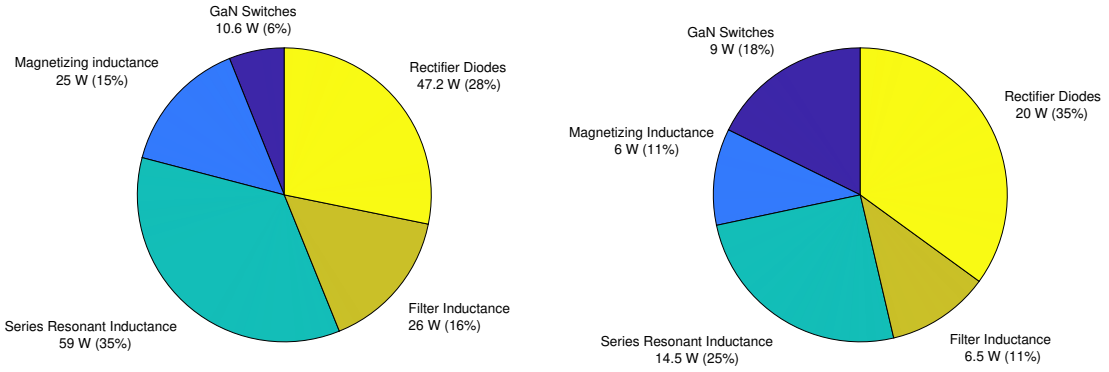


Figure 4-8: Total power losses of the LLC resonant circuit at resonant frequency, $f_{sw} = 150kHz$.

Figure 4-9 presents the power loss distribution at different switching frequencies



(a) Total power losses in the LLC resonant circuit at 140 kHz.

(b) Total power losses in the LLC resonant circuit at 180 kHz.

Figure 4-9: Total power loss under and over the resonant frequency.

than the resonant frequency. Figure 4-9a presents the simulation results at 140 kHz. Total losses under this conditions are equal to $P_{loss@140kHz} = 167W$. The losses are higher than when operating at resonant frequency, but at the same time the output power is higher as well. The efficiency of the whole circuit stays around 96.9%. Under the resonant frequency the RMS currents increase, and also the conduction interval decreases [20]. Still, the majority of the losses are produced by the series inductance and the rectifier diodes.

Furthermore, Figure 4-9b illustrates the distribution of the power losses above resonant frequency, at 180 kHz. Under this frequency, the total losses are equal to $P_{loss@180kHz} = 57W$. By operating above the resonant frequency, the losses decrease, but so does the output power. By calculating the ratio between the output and input power, the efficiency of the circuit keeps constant around the value of 96.2%. One thing to note is that although 35% of the losses are attributed to the rectifier diodes, if this percentage is translated into watts, it means only 20 W are lost out of the total 57 W. By comparison, in the case of operating the circuit at 140 kHz, the rectifier diodes generate only 28% of the losses, thus a smaller percentage. However, 28% out of 167 W represents 47.2 W, which means higher losses.

Finally, Figure 4-10 shows the efficiency curve of the resonant LLC converter versus its output power while varying the frequency from 140 kHz to 180 kHz. At

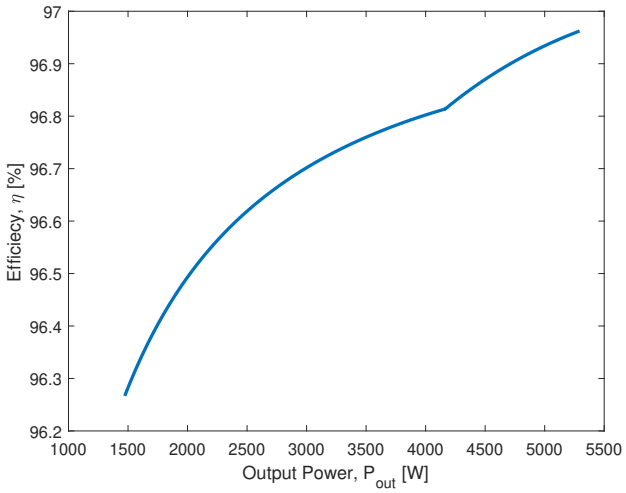


Figure 4-10: Efficiency curve for the designed LLC resonant converter as a function of the output power.

high load the efficiency is at its maximum value. On the other hand, the efficiency of the converter gradually decreases as f_{sw} rises and P_{out} decreases. However, the variation between efficiencies is fairly small as the frequency changes. The highest efficiency is registered around the maximum load, at around 5.2 kW with $\eta = 96.9\%$.

Chapter 5

Circuit Optimization

The previous chapter analyzed the losses of the system designed in Chapter 2. However, the design is not final without the optimization process. The aim of this step is to determine the appropriate values of the magnetizing and resonant inductances, of the capacitance, the optimum turn ratio and the switching frequency variation range, in order to have the least losses possible and to minimize the volume and cost of the converter.

The optimization script was built using the nonlinear programming solver, $fmincon$ in MATLAB. Let x be a vector defining all the design variables such as the switching frequency, f_{sw}, the DC voltage, V_{DC}, turn-on and turn-off gate resistors, $R_{G(ON)}$, $R_{G(OFF)}$, the diameter of the conductor, D, and the number of turns, N. They are variables of a nonlinear multi-variable function that define the losses of the system.

$$x = [f_{sw}, V_{DC}, R_{G(ON)}, R_{G(OFF)}, D, N] \tag{5.1}$$

Those six variables are considered for the initialization of the problem. Table 5.1 presents the lower and upper boundaries chosen for them. The output of the algorithm will have to take values in between these intervals. The idea behind of the optimization process is simple: set some key variables of the function in question to

	f_{sw} **[kHz]**	V_{DC} **[V]**	$R_{G(ON)}$ [Ω]	$R_{G(OFF)}$ [Ω]	D **[mm]**	N
Lower Boundary	80	500	10	1	0.05	2
Upper Boundary	200	700	30	10	10	100

Table 5.1: Initialization of the algorithm with the lower and upper boundaries of the key variables.

be optimized, develop some inequality constraints for the system to get the minimum values of the losses of the specified problem, and finally build an objective function to minimize the losses of the converter [25].

$$minP_{loss}(x) \tag{5.2}$$

To verify that the optimization solver completed its task, an exit flag is set. The exit flag is an integer, and depending on its output value it can mean: if it is a positive integer then the outcome of the solver is successful, a negative exist flag corresponds to an unsuccessful outcome, and a zero exit flag corresponds to the halting of the solver due to exceeding the maximum number of iterations.

Six inequality constraints have been used. Two of them are to assure that the turn on and turn off gate resistors ratio does not exceed 10 or goes below the ratio of 5, as written in equation (5.3) and (5.4). The other constraints refer to the magnetic components, since in the initial design the majority of losses were generated by the series resonant inductor. The number of turns should not go above the maximum number of turns calculated using the saturation value of the magnetic flux density, see equation (5.5). Another constraint is linked with the maximum number of turns depending on the core geometry. Again, the turn number should not exceed the maximum turn number, as illustrated in equation (5.6). The fifth inequality concerns the ratio between the number of turns and the number of turns per layer. This ratio should be higher than 1, as illustrated in equation (5.7). And finally, the last constraint is derived from constraint number 4, and can be seen in equation (5.8).

$$-\frac{R_{G(ON)}}{R_{G(OFF)}} + 5 \leq 0 \tag{5.3}$$

$$\frac{R_{G(ON)}}{R_{G(OFF)}} - 10 \leq 0 \tag{5.4}$$

$$-N + N_{sat} \leq 0 \tag{5.5}$$

$$N - \frac{Lwf \cdot w_e \cdot h_e}{h^2} \leq 0 \tag{5.6}$$

$$\frac{-N}{N_{tl}} + 1 \leq 0 \tag{5.7}$$

$$\frac{N \cdot D^2 \cdot \frac{\pi}{4}}{Lwf^2} - w_e \cdot h_e \leq 0 \tag{5.8}$$

After running the optimization algorithm, the exit flag is successfully 1, meaning that the solver converged to a possible solution. Therefore, the lowest losses are registered at a switching frequency of 110 kHz, with a DC bus voltage of 600 V, and the mention that the core geometry and materials of the three inductors is completely different from the initial design.

The new resonant tank at the new frequency is equal to: $L_r = 37.8\mu H$, $L_m = 31.5\mu H$ and $C_r = 58nF$. Fig. B-1 from Annex B shows the voltage gain vs. the normalized frequency for varying quality factor in the optimized design. Moreover, the waveforms of the currents and voltages at below, above and at the new resonant frequency are illustrated in Fig. B-2 and Fig. B-3.

5.1 GaN Power Losses and Rectifier Diodes

GaN GS66516T is the only type of switching device used for this project, meaning there is not much to optimize to have lower losses. Without repeating the method described in the previous chapter, with the help of the datasheet, the switching and conduction losses are calculated at the new switching frequency. Once again, these results are checked against a simulation in LTSpice and compared. The obtained results are very similar to the ones obtained in the initial design. Switching losses from the simulation are equal to $P_{SWITCH_S} = 3.35W$ compared to the losses obtained from the model $P_{SWITCH_M} = 2.7W$. Moreover, conduction losses are equal to $P_{COND_S} = 3.5W$, respectively $P_{COND_M} = 3.3W$. Different values of the losses can be seen in Figure 5-1, where it can also be noted the degree of accuracy of the developed model against the simulation.

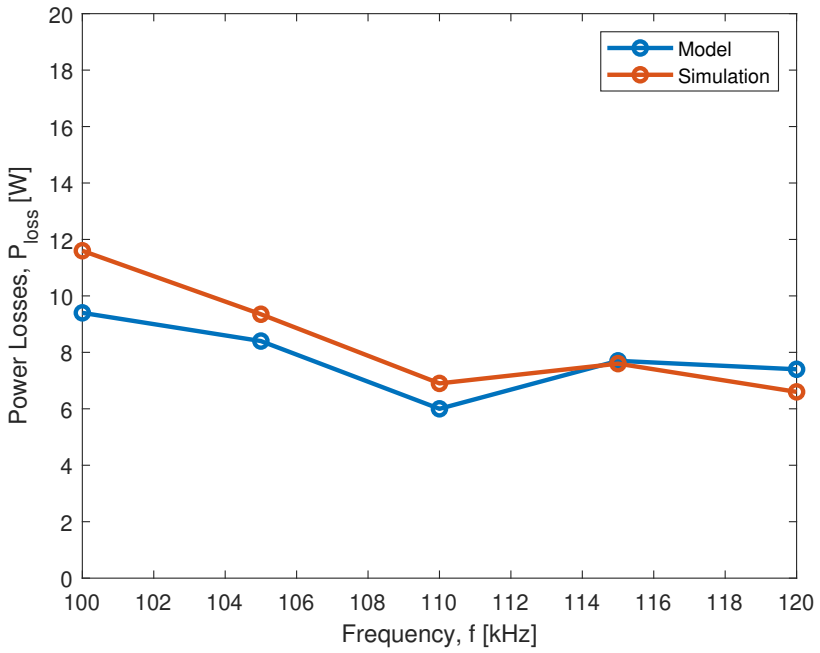


Figure 5-1: Comparison between GaN power losses obtained from the simulation vs. obtained from the model after optimization of the circuit.

In the case of the rectifier diodes, much like the GaN switches, the losses do not change significantly. The output current and voltage remains the same, even though the resonant frequency of the tank is changed. As a result, the conduction losses after

the optimization of the circuit remain equal to $P_{COND} = 41.3W$ and the switching losses are equal to $P_{SWITCH} = 0.4W$, summing a total of $P_{TOTAL} = 41.7W$.

5.2 Magnetic Components Loss Calculation

In the case of the three inductances, the new design parameters are presented in Table 5.2. The core type of the resonant and magnetizing inductances was correctly chosen in the intial design, however, the magnetic materials differs, ultimately changing the diameter of the conductor, the number of turns and the airgap, thus the losses.

	Value $[\mu H]$	**Core Material**	**Core Type**	**Diameter of conductor [mm]**	**Turns**	**Airgap [mm]**
L_r	37.8	3C94	ETD59	5.6	6	0.4
L_m	31.5	3C92	ETD54	6.7	4	0.14
L_f	1.01	3C96	ETD29	3	4	1.49

Table 5.2: Data for designing the inductances of the resonant converter.

The series resonant inductor's new optimized losses are much diminished than the originally calculated ones. The difference is especially visible when observing the copper losses. With an ETD59 core and 3C94 material, the core losses are still negligible with a value of $P_{CORE_{LR}} = 1.99 \cdot 10^{-6}W$. The copper losses at the resonant frequency become 90% smaller by: increasing the diameter of the conductor from 1.75 mm to 5.6 mm, decreasing the number of turns from 20 to 6 and also decreasing the size of the airgap from 6.83 mm to 0.4 mm. Therefore, the final value of the copper losses becomes $P_{CU_{LR}} = 16.5W$.

The same applies for the magnetizing inductance L_m. By changing the material of the core, the losses become equal to $P_{CORE_{LM}} = 1.04 \cdot 10^{-7}W$. The copper losses decrease in this case as well, even though, in the initial design, their ratio of the total losses was not high. Here as well, the diameter of the conductor was increased, while the number of turns and the length of the airgap were decreased. The final value of the copper losses is equal to $P_{CU_{LM}} = 2.2W$.

Figure 5-2 illustrates both the series and the magnetizing inductances already

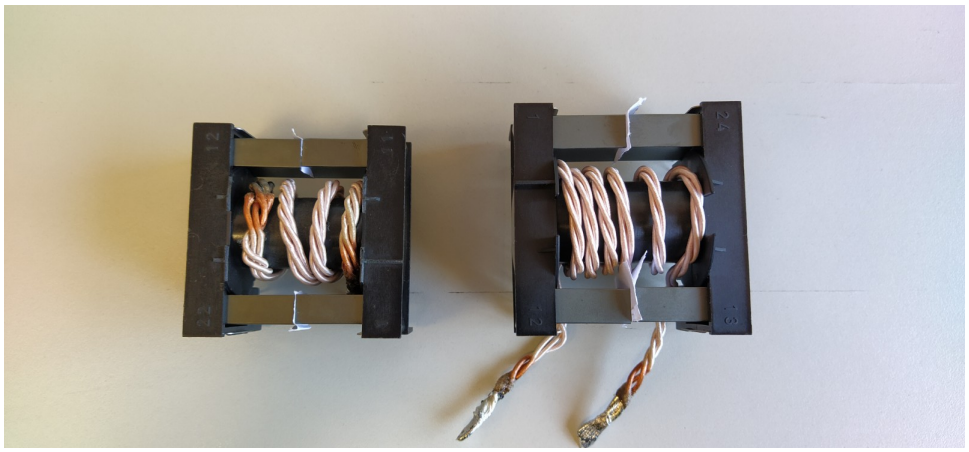
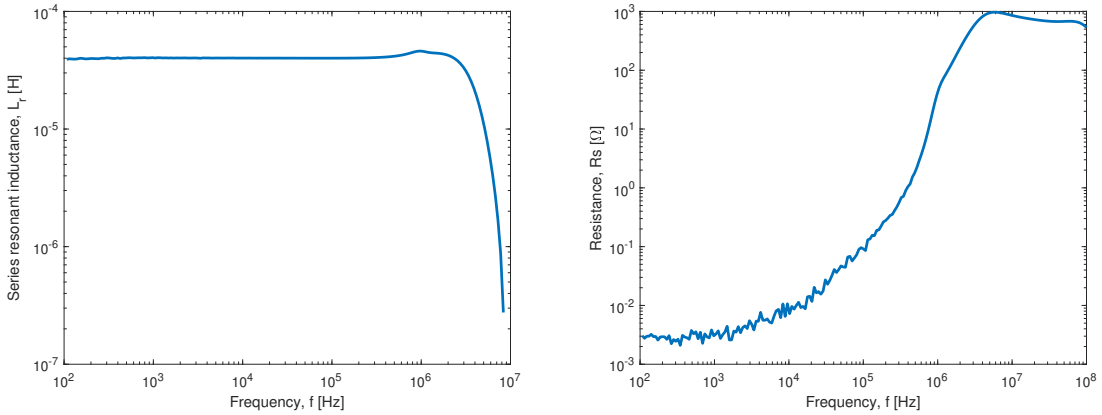


Figure 5-2: The already wounded inductances: the series inductance in the left and the magnetizing inductance in the right.

wounded. Litz wire was used in both of their construction. To build the series inductance, the approximate diameter of the conductor used is 5 mm instead of 5.6 mm. By putting it under test using the impedance analyzer, the results can be observed in Figure 5-3a and 5-3b.



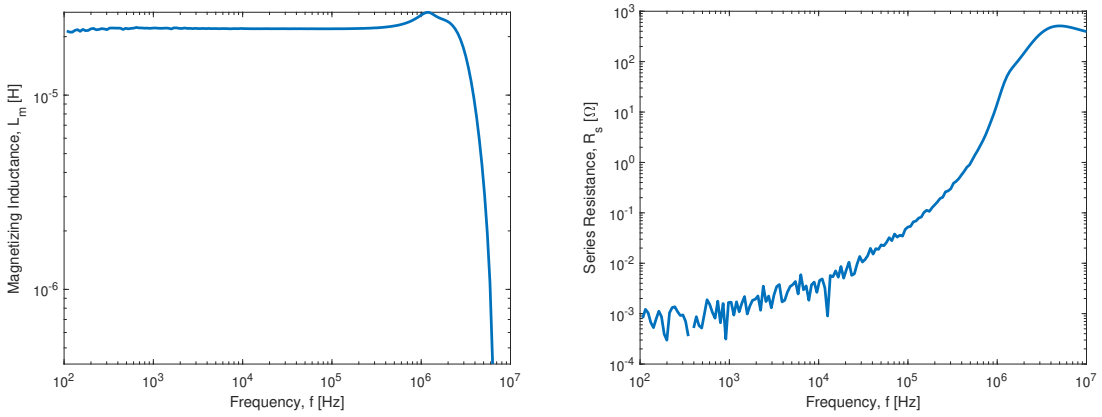
(a) Resonant series indutcance versus frequency. (b) Series resistance versus frequency.

Figure 5-3: Inductance and series resistance values of the series resonant inductor, L_r vs. frequency.

Looking at the graph, until around 500 kHz, L_r is constant and takes the value of approximately $40\mu H$, which is an admissible error compared to the designed $37.77\mu H$. Moreover, at a frequency of 110 kHz, the series resistor of the resonant inductor is equal to approximately $90m\Omega$, according to Figure 5-3b, and keeps increasing along

with the frequency.

For the case of the magnetizing inductance, L_m, the magnetic material 3C92 was not available, but because the characteristics of N97 material are relatively similar, it was decided to be used instead. Furthermore, the length of the air gap can be tuned only in intervals of 0.2 mm in the laboratory, and for this reason, it was not possible to build it with the required 0.14 mm. Taking into consideration all of the above, the resulting curves from the impedance analyzer can be observed in Figure 5-4.



(a) Magnetizing indutcance versus frequency.

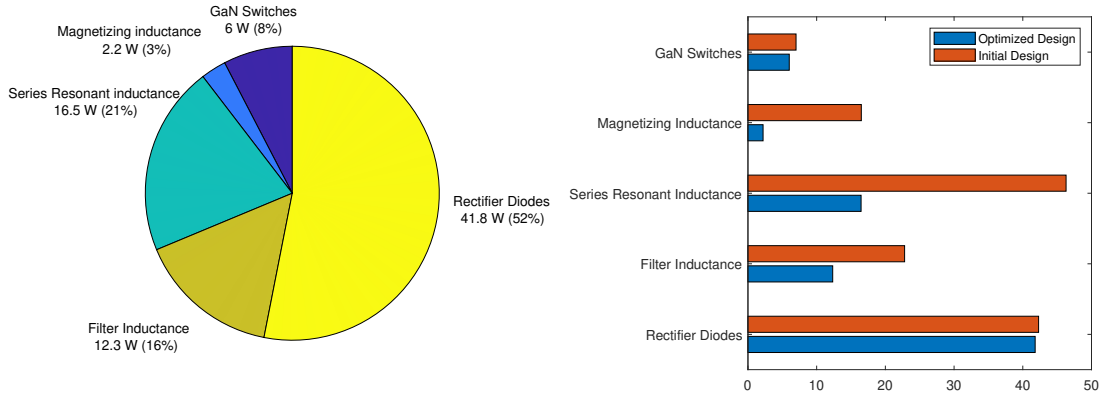
(b) Series resistance versus frequency.

Figure 5-4: Inductance and series resistance values of the magnetizing inductor, L_r vs. frequency.

At the frequency of interest, $f_{sw} = 110kHz$, the magnetizing inductance is equal to approximately $22\mu H$, well far from the designed $31.5\mu H$. This is the result of not using the right magnetic material and having a bigger air-gap length than designed. However, if the design is sent to a manufacturer, the resulting values should be closer to the desired ones. Nevertheless, the evolution of losses and inductor against the frequency would be similar to the data presented in this Figure 5-4.

5.3 Comparison Initial Design against Optimized Design

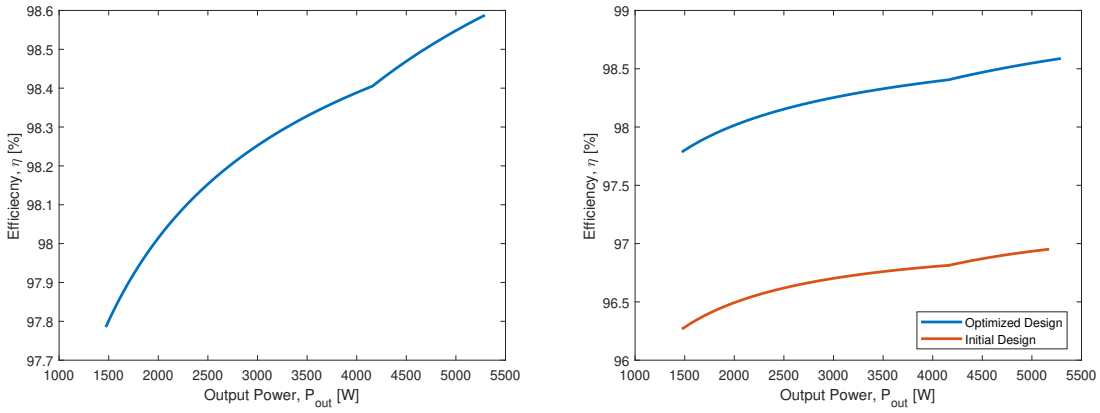
The losses of the whole circuit decrease drastically after the optimization process. In Figure 5-5a, the new distribution of power losses can be seen. The majority belongs to the rectifier diodes this time, while the series resonant inductor is accountable for only 21% of the losses of the whole system. Overall, the efficiency greatly increased to 98.4% at nominal load, compared to 96.8%, in the previous case, summing a total of 80 W of losses.



(a) Total power losses of the optimized LLC reso-(b) Total power losses of the initial design vs. the nant circuit at resonant frequency, $f_{sw} = 110kHz$.optimized design at 150 kHz and 110 kHz, respectively.

Figure 5-5: Comparison of the power losses.

For a clearer idea about the order of magnitude of the losses, the two circuits, non-optimized and optimized, are compared in Figure 5-5b. It is clear that the design of the magnetic components is of critical importance in the process of designing the LLC converter. The losses of the series resonant inductor are almost 3 times lower in the second design. Another significant difference can be observed at the magnetizing inductance, where even though the magnitude of the losses is lower than L_r, the losses still decrease by 7.5 times after the optimization process. In the case of the GaN switches and rectifier diodes, the losses are comparable in both designs. It makes



(a) Efficiency curve as a function of output power for the optimized LLC resonant converter.

(b) Comparison of the efficiencies levels of the two designs versus the output power of the converter.

Figure 5-6: Comparison of the efficiencies of the two designs.

sense, then, to implement such an algorithm for determining the best configuration for the magnetic components. It can make the difference between a highly efficient design and a bad converter.

The efficiency curve is shown in Figure 5-6a. As stated earlier, at nominal load, the efficiency is approximately equal to 98.4%. At high frequency and low output power, the converter is less efficient, just as in the initial design. The highest efficiency can be observed around 5.2 kW, and it is equal to 98.6%.

Finally, Figure 5-6b shows the two systems' efficiency on the same graph, for gaining another perspective. It can be seen that the optimized design is superior to the initial guess. At the same time, the efficiency of each system does not vary a lot with the output power, but slowly increases from 96.2% to 97% in the first design, and is 98% in the optimized design.

Chapter 6

Conclusions and Further Work

6.1 Conclusions

This thesis has discussed and analyzed the design process of an LLC converter optimized in order to obtain the lowest losses possible given its application. The main components such as the series resonant inductance, the magnetizing inductance, the series resonant capacitor and turns-ratio of the transformer must be properly identified. This process requires a lot of knowledge from the point of view of power electronics and magnetic components.

The novelty of this converter is represented by the use of GaN Systems switching devices instead of Si MOSFTs. With their ultra-low on-resistance and parasitic capacitances, they represent a reputable candidate for the design of a high-power density and high efficiency converter. By making use of them, and by having an optimized design of the magnetic components, a maximum efficiency of 98.6% could be achieved. However, the drawback of using these switches is the lack of extensive documentation about them.

An LTSpice simulation of the half-bridge LLC converter circuit was used to determine the switching characteristics. From the conducted simulations using the model provided by GaN Systems, resistive switching was observed, instead of the expected

inductive switching. This observation represented a challenge both from the point of view of documentation, but also from the point of view of building a model that would calculate the switching times, since the already well-known model for Si MOSFETs does not apply in this case. The obtained result is far from perfect, but it successfully estimates the trends of the losses with various degrees of accuracy when the parameters of the simulation are modified. The highest accuracy obtained was of 0.03% around the resonant frequency of the converter in the initial design, while, at the extremes of the range of the operating frequency, the error increases up to 20%. Moreover, the subject of estimating the losses of GaN switches is vast and not very developed yet and could be a topic of research on its own.

The total calculated losses are almost 135 W in the initial design, which does not include any optimization process. As a result, the efficiency of the converter reaches only 96.8% for nominal conditions, which is not an unacceptable result, but can be improved. Out of all the elements of the converter, the magnetic components influenced the most the magnitude of the losses. Most notably, the series resonant inductor and the poor "first guess" of its magnetic material, number of turns, diameter and length of the air-gap was the source for approximately one third of the total losses in all the conducted simulations.

In order to optimize the design, the key parameters, such as the diameter of the conductor of the inductances, the number of turns and the switching frequency, to specify a few, were chosen and included into an objective function. Using the nonlinear programming solver, $fmincon$, a new resonant frequency of the tank was determined, along with new configurations for the magnetic components. In this new design, the losses are noticeably smaller, adding up to approximately 80 W under nominal conditions. This translates into an efficiency of 98.4% compared to the 96.8% calculated in the first design. The majority of the losses are not represented anymore by the losses generated by the series resonant inductor, but by the output-diode losses, which had the same magnitude in the initial design.

In addition, the inductors forming the resonant tank, L_r and L_m were built following the optimized design parameters. In the case of the series resonant inductor,

the obtained value corresponds to the calculated one. However, the resulting value of the magnetizing inductor is $10\mu H$ less than the calculated one. This happened as a result of using a different type of magnetic material for the core, and not being able to tune the length of the air-gap with a good enough accuracy.

In conclusion, all of the objectives mentioned in the first chapter were completed. Namely, the theoretical aspects of the resonant LLC converter and it's design steps, the basic GaN structure and the magnetic components overview was covered in Chapter 2. The design of the half-bridge LLC converter was carried out in Chapter 3, along with the design of the magnetic components. Moreover, several simulations were conducted in order to understand and calculate the switching and conduction losses of the GaN switches. In addition to that, Chapter 5 presents the development steps and implementation results of the optimization algorithm for the LLC circuit. Finally, the efficiency is calculated at different operating points, both for the initial design and for the optimized design in order to make a comparison and see the improvement after the optimization.

6.2 Future Work

After completing the optimization process of the LLC converter, more improvements can be done to achieve a more accurate analysis of the losses, as well as towards the research of the topic, especially because the circuit involves GaN switches. Therefore, the future work that can be implemented is listed below:

- First, the construction of the proposed design in order to compare the obtained results with experimental results. In fact, this work was initially included in the objectives of the thesis, however, due to the circumstances, it was not possible to be carried out.

- An extended research can be done with the purpose to better identify the switching behaviour and switching times of the GaN switching devices. This would allow a further improvement of the model that estimates the switching losses.

- Use of a synchronous rectifier on the secondary side of the high power resonant converter for designing an efficient circuit. The system should offer a higher efficiency than Schottky or standard diodes.

- An analysis and optimization of cost and volume of the converter, to obtain the most convenient architecture from the point of view of the cost, volume and efficiency.

Appendix A

Tables

Core Name	**ETD29**	**ETD34**	**ETD39**	**ETD44**	**ETD49**	**ETD54**	**ETD59**
$V_e \cdot 10^{-9}$ $[m^3]$	5470	7460	11500	17800	24000	35500	51500
$Ae \cdot 10^{-6}$ $[m^2]$	76	97.1	125	173	211	280	368
$L_e \cdot 10^{-3}$ $[m]$	72	78.6	92.2	103	114	127	139
$w_e \cdot 10^{-3}$ $[m]$	22	23.6	28.4	32.2	36	40	45
$h_e \cdot 10^{-3}$ $[m]$	6.1	7.25	8.25	8.65	9.5	11	13

Table A.1: Available core sizes and their physical properties.

Material Name	**3C81**	**3C90**	**3C91**	**3C92**	**3C93**	**3C94**	**3C95**	**3C97**	**3C98**	**3F3_**	**3F5_**
$c \cdot 10^3$ $[\frac{W}{m^3 \cdot mT}]$	5.4e-11	1.966e-13	7.41e-13	3.12e-16	1.23e-16	2.4e-12	1.79e-14	1.12e-13	1.79e-14	1.96e-13	9.14e-14
x	1.59	1.84	1.64	2.17	2.32	1.59	1.91	1.74	1.91	1.84	1.81
y	2.32	2.68	2.91	3.13	3.00	2.74	2.91	2.96	2.91	2.68	2.74
B_{ac} $[mT]$	360	380	370	460	430	380	410	440	410	370	340
μ_r	4000	3735	3600	3500	4000	4000	3200	3500	3200	3500	650

Table A.2: Available ferrite materials and their Steinmetz coefficients.

Appendix B

Figures

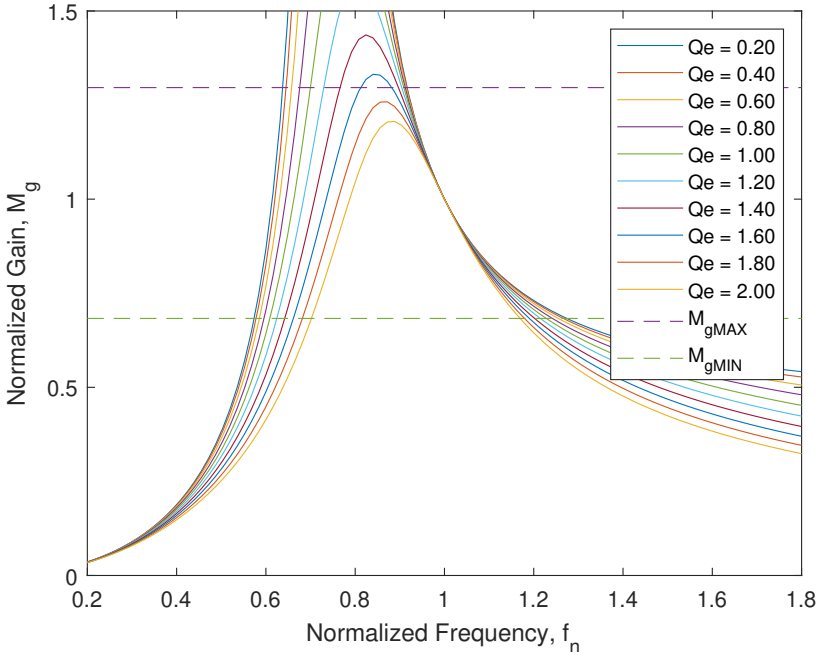


Figure B-1: Voltage Gain vs. Normalized Frequency for Varying Quality Factor in the Optimized Design. The new quality factor is equal to $O_e = 1.6$.

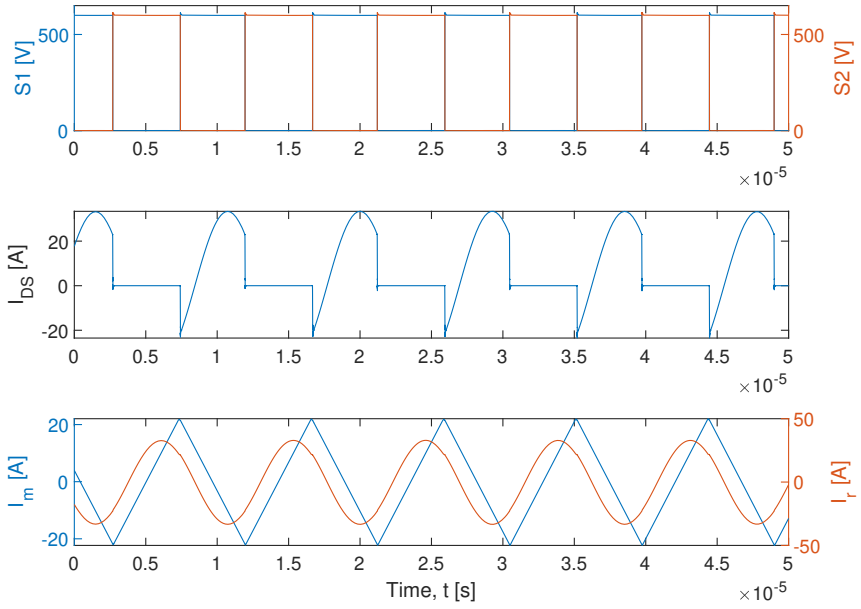
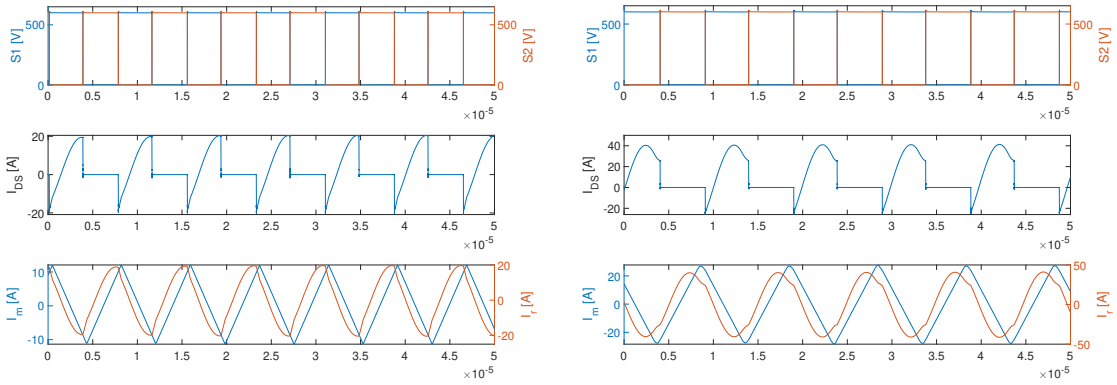


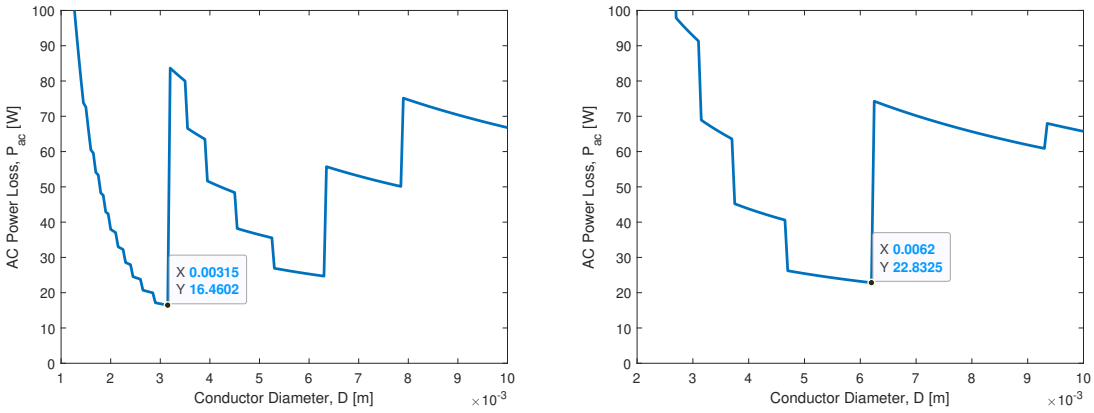
Figure B-2: Waveforms of the optimized circuit at the resonant frequency. In the figure are depicted the drain-source voltages of the two transistors S_1 and S_2, the drain-source current of S_2 and the magnetizing current and resonant current, I_m and I_r.



(a) Simulation at 130 kHz.

(b) Simulation at 100 kHz.

Figure B-3: Waveforms of the optimized circuit above the resonant frequency. In the figure are depicted the drain-source voltages of the two transistors S_1 and S_2, the drain-source current of S_2 and the magnetizing current and resonant current, I_m and I_r.



(a) Magnetizing inductor vs. conductor diameter. (b) Filter inductor vs. conductor diameter.

Figure B-4: Variation of AC power losses with the diameter calculated for the magnetizing and filter inductor.

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