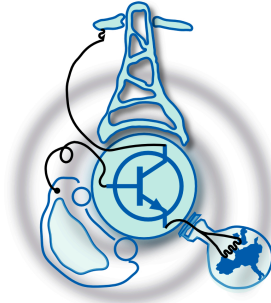


Analysis of Advanced Powertrain Architectures for Electric Racing Motorcycles Considering Hybrid Energy Storage and Wide-Bandgap Semiconductors



Submitted to the Department of Electrical Engineering, Electronics,
Computers and Systems
in partial fulfillment of the requirements for the degree of
Erasmus Mundus Master Course in Sustainable Transportation and
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Abstract

The rapid progress in the fields of energy storage and power electronics offers various promising improvements of conventional powertrain architectures. This thesis investigates the improvement potential of Hybrid Energy Storage Systems (HESSs) and Gallium Nitride (GaN) semiconductors in the powertrain of an electric racing motorcycle, designed for the MotoStudent competition.

To ascertain the state of the art, the powertrain architectures of several commercial electric motorcycles and racing prototypes are compared. Subsequently, the powertrain of the current prototype, developed at the University of Oviedo, is explained in detail and the performance is analytically assessed.

As first potential improvement, HESSs made of Lithium-Ion (Li-ion) batteries and Ultracapacitors (UCs) are evaluated. An optimization algorithm for the design of the HESS, which considers two semi-active topologies, is introduced. Further analysis juxtaposes the optimization results with pure Li-ion battery storage in terms of weight and volume. In the case of the MotoStudent load profile, results in favor of pure battery storage are presented.

Thereupon, the feasibility of a 500 A_{RMS} GaN traction inverter is analyzed. For this purpose, an electrical and thermal co-simulation is performed in PLECS. In order to accurately model the semiconductor losses, 3D lookup tables are utilized. Based on the results, a minimum number of sixteen parallel devices is determined to meet the requirements. As such high numbers of parallel devices have not been studied in literature yet, a double-pulse test Printed Circuit Board (PCB) is designed to evaluate the feasibility. The measurements carried out demonstrate the full functionality of the design and successful parallelization of sixteen GaN transistors.

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List of Acronyms

BEMF	Back Electromotive Force. 38, 39, 66, 70, 72
CMTI	Common Mode Transient Immunity. 97, 98
DSP	Digital Signal Processor. 104, 115
ESR	Equivalent Series Resistance. 32, 51
ESS	Energy Storage System. 43, 47, 54, 69, 109
GaN	Gallium Nitride. 3, 23, 27, 46, 77–79, 83, 87–89, 93, 95, 97, 109–111
HEMT	High-Electron-Mobility Transistor. 77–80, 83, 87–89
HESS	Hybrid Energy Storage System. 3, 23, 25, 47, 53, 59, 61, 65, 69–73, 109, 111
IGBT	Insulated-Gate Bipolar Transistor. 78
IPM	Interior Permanent Magnet. 29, 31, 37, 85
Li-ion	Lithium-Ion. 3, 27, 31, 32
LPSA	Low Power System Architecture. 114, 115
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor. 77, 78

NCA	Nickel Cobalt Aluminium Oxide. 32
NMC	Nickel Manganese Cobalt Oxide. 32
PCB	Printed Circuit Board. 3, 75, 95–97, 100–102, 108, 109, 111, 115
PWM	Pulse-Width Modulation. 35, 37
RMS	Root Mean Square. 36, 38, 41, 46, 76, 119–121
Si	Silicon. 77, 78
SiC	Silicon Carbide. 77
SOC	State of Charge. 42, 61, 62, 65
SPM	Surface Permanent Magnet. 29
SVM	Space Vector Modulation. 37
THD	Total Harmonic Distortion. 37
THI	Third Harmonic Injection. 37, 82
UC	Ultracapacitor. 3, 11, 27, 47–49, 51–53, 55–58, 60, 61, 68–72

List of Symbols

β	Torque factor load profile
$\eta_{Powertrain}$	Operating point dependent efficiency powertrain
\hat{I}	Current amplitude
\hat{I}_{switch}	Maximum current per discrete semiconductor
\hat{V}	Voltage amplitude
$\hat{V}_{Ac,ph-n}$	Maximum achievable phase-to-neutral voltage amplitude inverter
ω_e	Angular electrical frequency
ω_r	Angular rotor speed
$\omega_{base,norm}$	Normalized base angular rotor speed
ω_{base}	Base angular rotor speed - beginning of field weakening for nominal DC-link voltage
$\bar{\eta}_{UC}$	Average discharge efficiency UC
$\Psi_{d,q}$	d,q axis components flux linkage
Ψ_{PM}	RMS flux linkage permanent magnets
$\overline{P_{bat}}$	Power battery pack limited to maximum value
φ	Phase-shift fundamental AC phase voltage and phase current

ϑ	Angle of the active space vector
$C_{\theta 1-4}$	Equivalent thermal capacitances semiconductor package
C_{bat}	Nominal capacity battery pack
C_{cell}	Nominal capacity single battery cell
$C_{DC-link}$	Capacitance DC-link
$\cos(\varphi)$	Power factor
E_{off}	Energy dissipated during turn-off
E_{on}	Energy dissipated during turn-on
E_{UC}	Energy stored in an ultracapacitor
f_{out}	Fundamental frequency inverter output voltage
f_{sw}	Switching frequency
g_m	Transconductance
$i_{d,q}$	d,q axis component stator current
$I_{max,cell}$	Maximum current single cell
I_{phase}	RMS phase current rating
k_t	Motor torque constant
$L_{q,d}$	d,q axis inductances electric machine
M	Modulation index defined according to [1]
n	Rotational speed of electric machine
N_p	Number of parallel cells within a battery pack
N_s	Number of series cells within a battery pack

n_{base}	Base rotational speed of electric machine - beginning of field weakening for nominal DC-link voltage
$n_{parallel}$	Number of parallel discrete semiconductors per switch
N_{tot}	Total number of cells within a battery pack
P_{bat}	Power battery pack
P_{nom}	Nominal power battery pack
P_{off}	Average off switching losses per switching period
P_{on}	Average on switching losses per switching period
P_{sw}	Average total switching losses per switching period
P_{UC}	Power ultracapacitor
PP	Number of polepairs electric machine
R_s	Stator phase resistance
$R_{\theta 1-4}$	Equivalent thermal resistances semiconductor package
$R_{DS,on}$	Semiconductor Drain-Source on-resistance
$R_{G,off}$	Effective Gate turn-off resistance per device
$R_{G,on}$	Effective Gate turn-on resistance per device
R_{HA}	Equivalent thermal capacitance heatsink to ambient
R_{HA}	Equivalent thermal resistance heatsink to ambient
r_{pp}	Normalized voltage ripple amplitude
R_{TIM}	Equivalent thermal resistance thermal interface material
T	Torque of electrical machine

T_H	Heatsink temperature
T_j	Junction temperature
T_{sw}	Switching period
V_C	Voltage across C_{UC} in equ. circuit of ultracapacitor
$v_{a,b,c}$	Stator phase a,b,c instantaneous voltages
$v_{d,q}$	d,q axis components stator phase voltage
$V_{DC-link}$	Voltage in the DC-link
v_{DS}	Drain-Source voltage
$v_{GD,th}$	Gate-Drain threshold voltage reverse conduction
v_{GS}	Gate-Source voltage
$V_{nom,cell}$	Nominal voltage single cell
$V_{out,cutoff}$	Minimum voltage of ultracapacitor discharge
v_{pp}	Peak-to-peak ripple amplitude DC-link

Chapter 1

Introduction

In the last century, racing has evolved from an exotic event to mass entertainment, with teams constantly pushing the boundaries of physics. From a technical perspective, the rapid prototyping in motorsports and the urge for higher and higher performance is ideal soil for innovation. Formula 1, as an example, has not only driven the technology of combustion engines but also inspired an improved aerodynamics system for commercial refrigerators, which helps to save energy [8].

Nowadays, expectations on race series range further than the pure competition and include socially relevant topics. Thus it is not surprising that a very young and modern racing series, the Formula E, has specifically centered their design rules around systems, relevant for the transition towards more sustainable transportation [9].

Following these objectives, MotoStudent Electric, a student competition on the development of an electrically propelled racing motorcycle, allows students an in-depth insight into prototyping of electric vehicles. Once a prototype is built, the clear goal is to evolve the motorcycle further. The rapid progress in the fields of energy storage, power electronics and drive systems offers many potential improvements in the powertrain. Regarding electric motorcycles, literature merely provides any comprehensive analysis of cutting edge technology and the underlying potential.

This thesis will thus evaluate two of the most polarizing topics of the electric powertrain, namely Hybrid Energy Storage System (HESS) and the implementation of Gallium Nitride (GaN) semiconductors in the traction inverter.

Chapter 2

Motivation

As any competitive racing series, the MotoStudent electric competition is based on the desire to develop the prototype with the highest performance. This competition is therefore an ideal platform to implement cutting edge technology and test it under harsh conditions.

When improvements on system-level are analyzed, profound knowledge about the powertrain and its limitations is a prerequisite. Consequently, it is essential to ascertain the performance of the University of Oviedo's prototype of the season 2020 (MS6) and understand its limits in a first step.

As the MS6 has proven, the powertrain volume, especially regarding the energy storage system, is a critical point to improve. Likewise, reducing the weight offers a significant advantage over competitors in the different tests of the MotoStudent competition, including an acceleration event and the final race.

Hybrid energy storage and wide-bandgap semiconductors are both promising technologies with the potential to increase the volumetric and gravimetric density of the powertrain. However, the question of whether HESSs can enhance the system and if wide-bandgap semiconductors are feasible, considering the converter requirements, is not trivial to answer. Accordingly, an analysis of the above is of utmost interest on the way to an advanced powertrain architecture for the electric racing motorcycle.

Chapter 3

Objectives

The objective of this master thesis is to assess the potential of hybrid energy storage and the feasibility of a traction inverter design using GaN semiconductors, thereby increasing the power density.

In order to establish a profound basis, chapter 4 juxtaposes existing solutions of commercial sport motorcycles and specifically built racing designs like the MS6 MotoStudent prototype of the University of Oviedo. Further, the chapter provides a detailed overview of the current powertrain architecture of the MS6 prototype, explaining the global impact of the subsystems and establishing a theoretical foundation for the following chapters. Eventually, the performance of the MS6 is analytically evaluated to identify improvements.

Chapter 5 answers the question, whether hybrid energy storage can yield higher volumetric and gravimetric density than pure Lithium-Ion (Li-ion) battery design. In the beginning, some theoretical background for Ultracapacitors (UCs) is introduced. Following this, a literature research of hybrid energy storage topologies is conducted and the most promising topology or topologies selected for further analysis. Eventually, an optimization of hybrid energy storage and pure li-ion battery storage is carried out, in order to provide a clear answer to the previously formulated research question of the chapter.

Chapter 6 elaborates the design of a 500 A_{RMS} traction inverter, making use of GaN semiconductors. Electrical and thermal requirements are worked out and

verified by simulation, using 3D lookup tables for semiconductor losses. Throughout the chapter, critical design points of the GaN-Inverter are identified and evaluated.

Chapter 4

State of the Art

4.1 Powertrain Architecture of Electric Motorcycles

In recent years, electric motorcycles have gained increasing attention, following the trend of electric vehicles. Most electric sport motorcycles are currently designed by start-ups, specifically dedicated to the development of electric motorcycles. At the same time, some traditional manufacturers develop prototypes and few already released commercially available motorcycles. The following chapter provides an overview of the powertrain architectures of commercially available electric sport motorcycles and compares them with specifically designed racing prototypes.

The comparison in tab. 4.1 demonstrates that all electric motorcycles implement permanent magnet synchronous machines, however, using different magnet alignments. The short-time current capability of the inverters ranges from 500 A_{RMS} to 1000 A_{RMS} , with most sport motorcycles utilizing designs at the upper limit. Several different voltage levels of the Li-Ion batteries are identified, even between motorcycles of similar power. The energy storage capacity of the commercially available motorcycles is in the range of 12 kWh for all models with one exception. As the range of the MS6 is determined by the MotoStudent race, the storage capacity is noticeably smaller compared to commercial electric motorcycles or the UoN Electric Superbike,

Table 4.1: Powertrain architectures of electric motorcycles

Model	Company	Powertrain Architecture	Motor	Inverter	Energy Storage
SR/S (2020)	Zero Motorcycles Inc.	(a) ¹	82 kW IPM Synchronous Machine passively air-cooled	N.A 900 A_{RMS}	Li-Ion 12.6 kWh 102 V nom
eGo (2019)	Energica Motor Company S.p.A.	(a) ¹	107 kW PM Synchronous Machine (Type unknown) Liquid Cooled	N.A.	Li-Ion 11.7 kWh 300 V nom
C Evolution (2018)	BMW AG	(a) ¹	35 kW SPM Synchronous Machine Oil Cooled	N.A 500 A_{RMS}	Li-Ion 12.5 kWh 133 V nom
UoN Electric Superbike (2019)	University of Nottingham	(a)	> 200 kW PM Synchronous Machine (Type unknown)	750 V 1000 A_{RMS}	Li-Ion 12 kWh N.A.
MS6 (2020)	Wolfast University of Oviedo	(b)	42 kW IPM Synchronous Machine passively air-cooled	115 V 500 A_{RMS}	Li-Ion 4.16 kWh 75.6 V nom

¹ Assumed as inverter was mentioned in sources but no DC/DC converter

² Motor power refers to peak power, energy storage capacity to nominal capacity, as shown in equ. 4.1 and 4.2

Sources: [10], [11], [12],[13], [14], [15], [16], [17], [18]

which participates in a different competition. Two different powertrain architectures are encountered for the motorcycles of table 4.1, which are illustrated in fig. 4-1. Most motorcycles presumably utilize architecture (a), with a direct connection of the battery to the DC-Link. As the MS6 prototype is the only prototype known to use an intermediate DC/DC converter, this will be further investigated in the performance analysis.

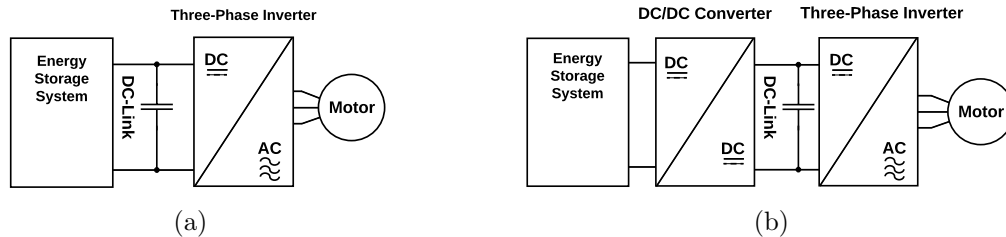


Figure 4-1: Powertrain architectures of electric racing motorcycles

4.2 Powertrain of the MS6 Prototype

In 2019/2020, the MotoStudent team Wolfast from the University of Oviedo changed from the combustion competition to MotoStudent electric. As the commercial manufacturers naturally withhold detailed information, the first electric prototype of the team Wolfast from the season 2019/2020 serves in this chapter as an example to introduce the subsystems and explain the global impact of them. To provide a foundation for the main chapter, the technical correlations of the subsystems are elaborated and the relevant equations are presented. The powertrain of the MS6, depicted in fig. 4-2, consists of a Li-ion battery storage, a DC/DC converter, a two-level three-phase DC/AC converter and an Interior Permanent Magnet (IPM) synchronous motor. In the following, the individual elements are described in more detail.

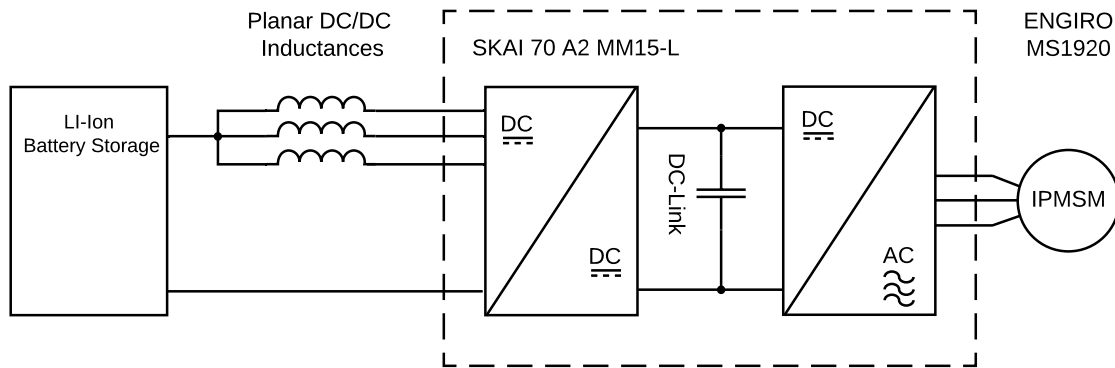


Figure 4-2: Powertrain architecture MS6 prototype

4.2.1 Battery Pack

As Li-ion is undoubtedly the dominant battery technology in today’s EV market, the majority of manufacturers use Li-Ion batteries as primary energy storage. What distinguishes the batteries of the big players is the cell chemistry and the cell type. The cell chemistry is mostly characterized by the positive electrode, the anode. Typical anode materials are Lithium Nickel Manganese Cobalt Oxide (NMC), for instance used in the BMW i3, and Nickel Cobalt Aluminium Oxide (NCA), employed in the Tesla model 3 [19].

In the MS6 prototype, the battery consists of a total of 462 cylindrical 18650 Li-Ion cells with NCA as anode material. The specifications of a single cell are the following:

Table 4.2: Specifications of a single INR18650-25R cell

Name	C_{nom} [mAh]	V_{nom} [V]	$I_{discharge,max}$ [A]	$C-rate_{max}$	ESR [m Ω]
INR18650-25R	2500	3.6	20	8	25

In table 4.2, the nominal capacity C_{nom} refers to the extractable energy at a discharge rate of 0.2 C. The equivalent series resistance ESR specifies the typical DC series resistance of the cell.

The battery pack of this year’s motorcycle MS6 is structured as depicted in fig. 4-3. Each module comprises of seven series and eleven parallel cells (fig. 4-3 (a)). Six of these modules, arranged as illustrated in fig. 4-3 (b), form the complete battery pack.

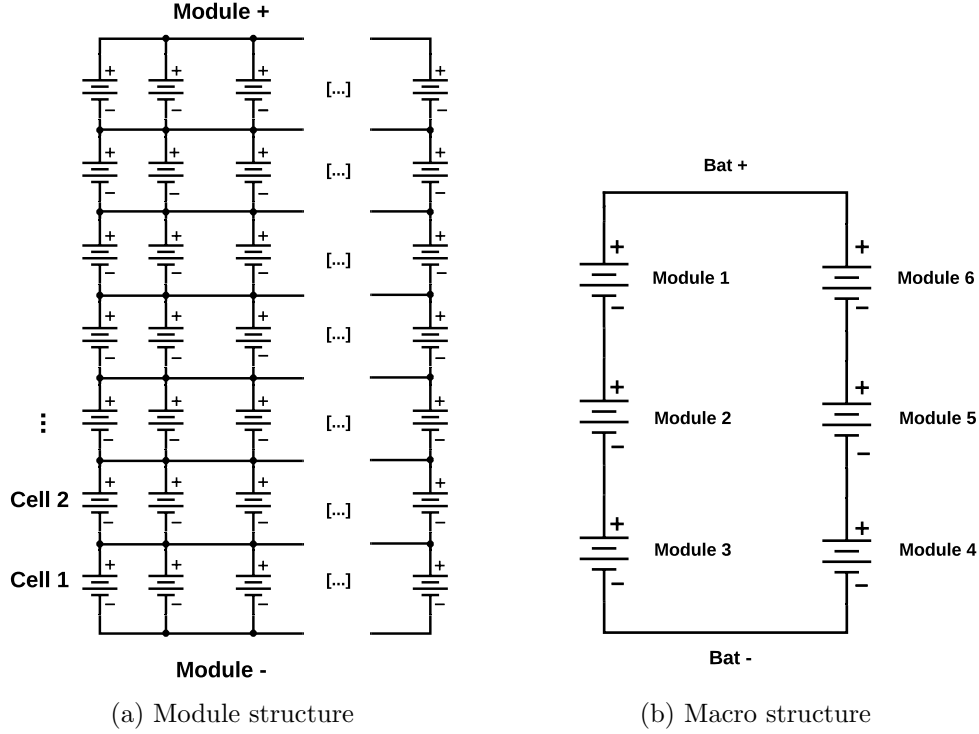


Figure 4-3: Battery pack design MS6 prototype

The capacity value of a battery pack, conventionally given by manufacturers in kW/h, is calculated, as shown in the following equations. It refers to the available energy, extracted at a specific C-rate. In the formula, C_{cell} depends on the chosen C-rate.

$$C_{bat}[kWh] = N_{tot} \cdot \frac{C_{cell}[Wh]}{1000} \quad (4.1)$$

with

- N_{tot} being the total number of cells.
- C_{cell} [Wh] being defined as:

$$C_{cell}[Wh] = V_{nom,cell} \cdot \frac{C_{cell}[mAh]}{1000} \quad (4.2)$$

The nominal power of the battery pack P_{nom} is determined through the number of series cells N_s and the number of parallel cells N_p according to:

$$P_{nom} = (V_{nom,cell} \cdot N_s) \cdot (I_{max,cell} \cdot N_p) \quad (4.3)$$

In equ. 4.3, the maximum current of the cell $I_{max,cell}$ refers to the maximum current that can be extracted while staying within the electrical and thermal limits. The latter heavily depends on the cooling system of the battery pack. Altogether the battery pack of the MS6 yields the following specifications:

Table 4.3: Specifications of the MS6 battery pack

	C_{nom} [kWh]	V_{nom} [V]	$I_{discharge,max}$ [A]	P_{nom} [kW]	ESR [mΩ]
MS 6 Bat. pack	4.16	75.6	440	33.26	23.86

4.2.2 DC/DC Converter

The powertrain of the MS6 Motorcycle utilizes a bidirectional DC/DC converter, which is illustrated in fig. 4-4. The DC/DC converter can increase the voltage if the power flow is from the battery to the DC-Link (Boost operation) and decrease the voltage if the power flow is reversed during regenerative braking (Buck operation). The DC/DC converter is built with three interleaved planar inductors, each capable of handling current up to 133 A. The advantage of an intermediate DC/DC Converter is the gained degree of freedom for the DC-Link voltage. In chapter 4.3, the effect of the DC/DC converter on the performance will be elaborated in more detail.

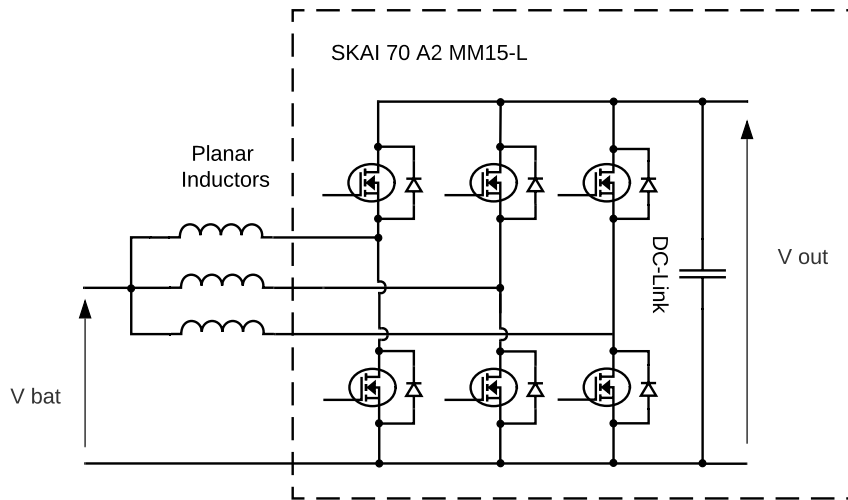


Figure 4-4: Interleaved DC/DC converter using three legs of the SKAI 70A2 MM15-L

4.2.3 Three-phase DC/AC Converter

The three-phase DC/AC converter consists of the other three legs of the SKAI 70 A2 MM15-L and is referred to as inverter hereinafter. It transforms the DC-Link voltage through Pulse-Width Modulation (PWM) into the desired three-phase voltages with sinusoidal fundamental at variable frequency.

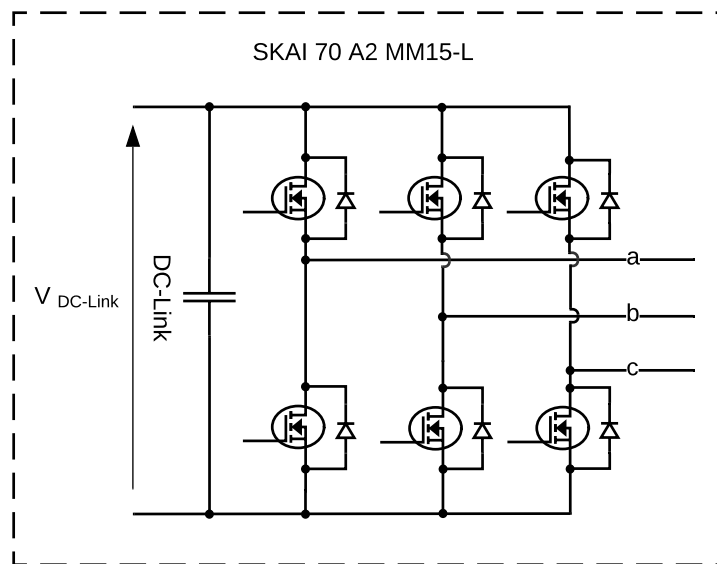


Figure 4-5: Three-phase two-level DC/AC converter using the remaining three legs of the SKAI 70A2 MM15-L

When the complete system constraints are evaluated, the inverter's current limit and maximum AC voltage play an essential role. The current limit is usually given as phase current limit and is derived from the maximum chip temperature of the semiconductor, thus depends on losses and the thermal system. Tab. 4.4 provides an overview of the specifications of the SKAI 70 A2 MM15-L.

Table 4.4: Maximum specifications of SKAI 70 A2 MM 15-L

Name	I_{phase} (cont.) [A]	I_{phase} (10 s) [A]	$V_{DC-Link}$ [V]	f_{sw} [kHz]
SKAI 70 A2 MM15-L	140	500	115	16

¹ Current ratings refer to Root Mean Square (RMS) quantities

The maximum achievable phase-to-neutral voltage amplitude $\hat{V}_{Ac,ph-n}$ of the AC voltage depends on the DC-Link voltage and the type of modulation. Several operating regions can be distinguished as illustrated in fig. 4-6.

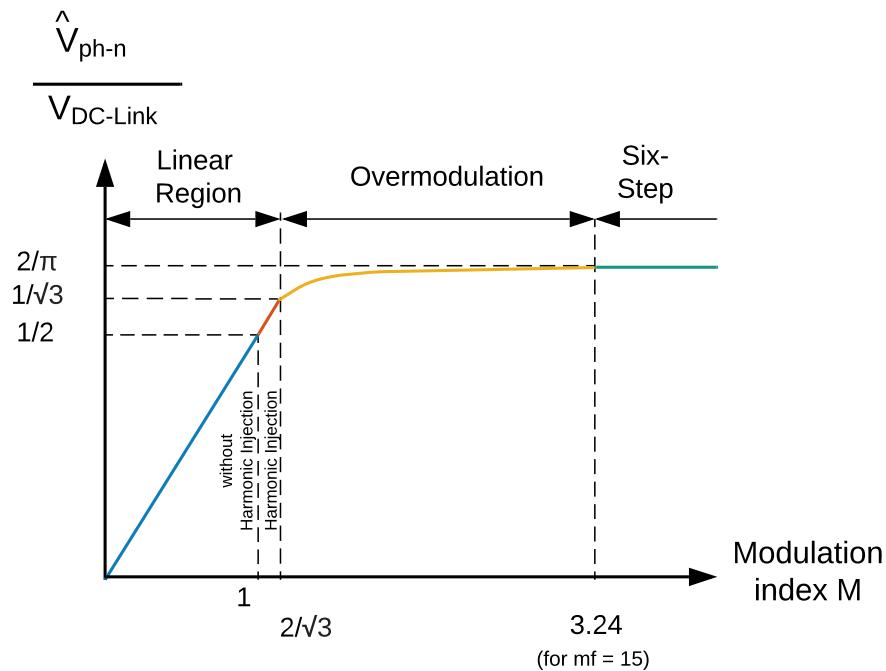


Figure 4-6: Maximum phase-neutral voltage amplitude in dependency of modulation index, adapted from: [1]

The modulation index M on the x-axis is calculated by

$$M = \frac{\hat{V}_{Ac,ph-n}}{V_{DC-Link}/2} \quad (4.4)$$

Through sinusoidal PWM, created with sine-triangle modulation, the maximum achievable voltage is $\frac{V_{DC}}{2}$, corresponding to a modulation index $M = 1$. The linear region can be extended to $\frac{V_{DC}}{\sqrt{3}}$ by using either the sine-triangle modulation with Third Harmonic Injection (THI) or Space Vector Modulation (SVM). Entering the overmodulation allows a further increase of fundamental AC amplitude, at the cost of higher Total Harmonic Distortion (THD). Eventually the highest fundamental amplitude is reached at $\frac{2V_{DC}}{\pi}$ in six-step operation [1], [20], with highest THD.

From a system point of view, the impact of the maximum phase-neutral voltage amplitude $\hat{V}_{Ac,ph-n}$ and the corresponding modulation index is of interest. These inverter parameters play an essential role for the motor control strategy and thus, motor performance. In the following chapter, the motor is introduced and the motor-inverter relation is explained.

4.2.4 Internal Permanent Magnet Motor

The heart of the powertrain consists of an IPM, provided to all teams by the Moto-Student organisation and mandatory to use by regulation.

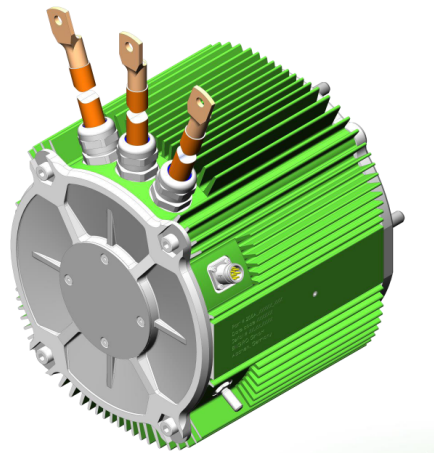


Figure 4-7: IPM Machine "ENGIRO-MS1920", source: [2]

The electric machine is an air-cooled synchronous motor designed for the high current architecture of the MotoStudent motorcycles. The defining characteristic of an internal permanent magnet motor is the magnetic anisotropy. Magnetic anisotropy describes the phenomenon that the magnetic reluctance opposing the stator magnetomotive force is rotor angle-dependent or, expressed in the parameters of the synchronous reference frame, $L_q > L_d$.

The motor is specified by the following parameters:

Table 4.5: Maximum specifications of ENGIRO MS1920 motor

Name	T [Nm]	I_{phase} (cont.) [A]	I_{phase} (10 s) [A]	n [rpm]	n_{base} [rpm]	Pole Pairs
ENGIRO MS1920	95	156	781	8000	4000	4

¹ Current ratings refer to RMS quantities

In order to relate the inverter's output voltage limit to motor quantities, the Back Electromotive Force (BEMF) is introduced. The underlying theory for the following analysis and clarifications of the utilized RMS-convention for the synchronous reference frame are given in appendix A.

Generally speaking, the BEMF describes the voltage in the stator windings, related to a change of the flux linked with them. It can be calculated as the vector sum of v_d and v_q . The following analysis is carried out in steady-state condition, thus there is no change in Ψ_d or Ψ_q . In this condition, the BEMF is calculated by:

$$|V_{BEMF}| = \sqrt{v_d^2 + v_q^2} = \sqrt{[R_s \cdot i_d - \omega_e \cdot \Psi_q]^2 + [R_s \cdot i_q + \omega_e \cdot \Psi_d]^2} \quad (4.5)$$

Neglecting stator resistance R_s and inserting Ψ_d and Ψ_q yields:

$$|V_{BEMF}| = \sqrt{[\omega_e \cdot L_q \cdot i_q]^2 + [\omega_e \cdot (L_d \cdot i_d + \Psi_{PM})]^2} \quad (4.6)$$

Getting back to the connection of motor and inverter as mentioned in chapter 4.2.3, the BEMF can be related with $V_{Ac,ph-n}$ according to:

$$V_{Ac,ph-n} = |V_{BEMF}| \cdot \sqrt{2} \quad (4.7)$$

Conventionally, the inductances and their current dependencies of the motor are measured through a test-bench setup. As this measurement could not yet be performed, the inductances are calculated through the motor control map, provided by the manufacturer.

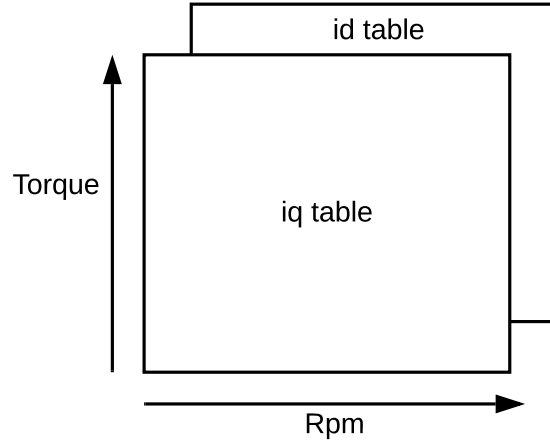


Figure 4-8: Illustration of motor control map

The motor control map contains the current vector components i_q , i_d in dependency of torque and motor speed, as illustrated in fig. 4-8.

Through equ. 4.5 and equ. A.10, the inductance as a function of the current can be calculated for the operating points, where field weakening is assured. In these operating points, the following condition, corresponding to the maximum M of 1.154 is assumed:

$$\frac{V_{bat}}{\sqrt{3}} = |V_{BEMF}| \cdot \sqrt{2} \quad (4.8)$$

The battery voltage at which the motor control map is valid is given as $V_{bat} = 96V$. Solving the equations yields the current dependency of L_q , L_d as shown in fig. 4-9.

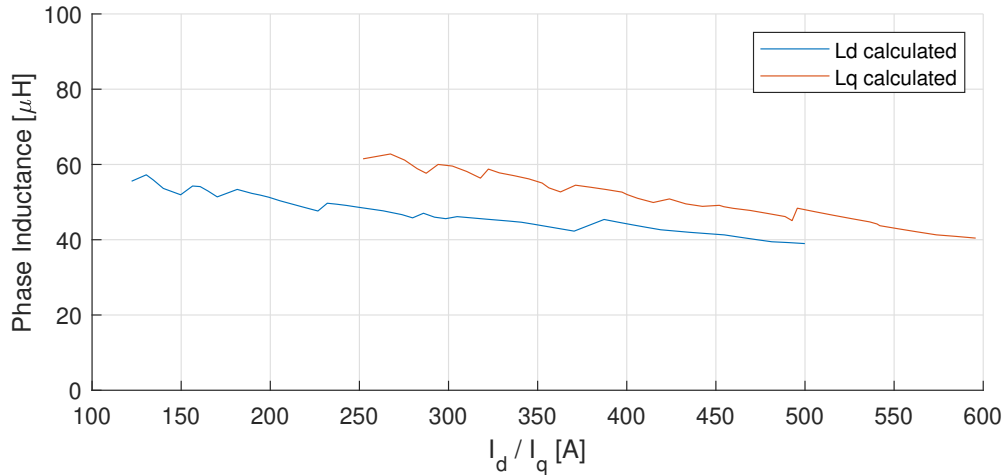


Figure 4-9: L_d , L_q in dependency of I_d / I_q (RMS-values)

These approximated inductances are used in the further development of this thesis, where relevant.

4.3 System Performance Analysis

The performance of the electric motorbike is evaluated at the final MotoStudent competition through several tests. For the electric powertrain, the strongest requirements are tested in the race (6 laps with an approximate distance of 30.5 km) and the acceleration event, with the goal to complete 150 m as fast as possible. The system is currently designed to achieve the best time in the race while staying within the thermal limits of the system. In order to improve the acceleration of the motorcycle, the peak performance, required for around 10 s, is analyzed in more detail.

As a foundation for this analysis, the maximum admissible torque is calculated for each individual system component in dependency of motor speed. It is to be noted that the following evaluation is carried out, neglecting losses in the powertrain and using idealizations for simplicity. Nevertheless, it allows an impression of the system limits and the deduction of a preliminary guideline for the system design. When a design is finalized, losses and more complex equations, e.g., for the field weakening region, could be adopted.

The maximum allowable torque, based on the maximum battery power can be calculated by:

$$T_{max,ESS} = \frac{P_{max,ESS}}{\omega_r} = \frac{V_{bat} \cdot I_{max,ESS}}{\omega_r} \quad (4.9)$$

The ESS consists of the battery and the DC/DC converter. Consequently, the dominant current limit, thus the lower current limit of battery and DC/DC converter, has to be considered. In the case of the MS6 motorcycle, the interleaved inductors of the DC/DC converter are the bottleneck with a maximum current of 400 A.

In order to calculate the limits associated with the inverter, a slightly different approach is utilized. The relation between motor torque and phase current is commonly described through the torque constant k_t defined in equ. 4.10.

$$k_t = T_{mot}/I_{phase} \quad (4.10)$$

This constant depends on multiple factors, including temperature, saturation of phase inductances and iron losses [21]. The torque constant at the maximum inverter RMS phase current of 500 A can be extracted through the motor map. Thus the maximum torque associated with the inverter can be calculated by

$$T_{max,Inv} = k_t \cdot I_{max,Inv} = 0.14 \cdot I_{max,Inv} \quad (4.11)$$

The maximum motor torque in dependency of speed is modeled through an approximation, considering constant torque and constant power region. To include the effect of several DC-Link voltages on the field weakening region, the normalized base speed $\omega_{base,norm}$ is introduced.

$$\omega_{base,norm} = \frac{V_{DC-link}}{V_{nom}} \cdot \omega_{base} \quad (4.12)$$

V_{nom} corresponds to the nominal DC-Link voltage at which ω_{base} , the start of the field weakening region, was determined. Both values are provided by the motor manufacturer.

The reduction of available motor torque in the field weakening region is modeled as seen in equ. 4.13

$$T_{max,Mot} = \begin{cases} T_{max} & \text{if } \omega < \omega_{base, norm} \\ T_{max} \cdot \frac{\omega_{base, norm}}{\omega_r} & \text{if } \omega \geq \omega_{base} \end{cases} \quad (4.13)$$

ω_{base} refers to the angular rotor speed where the field weakening region begins and T_{max} to the maximum torque in the constant torque region.

Plotting the limits all together yields the complete system limits according to

$$T_{max, System} = \min(T_{max, ESS}; T_{max, Inverter}; T_{max, Mot}) \quad (4.14)$$

In fig. 4-10, the system limits are plotted twice for different State of Charge (SOC) levels of the battery. The left graph depicts the situation for a fully charged battery, the right illustrates the empty state of the battery, thus significantly lower battery voltage. As a DC/DC is employed in the powertrain, the DC-Link Voltage V_{dc} is kept constant at 115 V.

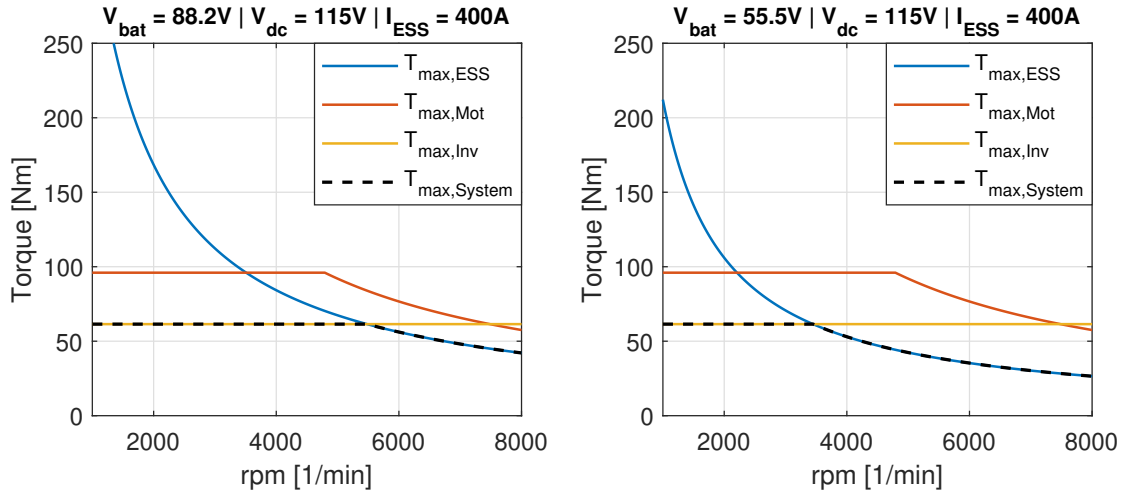


Figure 4-10: System limitations of the MS6 prototype in fully charged battery state (left) and empty battery state (right)

The plot demonstrates that the inverter torque limit is the dominant limit in the lower speed regions.

As the admissible torque by the Energy Storage System (ESS) decays inversely proportional to the speed, it becomes the dominant limit at a certain speed.

In terms of the system design, the DC/DC converter enables the decoupling of battery voltage and DC-link voltage, which corresponds to a horizontal shift of the $T_{max,Mot}$ curve and increases the constant torque region according to equ. 4.13. For reference, fig. 4-11 shows the limitation of the MS6 prototype if no DC/DC converter would be implemented.

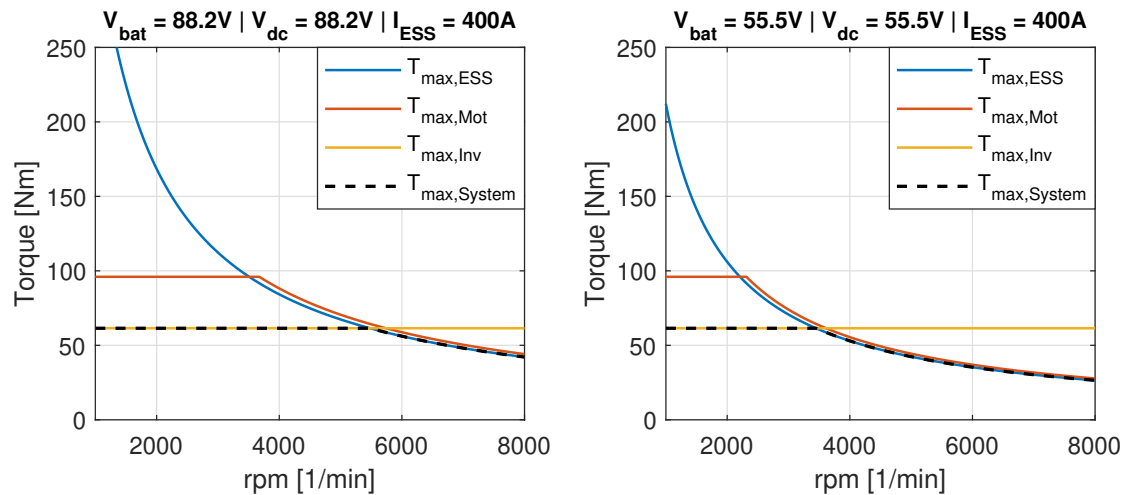


Figure 4-11: System limitations of the MS6 powertrain architecture without DC/DC converter in fully charged battery state (left) and empty battery state (right)

As can be seen from 4-11, the battery is still the dominant torque limit in the higher speed regions, even without a DC/DC converter.

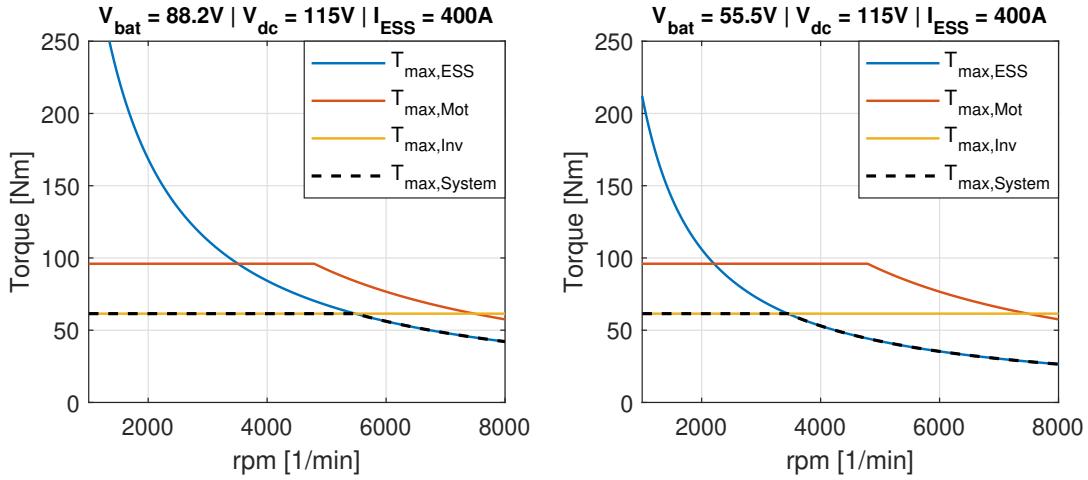
4.4 Roadmap Future Seasons

The main limiting factors of the current system were derived from fig. 4-10. As a first point, the inverter limits the torque at the lower speed regions. An inverter with higher current rating could significantly improve the torque up to the maximum torque of the motor in the lower speeds and therefore improve the acceleration of the motorcycle. A second point is the voltage and power rating of the battery, which involves the question if a DC/DC converter should be implemented. As long as the motor torque is not the dominant limit, a DC/DC converter cannot increase the overall system torque. Consequently, an evaluation of the dominant limit is carried out, whether a DC/DC converter maintains advantages when the battery is increased to a voltage of 121.8 V, which represents the maximum number of series cells while staying safely within the regulatory limit of 126 V. The result is visible in fig. 4-12, which will be explained in the following and serves as a roadmap for upcoming seasons. For clarification the configurations are quickly described in the following:

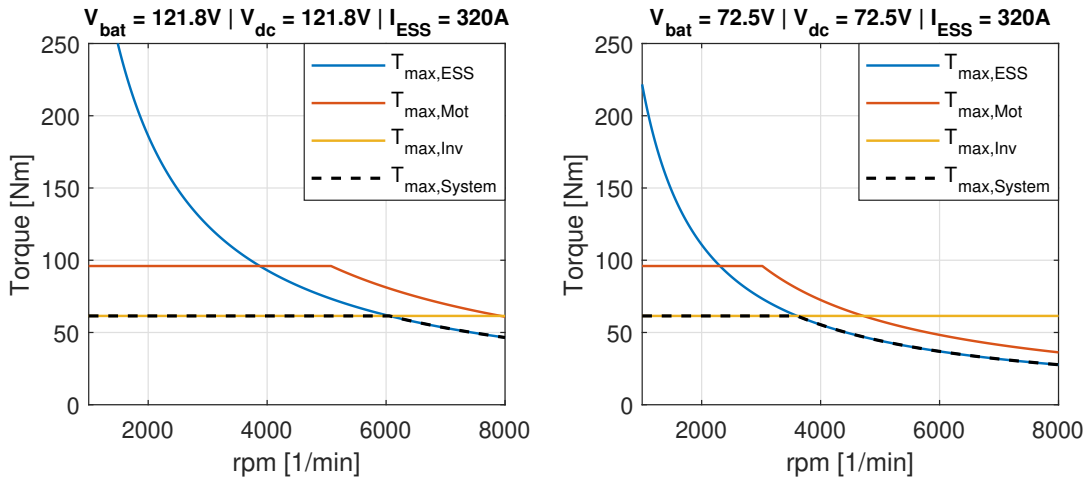
- Configuration I: Current state of the powertrain architecture
- Configuration II: Removal of DC/DC converter, increase of battery voltage
- Configuration III: Increase of inverter current capability

Step 1: Configuration I → Configuration II

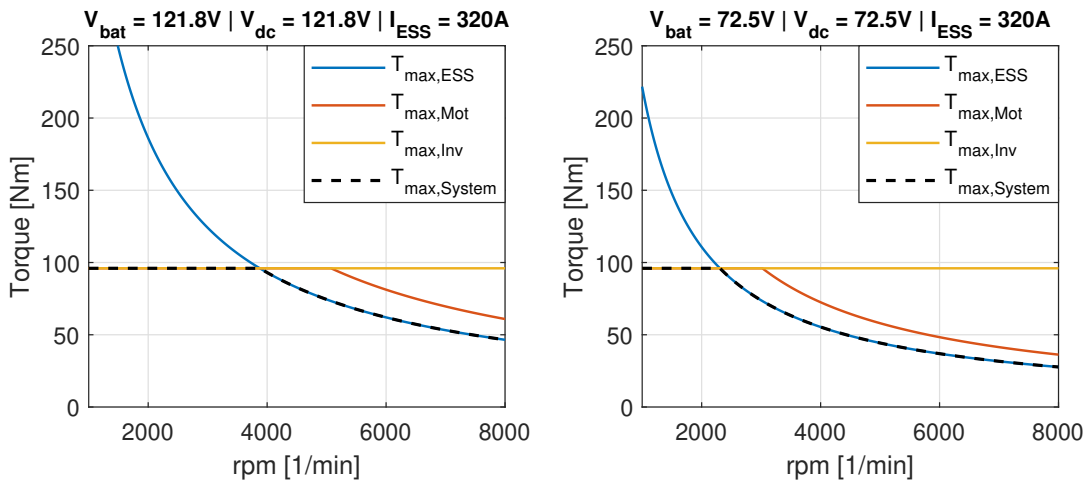
The first step includes the increase of nominal battery voltage, thus an increase of series cells while the current is reduced (corresponding to a reduction of parallel cells) to keep the volume constant. As shown in the plots of configuration II for both full and empty battery state, the inverter limits the torque in the lower speed regions and the battery in the higher speed regions. The motor is at no point the dominant limit. In this case, a DC/DC cannot increase the performance at any point. In return, this means that the setup of configuration II works well without an intermediate DC/DC converter. Generally, a higher power of the ESS, which consists only of the battery in



(a) Configuration I



(b) Configuration II



(c) Configuration III

Figure 4-12: Roadmap system design

configuration II, would be desirable to further improve the performance. However, this corresponds to an increase of parallel battery cells, which currently cannot be achieved due to volume constraints. The new battery design of configuration II contains 464 cells in comparison to 462 of the old design, thus approximately matches the volume. If any additional space could be assigned to the energy storage in future seasons, the battery power could be further increased. Of course, this represents a trade-off between increased torque capability and additional weight.

Step 2: Configuration II → Configuration III

Step two deals with the design of an inverter with an increased current rating. A RMS current rating of 780 A, however, represents an extremely high current for the low system voltage and no commercial inverter is specifically designed for these system ratings. As no experience in inverter development exists within the team yet, chapter 6 investigates an intermediate design, making use of GaN semiconductors with a desired current rating of $500 A_{RMS}$. This design serves as a foundation for the future goal of a GaN inverter with a current rating of $780 A_{RMS}$.

Chapter 5

Advanced Energy Storage - Evaluation of Hybrid Systems

5.1 Objective and Methodology

A significant part of the total costs, weight and volume of an electric vehicle comes from the energy storage system. Consequently, a lot of research attention is drawn by this subsystem with the aim to drive down the price and increase gravimetric and volumetric density. In motorsport applications, the costs of the prototype are usually not the primary design priority, however, reducing the weight and volume is essential for a competitive design.

The objective of this chapter is to evaluate the usage of a HESS and its potential to improve volumetric and gravimetric density. The analysis considers the implementation of a HESS, consisting of Li-Ion cells and UCs, and compares it to a pure battery ESS. In order to allow a realistic comparison, actual component data of different commercially available cylindrical Li-Ion cells and single-cell UCs serves as underlying database. As a first step, the fundamentals of UCs are revised and terminology and conditions of the analysis are clarified. In a second step, the database is introduced and the UC and Li-ion cells are compared in terms of their densities. The next section highlights the characteristics of the load profile. Afterwards, the common HESS architectures found in literature are reviewed and analyzed regarding

eligibility. Considering the established background, the HESS design optimization algorithm is explained and results are discussed and evaluated.

5.2 Fundamentals of Ultracapacitors

As ultracapacitors are introduced, some words are spent to explain the naming conventions and establish clarity. While reading about ultracapacitors, several different names can be encountered, which might lead to confusion at first. Essentially, double-layer capacitor, supercapacitor and ultracapacitors are interchangeable terms and mean the same [22]. In this thesis, these types of capacitors are referred to as ultracapacitors (UCs).

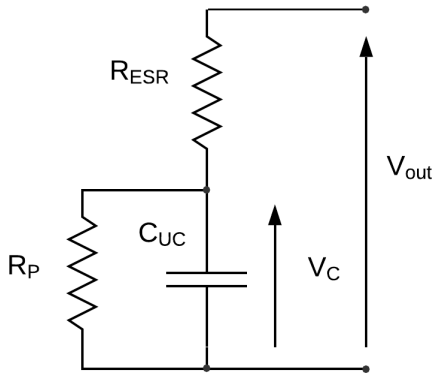


Figure 5-1: Equivalent circuit of UC including ESR with R_{ESR} and leakage Resistance R_P

A fundamental difference between capacitors and batteries is the form in which energy is stored. Batteries utilize chemical energy, while capacitors store energy in the electric field between the electrodes. In UCs, the double-layer capacitance stems from the interface of the solid electrode material surface and the liquid electrolyte situated in the micropores of the electrodes. Using the double-layer capacitance enables much higher capacitance values than other capacitor types [23].

The energy stored in an ultracapacitor can be calculated by

$$E_{UC} = \frac{1}{2} \cdot C \cdot V_C^2 \quad (5.1)$$

Extracting the nominal energy of a UC corresponds to a change of voltage until theoretically zero. Evaluating the power and energy density of UCs is not trivial, though. Manufacturers often provide the value for the maximum power in matched impedance condition. In this condition, exactly 50 % of the energy is transferred to the load and the other half is dissipated in the capacitor's ESR. For the operation in EVs, this is not a suitable discharge, as energy efficiency is poor and high losses would have to be dissipated through the thermal system.

With equ. 5.2, the author of [22] provides a more general calculation of the discharge power as a function of the discharge efficiency, which is valid for a constant power discharge until $V_{out} = V_{nom}/2$.

$$P_{UC} = 9/16 \cdot (1 - \bar{\eta}_{UC}) \cdot \frac{V_{nom}^2}{R_{ESR}} \quad (5.2)$$

Inherently, the equation considers the reduction of voltage in the UC during this discharge. Equ. 5.2 relates the discharge power and efficiency, however, the extractable energy for a discharge at a certain power, remains unknown. Literature in [23], [22] only mentions the usable voltage range until $V_{nom}/2$ for equ. 5.2, without any further elaboration. Thus the constant power discharge of an UC at $\bar{\eta}_{UC} = 90$ % is analyzed in more detail through a numerical simulation, seen in fig 5-2.

In the simulation, the effective voltage of the capacitance V_C and the terminal voltage V_{out} is given throughout the discharge. The simulation demonstrates that during discharge, the capacitor voltage decays nonlinearly. As the voltage decreases, the current rises to keep power constant. At the point where the equivalent load resistance equals the ESR of the UC, the system becomes unstable, current increases exponentially and the discharge cannot be maintained. The usable voltage in this example is approximately $V_{nom}/3$ and thus varies significantly from the literature value $V_{nom}/2$.

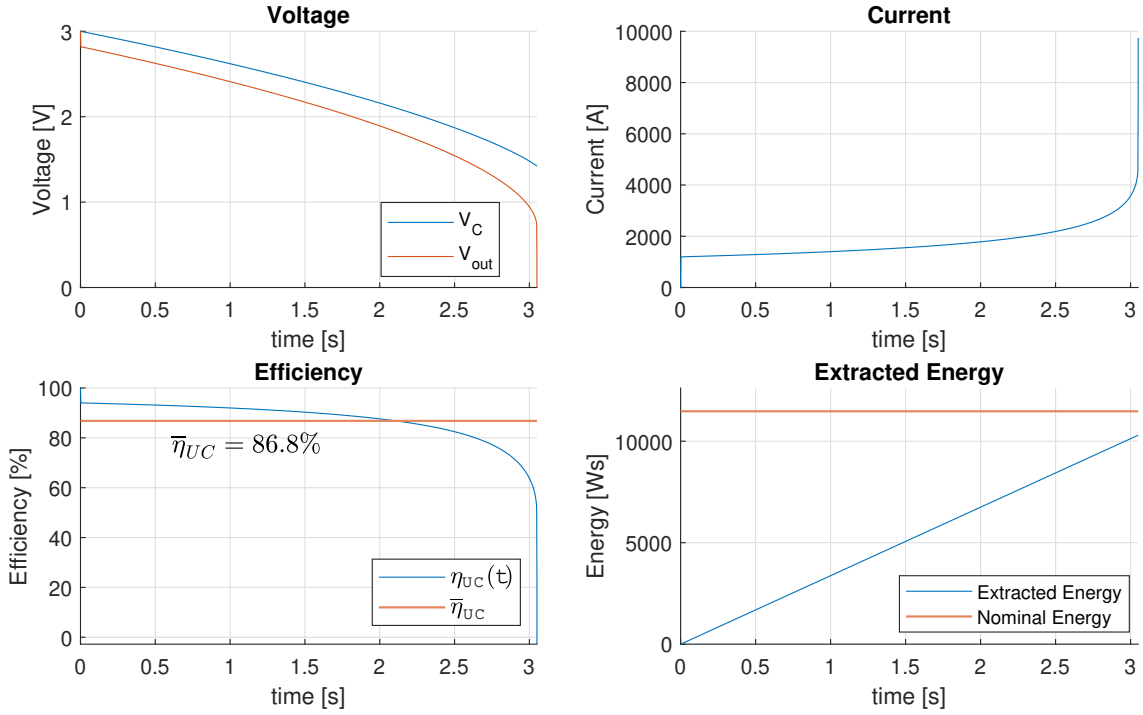


Figure 5-2: Constant power discharge of UC

Fig. 5-3 compares the constant power discharge for two different power levels. The calculated power, according to equ. 5.2 is 3.375 kW for a discharge with an efficiency of 90 %, and 10.125 kW for a discharge efficiency of 70 %. It is evident that the usable voltage range is completely different for the two scenarios. Juxtaposing the extractable energies, points out a significant difference in dependency of the discharge power. The remaining energy in the capacitor is still available, however, cannot be extracted at the desired power level [24], [25].

If the discharge efficiency is neglected, the absolute minimum discharge voltage of the UC can be calculated according to equ. 5.3 given in [26].

$$V_{out,cutoff} = 2 \cdot \sqrt{P_{UC} \cdot R_{ESR}} \quad (5.3)$$

In the further development of this thesis, the usable voltage range will be determined through equ. 5.3 and an added tolerance to maintain stability. The optimization algorithm will filter HESS design for which P_{UC} exceeds the value calculated with

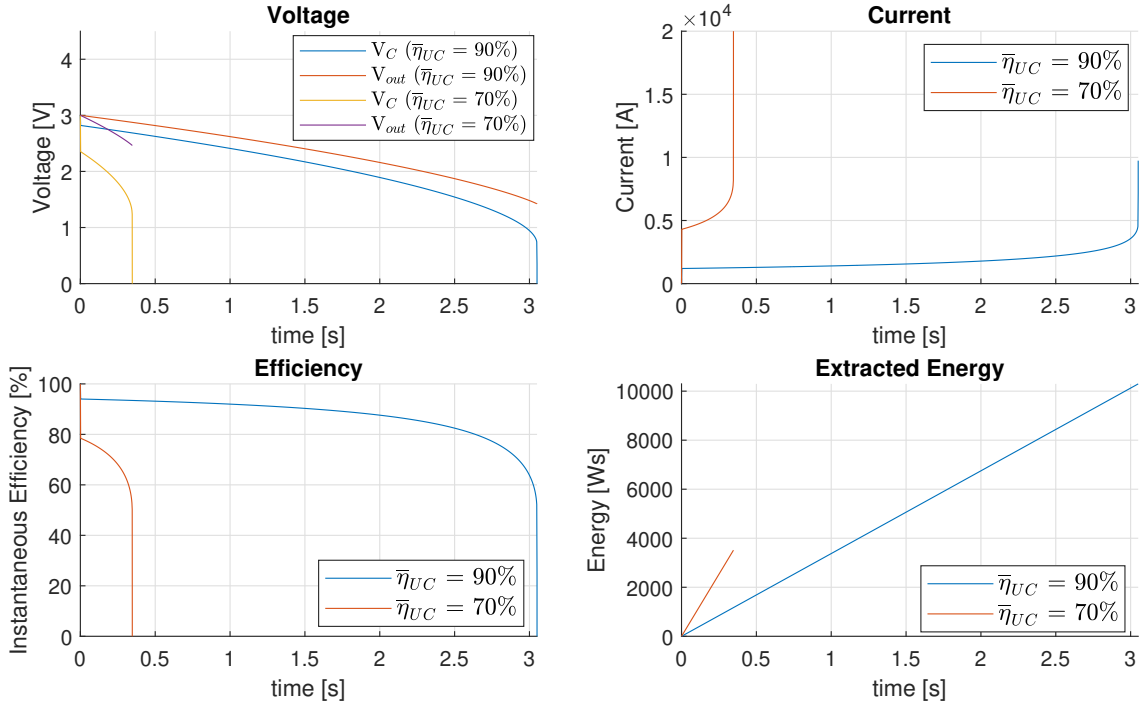


Figure 5-3: Comparison of constant power discharge at $\bar{\eta}_{UC} = 70 \%$ and $\bar{\eta}_{UC} = 90 \%$

equ. 5.2 for $\bar{\eta}_{UC} = 70 \%$, due to previously mentioned reasons of energy efficiency and thermal considerations. Furthermore, this chapter demonstrated the importance of the UCs Equivalent Series Resistance (ESR) regarding discharge limit and stability. As a consequence, it is included in all powerflow simulations in this thesis.

5.3 Volumetric Density of State-of-the-art Li-Ion Cells and Ultracapacitors

A common approach to comparing different types of energy storage is a plot, illustrating power density against energy density. If specific densities are used, thus the power and energy per weight, this plot is referred to as Ragone plot [27].

In the MS6 prototype, the volume is one of the most critical parameters of the energy storage, thus the volumetric densities will be analyzed in addition. As UCs and Li-Ion cells have shown rapid improvements in the last decades, a database of state-of-the-art components is created for this thesis. The database includes common

cylindrical 18650 and 21700 Li-Ion cells and single-cell UCs from various manufacturers. Since the cylindrical Li-Ion cells from different manufacturers exhibit great similarities per model, the plot is limited to a single manufacturer. Naturally, similar cells of other manufacturers could replace them.

With reference to the previous chapter, which explained the trade-off between power and extractable energy of UCs, it should be highlighted that a Ragone plot of UCs should state the corresponding discharge efficiency of UCs to be distinct. In fig. 5-4, for instance, the power density refers to a discharge efficiency of 70 %.

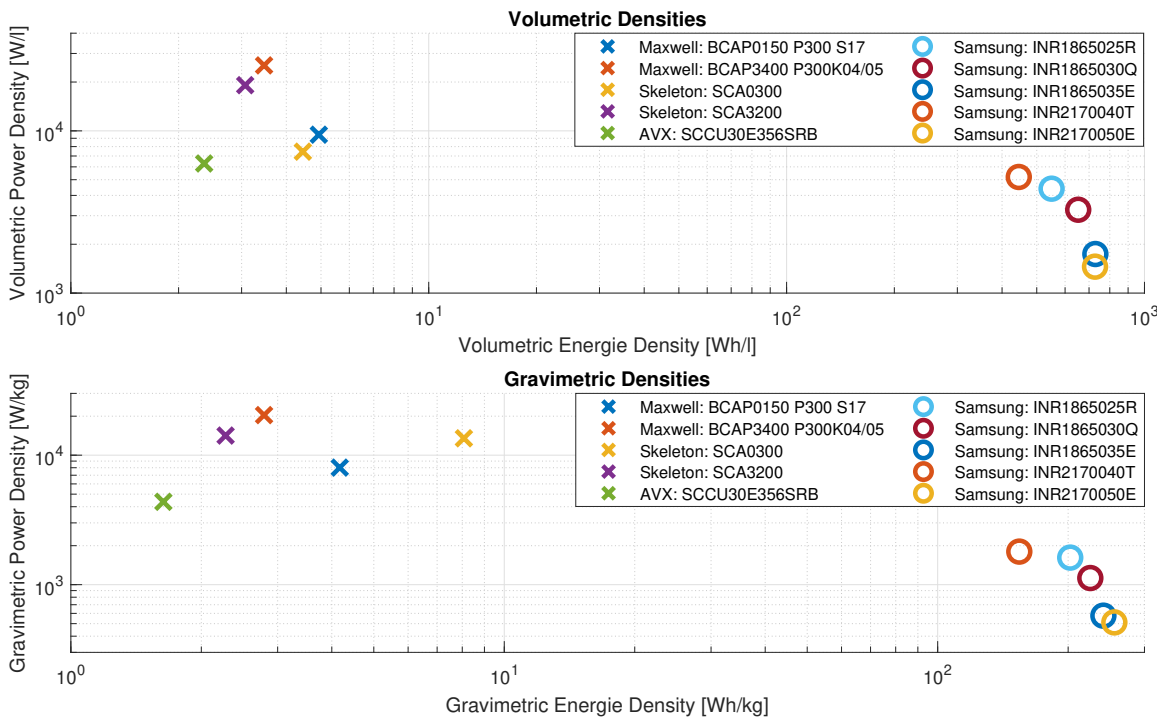


Figure 5-4: Volumetric/gravimetric power and energy densities of state-of-the-art Li-Ion cells and UC cells ($\bar{\eta}_{UC} = 70\%$)

The graph illustrates that the characteristics of Li-Ion cells vary a lot between different models. The battery cell design is eventually a compromise of energy and power capability of the cell. Generally speaking, Li-Ion cells provide relatively high energy density and low power density. Literature often distinguishes between energy and power cells, depending on the side of the spectrum they are designed for. UCs, on the other side, prove high power densities paired with significantly lower energy

density than Li-Ion cells. Comparing the UC cells with each other reveals big differences in power densities and energy densities. At this point, it is difficult to predict which cell is most suitable for a HESS. As a consequence the evaluation will consider all introduced models.

5.4 Energy Storage System Requirements

The design process of any ESS strongly relies on a realistic load power profile, which represents a combination of static and dynamic requirements. Obtaining this profile, however, is not trivial, if no measured data is available.

In the Wolfast MotoStudent team, the load profile originates from an emulated race trajectory. The race trajectory is created by a mechanical simulation and takes the physical constraints, e.g., applicable torque to the rear wheel, curve speed and maximum continuous power of the motor into account.

Fig. 5-5 shows the complete drive cycle of a race. The first lap, separated by the first vertical line, is the warm-up round. The second lap represents the first launched lap of the race, starting from a speed of zero. In the following five launched laps, consecutive race laps are displayed. The last lap is the so-called honor lap with low speed and torque requirements.

The torque profile of fig. 5-5 contains strong fluctuations between accelerations and braking maneuvers, characteristic for the motor sport environment. The load power of the ESS is derived from the mechanical power calculated through:

$$P_{ESS}(t) = P_{mech}(t) \cdot \eta_{Powertrain} \quad (5.4)$$

in which $\eta_{Powertrain}$ accounts for operating point dependent:

- Motor copper losses (measured phase resistance).
- Inverter conduction losses (formula provided by Semikron).
- Inverter switching losses (formula provided by Semikron).

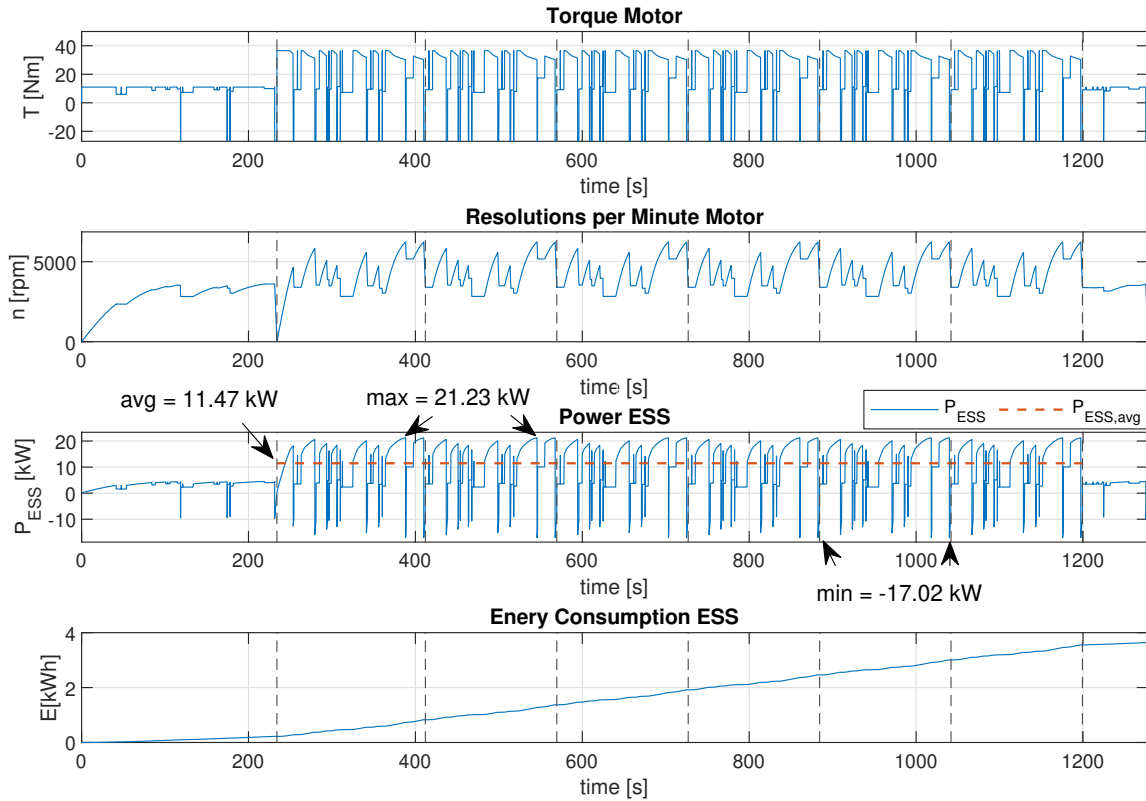


Figure 5-5: Torque, speed and power graph of the drive profile

Two points should be highlighted when analyzing the performance of the ESS:

1. In the race laps, peak power exceeds average power by a factor of 1.85.
2. During regenerative braking, the negative peak [-17.02 kW] reaches almost the positive peak power in motoring operation [21.23 kW].

In order to support such a driving profile, pure battery storage has to be designed for the peak power. As explained in chapter 5.3, Li-ion batteries are available as energy or power cells. Power cells characterize themselves by high power density but relatively low energy density for Li-ion batteries. The properties of energy cells are the opposite. Due to the high peak power requirement, the most compact design of a battery-only ESS favors the power cells for a profile as shown and cannot take advantage of cells with higher energy density.

5.5 Hybrid Energy Storage

This chapter discusses a hypothetical scenario in which a second type of energy storage is introduced to the system. The new storage element is able to provide the complete power fluctuations, or in other terms, the reactive power of the profile. Consequently, the battery storage only has to supply the average power, which is a decrease of over 50 % of the power requirement for the drive cycle of fig. 5.4. The hypothetical scenario describes the trade-off, an additional storage component, like an UC, introduces. The long term energy storage, in this case the Li-Ion battery, can utilize more energy-dense cells, which reduces the total number of cells necessary to fulfill the energy requirement. Evidently, the short-term storage element introduces additional volume, weight, cost and complexity to the system.

The question of whether the hybridization can improve the overall volumetric and gravimetric density depends on several factors. To start with, various ways of interconnecting the two energy storage types exist. In order to select the most suitable topology, the next chapter provides a review of hybrid energy storage topologies. The different topologies will be evaluated regarding their eligibility for the previously introduced load profile.

5.5.1 Topologies

The various topologies of a HESS differ by the position and interface of UC-pack and battery to the DC-link. The energy storage devices can be connected passively, as a direct electrical connection, or actively through a power converter. Depending on the type of connection, the power flow of battery, UC or both can be controlled at the expense of additional power electronics.

In the following, the topology is referred to as passive, if a direct electrical connection of both storage types to the DC-link is utilized. Semi-active topologies represent the architectures, in which one storage type is interfaced with a power converter and the other one passively. The architecture is addressed as active topology if both storage types are interfaced with a power converter.

As demonstrated in chapter 5.2, the utilization of the UC strongly depends on the minimum voltage of the UC. Thus the allowable voltage drop of the UC will be highlighted in the evaluation of the different topologies.

Passive Connection

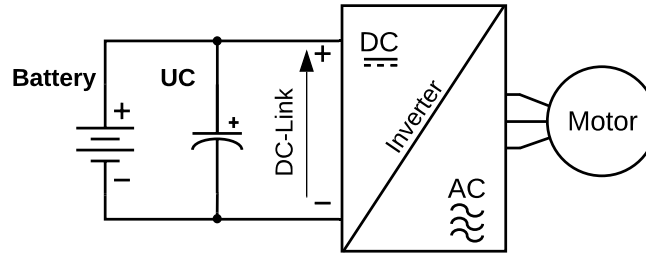


Figure 5-6: Passive HESS topology, adapted from [3]

Both battery and UC are directly connected to the DC-link. This represents the easiest connection of both energy storage devices, however offers the fewest controllability. The power flow is purely determined by the impedance of UC and battery and the UC essentially functions as a low-pass filter. Consequently, the utilization of the UC is poor and the same accounts for design flexibility. Both components have to be designed for the desired DC-link voltage [3], [28], [29].

Semi-active 1: UC Controlled / Battery Passive

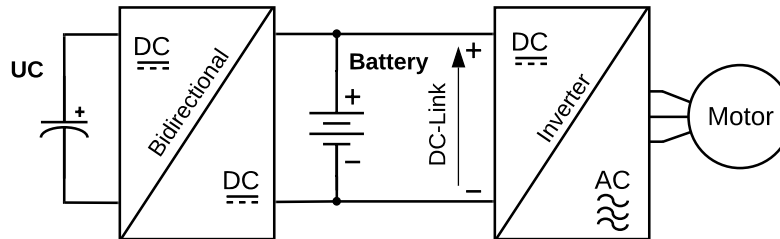


Figure 5-7: Semi-active HESS topology: UC controlled / battery passive, adapted from [3]

As UC utilization is the critical problem of the passive connection, there are several approaches to solving this problem by implementing one power converter.

The first semi-active topology connects the UC through a bi-directional DC/DC converter, whereas the battery remains directly connected. This allows a good utilization of the UC, as well as some design flexibility, as the maximum voltage of the UC-pack is variable. Problems related to this topology are the necessary peak power capability of the DC/DC Converter as well as few design flexibility for the battery pack. Additionally, as energy is extracted from the battery, the DC-link voltage decays. As presented in chapter 4.3 this leads to a reduced motor power and thus reduced speed capability if the motor is the dominant limiting factor [3], [28], [29].

Semi-active 2: UC Passive / Battery Controlled

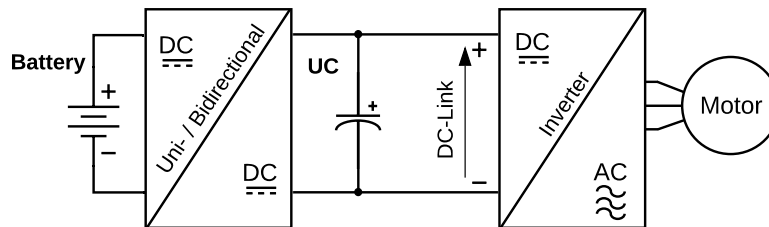


Figure 5-8: Semi-active HESS topology: UC passive / battery controlled, adapted from [3]

The second semi-active topology is a direct connection of the UC to the DC-link, whereas the battery is connected through a power converter. Similar to the previous topology, this leads to increased design flexibility for the converter interfaced device and reduced flexibility for the UC-pack. The power converter has reduce, which depends on the system but can be as low as the average of the load profile and can be unidirectional if all energy from regenerative braking is captured in the UC. Through the controlled power flow of the battery, the voltage of the UC can be regulated. UC utilization strongly depends on the admissible Δv of the DC-link voltage. In terms of power capability, a differentiation between continuous and short time peak power capability has to be made. The peak power capability depends on the combined power of both devices, which cannot be sustained infinitely as the accessible energy of the UC is conventionally much lower than of the battery. The continuous capability is

determined by the power of the battery and the DC/DC converter [3], [28], [29].

Active 1: Parallel Active Hybrid

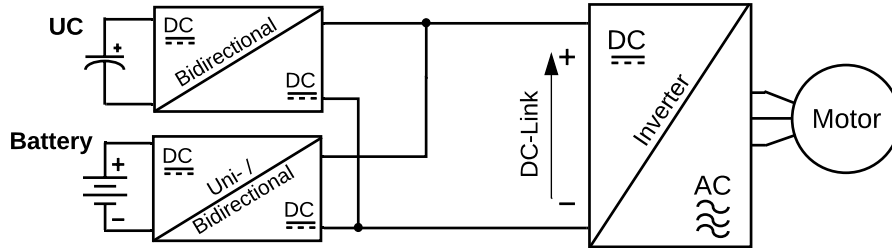


Figure 5-9: Active HESS topology: Parallel active hybrid, adapted from [3]

Active hybrid topologies correspond to a system where the power flow of both energy storage devices is actively controlled. In the parallel active hybrid, the UC is interfaced by a bidirectional DC/DC Converter with full power rating and one with reduced power rating, which can potentially be unidirectional. Alternatively, the converter interface is realizable as one multi-port converter. Maximum speed capability of the motor is ensured in any situation, as the DC-link voltage is controllable. This, however, comes at the expense of high part count and higher complexity of the system. Additionally, low efficiency can be expected when the UC is charged from the battery due to the two intermediate power conversions [3], [28], [29].

Active 2: Series Active Hybrid

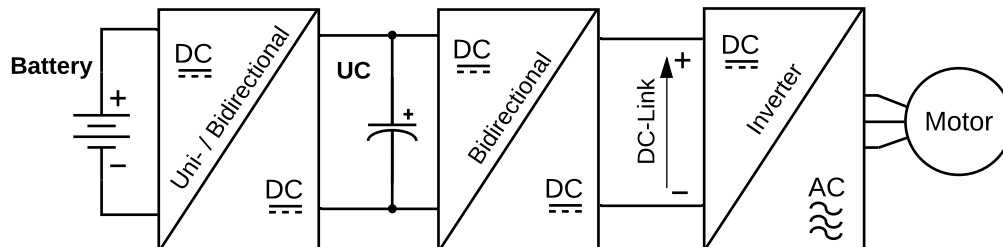


Figure 5-10: Active HESS topology: Series active hybrid, adapted from [3]

Another approach to a fully active connection is the series active hybrid. Once again, the same advantages as for the parallel active hybrid apply with the difference

of power flow efficiency. The efficiency is increased if power is flowing from battery to UC with one intermediate conversion, whereas the power flow from the battery to the inverter has two intermediate conversions and thus reduced efficiency [3].

Utilization of Partial Power Processing

In the context of HESSs, partial power processing represents a promising method to enhance the power converter structures of the previously introduced topologies. As the name indicates, partial power converters only process a proportion of the total active and reactive power and can thereby increase efficiency [30].

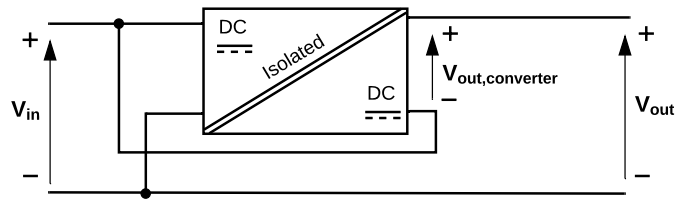


Figure 5-11: Scheme of a series connected partial power converter

Fig. 5-11 illustrates a series-connected partial power converter. In this thesis, this concept is not going to be evaluated, as the focus is on optimizing the cell quantities corresponding to the HESS, which contribute the dominant part of volume and weight. Nevertheless, this could be subject to future work, based on the results of this thesis.

5.5.2 Comparison

The different topologies introduced above can be compared according to several factors.

Table 5.1: Comparison of energy storage topologies

	Passive	Semi-active		Active	
		UC contr. Bat passive	UC passive Bat. contr.	Parallel Active	Series Active
Design Flexibility	-	o	o	+	+
Battery Stress	-	+	o	+	+
UC Utilization	-	+	o	+	+
Complexity	+	o	o	-	-
High Power Semicond.	0	2	0	2	2
Red. Power Semicond.	0	0	2	2	2

Both semi-active topologies are a good compromise between system complexity and additional power converter weight and volume, juxtaposed to advantages due to the hybridization. Comparing the two semi-active topologies with each other, they offer a trade-off between additional power converter resources and UC utilization. In general, the question of better suitability is qualitatively difficult to answer. Therefore, the following optimization investigates both semi-active topologies and provides quantitative data.

5.6 Optimization Algorithm

The hybridization of the energy storage essentially allows the designer to reduce the peak power requirements of the battery storage, by using another type of storage that can deliver this peak power. Less peak power requirement in the battery enables a shift towards cells with higher energy density. A resulting design might deliver more energy at the same power capability or more power at the same energy content. The

central question of this chapter is whether the utilization of two energy storage types allows an overall improvement in terms of gravimetric and volumetric density.

The underlying question contains an optimization problem. In simple terms, how many and which UC type in combination with which battery cell yields the minimum volume and weight. As this is the central question for all HESS, literature suggests many approaches to solve the problem. [31] utilizes a controlled elitist non-dominated sorting genetic algorithm, which is a variant of NSGA-II. An optimum number of battery cells and UCs is selected in order to optimize the HESS's life-cycles, mass and member functions of the fuzzy control. In [32] a study is carried out on the optimal number of battery cells and UCs while implementing several types of EMS control schemes. The control schemes include frequency rule-based control algorithms and closed-loop PI control of the UC recharge Power with a fixed SOC reference as control input.

In this thesis, the focus is set on an optimum design of the HESS for several commercially available UCs and Li-Ion cells laid out in chapter 5.3. The previously introduced driving profile will be utilized as load in the HESS optimization. As [32] reveals good performance for the PI-based control, a similar controller with variable gain is utilized to control the SOC of the UC. The control structure is depicted in fig. 5-12. Depending on the semi-active topology either $\overline{P_{bat}}$ (for battery active) or P_{UC} (for UC active) is extracted as output power reference of the power converter.

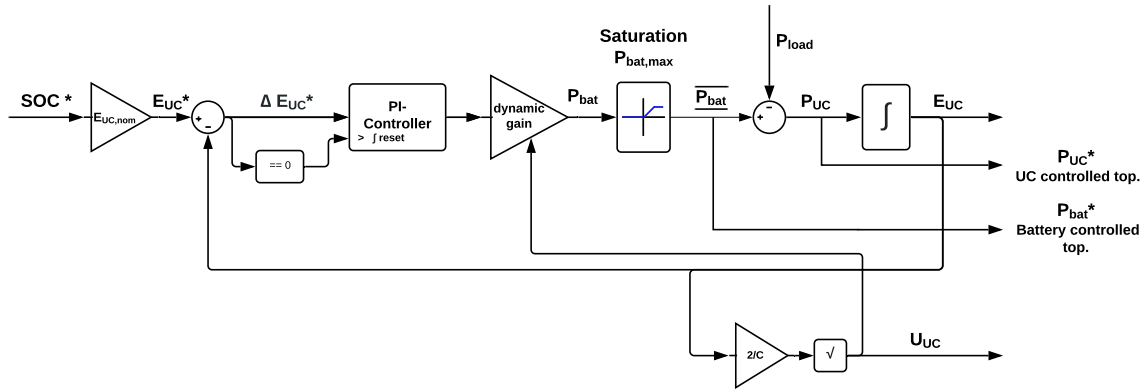


Figure 5-12: HESS control scheme for both semiactive topologies

In contrast to the presented papers, a so-called greedy algorithm is used to solve

the optimization problem. The greedy algorithm leads to the optimal solution by dividing the problem into several sub-problems and solving the local optimum for each of them [33].

The sub-problems for the HESS are the following:

1. Optimum SOC reference for the MotoStudent drive cycle for a certain UC-pack and corresponding nominal energy content.
2. Minimum required battery peak power $P_{bat,peak}$ for the MotoStudent drive cycle when a certain UC-pack is used.
3. Optimum combination of Li-Ion cells and UC cells in terms of volumetric/gravimetric density.

Sub-problem 1 and 2 are solved for each combination of UC and battery cell type and varying numbers of each. Subsequently, combinations violating the constraints are filtered and the volumetric/gravimetric density of each combination is evaluated. The overall flowchart for this optimization algorithm is presented in fig. 5-13.

The optimization algorithm's core is the function determining the required battery power in dependency of UC-pack parameters (C_{UC} , V_{nom} , R_{ESR}) and topology. This calculation is based on a simulation of the previously introduced load profile. Fig. 5-14 illustrates the flow chart of the function.

In a first loop, the SOC-setpoint (SOC*) of the UC is optimized. The SOC reflects the proportion of the UC energy in reference to the nominal UC energy. Generally, a higher SOC* is advantageous as more energy is available in default condition. However, the SOC* also has to be low enough to stay within the system's voltage boundaries during regenerative braking. Thus, starting from 100 % the SOC* is decremented by 1% each iteration. As long as the maximum UC Voltage is violated, the SOC* is decremented by 1 %. In the first iteration the maximum voltage constraint is obeyed, the optimum SOC* is reached, with an accuracy of 1 %.

Once the ideal SOC* is determined, a second loop optimizes the required maximum battery power. As long as the minimum voltage of the UC is not violated,

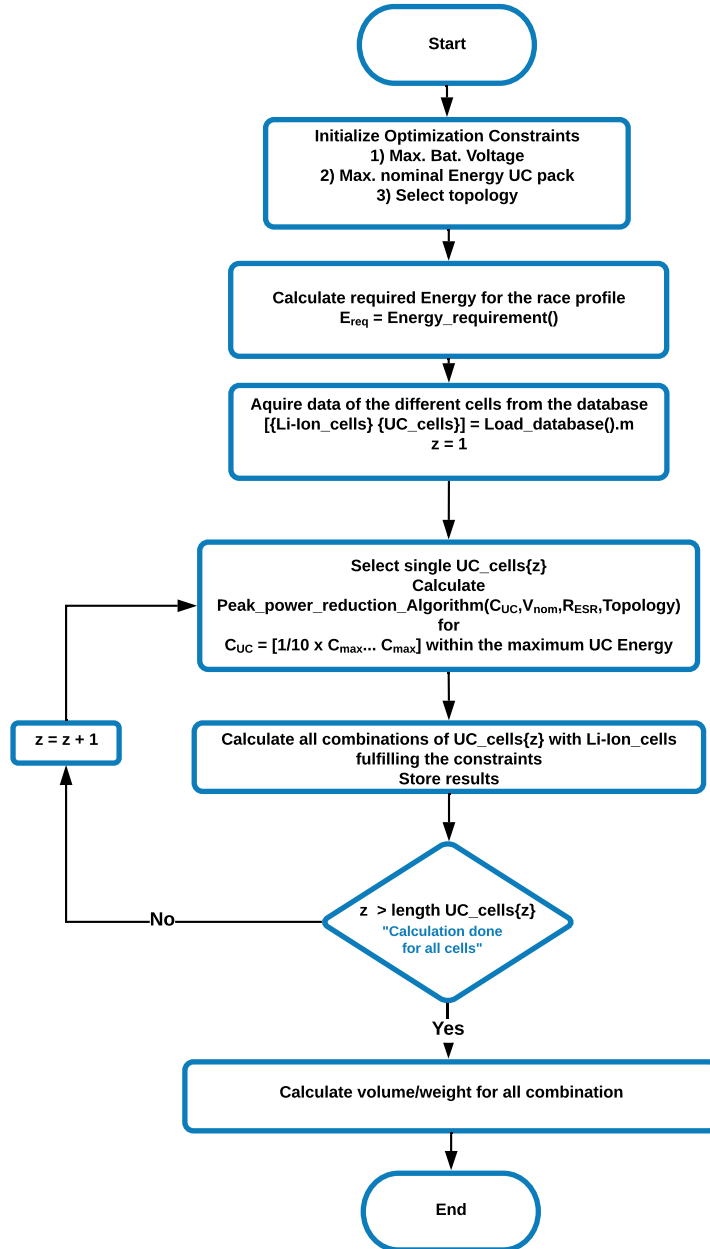


Figure 5-13: Flow chart optimization algorithm

the maximum battery power can be further reduced. An illustration of an optimized power flow for the UC active/ battery passive HESS (topology of fig. 5-7) can be seen in fig. 5-15. As the UC is interfaced through a power converter, the UC-pack voltage is a choice of design. In the example, the number of series capacitors N_s was set to 5, corresponding to a V_{max} of 15 V.

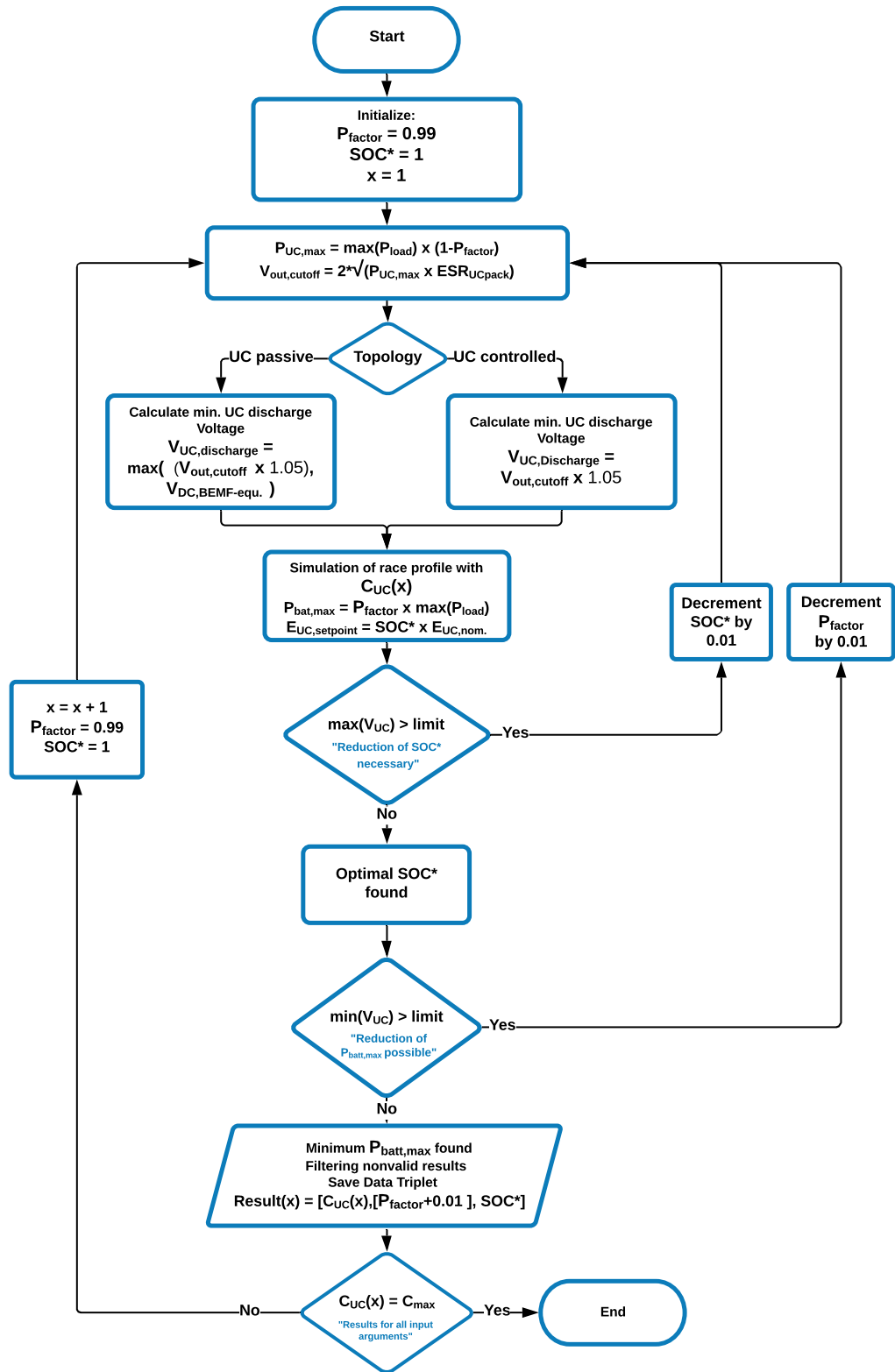


Figure 5-14: Peak power reduction algorithm in dependency of C_{UC}

As desired, the SOC* is exactly at the limit, where the maximum regenerative braking event increases the voltage to the UC voltage limit. Similarly, the peak battery power was reduced to a point where the strongest acceleration event reduces the UC voltage no further than the lower UC voltage limit.

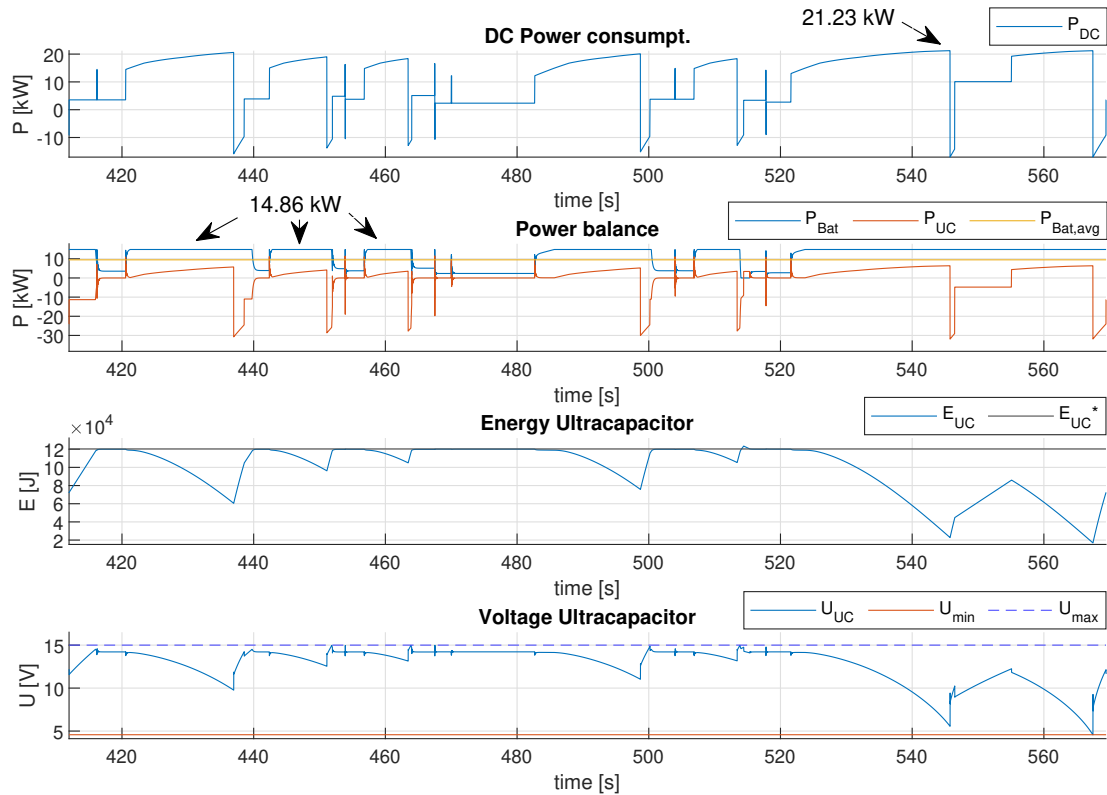


Figure 5-15: Exemplary powerflow of one launched lap for the UC active / battery passive HESS (fig. 5-7) for a UC-pack with $E_{nom} = 37.1$ Wh

Comparing the first graph with the second demonstrates that a reduction of maximum battery power from 21.23 kW to 14.86 kW could be achieved. Furthermore, the battery power fluctuations could be significantly reduced and regenerative braking energy exclusively circulates in the UC. In other terms, the power flow of the battery becomes unidirectional.

Fig. 5-16 presents the optimized power flow for the UC passive / battery active HESS. Due to the passive connection of the UC to the DC-link, the UC-pack's nominal voltage has to match the desired DC-link voltage (121.8 V). Furthermore, the

minimum voltage of the UC-pack and thus the minimum DC-link voltage is set to the limit, where the maximum producible AC voltage $\hat{V}_{Ac,ph-n}$ equals the BEMF $_{ph-n}$ according to equ. 4.7. As in the previous powerflow, the powerflow from the battery becomes unidirectional in fig. 5-16, which allows a simplification of the corresponding power electronics.

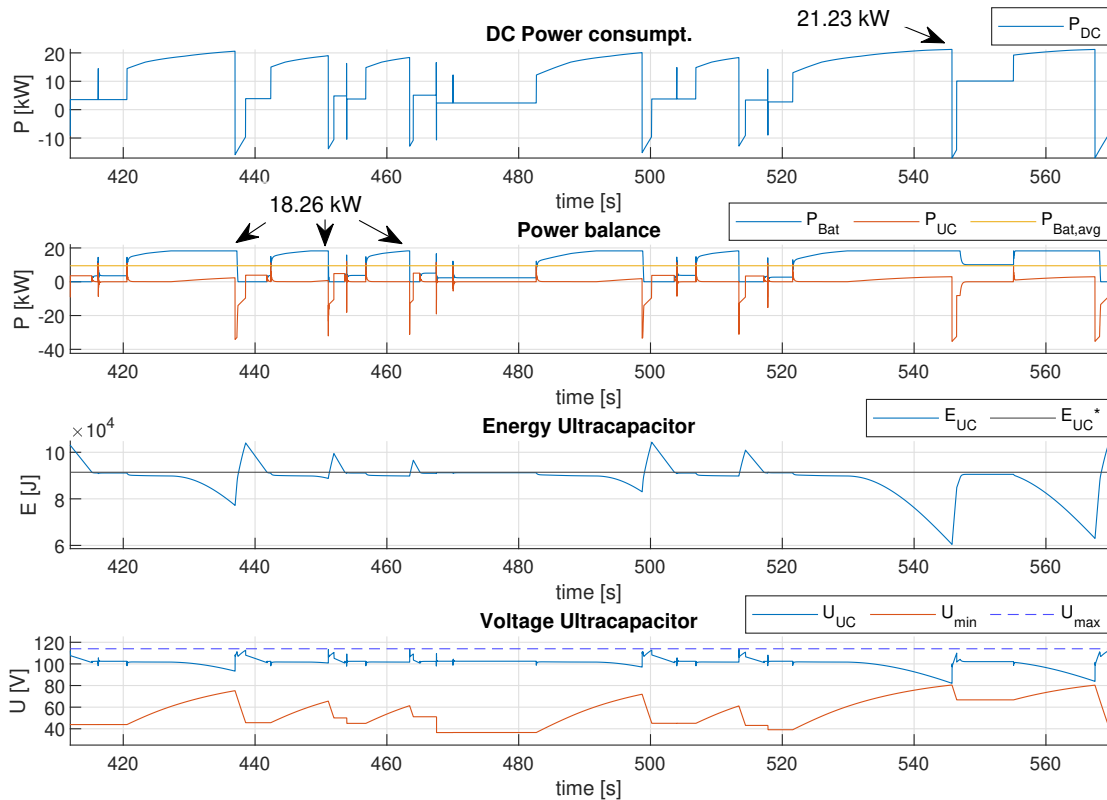
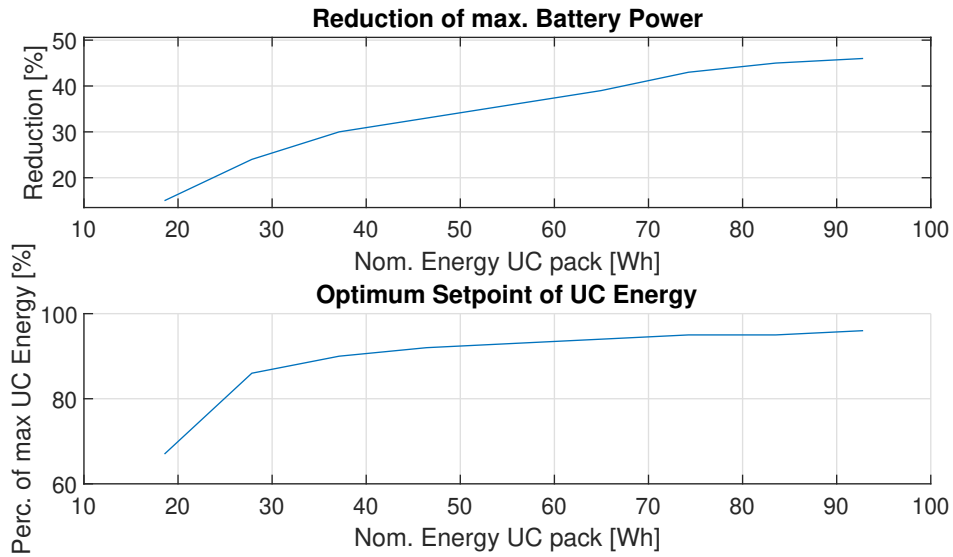
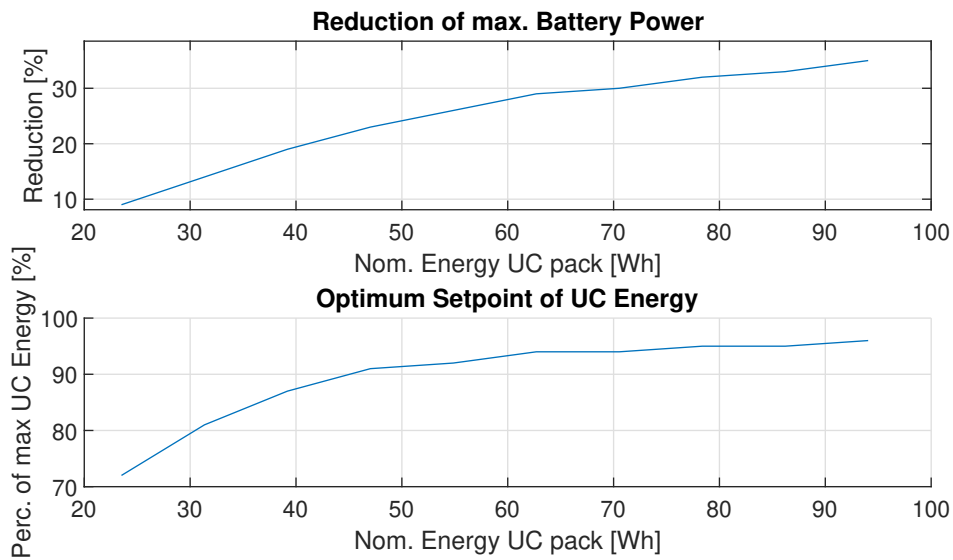


Figure 5-16: Exemplary powerflow for one launched lap for the UC passive / battery active HESS (fig. 5-7) for a UC-pack with $E_{nom} = 31.1$ Wh

Fig. 5-17 shows the achieved reduction of maximum battery power and the optimum setpoint for the two semi-active topologies. Within the depicted UC energy range, the peak power is reduced by approximately 45 % for the active UC topology in fig. 5-17 (a) compared to around 35 % for the passive UC topology in 5-17 (b). Generally speaking, topology (a) yields as expected better results due to the increased utilization of the UC.



(a) UC active / battery Passive HESS



(b) UC passive / battery active HESS

Figure 5-17: Achieved peak power reduction and optimal SOC* in dependency of nominal UC energy for the two semi-active topologies

5.7 Optimization Results

The optimization results yield the volume and weight for all valid combinations of UCs and Li-Ion battery cells in dependency of nominal UC-Pack energy and cell types. Mass and volume of the resulting systems consider only cell quantities. Any

further volume or mass of the mechanical structure, cooling, or additional converter structures is not taken into account at this point. As discussed in chapter 5.5.2, the optimization is performed for the two semi-active HESS topologies. The first topology interfaces the UC through a power converter and connects the battery directly to the DC-link (fig 5-7). The second topology utilizes a direct DC-link connection of the UC and interfaces the battery through a power converter (fig. 5-8). For the HESS topologies, the additional volume and weight of the power converter is not included in the results, however, it is considered as an additional factor in the final evaluation.

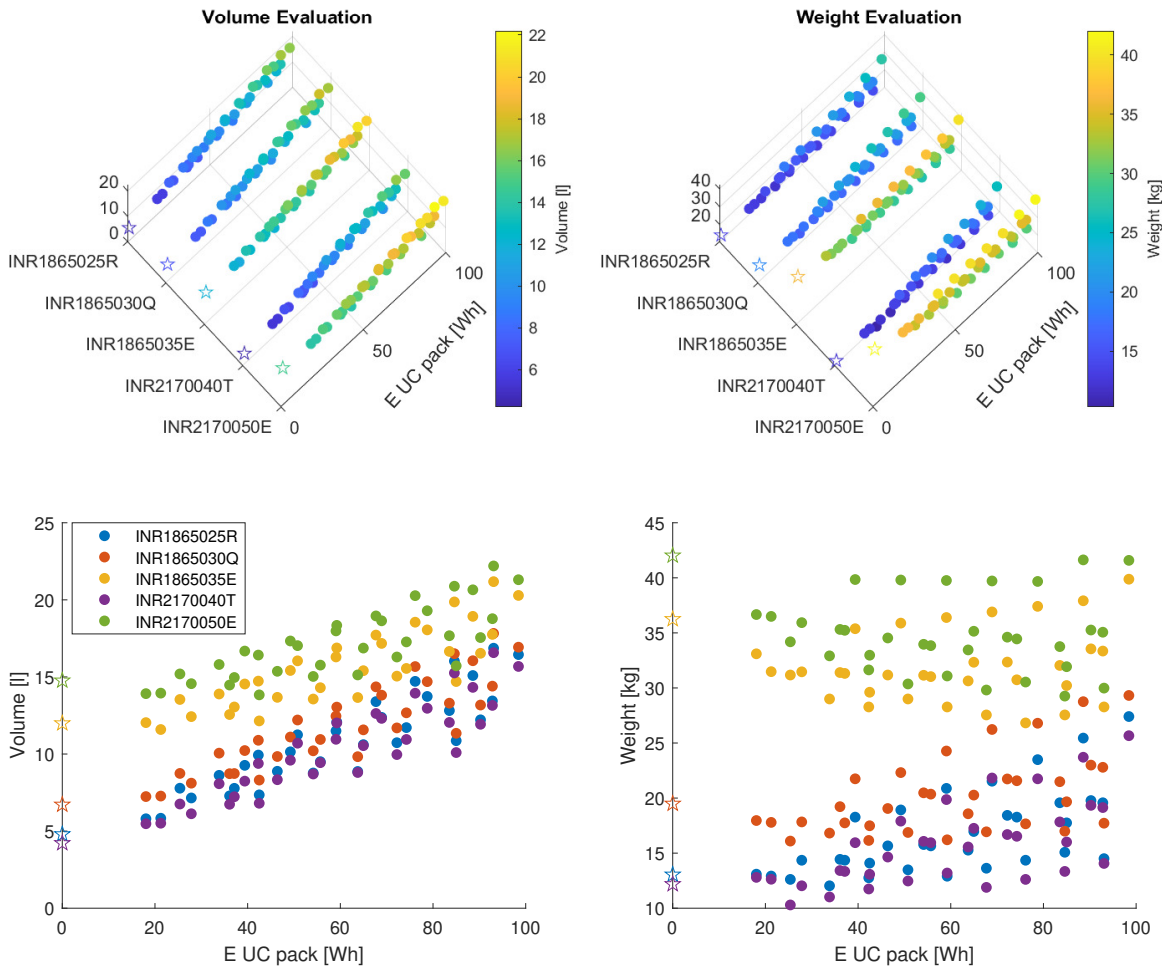


Figure 5-18: Optimization results for UC controlled / battery passive HESS

Fig 5-18 illustrates the result for the topology with passive battery connection and controlled UC as shown in fig 5-7. Each point depicts a combination of a UC pack and the indicated type of Li-Ion cell with the corresponding total volume and weight of

that HESS. The stars represent an optimum battery-only ESS for the respective cell. A comparison of the results for different Li-Ion cells demonstrates that the power cells (INR1865025R & INR2170040T) are most suitable, even in a HESS. For the tested load profile the shift towards cells with higher energy density cannot achieve a reduction of volume or weight. For the previously mentioned power cells the difference between pure battery storage and a hybrid system with rather low nominal energy in the UC-pack is close. In the case of the INR2170040T cell, a battery online ESS yields 4.2 l compared to 5.5 l for a HESS with a 18 Wh UC-pack. Plotting the weight over the volume allows an evaluation of the optimization goals in comparison.

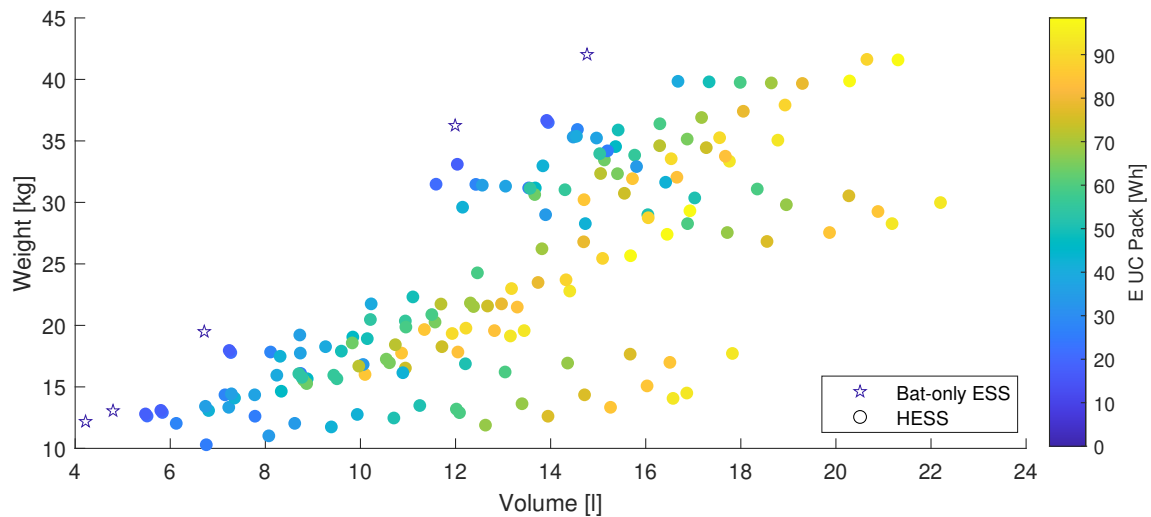


Figure 5-19: Optimization results (volume against weight) for UC controlled / battery passive HESS

From fig. 5-19, it is evident that pure battery storage yields the overall lowest volume. Regarding the cell weight, the HESS achieves lower results, however, the additional weight for the power converter yet has to be considered. The HESS with the lowest weight [10.3 kg] demonstrates around 1.88 kg less than the lightest battery only solution [12.18 kg]. Approximating the additional weight of the power converter, the overall weight seems to be competitive between both solutions.

Fig. 5-20 illustrates the optimization results for the second semi-active topology (UC passive / Battery controlled). Due to lower UC utilization, the optimization yields higher volume and weight, compared to fig. 5-19. Furthermore, it is noticeable

that more combinations are filtered out due to constraint violations. The combinations with low nominal UC-pack energy cannot obey the maximum voltage constraint in regenerative braking events, even at the minimum SOC* reference. Comparing the semi-active topologies, the minimum SOC* is higher for the topology with passive UC connection, as its lower limit is restricted by the BEMF. The first legitimate HESSs is encountered at a UC-pack energy of around 33 Wh.

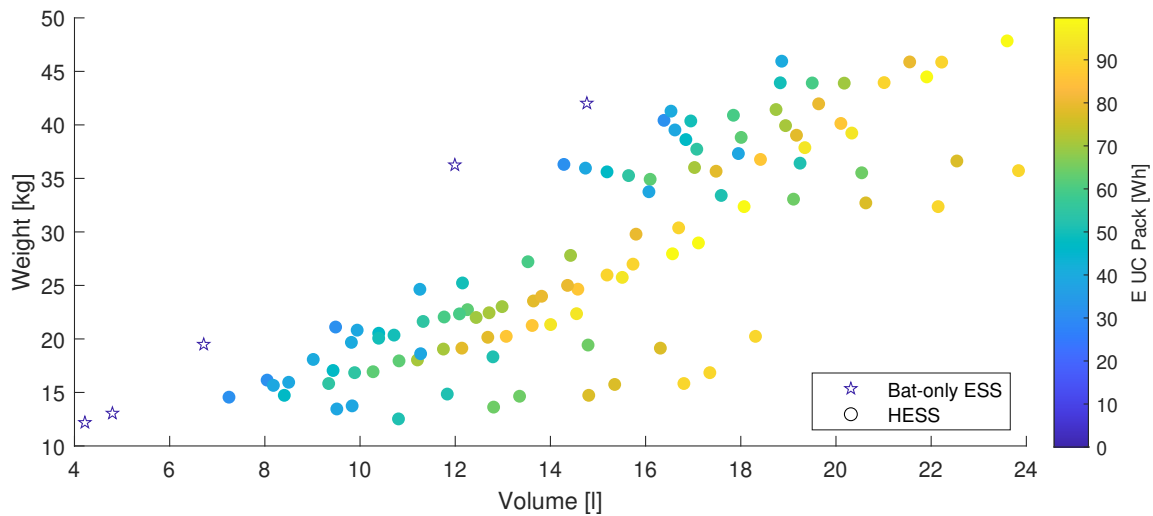


Figure 5-20: Optimization results (volume against weight) for UC passive / battery controlled HESS

Even though the passive UC connection offers advantages in terms of converter ratings and battery stress, the negative aspects of the reduced UC utilization prevail. All legitimate HESSs of fig. 5-20 demonstrate a significant increase in weight and volume, compared to pure battery storage. The combinations with the highest gravimetric density [14.56 kg, 7.25 l], as an example, represents an increase of 71.8 % in terms of volume and 19.5 % in terms of weight compared to the best battery-only solution [12.18 kg, 4.22 l]. The additional converter resources would add up to this.

An overall discussion of these results is provided after the sensitivity analysis regarding the load profile.

5.7.1 Sensitivity Analysis: Load Profile

In order to evaluate the potential of HESS for load profiles with stronger fluctuation and higher power in general, the factor β is introduced. The factor β represents the relation between the nominal torque and the maximum short-time torque of the machine according to

$$T_{mot,max} = T_{nom} + (\beta - 1) \cdot (T_{max} - T_{nom}) \quad (5.5)$$

The script that creates the load profile applies the torque depending on the sector of the race track and the beta-factor. The actual achievable beta depends on the energy of the battery and on the thermal capability of the drive. In this season, a feasible beta of 1.2-1.25 is projected, however, an analysis for higher values of beta can serve as a decision guideline for the following seasons.

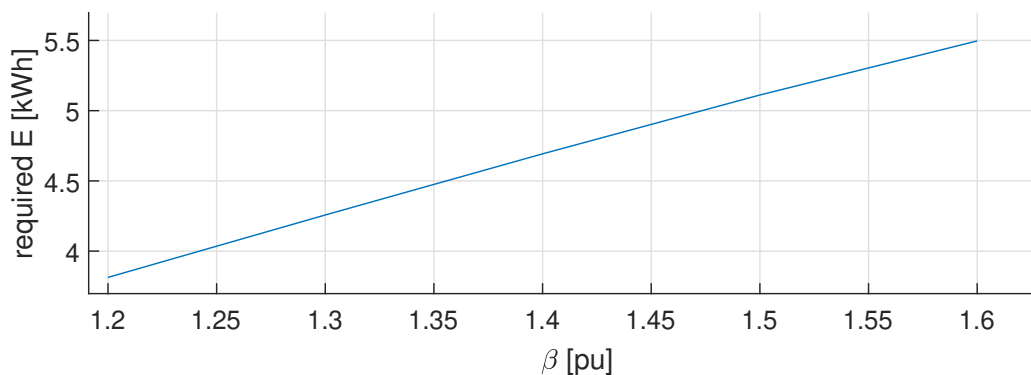


Figure 5-21: Required energy in dependency of overload factor β

In fig. 5-21 the required energy in dependency of the beta-factor is visualized. This energy is calculated through an analytical script considering the powertrain losses in dependency of the operating point. The required energy is provided as an input to the optimization algorithm.

As evident from fig. 5-22, the difference between battery-only storage and HESS with controlled UC interface remains similar for higher beta-factors. However, the topology with a passive UC connection becomes more and more disadvantageous in terms of volume, as beta increases. This can be explained by the higher speed in

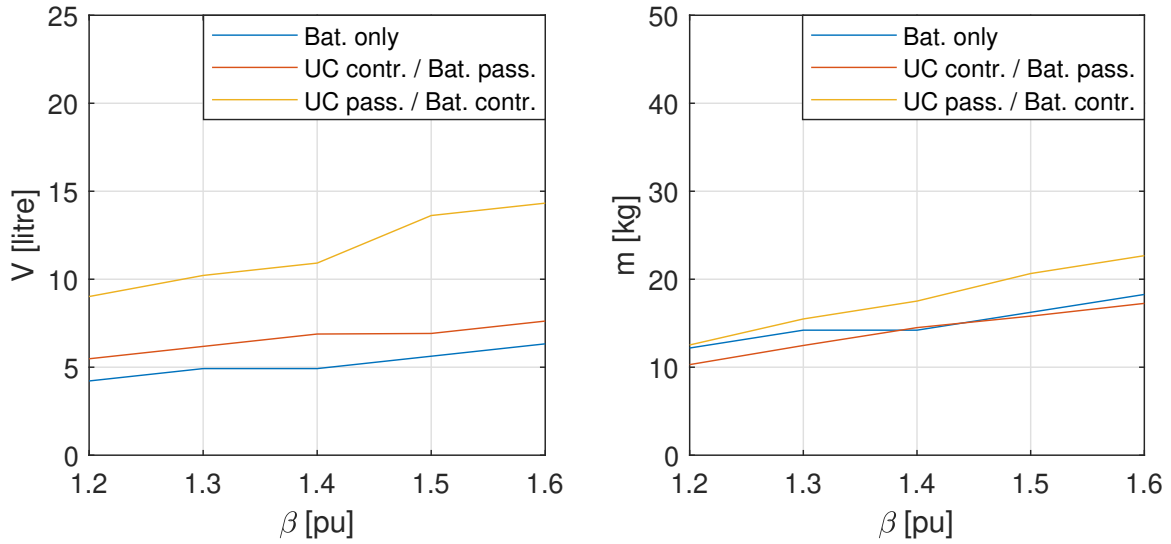


Figure 5-22: Mass/volume comparison of battery only storage and lowest HESS solution (individually for weight and volume) in dependency of overload factor β

the race track's straights, which results in higher BEMF and an increased minimum discharge voltage. Consequently, less energy can be extracted from the UC and utilization is further reduced.

5.7.2 Discussion of Results

The previous chapter provided a holistic analysis of UC HESSs, related power converter configurations and an optimization methodology. The volumetric and gravimetric density for optimized pure Li-Ion battery storage and HESS considering two semi-active topologies was evaluated and juxtaposed. Considering the load profile of the electric race motorcycle, the topology interfacing the UC with a power converter yields significant advantages over the direct DC-link connection. Overall, a hybridization of the energy storage cannot increase the volumetric density, however, gravimetric density can be reduced, considering only the parameters of Li-ion and UC cells. Taking all facts into consideration, the use of a HESS can not be recommended for the electric race motorcycle at this point, as the volumetric density is a critical design point of the current prototype. Nevertheless, a comprehensive and fast simulation approach was delivered, in which future Li-Ion and UC cells with

potentially higher energy density can be quickly reevaluated. Furthermore, the optimization methodology can be easily adapted to evaluate HESS for other applications, e.g., home or grid storage, where HESS might yield more promising results to reduce costs or increase cyclability.

Chapter 6

Advanced Power Conversion - Traction Inverter Design

6.1 Objective and Methodology

Chapter 4.4 demonstrated the impact of power converters on the tractive system. As core improvements, the removal of the DC/DC Converter and the increase of the inverter's current capability were identified. The following chapter's objective is to carry out a thorough design of a traction inverter, focusing on the high current capability, compact design, and good scalability for future MotoStudent seasons. As no previous experience with the parallelization of discrete semiconductors exists in the MotoStudent team, an intermediate design step towards the 780 A_{RMS} inverter of chapter 4.4 is taken. In this thesis, an inverter with a peak current capability of 500 A_{RMS} will be designed, aiming for a component with the same performance as the SKAI 70 A2 MM15-L, but higher power density. This intermediate development will serve as a foundation towards the 780 A_{RMS} inverter. The inverter design covers the definition of requirements, semiconductor selection, determination of DC-link capacitance and verification of the design in PLECS. As the high number of parallel devices is identified as a critical design point, a demonstrator Printed Circuit Board (PCB) is developed in order to evaluate the feasibility.

6.2 Requirements

Every electrical design initially relies on solid requirements. The following requirements have been determined as a result of previous chapters and are explained one by one.

Table 6.1: Requirements of the traction inverter

I_{phase} (10 s) [A]	I_{phase} (cont.) [A]	$V_{DC-link,max}$ [V]	$\Delta V_{DC-link}$ [%]	f_{sw} [kHz]	$T_{ambient,max}$ [°C]
500	> 140	≥ 126	± 5	≥ 16	40

¹ Current ratings refer to RMS quantities

The current capability I_{phase} represents the maximum RMS current rating of one phase. Consequently, for parallelized semiconductors the required peak current rating per semiconductor is

$$\hat{I}_{switch} = \frac{I_{phase} \cdot \sqrt{2}}{n_{parallel}} \quad (6.1)$$

assuming perfect parallelization. The total maximum current is derived by the maximum phase current requirement of 500 A_{RMS}. As the thermal time constant of the employed semiconductors is very small, the amplitude of the phase current has to be considered rather than the RMS-value. This assumption will be verified by the simulation of the thermal domain in PLECS.

The maximum DC-link value results from the maximum admissible voltage of the system (126 V), defined in the MotoStudent regulations version 2019/2020.

The switching frequency is specified as a minimum of 16 kHz, which is the switching frequency of the formerly used inverter. The maximum ambient temperature is selected as 40 °C, which is the maximum expected ambient temperature of any race event.

6.3 Semiconductor Selection

The semiconductor selection most significantly depends on the system voltage and power level. In the range of 200 V, Silicon (Si)-Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs) are the commonly employed semiconductors. GaN-High-Electron-Mobility Transistors (HEMTs) offer a more performant but expensive wide-bandgap alternative. For higher voltages around 450 V, both GaN and Silicon Carbide (SiC) transistors coexist and compete as wide-bandgap semiconductors. In order to get an overview of the different types of semiconductors, three transistors that can potentially fulfill the requirements are compared in table 6.2. As none of these discrete devices fulfills the current rating alone, the parallelization of multiple transistors is necessary.

Table 6.2: Max. ratings of suitable discrete switches, $T_j = 25^\circ\text{C}$

	Type	V_{DS} [V]	$I_{cont.}$ [A]	$R_{DS,on}$ [m Ω]	Price [€]	Area [mm ²]	Package
Infineon: IRF200P222	Si-MOSFET	200	182	5.3	6.70	542	TO 247
GaN Systems: GS66516T	GaN-HEMT	650	60	25	55.11	68.76	GaNPX®
ROHM SCT3017ALHR	SiC-MOSFET	650	118	17	96.77	542	TO 247

¹ Area of Si- and SiC-MOSFET takes the area covered by the TO247-package legs into account

Table 6.2 illustrates that the on-resistance $R_{DS,on}$ and the price of the Si-MOSFET is much lower than the competitors'. The density of the design, however, mostly depends on the area covered by the semiconductor. From this perspective, the GaN transistor represents the highest current capability per area, allowing more compact designs.

Eventually, the GaN Systems GaN-HEMT is chosen for the following reasons:

1. The higher voltage capability allows an easy adaptation of the inverter, if voltage levels are changed by regulations in future MotoStudent competitions.
2. The higher current rating per area and innovative packaging of the GaN-HEMT was predicted to yield the overall most dense design.

3. As GaN-HEMTs allow very high switching frequencies a DC-link capacitor made of ceramic capacitors could be enabled. This would further increase the power density of the converter. For this reason, the first design iteration will be carried out with a switching frequency of 100 kHz.

6.4 Characteristics of GaN-HEMTs

While the use of Si-MOSFETs and Insulated-Gate Bipolar Transistors (IGBTs) is generally well understood and documented in literature, there are some notable differences to the conduction and switching characteristics of GaN-HEMTs. Many switching applications, including the classic three-phase voltage source inverter, require the capability to conduct a current in both positive and negative direction. While Si-MOSFETs incorporate an intrinsic anti-parallel body diode, IGBTs are commonly paired with separate anti-parallel diodes to allow the third quadrant operation [34].

In contrast to IGBTs, GaN-HEMTs have the ability to conduct through the same channel in forward and reverse direction. If no gate voltage is applied, the so-called reverse self commutation takes place once a certain threshold voltage $v_{GD,th}$ from gate to drain is exceeded. The voltage drop in reverse self commutation can be described as

$$v_{DS} = -v_{GD,th} + i \cdot R_{DS,on} \quad (6.2)$$

It should be highlighted that in reverse self commutation $v_{GD,th}$ is a positive value and i is negative, and thus v_{DS} is a negative value as corresponding to negative conduction.

If the GaN-HEMT is turned off with a negative gate source voltage v_{GS} , this negative voltage adds to the threshold that has to be overcome before self commutations applies, according to

$$v_{DS} = -v_{GD,th} + v_{GS} + i \cdot R_{DS,on} \quad (6.3)$$

This behaviour is shown in the output characteristic of the GaN-HEMT depicted in fig. 6-1.

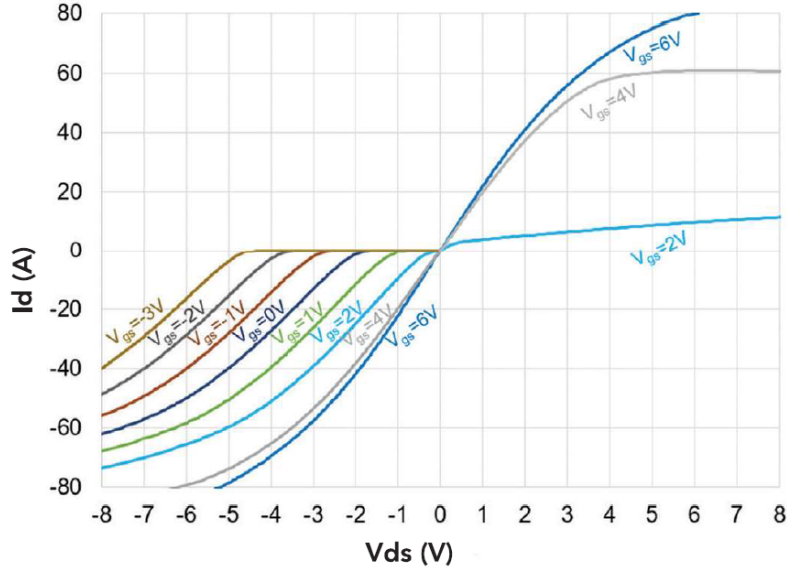


Figure 6-1: Output characteristic of GaN-HEMT, source: [4]

In reverse self conduction, the characteristic is similar to an anti-parallel diode with higher forward voltage drop V_f , with the clear difference, that a GaN-HEMT does not incorporate the reverse recovery effect of a Diode. If during reverse conduction a positive gate source voltage v_{GS} is applied, the conduction characteristic becomes similar to positive conduction with a resistance approximately equal to $R_{DS,on}$ [4], [35].

Fig. 6-1 illustrates this gated reverse conduction for $V_{GS} = 6 \text{ V}$.

6.5 Analysis of Semiconductor Losses

In order to identify the most loss-critical operating point of the inverter, an analytic description of semiconductor losses is introduced, illustrating the dependencies of conduction and switching losses. The analysis is carried out for one phase, as symmetric conditions are assumed. Consequently, the other two phases thus yield the same situation phase-shifted by 120° and 240° .

In the analysis, the following assumptions and simplifications are made:

1. The switching frequency f_{sw} is a lot higher than the fundamental frequency of the output voltage f_{out} .
2. Switching and dead times of the transistor are neglected.
3. Linear modulation is assumed as described in chapter 4.2.3.
4. The switching ripple of the AC-current and DC-link voltage is neglected.

The fundamental of the phase voltage is described by

$$v(t) = \hat{V} \cdot \sin(\omega t) \quad (6.4)$$

and the fundamental of the phase current by

$$i(t) = \hat{I} \cdot \sin(\omega t - \varphi) \quad (6.5)$$

where φ represents the phase shift between the fundamental of AC phase voltage and current.

Switching Losses

In PLECS, the switching losses are determined through 3D lookup tables, usually provided by the manufacturer. The lookup-tables store the dissipated energy during on and off switching in dependency of current, voltage and temperature as illustrated in fig. 6-2.

This approach allows high simulation speed while maintaining precise results. In the case of the GaN Systems GS66516T HEMT, the lookup table is paired with a formula. E_{off} losses, for instance, are selected depending on the operating point and altered according to

$$E_{off} = \begin{cases} E + (R_{G,off} - 2) \cdot (i > 0) \cdot \frac{v \cdot i}{2} \cdot \frac{3.4e-9 + \frac{4.4e-9 \cdot (i/48.8)}{1.3 + (i/48.8)}}{-v_{GS,off} + 1.3 + (i/48.8)} \cdot \frac{25}{T_j} & \text{if } i > 0 \\ E & \text{if } i < 0 \end{cases} \quad (6.6)$$

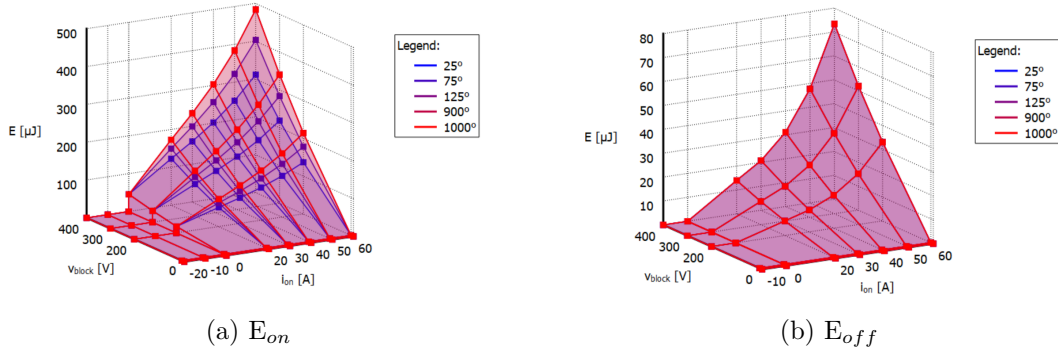


Figure 6-2: 3D lookup table of switching losses

Equ. 6.6 considers variations in gate resistance and gate source voltage from the nominal values. From the resultant switching energy, the average switching losses can be calculated through

$$P_{on} = E_{on}(i_{on}, v_{block}, T_j) \cdot f_{sw} \quad (6.7)$$

$$P_{off} = E_{off}(i_{on}, v_{block}, T_j) \cdot f_{sw} \quad (6.8)$$

in which

- i_{on} is described by equ. 6.5.
- v_{block} equals the DC-link voltage.
- T_j represents the junction temperature of the semiconductor.

$$P_{sw} = P_{on} + P_{off} \quad (6.9)$$

The lookup table of fig. 6-2 shows a positive gradient for higher values of current i , voltage v , and junction temperature T_j . As a consequence, the most critical operating point in terms of switching losses is at maximum DC-link voltage, maximum ambient temperature and maximum phase current.

Conduction Losses

Fig. 6-3 illustrates an example of the current in the top-side switch for the positive and the negative half-wave of the fundamental frequency for $M = 0.7$. Depending on the modulation index and the phase angle, the duty-cycle during positive and negative conduction phases strongly varies.

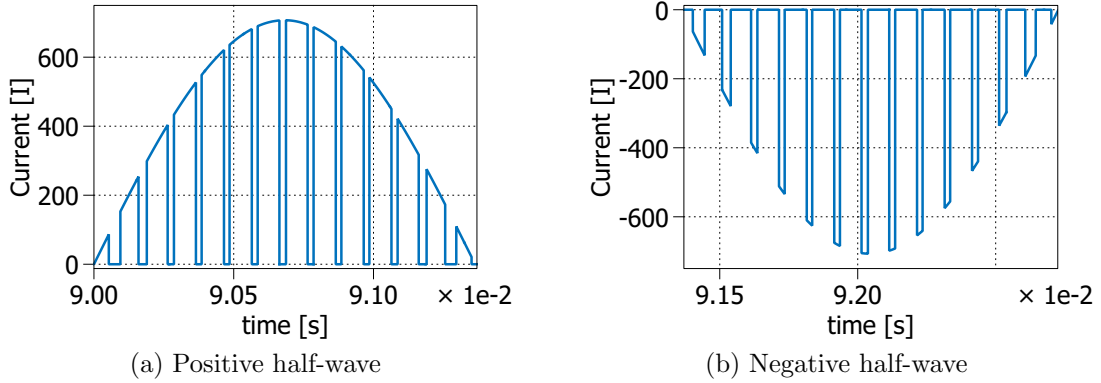


Figure 6-3: Current in top switch of three-phase inverter for $M = 0.7$, $\varphi = 0$

The average conduction losses, dissipated in one period in each of those phases, can be described by the following equations, derived from [34].

$$P_{avg,cond|i>0} = \hat{I}_{phase}^2 \cdot R_{DS,on} \cdot \left(\frac{1}{8} + \frac{\frac{M}{1.154} \cdot \cos(\varphi)}{3\pi} \right) \quad (6.10)$$

$$P_{avg,cond|i<0} = \hat{I}_{phase}^2 \cdot R_{DS,on} \cdot \left(\frac{1}{8} - \frac{\frac{M}{1.154} \cdot \cos(\varphi)}{3\pi} \right) \quad (6.11)$$

in which

- $\cos(\varphi)$ represents the power factor.

The division of M by the factor 1.154 accounts for the increased linear region, due to THI. Similar to the switching losses, the conduction losses and their dependencies are defined over 3D lookup tables in PLECS.

In the case of GaN-HEMTs, the $R_{DS,on}$ is nearly similar in both conduction phases thus the equation for the overall average conduction losses can be reduced to

$$P_{avg,cond} = P_{avg,cond|i>0|} + P_{avg,cond|i<0|} = \frac{1}{4} \cdot \hat{I}_{phase}^2 \cdot R_{DS,on} \quad (6.12)$$

As evident from equ. 6.12, the average conduction losses over one fundamental period are independent of the modulation index M and the power factor. However, higher values of M correspond to a shift of conduction losses towards the positive current half-wave.

6.6 Design of the DC-link Capacitor

The DC-link capacitor is one of the major components in a three-phase inverter. It provides a stable input voltage to the switching stage in the presence of currents, varying at the switching frequency. The DC-link capacitor is conventionally designed to meet a certain voltage tolerance. The following chapter's objective is to design the DC-link to comply with the specified requirement of $\Delta v = 5\%$.

A comprehensive derivation of analytic switching ripple is given in [5] and [36] and the relevant results will be summarized in the following. The analysis in the previously mentioned papers is developed for a space vector modulated inverter. However, [36] suggests the validity of carrier-based modulation with proper common-mode injection as used in this thesis. It should be emphasized that the calculation neglects the voltage ripple due to the ESR of the DC-link capacitor. This condition is assumed to be valid for the following analysis as the target of the converter design is a ceramic capacitor DC-link, for which the capacitive ripple is dominant.

Neglecting inverter losses the peak-to-peak voltage deviation can be calculated by

$$\Delta v_{pp} = \frac{\hat{I} \cdot T_{sw}}{C_{DC-link}} \cdot r_{pp}(M, \vartheta, \varphi) \quad (6.13)$$

as given in [5] with

- \hat{I} being the peak phase current.
- T_{sw} being the switching period.
- r_{pp} being the normalized voltage ripple amplitude, which is a function of the modulation index M , the angle of the active space vector ϑ and the phase angle φ as defined in equ. 6.5.

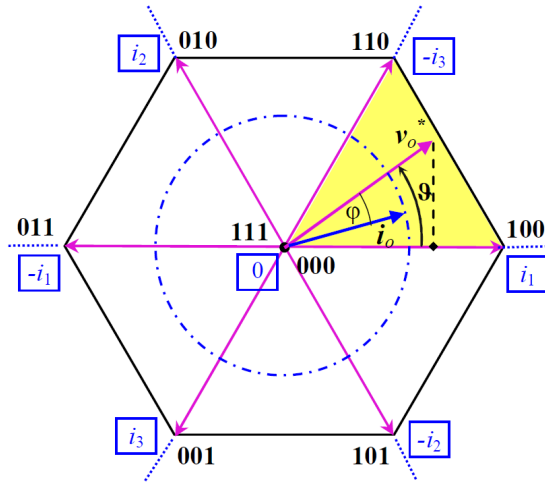


Figure 6-4: Space vector diagram illustrating angles and periodicity, source: [5]

Fig. 6-4 depicts the space vector with the commonly used switching states [S1 S2 S3] of the inverter legs. The voltage ripple of the DC-link shows periodicity between the sectors of the switching states, which corresponds to a $\vartheta = [0 - 60^\circ]$. The normalized voltage ripple amplitude used in equ. 6.13 can be calculated through

$$r_{pp}(M, \vartheta, \varphi) = \max(r_{pp}^A, r_{pp}^B) \quad (6.14)$$

with

$$r_{pp}^A(M, \vartheta, \varphi) = \frac{3}{8} \cdot M \cdot \cos(\varphi) \cdot \left(1 - \frac{\sqrt{3}}{2} \cdot M \cdot \sin(\vartheta + \frac{\pi}{3})\right) \quad (6.15)$$

$$r_{pp}^B(M, \vartheta, \varphi) = \frac{3}{8} \cdot M \cdot \left| \cos(\varphi) \cdot \left(1 - \frac{\sqrt{3}}{2} \cdot M \cdot \sin(\vartheta + \frac{\pi}{3})\right) + \frac{4}{\sqrt{3}} \cdot \sin(-\vartheta + \frac{\pi}{3}) \cdot \left(\frac{3}{4} \cdot M \cdot \cos(\varphi) - \cos(\vartheta - \varphi)\right) \right| \quad (6.16)$$

The normalized ripple amplitude r_{pp} for $\vartheta = [0 - 60^\circ]$ and multiple values of modulation index M are plotted in fig. 6-5. The phase angle of the IPM is calculated through a script, shown in appendix B.1. As evident from fig. 6-5, the normalized ripple amplitude strongly depends on the modulation index.

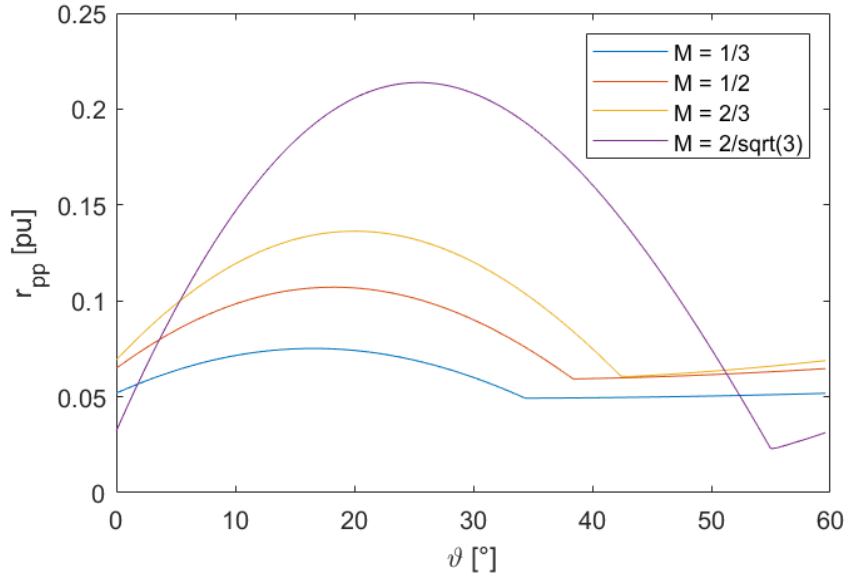


Figure 6-5: Normalized ripple amplitude r_{pp} for $\vartheta = [0, 60^\circ]$ and $\varphi = 56.4^\circ$

Since the inverter should be designed for the maximum modulation index of $M = 2/\sqrt{3}$, the maximum of the corresponding curve is inserted in equ. 6.13 in order to calculate the required capacitance. The result is a DC-link capacitance of minimum $124 \mu F$ to satisfy the $\Delta v = \pm 5\%$ requirement for the selected switching frequency of 100 kHz. This value of capacitance seems low enough to enable a ceramic

capacitor DC-link. In the feasibility study in chapter 6.8, this point will be reassessed in detail for a practical design, taking into account effective capacitance variation due to the DC-bias effect.

6.7 Verification: Simulation in PLECS

The inverter circuit is modeled in PLECS in order to evaluate semiconductor losses and the eligibility of off-the-shelf products for the thermal system. The simulation includes the modulation, the power stage of the inverter, the emulated motor load through current sources and the thermal subsystem.

Through the load current sources, any desired load condition (amplitude, frequency, phase angle) can be adjusted. Respective operating point parameters are calculated by the help of the script, shown in appendix B.1. The modulation scheme of the inverter was adjusted to allow the direct input of the desired modulation index. Details of the associated block (“PWM Mod.”) are given in appendix B.2.

3-Phase 2 level GaN-Inverter Loss Determination and Thermal Simulation with Emulated Motor Load

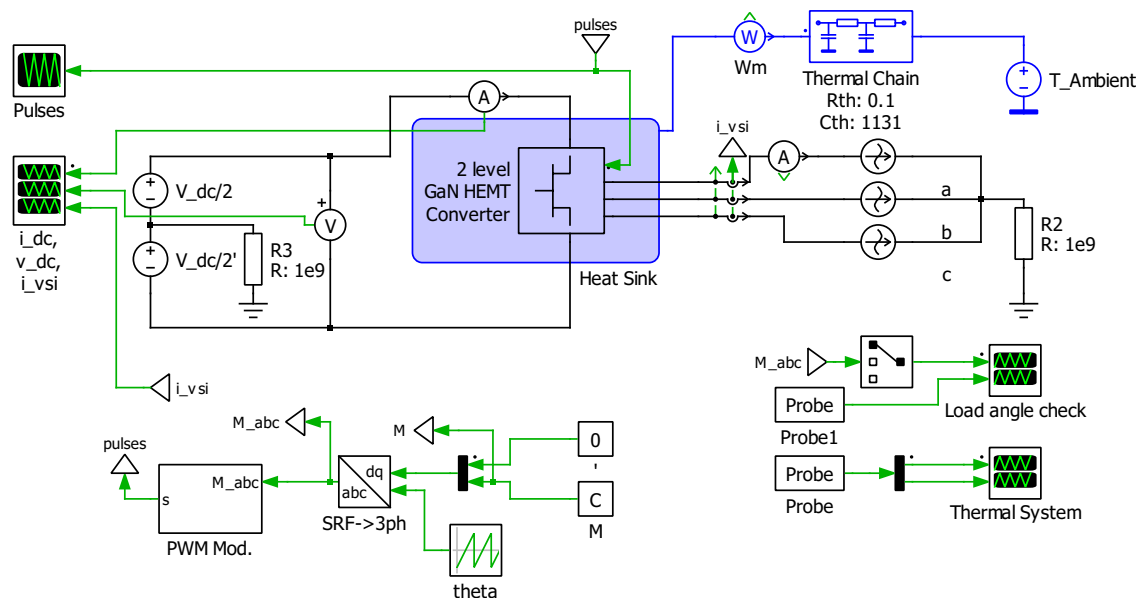


Figure 6-6: Simulation model of the two-level three-phase GaN inverter

As identified in chapter 6.5, the average of the total semiconductor losses is independent of the modulation index. Thus a simulation at a constant operating point

will yield the same average temperature as a dynamic test ,e.g., the 10 s full power requirement, which equals a strong acceleration. The difference in average conduction losses throughout positive and negative half-wave will be reflected in a temperature ripple. This ripple is most relevant at the maximum average temperature, which will be reached at the end of the acceleration phase. As the end of the 10 s acceleration approximately equals the end of the constant torque region ($M = 1.154$, $\text{rpm} = 5500$), the corresponding modulation index M will be used in the simulation.

Modeling semiconductor losses precisely is a central target of any power converter simulation. Simulation tools in SPICE-environment can achieve high precision for switching losses by utilizing detailed electrical models, which include parasitic elements [37]. With wide-bandgap semiconductors like the introduced GaN-HEMT and corresponding rise/fall times as low as under 5 ns, simulating the detailed switching transient, however, heavily reduces the simulation speed [38]. Evidently, there is a trade-off between simulation speed and detail.

When both thermal and electrical systems are simulated together, very low time constants derived from the switching dynamics are paired with very high time constants of the thermal system. Altogether, this results in low simulation speed. In PLECS, this dilemma is solved by electrically processing the switching instant as ideal lossless switching, and feeding losses, described through the previously introduced 3D lookup tables (fig. 6-2), to the thermal system. These losses depend on switching voltage, switching current, temperature and also on the properties of the implemented gate driver. In this thesis, the recommended value for the gate on-resistance $R_{G,on} = 10 \Omega$ and a conservative value of $R_{G,off} = 7 \Omega$ as gate resistance are selected as starting point. The relatively high off-resistance value originates from the maximum gate driver current capability used in the feasibility study in chapter 6.8. Underlying reasons for the selection of this driver will be explained in the respective chapter in more detail. As gate voltages, the values of a parallelization test board of GaN Systems, described in [7] of $v_{GS,off} = -5 \text{ V}$, $v_{GS,on} = 7 \text{ V}$ are used for a first simulative analysis. The negative off voltage is utilized to increase the gate driver's noise immunity and prevent false turn-on.

6.7.1 Thermal Analysis

The objective of the thermal analysis is to verify the compliance with the maximum temperature of the GaN-HEMT of 150 °C in any operating point. Off-the-shelf components are selected for the heatsink and thermal isolation material, connecting the HEMTs to the heatsink and providing electrical isolation. Multiple numbers of parallel devices are simulated in order to determine a suitable amount. The thermal system is modeled through the equivalent electrical Cauer network, as presented in fig 6-7.

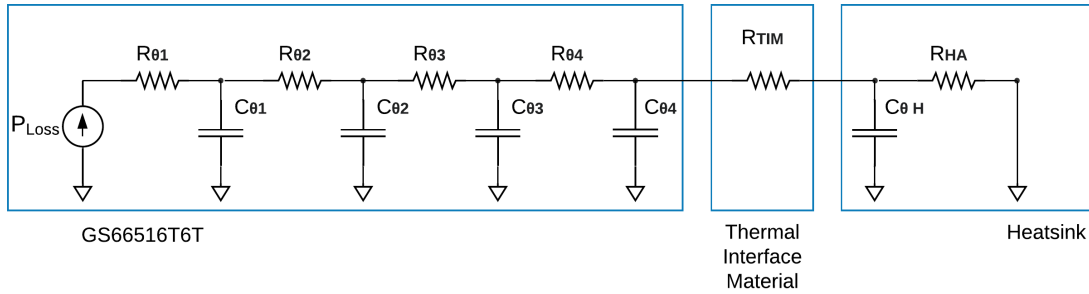


Figure 6-7: Cauer network of a single semiconductor connected to the heatsink

In the Cauer network of fig. 6-7

- $R_{\theta 1} = 0.011 \text{ K/W}$, $C_{\theta 1} = 4.25\text{e-}5 \text{ J/K}$ represents the GaN layer.
- $R_{\theta 2} = 0.231 \text{ K/W}$, $C_{\theta 2} = 2.96\text{e-}3 \text{ J/K}$ represents the Si layer.
- $R_{\theta 3} = 0.237 \text{ K/W}$, $C_{\theta 3} = 6.65\text{e-}4 \text{ J/K}$ represents the Attachment.
- $R_{\theta 4} = 0.021 \text{ K/W}$, $C_{\theta 4} = 1.01\text{e-}3 \text{ J/K}$ represents the Cu Base.

[39]

- $R_{TIM} = 1.84 \text{ K/W}$ representing BERGQUIST HI-FLOW 300P, a high performance isolating thermal interface material between semiconductor and heatsink suggested by GaN Systems in [40].
- $R_{HA} = f(\text{Airflow } (m^3/h)) \approx 0.1 \text{ K/W}$, $C_{\theta H} = 1131 \text{ J/K}$, representing the Heatsink Dau BF 151 , a commercial high-performance heatsink with bonded fins [41]. $C_{\theta H}$ was received from the manufacturer through E-mail contact.

Both, 10 s maximum ratings and continuous ratings are simulated in order to verify the proper operation of the inverter.

Operating point 1 - 10 s Peak Current (500 A_{RMS})

The first simulation is performed for a 10 s peak phase current of 500 A_{RMS} at the maximum ambient temperature of 40 °C. In order to find the necessary number of parallel switches, the simulation is repeated for 12, 14 and 16 parallel GaN-HEMTs per inverter leg. Both electrical properties and thermal description are adjusted for each simulation. With the thermal system per semiconductor as described, the simulation yield the following result:

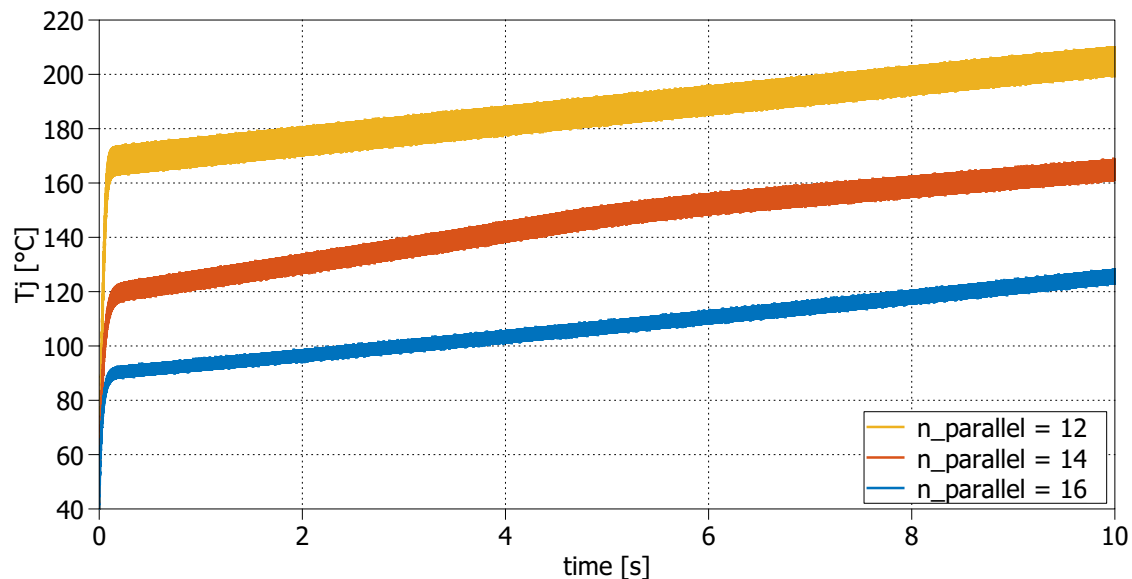


Figure 6-8: Junction temperature for several numbers of parallel GaN-HEMTs at maximum current of 500 A_{RMS} for 10 s

The thermal system response can be approximated as a step-change in semiconductor temperature followed by a linear rise. As illustrated in fig. 6-8, the number of parallel switches has a significant effect on the junction temperature of each semiconductor and the total losses. Fig. 6-9 depicts the temperature of the heatsink, which depends on the total semiconductor losses. Overall a minimum number of sixteen parallel devices is identified to keep a margin of approximately 20 °C to the maximum junction temperature of 150 °C.

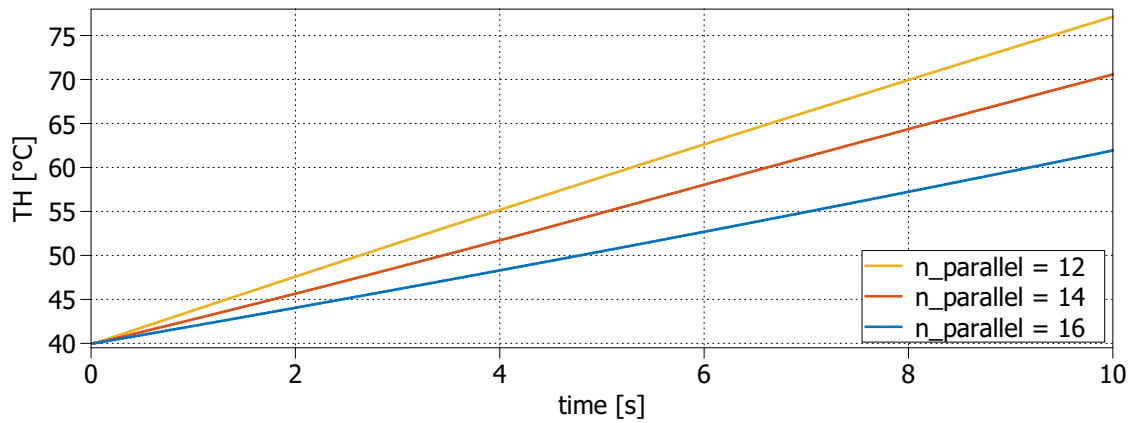


Figure 6-9: Heatsink temperature at maximum current of 500 A_{RMS} for 10 s

Operating point 2 - continuous rating (140 A_{RMS})

With the simulation model given in fig. 6-6, operating point two could be simulated, however, the simulation would require an excessive amount of time due to the high time constants associated with the heatsink. Thus the thermal system is slightly modified to yield steady-state results in an acceptable time. As the capacitance of the heatsink contributes to the biggest time constant, the thermal system is simulated without this capacitance, as seen in fig. 6-10.

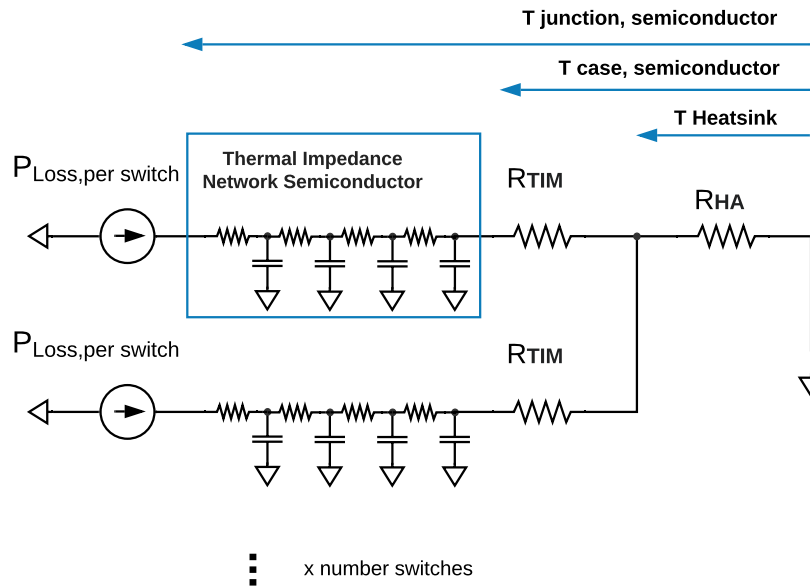


Figure 6-10: Thermal system for continuous rating analysis

This approach is a modified version of the mean-value analysis described in [34], with the difference that only the highest time constant is eliminated. The steady-state result provides the same average steady-state temperature with some negligible errors in the temperature ripple of the semiconductors. Fig. 6-11 depicts the junction temperature of a single semiconductor for the described simulation in order to verify continuous ratings. Due to the modified thermal system, the simulation converges to steady-state in under two seconds. The junction temperature stays well below $120\text{ }^{\circ}\text{C}$, thus the continuous ratings are satisfied.

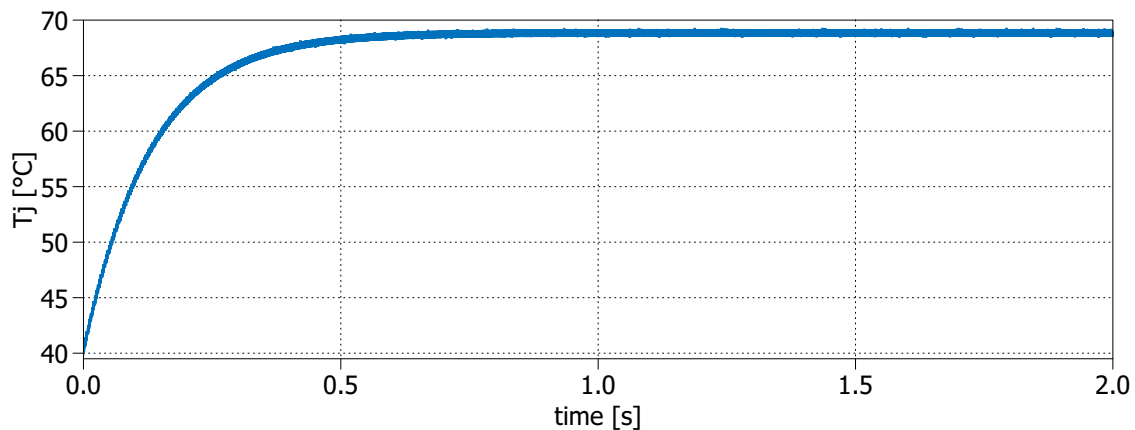


Figure 6-11: Junction temperature for $140\text{ }A_{RMS}$ continuous phase current

6.7.2 DC-link Voltage Ripple

In order to verify the coherence with the calculated ripple of chapter 6.6, a switching simulation including the DC-link is conducted. The block scheme of the adjusted simulation can be found in attachment B.3. The simulation is performed for the operating point with the maximum expected ripple ($I = 500\text{ }A_{RMS}$, $V_{Batt} = 21.8\text{ V}$, $M = 1.154$), as explained in chapter 6.6.

With an employed DC-link capacitance of $125\text{ }\mu\text{F}$, the simulation yields the results illustrated in fig. 6-12. In the graph, the predicted DC-link voltage variation calculated by equ. 6.13 and the simulated ripple are plotted together. The result shows a precise prediction of the ripple envelope in shape and amplitude. Due to the voltage drop in the equivalent series resistance of battery and power cables (R_1),

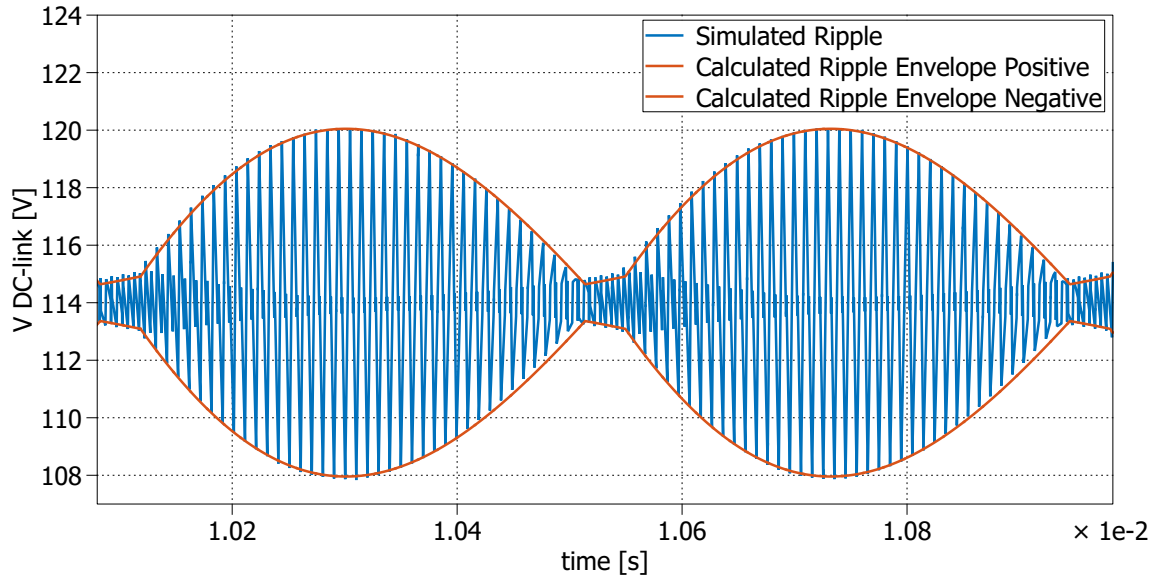


Figure 6-12: Comparison of calculated ripple envelope and simulated DC-link voltage ripple

the average DC-link voltage is slightly lower than the battery voltage of 121.8 V, which was used in the capacitance calculation. As a consequence the voltage ripple is marginally higher than the required $\Delta v = \pm 5\%$. Considering this voltage drop, the DC-link capacitance corresponding to the $\Delta v = \pm 5\%$ requirement can be corrected to $133 \mu F$.

6.8 Feasibility Study: High Numbers of Parallel GaN-HEMTs

Due to their temperature characteristics, GaN semiconductors are generally well suited for parallelization. A positive temperature coefficient of the on-resistance $R_{DS,on}$, as shown in fig. 6-13 (a) for the GS66516T, contributes to an equal current sharing during conduction. Furthermore, in the parallel setup, switching losses will shift from devices with higher temperature to lower temperature devices, owing to the negative temperature dependency of the transconductance g_m seen in fig. 6-13 (b). Both of these effects positively influence the temperature distribution of parallel switches [42], [43], [7].

$$g_m = \frac{\Delta i_D}{\Delta v_{GS}} \quad (6.17)$$

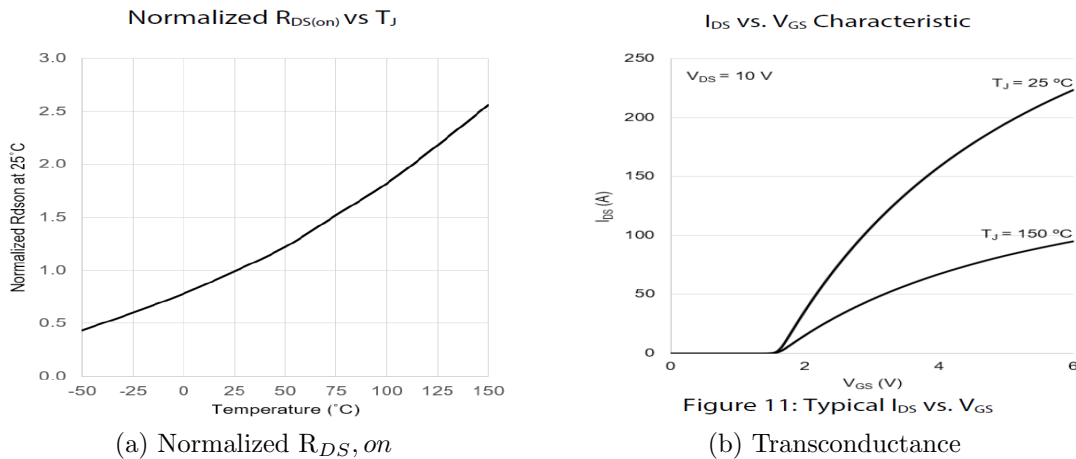


Figure 6-13: Temperature dependent parameters of GS66516T relevant for parallelization, source: [6]

However, the fast switching of the GaN devices requires increased attention on circuit parasitics, especially when devices are used in parallel operation. In [7], [43], the most critical circuit parasitics (fig. 6-14) and their effects are identified.

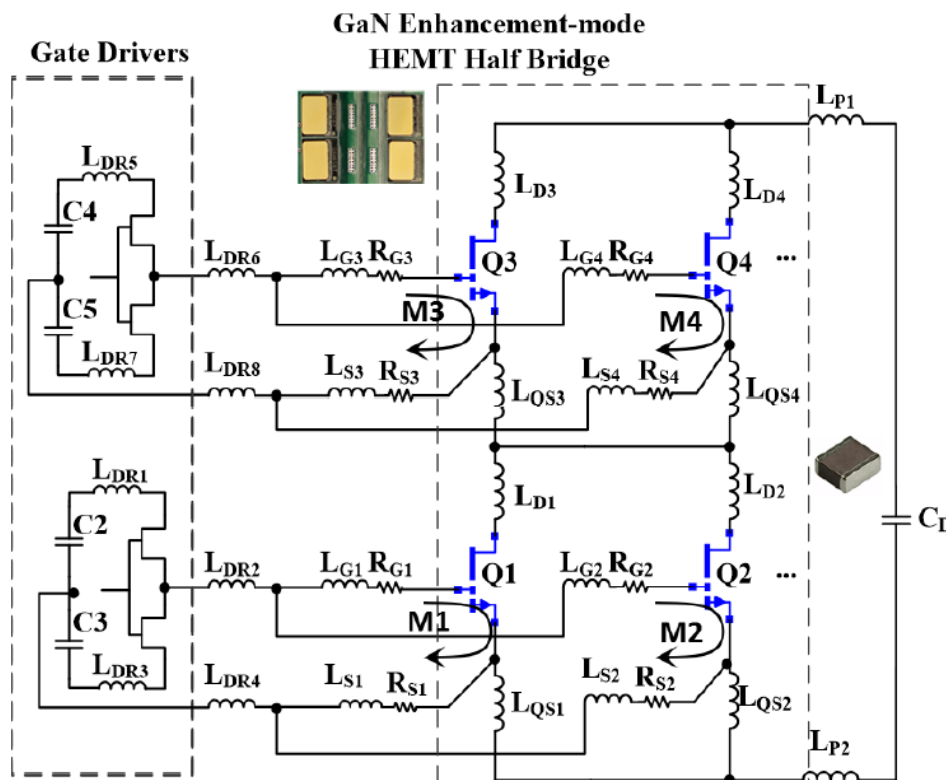


Figure 6-14: Equivalent half-bridge circuit diagram of two parallel GaN-HEMTs per switch, source: [7]

According to the analysis, the mutual inductance M_{1-4} , coupling power and gate loop, as well as the quasi-common inductance of the source L_{QS1-6} have the biggest impact on the switching process and should receive the greatest attention during the design. The previously mentioned references suggest an optimum layout and further verify the operation of a half-bridge with four GS66516T per switch.

[44] investigates the current distribution in 4 parallel GS66516T, including shunts for current measurement. Despite the use of specific low inductance shunts, the contribution to the quasi-common source inductance L_{QS1-6} resulted in reduced functionality of the circuit.

In [42], the parallel operation of three GS66516B is analyzed and the temperature distribution evaluated, which yields promising results.

Literature does not yet provide information on a number of more than four parallel GaN semiconductors. Thus in order to evaluate the feasibility of the MotoStudent GaN inverter, a double-pulse test PCB with sixteen parallel devices is designed and experiments conducted. As previously described, [44] provides an examples of a design, for which the current measurements of the transistors degrade the functionality of the system. Due to this reason, Drain or Source current measurements are purposely omitted in the demonstrator PCB.

6.8.1 Double-Pulse Test

The objective of the test PCB is to carry out a double-pulse test, verifying switching for currents up to 700 A, corresponding to the peak switched current in a 500 A_{RMS} inverter.

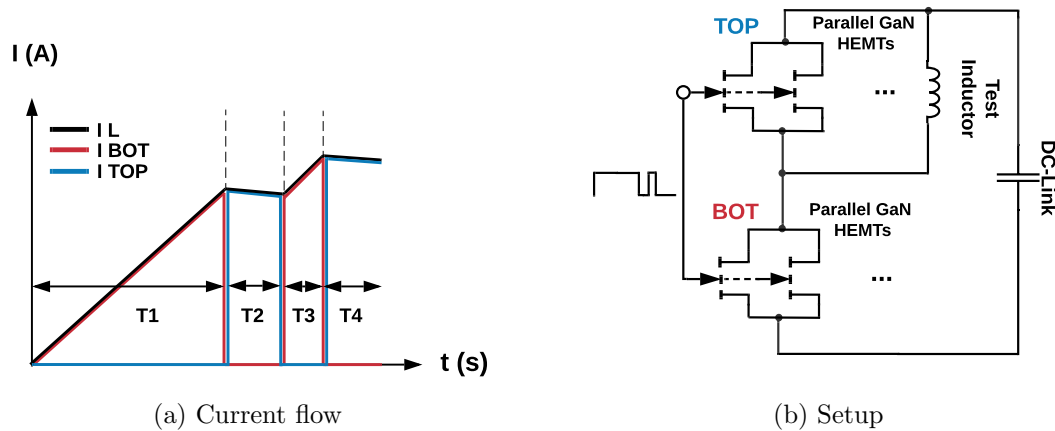


Figure 6-15: Double-pulse test

Fig. 6-15 illustrates the setup and the current waveforms of a double-pulse test. The objective of the double-pulse test is essentially to test the switching cell at the desired voltage and current levels. In the first time section T1, the current in the test inductor is ramped up to the desired switching current. Thereupon, the bottom switch is turned off and the switch-off transient can be examined. After the period T2, the bottom switch is turned on again and the switch-on dynamics can be investigated. In period T4, the bottom switch is turned off again, the coil is demagnetized and the

double-pulse test is terminated. In all switching periods, the top switch's control equals the negated control signal of the bottom switch to prevent a bridge short circuit. A suitable dead-time has to be implemented to prevent bridge short circuits during switching.

6.8.2 Design Demonstrator PCB

In order to characterize the switching behaviour of high numbers of parallel devices, a double-pulse test PCB is developed. The following section provides central information on the PCB design. The design is based on information given in [7], [45], and adjusted for the higher number of parallel switches. Hereinafter, the separate sub-circuits will be explained in more detail.

Fig. 6-16 illustrates the switching cell with sixteen parallel semiconductors per switch. Distributed gate and source resistors are added to each switch to ensure the damping of oscillations between the gates of the individual semiconductors [46].

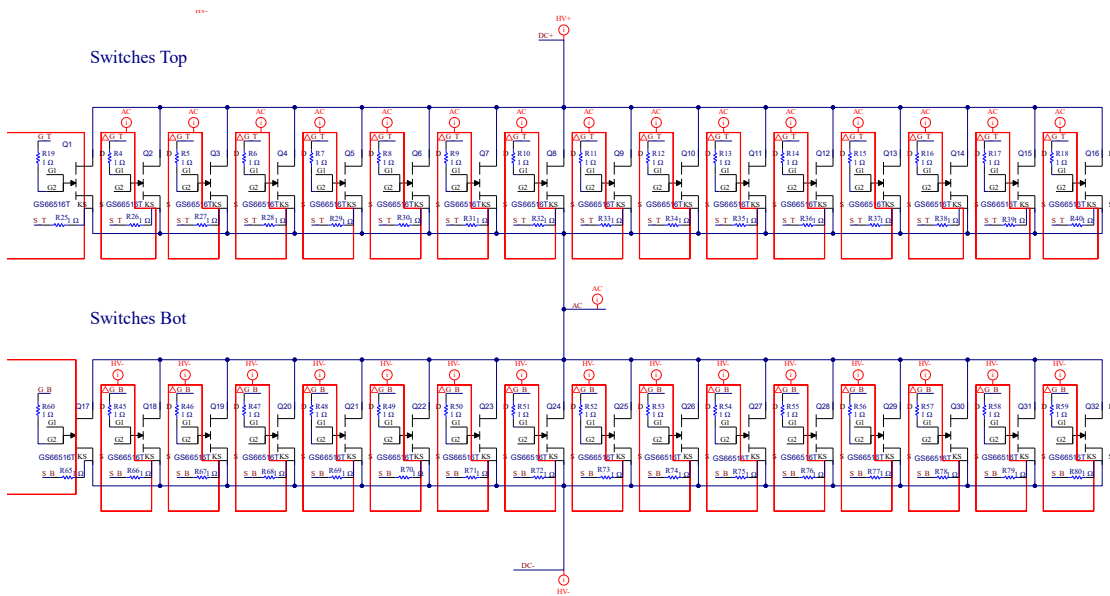


Figure 6-16: Parallel switches top and bot side

The DC-link consists of 28 ceramic capacitors with a nominal capacitance of $2.2 \mu F$ each. Considering the reduction of effective capacitance due to the DC-bias effect, which ceramic capacitors suffer from, the effective capacitance per ceramic

capacitor is approximately $1.1 \mu F$ [47]. This results in a total DC-link capacitance of around $31 \mu F$ per half-bridge or $93 \mu F$ for a complete inverter. As demonstrated in chapter 6.6, a total capacitance of around $133 \mu F$ is required in order to satisfy the voltage ripple requirements. A further increase of the total capacitance could be enabled through horizontally stacked ceramic capacitors or vertically placed MLCCs, as demonstrated in [48]. In the PCB, the configuration as it is with $93 \mu F$ is tested.

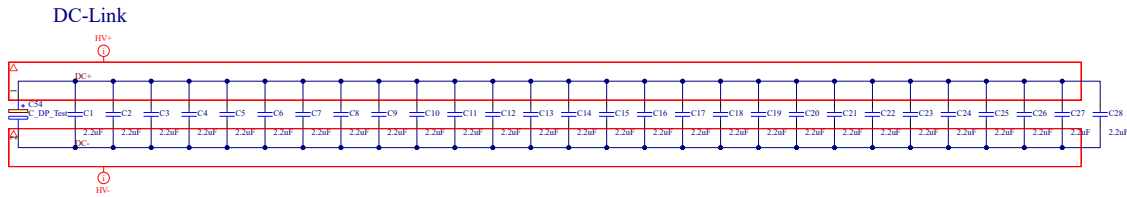


Figure 6-17: Ceramic DC-link plus additional electrolytic capacitor for double-pulse test

The common gate resistors are paired with Schottky-diodes in order to allow separate adjustment of switch-on and -off time. The initial gate resistances are designed to allow the fastest switching while staying within the driver’s current capability (IXDN630MYI - 30 A), which has the highest current capability of a single driver found on the market.

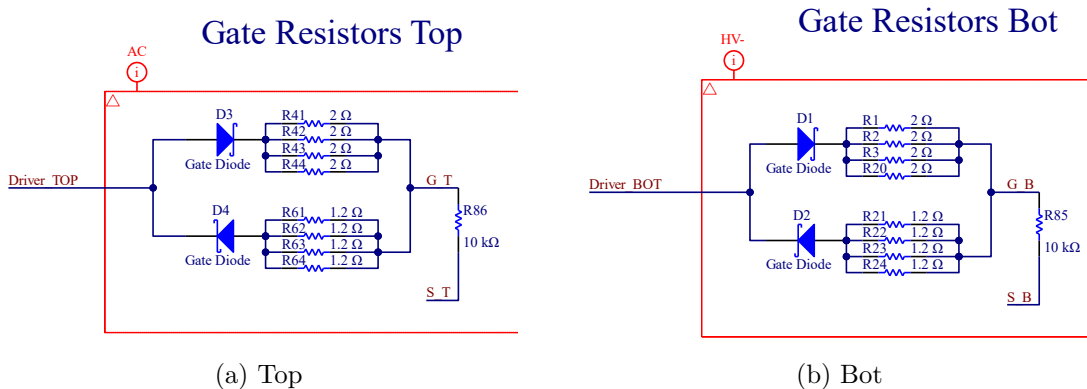


Figure 6-18: Gate resistors

Due to the fast switching capability of GaN semiconductors, high $\Delta v/\Delta t$ is expected for the AC node. Consequently, high Common Mode Transient Immunity (CMTI) of the gate drive circuit is essential to ensure proper functionality. This

is especially relevant for the top-side switches. In order to improve the CMTI, the DC/DC converters (U1, U2) are paired with common-mode chokes. Additionally, the signal isolation is accomplished through a high CMTI circuitry made from the bipolar junction transistors (Q33, Q34) and the LED emulator isolators (U3, U5) as recommended in [49].

Gate Driver TOP

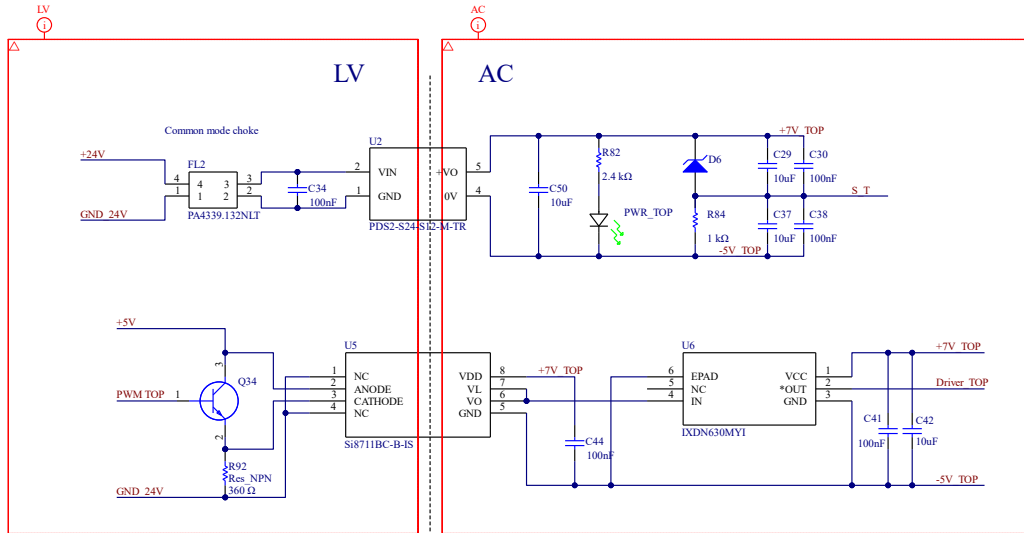


Figure 6-19: Gate driver top

Gate Driver BOT

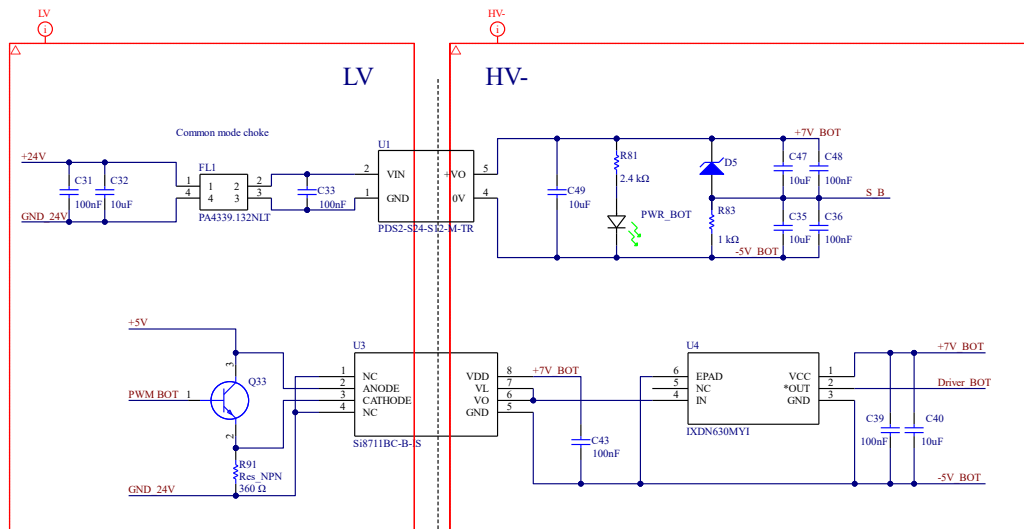


Figure 6-20: Gate driver bot

The dead time generation circuit prevents any bridge short circuit through hardware and thus improves the protection of the circuitry. The dead-time can be adjusted by the potentiometers VR1 and VR2, seen in fig. 6-21.

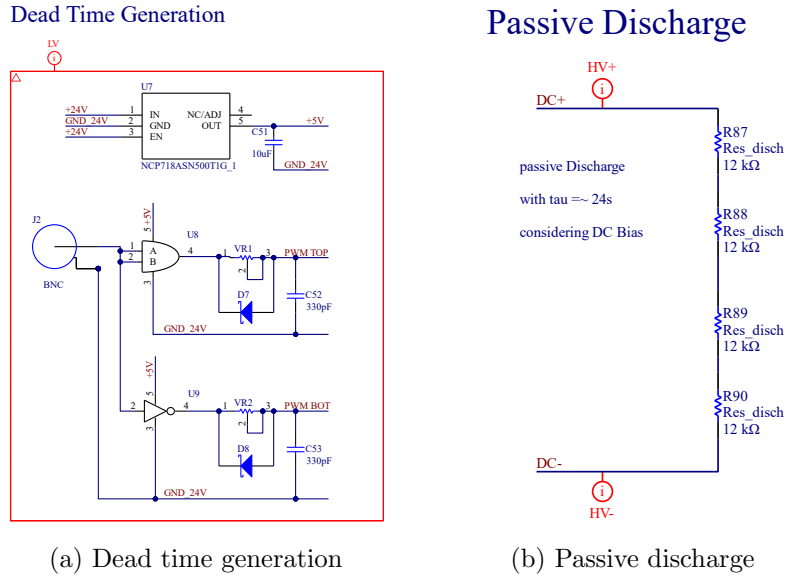


Figure 6-21: Peripheral safety circuits

A passive discharge circuit is added in order to avoid the presence of high voltage in the circuit when the source is removed.

6.8.3 Layout Demonstrator PCB

As described at the beginning of chapter 6.8, the layout of the half-bridge is of utmost importance. In order to guarantee a successful operation, parasitic inductances should be reduced as much as possible, especially in the commutation loop. After comparing several layout architectures found in literature, the final choice is made in favor of the layout depicted in fig. 6-22.

This layout is an adaption of the design of [7], with some modifications to make it suitable for the final application target in a three-phase inverter. The commutation loop is indicated for one top/bot switch pair with red arrows, the gate loops with green arrows. This layout provides a low commutation loop inductance, easy scalability to a desired number of parallel semiconductors, and high volumetric density of

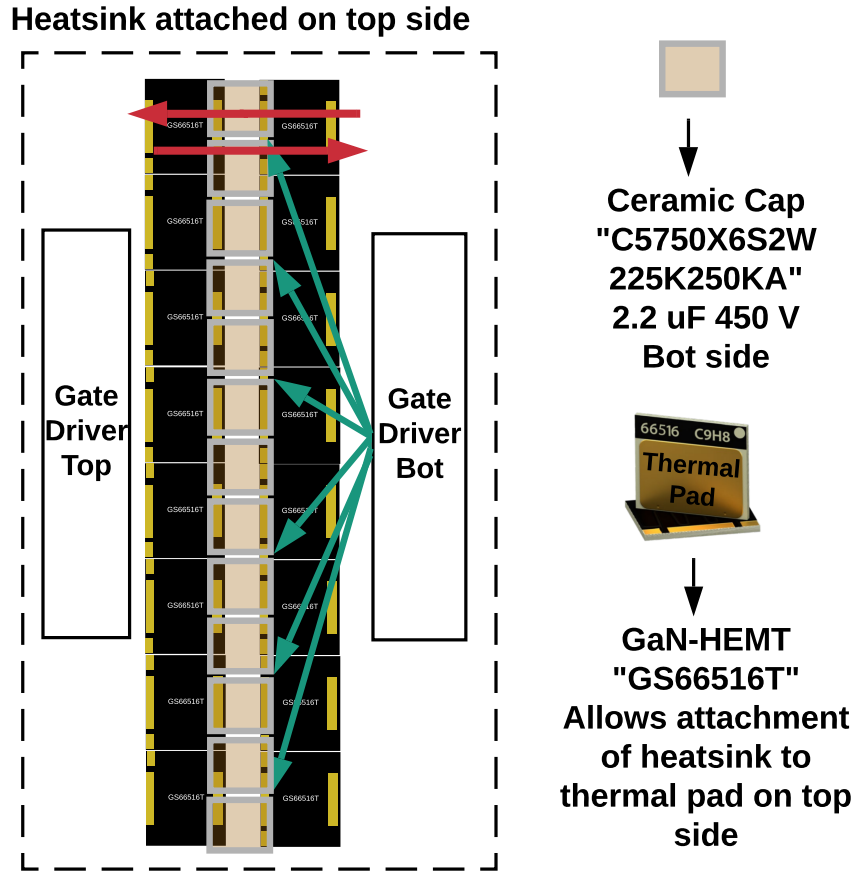


Figure 6-22: Final layout of the half-bridge, illustrated for eight parallel semiconductors

the circuitry. The heatsink can easily be attached to the top side of the PCB and the AC busbar on the PCB can be located between the switches, which is further visualized in fig. 6-23. As the gate-drive loop inhibits asymmetries between the parallel semiconductors, this loop has to be designed carefully. A practical test will focus on evaluating switching behavior and oscillations between the gates.

Fig. 6-23 highlights the commutation loop in the vertical PCB stack-up for one bottom and top switch. The white arrows in the figure mark the direction of currents during switching. Vias are depicted in blue. Through the design technique demonstrated in fig. 6-23, the parasitic inductance is reduced through flux cancellation. The current flow is in the opposite direction on adjacent layers, though a large portion of the magnetic field cancels out, thereby reducing the parasitic inductance [7].

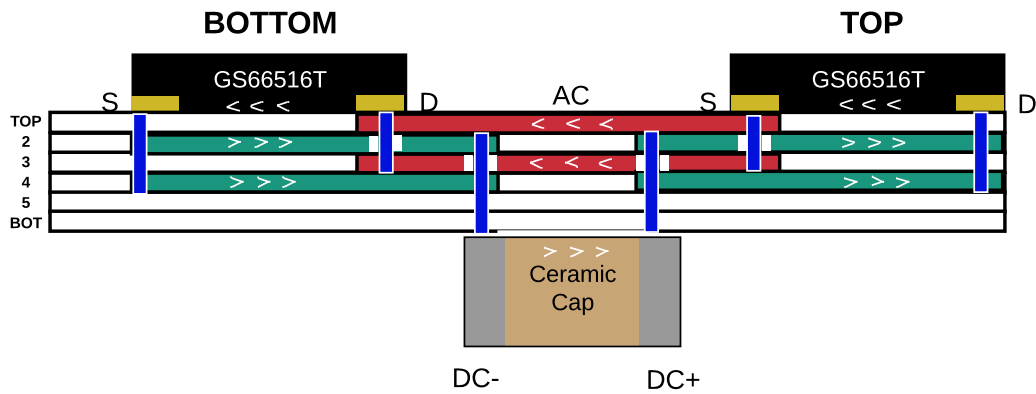


Figure 6-23: Design of the commutation cell

Another advantage of this design is, as mentioned, the location of the AC line on the top layer. Heavy copper PCBs allow thick copper layers up to 1 mm on the outer layers and the AC track can be connected to the heatsink by a thermal interface material. Both of these measures help to cope with the high currents and corresponding losses in the AC trace. The following images visualize the final PCB design, which was created in Altium. Fig. 6-24 depicts the top side of the PCB. The parallel switches of the half-bridge are located on the top side of the PCB. Due to the thermal pad on the top side of the GaN semiconductors, an easy interface to a heatsink is possible.

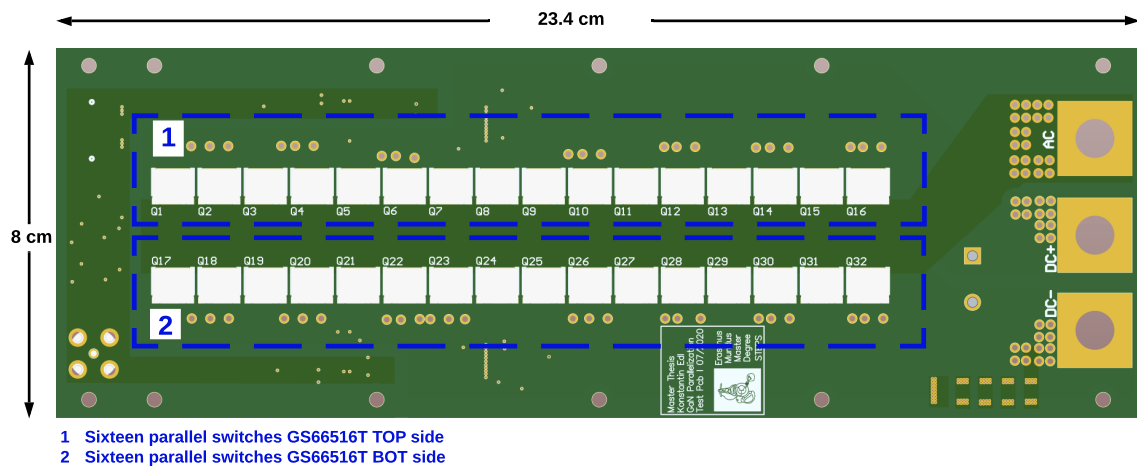


Figure 6-24: Top side of the PCB

The bot side of the PCB contains peripheral circuitry and test points of the individual switches. An electrolytic capacitor was added in order to provide the energy for the double-pulse test in the period T_1 and make it independent of the output impedance of the voltage source. In the final inverter, this capacitor is not necessary.

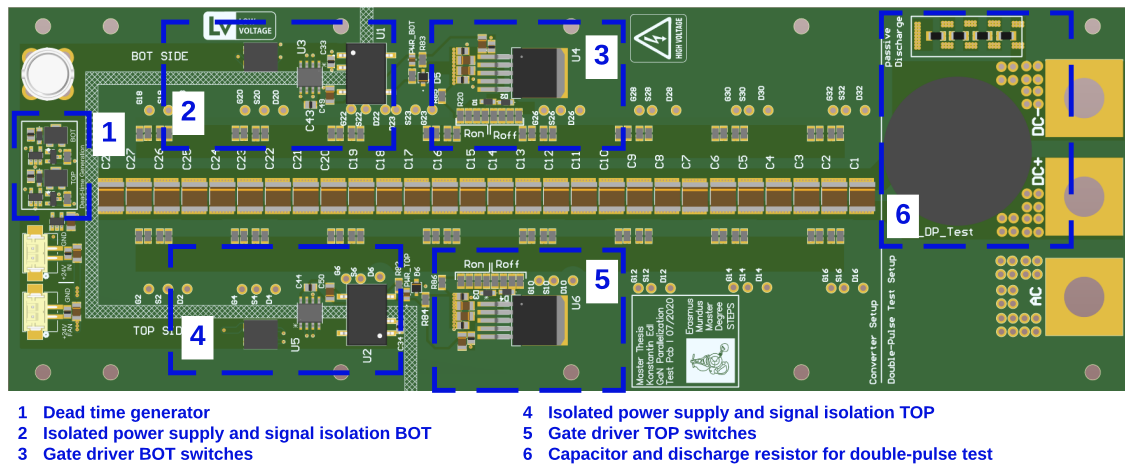
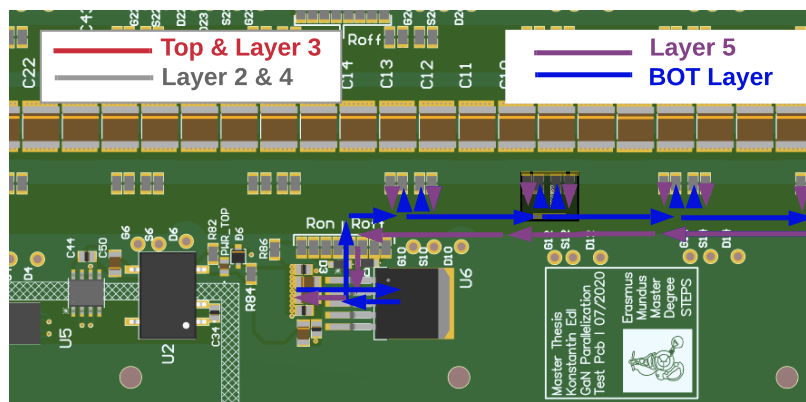


Figure 6-25: Bot side of the PCB

Fig. 6-26 highlights the commutation loop and the gate drive loop on the PCB. In this configuration, the commutation loop parasitics are equal for each top/bot switch pair, as they are provided with their individual DC-link capacitor.



To keep the difference in gate inductance small, the gate loop area is reduced as much as possible by using adjacent layers for the outward and return path. The layout of the complete gate loop is presented in appendix B.5.

A wide polygon track is used on the bottom layer to connect the gates of the individual switches and the return path is routed through a polygon track on the adjacent layer 5.

The final physical design of the demonstrator can be seen in fig. 6-27.

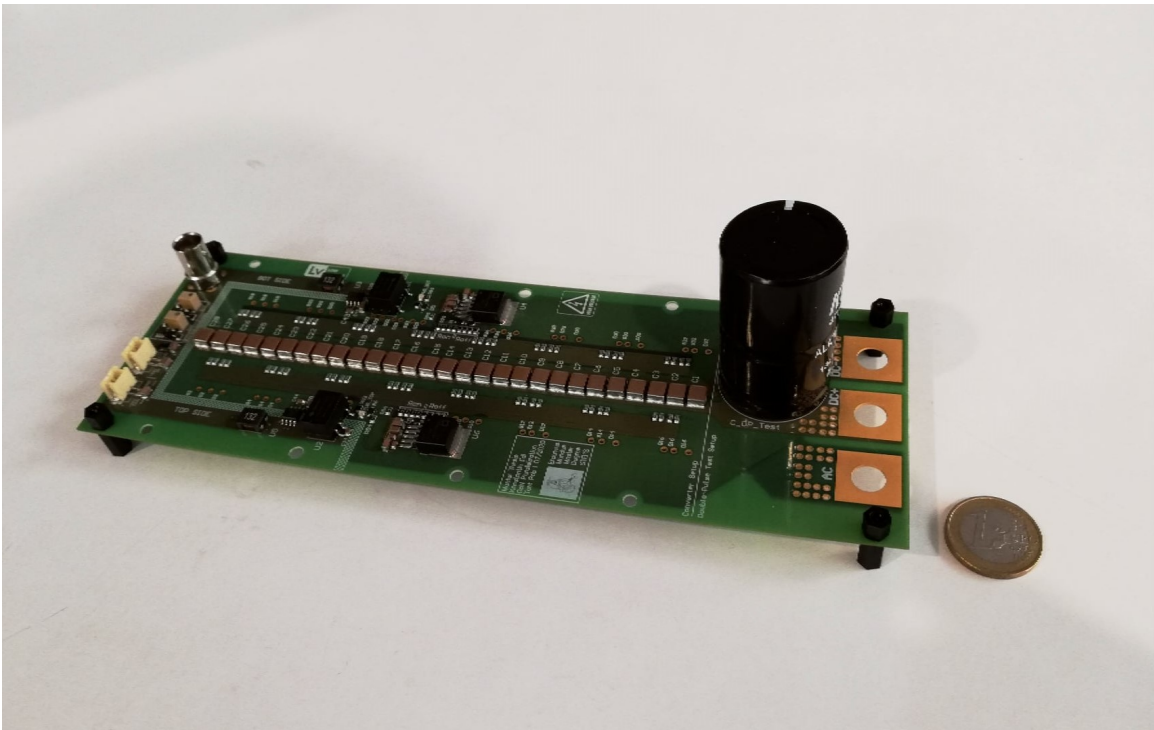
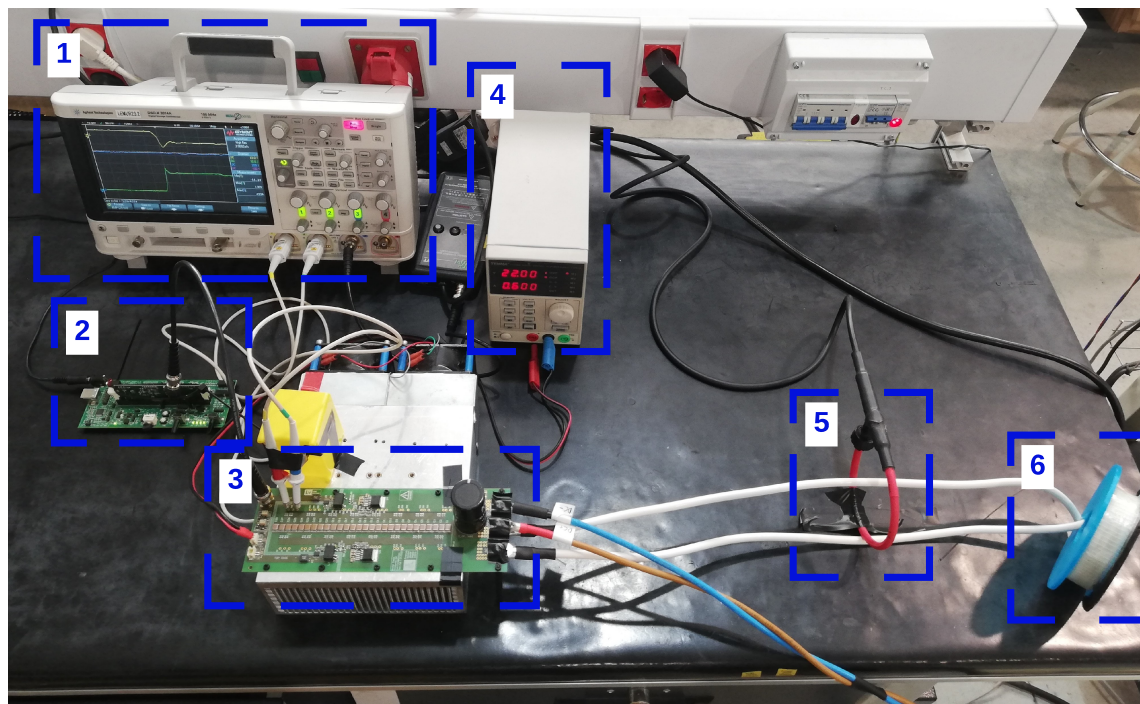


Figure 6-27: Final physical design of the demonstrator

6.8.4 Commissioning Demonstrator PCB

The objective of the commissioning is to analyze, whether the commutation cell with sixteen parallel transistors is able to switch the maximum rated DC-link voltage of 120 V and maximum switched current of 705 A. Furthermore, the transients of inner and outer transistors are compared, in order to evaluate the effect of the unequal gate drive loops.

Based on the setup described in chapter 6.8.1, a double-pulse test is carried out. The double-pulse control functionality is implemented on a TMS320F28335 Digital Signal Processor (DSP) from Texas Instruments. A brooks air coil with an inductance of $6 \mu\text{H}$ was wound specifically for this test, to enable load switching at the required current up to 705 A. The current measurement is performed with the CWT06 AC current probe from PEM Ltd., which is able to measure currents up to 1.2 kA.



1 Oscilloscope Agilent Technologies - DSO-3014A
2 DSP TMS320f28335 - Peripheral explorer kit
3 GaN Parallelization demonstrator PCB

4 Adjustable voltage supply TENMA - 72-10480
5 AC current probe PEM Ltd. - CWT06
6 Brooks air coil $6 \mu\text{H}$ - self-made for this test

Figure 6-28: Laboratory setup of the double-pulse test

Double-Pulse Test Results

Despite the highly experimental nature of these tests, full functionality of the chosen design could be verified. Fig. 6-29 illustrates the measured waveforms of the double-pulse test at a DC-link voltage of 160 V and 705 A. The DC-link voltage is increased to 160 V to compensate for the voltage drop during current ramp-up. In this manner, the actual voltage of 120 V is switched off.

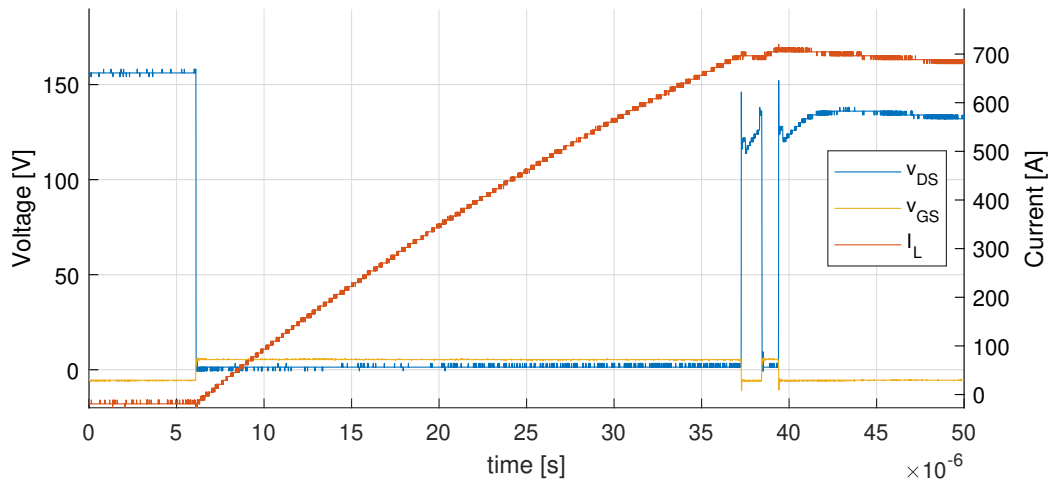


Figure 6-29: Waveforms of the double-pulse test at 120 V, 705 A for outer transistor Q18

The measurements of the double-pulse test depict the current in the test inductor I_L , Gate-Source voltage v_{GS} , and Drain-Source voltage v_{DS} . It has to be noted at this point that for the measurements, an oscilloscope with a maximum sample rate of 2 Gsa/s was used due to availability. As the sampling is unequal throughout the time base and increased during the fast switching transients, the measurements hold validity, however, generally, a higher sample rate is desirable. For reference, the actual oscilloscope image corresponding to fig. 6-29 is given in appendix B.6.

Switching Measurements

Fig. 6-30 displays the turn-on and turn-off transient in detail. It can be seen that both turn-on and turn-off represent clean switching, without sustained oscillations in v_{GS} . The switching transients reveal a fall time of 15 ns during turn-on and a rise

time of 13 ns during turn-off. The increased voltage before turn-on and after turn-off corresponds to the free-wheeling period of the opposite switch.

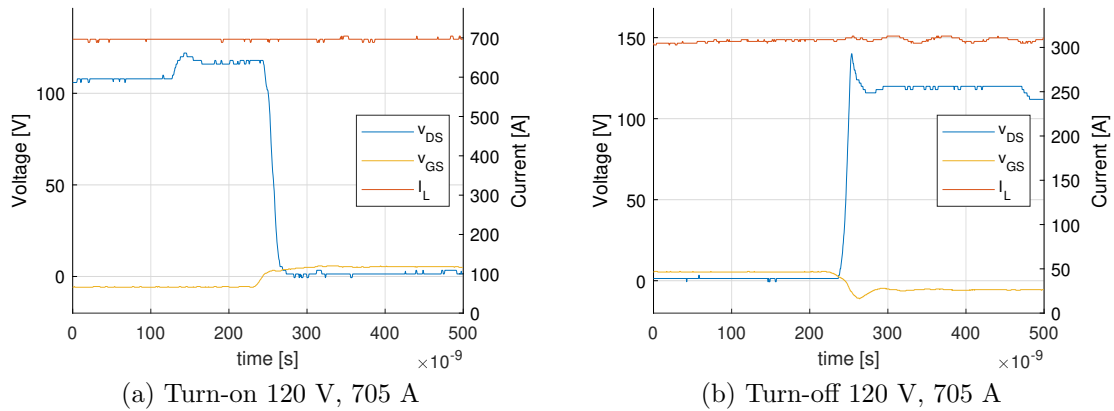


Figure 6-30: Switching transients at 120 V, 705 A for outer transistor Q18

Despite the fast switching, the overshoot during turn-off is only 27 V, indicating the successful design of a low inductive commutation cell. In appendix B.7, B.8, further turn-on and turn-off measurements for currents ranging from 200 A to 700 A are presented.

Evaluation of Parallelization

In order to identify potential mismatches in the switching dynamics of the parallel transistors, the transients are plotted together in fig. 6-31. Each of the curves was measured in a separate switching test, maintaining the same trigger point for v_{GS} . Through this comparison, differences in the waveform-shapes can be identified, indicating mismatches in circuit parasitics between the parallel transistors.

Fig. 6-31 reveals good agreement of the switching transients among all transistors. The allocation of transistor number and position can be done by the help of fig. 6-24. In terms of overshoot, equal numbers can be identified and in general fig. 6-31 indicates good parallelization of the transistors.

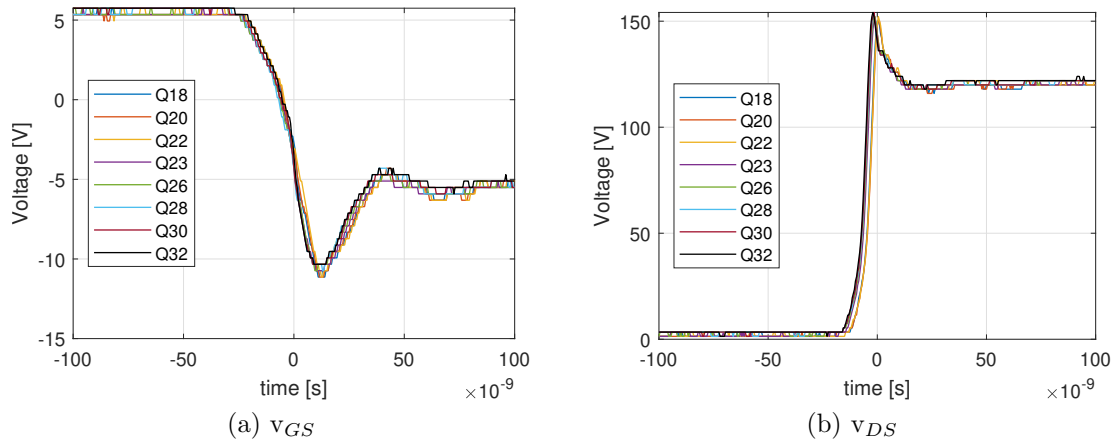


Figure 6-31: Comparison of switching transients of the parallel transistors

Thermal Evaluation

The objective of the thermal evaluation is to gain further insights into the parallelization and investigate the temperature distribution of the transistors. For that reason, the double-pulse test curve is continuously repeated, once the inductor current safely returns to zero. The waveforms of the test can be seen in appendix B.9.



Figure 6-32: Thermal image of the PCB

As the bus-bar temperature climbs quickly, few losses can be injected into the switches, before critical temperature close to the electrolytic capacitor is reached. At the operating point seen in the thermal image of fig. 6-32, it is visible, that bus-bar temperature close to the electrolytic capacitor is already around 86.3 °C. In contrast, no significant information about the temperature distribution among the parallel transistor can be obtained. As previously mentioned in chapter 6-22, the PCB design allows simple adaptation to reduce losses in bus-bars, e.g., the use of heavy copper tracks, and adapt the half-bridge for continuous operation. These adaptations are subject to future developments and can enable a meaningful thermal evaluation.

Chapter 7

Conclusions

In this thesis, the potential of HESSs and the feasibility of a GaN traction inverter for electric racing motorcycles were analyzed.

Chapter 4 provided an overview of the powertrain configurations of electric sport motorcycles and evaluated the current prototype's performance limits. An increase of the inverter's current capability was identified as an effective measure to improve the torque in the lower speed regions. For battery-only energy storage, the removal of the intermediate DC/DC converter and the increase of nominal battery-pack voltage was recommended.

Chapter 5 presented a holistic investigation of HESSs. Several HESSs topologies were reviewed and the semi-active topologies selected as most promising architectures for further analysis. An optimization of HESSs and the subsequent comparison with conventional battery-only ESSs was carried out for a typical MotoStudent drive cycle. The investigation yielded similar gravimetric power and energy density, however, less volumetric density of HESSs. Based on these conclusions, battery-only storage should be favored over HESS for electric motorcycles in the MotoStudent competition.

Chapter 6 demonstrated the design and simulation of a GaN traction inverter. Through an electrical and thermal co-simulation, sixteen GaN semiconductors were identified as minimum number of parallel transistors per switch to fulfill the requirements. As no information on such high numbers of parallel devices in literature exists, a feasibility study was carried out and a demonstrator PCB created. The full func-

tionality of the parallelization with sixteen devices could be verified by test. Due to these promising results, the feasibility of a complete GaN traction inverter for the electric racing motorcycle is confirmed.

Chapter 8

Future Developments

The previous chapters identified the development of a GaN traction inverter as highly beneficial in order to improve the power density of the powertrain. On the contrary, HESS could not achieve significant advantages over conventional pure battery storage. Further developments should thus follow the GaN traction inverter approach rather than the hybrid energy storage.

For the development of the GaN traction inverter, the feasibility of the high number of parallel chips could be verified. Further research should be conducted in:

1. The design of a complete three-phase traction inverter. Based on the half-bridge design presented in this thesis, the complete inverter development offers further research possibilities. An overall solution, including peripheral circuits (current and voltage measurements), the control of the inverter and communication interface, could be designed. A single PCB, including DC-link capacitors, semiconductors and busbars (DC+, DC-, AC) would be a significant contribution towards high power density. Priority should be given to the overall thermal management of the inverter, potentially including heavy copper tracks on the PCB or a metal-core PCB.
2. The development of overcurrent protection for the switches. As the implemented driver does not offer inherent protection features, more research should be dedicated to overcurrent safety circuits for the switches.

3. Innovative heatsink technologies could further increase power density. As the heatsink currently contributes a major part of the total volume and weight to the GaN inverter. [50] reports the use of honeycomb copper heatsink technologies in the google little box challenge. The usage of similar technologies could be evaluated for the traction inverter.

Chapter 9

Internship Report

In the months before the master thesis, an internship was carried out at the Moto-Student team Wolfast, to familiarize with the team, the electric motorcycle and to gain practical experience. The following report briefly summarizes the accomplished work.

Low Power System Architecture (LPSA)

In the internship, the complete Low Power System Architecture (LPSA) was developed and defined. The LPSA contains the low voltage supply architecture, peripheral safety circuits and the communication of the system. The final schematic can be seen in fig. 9-1.

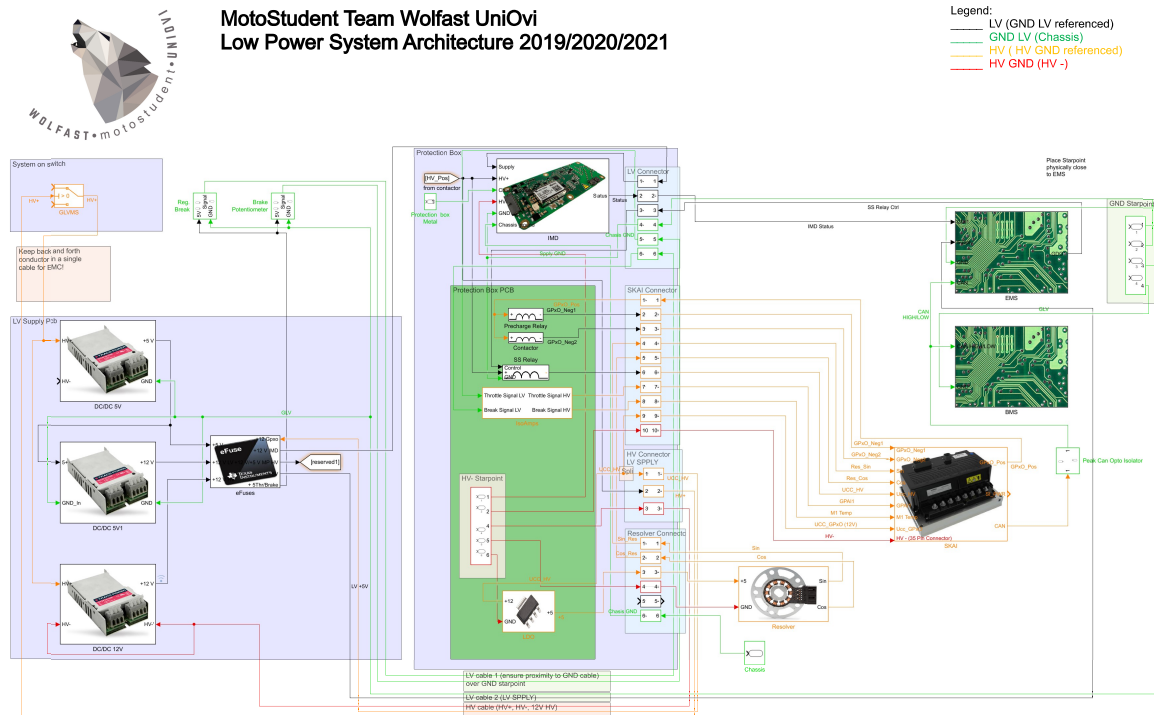


Figure 9-1: Low Power System Architecture (LPSA)

PCB Design (LPSA)

The following PCBs were designed as part of the LPSA. The protection box PCB contains the previously mentioned safety circuitry, for example the DC-link precharge and the inverter DSP-supply solid-state relay. The contactor PCB fulfills the purpose of relay control, relay suppression and reliable distribution of low power HV signals.

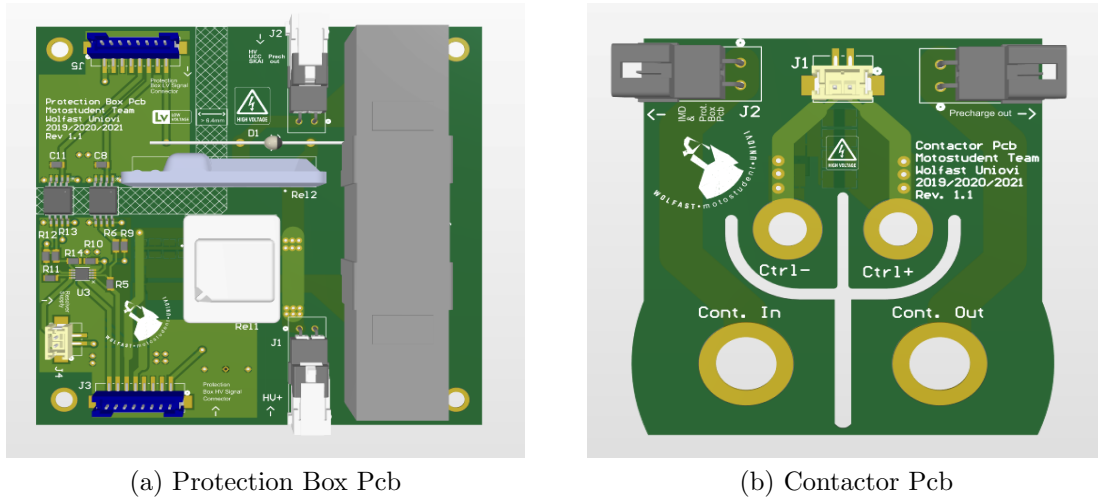


Figure 9-2: PCBs designed as part of the LPSA

Multi-domain Simulation

The multi-domain simulation is an essential tool to develop the control system and characterize the system. It was developed in a previous course of the university and refined throughout the internship. By concatenating several sub-simulations, a complete race simulation of 1200 s could be achieved. With this simulation, the differences between modeled load in Simulink ("Vehicle Body Block") and a more detailed mechanical simulation (SimBike) were revealed. In the Simulink simulation, the power consumption was significantly higher and the battery was drained before the end of the race. As a result, the decision was taken to develop a detailed mechanical model for the multi-domain simulation.

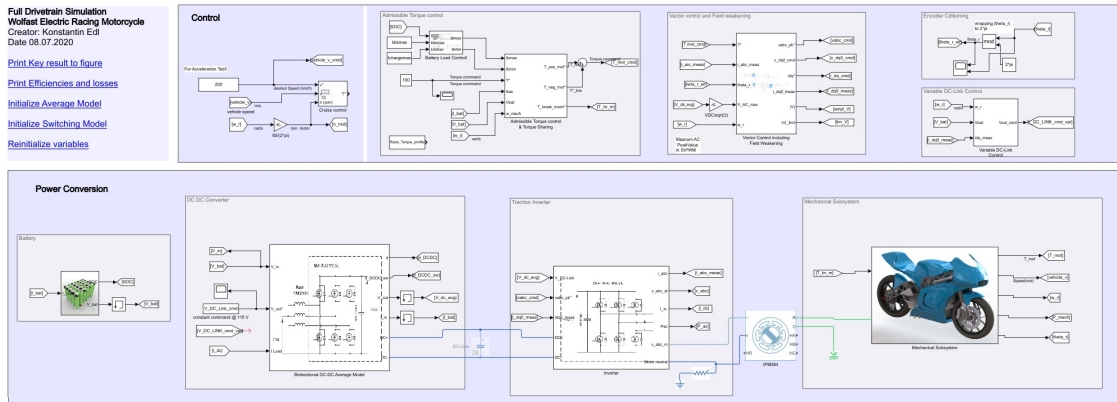


Figure 9-3: Simulink block-scheme multi-domain simulation

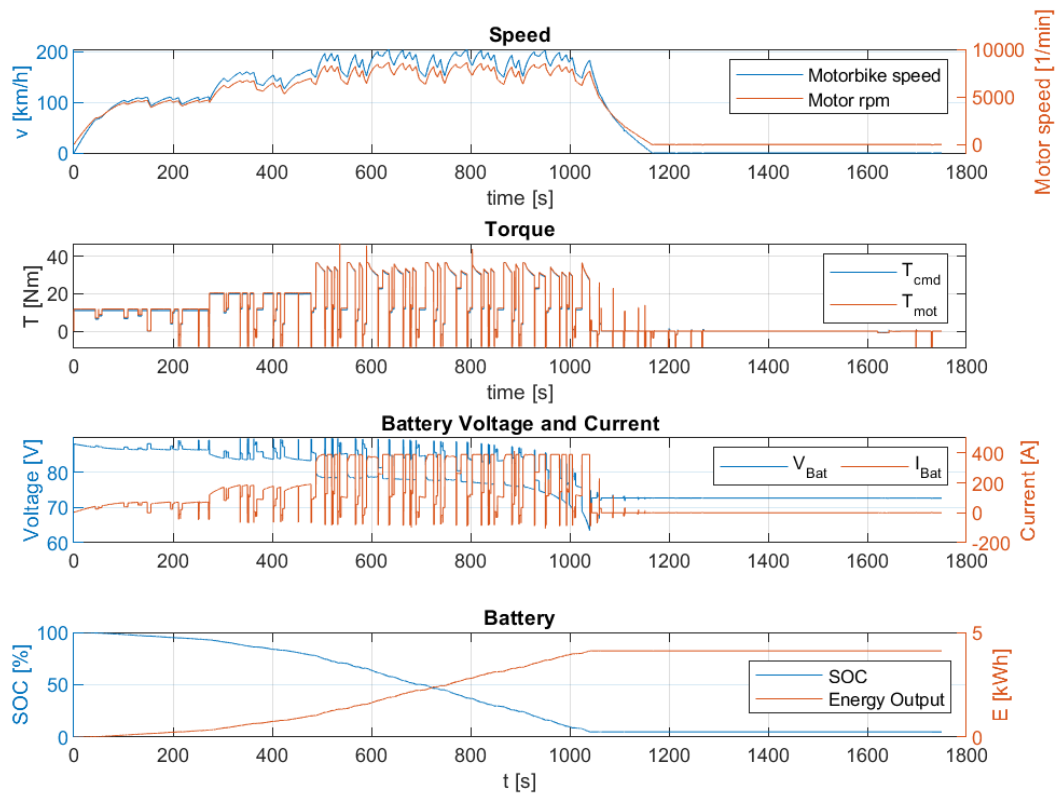


Figure 9-4: Full race simulation results part 1

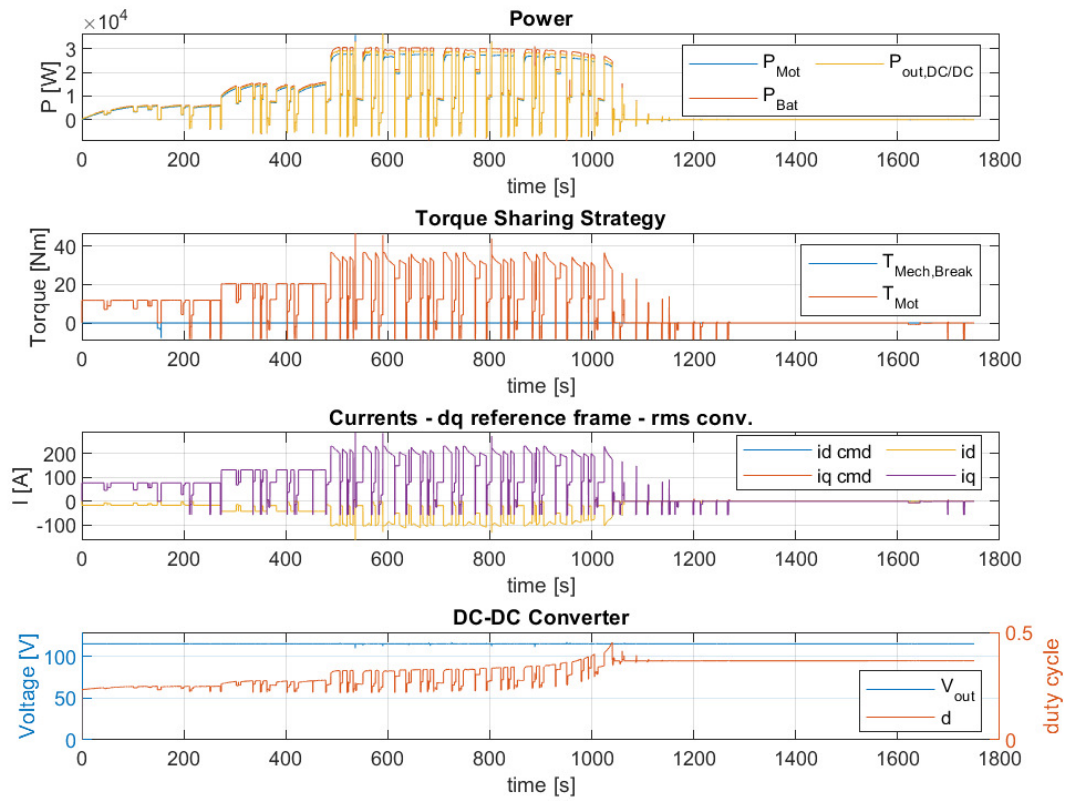
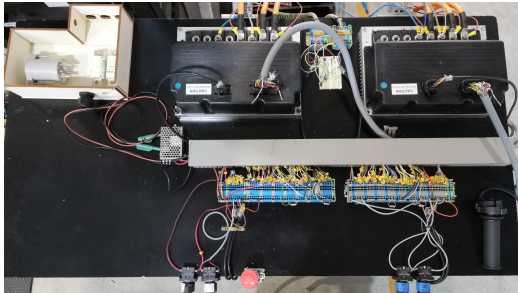


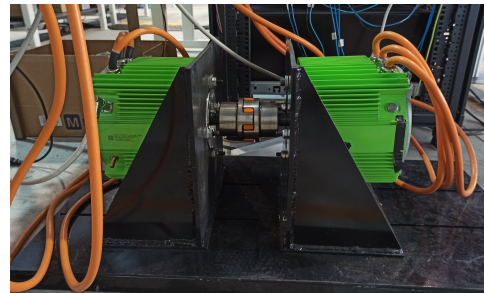
Figure 9-5: Full race simulation results part 2

Dynamometer

The dynamometer test bench was built up in order to carry out realistic powertrain test. As the inverters will eventually be connected in back-to-back configuration (shared DC-link), the power circulates between the machine under test and the load machine. In this setup, the full load profile of the primary machine can be tested and only losses have to be supplied by the grid.



(a) Back-to-back inverters



(b) traction and load motor

Figure 9-6: Dynamometer test bench setup

Appendix A

Synchronous Reference Frame Theory and RMS-Convention

In order to establish clarity for the elaborations in the thesis, the naming conventions and the synchronous reference frame theory are introduced in the following.

Conventionally in electrical machine theory, the electrical quantities are denoted with a superscript letter, signaling the reference frame and a lower script letter distinguishing stator and rotor quantities as in i_{qs}^r . Since the analysis deals with a synchronous motor with permanent magnets, all electrical quantities refer to the stator circuitry. Additionally, the complete investigation will be performed in the synchronous rotor reference frame. Thus for simplicity, these super and subscripts will be omitted. Furthermore, it should be highlighted that the RMS-convention is chosen for the rotor reference frame. Consequently, all values in the dq-reference frame reflect the RMS value of a single-phase quantity.

Given the following three-phase system :

$$v_a = \hat{V} \cdot \cos(\omega_e \cdot t) \quad (\text{A.1})$$

$$v_b = \hat{V} \cdot \cos(\omega_e \cdot t - 2/3 \cdot \pi) \quad (\text{A.2})$$

$$v_c = \hat{V} \cdot \cos(\omega_e \cdot t - 4/3 \cdot \pi) \quad (\text{A.3})$$

The dq-transformation in RMS-convention is structured as follows, assuming the

d-axis is initially aligned with the a-axis at $t = 0$ s.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \frac{\sqrt{2}}{3} \begin{bmatrix} \cos(\omega_e \cdot t) & \cos(\omega_e \cdot t - 2/3 \cdot \pi) & \cos(\omega_e \cdot t - 4/3 \cdot \pi) \\ -\sin(\omega_e \cdot t) & -\sin(\omega_e \cdot t - 2/3 \cdot \pi) & -\sin(\omega_e \cdot t - 4/3 \cdot \pi) \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (\text{A.4})$$

In the dq-reference frame the fundamental dynamic equations of a synchronous machine can be expressed as:

$$v_d = R_s \cdot i_d + \frac{\delta \Psi_d}{\delta t} - \omega_e \cdot \Psi_q \quad (\text{A.5})$$

$$v_q = R_s \cdot i_q + \frac{\delta \Psi_q}{\delta t} + \omega_e \cdot \Psi_d \quad (\text{A.6})$$

$$\Psi_d = L_d \cdot i_d + \Psi_{PM} \quad (\text{A.7})$$

$$\Psi_q = L_q \cdot i_q \quad (\text{A.8})$$

in which

- v_d, v_q are the RMS d,q axis components of the stator phase voltage.
- i_d, i_q are the RMS d,q axis components of the stator current.
- Ψ_d, Ψ_q are the RMS d,q axis components of stator flux linkage.
- R_s is the stator phase resistance.
- Ψ_{PM} is the RMS flux linkage of the permanent magnets.
- ω_e is the angular electrical frequency.

[51]

The motor torque can be derived from the fundamental equations according to:

$$T = 3 \cdot PP \cdot (\Psi_d \cdot i_q - \Psi_q \cdot i_d) \quad (\text{A.9})$$

with

- PP being the number of polepairs of the machine.

It is important to highlight the difference in the factor 3 at the beginning due to the RMS-convention, in comparison to the factor 3/2, valid for the 3/2-peak-convention. In the case of the IPM machine the torque equation may also be expressed as:

$$T = 3 \cdot PP \cdot [\Psi_{pm} \cdot i_q + (L_d - L_q) \cdot i_d \cdot i_q] \quad (\text{A.10})$$

Appendix B

Figures

B.1 Load Condition Calculation Script

```
%Initialisation of Parameters
Ld = 46e-6;           % D-axis Inductance at I = 414 Arms
Lq = 52e-6;           % Q-axis Inductane at I = 280 Arms
fe = 5500*4/60;       %Electrical frequency of operating point [Hz]
we = 2*pi*fe;         %Electrical angular frequency [rad_el/s]
%Complex phasor calculation of the IPM machine
Iq = 414*sqrt(2);     % Iq peak value [A]
Id = -280*sqrt(2);    % Id peak value [A]
I = Iq - (Id*1i);     % Complex current vector (peak values) [A]
PM_Flux = 0.0127;     % Rms value of PM Flux [Wb]
E = PM_Flux*sqrt(2)*we; % Peak value of PM back emf [V]
Xd = we*Ld;           % Q-axis Impedance
Xq = we*Lq;           % D-axis Impedance
V_dq = E+Iq*1i*Xq-1i*Id*1i*Xd; % D,Q - Voltage vector
phi = angle(V_dq) - angle(I); % Phase angle phi [rad]
phi_deg = phi*180/pi; % Phase angle phi [°]
BEMF = abs(V_dq);     % Amplitude of total BEMF [V]
M = BEMF/(121.8/2);   % Modulation index
```

Figure B-1: Script calculating load conditions of operating point

B.2 Modulation Block Scheme Voltage Source Inverter

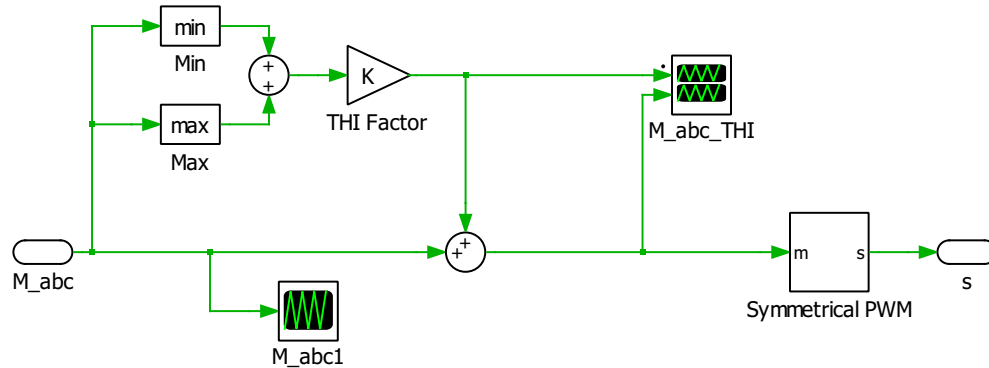


Figure B-2: PLECS block scheme pwm modulation including third-harmonic injection

B.3 Block Schemes DC-Link Ripple Simulation

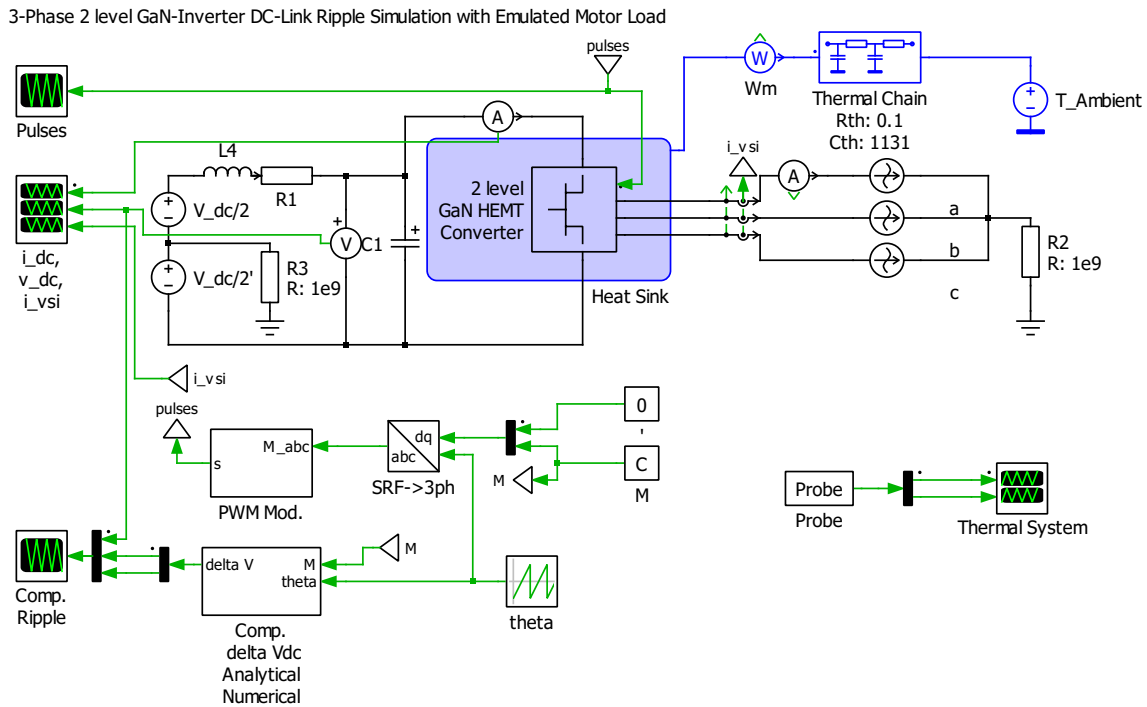


Figure B-3: PLECS block scheme of DC-link ripple simulation

B.4 Block Scheme Comparison Analytical and Numerical Ripple Determination

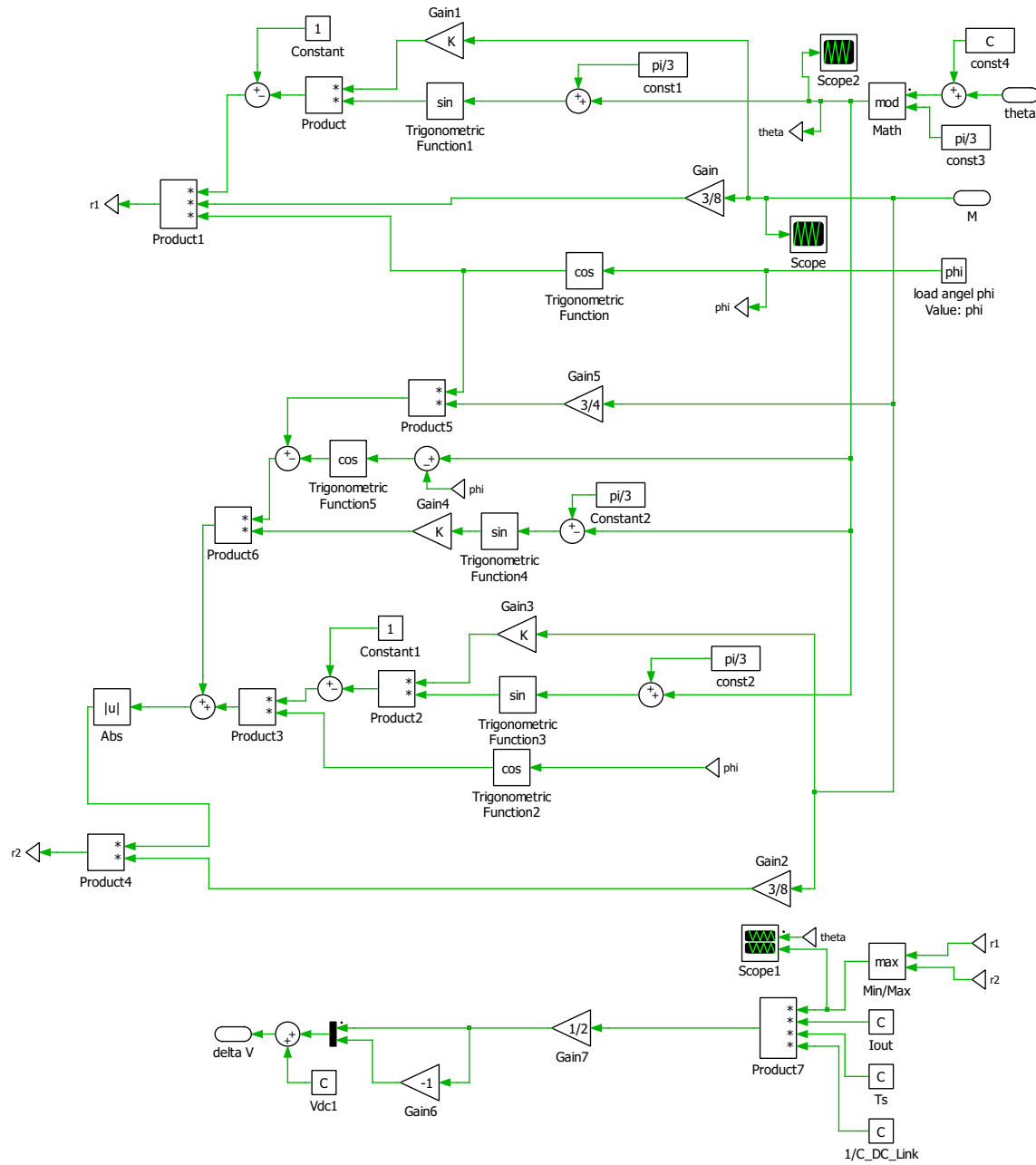
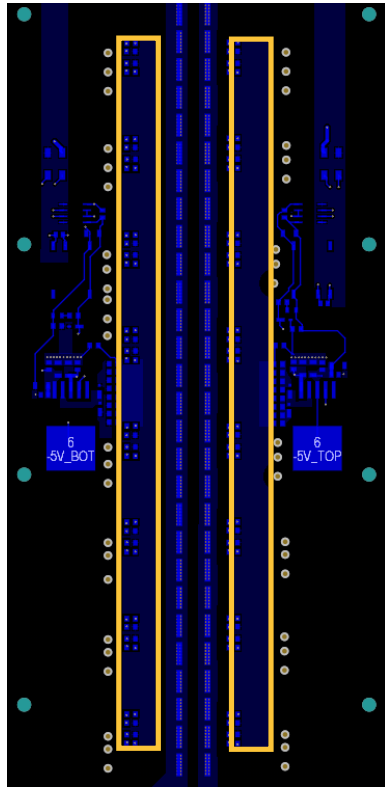
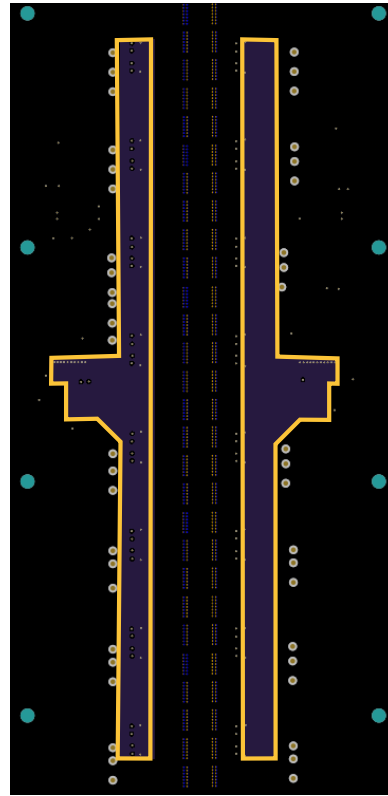


Figure B-4: PLECS block scheme analytical calculation of DC-link ripple

B.5 Layout Gate Loop



(a) Gate signal polygon - Bot layer



(b) Source signal polygon - Layer 5

Figure B-5: Design of gate loop, gate/source polygon tracks marked in yellow

B.6 Oscilloscope Image Turn-off 120 V, 705 A

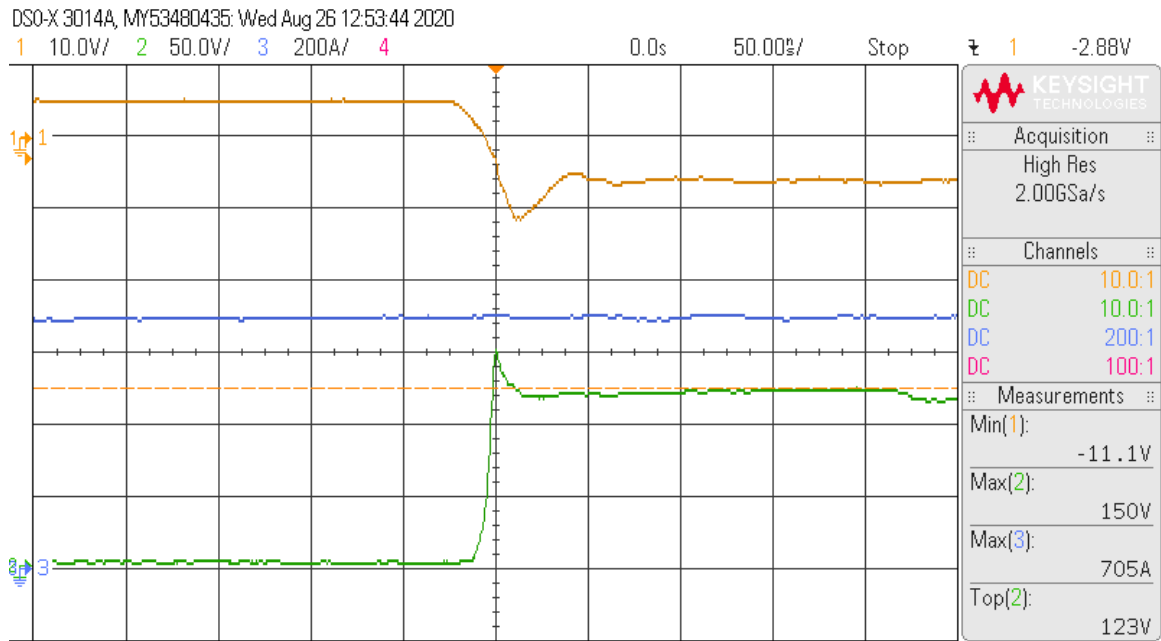
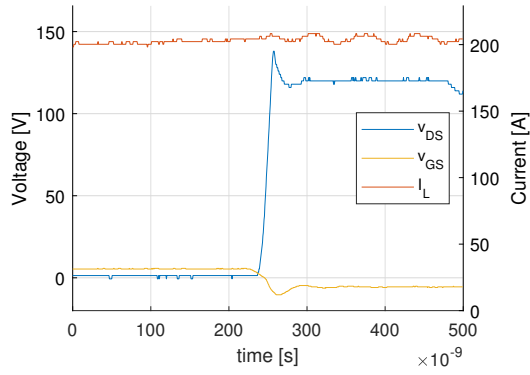
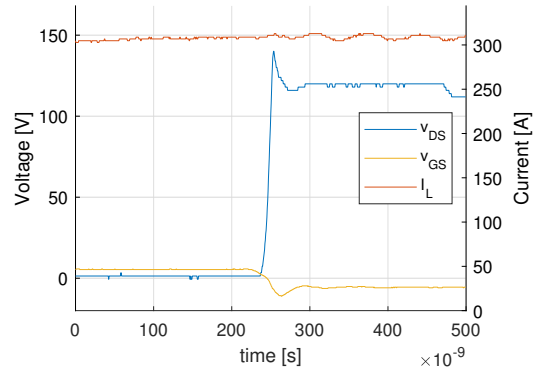


Figure B-6: Oscilloscope image of turn-off transient at 120 V, 705 A showing: v_{GS} (yellow), v_{DS} (green) and I_L (blue)

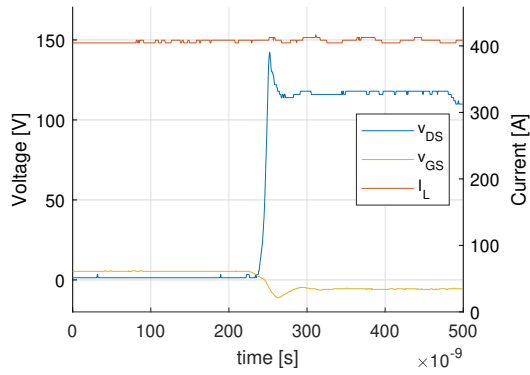
B.7 Turn-off at 120 V, Various Current Levels



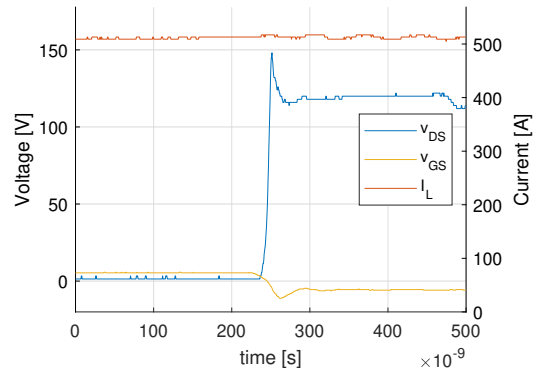
(a) 120 V, 210 A



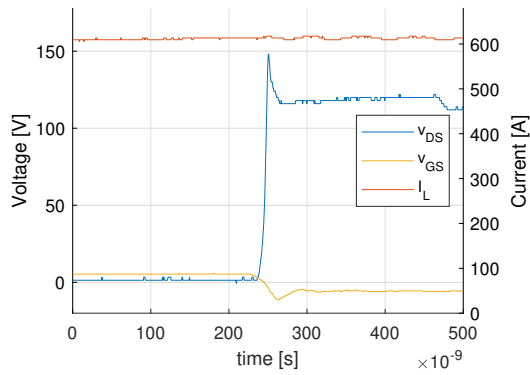
(b) 120 V, 313 A



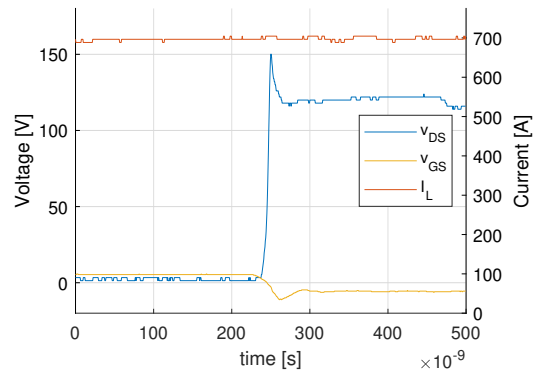
(c) 120 V, 417 A



(d) 120 V, 517 A



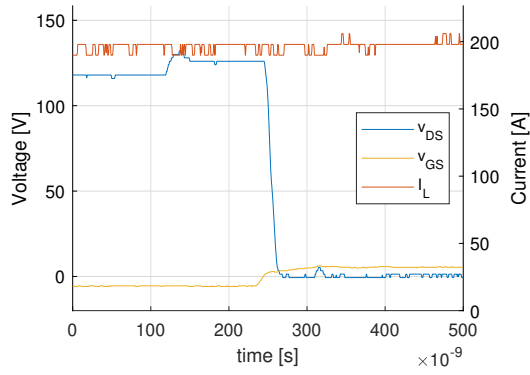
(e) 120 V, 618 A



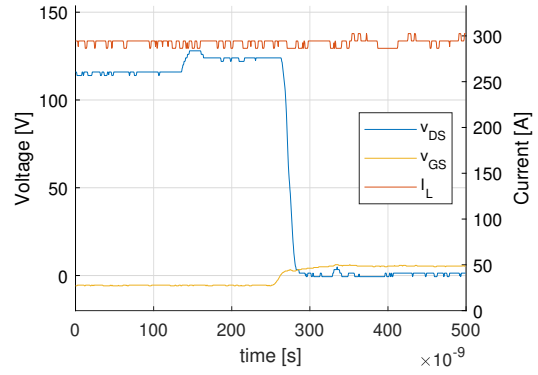
(f) 120 V, 705 A

Figure B-7: Turn-off at 120 V and currents up to 705 A

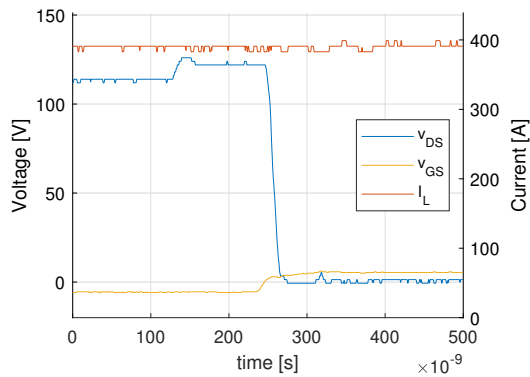
B.8 Turn-on at 120 V, Various Current Levels



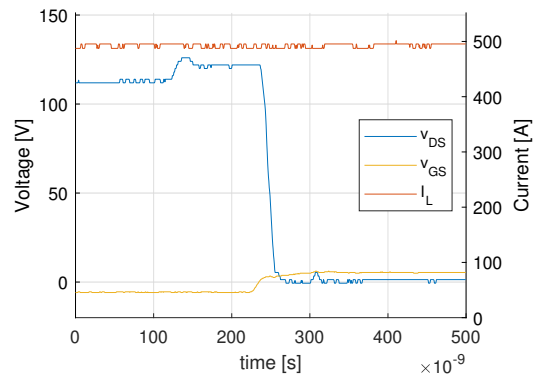
(a) 120 V, 206 A



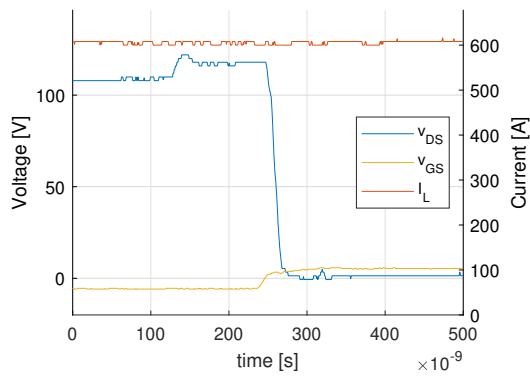
(b) 120 V, 303 A



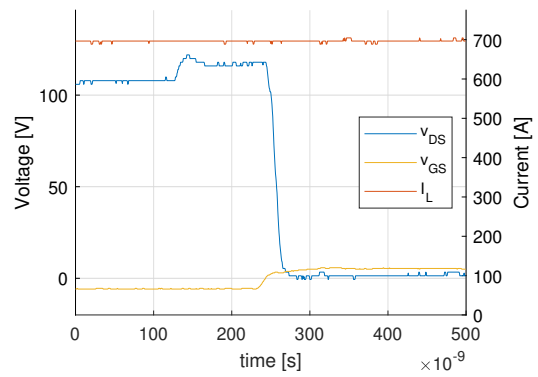
(c) 120 V, 399 A



(d) 120 V, 504 A



(e) 120 V, 616 A



(f) 120 V, 705 A

Figure B-8: Turn-on at 120 V and currents up to 705 A

B.9 Continuous Double-Pulse Operation

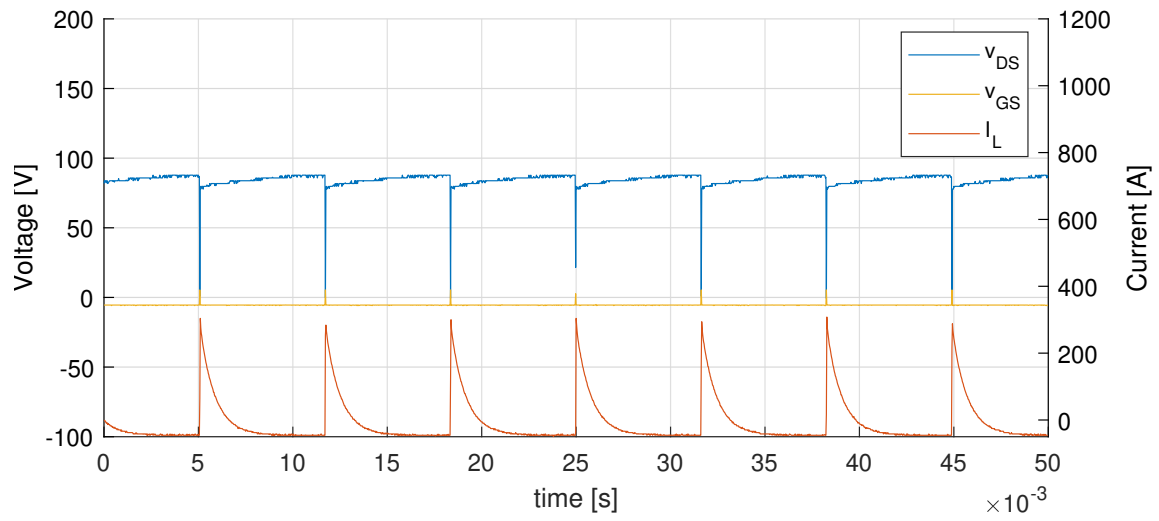


Figure B-9: Continuous double-pulse test to inject losses and evaluate the thermal system

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