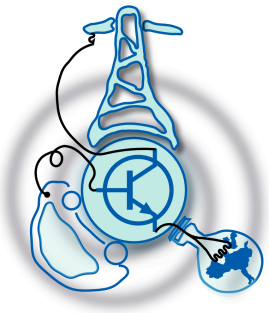
Design, Development and Preliminary Analysis of a Battery Cell Equalizer Based on Resonant Electronic Transformer



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Abstract

This work will consist on the research and analysis of a modular Electronic Transformer (ET) suitable for working in a battery equalizer. The ET will consist on an resonant isolated converter where the resonant inductance is integrated in the transformer. A simulation of the system will first show how with a basic control of the input bridge, the equalizer works, but no zero current switching (ZCS) is achieved, thus, efficiency is low. Methods to reduce the peak current of the ET will be also shown. A specific gate control topology will be proposed in this work. The resulting modulated topology provides high efficiency through soft switching, being valid for simple battery cell equailizer as it does not require either a central control or feedback loops. The effect of tolerances in the performance of the system will be finally assessed.

Keywords

Cell Equalizer, Electronic Transformer, Resonant Converter, Zero Current Switching, Tolerances Effect

Acknowledgments

To my classmates and professors from the Master Course and to SEA research group. To my family and friends.

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1. Introduction

Energy storage systems are used in many applications such as automotive, industrial, aerospace, etc. For each application, these storage systems need to fulfill certain requirements of reliability, security and energy demand. To fulfill the requirements, the combination in series of several cells can increase the overall level of voltage [1]. Cells are storage systems which often provide low levels of voltage.

As cells are connected in series, energy imbalance and different voltage levels among the battery cells may happen [2], [3]. This is a typical event known as the difference of the State-of-Charge (SoC), usually produced by internal and external sources. Internal sources include differences in manufacturing storage volume, internal impedance and self-discharge rate. External sources are mainly caused by temperature or multi-rank pack protection ICs, which unequally consume charge from the cell pack. Also, the concept of SoC is directly connected to the voltage level of each cell. The SoC parameter is measured in %. If one cell is at 100% SoC, it means that it has reached its maximum rated voltage. On the other hand, when the cell is at 0% SoC, it is at its minimum voltage.

The SoC difference among the cells affects the entire battery bank. The cells with higher and lower levels of SoC will define and limit the properties of the whole storage system. This can imply that the battery bank is not used efficiently, because when one cell reaches its maximum charge, the charging process of all cells must stop, as charging current is shared among them. In a similar way, during the discharging process, when one of the cells reaches its minimum SoC, the discharging process must cease. Fig. 1-1 shows the previous explanation.

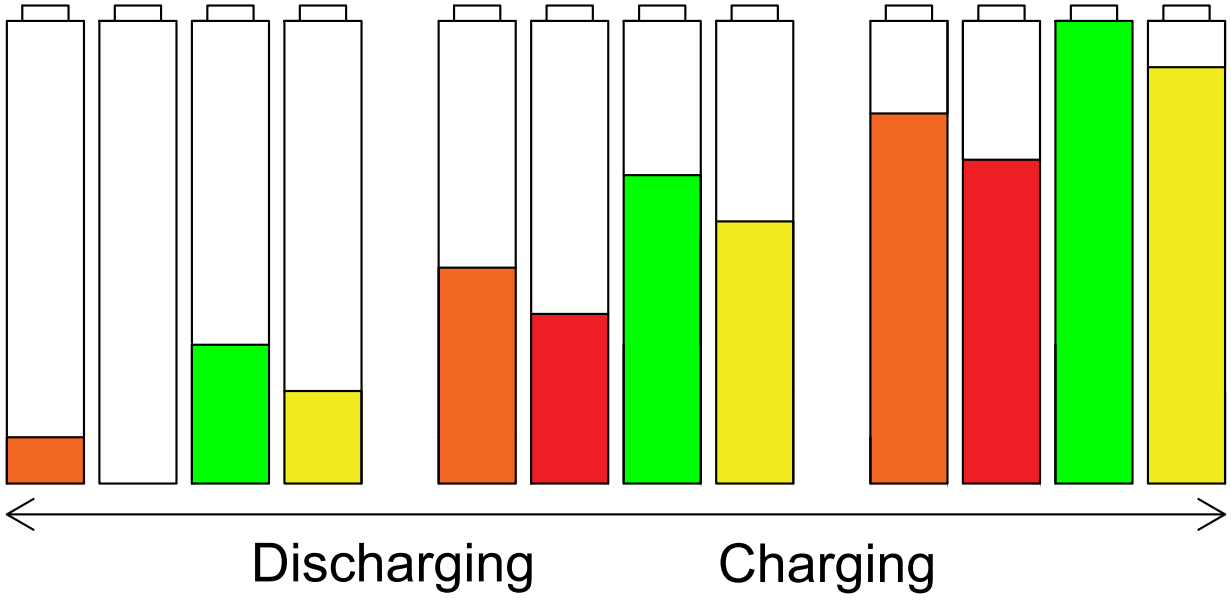


Figure 1-1: Imbalance produced in the SoC of different cells during the charging or discharging process [1].

In order to overcome this problem several solutions have been proposed. The aim of the proposed solutions is to balance or equalize the voltage among the cells connected in series in a battery pack.

This work will show the research of a possible equalization solution consisting on various modular ET connected with a proposed algorithm to control the input bridges. This ET is a topology which is currently under research in the SEA research group at the University Of Oviedo.

First of all, the objectives of the work and the state of the art of equalizers will be covered. After that, a simulation in PSIM will be performed showing the topology of the equalizer and how with a basic control of the input bridge the equalizer works, but no ZCS is achieved. Methods to reduce the peak current of the system will be also seen. Then, a new control algorithm will be proposed to control the input bridge of the ET, with the purpose

of providing ZCS during the equalization. The simulation and main waveforms of this new method will be shown and explained. This new implementation will try to reach a high efficiency, low cost, simple design and small size of the prototype. Finally, the conclusion and future works and trends will be commented.

2. Objectives

The main objective of this work is the design, validation and analysis of an equalizer comprising various ET working together to balance different input cells. A new gate control topology will be implemented with the purpose of achieving ZCS in the converters. A correct simulation of the system with this topology will be evaluated.

3. State of the Art

The main idea of an equalizer is to make equal all the voltages in the different cells connected in series in a battery pack. Therefore, the charging process does not stop when one of the cells reaches its maximum voltage value. In the same way, the discharging process does not stop when one cell reaches its minimum rated value. Equalizer topologies can be classified in different categories. The most important subcategories are two: passive methods, that dissipate energy (less efficient), or active methods, that ideally do not lose energy during the process (more efficient). Fig. 3-1 shows a classification of various topologies for cell balancing. Passive methods extract energy from the higher charged cells, and dissipate this energy through resistors, until voltages of all cells are equalized, to keep the charging process working. Active cell equalizing methods use external circuitry to remove charge from cells with higher voltage and move it to cells with lower voltage.

Active methods can be categorized as capacitor based, inductor or transformer based, and power converter based [4]. Capacitor based cell balancing is also known as charge shuttling equalization. These methods use external storage elements (usually capacitors) for storing energy and shuttling the energy among the cells. There are two main shuttling topologies: Switching capacitors topology and single switched capacitor topology. In switching capacitors, the total number of capacitors needed is one less than the number of cells while in single swiched capacitor only one capacitor is needed to balance all cells.

Inductor or transformer balancing methods use inductances or transformers to move energy from one cell or group of cells to another cell or group. The equalization time is lower than capacitor based methods, but the cost is increased due to the transformers and

inductances. Moreover, since switching frequency is usually high, filter capacitors are also needed to filter the high frequency.

Energy converters used for cell balancing have a fully control of the balancing process. Usually, solutions consisting on power converters are more efficient but they also imply more complexity and cost.

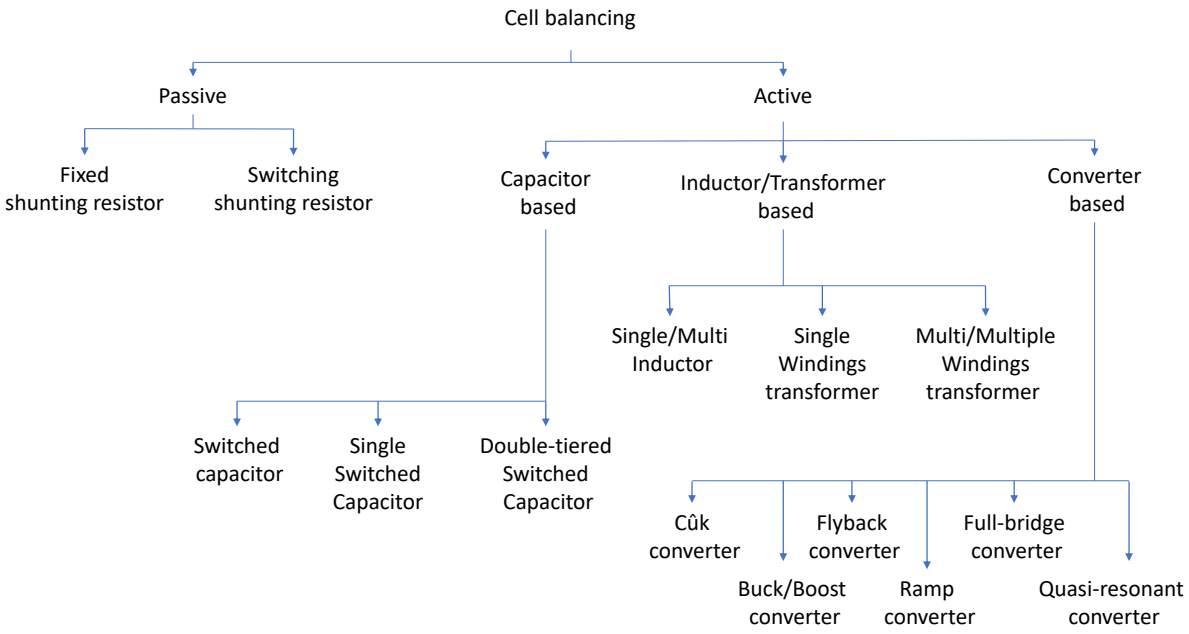
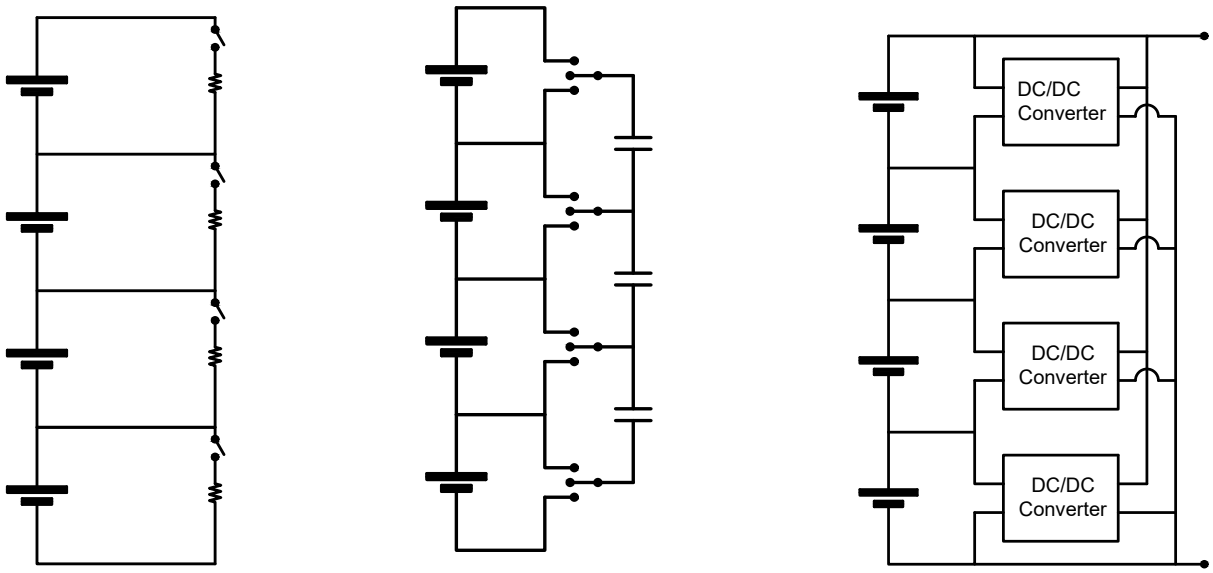


Figure 3-1: Cell equalizer topologies classification [4].

Several methods including passive equalization, switching capacitors schemes, and topologies using magnetic elements or dc-dc power converters are shown in [1]. Fig. 3-2 shows some of those topologies.

Fig. 3-2a shows a switched shunt resistor scheme, in which redundant energy is dissipated from cells close to 100% SoC. This is a reliable method, but low efficient for medium or high power applications. Moreover, this method is used only during the charging process. Two modes can be applied. The first one is that all switches are turned on when charging. This



(a) (b) (c)

Figure 3-2: Topologies for equalizers: a) Passive equalizer, b) Switching capacitors scheme, c) DC/DC converter for each cell [1].

way the cells with higher voltage levels will take more current through the resistors instead of charging the cell, so that cells with lower levels of voltage reach same voltage levels as the others. The second mode implies sensing and switch control, in order to open and close the desired switches for making cells with higher voltage dissipate more energy through the resistors, slightly increasing the overall efficiency.

In Fig. 3-2b the switching capacitors scheme is shown. This method consists on placing a capacitor in parallel with each pair of cells. Therefore, the total number of capacitors needed is one less than the number of cells. The capacitors connection is in series like the cells connection. A pair of switches is also needed for each cell, one that will be connected to the positive of the cell and one to the negative. The output of two pair of switches is the same. Each output is connected to the positive of each capacitor, with the exception of the last output, which is connected to the negative of the last capacitor connected in series. The switches work at 50% duty, which means that energy of cells with higher voltage is stored in the capacitors and when switches change position, the energy is transferred to emptier cells, allowing to balance the voltage among all cells.

Fig. 3-2c shows the connection of a dc/dc converter for each cell. This methodology consists on extracting energy from cells with higher levels of voltage and send this energy to the string. The cells with lower levels of voltage do not send energy to the string, they only receive it from the battery charger, which is connected to the voltage supply.

Advantages and disadvantages of the different topologies are also covered. Table 3.1 makes a comparison among different equalizer solutions in equalization speed, control complexity, applications or efficiency. Other parameters such as number of components, stress or cost may be also considered.

Table 3.1: Comparison of equalization topologies [4].

Topology	**Equalization Speed**	**Control Complexity**	**Applications**	**Efficiency**
Control shunting resistor	Good	Simple	Low Power	Poor
Single switched capacitor	Satisfactory	Medium	Medium/High Power	Medium
Full bridge converter	Very good	Complex	High Power	High

More information related to other equalization techniques and comparison tables is also provided in [5] and [6]. In addition, a more detailed explanation of a topology using a dc/dc converter for each cell can be found in [7].

To finish this section, some topologies of resonant converters are shown in [8]. The paper begins reviewing bus converters and proposes a particular topology of an ET based on a resonant converter that can be seen in Fig. 3-3. This topology comprises an input bridge composed by four switches connected in two legs, a transformer connected to the input

bridge, an output resonant tank and two switches (SRs) that connect the transformer to the output resonant tank. The transformer uses the leakage inductance as the inductance of the resonant tank, and the output capacitor of the topology is actually the capacitor of the resonant tank.

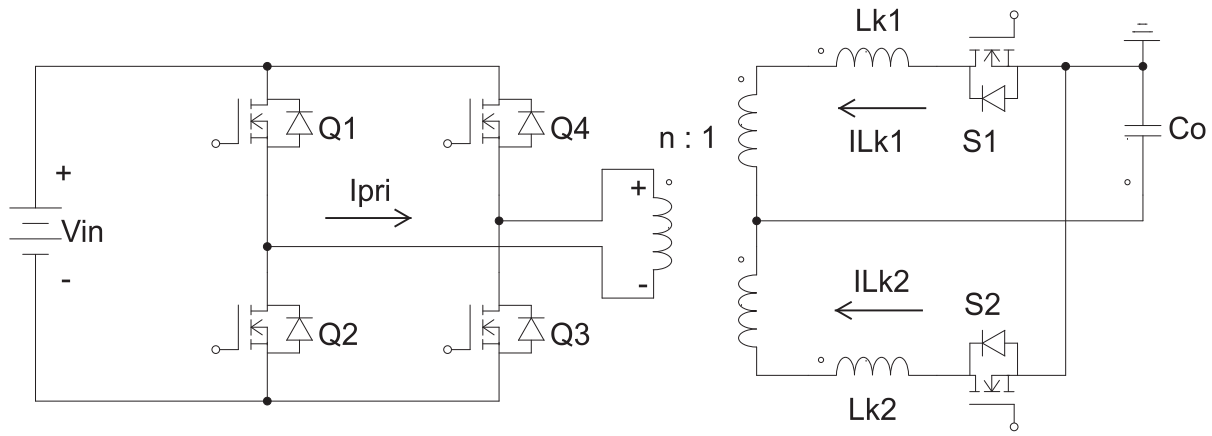


Figure 3-3: Example of a resonant converter schematic [8].

The integration of the resonant inductance in the transformer reduces the size and cost of the converter. Also, the magnetizing current is used to provide zero voltage switching (ZVS) of all switches. The resonance between the output capacitor and the leakage inductance of the transformer can provide ZCS for the output switches, and nearly ZCS for the input bridge switches. No total ZCS could be achieved due to the circulating magnetizing current.

Equation 3.1 defines the current through the leakage inductance when Q_1, Q_3 and S_1 are on, where I_o is the output current, V_{co} the initial voltage of capacitor Co, V_{in} the input voltage applied and I_{ro} is the initial current through inductor Lk. Lk is the leakage inductance of the secondary of the transformer and fulfills $Lk=Lk_1=Lk_2$. With a proper timing design, the initial value of the current I_{ro} should be zero. Equation 3.2 expresses the output voltage in the capacitor Co. This output voltage will be composed by a DC component (with a voltage equal to Vin/n) and a large ripple. Nevertheless, a second stage could easily get rid of this high frequency ripple with its input filter.

$$I_{Lk}(t) = I_o - (I_o - I_{ro})cos(\omega_{LC}t) + \frac{\frac{V_{in}}{n} - V_{co}}{\omega_{LC}Lk} sin(\omega_{LC}t) \tag{3.1}$$

$$Vc(t) = \frac{Vin}{n} - (Io - Iro)\sqrt{\frac{Lk}{Co}} sin(\omega_{LC}t) + \left(Vco - \frac{Vin}{n}\right) cos(\omega_{LC}t) \tag{3.2}$$

These converters can also eliminate body diode loss, something critical for high efficiency applications. Self-driven techniques can be applied to these converters, to reduce the drive loss. A self-driven method is shown in this paper, capable of achieving 95.5% efficiency at 500 W, 12 V, 45 A output. When compared to industry solutions, that method highly increases the power density.

However, in a cell balancing topology, the different input voltages of the cells will produce different current curves in each ET, so that the currents might not finish at the same time. If the input bridges gate signals change at the same time, some of the resonant currents might have a considerable high value at the time that the gate signals change, producing high switching losses. Tolerances in the leakage inductances may also affect to the current shape. The proposed topology of this project will try to solve this problem by controlling the input bridges one by one, making the gate signals to change exactly when the corresponding resonant current reaches a value very close to zero.

4. Topology of the equalizer

In this chapter the topology of the equalizer to be used will be shown. A basic gate control will be applied to check the obtained waveforms. To finish the chapter, various methods to reduce the peak current of the system will be explained.

Up to this point, it has been commented some equalizer solutions from different references. Now, the circuit shown in Fig. 3-3 will be taken for the design of the ET of this work. A modification will be performed over that topology, changing secondary switches S1 and S2 by uncontrolled diodes. The purpose of using diodes is to let the current flow only from the transformer to the output capacitors. In Fig. 4-1 two ET have been used, because there are two input cells. Being scalable and modular, the number of ETs needed in the topology will be the same that input cells used.

The main advantage of this ET topology will be the proposed gate control of this work. The control implementation will be simple and scalable for each ET, which is very important in systems where the inputs are serialized, and problems with shared voltages in the bus may appear. The proposed topology only shares a single clock signal, which is something easy to transmit among adjacent modules with low voltage difference, and redundancy is easy to obtain. In addition centralized control is not reliable against failures, whereas distributed control implies too much complexity.

One disadvantage of the topology is that the number of components is high, which implies higher cost of the system. Also the efficiency can be lower when compared to other options.

The starting parameters to be used in this topology will be the ones seen in Table. 4.1. Note that two values of frequency will be used: the frequency of the resonant tank f_{LC} and the switching frequency fs. The value of the inductance Lk_1 has been calculated with equation 4.1.

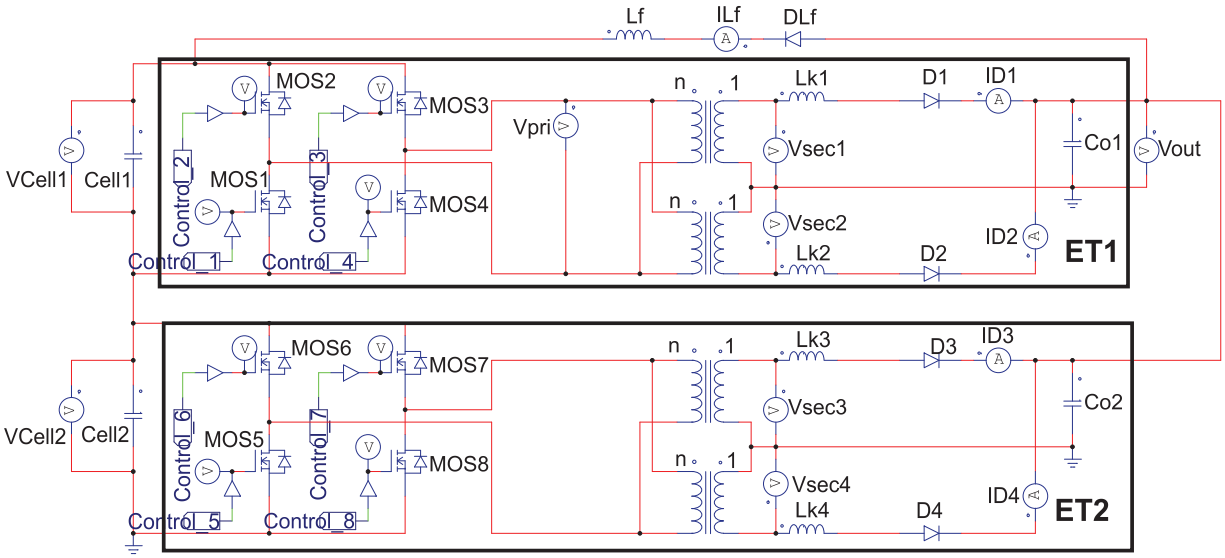


Figure 4-1: Schematic of the connection of two ETs.

Table 4.1: Initial parameters used in the ET.

Cells capacitance	10e-3 F
VinitialCell1	4 V
VinitialCell2	0 V
n	0.5
f_{LC}	800e3 Hz
fs	$f_{LC}/2$ Hz
ω_{LC}	$2\pi f_{LC}$ rad/s
ω**s**	2πfs rad/s
Co1, Co2	1e-6 F
Lk1, Lk2, Lk3, Lk4	3.9619e-08 H
L_f	10Lk1 H

$$Lk_1 = \frac{(\frac{1}{\omega_{LC}})^2}{Co1} \tag{4.1}$$

As it can be seen in Fig. 4-1, two cells have been connected in series, and two ETs have been connected to these two cells. The positive of the output capacitors is connected to an inductance L_f. This inductance stores the energy received in the output and injects it back to the cell pack. The principle of operation is to extract energy from the cells with higher voltage and inject it to the string so that cells with lower voltage reach the ones with higher voltage.

The input bridge will determine the primary voltage of the transformer (Vpri). The secondaries of the transformer will be proportional to the primary, having a voltage equal to Vin/n. When the voltage in the secondary of the transformer is higher than the output voltage, the corresponding leakage inductance has also a positive voltage, and positive current begins to circulate through the corresponding diode. This current will have a resonant shape because of the resonance between the leakage inductance and the output capacitor.

When the output voltage becomes higher than the voltage on the secondary of the transformer, the leakage inductance begins to discharge until the current reaches zero. While there is positive current flowing through Lk, the diode will be directly polarized (voltage in anode higher than in cathode) letting the current flow, but in the moment the current through Lk reaches zero, the diode becomes inversely polarized (voltage in cathode higher than in anode), preventing the current to have a negative value.

4.1 Basic gate control

The only thing that can be controlled in the ETs are the switches of the input bridges. For ET1, the input bridge comprises the switches MOS1 and MOS2 in one leg and MOS3 and MOS4 in the second leg. With the appropriate control of the bridges a resonant current waveform can be achieved. Being a modular system, the same happens to other ETs used.

Before explaining the proposed gate control topology, a basic control of the bridges will be shown in Fig. 4-2.

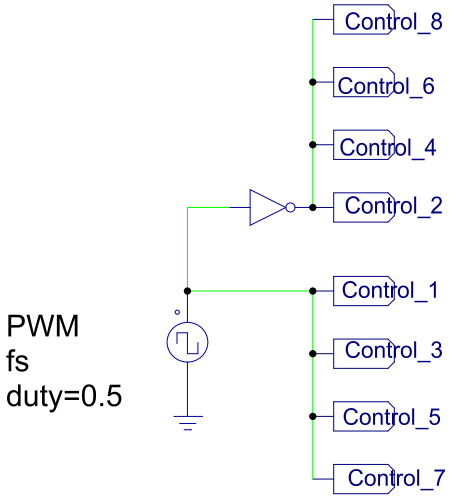
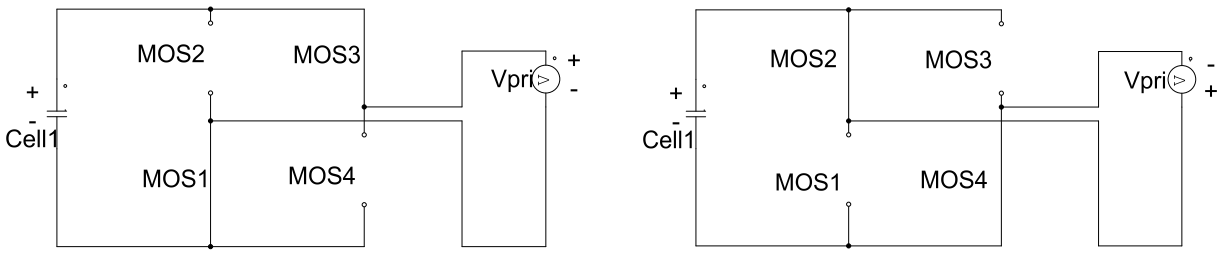


Figure 4-2: Basic control system for the ET.

For ET1, this basic control implies the two circuits shown in Fig. 4-3, each one for each semiperiod of the PWM signal (clock signal). The same is applied for ET2. If there is enough voltage applied to the gate-source of switches 1 and 3, the circuit of Fig. 4-3a is reached in the first semiperiod, where switches 1 and 3 are closed and switches 2 and 4 are open. This makes the primary of the transformer to have a positive voltage, equal to the input voltage. The voltage in the secondary will be proportional to the primary voltage, being Vin/n.

During the other semiperiod, the equivalent circuit is now the one shown in Fig. 4-3b, where switches 1 and 3 are now open and switches 2 and 4 are closed. The primary of the transformer has in this case a negative voltage applied.



(a) Switches 1 and 3 are closed and switches 2 and 4 are open in one semiperiod.

(b) Switches 2 and 4 are closed and switches 1 and 3 are open in the other semiperiod.

Figure 4-3: Equivalent circuits of the input bridge in one period.

4.2 Waveforms obtained in a simulation with the basic control

Let us now perform a simulation of the system shown in Fig. 4-1 with the control of Fig. 4-2. As it can be seen in Fig. 4-4, the currents through diodes D1, D2, D3 and D4 have a resonant shape, produced because of the resonance between the output capacitors Co and the leakage inductances Lk for each ET. The reason for plotting ID1 and ID4 in one graph and ID2 and ID3 in the other is for a better visualization of the difference of magnitude among currents from ET1 and ET2. The current expression that was defined in equation 3.1 is now affected by the inductance L_f and the other leakage inductances of the system.

Fig. 4-5 represents the output voltage obtained over capacitors Co1 and Co2. As it can be seen, this output voltage has non-negligible sinusoidal ripple. The output voltage is formed by a DC component, and a large ripple that can have a negative value. The output voltage expression that was defined in equation 3.2 is also affected by the inductance L_f and the other leakage inductances of the system.

A zoom will now be performed in order to see particularly issues of these resonant shapes. Fig. 4-6 shows the zoom of Fig. 4-4 for the interval between 0.5 msec and 0.505 msec. Fig.

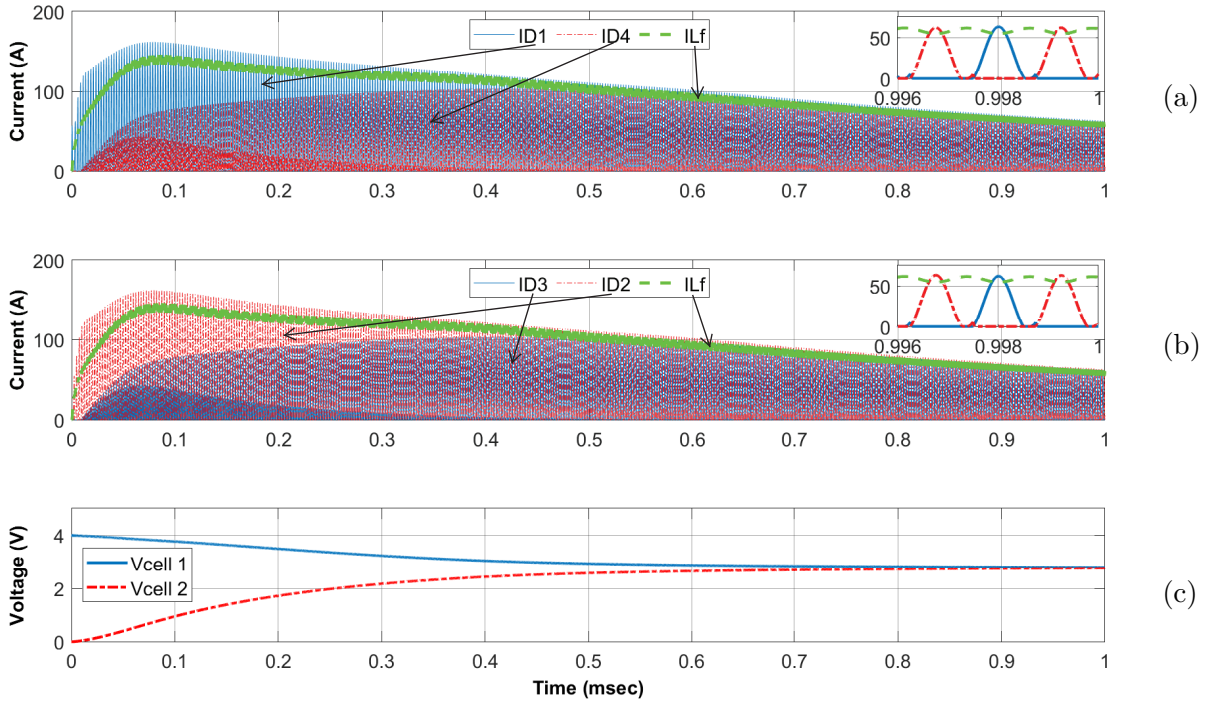


Figure 4-4: Main waveforms for the simulation of the equalizer with the parameters of Table 4.1.

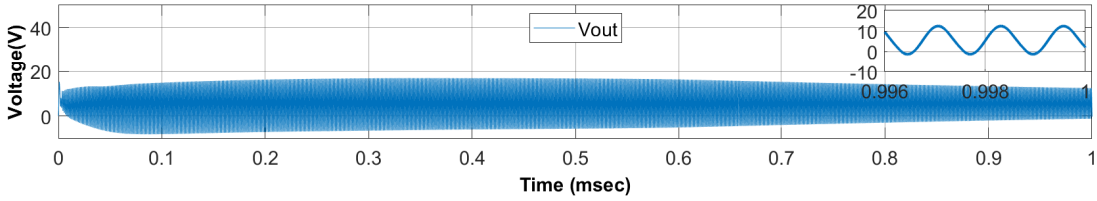


Figure 4-5: Output voltage.

4-6c shows that currents ID3 and ID4 do not fall below zero because the diodes become inversely polarized.

The polarization of diode D3 can be explained with Fig. 4-6d, where the output voltage (Vout) and the secondary of the transformer of ET2 ($Vsec_3$) are compared. When $Vsec_3$ is positive, it will have a voltage equal to $VCell_2/n$. When $Vsec_3$ is higher than Vout, Lk_3 begins to charge. The current flow will have a resonant shape because of the resonance between Lk_3 and Co_2. When $Vsec_3$ is lower than Vout, the current in Lk_3 discharges through diode

D3, until it reaches zero current. While it is positive current flowing through Lk_3, the diode is directly polarized and lets the current flow. Once the current reaches zero, the diode becomes inversely polarized preventing the current have negative sign. Until $Vsec_3$ becomes higher than Vout again, the current will remain zero.

Before the control signal changes, there is a small interval of time where $Vsec_3$ is higher than Vout again, which means that the current begins to resonate again, as it can be seen in Fig. 4-6c. The control signals of the basic control change with current flowing because of this second resonance, therefore, no ZCS is achieved, producing switching losses in the converter.

In Fig. 4-6a it can be seen that the resonant currents through ID1 and ID2 start to increase again in a determined moment before they reach zero current. This can be explained by the fact that before the current reaches zero, $Vsec_1$ becomes higher than Vout, making the inductor Lk_1 to charge again. The same happens with $Vsec_2$ and Lk_2.

Fig. 4-7 shows the resonant currents for the interval from 0.1 msec to 0.105 msec. Fig. 4-7a shows how the resonance is not achieved properly, and the control signals change when the currents through Lk_1 and Lk_2 are discharging, producing high switching losses. This situation occurs because the inductance Lf and the leakage inductances are affecting to the system, varying the ripple of the output capacitor. The voltage difference in the input cells is also affecting. Fig. 4-7c shows how the current through each diode resonate twice in one switching period because of the ripple of Vout, making the diode to become directly polarized again.

One more zoom has been performed in the interval between 0.8 msec and 0.805 msec and represented in Fig. 4-8. All the currents in this interval reach zero, and a second resonance in the same semiperiod is produced because of the secondaries in the transformers and the output voltage differences. It is also appreciated that currents do not reach zero at the same

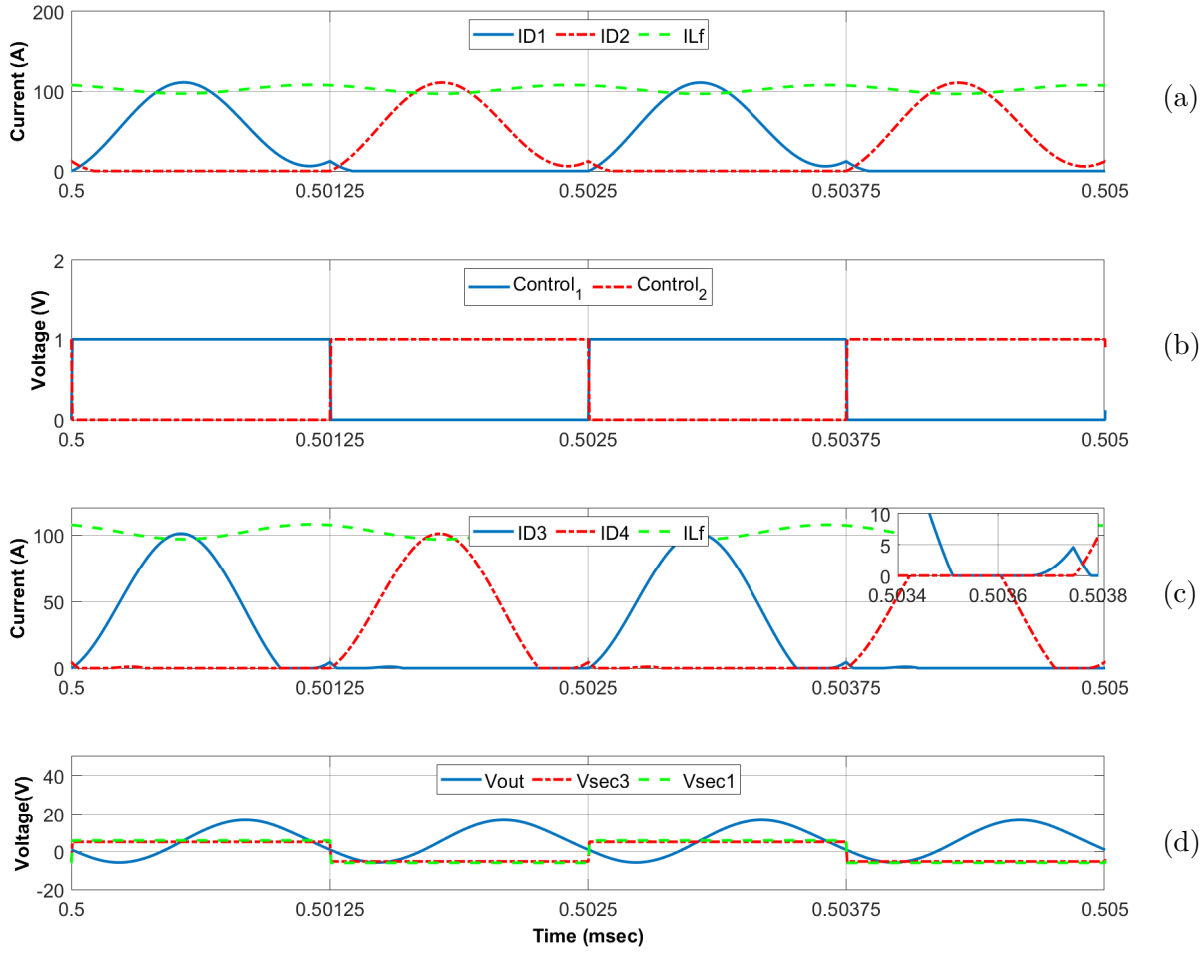


Figure 4-6: Zoom of Fig. 4-4 between 0.5 msec and 0.505 msec.

time. This can be explained with Fig. 4-8d where it can be seen that the secondaries Vsec1 and Vsec3 have different values due to the voltage difference in the input cells. Therefore, the leakage inductances begin to charge and discharge at different times.

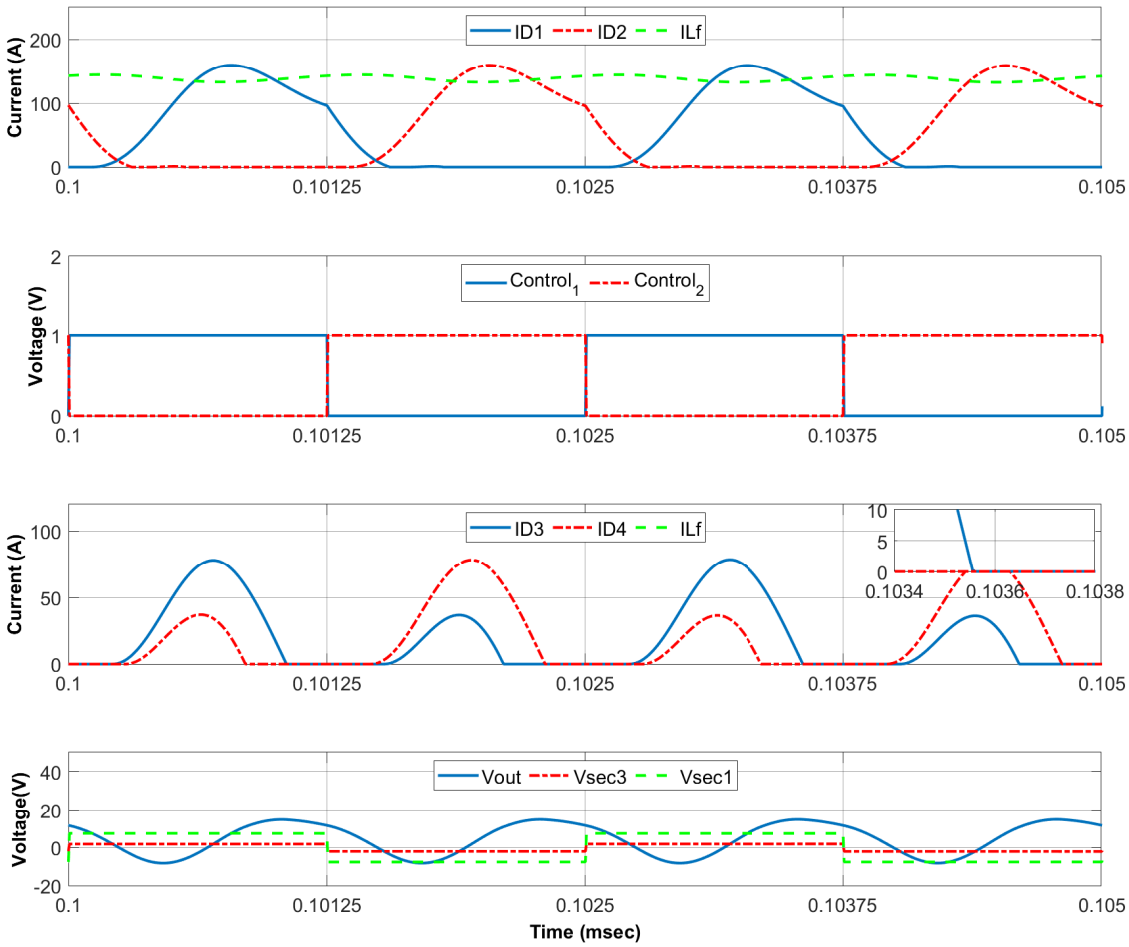


Figure 4-7: Zoom of Fig. 4-4 between 0.1 msec and 0.105 msec.

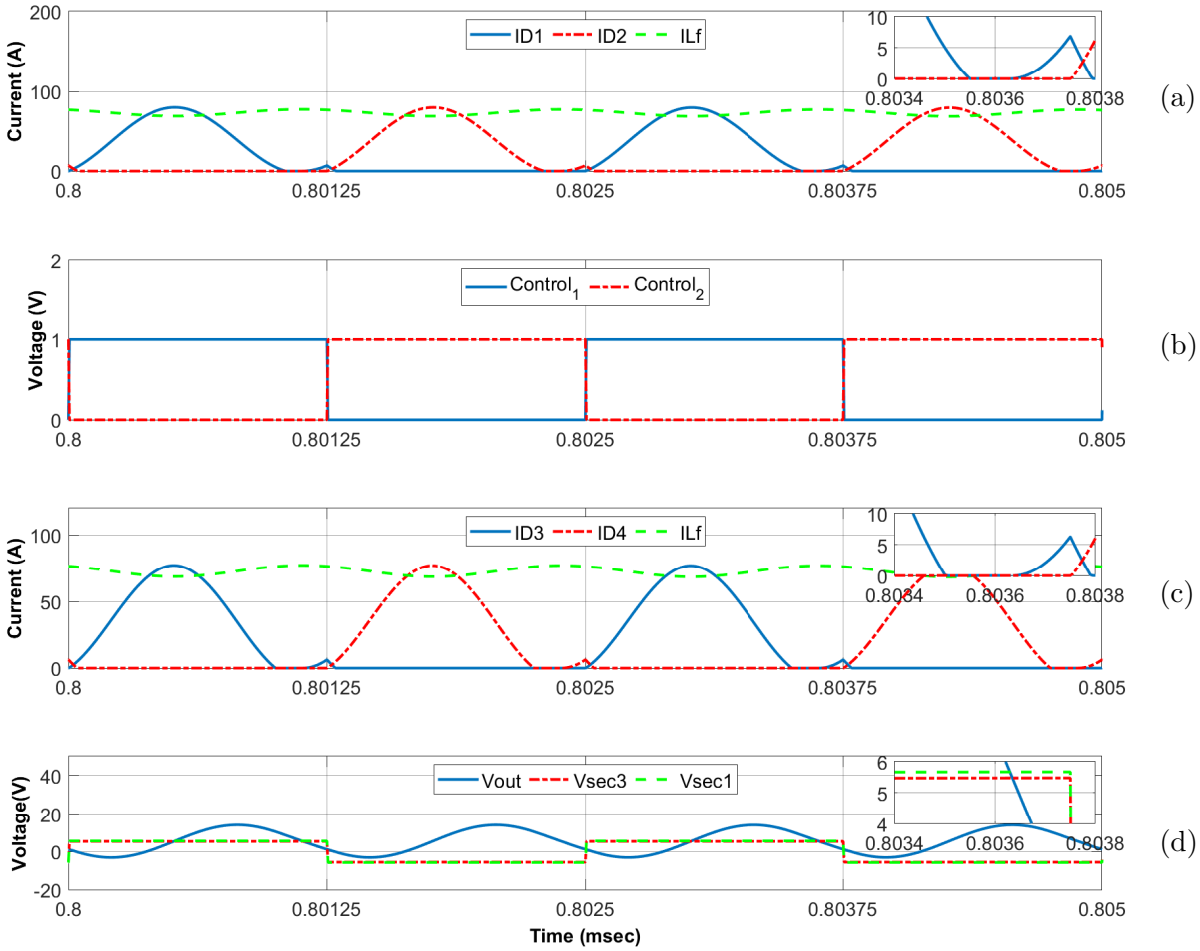


Figure 4-8: Zoom of Fig. 4-4 between 0.8 msec and 0.805 msec.

4.3 Limiting the peak current

This project also focuses on methods to limit the resonant peak current. Various techniques can be applied to reduce the peak current of the converters. The changed parameters of one method will be kept for the next ones.

4.3.1 Reduction of the voltage difference among cells

One of the things that can be done is reducing the voltage difference between cells. This is not really a true method because the equalizer has to be prepared to equalize any voltages that cells have. However, it is really rare to find cells totally discharged and totally charged in the same cell pack. The reduction of cells voltage difference reduces the current peak and also the equalization time. The results of changing VinitialCell_2 from 0V to 3.6V can be seen in Fig. 4-9.

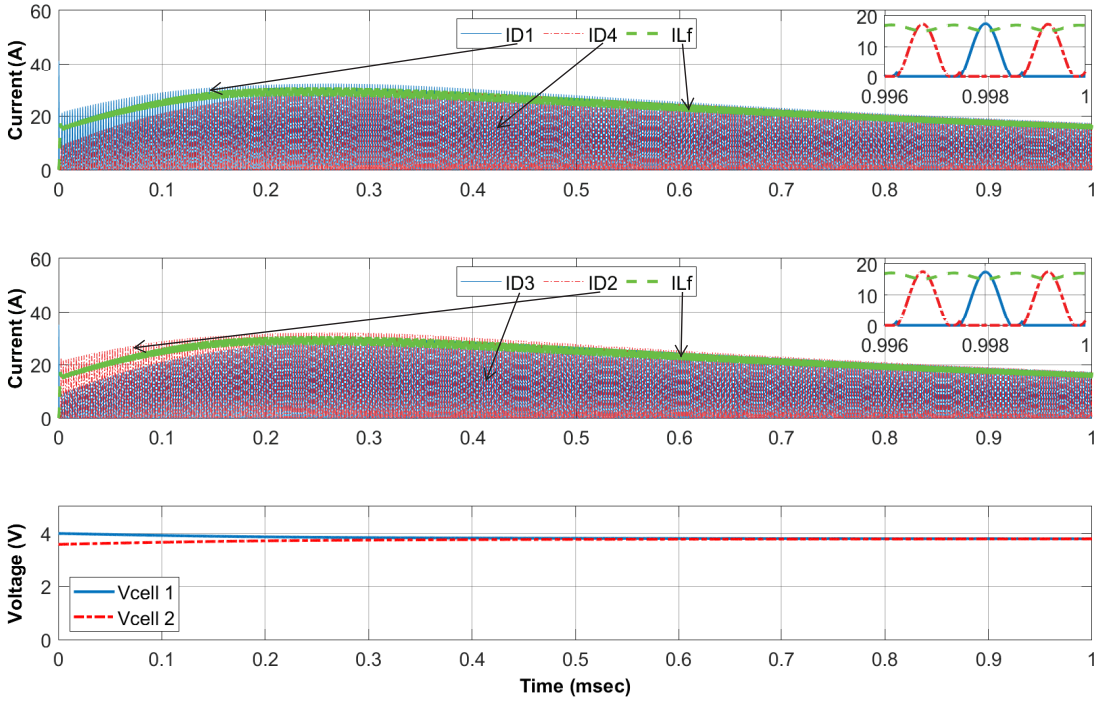


Figure 4-9: Main waveforms for the simulation of the equalizer changing VinitialCell_2 from 0V to 3.6V.

Fig. 4-10 shows a zoom of Fig.4-9 in the interval between 0.1msec and 0.105 msec. In Fig. 4-10c it can be seen how the phenomenon shown in Fig. 4-7c disappears, due to the reduced difference between the cells voltage. In this particular interval, ZCS would be achieved for Fig. 4-10c.

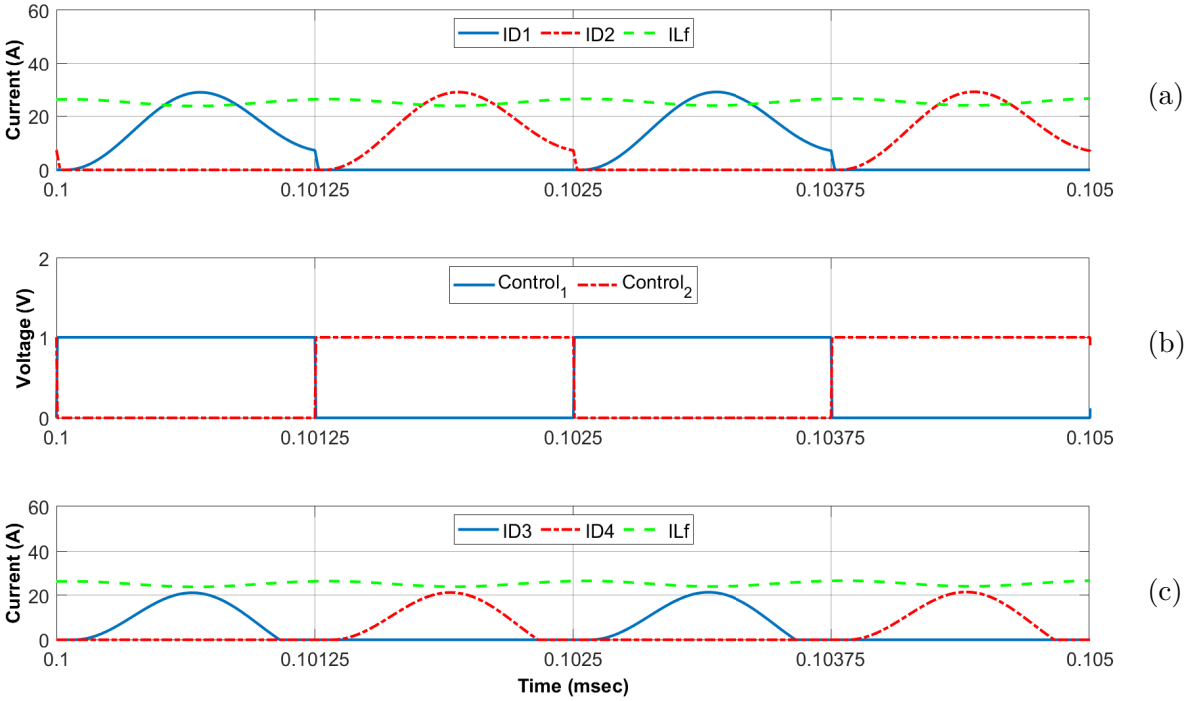


Figure 4-10: Zoom of Fig. 4-9 between 0.1 msec and 0.105 msec.

4.3.2 Reduction of the switching frequency.

Another technique that can be used is reducing the switching frequency of the converters. This means that the rest of the values that depend on fs also change. The disadvantage of reducing fs is that the equalization time increases, thus, a compromise should be reached. Fig. 4-11 shows how the peak currents continue to decrease.

In the case that the output is a single load, the output power is defined by the output voltage and the load, which means that if the switching frequency is reduced, the peak current has to increase, as the average value has to maintain. In the case of an equalizer, the

output voltage is fixed, but the output power is not defined the same way, which explains that the peak current decreases if the switching frequency is decreased.

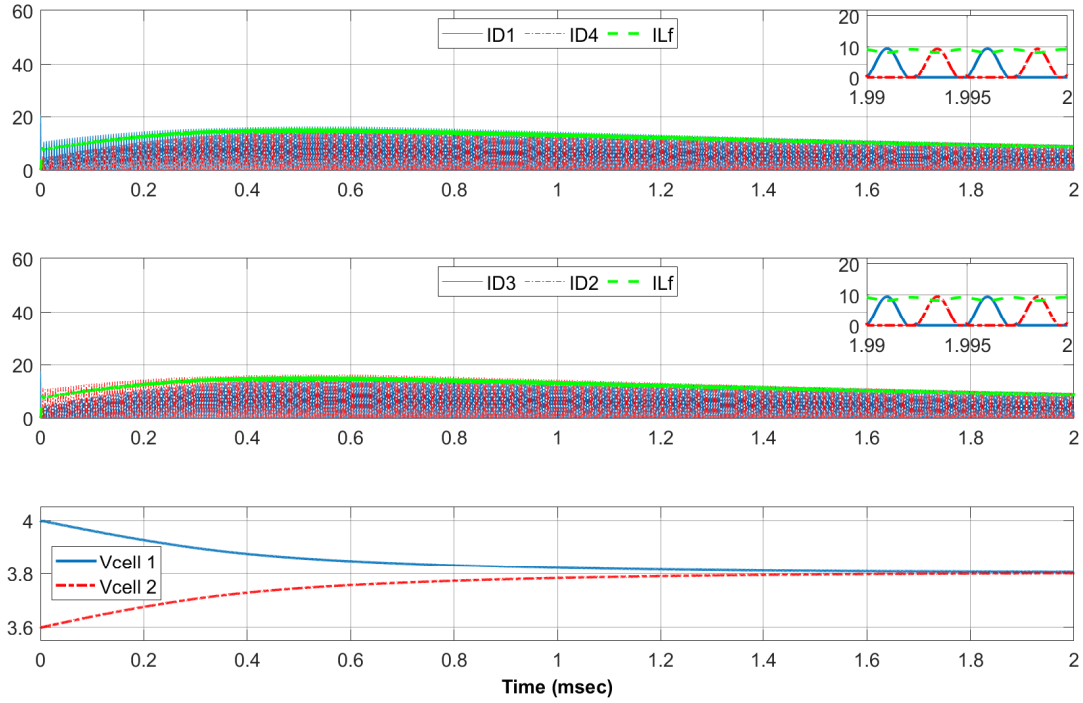


Figure 4-11: Main waveforms for the simulation of the equalizer changing fs from 400kHz to 200kHz and f_{LC} from 800kHz to 400kHz.

4.3.3 Increasing of Lf

Doubling the value of Lf also reduces the peak current of the resonant converter, as it can be seen in Fig. 4-12. However, this also increases the equalization time. A compromise should be reached once more.

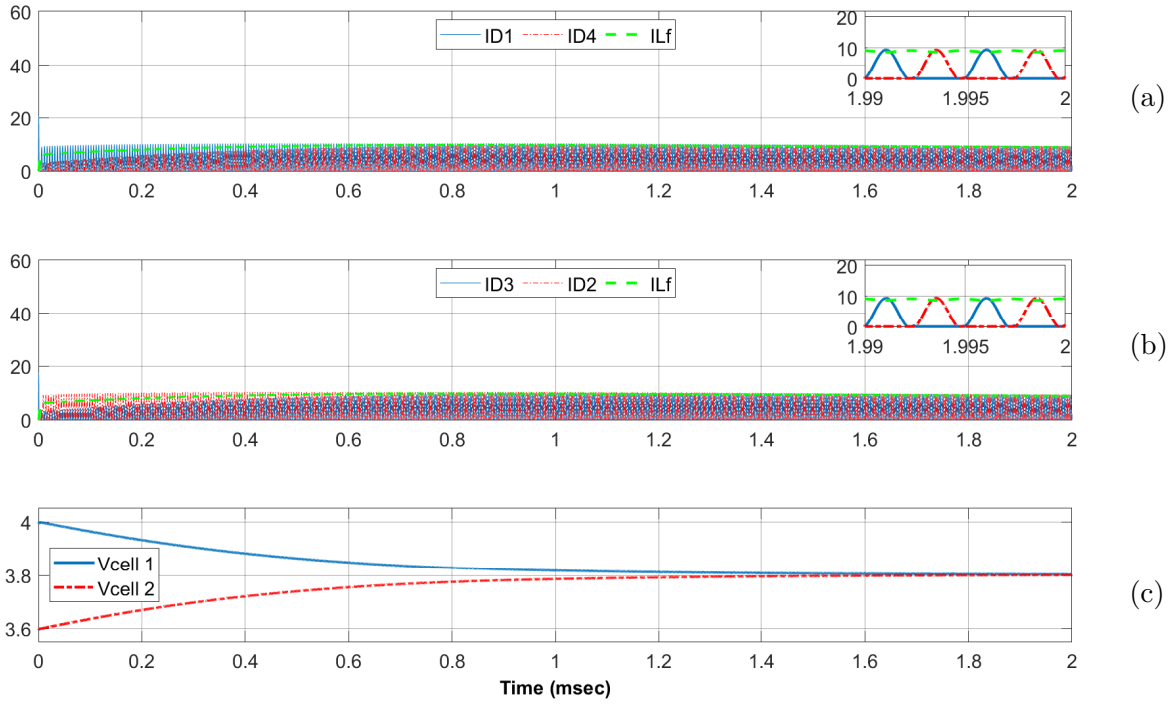


Figure 4-12: Main waveforms for the simulation of the equalizer doubling the value of Lf.

4.3.4 Reduction of Co and increasing of Lk

The last technique to reduce the peak current is to reduce Co. This means that using the relationship among Lk, fs and Co, Lk will increase. This technique also reduces the peak currents, but the equalization time is increased. Again, a compromise has to be reached. The effects of reducing Co and recalculating the value of Lk can be seen in Fig. 4-13.

If a zoom is taken from 8 msec to 8.01msec, it is appreciated how the currents reach zero and start the resonance again, an effect that was previously seen. This zoom can be seen in Fig. 4-14. Again, the currents reach zero at different times due to the voltage difference of the input cells. The output voltage in this case is always positive as the ripple has been reduced.

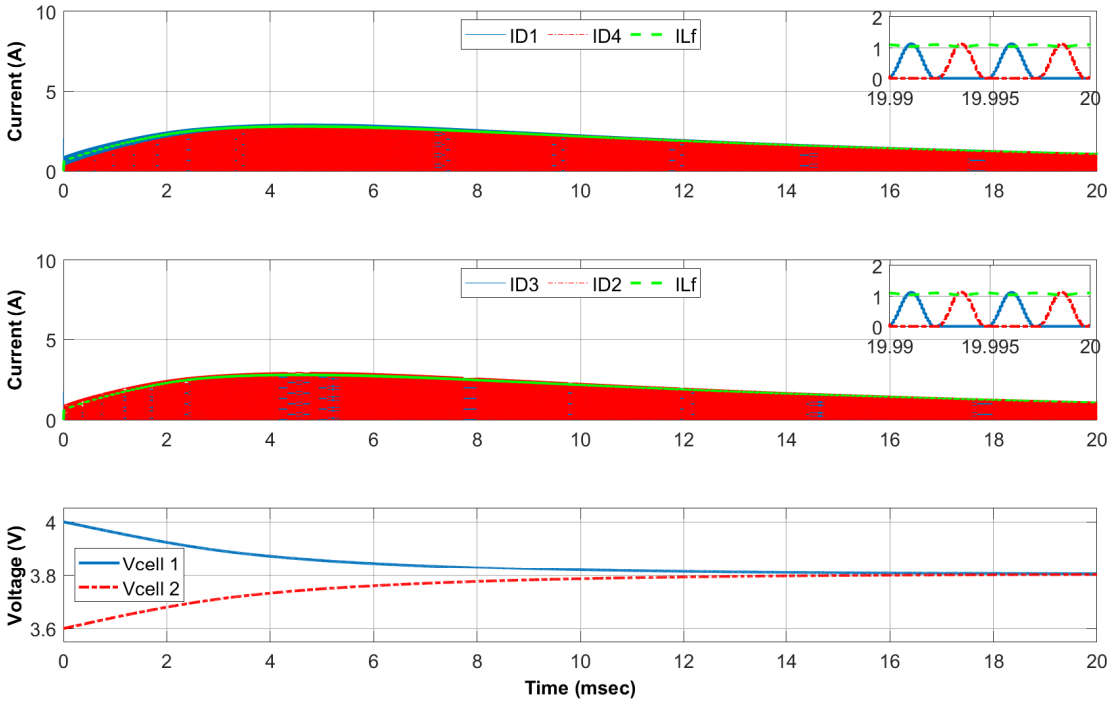


Figure 4-13: Main waveforms for the simulation of the equalizer with Co1 and Co2 equal to 100nF and recalculating Lk.

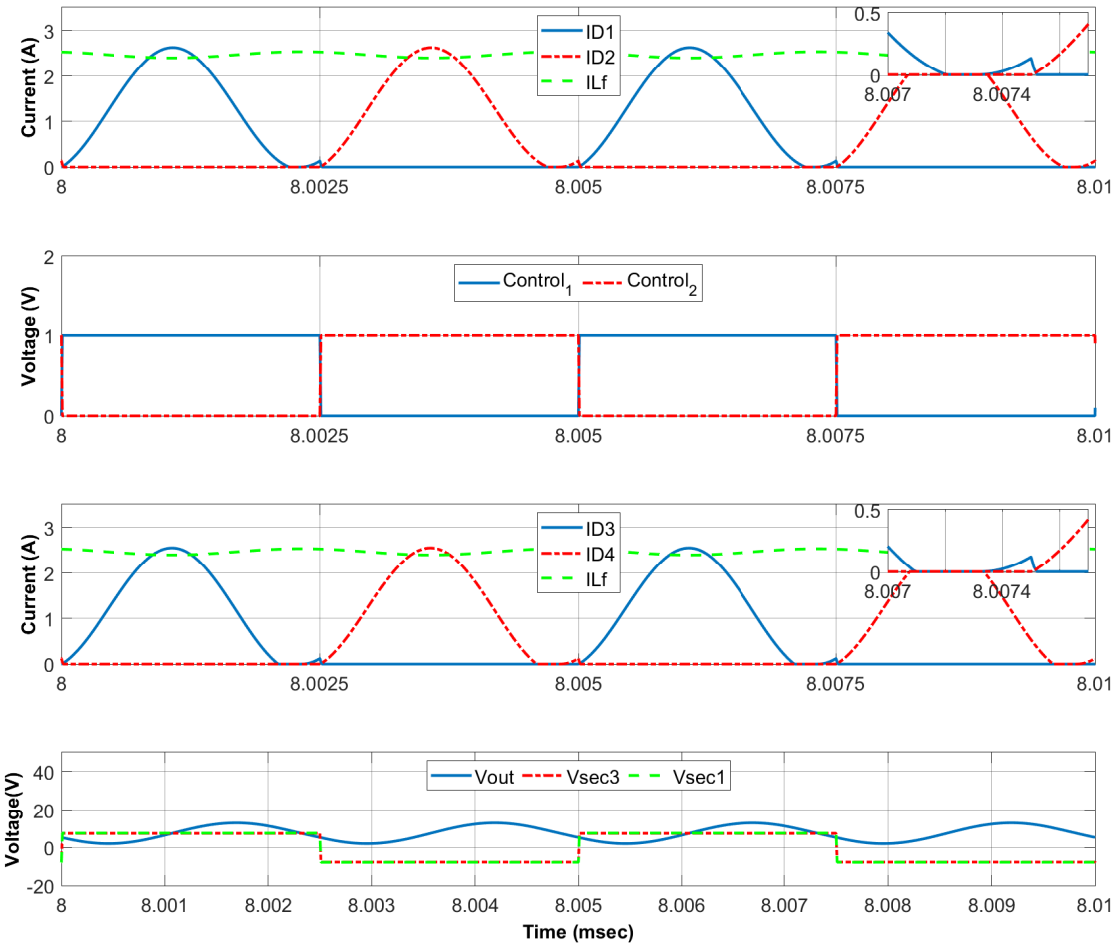


Figure 4-14: Zoom of Fig. 4-13 between 8 msec and 8.01 msec.

5. Proposed gate control topology

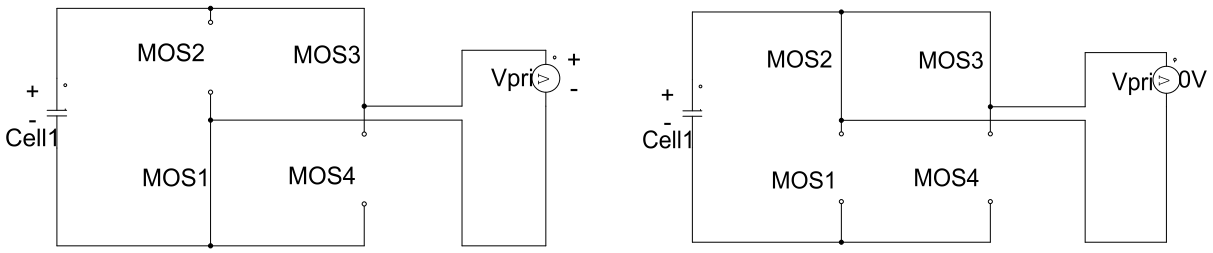
In this chapter, the proposed gate control topology will be explained. A simulation with this gate control topology will be performed to compare the obtained waveforms with the ones of the previous chapter. At the end of the chapter, some solutions to improve the system will be presented.

Up to this point, the topology of the equalizer that will be used has been described. A basic control and the waveforms provided have been also covered, showing the problem of not reaching ZCS in some cases. One of the problems that happened was that the currents started to resonate again in the same semiperiod. As it was shown, this second resonance was produced because the output voltage became higher than the secondary of the transformer, charging the leakage inductance again and directly polarizing the diode. This second resonance implies that there is current circulating when the gate signals change, producing high switching losses in the converter.

The aim of the proposed gate control topology is to fix that problem, so that when the switches of the input bridge change positions it is with zero current flow. This implies less switching losses, increasing the efficiency of the equalizer. The main intention of the proposed topology is to control one of the legs of the input bridge, making its switches change when the currents through the leakage inductances reach zero, shortcircuiting the transformer. The other leg of the input bridge will remain working as in the basic control scheme. This way, for a second resonance in the same semiperiod, the output voltage has to be negative sign. The leg composed by switches 3 an 4 will be the one that will remain working as in the basic control (PWM modulation), and the switches 1 and 2 will be controlled with the

proposed control topology.

With the proposed topology, there will be two different equivalent circuits for each semiperiod of the PWM signal, for a total of 4 equivalent circuits per period. The first two equivalent circuits can be seen in Fig. 5-1. Fig. 5-1a shows the equivalent circuit of the input bridge at the beginning of the first semiperiod. In this circuit, switches 1 and 3 are closed while switches 2 and 4 are open, as in the case of the basic control. This implies a positive voltage on the primary on the transformer, and therefore also in the secondary $Vsec_1$. While $Vsec_1$ is higher than the output voltage, the current through the corresponding leakage inductance will begin to increase. In addition, diode D1 becomes directly polarized. When the output voltage becomes higher than $Vsec_1$, the inductor current decreases until it reaches zero. In that moment, the diode becomes inversely polarized, and switches 1 and 2, from the first leg, will change their position. The equivalent circuit is then the one shown in Fig. 5-1b. Now the transformer is short-circuited and the secondary of the transformer will be 0V, which means that for a second resonance, the output voltage has to be negative.



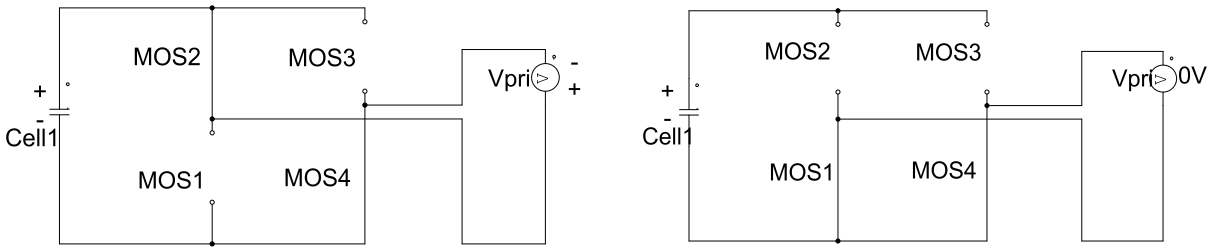
(a) Switches 1 and 3 are closed and switches 2 and 4 are open.

(b) Switches 2 and 3 are closed and switches 1 and 4 are open when ID1 decreases to zero Amps.

Figure 5-1: Equivalent circuits of the input bridge in the first semiperiod.

At the beginning of the second semiperiod, the second leg changes positions due to the PWM signal. Switches 2 and 4 are now closed while switches 1 and 3 are open. The equivalent circuit now is the one shown in Fig. 5-2a. In this case, the output voltage is higher than $Vsec_1$, thus ID1 remains zero, but the secondary $Vsec_2$ is now higher than Vout,

thus, ID2 begins to increase. Once ID2 starts to decrease and reaches zero for the same reasons as ID1 in the first semiperiod, switches 1 and 2 change their positions again, making a short-circuit in the transformer. The equivalent circuit is the one shown in Fig. 5-2b.



(a) Switches 2 and 4 are closed and switches 1 and 3 are open

(b) Switches 1 and 4 are closed and switches 2 and 3 are open when ID2 decreases to zero Amps.

Figure 5-2: Equivalent circuits of the input bridge in the second semiperiod.

The proposed gate control topology for solving this problem can be seen in Fig. 5-3 for ET1.

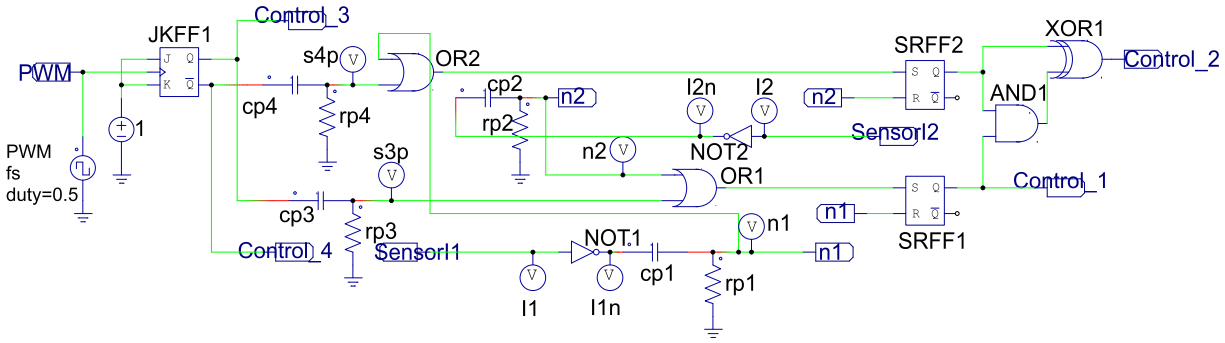


Figure 5-3: Proposed gate control topology.

As it can be seen, one current sensor is needed for measuring each current through the inductances Lk. The sensors placement can be seen in Fig. 5-4. The sensors will be composed by comparators to change from an analog signal to a digital signal. The values used for performing the simulation can be seen in Table 5.1.

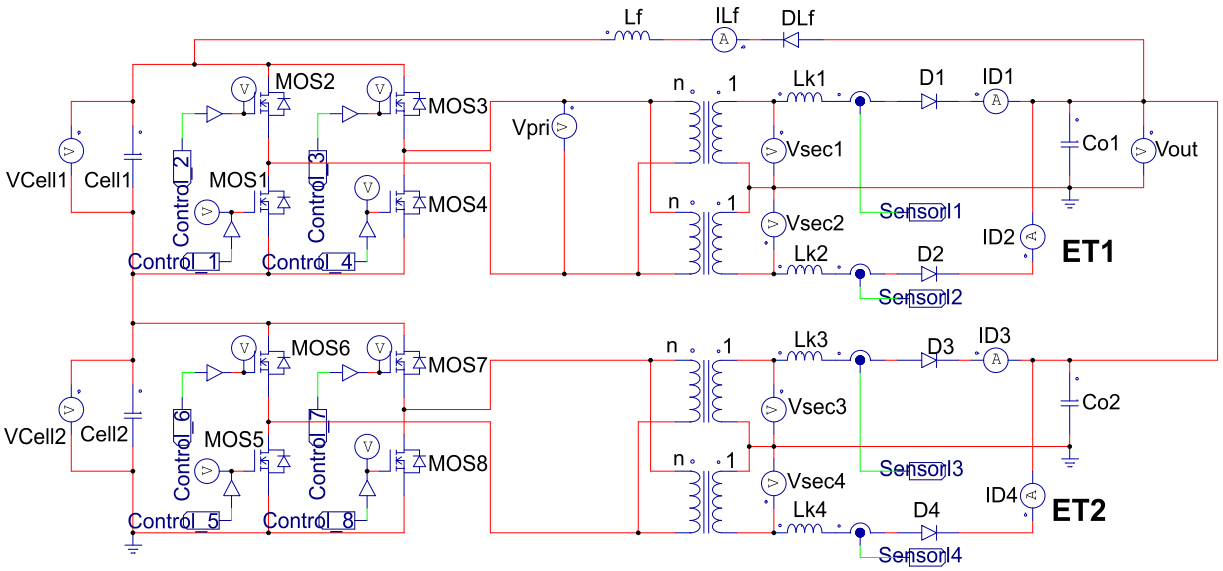


Figure 5-4: Schematic of the connection of two ET with current sensors.

Table 5.1: Parameters used for the simulation of the proposed gate control topology

Cells capacitance	10e-3 F
VinitialCell1	4 V
VinitialCell2	3.6 V
n	0.5
$\mathbf{f_{LC}}$	400e3 Hz
fs	f_{LC} Hz
ω_{LC}	$2\pi f_{LC}$ rad/s
ω**s**	2πfs rad/s
Co1, Co2	100e-9 F
Lk1, Lk2, Lk3, Lk4	1.5847e-06 H
Lf	20Lk1 H
cp1, cp2, cp3, cp4	47e-9 F
rp1, rp2	1 Ω
rp3, rp4	3.9rp1 Ω

In the proposed topology, the PWM signal will be the input to a JK flip-flop, which will divide the frequency by two and provide signals Control_3 and Control_4. That is why in this case fs has to be equal to f_{LC}. Two set-reset flip-flops will be the elements to control the gate signals for switches 1 and 2, each flip-flop for each gate signal. A set in the flip-flop will put the corresponding control signal to one, and a reset to zero. A driver will be used

for providing the final gate signals.

Two high pass filters will be used for setting the flip-flop connected to Control_1. When ID2 starts to increase, switches 2 and 4 are closed and switches 1 and 3 are opened, as it was shown in Fig. 5-2a. The high pass filter composed by resistor rp2 and capacitor cp2 provides a small pulse when current ID2 reaches zero after the resonance. This small pulse sets the flip-flop, making MOS1 to conduct. At the same time, this pulse resets the flip-flop that triggers switch 2, so that switches 1 and 2 change at the same time. There is also a protection circuit composed by gates AND1 and XOR1 that prevents switches 1 and 2 to conduct at the same time.

Thus, when current ID2 returns to zero, the leg composed by switches 1 and 2 will change, shortcircuiting the transformer, as it was shown in Fig. 5-2b. Then the second resonance will not be produced, and all four switches achieve almost ZCS (the magnetizing current continues to be neccesary).

The reason for providing a small pulse is that the flip-flop cannot have both inputs at high level, thus, after the small pulse both inputs will be zero, keeping the previous output, until the flip flop is activated again with a small pulse.

Another small pulse is triggered when switches 3 and 4 change position due to the PWM. This second pulse is also provided by a high pass filter and can also set the flip-flop to activate switch 1 and reset the other flip-flop to open switch 2. Thus, in the case that the resonant current ID2 returns to zero switches 1 and 2 will change. When switches 3 and 4 change, switches 1 and 2 will also change if they were not changed before by the other small pulse.

The proposed topology has also other two high pass filters for implementing the same process but for current ID1. Fig. 5-5 shows some waveforms of the proposed topology, where it can be seen how when current I2 returns to zero, signal control_1 changes from 0 to 1, due to the small pulse n2, which activates the flip-flop. Due to the previous explanation when

signal control$_1$ is set to 1, signal control$_2$ is 0 and viceversa. The truth table of the protection circuit composed by gates AND1 and XOR1 can be seen in table 5.2.

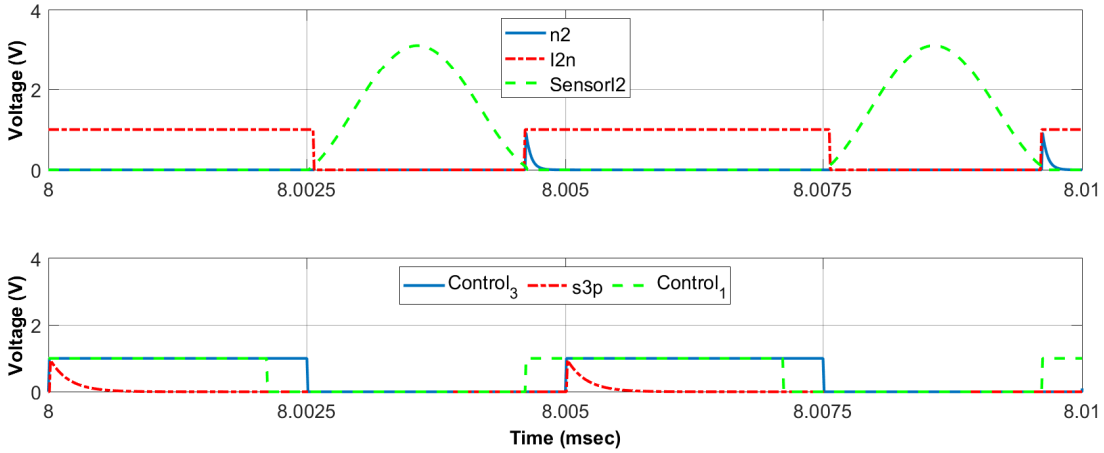


Figure 5-5: Main waveforms of the proposed control stage.

Table 5.2: Truth table for the protection of switches 1 and 2.

SRFF1 Q	SRFF2Q	Control_1	Control_2
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	0

As it was commented before, the proposed topology has to be repeated the same number of times that there are ETs, changing the sensors and the control signals. The advantage is that the clock input signal keeps the same for all of them.

5.1 Simulation with the proposed Topology

The main waveforms of the simulation performed with the proposed topology are represented in Fig. 5-6. A zoom has been represented in Fig. 5-7 in the interval between 8 msec and 8.01 msec to compare it with Fig. 4-14. It happens now that once the current reaches zero, it does not start to resonate again until a new switching cycle starts. This

was fixed by shortcircuiting the transformer once the currents returned to zero. Therefore, for a resonance in the same semiperiod, the output voltage has to be negative sign.

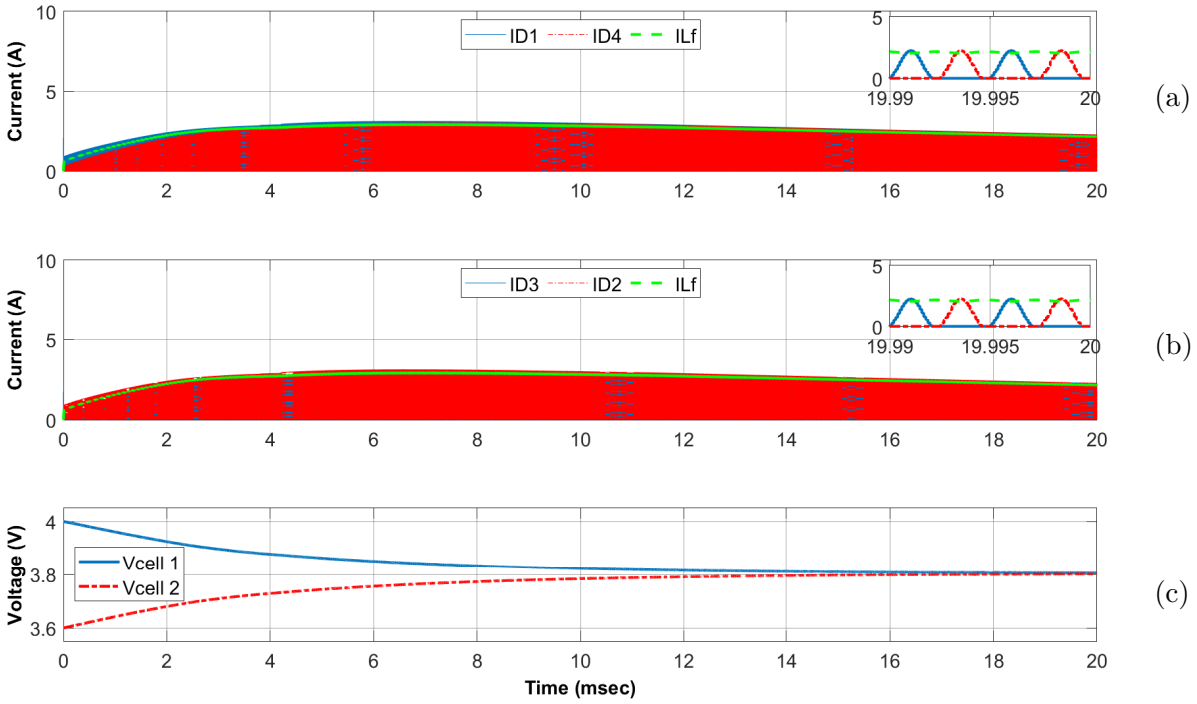


Figure 5-6: Main waveforms for the simulation of the equalizer with the proposed gate control topogoly.

Fig. 5-8 shows the interval between 4 msec and 4.01 msec. The current through Lk_1 starts to increase again before it reaches zero. This is produced because the voltage on the secondary becomes higher than the output voltage again. This is an effect that was previously seen and depends on the charging of Lf and on all the leakage inductances of the system. Therefore, when switches 3 and 4 change due to the PWM there is current circulating through Lk1. In this moment signal control1 is one and switch 2 should change because of the small pulse (signal s4p) produced by signal Control3. However, the protection circuit does not let both switches 1 and 2 to conduct at the same time, thus, until a reset is produced in the flip-flop connected to Control1, Control2 is not set. This reset is produced when Lk1 totally discharges, and in that moment switches 1 and 2 change position. The advantage is that ZCS is achieved for switches 1 and 2.

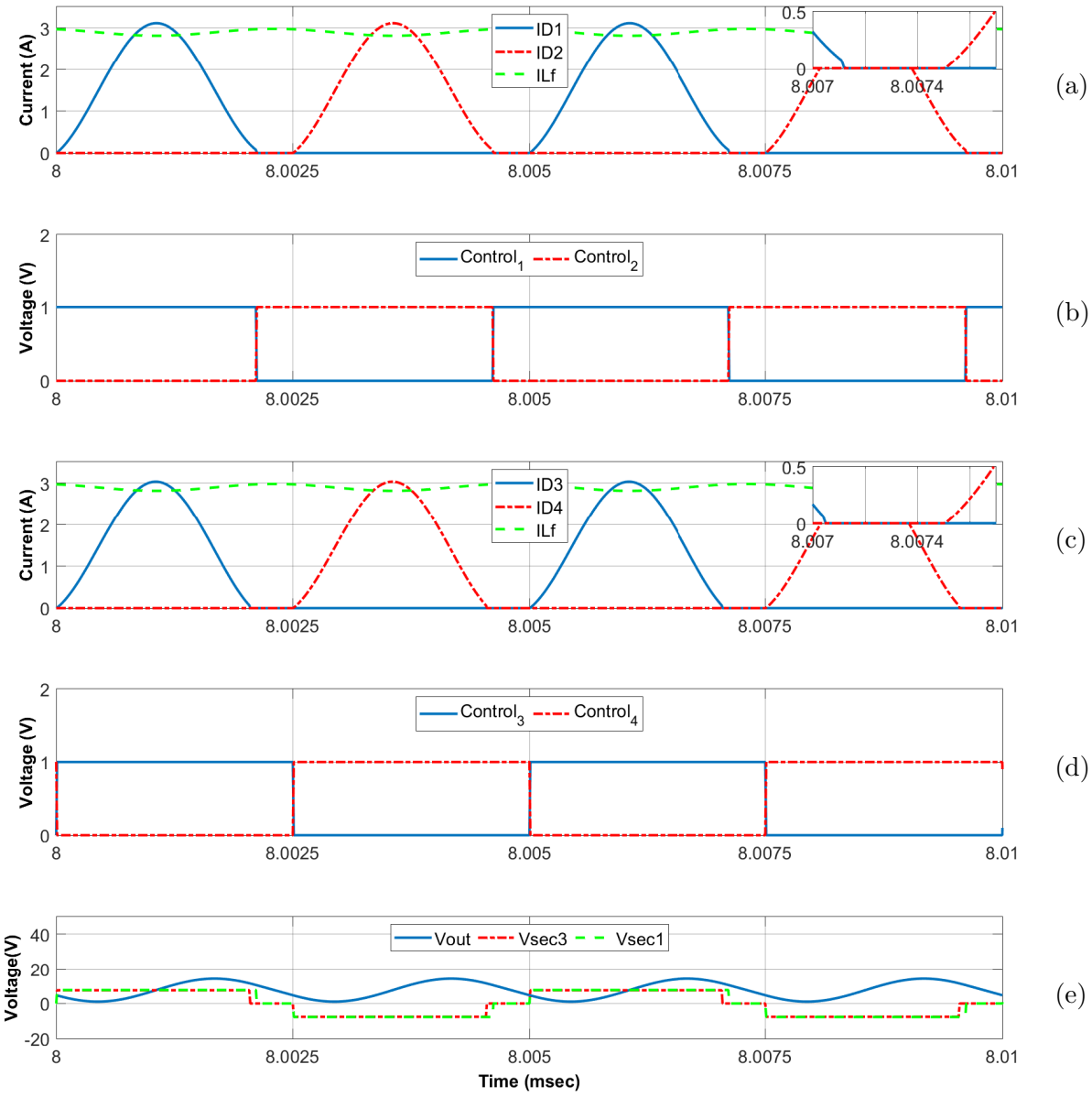


Figure 5-7: Zoom of Fig. 5-6 between 8 msec and 8.01 msec.

Fig. 5-9 shows the interval between 1 msec and 1.01 msec. The current is decreasing when the clock signal changes, producing high switching losses, an effect that was also previously seen. This also depends on the charging of Lf and the rest of values of Lk. As it was commented in Fig. 5-8, due to the protection circuit that prevents switches 1 and 2 to conduct at the same time, signals Control1 and Control2 do not change until ID1 is zero,

providing ZCS for switches 1 and 2. However, they change instantaneously when current ID2 is resonating, because in the protection circuit, signal Control1 has priority.

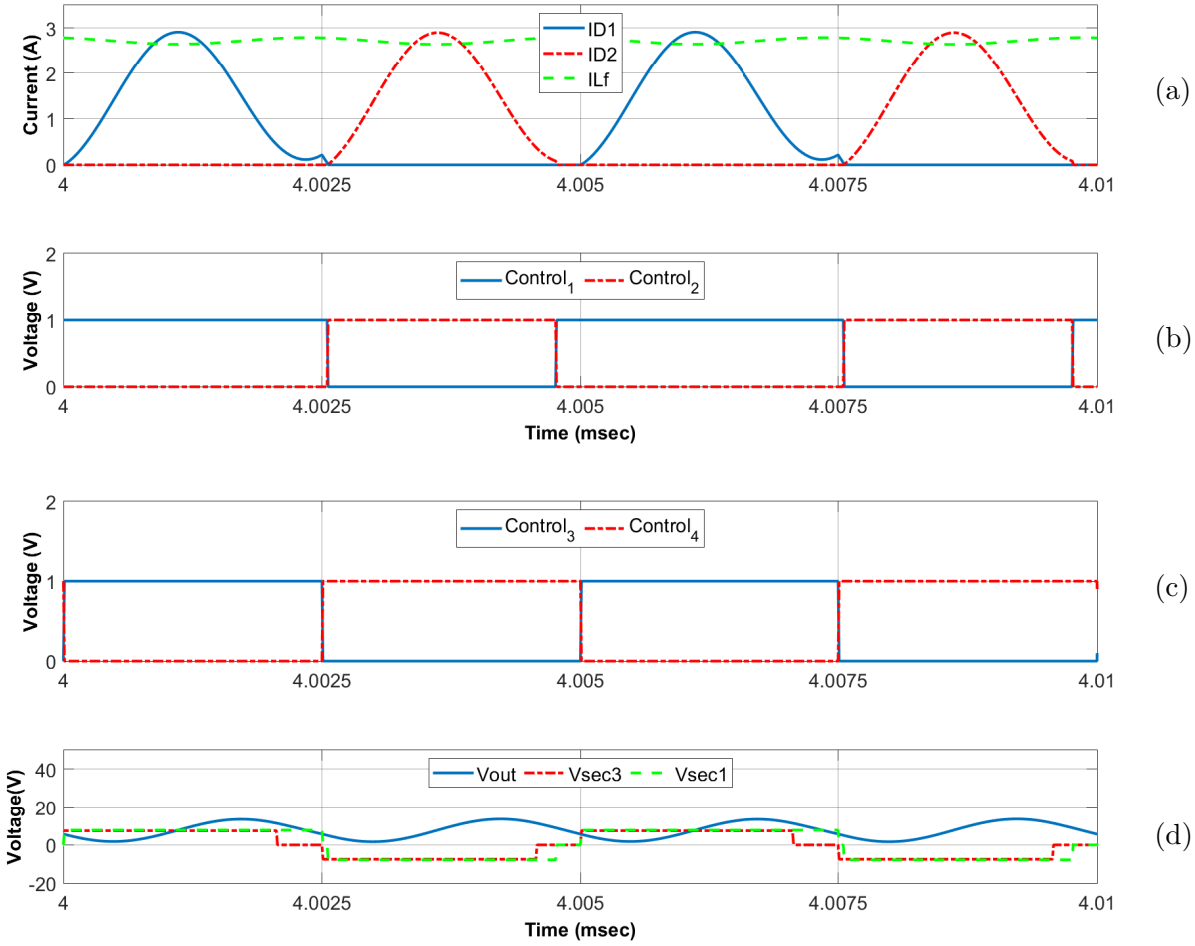


Figure 5-8: Zoom of Fig. 5-6 between 4 msec and 4.01 msec.

To avoid the problems that happen in Figs. 5-8a and 5-9a one thing that can be done is to vary the value of the switching frequency fs (f_{LC} keeps the same), as it directly affects to the current shape. The value of fs will now change from 400kHz to 360kHz (f_{LC} = 400kHz) and the results are plotted in Fig. 5-10.

The equalization obtained in Fig. 5-10 is slower compared to Fig.5-6c. But if a zoom is made, in Figs. 5-11 and 5-12 it can be seen that the waveforms now produce ZCS where before there were problems. On the other hand, not only the equalization speed but also the

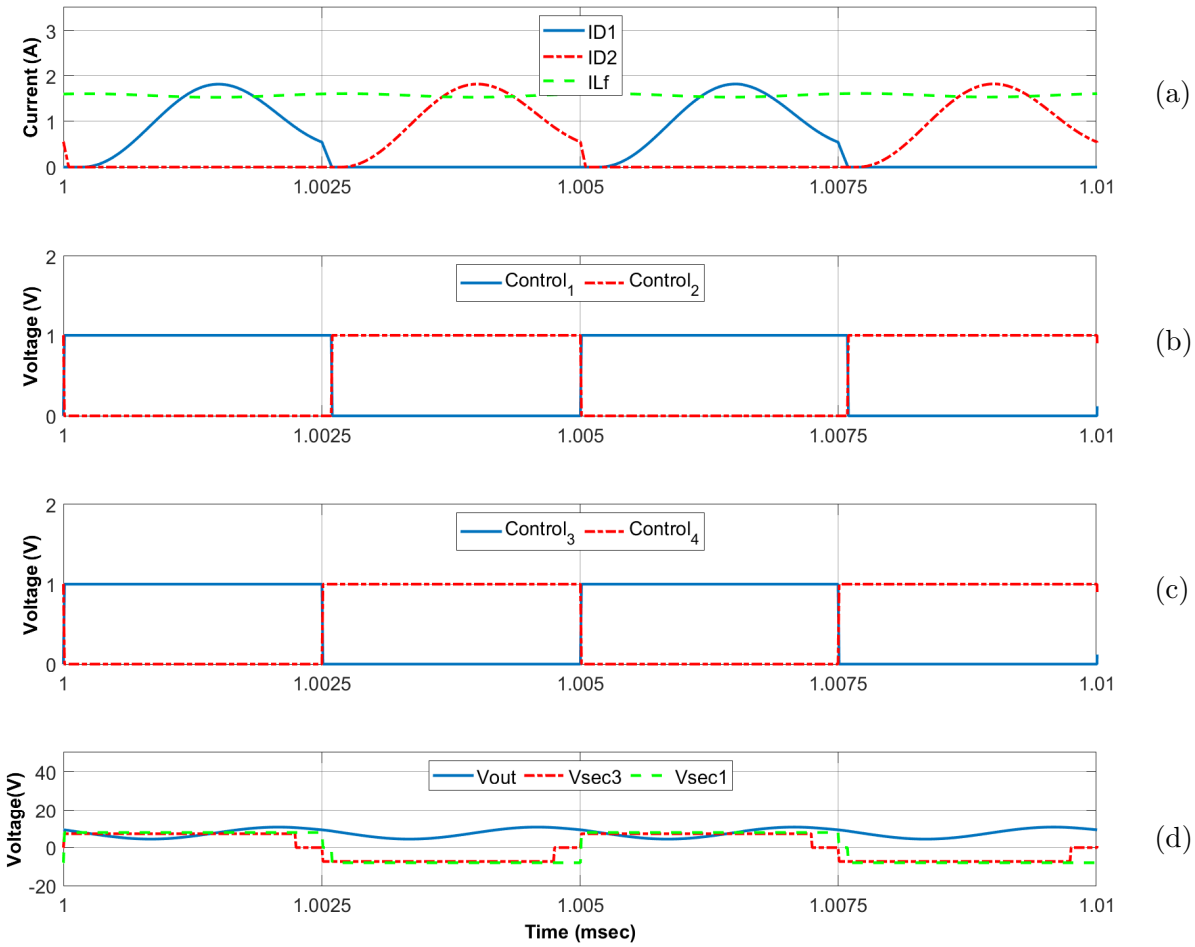


Figure 5-9: Zoom of Fig. 5-6 between 1 msec and 1.01 msec.

peak current value has been increased. If equalization speed is not key in the design, this could be a good solution for reducing switching losses.

The advantage of this method is that not only solves the problems with the current shape at the beginning, of the equalization but also fs can be varied during the process, reducing the current peak value and the equalization speed. The value of Lk can also be changed to control the current shape, but the disadvantage is that Lk cannot be varied during the equalization.

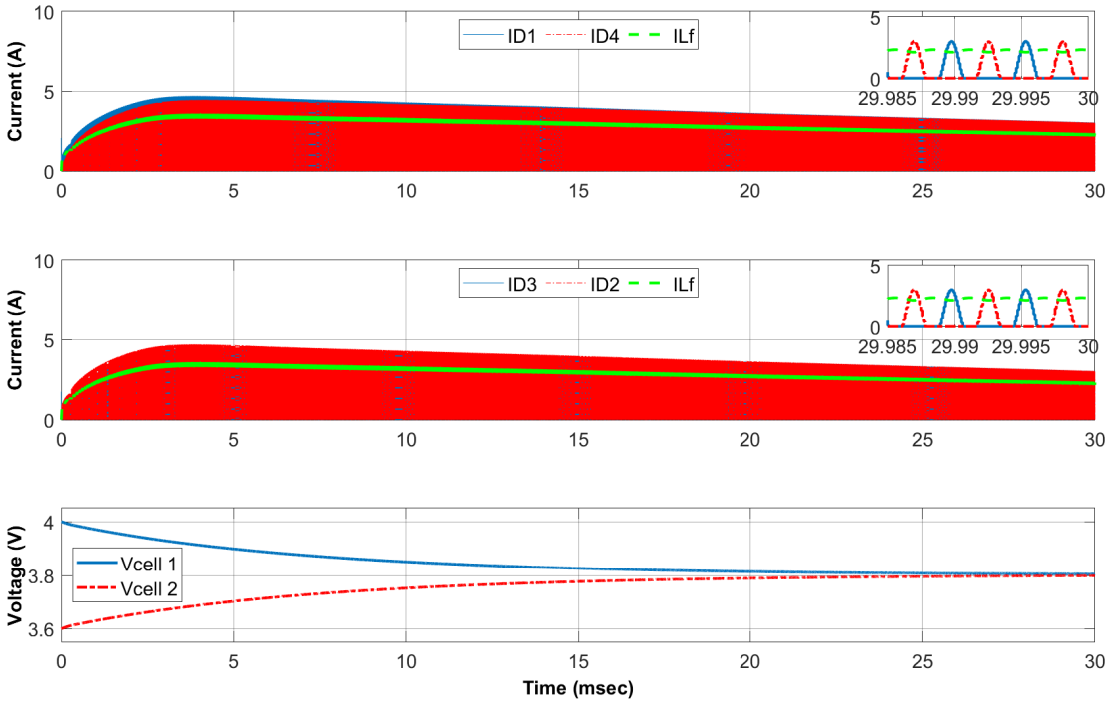


Figure 5-10: Main waveforms for the simulation of the equalizer changing fs from 400kHz to 360kHz.

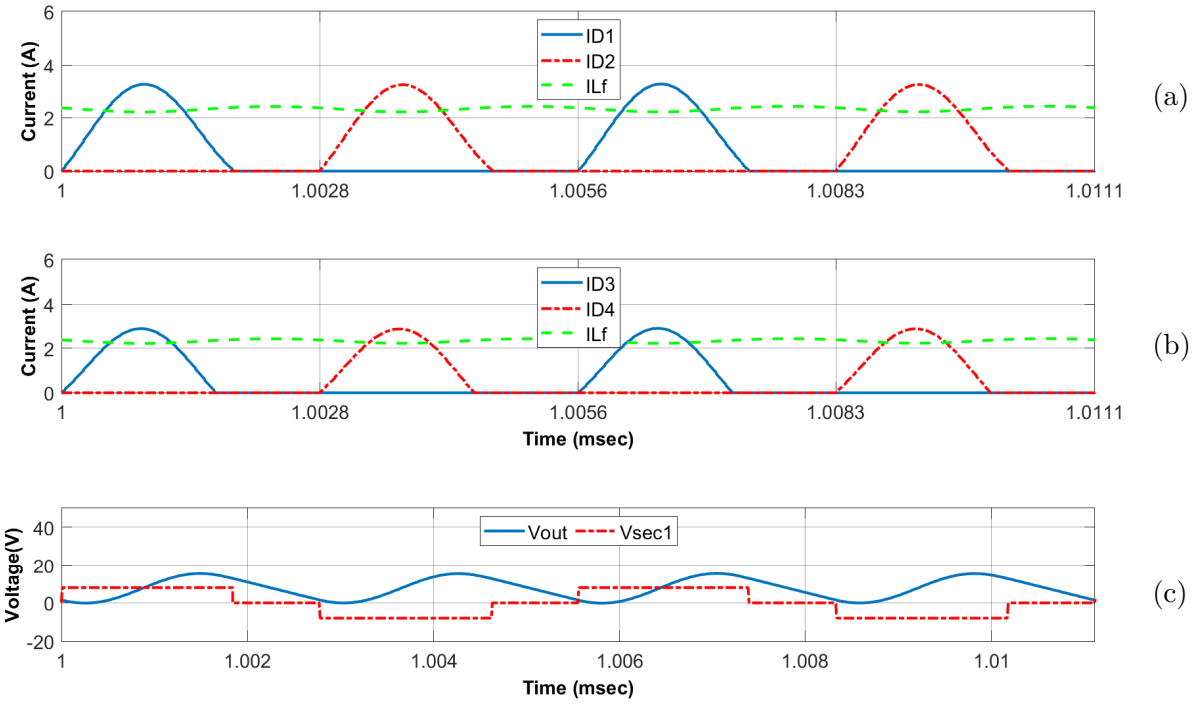


Figure 5-11: Main waveforms for the simulation from 1 msec to 1.0111 msec

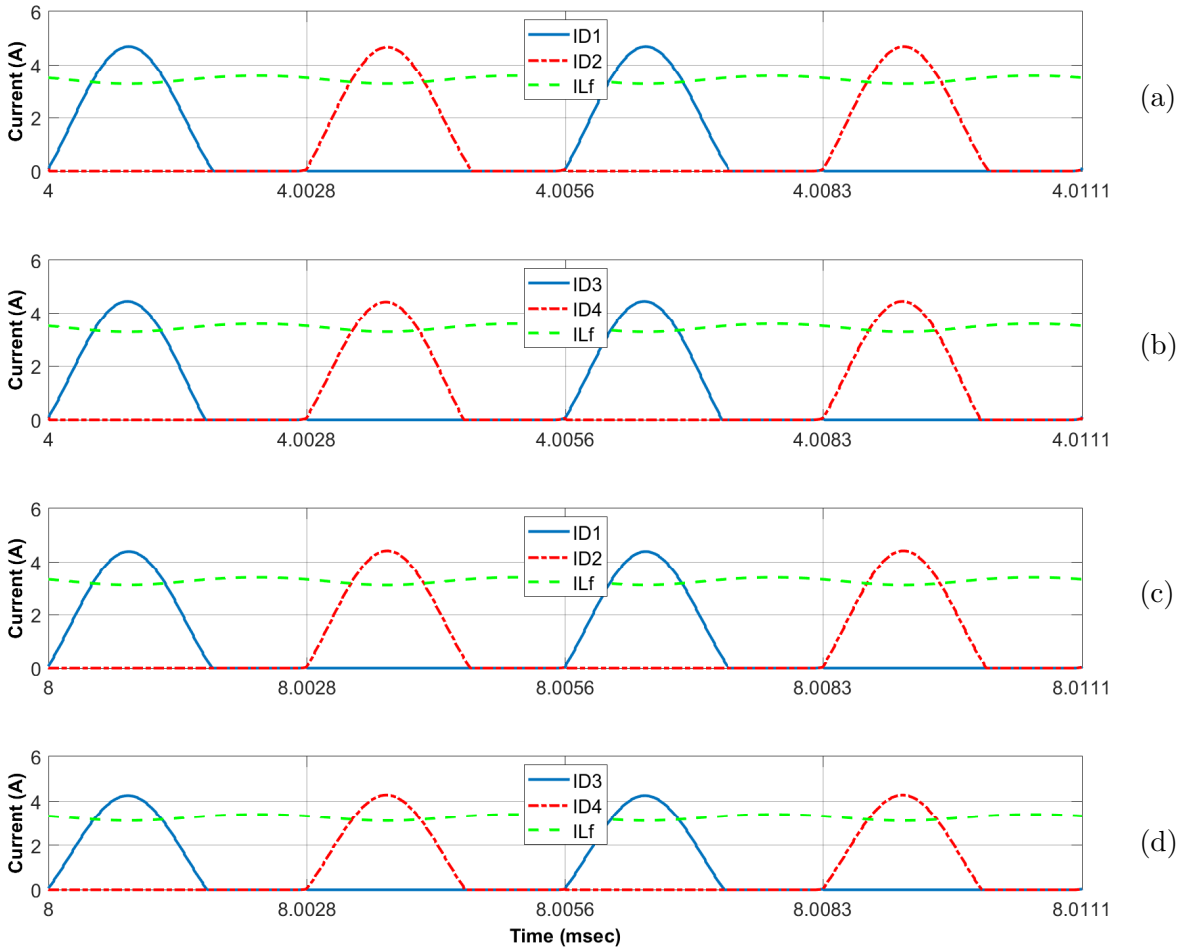


Figure 5-12: Main waveforms for the simulation in different intervals of time.

6. Adding the magnetizing inductance Lm to the system

In this chapter the magnetizing inductance Lm will be added to the system. The simulation and waveforms obtained with this new element will be shown. At the end of the chapter two solutions will be presented to solve problems.

Another element will be now introduced in the simulation, the magnetizing inductance Lm. The placement of Lm can be seen in Fig. 6-1. A new simulation will be performed with the parameters of table 5.1. However, in this case the voltage of Cell2 will change from 3.6V to 3.8V. The results can be seen in Fig. 6-2.

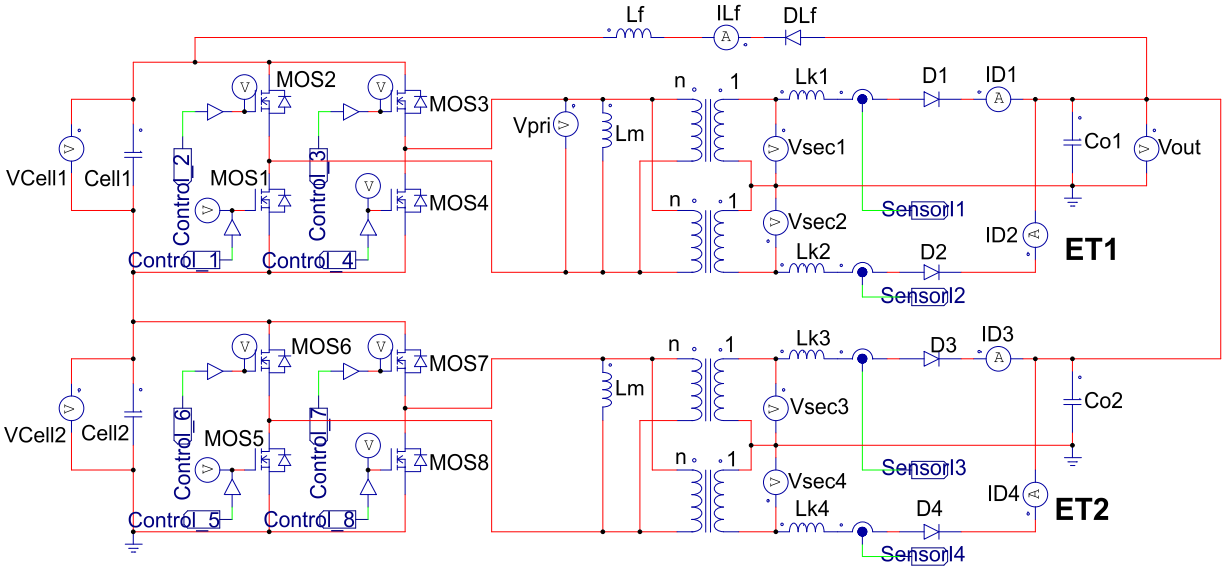


Figure 6-1: Placement of Lm.

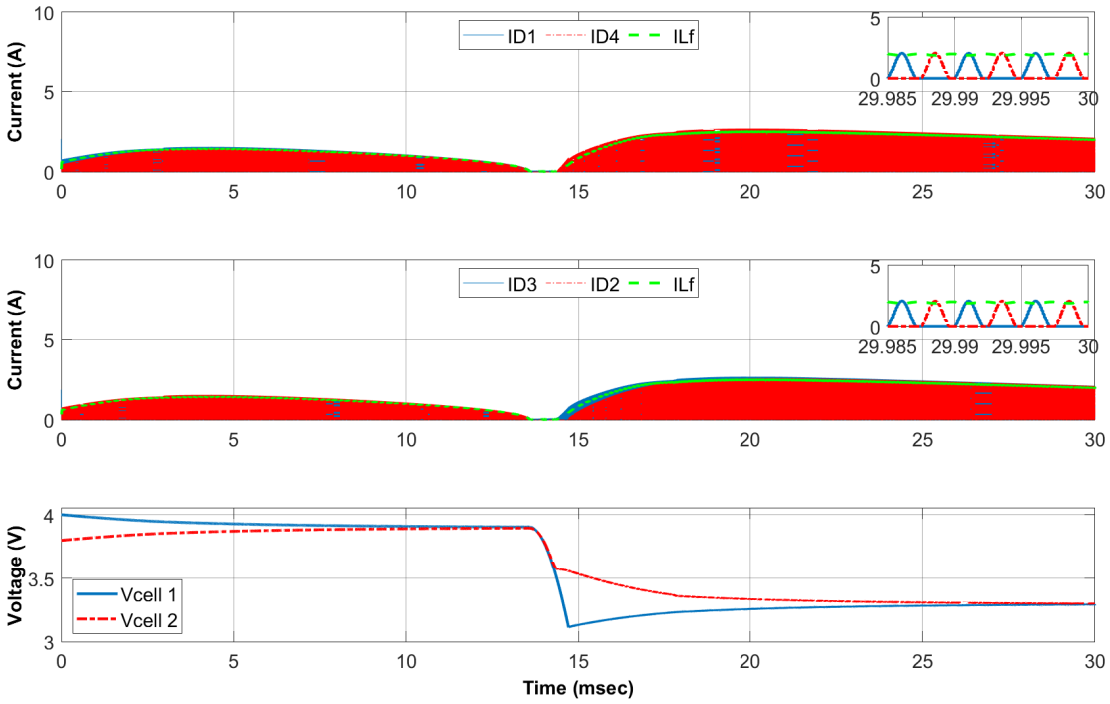


Figure 6-2: Main waveforms for the simulation with the introduction of Lm.

When the resonant currents are reduced to nearly zero, there is a moment in which the diodes of the proposed control topology stop detecting when there is current flowing through the leakage inductances Lk. This implies that no small pulses are produced when the current returns to zero, reset of the flip-flops is not activated, and control signals to switches 1 and 2 stop working. Therefore, the voltage balance over the transformer is not zero, thus, the inductance Lm begins to charge quickly, making a sudden discharge of the input cells.

Two solutions can be applied to overcome this problem: Placing series capacitors after the input bridges, or modifying the proposed topology, so that the signal that sets one flip-flop is the reset for the other flip-flop. These solutions are explained in the next sections.

6.1 Adding series capacitors

Adding series capacitors in the topology can solve the previous problem with the control signals. The placement of the series capacitors Cser1 and Cser2 in the schematic can be seen in Fig. 6-3. The value of the series capacitors can be seen in Table. 6.1.

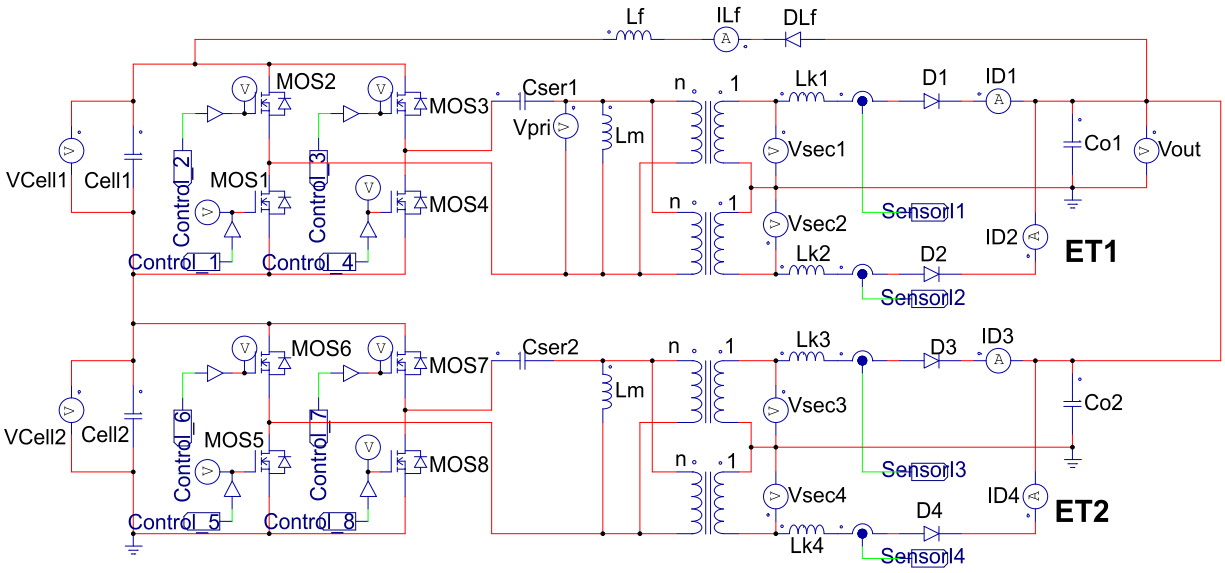


Figure 6-3: Placement of series capacitors Cser1 and Cser2.

Table 6.1: Series capacitors values

Cser1, Cser2	4.7e-6 F

The equalization now is performed correctly, as it can be seen in Fig. 6-4. This is produced because the output voltage achieves a considerable ripple, which prevents the resonant currents to have a low value. However, the peak value of the resonant currents has been increased. The equalizers should be powered off when the cells are equalized.

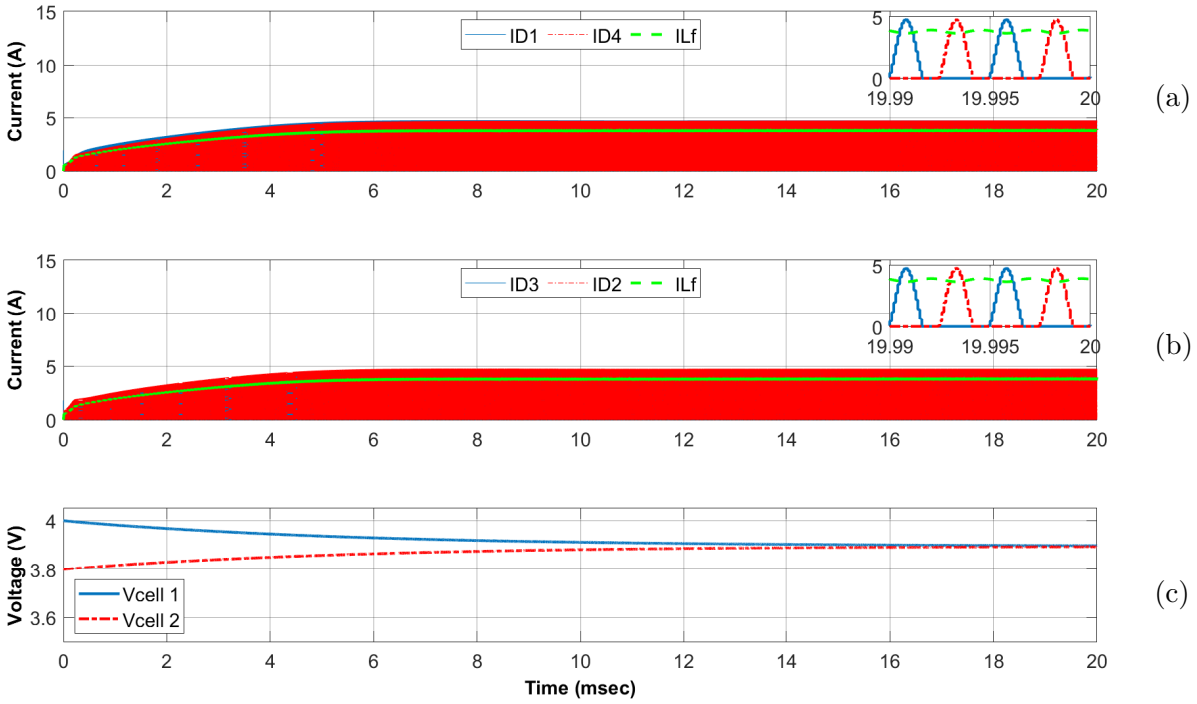


Figure 6-4: Main waveforms for the simulation adding Lm and series capacitors.

6.2 Modification of the proposed topology

A modification in the proposed topology can also solve the problem with the control signals. This solution connects the set of one flip-flop to the reset of the other. This way, signals $control_1$ and $control_2$ do not stop working because they can change either if the current returns to zero, or because of signals $control_3$ and $control_4$. The modification can be seen in Fig. 6-5.

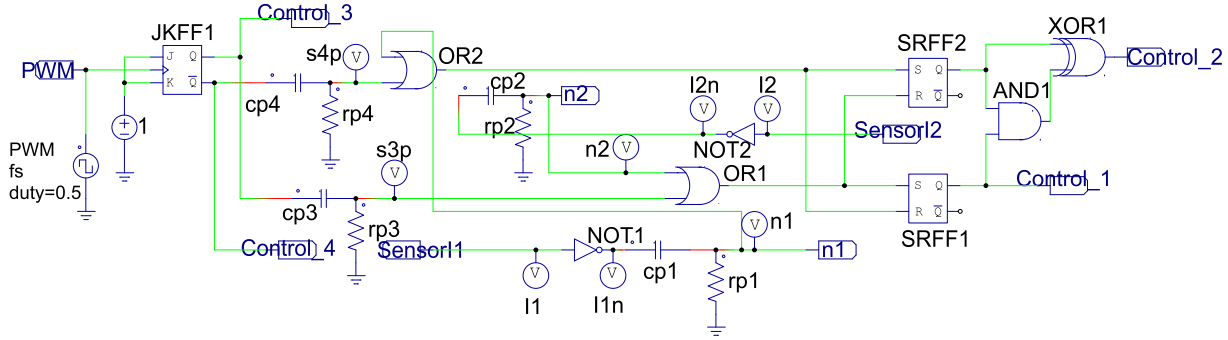


Figure 6-5: Modification of the proposed topology.

This modification will not change anything compared to the previous implementation if the system is well designed and the currents return to zero before the clock signal changes. The main waveforms of the system can be seen in Fig. 6-6. It can be seen that the peak value of the currents is lower compared to the placement of the series capacitors, which will produce lower conduction losses and higher efficiency of the equalizer.

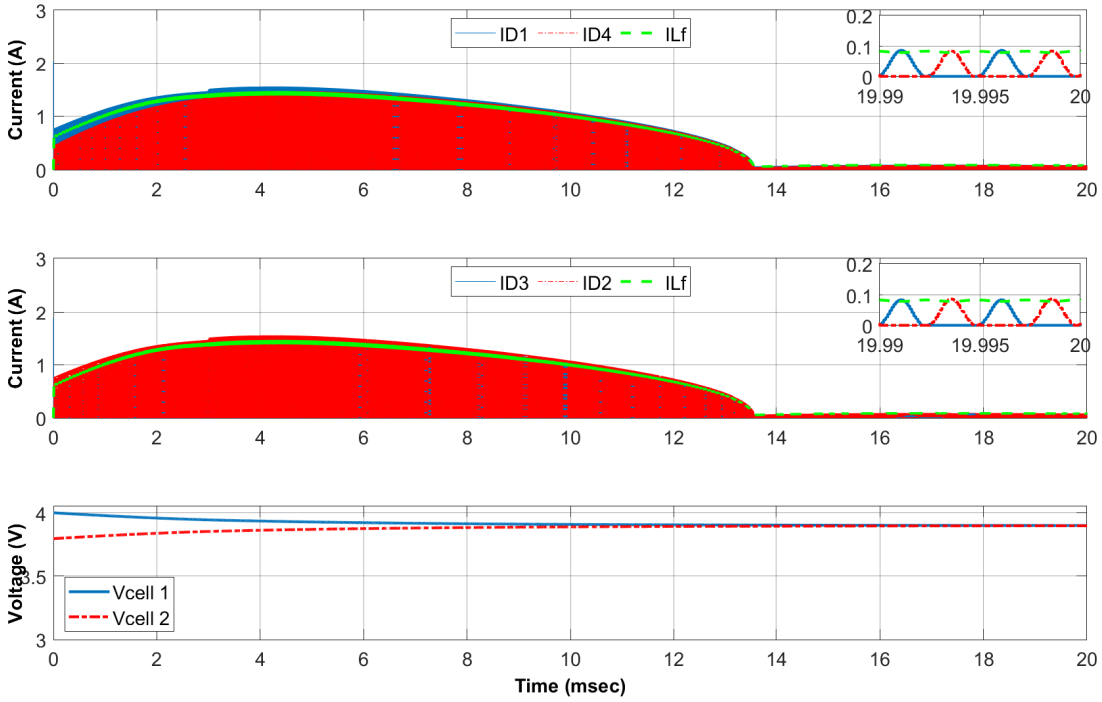


Figure 6-6: Main waveforms for the simulation with the modification of the proposed topology

7. Simulation with high capacitance of the input cells

In this chapter the input cells will be changed to have a high capacitance value and see the results. The capacitance of the input cells will change from 10e-3 F to 100F. The proposed topology with the modification seen in Fig. 6-5 will be used. The initial values of the input cells will be 4V and 3.8V. Inductance Lm will be also used. The results are the ones in Fig. 7-1.

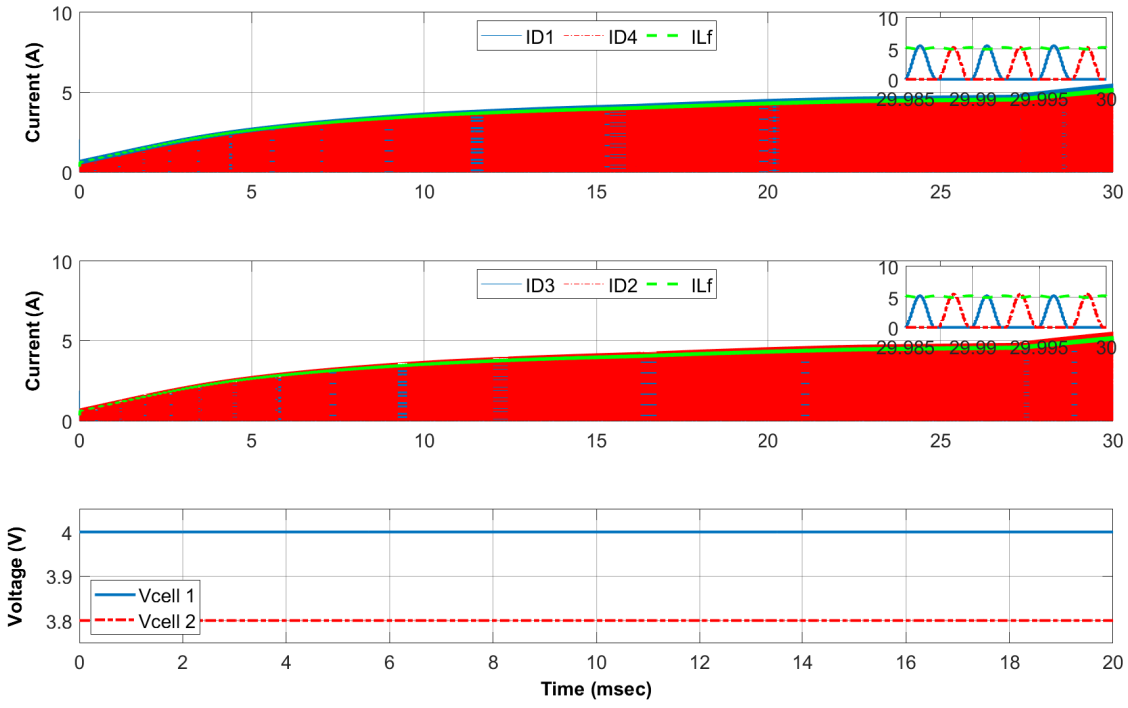


Figure 7-1: Main waveforms for the simulation for high capacitance input cell values.

It can be seen that with high capacitance of the input cells the waveforms present a

resonant shape. The equalization this time will take a lot of time because of the high capacitance of the input cells. That is why the voltage difference of the input cells seems to be constant. Until the output voltage is established ZCS may not be produced in some intervals because of different phenomenons that were previously seen (Figs. 5-8a and 5-9a). For solving this problems switching frequency variation may be also applied.

8. Effect of tolerances

In this chapter the effect of different tolerances in the leakage inductances Lk will be simulated. Two different cases will be shown to check the waveforms obtained. Finally, a differenciator circuit will be implemented to improve the behavior of the system.

8.1 Case 1

The tolerances on Lk will directly affect to the shape of the resonant currents and to the output voltage, according to equations 3.1 and 3.2. The parameters in Table 8.1 and the modified proposed topology of Fig. 6-5 will be considered now to perform a new simulation.

Table 8.1: Parameters for the tolerances in Lk (case 1).

Cells capacitance	10e-3 F
VoCell1	4 V
VoCell2	3.6 V
n	0.5
$\mathbf{f_{LC}}$	400e3 Hz
fs	f_{LC} Hz
ω_{LC}	$2\pi f_{LC}$ rad/s
ω**s**	2πfs rad/s
Co1, Co2	100e-9 F
Lk1, Lk2, Lk3, Lk4	1.5847e-06 H
$\mathbf{L_f}$	20Lk1 H
Lk2	1.1Lk1 H
Lk3	0.9Lk1 H
Lk4	1.1Lk1 H

The main waveforms obtained can be seen in Fig. 8-1. Now no ZCS is produced in ET1 because the tolerances affected to the resonant shape of ID1 and ID2, not letting the current to return to zero before the clock signal changes. This does not happen to ET2, since the resonant currents depend on the input voltage of each ET. No ZCS will imply higher switching losses for ET1. A zoom is represented of Fig. 8-2 to see these shapes. The equalization is also slower compared to the case in which no tolerances were used. The advantage here is that the peak current has been reduced. This will imply less conduction losses.

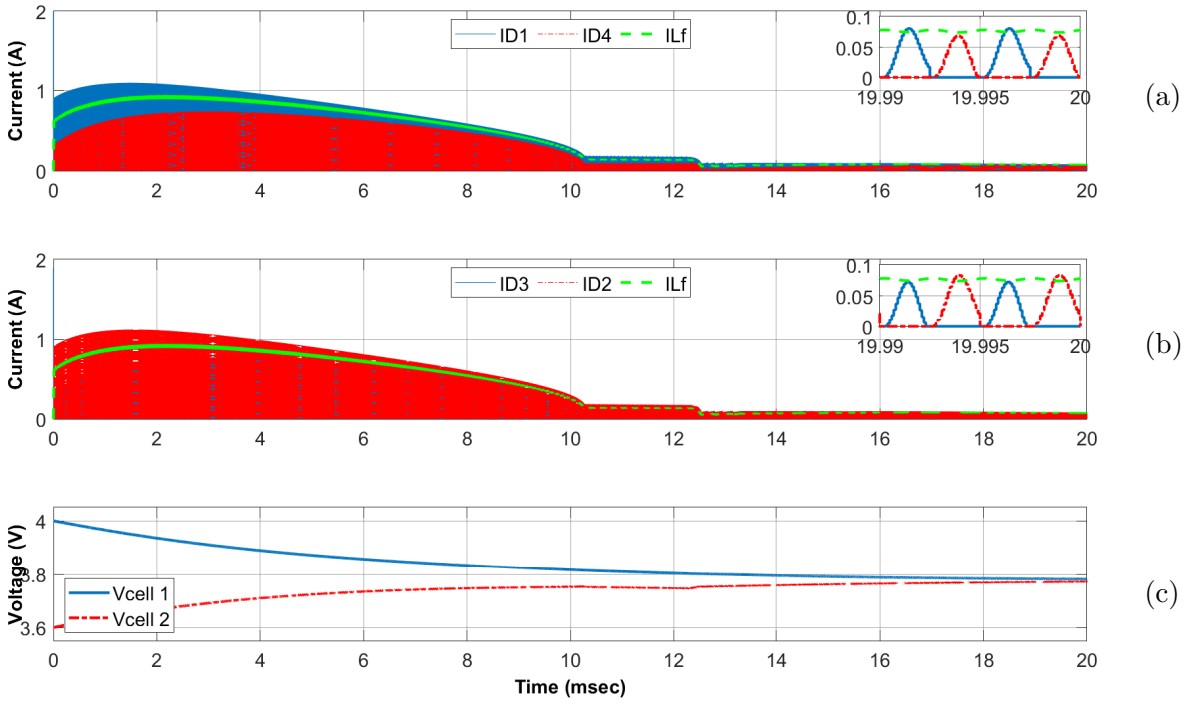


Figure 8-1: Main waveforms for the simulation of the equalizer with the tolerances of table 8.1.

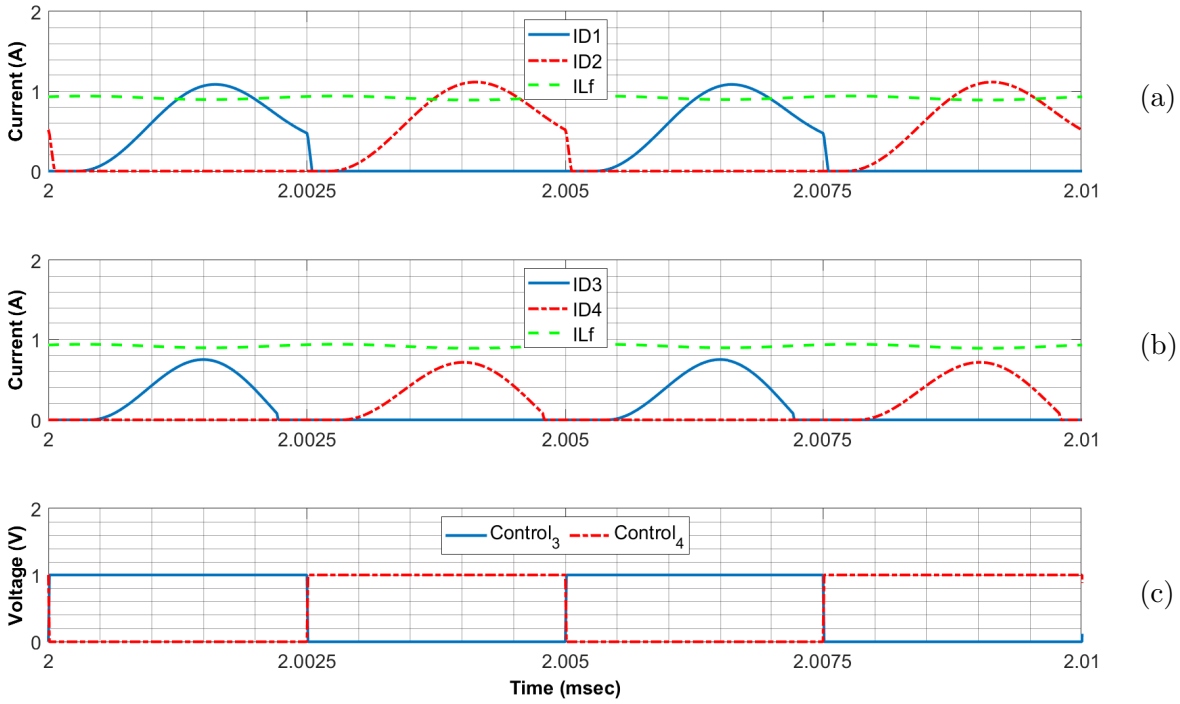


Figure 8-2: Zoom of Fig. 8-1 in the interval from 2 msec to 2.01 msec.

8.2 Case 2

The second case will have the leakage inductances shown in table 8.2. In this case, the voltage of Cell_1 finishes being lower than voltage of Cell_2, instead of having the same voltage. This is produced because of the tolerances effect, but it will be not a problem since an external circuit will shut the PWM off when both cell voltages are very close. The main waveforms of the simulation can be seen in Fig.8-3.

Table 8.2: Parameters for the tolerances in Lk (case 2).

Lk2	0.9Lk1 H
Lk3	1.1Lk1 H
Lk4	0.9Lk1 H

A zoom of Fig. 8-3 has been performed to see a particular issue of current ID2, which is not behaving properly. The zoom can be seen in Fig. 8-4. This is a phenomenon that

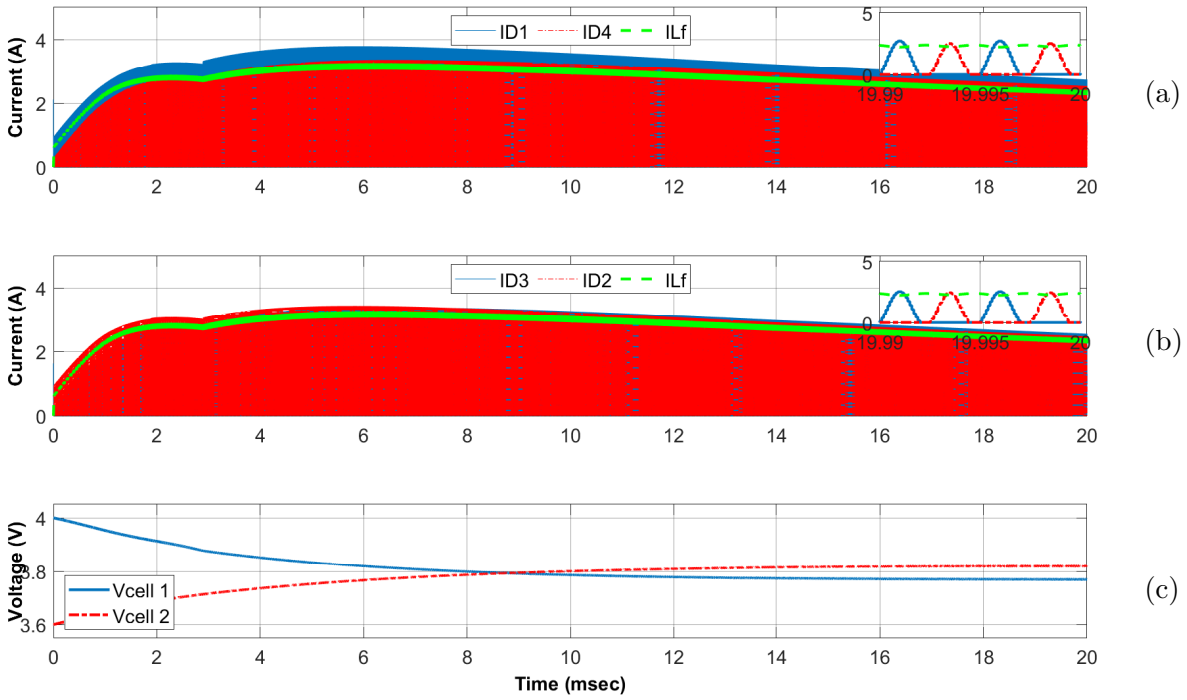


Figure 8-3: Main waveforms for the simulation of the equalizer with the tolerances of table 8.2.

was previously seen in Fig. 5-8a, which has been increased by the effect of the tolerances. The current begins to increase again before the PWM signal changes, due to the voltage difference between the output voltage and the secondary of the transformer, which directly polarizes the diode again in the same semiperiod.

To avoid this effect, another circuit will be proposed to activate the flip-flops when the derivative of the current becomes zero, achieving the lower possible switching losses.

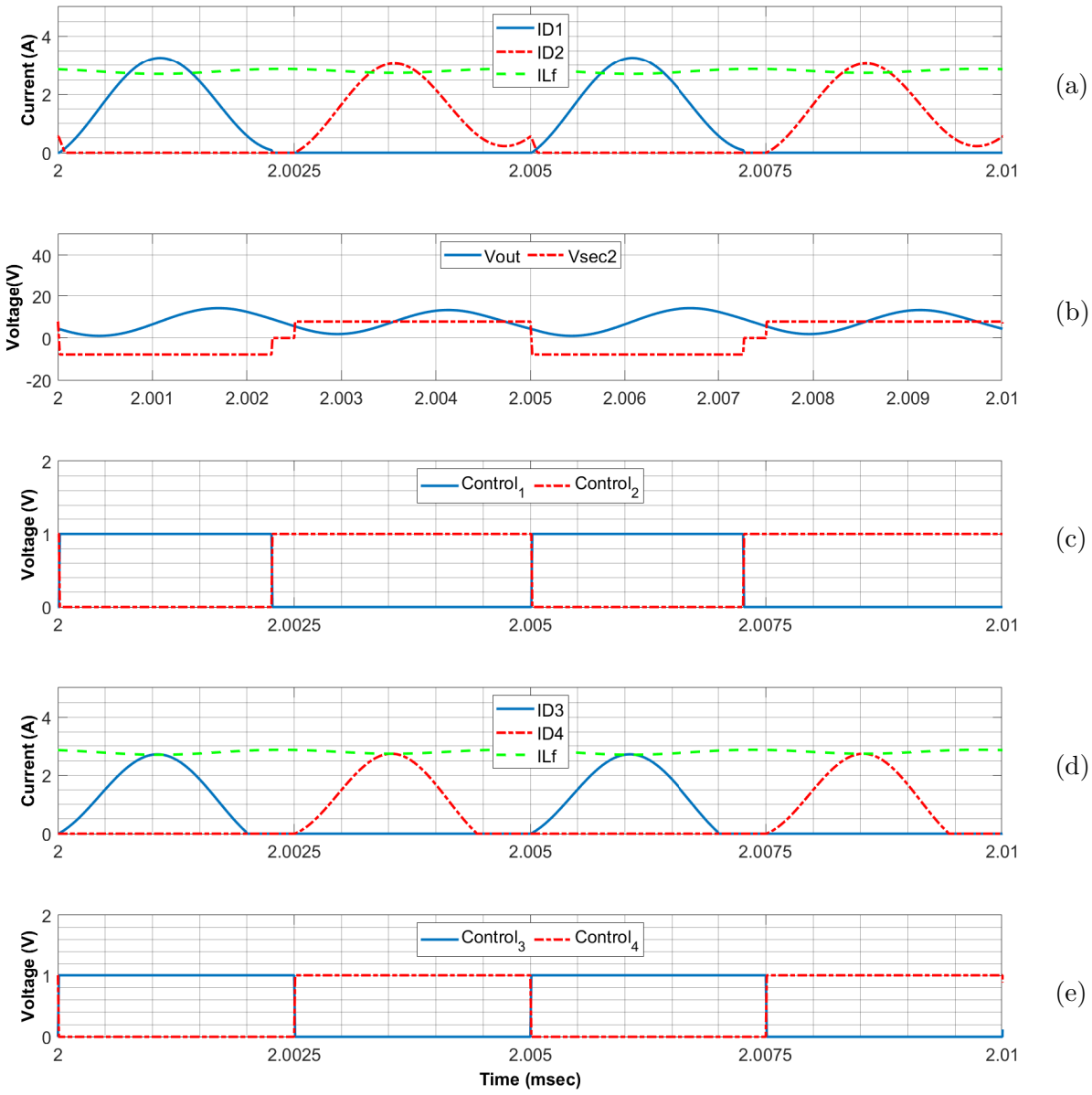


Figure 8-4: Zoom of Fig. 8-3 in the interval from 2 msec to 2.01 msec.

8.2.1 Implementation of a differentiatior circuit

The purpose of this circuit will be to reduce the switching losses that happened in Fig. 8-4a. This was explained because the output voltage became higher than the voltage on the secondary of the transformer before the resonant current returned to zero. This situation did not activate the flip-flops, thus, the transformer was not short-circuited. Being the output voltage higher than the secondary of the transformer, the corresponding inductor Lk started

to charge again, directly polarizing the diode. Now, the differentiatior circuit will short-circuit the transformer in the moment that the second resonance in the same semiperiod begins, reducing the switching losses. The topology of the differenciatior circuit can be seen in Fig. 8-5.

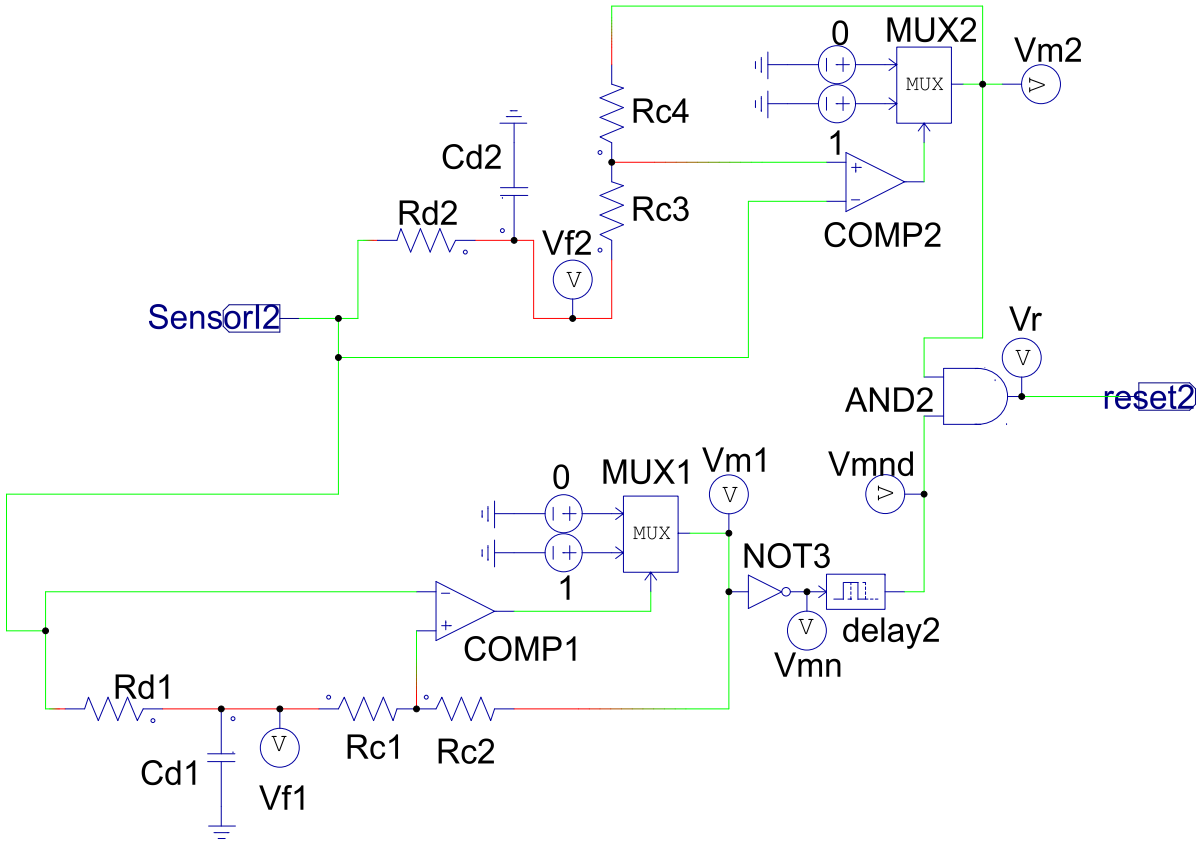


Figure 8-5: Proposed solution to fix the current waveform.

As it can be seen, the solution comprises two comparators with hysteresis. The input signals to comparator $COMP_1$ will be the measured currrent and the measured current delayed with a low pass filter composed by Rd_1 and Cd_1. This circuit detects the derivative of the measured current when it changes from negative to positive or from positive to negative.

As it is wanted to reset the flip flops of the proposed topology only when the current starts to rise again in the same semiperiod, a second comparator is needed. This second

comparator has as inputs the measured current and a low pass filter with a larger delay, composed by Rd_2 and Cd_2. With this second comparator, the output Vr will be only 1 when the current starts to increase for a second time in the same semiperiod. The delay is introduced to simulate the not gate. The parameters used for this circuit will be the ones shown in Table. 8.3. The output signal Vr will be introduced in the proposed topology through an OR gate that will be connected to the reset of the flip-flop. This change in the modified proposed topology can be seen in Fig. 8-6. This way, the differenciator circuit can also activate the reset of the flip-flops.

Table 8.3: Parameters used for the simulation of the differenciator circuit

Cd1	100e-9 F
Rd1	0.04/fs/Cdiff
Rc1	1e3 Ω
Rc2	100e3 Ω
Cd2	100e-9 F
Rd2	Rd1*2.55
Rc3	1e3 Ω
Rc4	220e3 Ω
delay2	0.004/fs sec

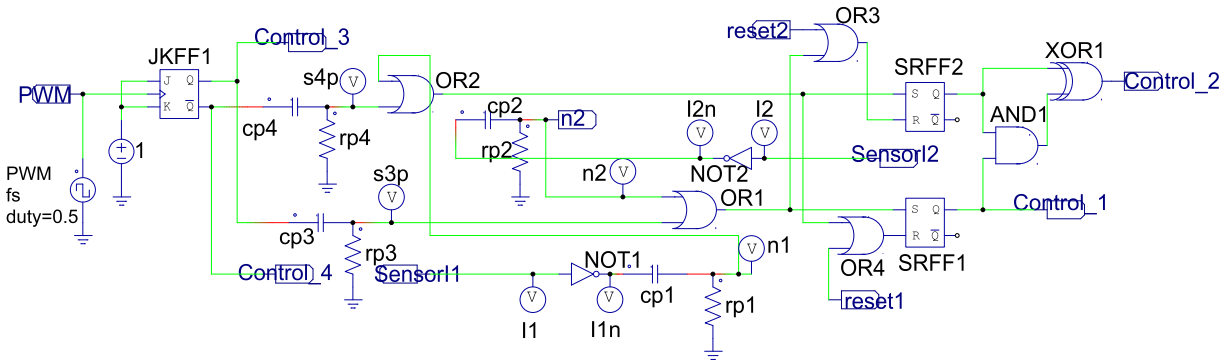


Figure 8-6: Proposed topology modified to include the new resets.

The main waveforms of the differenciator circuit can be seen in Fig. 8-7, where it is shown how the reset is only activated when the current signal starts to increase again. This reset

implies less switching losses in current ID2. Fig. 8-8 shows the effect of the differenciator circuit in the current shape.

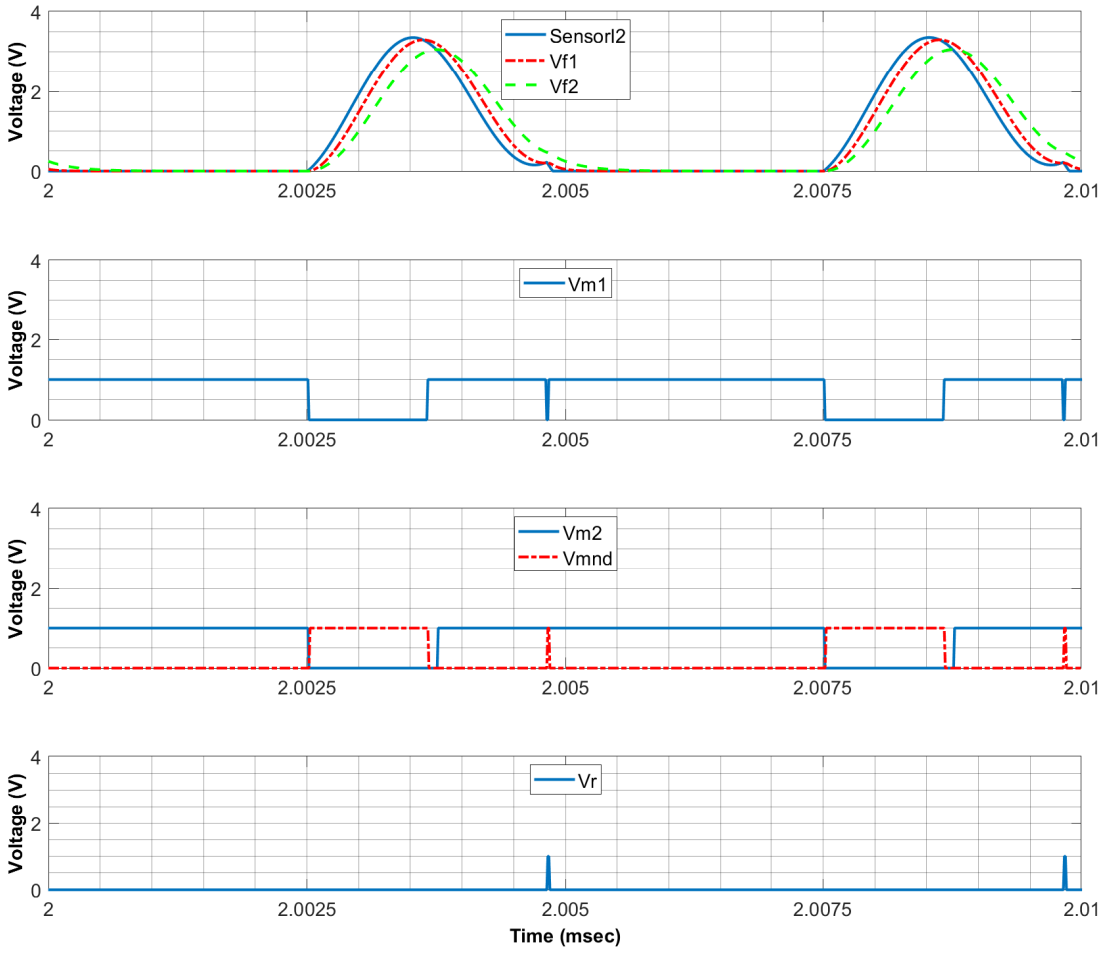


Figure 8-7: Main waveforms of the differenciator circuit.

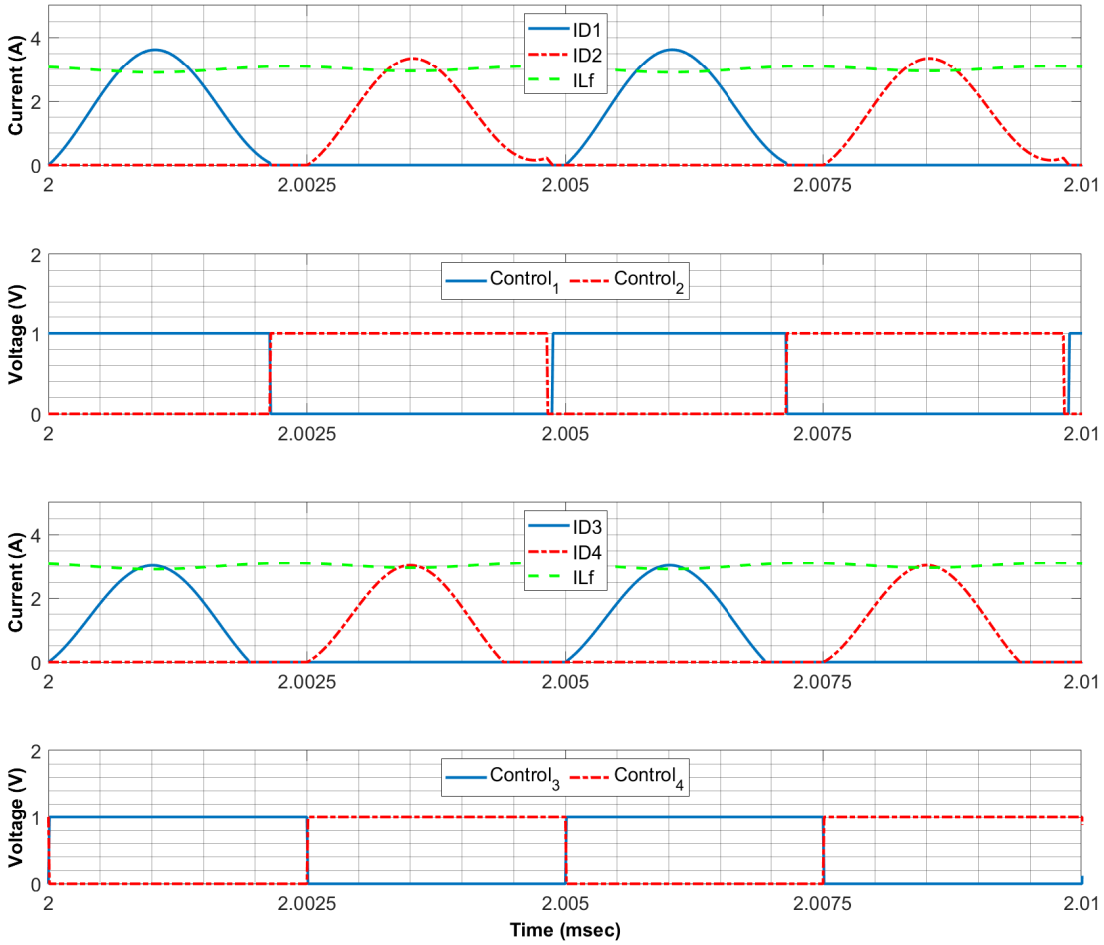


Figure 8-8: Main waveforms of the simulation including the differenciator circuit

9. Conclusion and Future Trends

In this work the research of a specific topology consisting on a modular resonant ET for being used in an Equalizer has been assessed. After commenting briefly the state of the art in battery equalizers, and performing a simulation with the topology, it was seen that a second resonance was produced in the same semiperiod of the clock signal. This second resonance produced high switching losses in the input bridge switches, as current was circulating in the moment of the switches position change.

Moreover, the current peak of the system was too high. After a research, four methods were implemented and explained to reduce the peak current through the system.

A new gate control topology was implemented for the ETs, whose objective is to provide nearly ZCS during the equalization of the input cells. No total ZCS is possible because of the magnetizing current. This new gate control topology solved the problem of the second resonance. However, some intervals during the transient still presented problems where no ZCS was achieved. To reduce the effect of this problem the switching frequency can be varied during the equalization, allowing to achieve ZCS during all the process.

After introducing the magnetizing inductance in the simulation and the input cells initial voltages were changed, it was seen that problems in the gate control signals appeared. When the current was very low, the diodes of the proposed topology were not able to detect when was current flowing through the system, making the gate control signals to stop working properly. Two solutions were implemented to fix this problem: Introducing series capacitors, and modifying the proposed topology, so that the set to one

flip-flop was the reset to the other. The second solution may be preferred because peak current is lower, thus, less conduction losses are achieved.

A simulation with a high value of the input cells capacitance was also performed. The equalization in this case is very slow, thus, it was nearly impossible to appreciate changes in the input cells voltages. However, the current shapes were behaving as expected.

Also the effect of the tolerances was simulated, giving equalization problems in some intervals. A differenciator circuit was implemented to reduce the switching losses when the current started to increase again in the same semiperiod. These problems may be also fixed with the variation of the switching frequency, but a deeper research should be done with this parameter. With the variation of the switching frequency, the differenciator circuit may not be necessary. More studies should be also performed with the effect of the tolerances, as this is something that is almost no information about in other papers.

To conclude, the proposed topology seemed to be working fine in simulation, giving the wanted results. The combination of this new gate control topology and the variation of the switching frequency could provide a very high efficiency and fast speed of the battery-cell equalizer. A simulation with three or more cells can be also performed in the future.

This project pretended to work also in the manufacturing of a prototype to try the proposed topology, but finally it was mainly focused in the simulations of the system. A prototype to validate this proposed topology can be developed in the future. The topology can be tried with batteries or with supercapacitors in different scenarios.

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