

Variable-width Hysteretic Analog Control for QSW-ZVS and TCM source/sink converters

Aitor Vazquez, *Member, IEEE*, Kevin Martin, *Student Member, IEEE*, Manuel Arias, *Member, IEEE*, and Javier Sebastian, *Senior Member, IEEE*.

Abstract- This paper proposes a very simple analog control for Quasi-Square-Wave Zero Voltage Switching (QSW-ZVS) and Triangular Current Mode (TCM) bidirectional converters. The proposed circuit controls the inductance current thanks to the use of a variable-width hysteretic current mode control. The upper and lower bounds of the hysteretic band are clamped to ensure QSW-ZVS operation with a single current command and independently from power flow direction. This enables the control to achieve a seamless transition between source and sink modes. The advantages and disadvantages of the proposed analog control are analyzed and two different power converters are built to demonstrate the validity of this solution: a 50W, 48V to 24V bidirectional buck converter and a 100W, 24V to 48V bidirectional boost converter.¹

I. INTRODUCTION

The presence of active loads and energy storage devices in power electronics systems has become very popular in the last decades. Different types of applications, such as zero emissions buildings [1], [2], electric mobility [3]-[5] or dc distribution grids [6]-[9], include more renewable energy sources in their power distribution architecture [10]-[13]. These sources impose two important characteristics: they generate a dc current or voltage; and they need energy storage systems, which, additionally, could be used for managing the energy in a smartest way. In this sense, the trend is combining traditional passive loads (those that only demand energy) with active loads (those with the capability to generate power under certain conditions, injecting current to the distribution system or the primary energy source). Therefore, bidirectional converters are mandatory to control these active loads. Furthermore, these bidirectional power converters are responsible for regulating its output voltage to provide a stable bus for any connected load (passive or active). This kind of converters are usually known as source/sink converters [14], as they can source current to the active load or sink it back into the primary energy source. The former case is the traditional passive in power systems or when an active load demands energy; the latter can appear when a single active load is connected to the output of the converter or even if several active and passive loads are connected and the passive loads demand less power than the power injected by the active loads.

Dc-dc power converters are typically designed for achieving high efficiency at full load. However, in the previously stated applications, converter efficiency at medium and low power is

actually more important. This requirement is based on the fact that energy storage systems need to be charged and discharged properly to keep their lifespan. Moreover, some active loads and renewable energies can only generate a partial amount of power during certain periods of time. Hence, a bidirectional dc-dc source/sink converter with a high efficiency at medium and light load is required in these applications.

Taking into consideration this need, a possible approach can be the use of Quasi Square-Wave Mode with Zero Voltage Switching (QSW-ZVS) [15], also known as Triangular Current Mode (TCM) [16]. In this operational mode, the inductance value is low and a high current ripple is managed by this power inductor. Thanks to this ripple, the minimum current through the inductance can be negative, allowing to discharge the output capacitor of the transistors during the dead-time. Therefore, ZVS can be achieved and the switching losses are drastically reduced [15]-[18]. This operational mode is very attractive when the design requires high efficiency at light loads. However, the control has to guarantee the operation in this particular mode, even when an active load is connected to the converter. In order to do so, the switching frequency has to increase when power decreases and vice versa, both to keep regulated the output voltage and to maintain ZVS (i.e. the large current ripple and the necessary amount of negative current).

This paper proposes a very simple analog control for QSW-ZVS and TCM bidirectional source/sink converters. The solution is based on a variable-width hysteretic current mode control (HCMC), in which only one command signal coming from a feedback loop is used. The proposed control can be easily adopted for different topologies and it allows us to achieve a smooth transition between source and sink mode.

This work is organized as follows. In Section II a summarized review of previously published control methods for QSW-ZVS is first introduced. After this, the proposed HCMC controller is presented. In Section III two different design examples are shown: for a synchronous buck converter and for a bidirectional boost converter. Based on this implementation, two different prototypes are built and tested in the laboratory. The main experimental results are summarized in Section IV. Finally, Section V outlines the conclusions of this work.

This work was supported in part by the Spanish Government under project MINECO-17-DPI2016-75760-R; in part by the Principality of Asturias under Severo Ochoa grant BP14-085; and in part by the European Regional Development Fund Grants.

A. Vazquez, K. Martin, M. Arias and J. Sebastian are with the Department of Electrical Engineering, Power Supply Systems Group, University of Oviedo, Gijón, 33204, Spain (e-mail: {vazquezaitor, martinkevin, sebas, ariasmanuel}@uniovi.es).

II. PROPOSED ANALOG CONTROL

A. Previously reported controls

QSW-ZVS and TCM modes impose the use of variable frequency control. Different approaches have been previously published to implement a control which regulates the output voltage and can keep the ZVS condition. Most of the proposed solutions are based on digital control [19]-[22], due to the complexity of managing the exact amount of negative current needed and to match the exact length of dead-time in order to discharge the output parasitic capacitor. In [20] a solution which mixes a digital peak current control and some calculations to establish the dead-time is proposed. In [21] the control calculates the on-time, off-time and dead-time every single switching period by measuring the input and output voltage and the current through the inductance. Furthermore, in [22] a digital valley current control is also proposed. All these solutions have two common disadvantages: they are, in general, complex and they require several measurements (voltages and current). Trying to avoid the first disadvantage, in [19] a very simple control based on events is proposed in which no calculation is made. However, even with this simplest approach, current and voltages still need to be measured. Moreover, the bidirectional implementation of this control needs twice as many voltage and current sensors. Another important disadvantage of all the previously presented control techniques is that the bidirectional power flow requires a transition between modes. In some cases, this change is only the measured current or the compared value (i.e. peak or valley current through the inductor). In other cases, it requires a complete different control scheme (replacing the measured output voltage by the input voltage, changing the feedback loop, etc.).

As it is well known, digital control has several advantages, such as adaptability and flexibility; however, the cost is the main disadvantage of these platforms. In the previously stated applications, the cost is a very restrictive constraint of design. This requirement is especially critical in dc nano and pico-grids, in which the power converters should be as simpler as possible, compact and inexpensive. Therefore, a simpler analog controller can be more adequate than a digital control for these applications. This paper aims to propose a very simple analog control, very inexpensive, with fewer components, able to perform QSW-ZVS mode in source/sink power converters and with a seamless change between modes.

B. Variable-width hysteretic current mode control

Some analog controllers available in the market are limited to control the peak or valley values of the inductance current but not both of them simultaneously [23]. Other possible controllers that allow to somehow control the peak and valley values are the Ramp Pulse Modulation (RPM) controllers [24]-[29]. These controllers were originally proposed to enhance the dynamic response of point of load converters by adding an internal ramp. This ramp was compared with the difference of the output voltage error and the current through the inductor. These controllers keep the converter working with almost the same switching frequency between half and full load operation. When the converter works at light load, the RPM controller

forces the converter to enter asynchronous Discontinuous Conduction Mode (DCM) and the switching frequency decreases. Due to this, bidirectional power flow is not allowed in RPM controllers. Therefore, another approach must be found.

Correct operation of QSW-ZVS mode requires keeping the inductor current within an upper and a lower bound as well as bidirectional power flow. As the current measurement was already required for the traditional QSW-ZVS voltage mode control, as it was depicted in Fig. 1, it seems appropriate to use a hysteretic current mode control [30]. Take as an example the generic theoretical waveform shown in Fig. 2, where the inductor current and the magnetizing and demagnetizing intervals are shown. The majority of peak current or valley current analog controllers only regulates i_{ctrl} or i_{ZVS} , keeping a constant magnetizing time (i.e. on-time, t_{on}) or a constant demagnetizing time (i.e. off-time, t_{off}) with a variable switching frequency.

Traditional HCMC analog controllers have a fixed-width hysteretic band, which does not ensure that these boundaries can be changed for a bidirectional power flow. Therefore, for proper QSW-ZVS operation, the hysteretic bandwidth has to be adjusted to keep the current between i_{ctrl} and $-I_{ZVS}$ for forward power flow (i.e. source mode, Fig. 2(a)) and between I_{ZVS} and a negative i_{ctrl} for reversed power flow (i.e. sink mode, Fig. 2(b)). It should be noted that i_{ctrl} is positive when the converter works in source mode and negative when it sinks current. In the same way, the current value i_{ZVS} only has two possible values: $-I_{ZVS}$ in source mode and I_{ZVS} in sink mode.

Variable-width HCMC has been previously implemented digitally for QSW-ZVS and TCM modes by adding and subtracting half the band-width to the control value to generate the upper and lower bounds [30], [31]. This solution cannot be easily implemented with analog circuitry so a different approach is taken.

For forward power flow (i.e. when the converter works in source mode, see Fig. 2(a)), $-I_{ZVS}$ could be used as the lower and fixed bound, while i_{ctrl} acts as the upper and controllable bound which allows a variable width of the hysteretic band. If i_{ctrl} is directly provided by a feedback loop, there is no need to implement analog adders, greatly simplifying the circuit. However, when the power flow has to be reversed, i_{ctrl} becomes negative and I_{ZVS} has to be used as the upper and fixed bound while i_{ctrl} is used as the new lower and controllable

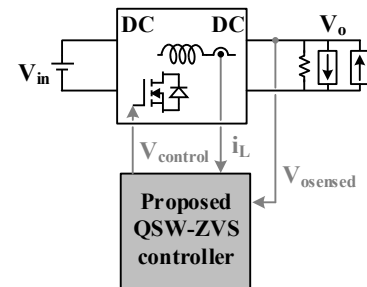


Fig. 1. Block diagram of a dc-dc source/sink converter.

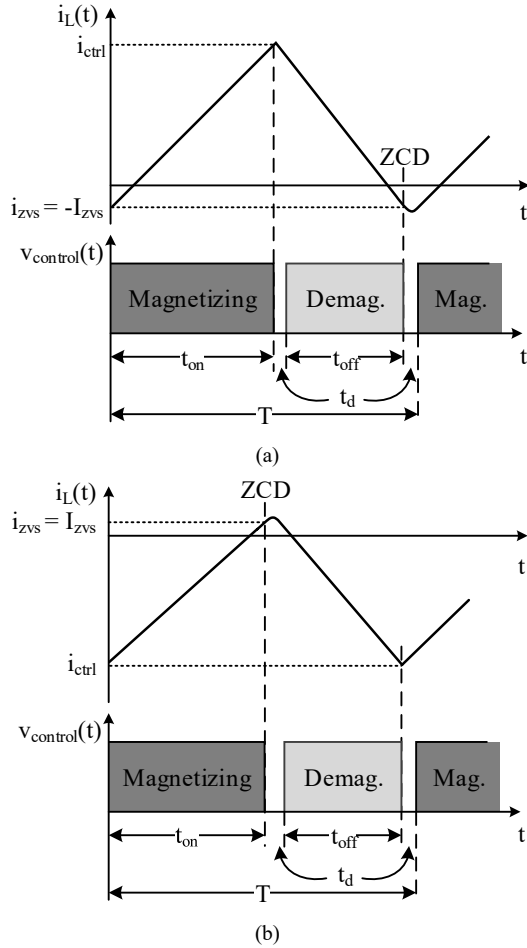


Fig. 2. Inductor current and control signals in QSW-ZVS mode for a generic topology. (a) Source mode. (b) Sink mode.

bound (i.e. the converter has to work in sink mode, see Fig. 2(b)).

In order to allow this change of the bounds, the circuit shown in Fig. 3 is proposed. This analog variable-width HCMC controller is implemented by using two simple comparators and a latch. The only input needed is the command v_{ictrl} , which can be determined by a feedback loop. The upper and lower values are set by clamping this v_{ictrl} voltage to V_{izvs} and $-V_{izvs}$ respectively, as it was stated before. The current through the inductor is compared with the lower and upper bounds and the latch generates two complementary signals, which can be used for driving the main transistors in the power stage. Additionally, a driver stage should be included to add the dead-times between

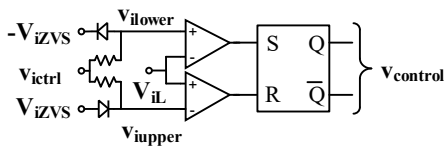


Fig. 3. Proposed circuit for implementing the variable-width HCMC controller.

these signals and to properly drive the power transistors. This basic structure has been presented in [32]; however, it was only used in a buck converter and a detailed analysis was not done.

In order to further clarify the proposed controller, a basic example of implementation is depicted in Fig. 4. Regarding the proposed controller, it should be noted the following remarks:

- The current through the inductor is sensed and a proportional voltage is obtained, v_{iL} .
- The control loop establishes v_{ictrl} , which is proportional to the desired peak or valley value of i_L , depending on whether the converter operates in source or sink mode.
- V_{izvs} and $-V_{izvs}$ fix the resonant current required for the operation in QSW-ZVS or TCM mode, scaled to match the current sensor gain.
- v_{iupper} and v_{ilower} determine the upper and lower bounds of the hysteretic band and depend on v_{ictrl} , V_{izvs} , $-V_{izvs}$ and the power flow direction.

The latch generates the driving signals, v_{mag} and v_{dmag} based on two events: Set and Reset. At the beginning of each switching cycle, the latch is set by the comparator, changing the value of v_{mag} from a logic '0' to a logic '1'. This signal should be applied to the main transistor, in order to magnetize the inductor. When the measured v_{iL} reaches the upper bound (v_{iupper}), the latch is reset and its outputs change. This upper bound is defined as the maximum value between v_{ictrl} and V_{izvs} . Then, v_{mag} is reset to '0' and the demagnetizing interval starts. The complementary output signal (v_{dmag}) can be used to be applied to a synchronous rectifier in a half-bridge configuration. After this interval, when v_{iL} reaches the lower bound (v_{ilower}), the latch is set again and a new switching period begins. This lower bound is defined as the minimum value between v_{ictrl} and $-V_{izvs}$.

During the start-up of the converter, v_{iL} is zero and cannot trigger any Set nor Reset events. In order to ensure the first

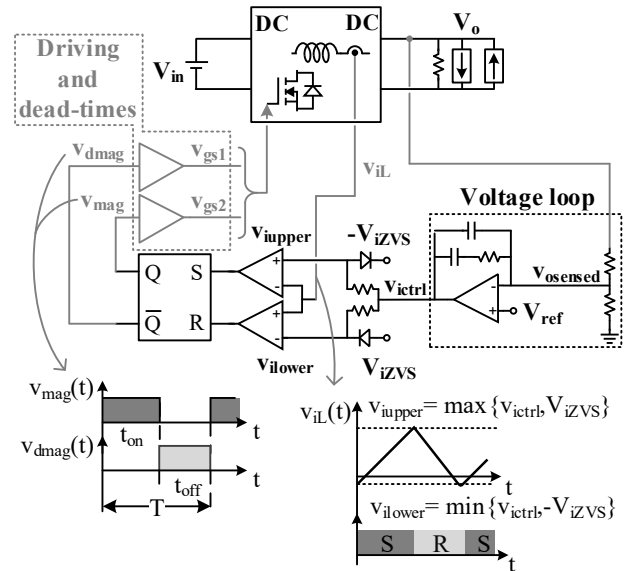


Fig. 4. Proposed variable-width HCMC control with the most representative waveforms.

switching cycle actually starts and the inductor is magnetized, the Q output of the latch should have a default value of '1'. As it was stated before, v_{ictrl} is determined by a control loop. In the example shown in Fig. 4, a simple type II voltage compensator is used to illustrate this. However, other type of control loop can be used instead to set the peak and valley current through the inductor.

A driving stage is mandatory to connect v_{mag} and v_{dmag} to the power stage. This driving circuitry not only provides the necessary amount of current to properly charge and discharge the gate of the MOSFET transistors, but it also includes the dead-times between both signals. The length of these dead-times can be either fixed [33] or adaptive [34], the latter being more efficient but significantly more complex and costly to implement.

Using the proposed circuit, there are three possible scenarios. When v_{ictrl} is greater than V_{iZVS} , the average inductor current is positive, power flows from input to output and the converter operates in source mode (see again Fig. 2(a)). If v_{ictrl} becomes smaller than $-V_{iZVS}$, the average inductor current is then negative, the power flow is reversed and the converter sinks current (see Fig. 2(b)). If v_{ictrl} takes a value between V_{iZVS} and $-V_{iZVS}$, the command provided by the control loop is ignored due to the clamping. In this situation, no net power is transferred to any direction and the converter operates at its maximum switching frequency (i.e. minimum switching period), which depends on V_{iZVS} , $-V_{iZVS}$ and the inductance value following equation (1)

$$T_{min} = t_{on} + t_{off} + 2 \cdot t_d = 2 \cdot I_{ZVS} \cdot L \cdot \left(\frac{1}{v_{on}} - \frac{1}{v_{off}} \right), \quad (1)$$

where I_{ZVS} is the corresponding current value for V_{iZVS} , v_{on} is the magnetizing voltage applied to the inductance during t_{on} , v_{off} is the demagnetizing voltage applied to the inductance during t_{off} and t_d is the dead-time.

C. Theoretical values for switching frequency variation, I_{ZVS} and dead-time

Some theoretical expressions can be extracted from the steady-state analysis for both buck and boost converters operating in TCM and QSW-ZVS. The detailed steady-state equations can be found in [15]-[18] as well as in [35]-[37]. Only the most significant expressions are summarized here, in order to help the designer to adjust the proposed control stage and the power stage. In this analysis, only buck and boost converters expressions for QSW-ZVS and TCM are derived; the first equation of the couple is for the buck converter, whilst the second is related to the boost topology.

The first interesting parameter is the variation of the switching frequency. The switching period can be derived directly from the steady-state analysis in terms of power (P), the inductance value (L) and the valley current through the inductor (i_{ZVS}). Hence the following equations can be derived:

$$T_{buck} = \left(\frac{2|P|}{V_o} - 2|i_{ZVS-buck}| \right) \cdot L \cdot \frac{V_{in}}{V_o \cdot (V_{in} - V_o)}, \quad (2)$$

$$T_{boost} = \left(\frac{2|P|}{V_{in}} - 2|i_{ZVS-boost}| \right) \cdot L \cdot \frac{V_o}{V_{in} \cdot (V_o - V_{in})}. \quad (3)$$

As can be seen in (2) and (3), the higher the power, the higher the switching period (i.e. the lower the switching frequency). This implies that the minimum switching frequency is reached at full power.

The second important parameter to set in the control is the value i_{ZVS} which corresponds to the needed current to achieve ZVS. This parameter can be found by applying the ZVS conditions. These are the following ones:

There is always a valid value of i_{ZVS} (even $i_{ZVS}=0$) if:

$$\text{Buck: } V_{in} \leq 2V_o, \quad (4)$$

$$\text{Boost: } V_{in} \leq \frac{V_o}{2}. \quad (5)$$

These are the sufficient ZVS conditions for buck (4) and boost (5) converters when they are working in QSW-ZVS mode ($i_{ZVS}=0$).

If (4) and (5) are not satisfied (i.e. only TCM operation is possible), then:

$$\text{Source mode: } i_{ZVS-buck} \leq -I_{ZVS-buck}, \quad (6)$$

$$\text{Sink mode: } i_{ZVS-buck} \geq I_{ZVS-buck},$$

$$\text{Source mode: } i_{ZVS-boost} \leq -I_{ZVS-boost}, \quad (7)$$

$$\text{Sink mode: } i_{ZVS-boost} \geq I_{ZVS-boost},$$

where the constant values $I_{ZVS-buck}$ and $I_{ZVS-boost}$ can be calculated as:

$$I_{ZVS-buck} = C_{sw} \cdot \omega_o \cdot \sqrt{V_{in}^2 - 2V_o \cdot V_{in}}, \quad (8)$$

$$I_{ZVS-boost} = C_{sw} \cdot \omega_o \cdot \sqrt{2V_o \cdot V_{in} - V_o^2}, \quad (9)$$

where C_{sw} is the equivalent output capacitance of the switching node (i.e. both output capacitances from the MOSFET power transistors in parallel) [34] and:

$$\omega_o = \frac{1}{\sqrt{L \cdot C_{sw}}}. \quad (10)$$

Therefore, once the MOSFET is chosen, it is possible to calculate the value of i_{ZVS} using (8) or (9). After determining i_{ZVS} , by applying (1) it is possible to know the maximum attainable switching frequency when the converter processes zero power.

Finally, the dead-time needed for achieving ZVS depends on the resonant voltage across the switching node and the resonant current between the magnetizing and demagnetizing sub-intervals. Both voltage and current can be calculated by solving the resonant equivalent circuit, yielding [15]-[18] and [35]-[37]:

$$v_{C_{sw-buck}}(t) = V_o \cdot \cos(\omega_o t) + \frac{i_{ZVS-buck}}{C_{sw} \cdot \omega_o} \cdot \sin(\omega_o t) + V_{in} - V_o, \quad (11)$$

$$v_{C_{sw-boost}}(t) = (V_o - V_{in}) \cdot \cos(\omega_o t) + \frac{i_{ZVS-boost}}{C_{sw} \cdot \omega_o} \cdot \sin(\omega_o t) + V_{in}, \quad (12)$$

$$i_{L-buck}(t) = i_{ZVS-buck} \cdot \cos(\omega_o t) + C_{sw} \cdot \omega_o \cdot V_o \cdot \sin(\omega_o t) + V_{in} - V_o, \quad (13)$$

$$i_{L-boost}(t) = i_{ZVS-boost} \cdot \cos(\omega_o t) - C_{sw} \cdot \omega_o \cdot (V_o - V_{in}) \cdot \sin(\omega_o t) + V_{in}. \quad (14)$$

By applying the ZVS conditions to (9) and (10), it is possible to obtain the dead-time, as

$$t_{d-buck} = \frac{1}{\omega_o} \cdot \left[\sin^{-1} \left(-\frac{(V_o - V_{in})}{\sqrt{V_o^2 + \left(\frac{i_{ZVS-buck}}{C_{sw} \cdot \omega_o}\right)^2}} \right) - \tan^{-1} \left(\frac{C_{sw} \cdot \omega_o}{i_{ZVS-buck}} \cdot V_o \right) \right] \quad (15)$$

$$t_{d-boost} = \frac{1}{\omega_o} \cdot \left[\sin^{-1} \left(-\frac{V_{in}}{\sqrt{(V_o - V_{in})^2 + \left(\frac{i_{ZVS-boost}}{C_{sw} \cdot \omega_o}\right)^2}} \right) - \tan^{-1} \left(\frac{C_{sw} \cdot \omega_o}{i_{ZVS-boost}} \cdot (V_o - V_{in}) \right) \right] \quad (16)$$

It should be noted that all the expressions from (9) to (16) are valid for TCM. The equivalent expressions for QSW-ZVS mode are obtained by simply cancelling $i_{ZVS-buck}$ or $i_{ZVS-boost}$ parameter in all the previous equations.

If a fixed dead-time is selected and the input voltage is ranging within certain values, then it is possible to calculate the voltage across the switching node by using (11) and (12). With this voltage, the increase in the switching losses can also be estimated and a tradeoff between the optimum value given by (15) and (16) and the fixed dead-time can be made.

According to this analysis, the proposed controller design only requires three steps. The first one is to calculate the clamping voltages, V_{iZVS} . To do so, soft switching conditions should be met. Therefore, using (6) to (9) the amount of current needed for achieving soft switching (i_{ZVS}) can be obtained. Once i_{ZVS} is known, the dead-time needed for full-ZVS can be calculated using (15) and (16) in the second step. With these values, the overall losses can be estimated using (11) to (14). Finally, in the third step, the compensator of the output-voltage feedback loop can be determined. However, it is important to note that the compensator design is independent of the controller stage; therefore, this compensator can be calculated following the general criteria.

III. EXPERIMENTAL RESULTS

A. Buck and boost prototypes

In order to validate the proposed control circuitry, two different prototypes were built in the laboratory. First, a simple synchronous buck converter is used to illustrate the seamless mode transition. Second, a synchronous boost converter is also built to demonstrate the flexibility of the controller. The main characteristics of both power converters and their components are summarized in Table I.

TABLE I
COMPONENTS AND MAIN SPECIFICATIONS FOR BUCK AND BOOST PROTOTYPES.

Parameter	Buck prototype	Boost prototype
V_{in} [V]	48	24
V_o [V]	24	48
f_s [kHz]	min. 40 max. 320	min. 40-max. 420
P [W]	± 50	± 100
Inductance [μ H]	69.6, RM8, N97, EPCOS. Litz wire 0.3mm. 97 turns	33, SER2918H-333KL. Coilcraft
Output capacitance [μ F]	445	450
Transistors	TPH7R006PL, Toshiba 60V, 60A, 8.9m Ω , 302pF	
Switch driver	ISL6700, Intersil	
Current sensor	CQ-3200. Hall-effect. AKM Semiconductors	

Both converters use exactly the same power MOSFETs because of their relative low price and size, their low on-resistance and an equivalent output capacitor of just 302pF. The converters were designed slightly different: the buck converter is designed to provide a maximum power of ± 50 W switching at 40kHz, whilst the boost converter is developed for providing ± 100 W with the same switching frequency at full load. In order to do so, the inductance value is different for each topology: 69.6 μ H for buck and 33 μ H for boost converter. Moreover, the power inductor of buck converter is custom designed based on a RM8 bobbin, whilst the one used in the boost converter is a commercial one from Coilcraft. Taking into account the inductance value and the output capacitor of the power MOSFETs, the necessary amount of negative current i_{ZVS} is 150mA and 300mA respectively for both converters. These values are calculated using (6) and (7). In both cases, the control circuitry is a simple type II regulator to provide the control command v_{ictrl} and to get a stable output voltage. It is designed following the general tips in [38]-[41] with a relatively small bandwidth and phase margin to clearly show its effect in the measurements. The driver is a basic ISL6700 half-bridge driver, with fixed dead-times.

In this kind of controls, it is critical to have an accurate, noise-free current measurement in order to ensure a tight control of the output voltage and the correct operation in QSW-ZVS of the converter. The implementation of the current sensor becomes a key design aspect, which will mostly impact the cost and the size of the control system. For this work, a CQ3200 Hall effect current sensor [42] is chosen due to three main reasons. First, it is simple to use and requires no additional circuitry, reducing the parts count and volume of the converter. The chosen model also provides a measurement offset, which simplifies the sensing of bidirectional current and removes the need for symmetrical supply voltages across the whole control circuit. Finally, this sensor has a bandwidth of 1MHz, which is enough to reproduce the triangular inductor current i_L . However, it is important to note that the limited bandwidth of the current sensor will slightly clip the peak and valley measurements. This clipping is more significant for larger values of i_L and should be accounted for when setting the clamping voltages for I_{ZVS} and $-I_{ZVS}$. The maximum error measured due to this clipping is around 5% and it keeps almost

constant with the power managed by the converter. In both prototypes, potentiometers are used to compensate the clipping and to ensure that the converter is always able to reach the peak or valley current to operate in QSW-ZVS regardless of the sensor effect. If the whole control circuit proposed in this paper was to be implemented in a single integrated circuit, it would be desirable to use an embedded current sensor with a very high bandwidth or to implement some mechanism which dynamically adapts the clamping values based on the processed power levels.

A detailed schematic circuit is shown in Fig. 5 for the buck converter prototype. A rail-to-rail operational amplifier (LT6220) is used for implementing the type II compensator as a voltage loop. The output of this operational amplifier is clamped as mentioned before, using two simple potentiometers (P_1 and P_2). These voltages establish the upper and lower bounds for the current. The inductor current is measured by using the said CQ3200 Hall effect current sensor. The signal provided by this current sensor is then compared with the upper and lower bounds by means of two rail-to-rail fast comparators (LMV7219). After the comparators, the latch is implemented using two NAND gates (model SN74LVC1G00). The Q signal is, for this buck converter, the magnetizing control signal, and the complementary one is the demagnetizing control signal. The dead-times are constant and they are set by a simple RC network; both R_{td} and C_{td} values are calculated for the needed dead-time to achieve ZVS given by (15) and (16); a pull-down resistor (R_{pd}) is also added for avoiding noise. A generic half-bridge driver (ISL6700) is employed for properly driving both MOSFET transistors. It should be noted that the magnetizing control signal is connected to the gate of S_1 transistor (i.e. the main transistor in source mode, HO output) and the complementary one is connected to S_2 (i.e. to the synchronous rectifier in source mode, LO output). Finally, an auxiliary power supply is employed to obtain the driving voltage (10V) and the voltage needed for the control stage (5V).

In the case of the boost converter prototype, the detailed schematic is almost equal to that employed in the buck converter. There are two small differences which can be seen in Fig. 6. The first one is that the magnetizing and demagnetizing control signals are crossed when compared to the buck converter. Therefore, for the boost converter the Q output of the latch should be connected to the LI input of the driver, because the main transistor in source mode (S_1) is now referred to ground in this converter. Complementary, the demagnetizing control signal is connected to HI input of the driver, because the synchronous rectifier in source mode (S_2) is floating. The second difference is obvious: the type II compensator is different when compared to the previous buck converter. These two differences only depend on the power stage topology used and they only affect to the connection of the driver. The proposed control stage remains the same for both cases.

The prototypes can be seen in Fig. 7, with the sub-stages highlighted and labelled; more precisely, the synchronous buck converter is shown in Fig. 7(a) and the synchronous boost converter is depicted in Fig. 7(b).

For the results shown in Fig. 8, the buck converter operates in steady state while processing 50W in source mode. The scope snapshots show the gate-to-source and drain-to-source voltages of the main power MOSFET. In Fig. 8(a) it can be seen how i_L closely matches the expected waveform when operating at full load. With an output current of 2.08A, the maximum value of i_L is slightly above 4A and its minimum is about 200mA. Due to the manual adjustment required with this implementation, the exact desired value of $-I_{ZVS}$ is not reached and the switching frequency is close to but slightly lower than the expected 40kHz. However, this does not significantly affect the correct operation in QSW-ZVS and the measured efficiency in this operating point is 97.5%.

Fig. 8(b) shows a close-up of the relevant waveforms during the main MOSFET turn-on. It can be clearly seen how, during the dead-time, i_L is negative, discharging the output capacitance of the MOSFET before its gate signal rises. Due to

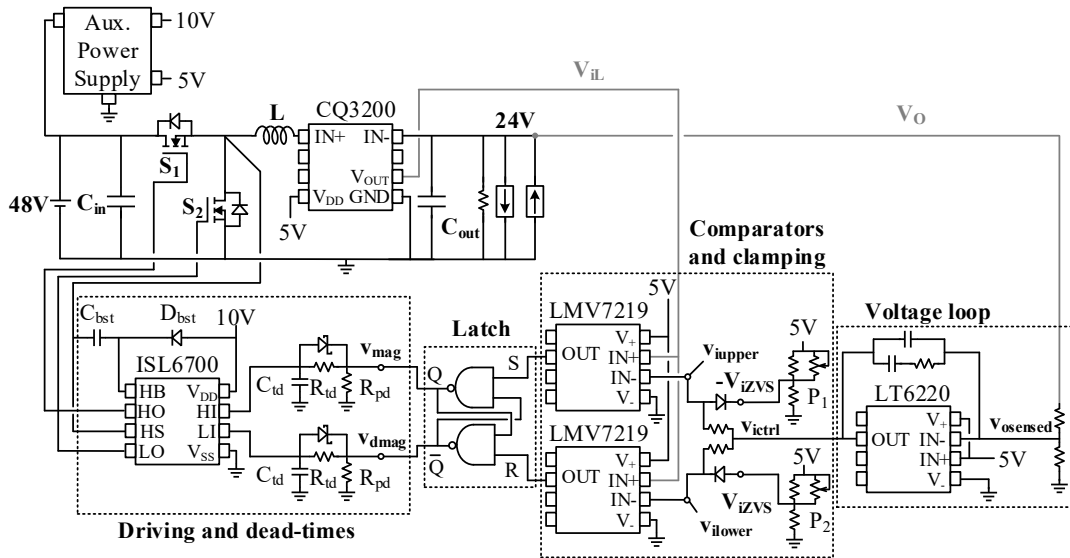


Fig. 5. Detailed schematic for buck converter prototype.

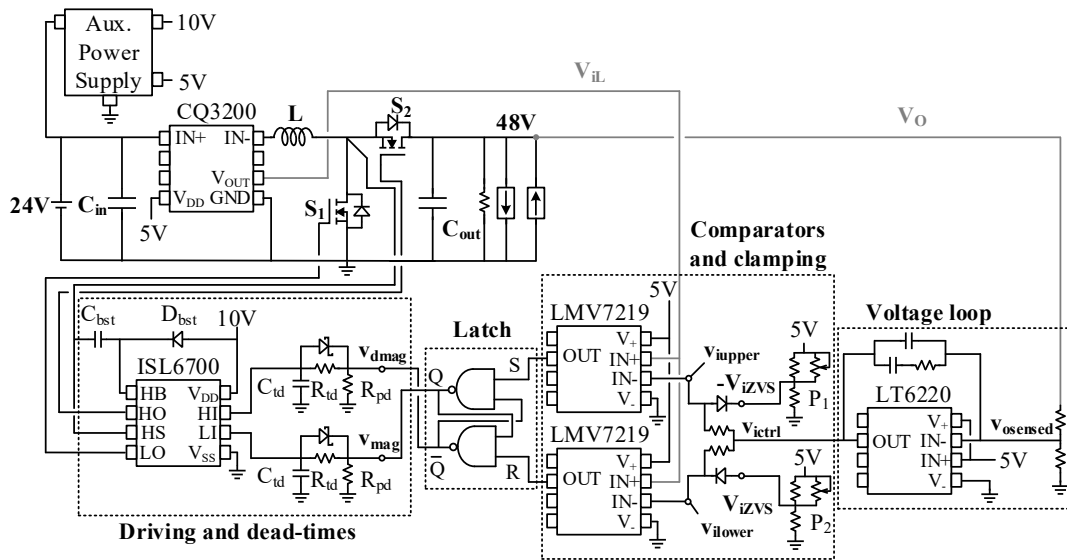


Fig. 6. . Detailed schematic for boost converter prototype.

the fixed length of the dead-times and how difficult it is to precisely adjust the value of $-V_{izvs}$ with the potentiometer, full ZVS is not achieved and the MOSFET is turned on with its output capacitor still charged to a little voltage under 5V. Although the converter operates in a partial soft switching condition, the increase in losses can be neglected. In order to ensure the converter operates exactly in QSW-ZVS mode, a slightly larger dead-time or an additional circuit to ensure that soft switching is always achieved should be used.

The same conclusions can be extracted for the operational waveforms of the boost converter. In this, two different captures of the main waveforms are shown in Fig. 9. Once again, the gate-to-source and drain-to-source voltages correspond to the main MOSFET. In this case, these waveforms are measured at two different power levels, in order to show how the control guarantees the QSW-ZVS operation in the whole power range. Specifically, in Fig. 9(a) the boost converter works at 10W whilst in Fig. 9(b) it provides 100W to the passive load.

As mentioned before for the buck converter, the control keeps the converter working in QSW-ZVS, as can be seen in the close-up depicted in Fig. 10. Even with the variation of the output power level, the control fixes the valley current through the inductor, achieving full ZVS during the main MOSFET turn-on, as can be seen in Fig. 10(a) at 10W and in Fig. 10(b) for 100W. The converters used for testing this control have not been optimized in terms of overall losses. However, the obtained efficiency is high enough due to the operation in QSW-ZVS.

Fig. 11 shows the efficiency against the output power for both converters. For simplicity, only the source mode efficiency is depicted. As can be seen in Fig. 11(a), the measured efficiency of the buck converter peaks a maximum value of 96.48% at 25W approximately. Even though this converter was originally designed for providing a maximum of 50W in source mode, some additional efficiency points were measured at 85W. On the other hand, the efficiency curve of the boost converter is slightly different in comparison with the previous

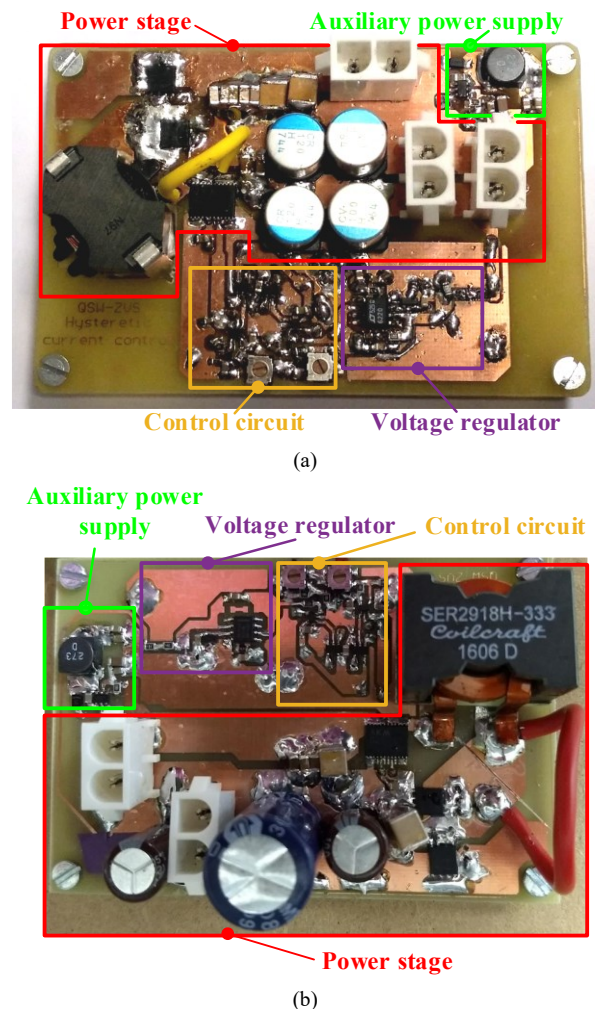


Fig. 7. Pictures of both prototypes. (a) Buck converter. (b) Boost converter.

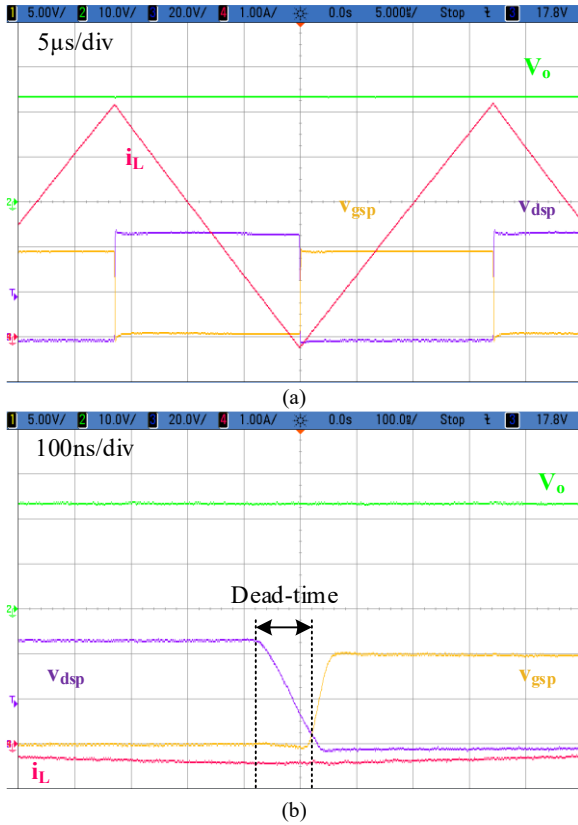


Fig. 8. Buck converter measured waveforms at 50W. CH1: Gate-to-source voltage (5V/div). CH2: Output voltage (10V/div). CH3: Drain-to-source voltage (20V/div). CH4: Inductor current (1A/div). (a) 5 μ s/div. (b) 100ns/div.

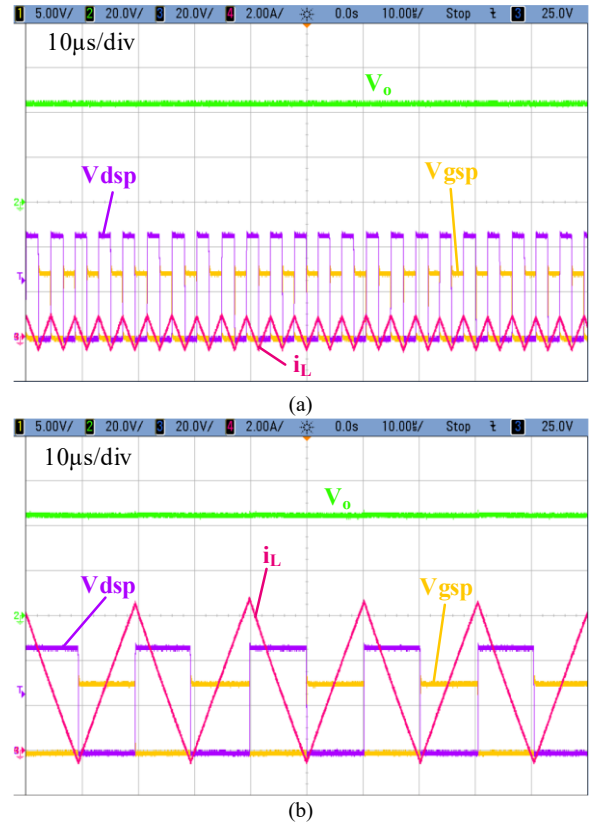


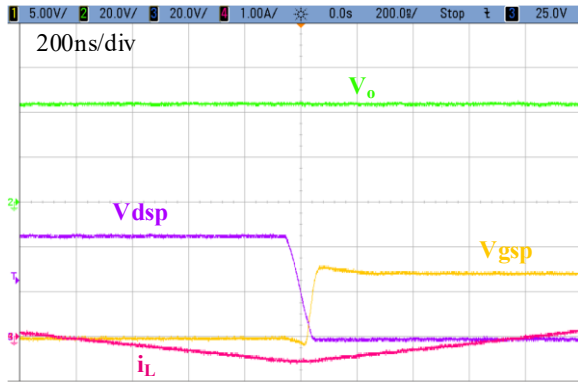
Fig. 9. Boost converter measured waveforms. CH1: Gate-to-source voltage (5V/div). CH2: Output voltage (20V/div). CH3: Drain-to-source voltage (20V/div). CH4: Inductor current (2A/div). Time scale: 10 μ s/div. (a) At 10W. (b) At 100W.

one. This is mainly due to the different design considerations made and the use of different inductance values, materials and components. In particular, this measured efficiency, depicted in Fig. 11(b), reaches a maximum of 97.75% at 28W. Then, it slowly drops to 95% at full load. It should be noted that both efficiencies are measured taking into consideration the control and driving power consumption.

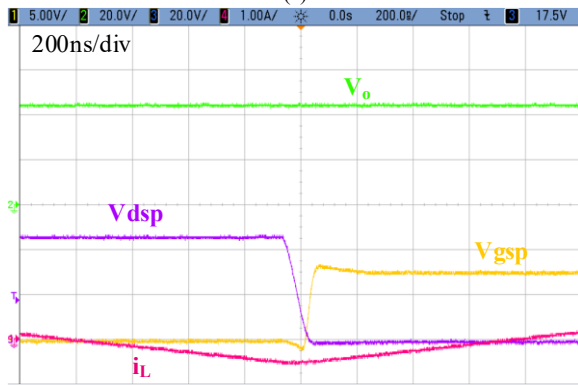
Another important issue in QSW-ZVS mode is the switching frequency variation as a function of the processed power. This variation has been measured for both converters and it is shown in Fig. 12 in source mode for simplicity. For buck converter, (see Fig. 12(a)), the switching frequency ranges from 25kHz at 85W up to 120kHz at 10W. At 50W, the switching frequency is 36kHz, which is slightly below the designed theoretical value of 40kHz. This is mainly due to the non-ideal behavior of the current sensor and the limited band-width of this component previously mentioned. The variation of the switching frequency for the boost converter is depicted in Fig. 12(b). In this case, the switching frequency ranges from 45kHz at full load up to 432kHz at 5W. Once again, the measured switching frequency at full load is slightly lower than the theoretical one, due to the previously stated effects on the current measurement. However, in both cases, the control allows to automatically change the switching frequency and to adapt it to preserve the QSW-ZVS operation.

Fig. 13 shows the dynamic behavior of the proposed control under different source and sink mode transitions. For simplicity, only the buck converter waveforms are shown to illustrate these transitions. The zero reference is the same for all four channels. It must be noted that channels 1 to 3 have an offset of 1.65V due to the current sensor, which is indicated in Fig. 13. It should be noted that, for these figures, the value of I_{ZVS} and $-I_{ZVS}$ in these tests is slightly higher than required to clearly show the hysteresis band during zero power operation.

Fig. 13(a) shows a load step from -50W to 50W. The three different operation modes the converter goes through are highlighted. First, the converter operates in sink mode and the average inductor current is negative. Its upper bound is V_{iZVS} and its lower bound is v_{ictrl} . Shortly after the load step, v_{ictrl} increases, reducing the width of the hysteresis band and the inductor current valley. For a few switching cycles when v_{ictrl} approaches zero, the hysteresis band is defined by V_{iZVS} and $-V_{iZVS}$. During this time, the switching frequency is maximum and there is no net power transfer in any direction. As v_{ictrl} continues increasing, it goes over V_{iZVS} and keeps enlarging the width of the hysteresis band, increasing the inductor current peak to enter source mode and provide the required current to the loads. A small overshoot can be seen in v_{iupper} as the implemented control loop provides a relatively small phase margin, close to 55°. Although the control loop is relatively



(a)



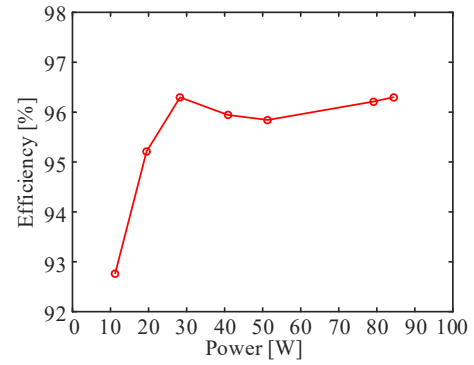
(b)

Fig. 10. Boost converter waveforms detail during the turn-on of the main MOSFET. CH1: Gate-to-source voltage (5V/div). CH2: Output voltage (20V/div). CH3: Drain-to-source voltage (20V/div). CH4: Inductor current (1A/div). Time scale: 200ns/div. (a) 10W. (b) 100W.

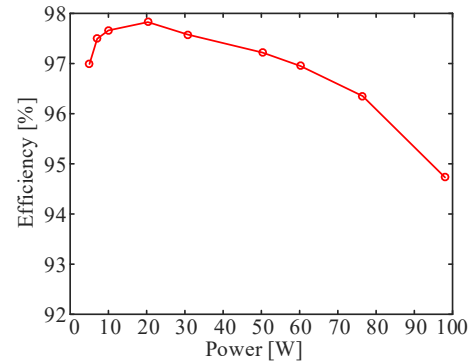
slow to clearly show the transition, it can be seen how V_o does not change significantly.

Fig. 13(b) shows a load step from 50W to 0W, as the passive load is disconnected. The converter goes through three operation modes again. First, the converter operates in source mode with positive average inductor current. Shortly after the load step, v_{ictrl} decreases, and for a few switching cycles there is no net power transfer in any direction. However, the control loop has to correct the output voltage offset caused by the load step and the converter operates in sink mode transferring a very low current from its output capacitor to the power source.

To further validate the proposed controller behavior against load steps, a rising and a falling load step from no load to full load and vice versa are depicted in Fig. 14. In this capture, the output voltage has been measured in AC to observe the dynamic response. As can be seen, the maximum overvoltage is below 200mV (less than 0.8%) and the settling time is around 300ms. Some measurements about the control-to-output transfer function are shown in Fig. 15(a) for buck converter and in Fig. 15(b) for boost converter. These transfer functions have been measured using a frequency response analyzer FRA6340 at different power levels. As can be seen, in both converters the transfer function is similar to a first order system, with a relatively low frequency pole, as it was expected due to the compensator design developed in this work. It should be noted

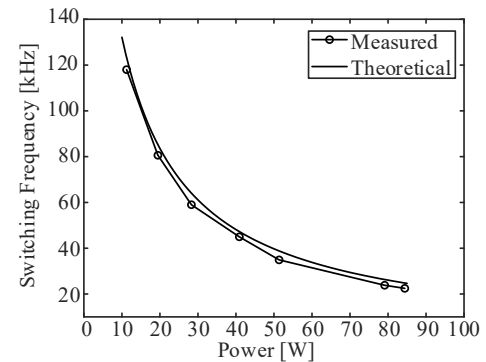


(a)

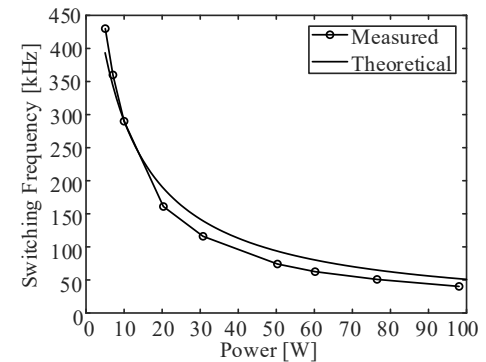


(b)

Fig. 11. Measured efficiency in source mode. (a) Buck converter. (b) Boost converter.



(a)



(b)

Fig. 12. Switching frequency variation versus the output power in source mode. (a) Buck converter. (b) Boost converter.

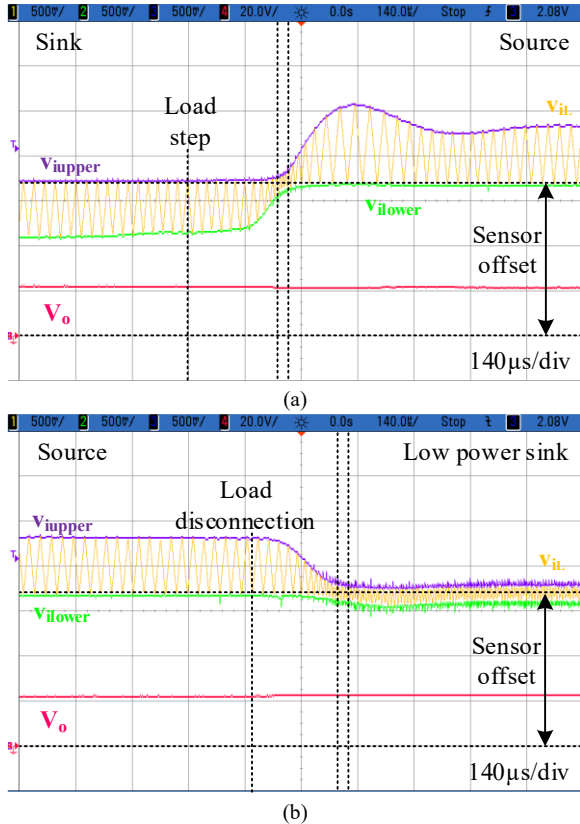


Fig. 13. Dynamic behavior of the QSW-ZVS source/sink buck converter: (a) load step from -50W (sink) to 50W (source) (b) load step from 50W (source) to 0W. CH1: Measured inductor current, v_{iL} (500mV/div). CH2: Lower hysteresis bound, $v_{i\text{lower}}$ (500mV/div). CH3: Upper hysteresis bound, $v_{i\text{upper}}$ (500mV/div). CH4: Output voltage (20V/div). Time scale: 140µs/div.

that the theoretical analysis in regards the dynamic behavior for TCM and QSW-ZVS modes is out of the scope of this paper.

Finally, Fig. 16 shows the steady state operation of the converter with an open circuit at its output, processing 0W. Although the output voltage is correctly regulated and the inductor current is well within bounds, it can be seen how this implementation, as most current based controls, is noise sensitive. While the current measurement is rather clean, both $v_{i\text{lower}}$ and $v_{i\text{upper}}$ pick up switching frequency noise. The main consequence of this effect is the increasing in the current ripple through the inductor when the converter works with no load. This may lead into a higher power consumption during the stand-by periods that should be taken into account if some regulation may apply. Integration of the control on a single IC could mitigate this issue.

B. Comparison with other control techniques

In order to highlight the advantages and disadvantages of the proposed control circuit, a basic comparison has been conducted in this section. Only the previously published works are used in this section and those techniques which deal with QSW-ZVS or TCM controllers. The main parameters of this

comparison are summarized in Table II. For the digital controllers, a brief description of the computational cost has been included. In these type of controllers, the component count is not specified, due to the complexity to obtain the number of logic gates or Look-Up Tables (LUT) from the manuscripts.

As can be seen in Table II, the digital controllers are preferred for interleaving solutions and adaptive scenarios. In those

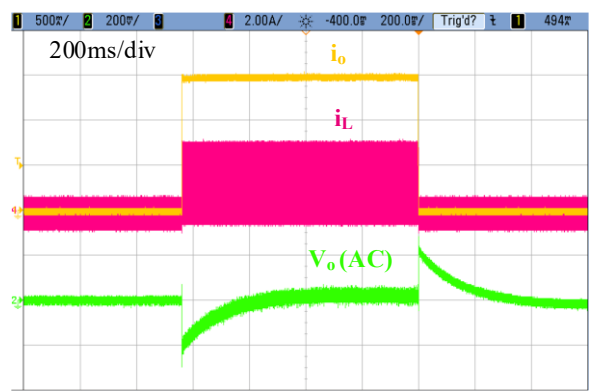


Fig. 14. Buck converter load step, from no load to full load and viceversa. CH1: Output current (500mA/div). CH2: Output voltage in AC (200mV/div.). CH4: Current through the inductor (2A/div). Time scale: 200ms/div.

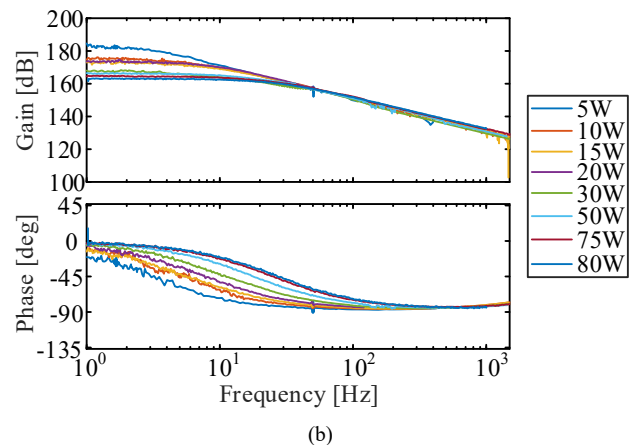
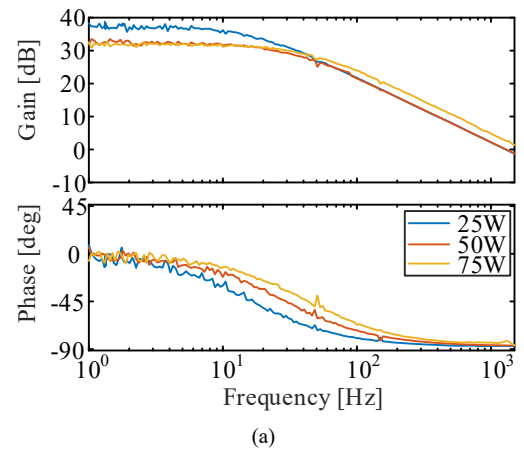


Fig. 15. Control-to-output transfer function measured at different power levels. (a) Buck converter (b) Boost converter.

IV. CONCLUSIONS

In this paper, an analog variable-width HCMC controller has been proposed for QSW-ZVS source/sink converters. The proposed controller has several advantages. First of all, it is a very simple approach, low price solution and low component count for implementing a QSW-ZVS mode: only a latch, two comparators and two clamping diodes are needed; besides, only a control command is necessary to set the peak or valley current. Second, the controller can be applied to every single PWM-based topology for implementing QSW-ZVS mode; the control can automatically vary the switching frequency, independently on the topology or the design, as the experimental results have demonstrated with a buck and a boost converter. Third, the controller can be implemented with different compensators for regulating current or voltage, depending on the final application. And fourth, the proposed controller achieves a smooth transition among the three modes (source, sink and no load) with any additional circuitry.

Conversely, the proposed analog controller also has several disadvantages. First, the quality of the current sensor chosen for this application plays a critical role in the implementation of the control circuit. The controller imposes the use of a high-bandwidth, highly linear current sensor, which can significantly simplify the need for additional circuitry which compensates the distortion of the measured inductor current, but it increases the cost of this solution. In this sense, the use of a simply sensing resistor could be more adequate to avoid these problems. However, this solution requires an additional voltage conditioner and it should be tested in future works. Second, the absence of a clock signal may lead into several problems if any sort of synchronization would be needed. This was the case of multi-phase power converters (or modular converters), in which an interleaved approach is needed for the control signals. In such a case, the proposed controller cannot be easily synchronized. In this sense, this synchronization problem should be addressed in future works with the proposed controller stage.

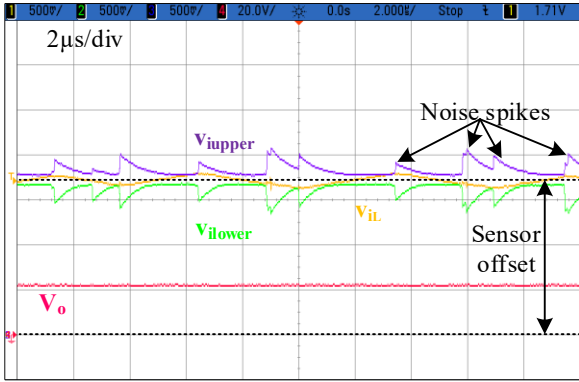


Fig. 16. Static operation of the QSW-ZVS source/sink buck converter at 0W, showing the control commands. CH1: Measured inductor current, v_{il} (500mV/div). CH2: Lower hysteretic bound, v_{ilower} (500mV/div). CH3: Upper hysteretic bound, v_{iupper} (500mV/div). CH4: Output voltage (20V/div). Time scale: 2µs/div.

applications, the digital controllers have a clear advantage, due to their flexibility. However, they usually need at least two voltage sensors and an additional current sensor per cell. Moreover, the computational cost is relatively high, because a DSP or a FPGA is employed in all cases. When looking at the analog solutions analyzed in Table II, it can be seen that only one uses a reduced number of discrete elements (similar component count to the proposed controller here). The other ones are much more complex regarding the number of elements needed. Besides, only one analog controller is able to perform a bidirectional power flow; nevertheless, in this case the transition between modes (i.e. power flow direction) is not automatically implemented and it needs an external signal to do so. Therefore, the analog controller proposed in this work presents a reduced component count with the bidirectional capability including a seamless transition between modes. On the other hand, the solution presented here is only proposed for single-stage power converters and current sharing and interleaving techniques must be studied in the future.

TABLE II
COMPARISON WITH OTHER CONTROL TECHNIQUES.

Reference	Type	Control method	Computational cost	Component count	Voltage sensors	Current sensors	Interleaving	Bidirectional
[16]	Digital	LUT based on power level + ZCD	DSP + FPGA + PI	N.A.	2	1 per cell	Yes	No
[19]	Digital	ZCD + ZVD events based on comparators	FPGA + PID	N.A.	2	1	Yes	Yes
[20]	Digital	Average current control	DSP + PI	N.A.	1	1 per cell	Yes	Yes
[21]	Digital	Current and frequency calculation	DSP + PID	N.A.	2	1	Yes	Yes
[22]	Digital	Switching surface controller	FPGA + PID	N.A.	1	0	No	No
[23]	Analog	Hysteretic single band with off-time limiter	Compensator + Hysteresis comparator + limiter + OR gate	5	1	1	No	No
[25]	Mixed	Hysteretic current band + digital controller for interleaving	Microcontroller + PLL + DAC + discrete logic elements	27	2	1	Yes	Yes
[26]	Analog	Hysteretic current band	Comparator + phase detector + charge pump + delay generator	24	1	0	No	No
Proposed	Analog	Variable Hysteretic Current	Compensator + comparator + latch + driver	6	1	1	No	Yes

REFERENCES

- [1] European Union, "Implementing the Energy Performance of Buildings Directive (EPBD)," Concert Action Energy Performance of Buildings, October 2013. [Online]: <http://www.epbd-ca.org/Medias/Pdf/CA3-BOOK-2012-ebook-201310.pdf>. [Last accessed: Jul. 2017].
- [2] Energy European Commission, Nearly zero-energy buildings. [Online]: <https://ec.europa.eu/energy/en/topics/energy-efficiency/buildings/nearly-zero-energy-buildings>. [Last accessed: Jul. 2017].
- [3] R. Naayagi, "A review of more electric aircraft technology," Energy Efficient Technologies for Sustainability (ICEETS), 2013 International Conference on, pp. 750-753, April 2013.
- [4] A. Boulanger, A. Chu, S. Maxx and D. Waltz, "Vehicle Electrification: Status and Issues," *Proceedings of the IEEE*, vol. 99, no. 6, pp. 1116-1138, June 2011.
- [5] C. Chan and Y. S. Wong, "The state of the art of electric vehicles technology," *Power Electronics and Motion Control Conference, 2004. IPEMC 2004. The 4th International*, vol. 1, pp. 46-57, Aug. 2004.
- [6] T. Dragičević, X. Lu, J. C. Vasquez and J. M. Guerrero, "DC Microgrids—Part I: A Review of Control Strategies and Stabilization Techniques," in *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4876-4891, July 2016.
- [7] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna, and M. Castilla, "Hierarchical control of droop-controlled AC and DC microgrids — a general approach toward standardization," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, Jan. 2011.
- [8] M. Rodriguez, G. Stahl, L. Corradini, and D. Maksimovic, "Smart DC power management system based on software-configurable power modules," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1571-1586, Apr. 2013.
- [9] L. R. Lewis, B. H. Cho, F. C. Lee and B. A. Carpenter, "Modeling, analysis and design of distributed power systems," *Power Electronics Specialists Conference, 1989. PESC '89 Record., 20th Annual IEEE*, Milwaukee, WI, 1989, pp. 152-159 vol.1.
- [10] Sparacino, A.R.; Reed, G.F.; Kerestes, R.J.; Grainger, B.M.; Smith, Z.T., "Survey of battery energy storage systems and modeling techniques," Power and Energy Society General Meeting, 2012 IEEE, vol., no., pp.1,8, 22-26 July 2012.
- [11] Affanni, A.; Bellini, A.; Franceschini, G.; Guglielmi, P.; Tassoni, C., "Battery choice and management for new-generation electric vehicles," *Industrial Electronics, IEEE Transactions on*, vol.52, no.5, pp.1343,1349, Oct. 2005.
- [12] F. Blaabjerg, F. Iov, T. Kerekes and R. Teodorescu, "Trends in power electronics and control of renewable energy systems," *Power Electronics and Motion Control Conference (EPE/PEMC), 2010 14th International*, pp. K-1-K-19, Sept. 2010.
- [13] Y. Li and Y. Han, "A Module-Integrated Distributed Battery Energy Storage and Management System," in *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8260-8270, Dec. 2016.
- [14] R. Kollman, J. Betten, and B. S. Lee, "Power supply solution for DDR bus termination," Analog Applications, 2001.
- [15] V. Vorperian, "Quasi-square-wave converters: topologies and analysis," *IEEE Transactions on Power Electronics*, vol. 3, no. 2, pp. 183-191, Apr. 1988.
- [16] C. Marxgut, J. Biela, and J. W. Kolar, "Interleaved triangular current mode (TCM) resonant transition, single phase PFC rectifier with high efficiency and high power density," in *Proc. Int. Power Electronics Conf.- ECCE ASIA -*, Jun. 2010, pp. 1725-1732.
- [17] D. Maksimovic, "Design of the zero-voltage-switching quasi-squarewave resonant switch," in *Proc. 24th Annual IEEE Power Electronics Specialists Conf. PESC '93 Record*, Jun. 1993, pp. 323-329.
- [18] B. Ray and A. Romney-Diaz, "Constant frequency resonant topologies for bidirectional DC/DC power conversion," in *Proc. 24th Annual IEEE Power Electronics Specialists Conf. PESC '93 Record*, Jun. 1993, pp.1031-1037.
- [19] A. Vazquez, A. Rodriguez, D. G. Lamar and M. M. Hernando, "Master-slave technique for improving the efficiency of interleaved synchronous boost converters," *2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Santander, 2014, pp. 1-9.
- [20] Andreassen, Pal; Undeland, T.M., "Digital Control Techniques for Current Mode Control of Interleaved Quasi Square Wave Converter," *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, vol., no., pp.910,914, 16-16 June 2005.
- [21] Jong-Bok Baek; Woo-In Choi; Bo-Hyung Cho, "Digital Adaptive Frequency Modulation for Bidirectional DC-DC Converter," *Industrial Electronics, IEEE Transactions on*, vol.60, no.11, pp.5167,5176, Nov. 2013.
- [22] Yousefzadeh, V.; Babazadeh, A.; Ramachandran, B.; Alarcon, E.; Pao, L.; Maksimovic, D., "Proximate Time-Optimal Digital Control for Synchronous Buck DC-DC Converters," *Power Electronics, IEEE Transactions on*, vol.23, no.4, pp.2018,2026, July 2008.
- [23] R. Redl and N. O. Sokal, "Current-mode control, five different types, used with the three basic classes of power converters: Small-signal AC and large-signal DC characterization, stability requirements, and implementation of practical circuits," in *Proc. IEEE Power Electronics Specialists Conf*, Jun. 1985, pp. 771-785.
- [24] T. F. Schiff, "Switching Power Supply Control," U.S. Patent, no. US 7,595,617, Sept. 2009.
- [25] On Semiconductor, "ADP3211: 7-Bit, Programmable Single-Phase Synchronous Buck Controller." [Online]: <https://www.onsemi.com/pub/Collateral/ADP3211-D.PDF>. Last time accessed: Feb. 2019.
- [26] K. Lee and H. Zou, "Comparison between Ramp Pulse Modulation (RPM) and constant frequency modulation for the beat frequency oscillation in voltage regulators," 2010 IEEE Energy Conversion Congress and Exposition, Atlanta, GA, 2010, pp. 3101-3106.
- [27] K. Lee, "Method for Generating a Signal and Structure Therefor," U.S. Patent, no. US 8,643,355, Feb. 2014.
- [28] Y.C. Wan, J.R. Huang, C.H. Wang, C.F. Chung, "Voltage Regulator and Pulse Width Modulation Signal Generation Method Thereof," U.S. Patent, no.20120146608, Jun. 2012.
- [29] V. Li, P. Liu, Q. Li and F. C. Lee, "Improved current-mode control with single-cycle load transient," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 343-349.
- [30] Y. Wen and O. Trescases, "Analysis and comparison of frequency stabilization loops in self-oscillating current mode DC-DC converters," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4753-4766, Oct. 2013.
- [31] P. Scortaru, D. V. Nicolae, M. Cernat, and Z. Puklus, "Reversible DCto-DC converter for a dual voltage automotive system using zero voltage switching technique," in *Proc. 11th Int. Conf. Optimization of Electrical and Electronic Equipment*, May 2008.
- [32] K. Martin, A. Vázquez, M. Arias and J. Sebastián, "A very simple analog control for QSW-ZVS source/sink buck converter with seamless mode transition," 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL), Padua, 2018, pp. 1-6.
- [33] S. Chen, O. Trescases, and W. T. Ng, "Fast dead-time locked loops for a high-efficiency microprocessor-load ZVS-QSW DC/DC converter," in *Proc. IEEE Conf. Electron Devices and Solid-State Circuits*, Dec. 2003, pp. 391-394.
- [34] D. Costinett, D. Maksimovic, and R. Zane, "Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 985-995, Feb. 2015.
- [35] Sable, David Mark, "Optimization of spacecraft battery charger/discharger systems," Ph.D. dissertation, Virginia Tech. University, Virginia, 1991. [Online]: <https://vtechworks.lib.vt.edu/handle/10919/39782>. Last time accessed: 05/13/2019.
- [36] B. Su, J. Zhang and Z. Lu, "Totem-Pole Boost Bridgeless PFC Rectifier With Simple Zero-Current Detection and Full-Range ZVS Operating at the Boundary of DCM/CCM," in *IEEE Transactions on Power Electronics*, vol. 26, no. 2, pp. 427-435, Feb. 2011.
- [37] Z. Liu, Z. Huang, F. C. Lee, Q. Li and Y. Yang, "Operation analysis of digital control based MHz totem-pole PFC with GaN device," 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Blacksburg, VA, 2015, pp. 281-286.

- [38] R.W. Erickson and D. Maksimovic, "Fundamentals of Power Electronics," Chapter 9, "9.5 Regulator Design", Eds. New York: Kluwer Academic Publishers, 2001, pp-347-354.
- [39] On Semiconductor, "DC-DC Converters Feedback and Control," [Online]: <https://www.onsemi.com/pub/Collateral/TND352-D.PDF>. Last accessed: May 2019.
- [40] On Semiconductor, "AND8143/D: General Approach for Optimizing Dynamic Response for Buck Converter," Appl. Note AND8143/D. Jan. 2011. [Online]: <https://www.onsemi.com/pub/Collateral/AND8143-D.PDF>. Last accessed: May 2019.
- [41] Texas Instruments, "Demystifying Type II and Type III Compensators Using OpAmp and OTA for DC/DC Converters," Appl. Note SLVA662. Jul. 2014. [Online]: <http://www.ti.com/lit/an/slva662/slva662.pdf>. Last accessed: May 2019.
- [42] Asahi Kasei, "CQ-3200 High-speed response coreless current sensor datasheet," Asahi Kasei, Datasheet, 2016.