Universidad de Oviedo
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DOCTORAL THESIS

Advanced Power-electronic Converters Based-on GaN Semiconductors

presented by:

Ander Avila Del Pozo

Supervised by:

Dr. Alberto Rodriguez Alonso (Universidad de Oviedo)

Dr. Asier Garcia Bediaga (IKERLAN)

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TESIS DOCTORAL

Convertidores Avanzados de Potencia Basados en Semiconductores de GaN

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Eskerrik asko danori,
Muchas gracias a todos,
Many thanks to all,

Ander

</div>

Abstract

Research on power electronics has significantly grown, mainly due to worldwide interest in sustainable energy and electrification of traction systems. Moreover, as energy transport and conversion systems evolve and advance, power electronics becomes also more complex. Hence, although power converters based on Silicon (Si) present a good balance between performance and cost, along with high reliability and maturity, the limits in terms of power density, operation temperature, and switching frequency of Si power devices are close to being reached. Then, advanced power converter topologies and new semiconductors, especially based on Wide-bandgap (WBG) materials, tend to develop higher efficiency and higher power density solutions. Regarding WBG devices, Silicon Carbide (SiC) and Gallium Nitride (GaN) are the most promising power switches due to a higher switching frequency capability than Si-based devices, among other benefits.

Advantages of using WBG devices on current applications are mainly focused on the development of high-frequency power converters, reducing the size and improving the efficiency. While SiC devices have already been put into practice for high power applications, the trend of GaN devices has been moved from radio frequency power amplifiers and microwave solutions to power applications with higher voltage requirements ($> 200\,\mathrm{V}$) in recent years. The interest of GaN-based transistors is mainly associated with the high electron mobility layer, also known as the two-dimensional electron gas (2DEG). This structure provides a low condition losses and high-switching capability.

However, GaN devices present specific challenges related to their implementation on power electronics. Differential characteristics related to conduction, high-switching speed capability, gate requirements, and thermal cooling are some of the main design challenges. Therefore, spe-

cial attention must be devoted to these design considerations in order to take full advantage of GaN semiconductors. Besides, there is a need to establish the benefits and limitations of these power devices. It is expected that GaN will be primarily a potential alternative for medium power solutions (in the 200-600 V range), medium/high frequency and particularly in medium/high-end applications. The main objective of this thesis is to answer questions regarding the use of GaN devices and define optimal design considerations. Hence, the thesis presents a comprehensive analysis of differential characteristics, that define the design considerations and challenges. Minimum dead-time and gate driver requirements are defined. Gate driver is designed to achieve high switching speed but without exceeding gate limitations of GaN devices.

Afterwards, the thermal limits of current GaN devices are evaluated. An analysis based on the use of heat-spreading materials and parallelization of various devices is presented, increasing the thermal cooling capability. In addition, detailed analysis of hard- and soft-switching operation, is included, defining the most suitable operation modes. Besides, the converter performance is evaluated and experimentally validated, analyzing the impact of working with high-switching frequency. This analysis includes single-cell and multi-cell topologies, defining the sustainability of implementing then with GaN devices. The study carried out in this thesis is organized into six different chapters, evaluating from differential characteristics and challenges of GaN devices, until its benefits and limitations on developing GaN-based power converters.

Resumen

Debido al reciente interés en las energías renovables y la electrificación
de los medios de transporte, la relevancia de los sistemas de conversión
ha incrementado en los últimos años. La mayoría de los convertidores de
potencia construidos hasta la fecha están basados en silicio (Si) presen-
tando unas buenas prestaciones en cuanto a rendimiento y coste, junto
con una alta fiabilidad debido a la madurez de la tecnología. No ob-
stante, a medida que estas aplicaciones evolucionan y avanzan, la elec-
trónica de potencia se vuelve más compleja y los límites en términos de
densidad de potencia, temperatura de operación y frecuencia de trabajo
del Si están a punto de ser alcanzados. Por lo tanto, es necesario el de-
sarrollo de nuevos convertidores de potencia y nuevos semiconductores
basados en materiales novedosos, como los de banda ancha prohibida
(WBG), para desarrollar soluciones de una mayor eficiencia y densidad
de potencia. En el contexto de semiconductores WBG, el carburo de
silicio (SiC) y el nitruro de galio (GaN) se sitúan actualmente cómo los
materiales más prometedores, siendo capaces de trabajar a una mayor
frecuencia entre otros beneficios. Las ventajas de trabajar con semi-
conductores WBG resulta en aplicaciones que son capaces de trabajar
a mayores frecuencias de conmutación, reduciendo el tamaño y mante-
niendo altas eficiencias. Mientras que ya se han demostrado algunos de
los beneficios de implementar SiC en aplicaciones de media-alta poten-
cia, la aplicación del GaN comenzó a darse en amplificadores de radio
frecuencia y soluciones microondas. Recientemente se está empezando
a implementar en electrónica de potencia. Uno de los mayores intereses
del GaN está relacionado con su canal de alta movilidad, también cono-
cido como gas bidimensional de electrones (2DEG). Las características
de este canal permiten reducir las pérdidas tanto en conducción como
en conmutación.

Sin embargo, el uso de los componentes de GaN en electrónica de potencia supone unos retos. La mayoría de estos están relacionados con las características diferenciales de estos componentes, en comparación con los dispositivos de Si. La alta velocidad de conmutación, los requerimientos por puerta y la disipación de las pérdidas serían unos de los mayores retos a la hora de diseñar convertidores basados en GaN. Al tratarse de una tecnología novedosa, existe la necesidad de establecer los beneficios y limitaciones de esta. Se espera que el GaN se convierta en una solución alternativa para las aplicaciones de media potencia, media/alta frecuencia y aplicaciones de altas prestaciones.

Con todo esto, el objetivo principal de esta tesis es responder a las incógnitas relacionadas al uso de los semiconductores de GaN, definiendo para ello las consideraciones de diseño a tener en cuenta. En este trabajo se presenta por lo tanto un análisis exhaustivo de las características de los semiconductores basados en GaN, se definen los retos y se proponen soluciones para aprovechar al máximo estos dispositivos. Entre otras cosas, se define el tiempo muerto mínimo y el diseño del ataque de puerta sin exceder los límites del dispositivo. Se evalúan también los límites térmicos de la tecnología. Para ello, se analiza el uso de materiales de alta conductividad térmica, mejorando así la capacidad de disipación térmica de los componentes de GaN. Se realiza también una evaluación detallada de los semiconductores en diferentes modos de operación. Se analiza la distribución de pérdidas trabajando en conmutación dura, es decir contemplando tanto perdidas de conmutación en el encendido como en el apagado. Asimismo, se considera un sistema operando con conmutaciones dulces, es decir sin perdidas de encendido. Gracias a este análisis se definen los modos de operación óptimos de los convertidores basados en GaN.

Además del análisis detallado del rendimiento de los semiconductores, también se realiza un análisis a nivel convertidor. Para ello se define un método de optimización que determina el diseño óptimo en base a la eficiencia y densidad de potencia del sistema completo. Una vez se define la metodología de análisis, esta se aplica a diferentes topologías con el fin de definir la potencialidad del GaN en convertidores con una sola celda y multicelda. Este análisis es validado experimentalmente. El estudio que se realiza en este trabajo se presenta en seis diferentes capítulos en los que se evalúan desde las características diferenciales y retos del GaN, hasta su aplicabilidad en la electrónica de potencia.

Resume

A cuenta del interés reciente nes enerxíes renovables y la lletrificación
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tamañu y manteniendo eficiencies altes. Mentes que yá se demostraren
dalgunos de los beneficios d'implementar SiC n'aplicaciones de poten-
cia media-alto, l'aplicación del GaN empezó a dase na microondas y
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tiques diferenciales d'estos componentes, en comparanza colos dispositivos de Si. L'alta velocidá de conmutación, los requerimientos per puerta y la disipación de les pérdides sedríen unos de los retos mayores a la hora de diseñar convertidores basaos en GaN. Al tratase d'una tecnoloxía novedosa, existe la necesidá d'afitar los beneficios y llimitaciones d'esta. Espérase que'l GaN se vuelva una solución alternativa pa les aplicaciones de media potencia, media/alta frecuencia y aplicaciones de prestaciones altes.

Con too esto, l'oxetivu principales d'esta tesis ye responder a les incógnites rellacionaes al usu de los semiconductores de GaN, definiendo pa ello les consideraciones de diseñu a tener en cuenta. Nesti trabayu preséntase polo tanto un análisis al detalle de les característiques de los semiconductores basaos en GaN, defínense los retos y propónense soluciones p'aprovechar al máximu estos dispositivos. Ente otres coses, defínese'l tiempu muertu mínimu y el diseñu del ataque de puerta ensin pasar los llímites del dispositivu. Evalúense tamién los llímites técnicos de la tecnoloxía. Pa ello, analízase l'usu de materiales de conductividá térmica alto, ameyorando asina la capacidá de disipación térmica de los componentes de GaN. Faise tamién una evaluacón detallada de los semiconductores en maneres estremaes d'operación. Analízase la distribución de pérdides trabayando en conmutación duro, ye dicir, contemplando mesmo les pérdides de prendíu que d'apagáu. Asinamesmo, considérase un sistema operando con conmutaciones dulces, ye dicir, ensin pérdides de prendíu. Gracies a esti análisis defínense les maneres óptimes d'operación de los convertidores basaos en GaN.

Amás del análisis detalláu del rendimientu de los semiconductores, tamién se fai un análisis a nivel convertidor. Pa ello defínese un métodu d'optimización que marca'l diseñu óptimu en base a la eficiencia y densidá de potencia del sistema completu. Una y buena se define la metodoloxía d'análisis, esta aplícase a topoloxíes diferentes cola fin de definir la potencialdiá del GaN en convertidores con una celda sola y multicelda. Esti análisis ye validáu de forma esperimental. L'estudiu que se fai nesti trabayu preséntase en seis capítulos estremaos nos que s'evalúen dende les característiques diferenciales y retos del GaN, hasta la so aplicabilidá na electrónica de potencia.

Contents

Chapter 1

Introduction: From Silicon to Wideband-Gap Materials

POWER ELECTRONICS plays a key role in the evolution and advances of many different applications. Besides, Power electronics has been evolved, making significant contributions on the recent technological growth. For example, the electrification of traction systems or the generation-storage-distribution cycle of the electric energy are carried out by power electronic converters. The main objective of these converters is to transform the energy into useful electricity. Besides, with increasingly worldwide interest in sustainable energy with reduced impact on environment the research related to improve power electronics performance has significantly grown. Moreover, the energy consumption in electrical form results on lower environmental pollution [1]. However, from generation to end-user application, conversion of energy results on power losses.

Therefore, the trend of power converters development calls for higher efficiency, higher power density, and higher reliability, all while providing a lower overall system cost [2]. On the one hand, a great contribution of these goals will be made by advanced power converter topologies, which enables the extension of the operation frequency range, and thus, increases power density. It is a well-known fact that the increase of operation frequency usually reduces the volume of magnetic elements,

something already put into practice in low-power applications thanks to
the availability of fast and efficient semiconductors. Otherwise, this fact
is becoming a reality in high-power applications due to new Wideband-
Gap (WBG) semiconductors with better performance [3–5] and the de-
velopment of new magnetic materials with higher magnetic saturation
and lower loss densities [6]. Therefore, the development of converters
based-on new materials will be essential for near future developments.

In this context, this first chapter presents the current state and
future trends of power electronics. Then, with the aim of improving
power conversion systems based on new semiconductor materials, the
motivation and main objectives of this work are summarized. Finally,
the outline of the thesis is introduced, highlighting the most relevant
content of each chapter.

1.1   The Global Picture

Power electronics appears in most of the fields of our life, as it is depicted
in Figure 1.1. Beginning with consumer electronics, power electronics
can be found in power appliances, such as induction cooking, personal
computers, battery chargers, etc. Regarding industry, almost all the
motors employed are controlled by power drives. Moreover, renewable
energy generation systems require from power electronics, in order to
adapt the energy into usable electricity. The produced renewable energy
grows in last decade, up to 18% of the total generated energy [7].

Furthermore, referring to electro-mobility, remarkable advances
have been achieved in recent years. However, the number electric vehi-
cles is far from representing, being less than 1% of the market share [8].
There are still some technological barriers, such as limited driving range
or long battery charging times, that limit the competitiveness of these
solutions [9]. The development of even higher energy density batter-
ies [10] and innovative solutions for battery charging systems [9, 11],
are some of current ongoing research topics, so as to accelerate the
transition from traditional combustion vehicles to electric mobility.

Thus, the rapid growth of applications requires from more efficient,
compact and cost effective Switching Mode Power Supplies (SMPS)
[12, 13]. In this section, the evolution of power converters and the per-
formance of semiconductors is described, defining the trend of power
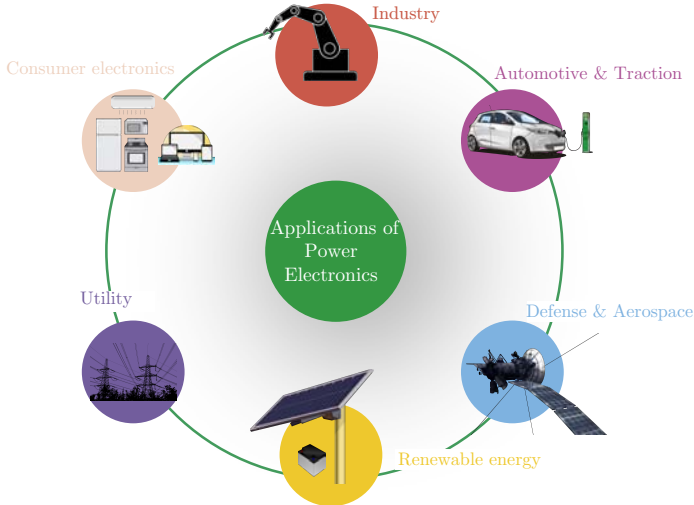electronics in recent years.

Figure 1.1: Power electronics irruption on last decades.

1.1.1 Power converters evolution

The performance of power converters is mainly associated to power losses, weight, volume, cost or failure rate. Analyzing the evolution of commercial SMPS, there is a clear tendency on continuous improving power converter overall performance [14]. Considering Photovoltaic (PV) inverters for residential applications, the produced power losses are reduced by a factor of 2 every 10 years as it is presented in [15]. Moreover, regarding the cost evolution of power systems in automotive and traction, an overall cost reduction of 10% per year is expected [8]. In addition, the size of power supplies has also been reduced by a factor of 10 every 20 years [15, 16].

The enhancement of power electronic converters is mainly enabled by the performance improvement of power electronic components. The power electronics converters evolution demonstrates that semiconductors led this change [15]. In addition, new power converter topologies are also improving power converters performance, achieving ultra-high efficiencies [17, 18]. However, many novel topologies are based on standard topologies, but with higher system complexity.

1.1.2 Performance of semiconductors

Power switching devices based on Sillicon (Si) have dominated the market of SMPS in the last decades. The main reasons are a good balance between performance and cost and a high reliability and maturity of the Si technology. Nevertheless, Si shows some limitations related to its operating temperature, voltage blocking capability and switching frequency. Consequently, there is a need to develop new generation power semiconductors in order to overcome limitations of Si technology. The use of WBG power switches promises to break current Si-based switches performance limits [4, 5, 19]. In addition, the interest of industry and academia in new semiconductors based on WBG materials has considerable increased in the last decade, especially for high-performance converters or in applications with strict requirements.

In this context, WBG materials, such as Sillicon Carbide (SiC), Gallium Nitride (GaN) or diamond show superior properties [3]. SiC and GaN are currently the two most promising WBG devices, mainly due to current availability and development stage of semiconductors [4]. Figure 1.2 shows a comparison of material properties. The main benefits of these characteristics applied to power devices in comparison with Si-based counterparts are summarized below:

(a)

(b)

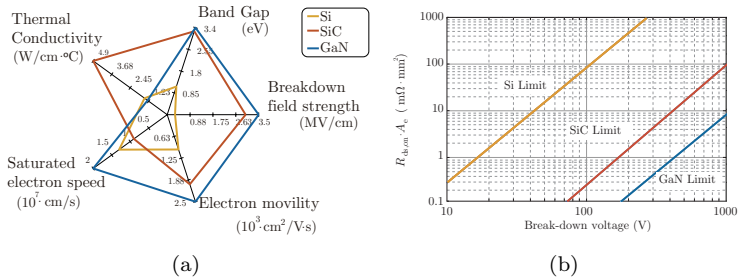**Figure 1.2:** Comparison of Si, SiC and GaN material properties: (a) generic characteristics comparison and (b) conduction resistance $R_{ds,on}$ per area A_e.

▶ *Thermal conductivity.* WBG semiconductors present higher thermal conductivity and a higher melting point, with the exception of GaN. These properties involve a higher temperature operation levels keeping electrical characteristics with a slightly variation of

forward reverse characteristics. Hence, SiC devices are suitable for extreme conditions where Si based converters cannot work.

▶ *Electric field and energy gap.* Higher electric field and a higher energy gap of WBG semiconductors results on higher breakdown voltage and a higher doping level. Thus, a thinner material is needed to achieve the same blocking voltage as blocked by Si. Then, it produces lower conduction losses because of the reduction of the on-resistance [see Figure 1.2(b)].

▶ *Saturation electron drift velocity.* These devices can operate at higher switching frequency with lower switching losses.

Then, WBG allows to operate at high-switching frequency, high-voltage and high-temperature, improving the performance of conversion systems. Consequently, these materials are game-changing power electronics. Figure 1.3 shows a general view of the map of application os each technology [20, 21], considering already published devices. Si
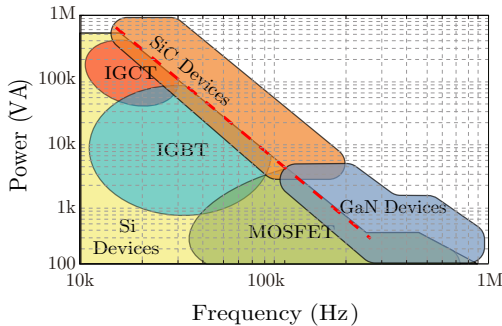
Figure 1.3: Power *versus* frequency map of current power switches technologies application.

devices (IGCT, IGBT, MOSFET, Sujer-Junction) are used for different power and frequency ranges limited by Si physical limits, as it is depicted in Figure 1.3 with dashed lines. However, SiC semiconductors are expected to cover high-voltage ($\geq 650\,\text{V}$) applications owing to the availability of good quality bulk substrates and good thermal properties of the material [4]. SiC semiconductors have already been demonstrated to improve the performance of power converters at medium-high voltage

range [22–26]. It has been demonstrated that for railway applications, the use of SiC devices achieves a total size reduction of the 30% [25].

On the contrary, experts do not expect that GaN devices will be so competitive in high-power/high-voltage levels [4, 20, 21]. Although GaN material high-frequency and high-voltage characteristics, the lack of good quality bulk substrates limits the blocking voltage. Moreover, it is attributable to the lateral structure of current available devices and packaging techniques [27], among other characteristics. The lateral structure ensures a low conduction resistance $R_{\mathrm{ds,on}}$ but limits the breakdown voltage capability of current devices [28]. The implementation of a GaN based devices on a vertical structure will result on a better blocking voltage capability [28, 29], but it is in a too early development stage and it will not be analyzed in this work.

Therefore, current available GaN devices are presented as competitive a solution to overcome the Si limits in low ($<200\,\mathrm{V}$) and medium-high voltage ($\leq 650\,\mathrm{V}$) applications. There has been an increasing industrial interest in GaN devices in the last decade [20, 30, 31]. Furthermore, GaN technology has been improving fast, primarily because of light-emitting diodes manufacturing, and now due to the development of power semiconductors [31].

1.2   GaN Devices in Power Electronics

The trend of GaN devices implementation has been move from microwave solutions [32, 33] to power applications with higher voltage requirements ($> 200\,\mathrm{V}$). As is depicted in Figure 1.4, GaN devices with a higher breakdown voltage than $200\,\mathrm{V}$ were not available until recent years. *International Rectifier* (IR) announced the first commercial GaN-on-Si power device in 2010 with a breakdown voltage of 7 - 13.2 V and an output current of 30 A [34]. This announcement was quickly followed by *EPC* ($200\,\mathrm{V}/12\,\mathrm{A}$) [35]. Currently, there are more than ten semiconductors companies providing GaN power devices, as a result of a great research. The research has been focused mainly on the development of the GaN-on-Si transistor.

As the GaN based devices for power conversion applications is significantly growing, the manufacturers of these devices are anticipating changes, in order to dominate GaN power devices market. This can be seen in recent news and projects of those industrial companies.
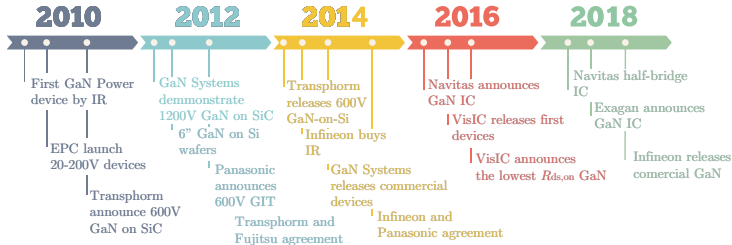
Figure 1.4: Milestones in GaN power electronics development since in 2010 the first GaN power device was announced.

► The acquisition of *IR* by *Infineon* (January 2015) [36].

► The license agreements between *Infineon* and *Panasonic* (March 2015) [37].

► The license agreements between *Transphorm* and *Furukawa* (May 2014) [38].

► The will of several firms to move onto the mass production stage (*Transphorm/Fujitsu*) [39].

► More than 1,960 worldwide patented inventions related to GaN for power electronic applications up to April 2015 and more than 200 patent applicants [40].

► *Infineon* impulse European projects: HipoSwitch [41], PowerBase (2015-2018) [42] and UltimateGaN (2019-2022) [43].

► *Analog Devices* Acquires *Linear Technology* (March 2017).

Furthermore, GaN high-switching capability supposes design challenges, such as the reduction of stray inductance [44], among others. Most of current GaN devices are available with a low stray inductance package [20]. Otherwise, the use of these optimized and small packages can be a challenge when designing the cooling system. Therefore, some of the most challenging design aspects when implementing GaN devices are listed below. Moreover, an overview of ongoing academy research and potential applications of current GaN semiconductors are presented.

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1.2.1 Main challenges

Due to the particularities GaN devices, it is important to identify the specific challenges of designing GaN based power converters. Although there are many aspects to consider in the design of a GaN based power converter, this work summarizes the most relevant ones that affect to the design of GaN-based power converters. These design challenges are focused on differential characteristics of GaN in comparison with more commonly used Si semiconductors.

Gate characteristics

The gate driver is the circuit that is connected to the gate of the semi-conductor in order to control its turn-on/turn-off. There are many commercially available gate driver boards for Si devices but almost all of them are not suitable for GaN due to unique characteristics of the gate [45, 46]. For that reason, it is relevant to identify the needs of GaN so as to control it in an optimal way.

Reverse conduction

Although GaN transistors perform significantly better by most metrics compared to their silicon equivalents, the "body diode" forward voltage is higher than for Si counterpart and can be a major contributor to power losses during dead-time. For this reason, it is very important to choose a right value of dead-time so that looses could be minimized [47]. Therefore, the high self-commutated reverse conduction losses have to be considered since it can be a major factor in a GaN-based power converter design, depending on the reverse conduction period.

Dynamic $R_{\mathrm{ds,on}}$

Dynamic $R_{\mathrm{ds,on}}$, also known as "current collapse", is a phenomenon whereby the drain current decreases as a consequence of electron trapping at surface states near the gate edge. Those electrons are trapped due to the unevenly distributed electric field causing a reduction of conduction channel density after the device turns-on. In addition, there is an undesirable memory effect caused by the polarization of the heterojunction [27]. That effect increases proportionally to the blocking voltage, as has been demonstrated in [48, 49]. Additionally, the "hot

electron effect" from switching causes more electron trapping, penetrating deeper traps at impurities in lower layers and causing long-term degradation [48].

Indeed, GaN manufacturers such as *EPC*, *Panasonic*, *Transphorm* and *Infineon* have announced that they are working on reducing the effect of this issue [31,50]. However, it is important to be aware that this issue still exists even if it has been significantly reduced. It mainly has some effect on modeling and losses analysis at MHz switching range [49].

High di/dt and dv/dt effects

The very short switching time for GaN devices results on high di/dt and dv/dt that have to be considered, due to the induced voltage. These induced voltages can generate an overvoltage that will lead to a dielectric breakdown if the rated output voltage or the rated gate voltage is exceeded [27]. Therefore, as a result of the high-frequency operation of GaN based power converters, the layout has to be carefully considered reducing every loop formed by the layout connections [51]. Since the common source inductance of the package is reduced by the novel packaging technologies, the dominating parasitic is the commutation inductance of the Printed Circuit Board (PCB) layout. Hence, the layout of the converter determines the performance of the overall conversion systems.

In [52], parasitic inductances and capacitors influence is analyzed for a GaN based half-bridge module. Some layout recommendations are also included in [51] and the effects of PCB layout in GaN based power converters are analyzed in [44]. The results of these layouts are experimentally analyzed achieving reduced layout stray inductances ($<2\,\mathrm{nH}$) .

Thermal cooling

The thermal conduction and dissipation of these devices are key features in order to obtain their electrical advantages and ensure long lifetime. Furthermore, cooling down GaN devices is a challenging task due to the small area of the heat source [53]. The package and the thermal pad of these switching devices are relatively small, being challenging to extract all the heat from devices without exceeding the maximum junction temperature in high-power applications [54].

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Therefore, specially attention must be devoted in the design of the cooling system in order to take full-advantage of these devices benefits.

1.2.2 Academy research

Figure 1.5 presents some of the most relevant GaN-based power converter prototypes found in the literature. These converters are classified considering the operation mode and the number of devices. When analyzing the implementation trends of GaN devices, two tendencies are identified. On the one hand, soft-switching operation mode is used to work at high-switching frequency (200 kHz - 1 MHz) for output power levels around 2 kW. Topologies with soft-switching capability such as Dual Active Bridge (DAB) [55], LLC resonant dc-dc [56], Totem-pole [57] or full-bridge [58] are selected to achieve high-frequency. This working conditions reduce the power converter overall size as in [56, 59, 60], achieving high power density (> 5 kW/l).
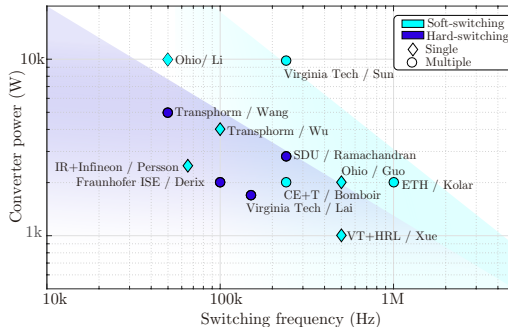

Figure 1.5: Power *vs.* frequency map of GaN-based power converter prototypes proposed in literature.

On the other hand, for the implementation of GaN devices on higher power applications (> 2 kW), multiple devices connected in parallel [61, 62] or various interleaved converters [59, 60, 63–65] are used, most of them in soft-switching operation. Although multiple devices and soft-switching mode are the most common operation conditions, [66] presents a compact inverter based on a single GaN device and a hard-switching operation mode. However, the dead-time selection ensures soft-switching operation mode, reducing power losses at full-load conditions.

Regarding high-efficiency and high-power density converters, in September 2014 *Google* and *IEEE* launched the "Little Box Challenge" (LBC). This was a worldwide competition to build the world smallest 2 kW single-phase solar-inverter in order to push the forefront of power density in today's converter systems further [67]. Analyzing the converters of the finalist, 73% of the converters were based on GaN devices achieving outstanding efficiencies with a reduced size [67]. The winner power converter (CE+T) was also based on GaN devices, achieving a high efficiency (>97%) in a compact size (8.85 kW/l) [68].

The presented works help to identify some of the potential applications of GaN devices. However, even if the prototypes presents two tendencies for the implementation of GaN devices, the impact on the power converter performance of using GaN devices for power electronics is not clear.

1.2.3 Potential applications

The benefits of using WBG devices has already been proven in automotive converters [55, 69]. Furthermore, high efficiencies are achieved in applications, such as induction power transfer systems [70] or photovoltaic applications [71].

The next stage in the development of GaN based power converters will be the consolidation of this technology as a final solution. Indeed, the application is not defined yet, but there is a high expectation for the implementation of GaN in many applications. Considering that GaN is still under development, there are not many commercialized applications based on GaN semiconductors found in the literature. Furthermore, the low availability and especially the high cost and reliability concerns of these components in comparison with its counterparts make difficult the inclusion in the actual market [72]. The application diversity will vary depending on the future evolution of GaN devices. Currently it will be difficult to incorporate GaN devices into wind energy and rail traction applications [30]. It is expected that GaN will be primarily a potential alternative for medium power solutions (in the 200-600 V range), medium/high frequency and particularly in medium/high-end applications [20]. Therefore, until the cost of GaN semiconductors decreases and reliability concerns improve, the range of potential applications is defined for medium/high-end applications [72].

In addition, recent works have shown benefits of using GaN on three

main sectors of these application ranges: consumer electronics, small
dc/dc, wireless chargers, Power Factor Correction (PFC) and power
supplies; power generation, PV inverters and micro-inverters, and trans-
port, Plug-in Hybrid Electric Vehicles/Electric Vehicle (PHEV/EV).
Hence, different application areas where GaN devices will improve
power converters performance beyond state of the art solutions. Three
main application areas are identified: consumer electronics, power gen-
eration and transport.

Consumer Electronics

For instance, *CORSAIR* (supplier of high-performance PCs products
for the gaming community) establishes a new class of ac/dc GaN
(*Transphorm*) based Power Supply Unit (PSU). By the use of a bridge-
less totem-pole PFC, the company has achieved an efficiency of 99%.
According to designers: 'GaN increases the PSU's characteristics com-
pared with its Si Super-junction equivalent MOSFET' [73]. The power
output is increased by 6.5% in an 11% smaller package, all this at the
same temperature value [73].

In addition, *Navitas Semiconductor* has announced that *GaN Fast™*
power devices enable the *'Mu One'*. An universal 45 W power adapter
with an unprecedented ultra-slim profile [74]. Therefore, the potential-
ity of GaN for consumer electronics has already been demonstrated.

(a)   (b)

Figure 1.6: GaN based commercial solutions: (a) *CORSAIR*'s new
AX1600i power supply unit PSU with 1600 W [73] and (b) a GaN 45W
power adapter with an unprecedented 14 mm ultra-slim profile by *Navi-
tas* [74].

Power Generation

Renewable energy sources, including hydro-power, wind power, PV, etc., are increasing in the global electricity generation share. Among those, especially PV energy has been in the focus of many countries, such as China or India, resulting in a steep rise in the numbers of installations [75]. Furthermore, the recent advance in WBG semiconductors is showing a great impact on the PV converters. These conversion systems are mainly influenced by the efficiency and the power density, bearing in mind the cost [76]. That is why WBG semiconductors appears as an attractive alternative to current Si-based PV inverters. In addition, there are several research works in the literature showing the advantages of GaN [77–80] and SiC [81] based PV inverters.

There are already some companies developing WBG-based solar inverters that will be available soon. Solar inverter manufacturers claimed to different WBG devices. Some of them like *Mitsubishi* and *Omron* have recently show PV inverter prototypes based on SiC [82]. Otherwise, *Yaskawa* announced the first GaN based power inverter [83]. Although SiC is currently in a more mature stage; GaN could displace SiC as a result of a better price expectation [83].

Besides, there is an increasingly interest on developing PV micro-inverters and module-integrated converters based on GaN semiconductors [84–86].

Transport

The current electrical powertrains for transport applications are being served by Si based IGBTs. Nevertheless, it is expected that 1200 V and 1700 V will be the most commonly used voltage levels [87], opening the possibility to use SiC devices. In addition, it is expected that PHEV/EV will be a key application for GaN market [20,30,87], in spite of the limited blocking voltage capability of current available GaN devices. For that purpose, there is a need to establish the efficiency improvements and reliability concerns of actual GaN devices. Although there are wide different transport applications, PHEV/EV will be the most potential one as it is analyzed in [87].

The implementation of power converters based on this kind of semiconductors will lead to following benefits [72]:

▶ The development of high-frequency chargers, reducing the size and improving the efficiency by the use of GaN and SiC devices

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[55, 88]

► The development high-efficiency and small-size power converters.
As a result of better performance offered by SiC devices, electric
or hybrid powertrains for cars, aircrafts, ships, buses, etc. will
be implemented soon. Instead, it is not expected to use GaN for
that area until devices with higher blocking voltage capability are
developed.

In addition, with the ground breaking progress indicated by recent
success in passing *JEDEC* qualification of 600 V rated GaN transistors [89], reliability can now be assessed to justify the suitability of GaN
for the stringent automotive applications. Besides, *DELTA* has developed a high-efficiency and compact GaN-based 3.3 kW charger with an
efficiency better than 95% and a reduction of the volume by 30% [90].

Thus, the advantages of the future of using GaN and SiC on transportation electrification systems are clear. That is why several car
manufactures have already been making researches in order to make
their mind between GaN and SiC technology.

Japanese automakers are currently using a variety of substrate materials, including SiC, to work on power models in the 1200 V and may
be pushing beyond it. For example, *Nissan* claimed to have developed
world's first inverter using SiC diode for vehicle use in September 2008,
and implemented in the *XTRAIL FCV* (Fuel cell Vehicle). *Mitsubishi*
is actively pursuing SiC technology research and development for their
PHEV/EVs, and *Honda/ROHM* appears poised to bring a SiC power
module to the market. These automakers are currently using a variety
of substrate materials, including SiC, to work on power modules in the
1200 V range and may be pushing beyond it [72].

Nevertheless, other companies such as *Toyota* or *Ford* are pursuing
GaN as an alternative to Si. It is possible, though no evidence was
found to confirm, that *Toyota* is developing a breakthrough technology
which would allow cost-competitive production of GaN devices [72].

Ford Motor Company presented its vision on the potential application of GaN power devices in their next-generation electrified vehicles [91]:

*'Although the mismatch between GaN and Si lattices creates significant difficulties in epitaxial film growth, the promise of GaN performance at a cost comparable to silicon counterparts makes it a primary
candidate of interest for the PHEV/EV application. We recognize the*

superior material properties of GaN and its suitability as power switching transistors.'

Lateral GaN power devices are expected to exhibit excellent performance in medium range power modules [87, 92]. Thus, for some manufacturers, GaN has the best potential as the post Si power device among current available semiconductor materials [93, 94].

1.3 Motivation and Objectives

Based on the uncertainties and the challenges of implementing this technology on power electronics, the aim of this thesis is to answer the questions regarding the use of GaN devices. Therefore, a comprehensive analysis, evaluation and validation of GaN-based power converters is presented. These results are verified by simulations or/and experimental measurements for different applications. Therefore, the main objectives of the thesis are given in the following:

- ▶ Understand the *differential characteristics of GaN devices* in comparison to Si/SiC counterparts, defining challenges and design considerations

- ▶ Define the *gate circuit design*, along with a *dead-time control strategy*, without exceeding gate specifications of GaN devices.

- ▶ *A*nalyze of hard- and soft-switching operation modes, including the losses of incomplete soft-switching transitions.

- ▶ *Thermal limits improvement* based on heat-spreading materials and parallelization of various devices.

- ▶ Propose a *general power losses model and experimental measurement method* for GaN devices, achieving a good agreement between theoretical and experimetnal results for diffeent operating conditions.

- ▶ Define the most *optimal converter design* for GaN semiconductors, evaluating the whole performance of the power converter.

- ▶ Evaluate the *potentiality of GaN devices* in detail for various applications. This analysis includes single-cell and multi-cell topologies, defining the sustainability of implementing then with GaN devices.

1.4   Outline of the Thesis

The main goal of this thesis is to provide the reader with an understanding of deferential characteristics of novel GaN devices and its implementation in power electronics. Within this introductory chapter, the state of the art of power electronics and WBG devices have been summarized, introducing the benefits and challenges of GaN devices. Besides, the works presented in academia have been listed, analyzing the main research topics related to GaN devices. Although GaN devices are on an early development stage, potential applications are presented. Then, once the background of the topic has been described, the motivation and objectives of this thesis have been presented, which are further analyzed in following chapters.

The first part of Chapter 2 presents GaN devices characteristics in comparison to commonly used Si and SiC power switches. Analytical, simulation and data-sheet characteristics are used in order to describe the benefits and limitations of GaN devices. In this manner, the most critical design aspects are identified and more deeply analyzed during this Chapter 2. Considering these distinctive aspects, different analytical models are proposed to deal with: dead-time selection, gate driver design, switching losses (hard- and soft-switching), and thermal management. Even if GaN devices presents low power losses with high switching speed capability, it is essential to define the optimal operating conditions. In addition, the use of heat-spreading materials as a media to improve GaN devices thermal capability is analyzed, along with the parallelization of various devices.

In Chapter 3, the analysis presented in previous chapter is evaluated and experimentally validated. Gate driver designs are presented, achieving a proper gate driving performance. Moreover, dead-time control strategy relevance is presented, along with a symmetrical gate driver circuit for parallel-connected devices. Regarding thermal management, different cooling configurations are evaluated, i.e. top and bottom side cooling. The benefits of paralleling devices and heat-spreading materials are demonstrated and validated on experimental prototypes. In addition, power losses distribution is analyzed, providing a power losses model for different operating conditions. This model is evaluated for a well known synchronous buck converter, working at different operation modes. Then, the performance of GaN devices operating at different switching frequency, current ripple and number of

devices in parallel is evaluated. Furthermore, the power losses model is validated through experimental measurements. A steady-state calorimetric method is described, measuring the temperature difference of the heatsink.

Then, the most suitable operating conditions for GaN devices are defined. However, it is not clear the benefits of operating at these operating conditions for every component that conform a power converter. Therefore, Chapter 4 analyzes the benefits and limitations of working with high-performance GaN devices at converter level. Indeed, the losses or/and volume impact of these devices for the previously defined design space is evaluated. Moreover, a design optimization routine based on these models (introduced in this chapter and detailed in Appendix A) and power losses model of semiconductors presented in Chapter 3 is proposed. Hence, the optimal design based on GaN devices can be defined in terms of efficiency and power density.

This motivates Chapter 5, where the optimal design based on GaN devices is analyzed for different topologies. Hence, the use of GaN devices for single-cell and multi-cell configurations is validated in a case study. Besides, the power losses model is validated along with the analysis presented during this work. Hardware prototype presented in previous chapters are used to validate the presented analysis.

Finally, in Chapter 6, the main conclusions of this thesis are summarized, highlighting the main contributions. Furthermore, future works related to the presented work are pointed out.

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Chapter 2

GaN Semiconductors Technology

An effective utilization of GaN devices requires a good understanding of their characteristics and differential aspects. This knowledge is essential also to identify the most relevant benefits and limitations of GaN devices in comparison with its Si/SiC counterparts. For that purpose, this chapter first introduces GaN devices in Section 2.1. Properties of different structures are summarized, based on current available devices [31].

Then, in Section 2.2, differential static and dynamic characteristics are evaluated in comparison with Si and SiC semiconductors. Conduction and switching characteristics are analyzed, along with the properties of gate and thermal cooling capability. The performance of GaN devices is analyzed through analytical model and SPICE simulations. SPICE models have been proven to achieve a good agreement with experimental measurements, when analyzing devices performance [95,96]. As it will be shown, dead-time selection, switching losses distribution, driver requirements and thermal management play a key role when analyzing the performance of GaN devices.

Section 2.3 analyzes the minimum dead-time selection in order to reduce losses related to dead-time instances. Afterwards, in Section 2.4 the power losses distribution is defined to evaluate the switching losses relevance. Data-sheet characteristics are considered along with Double Pulse Test (DPT) to analyze the switching energy. Moreover, an analyt-

ical model to estimate soft-switching losses is proposed in Section 3.4.2. Section 2.5 analyzes the impact of gate driver characteristics on the design of the driver. An analysis of gate voltage safety margin and false turn-on is carried out, defining design recommendations for a suitable operation. In addition, considering the small size of GaN devices, the thermal capability is limited. Therefore, the impact of increasing the thermal dissipation area with heat-spreading materials is evaluated in Section 2.6.

Finally, Section 2.7 concludes with a summary of the main relevant characteristics analyzed in this chapter, along with the most important conclusions.

2.1 GaN Devices

The characteristics of GaN devices have made a great progress, due to the advance of device structures and GaN material quality. By contrast, GaN power devices are still in a non-mature stage. There are already commercialized GaN based power semiconductors (see Section 1.2). However, as there are not free-standing GaN substrates, GaN epilayers have been mainly grown on foreign substrates like Si, SiC or sapphire. GaN epilayers grown on Si substrates are presented as a low cost and mature technique [97]. For this reason GaN-on-Si devices will be the most competitive solution in the near future with an expectation to match prices of Si [97, 98].

GaN devices are grown on a lateral structure achieving a low conduction resistance. Figure 2.1 shows the most typical GaN structure with the main three contacts: Source, Gate and Drain. These devices are developed on a lateral structure formed by different layers. A thick undoped GaN layer is grown on the foreign substrate (Si, SiC or sapphire). On the top of that GaN layer, a high-conductivity Aluminium Gallium Nitride (AlGaN) layer is built. This AlGaN/GaN based heterostructure was first demonstrated by *Khan et al.* in 1993 [99]. At the interface between GaN and AlGaN layers, a Two Dimensional Electron Gas (2DEG) appears. That is generated by the conduction band discontinuity between AlGaN and GaN. This feature results on a very high electron carrier mobility (1200–2000 cm^2/Vs) with a low conduction resistance, making GaN High-Electron-Mobility Transistor (HEMT) a promising device for power conversion applications.

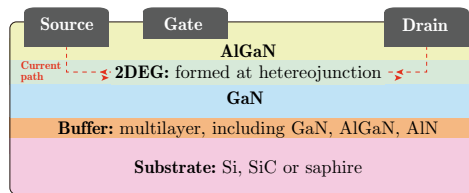The interest of GaN-based transistors is mainly associated with the

Figure 2.1: GaN HEMT lateral structure, differing between different material layers which conform the hetereojunction.

high electron mobility layer 2DEG obtained at the interface between Al-GaN and GaN epilayers, forming the HEMT structure. Consequently, such transistors are "naturally" normally-on devices, also known as depletion mode devices. However, the use of depletion mode semiconductors increase the complexity of power converters due to reliability concerns. Then, great research efforts have been put in recent years on developing normally-off structures. Several approaches related to mechanisms that provide a default 2DEG layer interruption have been proposed, acting on the gate [31]. A way to fabricate a normally-off device is to inject negative charges into AlGaN layer in order to generate some holes bellow the gate and lift the threshold voltage to a positive value.

There are three main methods presented in the literature to fabricate normally-off HEMTs [4,27]: non-insulated gate, insulated gate and cascode. The major limitation of cascode structure is the lack of direct control of the GaN devices switching behaviour. Thus, in this work, non-insulated and insulated gate structures are analyzed.

2.1.1 Non-insulated gate

The first commercially available power GaN device was the *EPC* eGaN FET [35]. For this device a p-doped GaN cap is deposited below the gate, making the gate threshold voltage positive. This treatment leads to a diode-like gate characteristic with a positive gate current when the voltage between the gate and the source is above the threshold [31].

Furthermore, *Panasonic* presented GaN based normally-off devices with a similar deposition of a p-doped cap beneath the gate. Nevertheless, in this case *Panasonic* Gate Injection Transistor (GIT) use Al-

GaN [100]. These structures require a constant driver current consumption. Besides, *Infineon* and *Panasonic* made an agreement in order to develop similar structure, known as CoolGaN for *Infineon* devices [37].

2.1.2 Insulated gate

Other manufacturers developed normally-off architectures with insulated gates to reduce gate current and losses. This architecture consists on putting an insulating/oxide cap between the gate and the AlGaN layer. These devices are also known as MOSHFETs or MISHFETs due to the oxide insulator cap [31]. *HRL Laboratories* has used CF4 plasma treatment to deplete the 2DEG cap under the gate when the gate to source voltage is below a positive threshold. Then, a gate insulator is placed under the gate to prevent significant gate current [101].

In addition, *GaN Systems* also developed normally-off insulated gate GaN based power devices [27]. However, there are not technical publications found about the used treatment to achieve normally-off operation.

2.2 Characterization of Devices

Currently available GaN devices can be divided into two voltage ranges: "medium-low" (100 - 200 V) and "medium-high" ($\geqslant$650 V). In the "medium-low" voltage range GaN devices are competing with Si MOSFETs, while in the "medium-high" Si Super-junction and SiC MOSFETs present similar characteristics. In this case only 650 V GaN devices are considered in the "medium-high" voltage range, as the 900 V switches are on an early development stage [102]. For a general comparison of current available devices, four performance indicators are defined: conduction resistance ($R_{ds,on}$) per current (mΩ·A), output capacitor charge (Q_{oss}) per $R_{ds,on}$ (μC· mΩ), gate charge Q_G per $R_{ds,on}$ (nC·$m\Omega$), and junction-to-case thermal resistance ($R_{th_{j-c}}$) per area (℃/W· mm^2).

Regarding conduction characteristic, GaN presents lower conduction resistance per current over the whole voltage range. However, on the "medium-high" voltage range the difference between three technologies is lower, achieving similar conduction characteristic, as it is depicted in Figure 2.2(a). In terms of Q_{oss}, analyzed GaN devices also overcome its counterparts as a consequence of lower output capacitance C_{oss}. Q_{oss} is a relevant parameter, along with reverse recovery charges Q_{rr}, when determining switching losses. Hence, low Q_{oss} of GaN devices results
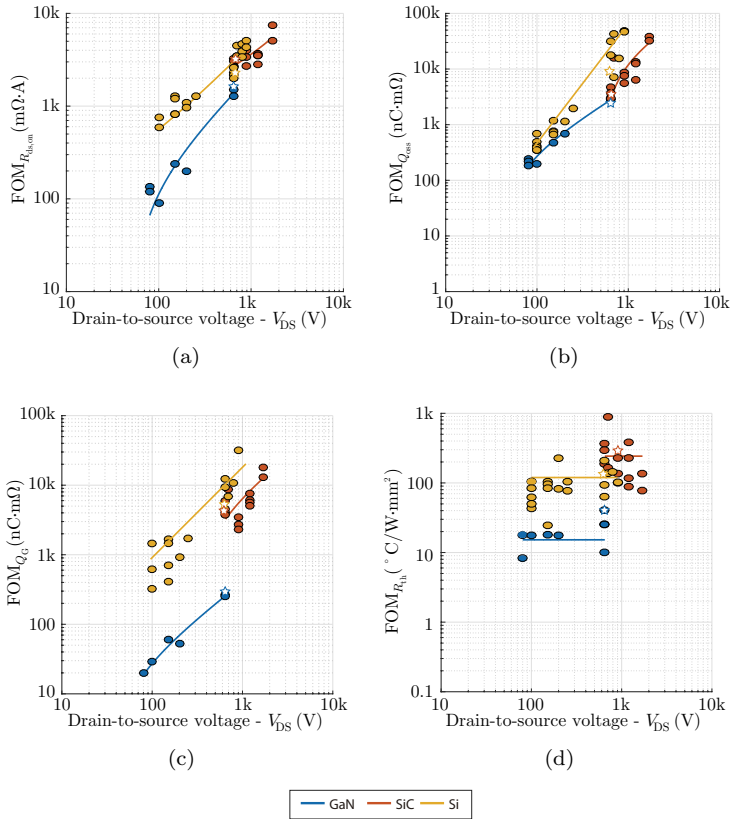
Figure 2.2: GaN characteristics comparison with its Si/SiC counterparts based on four performance indicators: (a) conduction characteristic per current, (b) output capacitor charge per conduction resistance (c) gate charge per conduction resistance and (d) thermal cooling capability per area.

on an improvement of switching performance. Furthermore, one of the most distinctive characteristics comparing three devices technologies is related to the gate charge. Gate charge requirement of GaN devices is lower, enabling high switching operation with low gate driver requirements.

The thermal performance of devices is compared with a thermal figure of merit (FOM_{th}), assuming that the device can be effectively

cooled through one side [53].

$$\text{FOM}_{\text{th}} = R_{\text{th}_{j-c}} \cdot A_{\text{e}} \tag{2.1}$$

where A_{e} is the thermal pad area also known as effective area.

The cooling capability of GaN devices is lower than for Si or SiC, as a consequence of a reduced size and a worse thermal characteristic (see Figure 1.2(a)). Moreover, the thermal characteristic of GaN material is also worse comparing to Si and even worse than SiC (see Figure 1.2). Although the small size results in compactness solutions, the package limits the heat transfer capability, being challenging to extract the heat from such small packages. Considering this cooling limitation, thermal cooling capability is evaluated in Section 2.6. Besides, the use of heat-spreading materials in order to improve thermal cooling capability is proposed.

The analysis of this chapter will be focused on "medium-high" semiconductors, as the benefits and limitations of "low-medium" devices have been widely discussed in the literature [53, 103–105]. Table 3.1 compares three semiconductors based on different technologies for similar specifications (400 V/15 A). Analyzed devices present similar conduction resistance, but GaN shows up better switching performance, with lower Q_{oss} and negligible Q_{rr}. However, the main limitation of GaN device is related to the thermal cooling capability.

Table 2.1: Electrical and thermal characteristics of GaN devices.

Parameter	Si [106]	SiC [107]	GaN [108]	
Drain-to-source maximum voltage-V_{DS}	650	900	600	V
Drain-to-source maximum current-I_{DS}	33	39	35	A
Conduction resistance-$R_{\text{ds,on}}$@25 °C	65	78	**55**	$m\Omega$
Free-wheeling resistance-$R_{\text{ds,FWD}}$@25 °C	84	83	75	$m\Omega$
Free-wheeling voltage drop-V_{SD}	**0.6**	1.3	1.5	V
Output capacitor charge-Q_{oss}@400V	470	55	**41**	nC
Reverse recovery charge-Q_{rr}@400V	10	0.055	**0**	μC
Gate-to-source maximum voltage-V_{GS}	10	18	4	V
Gate-to-source threshold-V_{th}	3.5	4.5	1.4	V
Gate charge-Q_{G}	64	58	**5.8**	nC
Thermal performance-FOM$_{\text{th}}$	155.4	**193.71**	43.8	$mm^2 \cdot °C/W$

Therefore, the characteristics presented in Figure 2.2 and Table 3.1

highlights the benefits and limitations of GaN devices. However, a more detailed analysis is needed in order to identify how to take full advantage of GaN-based devices. Then, conduction, switching and gate driver characteristics are analyzed, highlighting differential characteristics that need to be considered in comparison with commonly used devices, i.e. Si and SiC.

2.2.1 Conduction characteristics

GaN devices heterojunction structure HEMT does not have a doping or p-n junction, as it occurs for MOSFETs [4]. Instead, GaN devices present a self-commutated forward and reverse conduction due to the 2DEG channel. Indeed, symmetrical bi-directional conduction resistance is achieved when the gate-to-source voltage (V_{GS}) exceeds the threshold voltage (V_{th}). Moreover, when device is in open-state, i.e. V_{GS} is lower than V_{th}, GaN HEMT structure allows a free-wheeling conduction with negligible Q_{rr}. Conduction tests are simulated using SPICE models, for different operation conditions. Then the on-state and free-wheeling conduction characteristics are obtained for the analyzed GaN switches IGO60R070D1 [108].

Fordward and reverse conduction

Conduction characteristic is depicted in Figure 2.3(a), showing the high impact of the turn-on gate voltage $V_{GS,on}$ on output characteristic. Hence, an optimal $V_{GS,on}$ has to be selected in order to reduce conduction losses. Moreover, the conduction resistance $R_{ds,on}$ presents a low variation respect to devices current I_d and a positive thermal coefficient (see Figure 2.3). This means that the resistance increases with temperature. Thus, in case of paralleling devices, the positive thermal coefficient enables a natural balancing of current sharing through devices.

Conduction resistance relation with T_j is approximated with a second order polynomial, achieving a good agreement for different currents [see Figure 2.3(b)].

$$R_{ds,on}(T_j) = R_{ds}@25°C \cdot (a_{R,on} + b_{R,on} \cdot T_j + c_{R,on} \cdot T_j^2). \qquad (2.2)$$
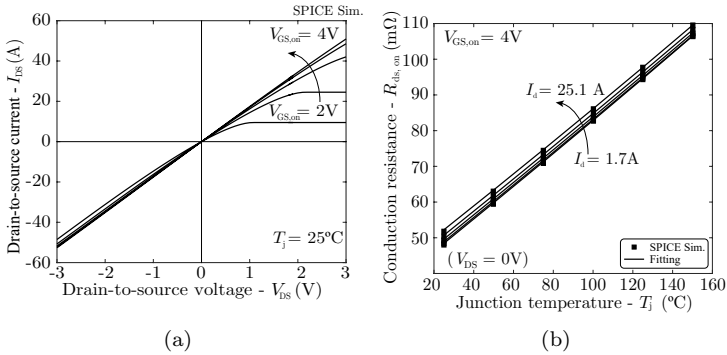
Figure 2.3: Fordward and reverse conduction characteristic of GaN devices: (a) Output characteristic and (b) conduction resistance variation respect to T_j and I_d.

Free-wheeling conduction

However, free-wheeling reverse conduction of GaN devices ($V_{GS,off} \leq 0\,V$) presents a high reverse voltage drop (V_{SD}) [Figure 2.4(a)]. The lack of a "body diode" results on a higher V_{SD}, increasing free-wheeling conduction losses. The relevance of these losses can be higher than in a conventional Si/SiC devices, as it is compared in Table 3.1. Moreover, with negative $V_{GS,off}$ reverse voltage drop increases, as it is presented in Figure 2.4(a).

The increase of the total voltage drop can be approximated with (2.3).

$$V_{SD} = V_{th} - V_{GS,off} + I_d \cdot R_{ds,FWD} \tag{2.3}$$

Regarding the free-wheeling conduction resistance $R_{ds,fwd}$, it also presents a positive thermal coefficient, as it is shown in Figure 2.4(b). $R_{ds,fwd}$ can be also approximated with (2.2). In comparison with $R_{ds,on}$, $R_{ds,fwd}$ is larger. Furthermore, free-wheeling conduction presents a high voltage drop [see Figure 2.4(b)]. Although V_{SD} decreases with the increase of T_j, the junction temperature affects weakly to the V_{SD} variation.

Therefore, free-wheeling conduction losses have to be considered when designing a GaN-based power converter, since it can be a major factor on total power losses. In Section 2.3 the minimum dead-time selection is modeled, in order to minimize this effect.
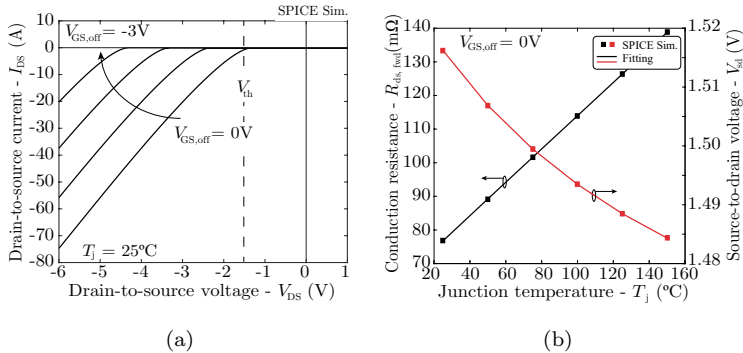
Figure 2.4: Free-wheeling (open-state) conduction characteristic: (a) Output characteristic with respect to different $V_{\text{GS,off}}$ and (b) $R_{\text{ds,fwd}}$ and V_{SD} variation with respect to T_{j}.

2.2.2   Switching characteristics

The equivalent circuit of a power switch is analyzed for the understanding of differential switching characteristics of GaN semiconductors. The equivalent circuit of the semiconductor is formed by an input gate resistor R_{G}, parasitic capacitances (C_{GS}, C_{GD} and C_{DS}) and parasitic inductances related to the package (see Figure 2.5). Although there is not a "body diode", GaN devices structure allows free-wheeling conduction, represented with a dashed lined diode in Figure 2.5. Besides, the channel current $i_{\text{ch}}(t)$ through the device is proportional to the gate to source voltage $v_{\text{GS}}(t)$ (2.4), which is represented with a regulated current source in Figure 2.5.

$$i_{\text{ch}}(t) = g_{\text{m}} \cdot (v_{\text{GS}}(t) - V_{\text{th}}) \tag{2.4}$$

being g_{m} the transconductance characteristic.

Transconductance

The transconductance of GaN devices present negative thermal coefficient, i.e. transconductance drops with the increase of T_{j}, as it is shown in Figure 2.6. For Si/SiC MOSFETs the variation of the transconductance with the temperature is negligible [109].The transconductance
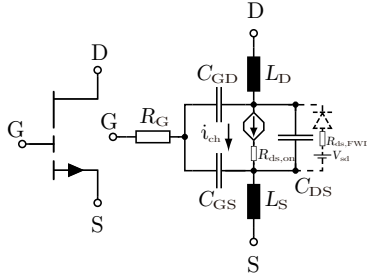
Figure 2.5: Equivalent semiconductor circuit of GaN devices.

variation $g_\mathrm{m}(T_\mathrm{j})$ can be obtained with a linear approximation

$$g_\mathrm{m}(Tj) = a_\mathrm{gm} \cdot T_\mathrm{j} + b_\mathrm{gm} \cdot T_\mathrm{j}. \tag{2.5}$$
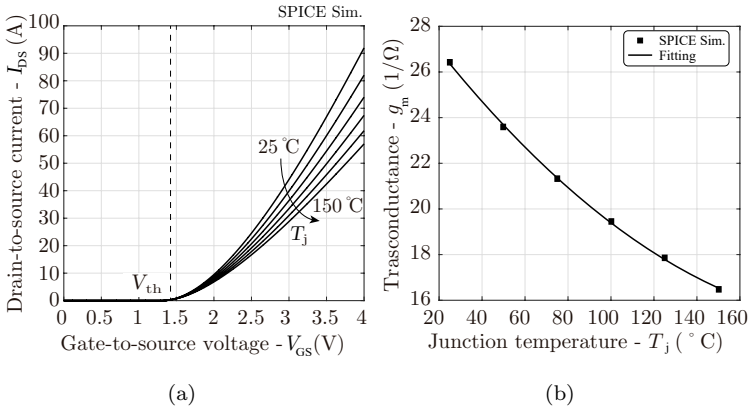
Figure 2.6: SPICE simulation results of the effect of junction temperature on: (a) transfer characteristic and (b) transconductance.

The variation of transconductance can be relevant when calculating switching losses of GaN devices [31]. Therefore, temperature variation is considered in the analysis of switching losses distribution presented in Section 3.4.1.

Parasitic capacitances

Analyzing equivalent circuit components, parasitic capacitors are commonly presented in three different groups of capacitances: input capacitance ($C_{\mathrm{iss}} = C_{\mathrm{GS}} + C_{\mathrm{GD}}$), output capacitance ($C_{\mathrm{oss}} = C_{\mathrm{DS}} + C_{\mathrm{GD}}$) and reverse transfer capacitance ($C_{\mathrm{rss}} = C_{\mathrm{GD}}$). They exhibit a non-linear dependency on the applied drain-to-source voltage V_{DS}, as it is depicted in Figure 2.7(a). C_{oss} and C_{rss} capacitances decrease as V_{DS} increases, having a weak variation at high voltage ($>300\,\mathrm{V}$).

As a consequence of this non-linearity, the charge and energy stored in parasitic capacitances exhibit also a non-linearity with respect to V_{DS}. On the one hand, for the modeling of the charge stored in C_{oss} (V_{DS}), a linear equivalent capacitance $C_{\mathrm{eq,Q}}$ which presents the same charge as C_{oss} for the applied V_{DS} is derived, as it is proposed in [110]

$$C_{\mathrm{eq,Q}}(V_{\mathrm{DS}}) = \frac{\int_0^{V_{\mathrm{DS}}} C_{\mathrm{oss}}(v_{\mathrm{D}})\mathrm{d}v_{\mathrm{D}}}{V_{\mathrm{DS}}} = \frac{Q_{\mathrm{oss}}(V_{\mathrm{DS}})}{V_{\mathrm{DS}}}. \tag{2.6}$$

On the other hand, the energy stored in the non-linear C_{oss} (V_{DS}) can be approximated in a similar way. The equivalent capacitance which stores the same amount of energy $C_{\mathrm{eq,E}}$ is obtained solving (2.7)

$$C_{\mathrm{eq,E}}(V_{\mathrm{DS}}) = 2 \cdot \frac{\int_0^{V_{\mathrm{DS}}} v_{\mathrm{D}} \cdot C_{\mathrm{oss}}(v_{\mathrm{D}})\mathrm{d}v_{\mathrm{D}}}{V_{\mathrm{DS}}^2} = \frac{2 \cdot E_{\mathrm{oss}}(V_{\mathrm{DS}})}{V_{\mathrm{DS}}^2} \tag{2.7}$$

GaN devices present low equivalent capacitances [see Figure 2.7(b)] due to lower variation of the output capacitance in comparison with Si/SiC counterparts.

In addition, it should be noted that C_{iss} presents a weak change with respect to V_{DS}. However, C_{iss} has a nonlinear relation with the gate to source voltage. The C_{iss}-V_{GS} relation can be obtained from total gate charge curves depicted in Figure 2.7(c) and solving (2.8).

$$C_{\mathrm{iss}} = \frac{dQ_{\mathrm{G}}}{dv_{\mathrm{gs}}} = \begin{cases} C_{\mathrm{iss1}}@[v_{\mathrm{gs}} \leq V_{\mathrm{plt}}] \\[2mm] C_{\mathrm{iss2}}@[v_{\mathrm{gs}} > V_{\mathrm{plt}}] \end{cases} \tag{2.8}$$

where V_{plt} is the gate-to-source plateau voltage.
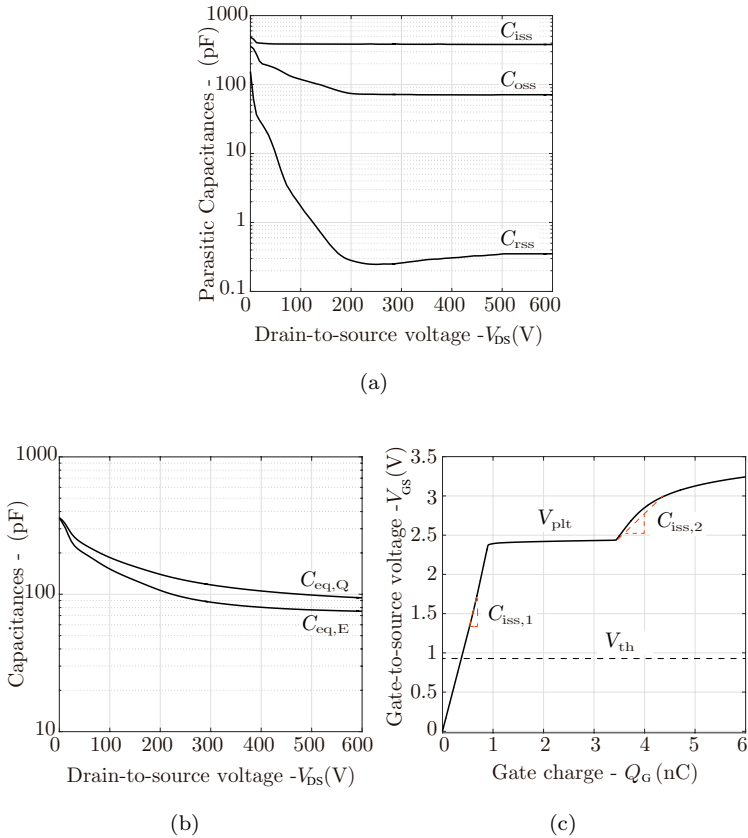
(a)

(b)

(c)

Figure 2.7: Switching characteristics of GaN devices, obtained from datasheet [108] and SPICE models: (a) parasitic capacitances voltage dependence, (b) equivalent output capacitor charge and equivalent output capacitor energy, and (c) total gate charge characteristic.

2.2.3 Gate characteristics

Considering the low gate charge characteristic of GaN devices [see Figure 2.2(c)], a rapid gate to source voltage transition is expected. Moreover, the Miller plateau voltage is low, as it is depicted in Figure 2.7(c), being possible to achieve high slew rate (about 20V/ns [111]). The gate capacitance C_{GS} is much lower for GaN devices resulting in a higher

switching speed capability. Furthermore, a high Miller capacitance C_{GD} in comparison with a relatively small gate capacitance C_{GS} supposes a better control of the switching transition due to a direct control of the Miller charge [45, 46].

Considering again similar characteristic Si/SiC counterparts, GaN device presents lower Q_G, with a lower V_{th} and V_{plt} (see Table 3.1). Then, the switching speed is evaluated, which is limited by the charge of Miller capacitance Q_{GD} and the charging current I_g. Minimum switching times are obtained without considering external gate resistance

$$t_{on,min} = \frac{R_G \cdot Q_{GD}}{V_{GS,on} - V_{plt}}$$

$$t_{off,min} = \frac{R_G \cdot Q_{GD}}{V_{plt} - V_{GS,off}}$$

(2.9)

where maximum turn-on gate voltage $V_{GS,on}$ and minimum turn-off gate voltage $V_{GS,off}$ and plateau voltage V_{plt} limit the switching times.

It has to be noted, when comparing switching times of different technologies, that the analyzed SiC devices present large internal gate resistance. GaN device achieves 4.5 times faster switching time than SiC and 2.12 times faster than Si Table 2.2. However, switching without an external gate resistance results in gate oscillations, exceeding in some cases maximum gate voltage, as it is presented in Figure 2.8. In addition, GaN devices present low transconductance [see Figure 2.6]. This means that in order to avoid high conduction losses at high currents, the gate should be driven close to the specified maximum value, i.e. 3.5-7 V depending on the selected device.

In addition, Figure 2.8 shows a SPICE simulation of a half-bridge structure, driving GaN devices without external gate resistances. Half-bridge structure is selected as one of the most commonly implemented configuration. As a consequence of high switching speed (di/dt) a voltage is generated in the complementary switch ($V_{GS,s2}$), resulting in in false turn-on (see Figure 2.8). Hence, the selection of a proper gate resistance and gate voltage is crucial for GaN devices performance. Therefore, although GaN devices present better conduction and switching characteristics than other semiconductor technologies, the gate driver circuit must be designed with special care, as it is presented in Section 2.5.

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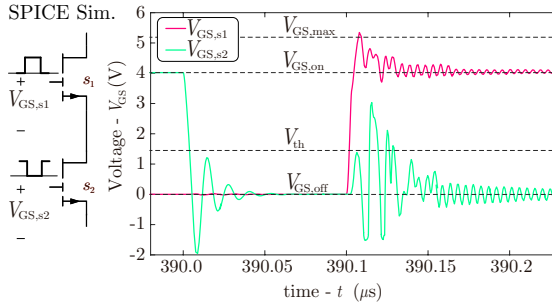
Figure 2.8: SPICE simulation of gate-to-source voltages of high-side (s_1) and low side (s_2) switches when turning-on s_1 switch without external gate resistance.

In addition, driver requirements are related to the energy delivered when charging/discharging of the input capacitance C_{iss}

$$Q_{\text{G}}(v_{\text{gs}}) = \int_{V_{\text{GS,off}}}^{V_{\text{GS,on}}} C_{\text{iss}}(v_{\text{gs}})dv_{\text{gs}} \tag{2.10}$$

Then, the required driver power is related to the gate charge $Q_{\text{G}}(v_{\text{gs}})$ resulting in (2.11).

$$P_{\text{drv}} = \underbrace{\Delta V_{\text{GS}} \cdot Q_{\text{G}}(v_{\text{gs}})}_{E_{\text{drv}}} \cdot f_s$$

$$\text{where} \quad \Delta V_{\text{GS}} = V_{\text{GS,on}} - V_{\text{GS,off}} \tag{2.11}$$

In Table 2.2, gate driver energy of Si, SiC and GaN devices are compared. GaN switches with low Q_{G} results in 19.4 times less gate driving energy compared to Si and 25.4 times compared to SiC. Therefore, losses related to driver can be neglected even for high-switching frequencies, being one of the most differential benefits when comparing to Si/SiC counterparts.

2.3 Dead-time Selection

Considering GaN devices free-wheeling conduction characteristic (see Figure 2.4), an excessive dead-time results on considerably relevant

Table 2.2: Driving energies comparison

Characteristics	Si [106]	SiC [107]	GaN [108]	
Internal resistance	0.85	2.2	0.78	Ω
Gate charge	64 nC	58 nC	5.8	nC
Turn-on/turn-off gate voltage	18/0	20/-2	4/-2	V
Turn-on/turn-off times (without resistance)	2.39/1.49	5.15/3.18	1.13/0.73	ns
Driving energy E_{drv}:	0.97	1.27	0.05	μJ

power losses. Then, the definition of the minimum dead-time that ensures an operation without shoot-through will be essential for converters with half-bridge configuration based on two active GaN switches (see Figure 2.9). For the selection of the dead-time, turn-on and turn-off dead-times are separately analyzed, as the loss mechanism of both transients is different. Minimum dead-times are obtained based on the analytical switching process model presented in [112], but considering gate driver rising and falling times along with the influence of turn-on and turn-off gate-to-source voltages. It is further assumed an ideal PCB layout, with low effect of stray inductances in order to simplify the analysis.

Furthermore, a half-bridge configuration is assumed, with a positive output current as it is depicted in Figure 2.9.

2.3.1   Turn-off dead-time

The turn-off dead-time is obtained from the mismatch between main device (s_1) turn-off interval ($t_{\text{off},1}$) and synchronous device (s_2) turn-on ($t_{\text{on},2}$) interval [see Figure 2.9(a)].

Regarding $t_{\text{off},1}$, $V_{\text{GS,off}}$ is applied to the main switch, the input capacitance C_{iss} is being discharged through gate resistance $R_{\text{g,off}}$.

$$v_{\text{GS,s1}}(t) = V_{\text{GS,off}} + (V_{\text{GS,on}} - V_{\text{GS,off}}) \cdot e^{-\frac{t}{C_{\text{iss}} R_{\text{g,off}}}} \tag{2.12}$$

(a)

(b)
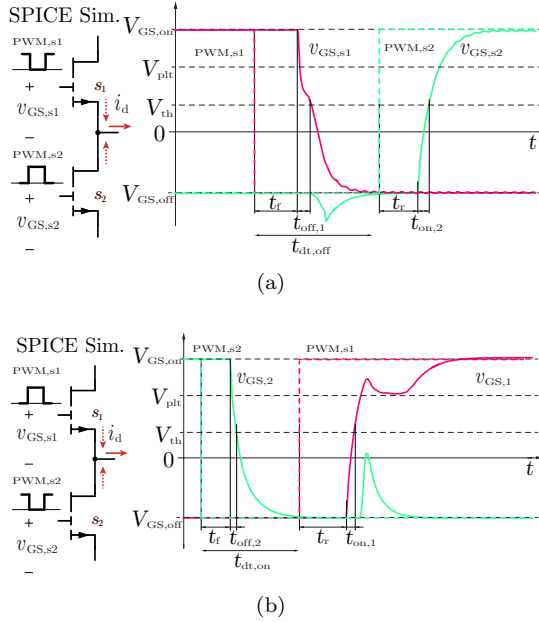
Figure 2.9: Dead-time conduction instances definition: (a) turn-off dead-time and (b) turn-on dead-time.

$t_{\text{off},1}$ is obtained, solving (2.12) for $v_{\text{GS,s1}}(t) = V_{\text{th}} + I_{\text{d}}/g_{\text{m}}$

$$
t_{\text{off},1} = R_{\text{g,on}} \cdot C_{\text{iss}} \cdot \left[\ln \left(\frac{V_{\text{GS,off}} \cdot g_{\text{m}} - V_{\text{th}} \cdot g_{\text{m}} - I_{\text{d}}}{g_{\text{m}} \cdot (V_{\text{th}} - V_{\text{GS,off}})} \right) \right.
$$
$$
\left. - \ln \left(\frac{g_{\text{m}} \cdot (V_{\text{GS,on}} - V_{\text{th}})}{V_{\text{GS,off}} \cdot g_{\text{m}} - V_{\text{th}} \cdot g_{\text{m}} - I_{\text{d}}} \right) \right] \tag{2.13}
$$

being dependent on device current I_{d} because the current is flowing through synchronous device in that instance.

In addition, $t_{\text{on},2}$ is calculated for the gate circuit, applying $V_{\text{GS,on}}$ to the gate, charging C_{iss} through gate resistance $R_{\text{g,on}}$

$$
v_{\text{GS,s2}}(t) = V_{\text{GS,on}} + (V_{\text{GS,off}} - V_{\text{GS,on}}) \cdot e^{-\frac{t}{C_{\text{iss}} R_{\text{g,on}}}} \tag{2.14}
$$

and thus solving it for $v_{\mathrm{gs,s2}}(t){=}V_{\mathrm{th}}$ considering gate driver falling time

$$t_{\mathrm{on,2}} = R_{\mathrm{g,on}} \cdot C_{\mathrm{iss}} \cdot \ln \left(\frac{V_{\mathrm{GS,on}} - V_{\mathrm{GS,off}}}{V_{\mathrm{GS,on}} - V_{\mathrm{th}}} \right) \tag{2.15}$$

The minimum turn-off dead-time is obtained to be only related to gate characteristics of GaN device and gate driver specifications, such as gate driver rising t_{r} and falling t_{f} propagation delays, as it can be deduced from Figure 2.9(a).

$$t_{\mathrm{dt,off}} = t_{\mathrm{off,1}} + t_{\mathrm{f}} - 2 \cdot t_{\mathrm{on,2}} - t_{\mathrm{r}} \cdot \frac{V_{\mathrm{th}}}{V_{\mathrm{GS,on}}} \tag{2.16}$$

where t_{r} is adapted considering longer t_{r} than $t_{\mathrm{on,2}}$ [113].

2.3.2 Turn-on dead-time

The minimum turn-on dead-time compensates main device turn-on ($t_{\mathrm{on,1}}$) and synchronous device turn-off ($t_{\mathrm{off,2}}$) intervals.

Assuming that the characteristics of main and synchronous devices are the same, turn-on and turn-off delay intervals are obtained in the same way that in the case of turn-off dead-time. However, both intervals finish when $v_{\mathrm{GS}}(t)$ gets V_{th}. This is true because the current that is flowing through the device that is turning-off is negative [see s_2 in Figure 2.9(b)]. Therefore, $t_{\mathrm{on,1}}$ and $t_{\mathrm{off,2}}$ can be obtained solving (2.15) to obtain $t_{\mathrm{on,1}}$ and (2.12) for $v_{\mathrm{gs}}(t) = V_{\mathrm{th}}$

$$t_{\mathrm{off,2}} = R_{\mathrm{g,off}} \cdot C_{\mathrm{iss}} \cdot \ln \left(\frac{V_{\mathrm{GS,on}} - V_{\mathrm{GS,off}}}{V_{\mathrm{th}} - V_{\mathrm{GS,off}}} \right). \tag{2.17}$$

being $t_{\mathrm{off,2}}$ independent on the device current, as the current is flowing trough the free-wheeling diode of the synchronous device.

Then, minimum turn-on dead-time is obtained considering both intervals and gate driver characteristics

$$t_{\mathrm{dt,on}} = t_{\mathrm{off,2}} + t_{\mathrm{f}} - 2 \cdot t_{\mathrm{on,1}} - t_{\mathrm{r}} \cdot \frac{V_{\mathrm{th}}}{V_{\mathrm{GS,on}}} \tag{2.18}$$

This model will be used to determine the minimum dead-time for different devices and driver characteristics of the prototypes presented in Section 3.2.

2.4 Switching Losses Distribution

The distribution of switching losses is relevant for the evaluation of the most suitable operation conditions. Turn-on energy E_{on} is obtained by the integrating of $v_{\text{d}}(t) \cdot i_{\text{d}}(t)$ over turn-on period. However, charging/discharging energy of the complementary device is not considered on this integration, but it produces losses on the turn-on transition [114]. Hence, the measured E_{on} has to be corrected to

$$E_{\text{on}} = E_{\text{vi,on}} + E_{\text{oss}} + \frac{1}{2} \cdot C_{\text{eq,Q}}(V_{\text{d}}) \cdot V_{\text{d}}^2 \qquad (2.19)$$

where $E_{\text{vi,off}}$ corresponds to the voltage and current overlapping energy and E_{oss} is the output capacitance self-charging losses.

Regarding turn-off switching losses, the amount of energy obtained from the integration of $v_{\text{d}}(t) \cdot i_{\text{d}}(t)$ includes: voltage and current overlapping energy $[E_{\text{vi,off}}(V_{\text{d}}, I_{\text{off}})]$ and E_{oss}. Nevertheless, as the device is turned-off and does not produce self-charging losses. Thus, $E_{\text{vi,off}}$ only contributes to turn-off losses and the expression has to be revised to

$$E_{\text{off}} = E_{\text{vi,off}} - \frac{1}{2} \cdot C_{\text{eq,Q}}(V_{\text{d}}) \cdot V_{\text{d}}^2 \qquad (2.20)$$

The obtained, turn-on and turn-off energies are corrected for the switching energy distribution obtained with (2.19) and (2.20), respectively (see Figure 2.10). Therefore, turn-on losses of GaN devices are related to the overlapping of $v_{\text{d}}(t)$ and switching current $i_{\text{d}}(t)$ $[E_{\text{vi}}(V_{\text{d}}, I_{\text{on}})]$ during t_{on}, and output capacitance self charging/discharging $[E_{\text{oss}}(V_{\text{d}})]$, which are only dependent on switching voltage V_{d} (see Figure 2.10). Besides, turn-off energy is only related to $v_{\text{d}}(t)$ and $i_{\text{d}}(t)$ overlapping during t_{off} $[E_{\text{vi}}(V_{\text{d}}, I_{\text{off}})]$.

When analyzing switching energy, a great difference between turn-on and turn-off energy is observed in Figure 2.10. This switching losses distribution will be essential for the power losses analysis presented in next chapters.

2.5 Driver Requirements

Dynamic of gate characteristics are analyzed, as a consequence of the gate characteristics presented in Section 2.2.3. When analyzing the
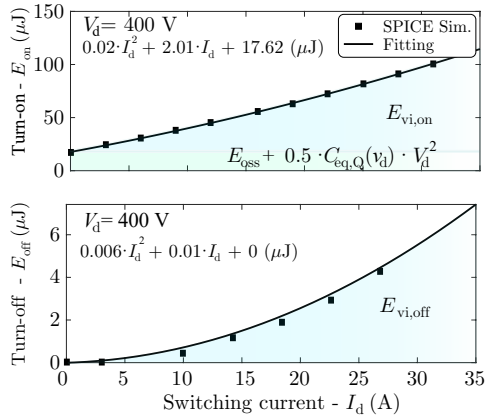
Figure 2.10: Switching energy distribution of analyzed GaN devices IGO60R070D1- [108].

dynamic of GaN devices special attention must be paid to the voltage safety factor ($\frac{V_{GS,max}}{V_{GS}}$) and the low gate threshold voltage, that can result on unwanted turn-on. Moreover, current controlled driver design is analyzed due to diode-like gate characteristic that presents non-insulated gate GaN devices [37].

2.5.1 Voltage safety factor

The gate to source voltage safety factor ($\frac{V_{GS,max}}{V_{GS}}$) of GaN ($<1.3$) is even lower than in SiC switches (<1.7) [115]. Then, attention must be devoted to the selection of a proper gate driver circuit components. The gate resonant circuit formed at the turn-on (see Figure 2.11) is analyzed, for a commonly used gate driving circuit.

The gate circuit is composed of input capacitance C_{iss}, gate stray inductances L_G and L_S, intrinsic gate resistance R_G and external gate resistance $R_{g,ext}$ (2.21).

$$v_{g,in}(t) = i_G(t) \cdot R_{g,on} + (L_G + L_S) \cdot \frac{\mathrm{d}i_G(t)}{\mathrm{d}t} + v_{gs}(t)$$

$$\text{being} \quad i_G(t) = C_{GS} \cdot \frac{\mathrm{d}v_{gs}(t)}{\mathrm{d}t} \tag{2.21}$$

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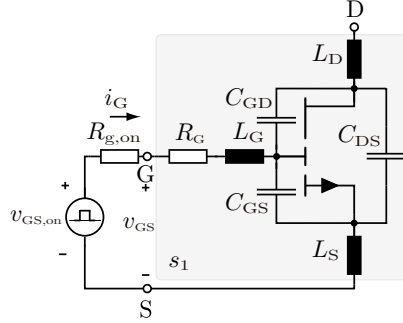
Figure 2.11: Driver external gate resistance selection equivalent circuit.

Solving differential equation (2.21), Laplace transform is derived

$$\frac{V_{\mathrm{g,in}}(s)}{v_{\mathrm{gs}}(s)} = \frac{\frac{1}{(L_{\mathrm{G}}+L_{\mathrm{S}})\cdot C_{\mathrm{GS}}}}{s^2 + \frac{R_{\mathrm{g,on}}}{(L_{\mathrm{G}}+L_{\mathrm{S}})}\cdot s + \frac{1}{(L_{\mathrm{G}}+L_{\mathrm{S}})\cdot C_{\mathrm{GS}}}}. \tag{2.22}$$

Then, the dynamic is analyzed, comparing (2.22) to the standard second order system.

$$H(s) = \frac{\omega_{\mathrm{n}}^2}{s^2 + 2\cdot\zeta\cdot\omega_{\mathrm{n}} + \omega_{\mathrm{n}}^2} \tag{2.23}$$

being ω_{n} the natural frequency and ζ the damping ratio. In this case, ω_{n} correspond to the resonance frequency of parasitics components (2.24) while the damping ratio is defined by (2.25)

$$\omega_{\mathrm{n}} = \frac{1}{\sqrt{(L_{\mathrm{G}}+L_{\mathrm{S}})\cdot C_{\mathrm{GS}}}} \tag{2.24}$$

$$\zeta = \frac{1}{2}\cdot R_{\mathrm{g,on}}\cdot\sqrt{\frac{C_{\mathrm{GS}}}{L_{\mathrm{G}}+L_{\mathrm{S}}}} \tag{2.25}$$

Figure 2.12 shows the influence of the gate resistance $R_{\mathrm{g,on}}$ on the damping ratio. Considering the characteristics of IGO60R070D1 [108] and an stray inductances presented in Table 3.5, a damping ratio higher than 0.4 is defined for analyzed GaN devices achieving low overvoltage with a minimum $R_{\mathrm{g,on}}$ of 5.68 Ω.
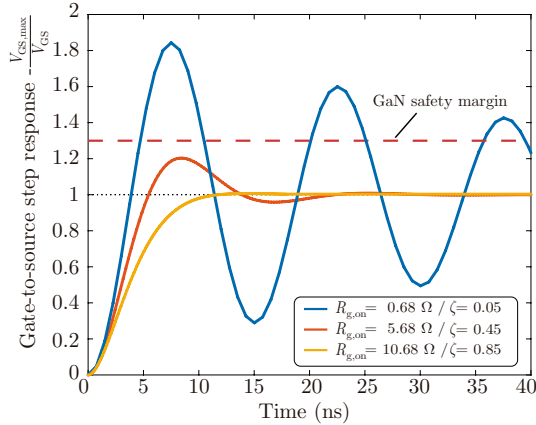
Figure 2.12: Driver external gate resistance selection, V_{GS} step response.

Therefore, optimal gate pull-up $R_{g,on}$ and pull-down $R_{g,off}$ resistances must be selected to reduce gate voltage peak voltage. Referring $R_{g,off}$ some recommendations are outlined in [46], defining a $R_{g,off}$ ten times lower than turn-on gate resistance.

2.5.2 False turn-on

The threshold voltage of GaN devices is very low (0.7-2 V). Indeed, any ringing caused by the induced voltage on stray inductances can result on an unwanted turn-on of the semiconductor as it is analyzed for SiC in [116]. Figure 2.13 shows the equivalent circuit of the turn-off transition of low-side switch s_2, where the rapid turn-on of high-side device s_1 can lead to a high dv/dt on s_2.

This transient equivalent circuit is analytically evaluated, solving the differential equation system represented with (2.26) and (2.27).

$$0 = i_G(t) \cdot R_{g,off} + (L_G + L_S) \cdot \frac{di_G(t)}{dt} + v_{gs}(t) + L_S \cdot \frac{di_d(t)}{dt}$$
$$\text{being} \quad i_G(t) = (C_{GS} + C_{GD}) \cdot \frac{dv_{gs}(t)}{dt} - C_{GD} \cdot \frac{dv_{ds}(t)}{dt} \tag{2.26}$$
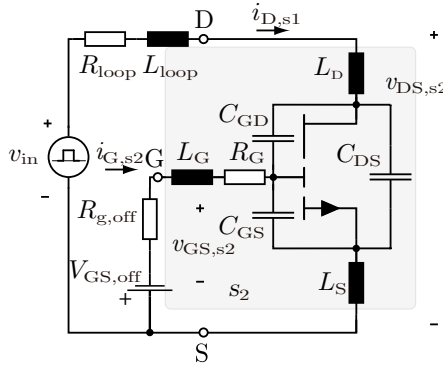
Figure 2.13: Driver turn-off voltage selection, synchronous device equivalent circuit.

$$v_{in}(t) = i_d(t) \cdot R_{Loop} + (L_{Loop} + L_S + L_D) \cdot \frac{di_G(t)}{dt} + v_{ds}(t)$$
$$+ L_S \cdot \frac{di_G(t)}{dt} \quad (2.27)$$
$$\text{being} \quad i_d(t) = (C_{DS} + C_{GD}) \cdot \frac{dv_{ds}(t)}{dt} - C_{GD} \cdot \frac{dv_{gs}(t)}{dt}$$

Then, solving (2.26),(2.27), Laplace transform is derived and the step response of those voltages is evaluated for an input voltage step $v_{in}(t)$: $\frac{V_{gs}(s)}{v_{in}(s)}$ and $\frac{V_{ds}(s)}{v_{in}(s)}$

Figure 2.14 shows how the $R_{g,off}$ affects directly to the peak voltage of the gate. Then, $R_{g,off}$ needs to be reduced in order to avoid false-turn-on. However, as the $R_{g,off}$ increases the damping factor also increases, reducing the gate-to-source ripple. Therefore, a trade-off between damping and the peak voltage needs to be considered when choosing $R_{g,off}$. In addition, a negative $V_{GS,off}$ is recommended so as to reduce the peak voltage avoiding false turn-on of s_2. Otherwise, even for low $R_{g,off}$, this driver configuration will result on false turn-on, as it is shown in Figure 2.14.

Therefore, driver resistors and voltage has to be chosen correctly
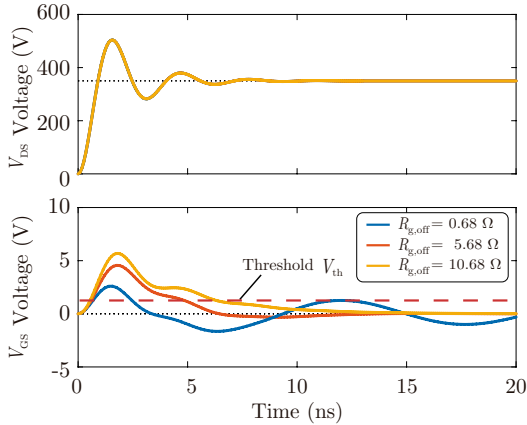
Figure 2.14: Driver turn-off voltage selection, dynamic response of V_{GS} and V_{DS} for various $R_{g,off}$.

in order to take full advantage of GaN devices benefits but without exceeding gate voltage safety margin and avoiding false turn-on.

2.5.3 Current controlled driver

Specific driver is designed according to the characteristics of GIT devices [108, 117]. Figure 2.15(a) shows the equivalent circuit of GIT device, with an internal gate-to-source diode D_{GS}.

The fact that the gate is not insulated and has a p-n junction from gate to source, allows the gate to sink current above a certain V_{GS} value. The diode D_{GS} has a typical dropout voltage of 3 V, so, if a higher voltage is applied to the gate, a current will flow through the gate to the source. This current will be limited by the device input impedance and also by the gate circuit output impedance. The designed gate circuit uses a positive power supply and a capacitor to generate a negative temporary gate voltage [see Figure 2.15(b)].

Figure 2.16 depicts waveforms of one switching cycle simulated with SPICE models. The switching on transition begins with the turning-on of s_1. Gate voltage $V_{GS,1}$ is below the voltage of the internal diode ($V_{D_{GS}}$) and both C_{ss} and C_{iss} are charged with $\tau = R_{GS,on} \cdot C_{iss}$, until $V_{GS,1} = V_{Dgs}$, assuming $C_{ss} >> C_{iss}$. Then, C_{ss} is further charged to
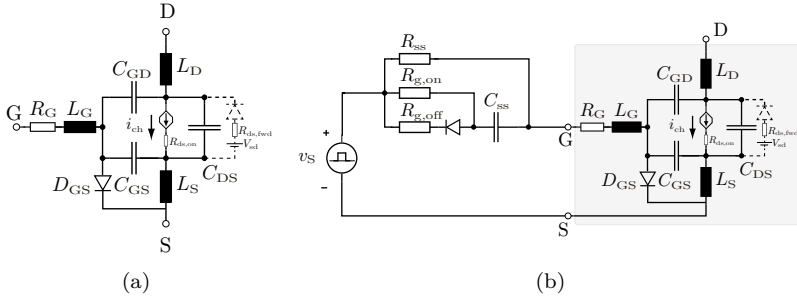
Figure 2.15: Current controlled driver: (a) equivalent circuit of GIT devices and (b) gate driver circuit.

$V_{\text{Css,max}}$

$$V_{\text{Css,max}} = V_{\text{gg}} - V_{\text{Dgs}} \tag{2.28}$$

where V_{gg} is the voltage of the push-pull. During turn-on interval, C_{ss} is charged and only a current I_{ss} is flowing, which is defined with R_{ss}.

When analyzing the turn-off transition, as C_{ss} is charged to $V_{\text{Css,max}}$, the capacitor voltage is applied to the gate but it is negative. Then, C_{ss} and C_{iss} are discharged through $R_{\text{GS,off}}$. This interval ends when C_{ss} and C_{iss} are charged at the same voltage, i.e. turn-off gate voltage ($V_{\text{GS,off}}$). If losses in $R_{\text{GS,off}}$ during this phase are neglected, $V_{\text{GS,off}}$ can be calculated using the principle of charge conservation:

$$C_{\text{iss}} \cdot V_{\text{Css,max}} - C_{\text{ss}} \cdot V_{\text{Css,max}} = C_{\text{iss}} \cdot V_{\text{GS,off}} - C_{\text{ss}} \cdot V_{\text{GS,off}}$$

$$V_{\text{GS,off}} = V_{\text{Dgs}} - \frac{C_{\text{ss}}}{C_{\text{ss}} + C_{\text{iss}}} \cdot V_{\text{gg}} \tag{2.29}$$

being $V_{\text{GS,off}}$ negative if $C_{\text{ss}} > \frac{V_{\text{Dgs}}}{V_{\text{gg}} - V_{\text{Dgs}}}$.

Regarding the sizing of gate driver components, turn-on and turn-off gate resistances are selected in order to do not overcome the maximum allowed gate-to-source voltage, as it is analyzed for common drivers in Section 2.5. Besides, the additional capacitance C_{ss} and resistance are defined in order to achieve a negative gate-to-source voltage $V_{\text{gs,off}}$.

The required C_{ss} for a defined $V_{\text{gs,off}}$ is obtained, solving (2.29).

$$C_{\text{ss}} = C_{\text{iss}} \cdot \frac{V_{\text{Dgs}} - V_{\text{gs,off}}}{V_{\text{gg}} + V_{\text{gs,off}} - V_{\text{Dgs}}} \tag{2.30}$$
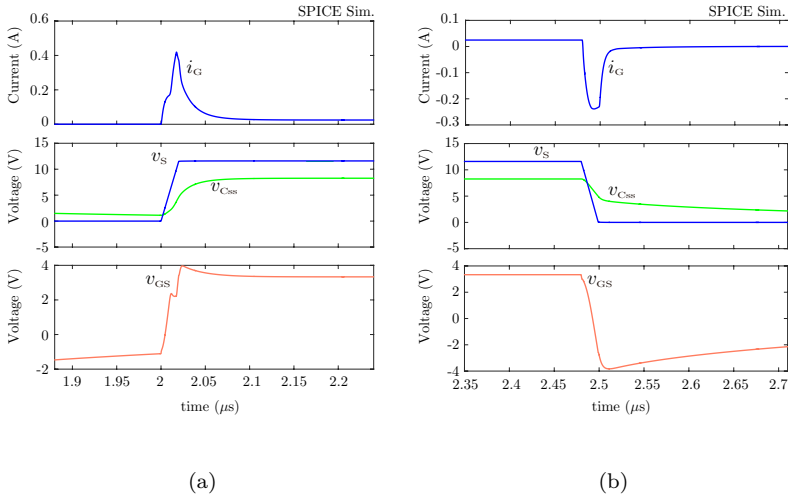
Figure 2.16: SPICE waveforms of the gate drive circuit with decoupling capacitor C_{ss}, during one switching cycle: (a) turn-on and (b) turn-off transient.

Then, R_{ss} is defined for a reduced I_{ss} current, which will be flowing continuously through driver

$$R_{\text{ss}} = \frac{V_{\text{gg}} - V_{\text{Dgs}}}{I_{\text{ss}}} \tag{2.31}$$

Moreover, the time constant τ_{ss} related to the discharge of the capacitance C_{ss} is defined to be higher than the dead-time ($>100\,\text{ns}$), so when the complementary device turns-on, the device that is off still has negative V_{GS}, reducing false turn-on risk.

$$\tau_{\text{ss}} = R_{\text{ss}} \cdot (C_{\text{ss}} + C_{\text{iss}}) > t_{\text{dt}} \tag{2.32}$$

2.6 Thermal Analysis

A simple cooling system for power converters typically consists of a heatsink and a Thermal Interface Material (TIM) between the heat source (devices) and the heatsink, as it is shown in Figure 2.17. For this analysis, the active area of IGO60R070D1 ($13.9\text{x}5.6\,\text{mm}^2$) [108] is

considered. Moreover, 40x40 mm^2 heat-sink with a thermal resistance of 3.7 °C/W is considered, along with two types of TIMs: WLFT40R25 (adhesive) and Hi-Flow 300P (non-adhesive).

Refering to TIM, the conductive thermal resistance is proportional to the thickness of the material (d) and inversely proportional to the thermal conductivity (λ) and material surface (A)

$$R_{\mathrm{th,d}} = \frac{d}{\lambda \cdot \eta_\lambda \cdot A}. \tag{2.33}$$

being η_λ thermal conduction efficiency.

2.6.1 Thermal limits

Power losses of devices needs to be dissipated in order not to excess the maximum allowed junction temperature $T_{\mathrm{j,max}}$. Semiconductors are assumed to be mounted, via TIM, on a heatsink, which is at T_{hs} temperature (see Figure 2.17). Junction-to-case ($R_{\mathrm{th_{j-c}}}$) and case-to-heatsink ($R_{\mathrm{th_{j-hs}}}$) thermal resistances are inversely proportional to the effective area (A_{e}) of devices, which increases with the number of parallel devices (2.34) (see Figure 2.17).

$$\begin{aligned} R_{\mathrm{th_{j-c}}}(A_e) &= r_{\mathrm{th_{j-c}}}/(A_{\mathrm{e}} \cdot N_{\mathrm{p}}) \\ R_{\mathrm{th_{c-hs}}}(A_e) &= r_{\mathrm{th_{c-hs}}}/(A_{\mathrm{e}} \cdot N_{\mathrm{p}}) \end{aligned} \tag{2.34}$$

where $r_{\mathrm{th_{j-c}}}$ and $r_{\mathrm{th_{c-hs}}}$ are junction-to-case and case-to-heatsink specific thermal resistance (mm^2°C/W), respectively.

Then, power losses limit of semiconductors ($P_{\mathrm{d,lim}}$) is obtained evaluating resistances of the thermal network $R_{\mathrm{th_{j-c}}}$ and $R_{\mathrm{th_{c-hs}}}$.

$$P_{\mathrm{d,lim}} = \frac{T_{\mathrm{j,max}} - T_{\mathrm{hs}}}{R_{\mathrm{th_{j-c}}}(A_{\mathrm{e}}) + R_{\mathrm{th_{c-hs}}}(A_{\mathrm{e}})} \tag{2.35}$$

Considering GaN devices with low stray inductance package, i.e. small A_{e}, the impact of thermal resistances is very high, reducing the thermal cooling capability. Nevertheless, the use of N_{p} number of devices increases the power dissipation capability for a junction-to-heatsink specific resistance ($r_{\mathrm{th_{j-hs}}}$)

$$P_{\mathrm{d,lim}} = \frac{T_{\mathrm{j,max}} - T_{\mathrm{hs}}}{r_{\mathrm{th_{j-hs}}}} \cdot (A_{\mathrm{e}} \cdot N_{\mathrm{p}}) \tag{2.36}$$
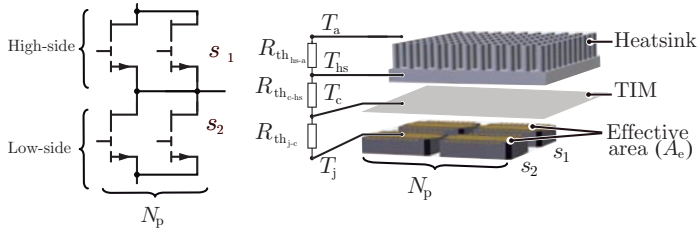
Figure 2.17: GaN devices in half-bridge configuration, with N_{p} number of devices connected in parallel, electrical and thermal equivalent circuit.

Hence, optimum number of devices has to be considered in order to satisfy the maximum allowed semiconductor losses (2.36) for a $T_{\mathrm{j,max}}$ and the minimum power losses. Moreover, an increase on the active area of devices using heat-spreading materials will improve the thermal performance of current GaN devices.

2.6.2 Heat-spreading

In this section, the effect of heat-spreading materials on thermal performance of GaN switches is analyzed, which have been already proposed for power modules [118, 119]. As a consequence of a change on the surface area through which the heat flows, an additional resistive component, has to be considered, i.e. the spreading resistance. Spreading resistance depends on relation ϵ between active area of the devices $A_{\mathrm{e}} \cdot N_{\mathrm{p}}$ and the spreading area A_{sp} (2.37).

$$\epsilon = \sqrt{\frac{A_{\mathrm{e}} \cdot N_{\mathrm{p}}}{A_{\mathrm{sp}}}}. \tag{2.37}$$

The calculation of the spreading resistance for cooling solutions of GaN devices is based on the detailed derivation of the average spreading resistance presented in [118]. Moreover, the simplifications applied to a power module case study presented in [119] are revised for discrete GaN characteristics. In this case the heat-spreading material is placed between the heat source, i.e. GaN device, and the TIM, as it is depicted in Figure 2.18, considering N_{p} number of paralleled devices.

Then, for the configuration presented in Figure 2.18(b), the thermal

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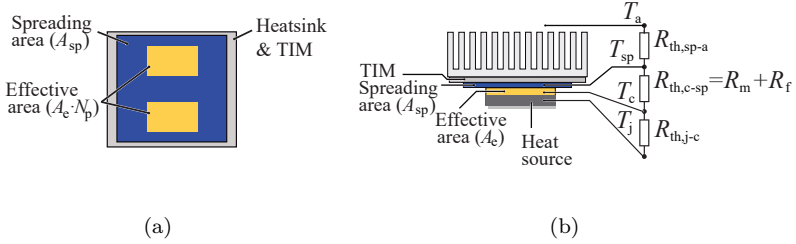
Figure 2.18: Cooling system geometry which consists on a heat source, a spreading material, a TIM and a heatsink : (a) cooling system diagram and (b) thermal resistance equivalent circuit.

resistance equivalent circuit can be written as (2.38).

$$R_{\text{th,eq}} = \frac{R_{\text{th,j-c}}}{N_{\text{p}}} + \underbrace{R_{\text{m}} + R_{\text{f}}}_{R_{\text{th}_{\text{c-sp}}}} + R_{\text{th}_{\text{sp-a}}} \tag{2.38}$$

where $R_{\text{th}_{\text{c-sp}}}$ is composed of conductive resistance R_{m} and spreading resistance R_{f}, while $R_{\text{th}_{\text{sp-a}}}$ includes the TIM and heatsink thermal resistance

$$R_{\text{th}_{\text{sp-a}}} = \frac{d_0}{\lambda_0 \cdot A_{\text{sp}}} + R_{\text{th,hs}} \tag{2.39}$$

where λ_0 is the thermal conductivity, which is pressure dependent, d_0 is the thickness of the TIM and the area A_{sp} is related to the heat-spreading material.

Moreover, resistances that conform $R_{\text{th,c-s}}$ are analyzed for d_{sp} thickness and λ_{sp} thermal conductivity, being:

$$R_{\text{m}} = \frac{d_{\text{sp}}}{\lambda_{\text{sp}} \cdot A_{\text{sp}}} \tag{2.40}$$

and

$$R_{\text{f}} = \frac{\psi}{\lambda_{\text{sp}} \cdot \sqrt{A_{\text{e}} \cdot N_{\text{p}}}} \tag{2.41}$$

where ψ is the dimensionless constriction resistance approximated with (2.42) [118].

$$\psi = \frac{1}{2} \cdot (1-\epsilon)^{\frac{3}{2}} \cdot \frac{\tanh\left(\sigma_c \tau\right) + \frac{\sigma_c}{B_i}}{1 + \sigma_c \cdot B_i \cdot \tanh\left(\sigma_c \tau\right)} \qquad (2.42)$$

being

$$\sigma_c = \pi + \frac{1}{\sqrt{\pi} \cdot \epsilon} \quad , \quad \tau = d_{sp} \cdot \sqrt{\frac{\pi}{A_{sp}}} \qquad (2.43)$$

and with an approximation of the Biot number B_i [119], which is dependent on the previously defined $R_{th_{sp-a}}$

$$B_i = \frac{1}{R_{th_{sp-a}} \cdot \lambda_{sp} \cdot \sqrt{\pi \cdot A_{sp}}}. \qquad (2.44)$$

Then, the impact of spreading resistances is evaluated for graphite heat-spreading material with high thermal conductivity [1950 W/(m·℃)] and $10\,\mu$m of length (EYG-A091201V). The variation of total equivalent thermal resistance with the incursion of heat-spreading material is depicted in Figure 2.19(a) for the spreading area ratio $A_{sp}/(A_e \cdot N_p)$.

The spreading area is limited by the half of heatsink surface (A_{sp}). Figure 2.19(a) shows how the equivalent resistance is reduced as effective area increases, especially when the TIM resistance has great influence. Actually when the size of the semiconductor is small or the TIM thermal conductive is high, such as adhesive TIMs. Therefore, the selection of a TIM that provides electrical isolation with high thermal conductivity is also relevant for GaN devices [see Figure 2.19(a)]. Moreover, even if a heat-spreading resistance is added, the increase of the area A_{sp} reduces the TIM resistance, improving the system thermal cooling capability.

In addition, the use of N_p number of devices increases the active area while reduces the equivalent resistance, as it is presented in Figure 2.19(b). Hence, the use of multiple devices is relevant for systems with high cooling capability requirement.
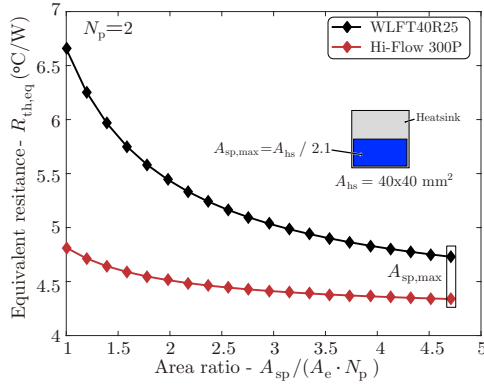
(a)
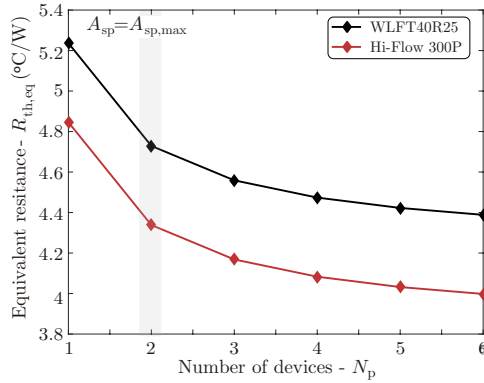
(b)

Figure 2.19:   Heat-spreading for IGO60R070D1- [108] device and WLFT40R25 TIM with a graphite spreading material (EYGS091210): (a) analyzing the impact of spreading area A_{sp} for N_p=2 and (b) evaluating the impact of different number of N_p devices connected in parallel, for the maximum A_{sp}, considering a heatsink of 40x40 mm^2.

2.7   Conclusions

In this chapter, the main differential characteristics have been ana-
lyzed, defining the benefits and limits of GaN devices. First, GaN
devices characteristics are compared to Si and SiC counterparts. GaN
semiconductors present lower overall conduction resistance even com-
pared to Si Super-junction devices in the range of 600 V. Moreover,
GaN present lower output capacitance along with lower gate charge re-
quirement. This results on lower switching and driver losses. However,
special attention must be devoted when designing gate driver to not
excess the maximum allowable gate voltage and to avoid false turn-on.
Furthermore, the gate driver is analyzed defining the gate resistances
and voltages for a suitable operation of GaN devices.

In addition, even if GaN devices have a negligible reverse recovery
free-wheeling conduction, losses generated in these conduction instances
is higher than for Si or SiC MOSFETs. Therefore, dead-time conduction
instances are analyzed, defining the minimum dead-time, in order to
reduce losses related to free-wheeling conduction instances.

Regarding switching characteristics, the high-switching speed of
GaN devices and corresponding low switching losses have been eval-
uated, defining scaling derivations based on SPICE models. As GaN
presents a higher variation of the transconductance with the junction
temperature than other technologies, scaling derivations are also defined
considering this thermal effect.

Furthermore, thermal cooling limits are analyzed and the use of
heat-spreading materials is proposed. The increase of thermal pad
through high thermal conductivity heat-spreading materials results on
an enhancement of cooling capability. Besides, paralleling GaN de-
vices will be essential for medium-high power converters, in order to
distribute power losses through larger dissipation area.

Therefore, this chapter highlights the conduction and switching ben-
efits of GaN devices. Moreover, a dead-time selection model is proposed,
along with an analysis of driver requirements and an improvement of
thermal cooling system. The analysis presented in this chapter will
be validated in Chapter 3 at different operation conditions and with
experimental measurements.

Chapter 3

Performance Evaluation of GaN Semiconductors

T HE most differential aspects that need to be considered when using GaN power devices have been analyzed in Chapter 2. In this chapter, these requirements and differential characteristics are taken into consideration for the design, evaluation and validation of GaN-based power converters.

First, in Section 3.1 two experimental prototypes based on GaN devices are presented, which are used along the chapter to validate the analysis presented in Chapter 2. Afterwards, design challenges are presented in Section 3.2. The driver design needs to be especially considered, in order to not overcome voltage safety margin and to avoid false-turn on (Section 2.5). Voltage and current controlled driver designs are presented. Moreover, as a consequence of the open-state conduction characteristic of GaN devices, different dead-time control strategies are proposed in Section 3.2.2. Also, the parallelization of GaN devices has been presented as essential in order to increase the thermal cooling capability in Section 2.6. Parallelization aspects related to layout are presented in Section 3.2.3, achieving an current sharing between parallel-connected devices.

In Section 3.3, thermal limits of GaN devices are evaluated for different cooling configurations. Top side and bottom side cooling configurations presented in [54] are analyzed. Furthermore, the analysis of the incursion of heat-spreading material analyzed in Section 2.6 is

evaluated for both configurations. The analysis of different cooling solutions is experimentally validated with the two prototypes presented in Section 3.1.

Section 3.4 evaluates power losses of GaN devices for a half-bridge configuration. Considering the characteristics obtained in Chapter 2, a power losses model is presented. The impact of switching voltage and junction temperature on the switching losses distribution is analyzed defining a switching losses model. In addition, the distribution of power losses is evaluated on a well known synchronous buck converter, defining the most critical factors. This analysis is an extended version of the results presented in [120]. In addition, the analysis includes the power losses of GaN devices at different operating conditions. Therefore, analyzing the losses breakdown, the most suitable operating conditions are identified. Besides, the obtained results are experimentally validated. For that purpose, steady state calorimetric measurements at converter level are carried out.

Finally, in Section 3.5, the conclusions obtained in this chapter are summarized.

3.1   GaN-based Converter Prototypes

GaN-based power boards presented in [54] are used to validate the results obtained in Chapter 2. With the aim of performing a general analysis, half-bridge configuration is selected, defining a configurable hardware in order to validate different concepts. Besides, power stage is controlled by an external hardware sending the control signals through the control connector. Figure 3.1 shows a general view of the validation set-up, which is formed by a power stage and control stage. On the one hand, power stage is conformed by different boards: power board, capacitors, etc. These boards are connected to a rack, being possible to configure it for different topologies. On the other hand, the control stage is developed on a National Instrument SbRIO controlling the power stage by its inputs and outputs, which are adapted via conditioning board (Interface).

Two power boards based on different GaN devices are used in this work. Figure 3.2 shows top and bottom layers of the converter based on GaN devices with insulated gate (650 V/60 A) [121]. The presented prototype contains driver, sensing conditioning, protections, semiconductors and a heatsink on the top side.
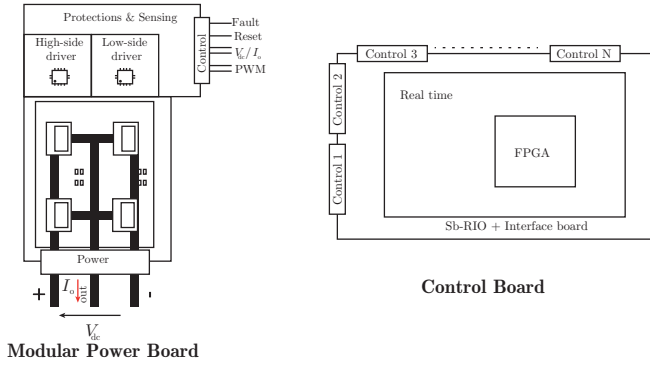
Figure 3.1: General scheme of the configurable set-up, which includes power and control stages.
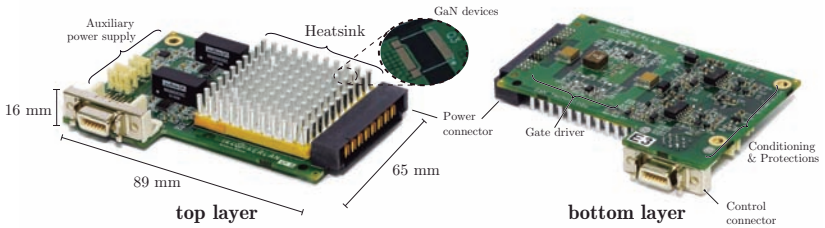
Figure 3.2: Half-bridge configuration power board based on GS61008T-[122], top-cooled.

Figure 3.3 shows a similar power board but based on GIT devices. Moreover, these devices are bottom-side cooled.
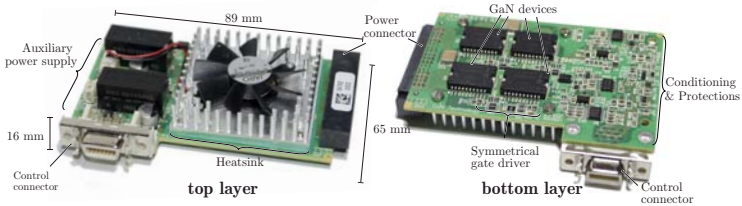
Figure 3.3: Modular half-bridge power board presented in [54] based on paralleled GaN devices IGO60R070D1- [108].

The area of the heat source (thermal pad) is relatively small, limiting

the thermal capability (2.36), as it is presented in Section A.0.1. Hence, the performance of two GaN devices with different cooling structure is evaluated: top-side and bottom-side cooled devices. The characteristics of these devices are summarized in Table 3.1.

Table 3.1: Electrical and thermal characteristics of GaN devices.

Parameter	GIT [108]	HEMT [122]	
Drain-to-source voltage-V_{DS}	650	600	V
Conduction resistance-$R_{\mathrm{ds,ref}}$@25 ℃	32	55	mΩ
Maximum temperature-$T_{\mathrm{j,max}}$	150	150	℃
Junction-to-case resistor-$R_{\mathrm{th_{j-c}}}$	0.3	0.8	℃/W
Junction-to-package resistor-$R_{\mathrm{th_{j-b}}}$	3	5	℃/W
Active area-A_{e}	3.1 x 6.5	3.2 x 13.7	mm x mm
Thermal performance-FOM$_{\mathrm{th}}$	5.50	30.23	mm$^2\cdot$℃/W

In addition, thermal characteristics of these prototypes will be analyzed in detail in Section 3.3 and power losses distribution is evaluated in Section 3.4.

3.2 Design Considerations

Considering unique characteristics of GaN switches, it is important to identify the specific challenges of designing GaN based power converters. Although there are many aspects to consider in the design of a GaN based power converter, this work is mainly focused on gate driver design, dead-time control and parallelization of devices. These design aspects are considered, as a consequence of the importance of proper driving signals (Section 2.5), the impact of dead-time losses (Section 2.2.1) and the importance of paralleling GaN devices (Section 2.6).

3.2.1 Driver design

Different aspects related to gate driver design of two types of available GaN devices are analyzed in this subsection: normally-off HEMT [122] and GIT [108]. GaN HEMT devices present a most commonly implemented voltage controlled gate, while for turning-on GIT devices

their gate current must be controlled due to the diode forward voltage (around 3.5 V) [117].

Voltage controlled driver

In this configuration, the widely used gate driver circuit based on push-pull gate driver circuit with turn-on and turn-off gate resistance is employed for a 650 V GaN HEMT with insulated gate (GS66516T- [122]). Then, the analysis presented in Section 2.5 is used to define the gate resistances and voltages in order to not excess voltage safety margin and to avoid false turn-on.

For that purpose a turn-on gate resistance of 24 Ω is defined. In this manner, V_{GS} is lower than the maximum V_{GS}, as it is depicted in Figure 3.4. The increase of the turn-on resistance reduces the overvoltage on the V_{GS}, as it is analyzed in Section 2.5. Moreover, false turn-on is also avoided. However, the switching speed is reduced with the increase of the turn-on gate resistance. Another possibility would be the use of negative turn-off voltage. However, for design simplicity and to avoid negative voltages, negative turn-off voltage is not considered. Moreover, the gate requirements are fulfilled with this design.
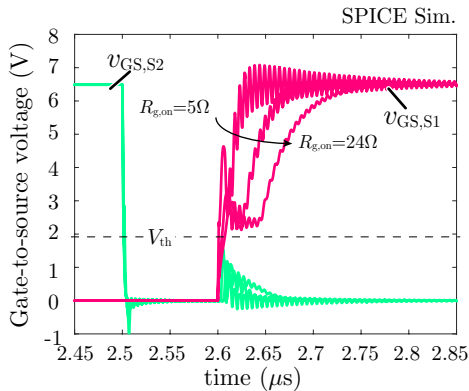
Figure 3.4: SPICE gate-to-source voltage of the voltage controlled driver for HEMT devices.

Gate driver design is validated through experimental measurements. Figure 3.5 shows V_{GS} of half-bridge configuration without exceeding voltage safety margin and without false turn-on.
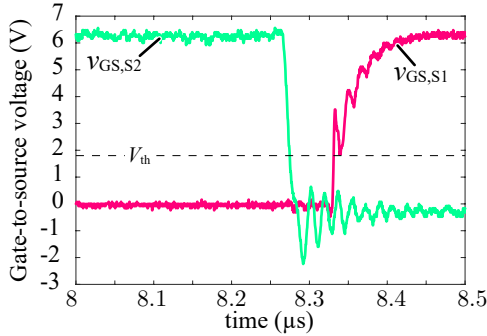
Figure 3.5: Experimental gate-to-source voltage of the voltage controlled driver for HEMT devices.

Current controlled driver

Gate driver circuit is designed based on the theoretical and simulation results presented in Section 2.5.3. Figure 3.6 presents the experimental measurements of the gate-to-source voltage. In this case a gate resistance of $10\,\Omega$ is selected, achieving a low overvoltage on the V_{GS}. The maximum allowed V_{GS} is not exceed when turning-on, as it is demonstrated in Figure 3.6(a), validating the analysis presented in Section 2.5.

Moreover, the current controlled driver design presented Section 2.5.3 achieves negative turn-off voltage. Hence, a negative $V_{\mathrm{GS,off}}$ is ensured, avoiding false turn-on as it is depicted in Figure 3.6(b).

3.2.2 Dead-time control

The analysis presented in Section 2.3 applies also for the gate driver circuit of GIT devices, as the series capacitor C_{ss} is considerably higher than C_{iss}. Therefore, minimum dead-times are calculated, considering the characteristics of selected GaN devices (see Table 3.1). Table 3.2 shows the results obtained for driver designs presented in Section 3.2.1. These results will be validated in the experimental section, avoiding shoot-through with reduced power losses.

Commonly symmetrical dead-time control is used for a half-bridge configuration, i.e. both dead-time instances ($t_{\mathrm{dt,on}}$ and $t_{\mathrm{dt,off}}$) are the same. However, this dead-time control strategy can result on high dead-
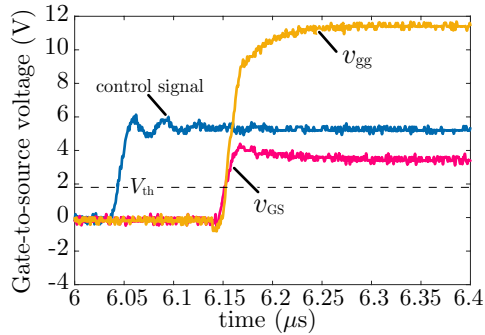
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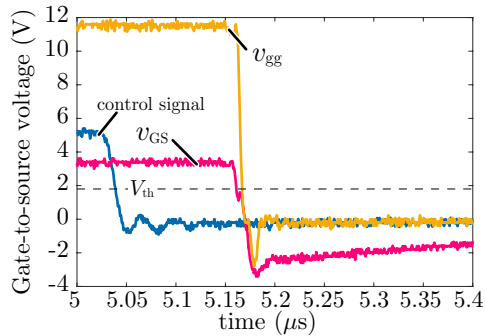
(b)

Figure 3.6: Experimental gate-to-source voltage of the current controlled driver for GIT devices: (a) turn-on and (b) turn-off.

time conduction energy E_{dt} when long dead-times are needed in order to achieve Zero-Voltage Switching (ZVS) transition. However, only turn-on dead-time needs to be increased in order to achieve ZVS. Then, applying different $t_{dt,on}$ and $t_{dt,off}$, i.e. asymmetrical dead-time control, impact of dead-time losses will be reduced. Afterwards, the impact on power losses is analyzed, comparing power losses of both dead-time control strategies.

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Table 3.2: Minimum dead-time results.

Characteristics	GIT [108]	HEMT [121]	
Gate charge	5.8	12.1	nC
Turn-on/turn-off gate voltage	4/-3	6.5/0	V
Turn-on/Turn-off resistance	10/10	24/0	Ω
Gate driver	SI8261BAC	1EDI20N12AF	
Propagation delay on/off	60/50	137/143	ns
Turn-off dead-time $t_{dt,off}$ (10 A):	45	85	ns
Turn-on dead-time $t_{dt,on}$:	80	80	ns

3.2.3 Parallelization of GaN devices

GaN devices conduction resistance presents a positive temperature co-efficient characteristic [see Figure 2.3(b)]. This characteristic tends to compensate static current balancing when paralleling devices. However, the dynamic current balancing will be the most influential factor, due to high-switching frequency operation and high commutation speed of GaN devices. Besides, the low threshold voltage together with a high commutation speed, implies a greater driver loop consideration, ensuring a high $dv(t)/dt$ immunity [123].

Hence, it is noteworthy to design a low stray inductance and symmetric layout to ensure a balanced dynamic current. Moreover, equal gate drive loop length provides an identical turn-on and turn-off times, keeping a good thermal balancing [124, 125]. Figure 3.7 shows an identical gate resistances circuits driving parallel-connected devices from the same driver and control. This gate circuit ensures a balanced gate-to-source voltage as a consequence of similar gate loop. In addition decoupling capacitors are located near to the driver circuit. Driving voltages along with $R_{g,on}$ and $R_{g,off}$ have been selected bearing in mind the analysis presented in Section 2.5. Furthermore, parasitic inductances of the gate driver have to be reduced, locating the driver as close as possible to the switch, as it is depicted in Figure 3.7. The use of the proposed gate driver scheme will ensure a well distributed losses among parallel-connected devices.

The thermal distribution is evaluated in buck configuration at hard-switching operation mode. Figure 3.8(a) shows how even for transient there is a minor difference of temperature between paralleled devices.
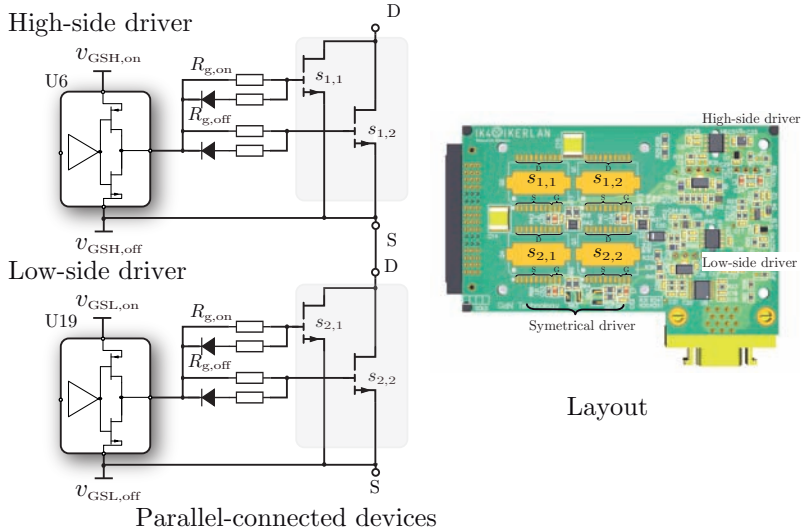
Figure 3.7: Parallel-connected devices gate driver scheme and layout proposal.

The main difference appears when comparing high-side with low-side devices, due to higher losses of high-side devices. When achieving the steady-state the distribution is even better, as it is depicted in Figure 3.8(b). Hence, it is demonstrated that the designed driver ensures an evenly shared current through parallel-connected switches.
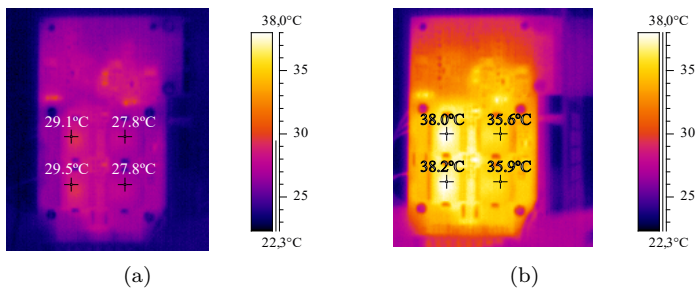
Figure 3.8: Validation of balanced current sharing via thermography: (a) switching transient of synchronous buck converter and (b) switching of synchronous buck converter at steady-state ($350\,\mathrm{V}/10\,\mathrm{A}/20\,\mathrm{kHz}$).

3.3 Thermal Limits Evaluation

Cooling variants of the prototypes presented in Section 3.1 are compared. The most critical elements of the cooling system are identified in order to take full advantage of GaN devices in power applications where high heat cooling capability is needed. Moreover, the impact of heat-spreading materials and parallel-connected devices is evaluated.

In this case, the top-side cooled package shows up the best thermal performance based on FOM_{th} (2.1), due to a lower junction-to-case thermal resistance (see Table 3.1). Nevertheless, the performance comparison of both solutions is not trivial, due to differences on the cooling system configuration and the relevance of A_e on the power dissipation capability (2.36). Then, two different solutions are compared, with the aim of studying the thermal performance at the power converter level: one with a thermal pad on the top-side, and the other on the bottom-side.

Moreover, it is worth pointing out that, as in this case all devices share the same heat sink, the thermal pad of each device must be electrically isolated. In terms of heatsink assembly, adhesive TIMs provide the possibility to avoid mechanical elements, e.g. screws and/or springs. However, it is not easy to assure a proper level of pressure, and the thermal performance could not be good enough in some high-power applications. On the contrary, non-adhesive TIMs achieve better thermal performance, reaching thermal resistance below $2\,°C/W$ even for such small active area [see Figure 3.9]. Thus, considering the high impact of TIM thermal resistance an enhancement of the cooling capability is required.

3.3.1 Cooling configurations

Power boards based on top-side cooled and bottom-side cooled GaN devices, presented in Section 3.1 are thermally evaluated. Furthermore, in order to evaluate the enhancement of heat-spreading material, top-side cooled configuration with heat-spreading material is also analyzed. Therefore, the thermal performance of three different configurations is compared: top-side cooled, top-side cooled with heat-spreading (top-side sp) and bottom-side cooled. This theoretical model, based on different assumptions is only valid for a simplified model to provide a performance approach. Table 3.3 presents the specifications of the three configurations.
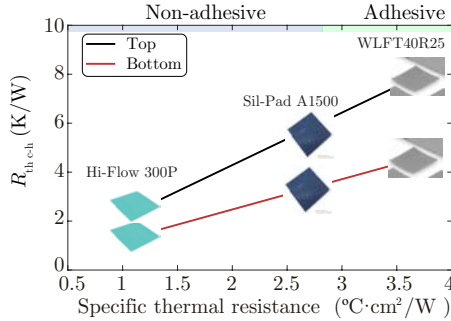
Figure 3.9: Impact of thermal resistance of different TIM, considering the effective area of top and bottom cooled devices.

Table 3.3: Specifications of cooling configurations.

PCB Specifications	Top	Top-sp	Bottom	
FR4 layers thickness	0.35	0.35	0.1	mm
Cu layers thickness	0.07	0.07	0.035	mm
Spreading thickness	-	$10 \cdot 10^{-3}$	1	mm
Spreading material	-	EYG-A091201V	Cu inlay	
TIM material	WLFT404R25	WLFT404R25	Hi-Flow 300P	
TIM active area	20.2	652	600	mm^2
Material properties	**Thermal conductivity**			
FR4	0.25			W/(m·°C)
Hi-Flow 300P	1.6			W/(m·°C)
WLFT404R25	0.4			W/(m·°C)
Cu-inlay	372			W/(m·°C)
EYG-A091201V	1950			W/(m·°C)

Top-side without heat-spreading

Top-side cooling seems to be a straightforward solution, transferring the heat directly through the heatsink. Besides, some micro-vias have been included in the PCB to increase thermal and electrical conduction through every possible layer (see Figure 3.10).

The equivalent junction-to-ambient resistance of the thermal equivalent circuit presented in Figure 3.10 is obtained solving (3.1), assuming
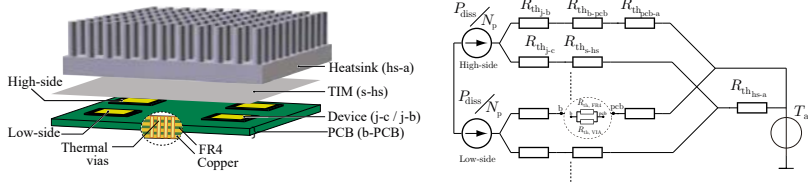
Figure 3.10: Top-cooled half-bridge configuration, i.e. high-side and low-side switches, with heatsink and micro-vias, along with the equivalent thermal circuit for N_{p} parallel-connected devices.

both sides (top and bottom) cooling.

$$R_{\mathrm{th}_{\mathrm{j-a,HEMT}}} = \frac{R_{\mathrm{th}_{\mathrm{j-a,TOP}}} \cdot R_{\mathrm{th}_{\mathrm{j-a,BOT}}}}{R_{\mathrm{th}_{\mathrm{j-a,TOP}}} + R_{\mathrm{th}_{\mathrm{j-a,BOT}}}} \quad \text{where}$$

$$R_{\mathrm{th}_{\mathrm{j-a,TOP}}} = \frac{R_{\mathrm{th}_{\mathrm{j-c}}} + R_{\mathrm{th}_{\mathrm{s-hs}}}}{2 \cdot N_{\mathrm{p}}} + R_{\mathrm{th}_{\mathrm{hs-a}}}, \qquad (3.1)$$

$$R_{\mathrm{th}_{\mathrm{j-a,BOT}}} = R_{\mathrm{th}_{\mathrm{j-b}}} + R_{\mathrm{th}_{\mathrm{b-PCB}}} + R_{\mathrm{th}_{\mathrm{PCB-a}}}$$

being $R_{\mathrm{th}_{\mathrm{c-hs}}}$ the thermal resistance of the TIM (WLFT404R25) and $R_{\mathrm{th}_{\mathrm{b-PCB}}}$ the thermal resistance of the PCB.

A first theoretical approximation is obtained solving (2.33) for materials properties and PCB characteristics presented in Table 3.3. For the PCB thermal resistance a parallel equivalent between Cooper (Cu) thermal vias (3.2) resistance and FR4 dielectric is assumed, as it is proposed in [126].

$$R_{\mathrm{th}_{\mathrm{b-PCB}}} = \frac{d_{\mathrm{via}}}{\lambda_{\mathrm{p}} \cdot \pi \cdot N_{\mathrm{v}} \cdot [\phi_1/2^2 - (\phi_1/2 - \phi_2/2)^2]} \qquad (3.2)$$

being d_{via} the length of the via, λ_{p} the conductivity of the copper, N_{v} the number of vias, ϕ_1 drilled diameter and ϕ_2 plated hole diameter.

However, a large PCB-to-ambient resistance is assumed, considering that all the heat is transferred through the heatsink ($R_{\mathrm{th}_{\mathrm{j-a,TOP}}}$). Then, solving (3.1) for the obtained thermal resistances the total junction-to-ambient resistance distribution is presented in Table 3.4.

Moreover, the maximum allowed power losses P_{lim} is obtained with (2.35), setting P_{lim} to be lower than 19.13 W.

Top-side with heat-spreading

Similar as in the top-side configuration, the heat is directly transferred through the heatsink but including a heat-spreading material between heat source and TIM (WLFT404R25), as it is depicted in Figure 3.11. A spreading material with high thermal conductivity is used (EYG-A091201V) in order to increase even more the effective area ($> A_\mathrm{e} \cdot N_\mathrm{p}$) and thus reduce the TIM resistance impact.
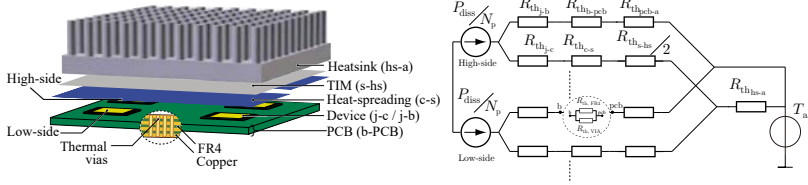
Figure 3.11: Top-side cooled prototype including a heat-spreading material, with heatsink and micro-vias, along with the equivalent thermal circuit.

The thermal network presented in Figure 3.11 is solved, obtaining following equivalent resistance:

$$R_{\mathrm{th_{j-a}}} = \frac{R_{\mathrm{th_{j-a,TOP}}} \cdot R_{\mathrm{th_{j-a,BOT}}}}{R_{\mathrm{th_{j-a,TOP}}} + R_{\mathrm{th_{j-a,BOT}}}} \quad \text{where}$$

$$R_{\mathrm{th_{j-a,TOP}}} = \frac{R_{\mathrm{th_{j-c}}} + R_{\mathrm{th_{c-sp}}}}{2 \cdot N_\mathrm{p}} + \frac{R_{\mathrm{th_{s-hs}}}}{2} + R_{\mathrm{th_{hs-a}}}, \qquad (3.3)$$

$$R_{\mathrm{th_{j-a,BOT}}} = R_{\mathrm{th_{j-b}}} + R_{\mathrm{th_{b-PCB}}} + R_{\mathrm{th_{PCB-a}}}$$

Although the heat-spreading material adds a thermal resistance ($R_{\mathrm{th_{c-s}}}$) into the thermal network, the equivalent junction-to-ambient resistance reduces as the TIM resistance has been reduced. Therefore, the maximum allowed power losses P_lim is increased up to 28.45 W.

Bottom-side with Cu inlay

In the bottom-side cooling configuration, different techniques can be used to improve the thermal performance during the design of PCB: using copper as a heat spreading media, introducing thermal vias on the PCB, increasing the thermal pad or inserting Cu inlay, among others
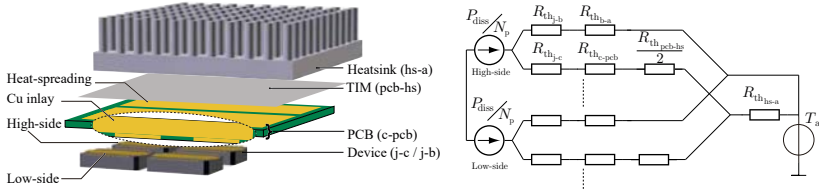
Figure 3.12: Bottom cooled configuration, with internal copper layers (Cu inlay) and equivalent thermal circuit.

[127,128]. For this configuration, Cu inlay with heat spreading has been demonstrated as the solution with the best performance [129].

The converter based on devices with bottom thermal pad has a direct contact with internal Cu through laser vias as it is depicted in Figure 3.12. Moreover, the area that is in contact with the TIM is bigger than in the top cooled variant. Using these techniques (increasing thermal pad and Cu inlay with laser vias), lower TIM thermal resistance is achieved due to heat flow spread over a wider area. However, the thermal resistance and the temperature of the PCB have to be considered, since almost all the heat is dissipated through this element, and it could be critical in some cases.

The equivalent junction-to-ambient resistance of the bottom cooling solution is derived (3.4)

$$
\begin{aligned}
R_{\mathrm{th_{j-a}}} &= \frac{R_{\mathrm{th_{j-a,TOP}}} \cdot R_{\mathrm{th_{j-a,BOT}}}}{R_{\mathrm{th_{j-a,TOP}}} + R_{\mathrm{th_{j-a,BOT}}}} \quad \text{where} \\
R_{\mathrm{th_{j-a,TOP}}} &= R_{\mathrm{th_{j-b}}} + R_{\mathrm{th,b-a}}, \\
R_{\mathrm{th_{j-a,BOT}}} &= \frac{R_{\mathrm{th_{j-c}}} + R_{\mathrm{th_{c-PCB}}}}{2 \cdot N_{\mathrm{p}}} + \frac{R_{\mathrm{th_{PCB-hs}}}}{2} + R_{\mathrm{th_{hs-a}}}
\end{aligned}
\tag{3.4}
$$

being $R_{\mathrm{th_{PCB-hs}}}$ the TIM thermal resistance (Hi-Flow 300P), $R_{\mathrm{th_{c-PCB}}}$ the PCB thermal resistance and assuming $R_{\mathrm{th_{b-a}}}$ to be large for the analytical model.

The PCB thermal resistance is obtained for a $1\,\mathrm{mm}$ width Cu inlay, considering the GIT device active area $(43\,\mathrm{mm}^2)$, and Cu as heat-spreading material (2.38)-(2.44). For the TIM thermal resistance a wider active area is considered $(600\,\mathrm{mm}^2)$, as it is shown in Figure 3.12.

Even with the inserted PCB thermal resistance, the bottom cooled solution presents a lower overall $R_{\mathrm{th_{j-a}}}$ due to the reduction of the TIM

resistance (see Table 3.4). Power losses limit is higher than in the top-cooling configurations (P_{lim}=39.5 W) due to lower overall $R_{\text{th}_{j-a}}$.

Table 3.4: Cooling solutions results.

Thermal resistance	Top	Top-sp	Bottom	
Surface-to-heatsink - $R_{\text{th,s}-\text{hs}}$	8.01	0.57	0.152	°C/W
Heatsink-to-ambient - $R_{\text{th,hs}-\text{a}}$	3.15	3.15	2.5	°C/W
Case-to-PCB - $R_{\text{th,c}-\text{PCB}}$	-	-	0.05	°C/W
Case-to-spreading - $R_{\text{th,c}-\text{sp}}$	-	0.01	-	°C/W
Package-to-PCB - $R_{\text{th,b}-\text{PCB}}$	3.43	3.43	-	°C/W
Junction-to-ambient - $R_{\text{th,j}-\text{a}}$	5.23	3.51	2.84	°C/W
Dissipated power - P_{dis}	19.13	28.45	39.5	W

However, when comparing $R_{\text{th}_{j-\text{hs}}}$ equivalent resistance, Top-sp and Bottom configurations presents similar performance. The use of high thermal conductivity heat-spreading material clearly reduces the impact of adhesive TIM. Therefore, the thermal cooling capability of top-cooled configuration is improved. Besides, the use of Cu inlay along with Cu heat-spreading achieves similar thermal performance than top-cooled devices.

3.3.2 Experimental evaluation

Top and bottom cooled boards presented in [54] are used for the experimental evaluation of three cooling solutions and validate the theoretical analysis (see Figure 3.13). Thermal performance of three cooling solutions is compared for a maximum junction temperature point below 125 °C. Figure 3.13 depicts two prototypes based on top-side (HEMT) and bottom-side (GIT) cooled devices and different heatsinks. In addition, Figure 3.13(c) shows heat-spreading material included between TIM and heat source for the top-side cooling configuration with heat-spreading (Top-sp).

For the thermal evaluation of each solution, devices of two power boards are characterized through conduction tests. Each board contains a half-bridge configuration, which is formed with two devices connected in parallel, as it is depicted in Figure 3.14(a).

For this characterization, the voltage drop (v_{TOP} and v_{BOT}) of the switches is measured, along with four heatsink temperatures (T_{hs}) and

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(a)

(b)

(c)
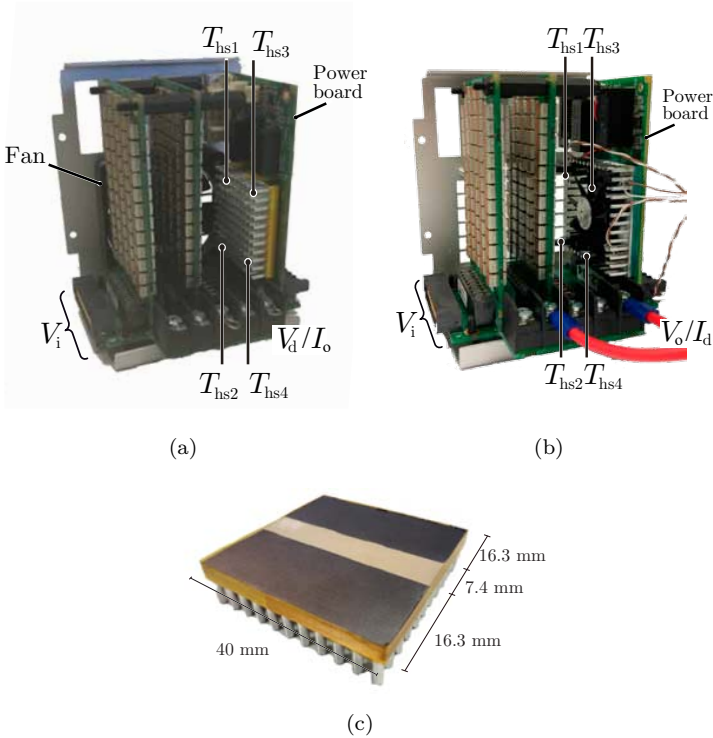
Figure 3.13: Half-bridge configuration power boards: (a) top-cooled pro-
totype based on [122] and with external forced-air heatsink, (b) bottom-
cooled prototype based on [108] with integrated fan heatsink and Cu-inlay;
and (c) top-side heatsink with heat-spreading material for the Top-sp con-
figuration.

ambient temperature (T_a), as it is presented in Fig. 3.14. Thermal
and electrical readings are obtained until the thermal equilibrium of
heatsink temperatures is achieved. The half-bridge is operated keeping
all switches (s_1, s_2, s_3 and s_4) in on-state with a controlled current
(I_d). A laboratory power supply in constant current mode is used to
adjust the current I_d and thus the dissipated power P_{dis}. Moreover, Fig-
ure 3.14(b) shows how the heatsink presents an evenly distributed tem-
perature, without great variations between measured points. Nevethe-
less, the maximum heatsink temperature is considered for the heatsink

temperature estimation.
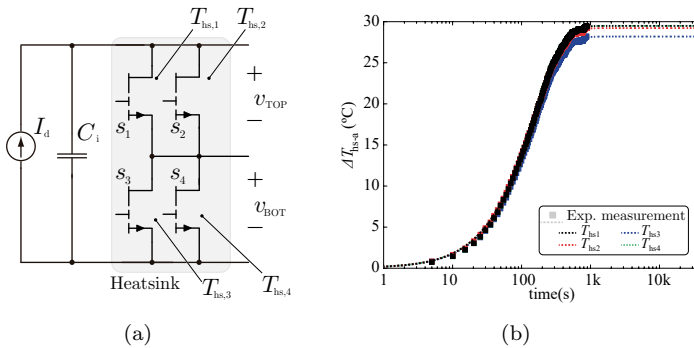
Figure 3.14: Experimental validation set-up: (a) half-bridge configuration scheme, with two GaN devices in parallel and (b) heatsink-to-ambient measurements

Then, thermal performance of different variants is evaluated considering different indicators: estimated junction temperature, total junction-to-ambient thermal resistance $R_{\mathrm{th_{j-a}}}$ and equivalent thermal resistance distribution. Even if the comparison between both solutions is not straightforward due to differences on the package of devices, heatsinks and TIM materials, these indicators identify the most suitable cooling solution. Furthermore, the enhancement of using a heat-spreading material for the top-side cooling configuration is evaluated, comparing $R_{\mathrm{th_{j-a}}}$ distribution of both configurations.

Junction temperature estimation

For the junction temperature estimation, Temperature Sensitive Electrical Parameter (TSEP) based on $R_{\mathrm{ds,on}}(T_j)$ is used. In order to extract conduction resistance dependence on the junction temperature iso-thermal measurements are performed with a short current pulse. As there is no significant self-heating during the pulse, junction temperature is iso-thermal with case temperature (T_{c}). Hence, it is possible to characterize $R_{\mathrm{ds,on}}$ at different T_{j} measuring T_{c} (3.5) [54].

$$T_{\mathrm{c}} \approx T_{\mathrm{j}} \qquad R_{\mathrm{DS_{on}}}(T_c) \approx R_{\mathrm{DS_{on}}}(T_j) \tag{3.5}$$

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Thus, $R_{\mathrm{ds,on}}$ is characterized for different T_{j} measuring T_{c}, as it is proposed in [54]. It has to be noted, that there is no degradation of the conduction resistance due to trapping electrons during this measurements, i.e. no dynamic $R_{\mathrm{ds,on}}$ effect. Hence, only temperature-dependent changes of $R_{\mathrm{ds,on}}$ are evaluated, since there are no off-state voltage stresses, as a consequence of very small voltage drop (V_{DS}) in conduction [49].

Therefore, measuring the voltage drop (v_{TOP} and v_{BOT}), controlled current I_{d} and T_{c}, $R_{\mathrm{ds,on}}(T_{\mathrm{j}})$ is obtained [see Figure 3.14(b)]. These results, can be approximated with (3.6) and (3.7), for reference on-state resistance ($R_{\mathrm{ds,ref}}$@25°C).

$$R_{\mathrm{ds,HEMT}}(T_{\mathrm{j}}) = R_{\mathrm{ref,HEMT}} \cdot (0.832 + 0.006 \cdot T_{\mathrm{j}} + 1.773 \cdot 10^{-5} \cdot T_{\mathrm{j}}^2) \quad (3.6)$$

$$R_{\mathrm{ds,GIT}}(T_{\mathrm{j}}) = R_{\mathrm{ref,GIT}} \cdot (0.840 + 0.006 \cdot T_{\mathrm{j}} + 1.366 \cdot 10^{-5} \cdot T_{\mathrm{j}}^2) \quad (3.7)$$
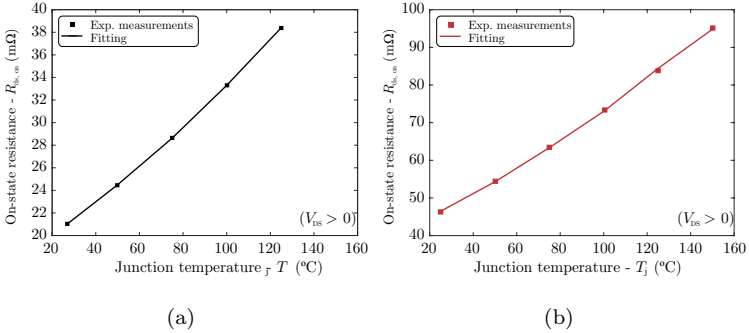
Figure 3.15: Experimental on-state resistance in relation to junction temperature [54]: (a) GaN HEMT and (b) GaN GIT.

It has to be noted that even if $R_{\mathrm{ds,TOP}}$ is lower than $R_{\mathrm{ds,BOT}}$ the same amount of power losses are considered for the comparison of cooling configurations.

Performance comparison

Regarding the performance comparison, a controlled current I_d is conducted through high-side and low side paralleled devices resulting on distributed thermal dissipation. Thermal images of bottom layers validate a well distributed heat dissipation through paralleled devices, as it is illustrated in Figure 3.16 for three configurations.

(a)

(b)

(c)
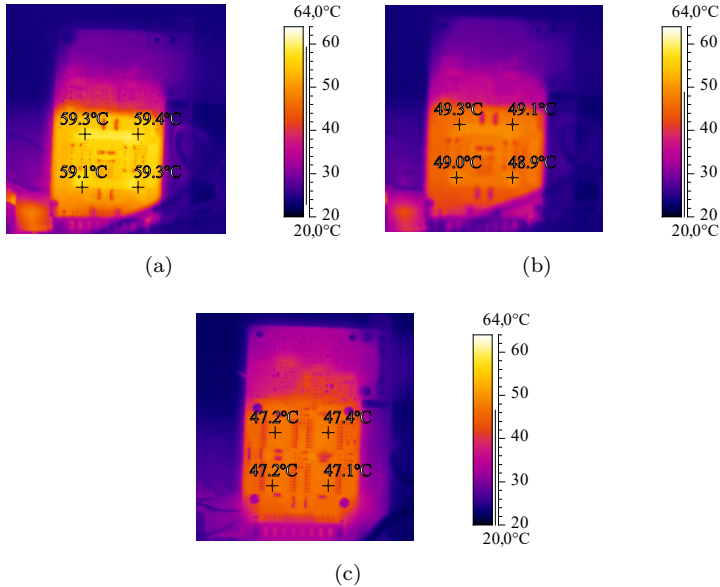
Figure 3.16: Top and bottom cooling power boards thermal comparison (P_{diss}=8 W): (a) power board based on top-side cooled devices, (b) power board based on top-side cooled devices with heat-spreading material and (c) power board based on bottom-side cooled devices.

Moreover, measuring the voltage drop (v_{TOP} and v_{BOT}) and the controlled current I_{DS}, $R_{ds,on}$ is obtained, and thus solving (3.6),(3.7) T_j is estimated.

Then, junction temperature in function of power losses is obtained, defining the allowed maximum power losses at $T_j = 150\,°C$, as it is depicted in Figure 3.17(a). For the same power losses, the junction temperature of the bottom cooled variant is lower, as a result of a better thermal management.

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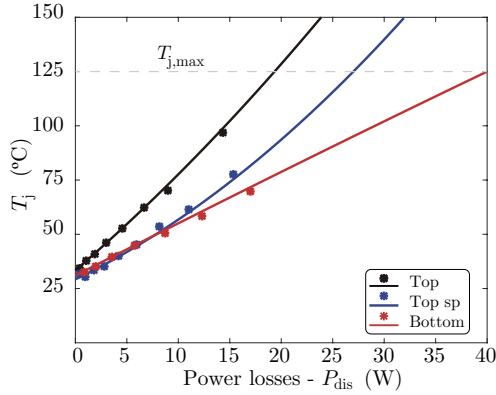
(a)
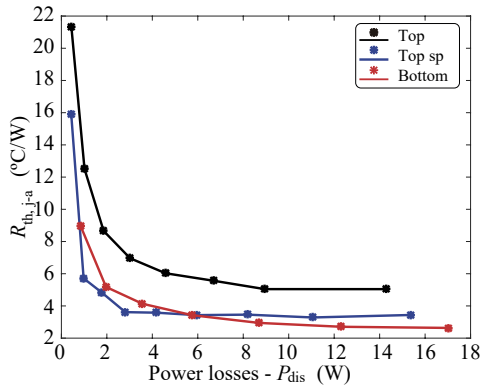
(b)

Figure 3.17: Comparison of thermal distribution of different cooling so-
lutions ($P_{\mathrm{dis}}=8\,\mathrm{W}$): Top and bottom cooling power boards thermal perfor-
mance indicators based on experimental measurements: (a) T_{j} estimation
and (b) total junction-to-ambient thermal resistance.

The total $R_{\mathrm{th,j-a}}$ of different configurations is derived from the mea-
sured ambient and estimated junction temperature. In Figure 3.17(b)
bottom cooled configuration appears as the best cooling solution, with
a reduction of 40% of thermal resistance at 14 W power losses.

Comparing the thermal resistance distribution, a good matching

between the theoretical and experimental results is observed for the top-cooled solution in Figure 3.18. However, as bottom-cooled variant presents a more complex system the estimation results in a higher difference between experimental and theoretical analysis.

In addition, spreading material placed between device active area and TIM increases the TIM active area, reducing the impact of this material resistance. This solution results on a reduction of the TIM resistance by 75%, comparing Top configuration with Top-sp solution (see Figure 3.18). Moreover, the use of Cu inlay with laser vias, along with heat-spreading, results on low PCB thermal resistance and a reduced impact of TIM resistance.
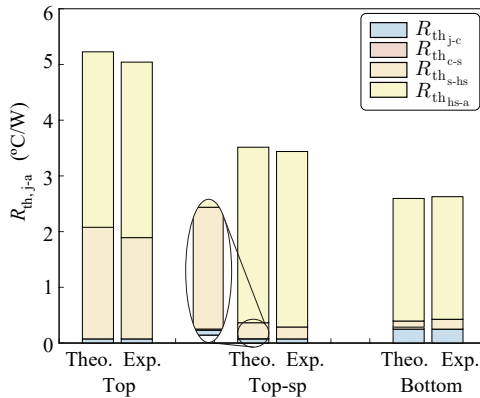
Figure 3.18: Thermal resistance distribution for three analyzed cooling configurations (P_{diss}=14 W): top-side cooling (Top), top-side cooling with spreading (Top-sp) and bottom-side cooling (Bot).

The main difference of both solutions, without considering heatsink-to-ambient resistance, is related to the resistance between the device thermal pad and the heatsink. Although bottom cooled has the impact of the Cu inlay resistance, the increase of the contact area reduces the TIM thermal resistance, resulting in lower surface-to-heatsink resistance than in the top cooling configuration. Thus, when designing a thermal solution for GaN devices with such small package it is essential to increase the contact area to reduce the TIM resistance, being possible to increase the power dissipation capability, as it is depicted in Figure 3.18. Nevertheless, cooling through PCB requires a more complex manufacturing processes. Moreover, the use of a high conductivity

heat spreading reduces the impact of the surface-to-heatsink resistance
increasing the cooling capability of the top-side cooled variant.

Therefore, it is demonstrated that not only the use of a better
heatsink reduces the overall resistance but the reduction of the TIM
resistance on the bottom-cooled solution improves the thermal man-
agement performance (see Figure 3.18).

3.4 Power Losses Distribution

The main goal of this analysis is to define distribution of power losses
for the optimal implementation of GaN devices on medium/high-power
converters. Thus, half-bridge configuration with an inductive element
connected to the midpoint is evaluated. In this configuration, the in-
ductive current is formed by a fundamental current $i_o(t)$ and a current
ripple Δi, expressed as per-unit, at a switching frequency f_s, as it is
depicted in Figure 3.19 for different topologies. Moreover, when ana-
lyzing the switching transients, turn-on I_{on} and turn-off I_{off} currents
are differed:

$$\begin{aligned}
I_{on} &= i_o(t) - i_o(t) \cdot \Delta i \\
I_{off} &= i_o(t) + i_o(t) \cdot \Delta i
\end{aligned} \tag{3.8}$$

In the case of dc-dc converters $i_o(t)$ is a constant average current I_o.
For a synchronous buck converter, a triangular current with $i_o(t){=}I_o$,
I_{on} decreases with the current ripple, while I_{off} switching current in-
creases (3.8). On the contrary, for dc-ac, $i_o(t)$ is a sinusoidal current
with a peak amplitude of I_o at a fundamental frequency f_o. Neverthe-
less, an equivalent theoretical analysis of power losses can be presented
considering an inductive triangular current.

The design space, which is conformed by Δi, N_p, f_s, $t_{dt,on}$ and
$t_{dt,off}$, is used for the evaluation of the converter performance. Variation
of the current ripple not only affects to power losses, but also results
on different operation modes, as it is depicted in Figure 3.20. Low
current ripple ($\Delta i{<}1$) presents hard-switching for both commutations
(turn-on and turn-off), whereas an increase of the current ripple can
result on soft-switching operation. If the current ripple is equal to
I_o ($\Delta i{=}1$), Zero-Current Switching (ZCS) is achieved, being turn-on
switching losses only related to the output capacitance ($E_{on}{=}E_{oss}$).
Besides, if the current ripple is increased until I_{on} is negative, ZVS
transition can be accomplished, if dead-time is long enough.

(a)

(b)
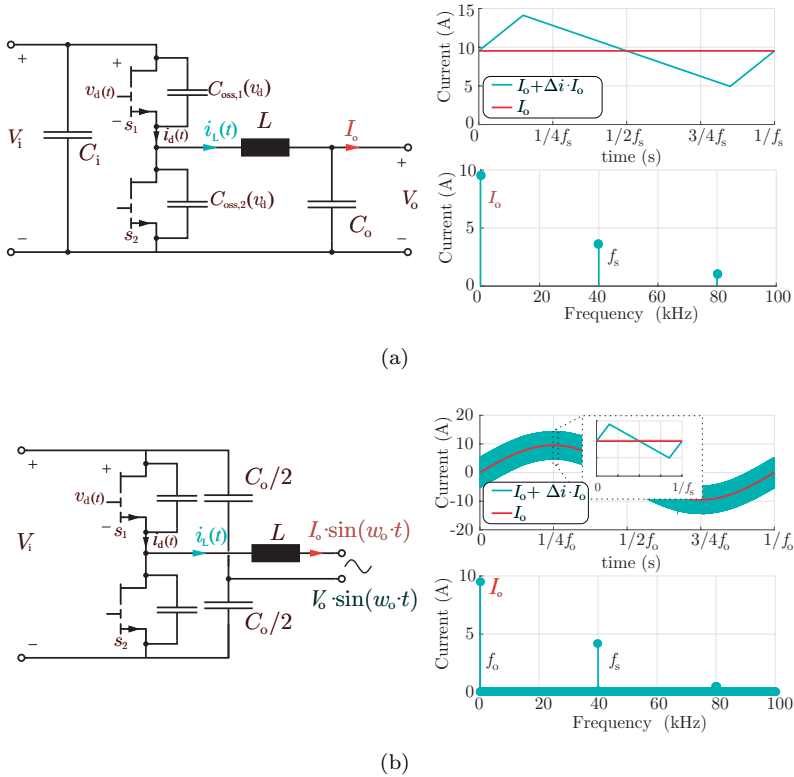
Figure 3.19: Half-bridge configuration for different topologies: (a) dc-dc synchronous buck and (b) dc-ac single phase inverter.

Then, after defining a power losses model of semiconductors switching losses needs to be analyzed. Moreover, soft-switching transitions are evaluated, presenting an analytical ZVS model.

3.4.1 Switching losses

Once switching characteristics have been analyzed in Section 2.2.2, switching transients are evaluated in order to define switching losses distribution. Switching losses are evaluated through SPICE models and DPT. Moreover, reverse recovery energy is negligible for GaN devices and it is not considered as a part of turn-on losses. Besides, scaling

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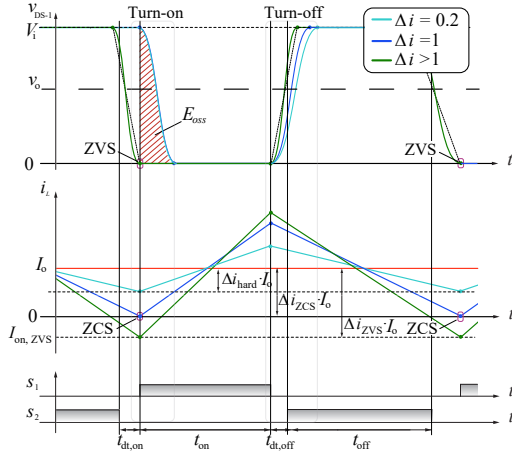
Figure 3.20: Current ripple influence on the operation mode of a synchronous buck converter: hard-switching (0.2), zero-current-switching ZCS (1) and zero-voltage-switching ZVS (>1).

methods are defined in order to obtain switching losses for different operating conditions.

For this analysis, stray inductance of GaN devices [108] and power board layout characteristics [44] are considered, which are summarized in Table 3.5.

Table 3.5: Parasitics related to package and converter layout.

Package parasitics [108]	Value	Unit
Gate stray inductance - L_G	3	nH
Drain stray inductance - L_D	0.8	nH
Source stray inductance - L_S	0.3	nH
Converter typical parasitics [44]	**Value**	**Unit**
Power loop stray inductance - L_{loop}	2	nH
Power loop stray resistor - R_{loop}	1.2	mΩ
Gate loop stray inductance - $L_{G,loop}$	5	nH

Analysis of switching transients

A typical hard-switching transition consist of turn-on and turn-off transient. For the analysis, a DPT is performed, dividing turn-on and turn-off transients into four stages: turn-on delay, turn-on main transition, turn-off delay and turn-off main transition.

1. *Turn-on delay - $t_{on,1}$:*

   During this interval, the C_{GS} is charged until it reaches V_{th}. As the semiconductor is in open state, there is not current flowing through the channel, an the current is flowing through high-side semiconductor [see Figure 3.21(a)]. Hence, during this delay period only gate characteristics needs to be considered until V_{GS} reaches V_{th} and turn-on main transition begins.

2. *Turn-on main transition - $t_{on,1}$:*

   With the beginning of turn-on transition, the device starts conducting according to V_{GS} and (2.4). This transition ends when either V_{DS} decreases to zero or I_d gets the load current. V_{DS} tends to drop first, mainly due to high-switching capability of GaN devices and considering small gate resistance, low stray inductance or high load current [130]. On the contrary, I_d would reach first the load current. Moreover, as a result of negligible Q_{rr} GaN devices presents a relatively clean turn-on current. Nevertheless, a current bump is observed when turning on GaN devices, as it is depicted in Figure 3.21. This overcurrent is mainly generated by the charging/discharging current from parasitic capacitors C_{oss} [see Figure 3.21(a)].

3. *Turn-off delay - $t_{off,1}$:*

   As occurs in the turn-on transient, there is a delay period until turn-off main transient begins. When the gate signal is set to zero the C_{iss} of the semiconductors is discharged, until V_{GS} decreases to $V_{th} + \frac{I_d}{g_m}$. In this interval the current is flowing the main switch, as it is shown in Figure 3.22(a).

4. *Turn-off main transition - $t_{off,2}$:*

   Then, turn-off main transition begins with $V_{GS}=V_{th} + \frac{I_d}{g_m}$ and ends when V_{DS} reaches bus voltage or I_d drops to zero. As occurs for main turn-on transition to determine which of them occurs

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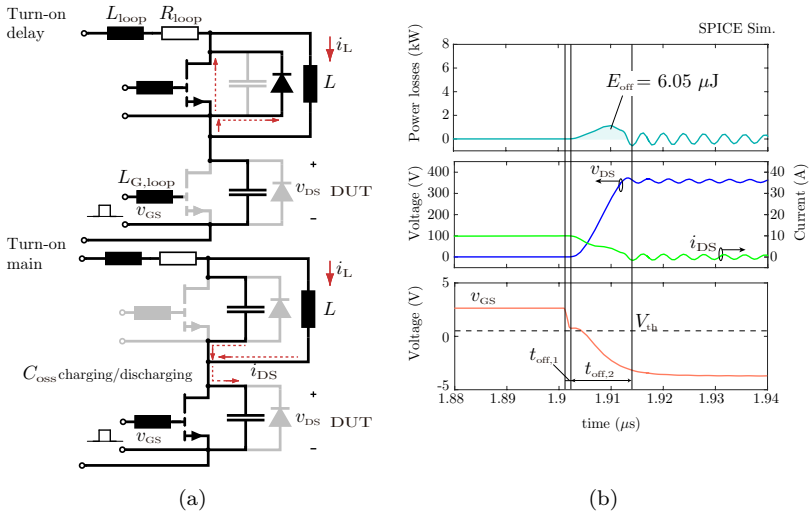
Figure 3.21: Turn-on switching transition for a DPT test (350 V/10 A) of
the IGO60R070D1 [108]: (a) equivalent scheme of turn-on delay and turn-
on main transition, and (b) switching energy, drain-to-source voltage and
current, along with the gate-to source voltage.

first the gate resistance, stray inductance and load current needs
to be analyzed. Moreover, turn-off losses are lower comparing to
turn-on ones for the same voltage and current requirement as it
is depicted in Figure 3.22.

In this case ringing periods are not considered, as the produced losses
can be neglected [130] (see Figure 3.21-3.22). In addition DPT is per-
formed for different operation conditions, in order to evaluated the influ-
ence of switching current, switching voltage and junction temperature
on switching losses.

Scaling and approximation

On the one hand, the voltage increase results on a proportional increase
of turn-on and turn-off losses, as it is depicted in Figure 3.23(a). Then,
scaling approximations are obtained for V_d considering a reference swit-
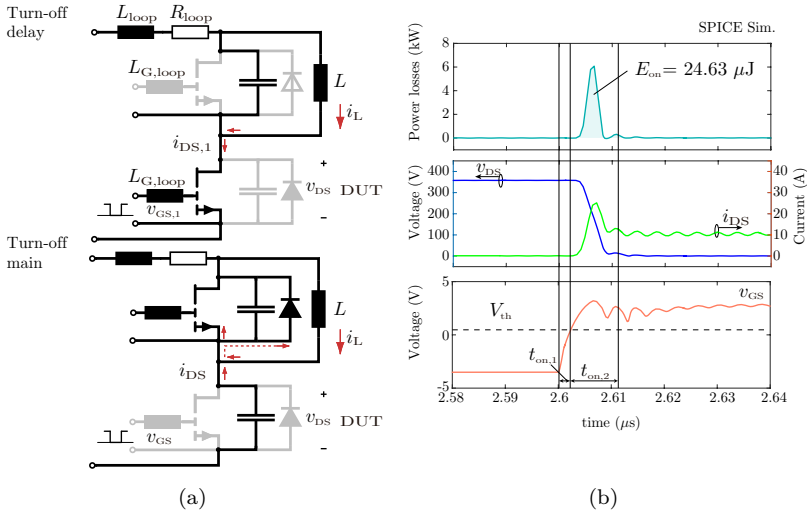
Figure 3.22: Turn-off switching transition for a DPT test ($350\,\mathrm{V}/10\,\mathrm{A}$) of the IGO60R070D1 [108]: (a) equivalent scheme of turn-off delay and turn-off main transition, and (b) switching energy, drain-to-source voltage and current, along with the gate-to source voltage.

ching voltage $V_{\mathrm{d,ref}}$

$$
\begin{aligned}
E_{\mathrm{on}}(V_{\mathrm{d}}) &= E_{\mathrm{on}}(V_{\mathrm{d,ref}}) \cdot \frac{V_{\mathrm{d}}}{V_{\mathrm{d,ref}}}, \\[2mm]
E_{\mathrm{off}}(V_{\mathrm{d}}) &= E_{\mathrm{off}}(V_{\mathrm{d,ref}}) \cdot \frac{V_{\mathrm{d}}}{V_{\mathrm{d,ref}}}.
\end{aligned}
\tag{3.9}
$$

On the other hand, Figure 3.23(b) shows the impact of T_{j} at different current values. The increase of the temperature results on higher turn-on energy. Otherwise, the impact of T_{j} is negligible for turn-off characteristic as it is depicted in Figure 3.23(b). This is a result of the impact of T_{j} on the transconductance. Therefore, an approximation to the effect of T_{j} on the turn-on energy is obtained with (3.10) considering

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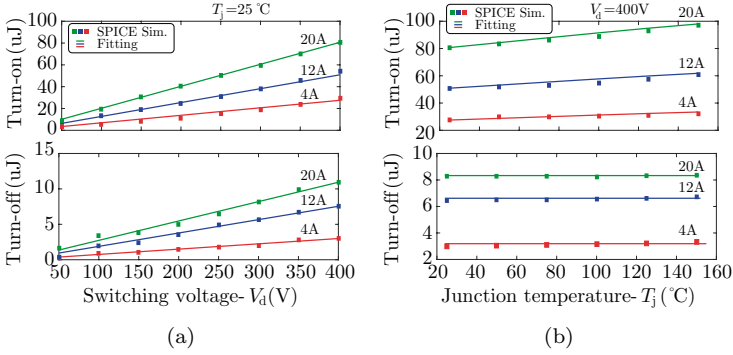
Figure 3.23: Scaling approximations of switching energy: (a) the impact
of different switching voltage V_d and (b) different T_j.

the transconductance relation with T_j presented in Figure 2.6.

$$E_{on}(Tj) = E_{on}(25C^\circ) \cdot k_{gm} \quad \text{where} \quad k_{gm} = \sqrt{\frac{g_m(T_j)}{g_m(25C^\circ)}} \qquad (3.10)$$

where the transconductance variation $g_m(T_j)$ is approximated with
(2.5).

This effect has not a high impact on switching energy, as it is shown
in Figure 3.23(b) and will be analyzed hereafter.

Figure 2.10 shows that GaN devices present a high difference be-
tween turn-on and turn-off switching energies. Then, the impact of
these difference is analyzed. An approximation of E_{on} and E_{off} for a
given V_d voltage is made using a second order polynomial, considering
N_p number of devices and T_j=25°C.

$$E_d = \left(c_d \cdot \left(\frac{I_d}{N_p} \right)^2 + b_d \cdot \frac{I_d}{N_p} + a_d \right) \cdot N_p$$
$$= \frac{c_d}{N_p} \cdot I_d{}^2 + b_d \cdot I_d + a_d \cdot N_p \qquad (3.11)$$

being I_d the switching current, I_{on} for turn-on and I_{off} for turn-off
transient.

Hence, considering switching energies distribution presented in Fig-
ure 2.10 and the second order fitting (3.11), the term which is inde-

pendent of the current (a_{on}) is related to the energy of the voltage-dependent output capacitor $C_{\mathrm{oss}}(v_{\mathrm{d}})$ charge (3.12).

$$a_{\mathrm{on}} \approx N_{\mathrm{p}} \cdot C_{\mathrm{Q,eq}}(V_{\mathrm{d}}) \cdot V_{\mathrm{d}}^2 \tag{3.12}$$

considering the same C_{oss} for high-side and low-side devices and the equivalent charge capacitance (2.6).

On the contrary, as for the turn-off transient $E_{\mathrm{oss}}(v_{\mathrm{d}})$ is not part of turn-off energy, all turn-off losses are related to the $v_{\mathrm{d}}(t)$ and $i_{\mathrm{d}}(t)$ overlapping ($a_{\mathrm{off}} = 0\mu\mathrm{J}$).

Considering turn-on and turn-off approximation terms (3.11), switching energy E_{s} per device is obtained as a function of current ripple Δi and N_{p} number of devices. Besides, it is assumed a turn-on current (I_{on}) that decreases with Δi and a turn-off current (I_{off}) that increases with Δi [120].

$$E_{\mathrm{s}} = (\Delta i \cdot I_{\mathrm{o}})^2 \cdot \frac{c_{\mathrm{off}} + c_{\mathrm{on}}}{N_{\mathrm{p}}}$$
$$+ \Delta i \cdot I_{\mathrm{o}} \cdot \left(2 \cdot I_{\mathrm{o}} \cdot \frac{c_{\mathrm{off}} - c_{\mathrm{on}}}{N_{\mathrm{p}}} + b_{\mathrm{off}} - b_{\mathrm{on}} \right) + \gamma \tag{3.13}$$

being γ the factor which is independent of the current ripple

$$\gamma = N_{\mathrm{p}} \cdot Q_{\mathrm{oss}} \cdot V_{\mathrm{d}} + \frac{I_{\mathrm{o}}^2 \cdot (c_{\mathrm{off}} + c_{\mathrm{on}})}{N_{\mathrm{p}}} + I_{\mathrm{o}} \cdot (b_{\mathrm{off}} + b_{\mathrm{on}}). \tag{3.14}$$

Turn-on and turn-off energy curves present a linear tendency, as it can be deduced from Figure 2.10. Hence, as $b_{\mathrm{on}} >> c_{on}$ and $b_{\mathrm{off}} >> c_{\mathrm{off}}$, the total switching losses can be simplified to (3.15).

$$E_{\mathrm{s}} \approx \underbrace{I_{\mathrm{o}} \cdot [(1 - \Delta i) \cdot b_{\mathrm{on}}] + N_{\mathrm{p}} \cdot C_{\mathrm{Q,eq}}(V_{\mathrm{d}}) \cdot V_{\mathrm{d}}^2}_{E_{\mathrm{on}}}$$
$$+ \underbrace{I_{\mathrm{o}} \cdot [(1 + \Delta i) \cdot b_{\mathrm{off}}]}_{E_{\mathrm{off}}} \tag{3.15}$$

Therefore, if b_{on} is bigger than b_{off}, total switching energies are reduced when Δi increases. This assumption is valid for GaN switches, which present higher turn-on than turn-off losses (see Figure 2.10). Furthermore, the switching losses also increase with the output capacitor charge for N_{p} number of devices (3.15).

It has to be noted that, in order to avoid switching losses related to
output capacitor the converter needs to be operated under ZVS condi-
tions.

3.4.2   Soft-switching losses: ZVS

In a half-bridge with an inductive component connected to the mid-
point (see Figure 3.19) ZVS can be achieved. Analyzing the half-bridge
with s_1 and s_2, when s_2 is conducting and the output capacitance of s_1
(C_{oss_1}) is charged to V_i. Then, when turning-off s_2, all the switches are
in open-sate and the current flows free-wheeling diodes. This current
discharges C_{oss_1} and transfers the energy to C_{oss_2}. If the inductive en-
ergy is high enough within an open-state time interval ZVS is achieved,
as it is depicted in Figure 3.24(a).

Hence, ZVS operation requires a negative current $I_{\text{on,ZVS}}$ of the
inductive component (L), that charges/discharges output capacitances
(C_{oss_1},C_{oss_2}) within dead-time $t_{\text{dt,on}}$ as it is depicted in Figure 3.24(a).

The required energy for ZVS can be derived from the energy balance
presented in [110]

$$E_{\text{init.}} + E_{\text{del.}} = E_{\text{fin.}} + E_{\text{dis.}} \tag{3.16}$$

Moreover, in this work the influence of N_{p} paralleled devices is con-
sidered. Then, the energy balance is solved, for the following conditions:

▶ Initial energy: $E_{\text{init.}} = \dfrac{1}{2} \cdot L \cdot I_{\text{on,ZVS}}^2 + E_{\text{oss}}(V_{\text{d}}) \cdot N_{\text{p}}$

▶ Delivered energy: $E_{\text{del.}} = -Q_{\text{oss}}(V_{\text{d}}) \cdot V_{\text{d}} \cdot N_{\text{p}}$

▶ Final energy: $E_{\text{fin.}} = E_{\text{oss}}(V_{\text{d}}) \cdot N_{\text{p}}$

▶ Dissipated energy: $E_{\text{dis.}} = 0$

$$\frac{1}{2} \cdot L \cdot I_{\text{on,ZVS}}^2 > N_{\text{p}} \cdot C_{\text{Q,eq}} \cdot V_{\text{d}}^2 \tag{3.17}$$

However, if conditions presented before are not fulfilled, incomplete
Zero-Voltage Switching (iZVS) occurs [see Figure 3.24(b)]. This means
that the top side switch turns-on before the resonant transition ends
with a voltage ΔV [110]. Indeed, dead-time is so small that the energy
will not be transmitted between the capacitors before the semiconductor
is turned on.
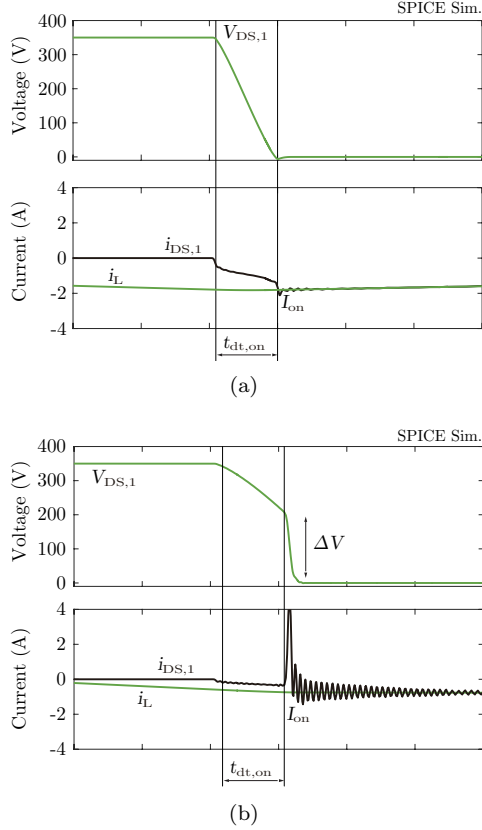
Figure 3.24: ZVS transitions for different turn-on current conditions: (a) complete ZVS and (b) incomplete ZVS due to low turn-on current within an insufficient turn-on dead-time.

Therefore, a resonant analysis of the circuit is performed, in order to define $t_{\mathrm{dt,on}}$ and $I_{\mathrm{on,ZVS}}$ more precisely. ZVS is achieved if the switch node voltage of the high-side device $[v_{\mathrm{d,1}}(t)]$ excess input voltage V_{i}, turning-on the body diode of s_1 [120].Then, the current for ZVS operation is obtained by (3.18) within a dead-time $t_{\mathrm{dt,ZVS}}$

$$I_{\mathrm{on,ZVS}} > \sqrt{\frac{2 \cdot C_{\mathrm{Q,eq}} \cdot V_{\mathrm{i}}(V_{\mathrm{i}} - 2V_{\mathrm{o}})N_{\mathrm{p}}}{L}}, \tag{3.18}$$

81

$$t_{\text{dt,ZVS}} = \frac{1}{\omega_{\text{r}}} \left(\tan^{-1} \left(\frac{V_{\text{o}}}{I_{\text{on,ZVS}}} \right) + \frac{\pi}{2} \right)$$

$$\text{where} \quad \omega_{\text{r}} = \sqrt{\frac{1}{2 \cdot L \cdot C_{\text{Q,eq}}}}$$

(3.19)

Moreover, the effect of dead-time $t_{\text{dt,on}}$ on the energy dissipated during dead-time $[E_{\text{dis.,dt}}(t_{\text{dt,on}})]$ is assumed to be linear. In this case with the $t_{\text{dt,ZVS}}$ obtained with (3.19) complete ZVS is achieved. Then, for $t_{\text{dt,ZVS}}$ the ΔV is zero and thus $E_{\text{dis.,dt}}(t_{\text{dt,ZVS}})$ is calculated to be

$$E_{\text{dis.,dt}} = N_{\text{p}} \cdot C_{\text{Q,eq}} \cdot V_{\text{d}}^2 - \frac{1}{2} \cdot L \cdot I_{\text{on,ZVS}}^2$$

(3.20)

Thus, expressions for iZVS presented in [110] are revised including the effect of dead-time (3.20). Then, solving the energy balance (3.16), ΔV can be calculated with (2.6) and (2.7) equivalent capacitances, for the following conditions:

▶ Initial energy: $E_{\text{init.}} = \frac{1}{2} \cdot L \cdot I_{\text{on,ZVS}}^2 + E_{\text{oss}}(V_{\text{d}}) \cdot N_{\text{p}} + E_{\text{dis.,dt}}(t_{\text{dt,on}})$

▶ Delivered energy: $E_{\text{del.}} = - [Q_{\text{oss}}(V_{\text{d}}) - Q_{\text{oss}}(\Delta V)] \cdot V_{\text{d}} \cdot N_{\text{p}}$

▶ Final energy: $E_{\text{fin.}} = [E_{\text{oss}}(V_{\text{d}} - \Delta V) + E_{\text{oss}}(\Delta V)] \cdot N_{\text{p}}$

▶ Dissipated energy: $E_{\text{dis.}} = 0$

Thus, if complete ZVS transition is achieved, with a $I_{\text{on,ZVS}}$ within a $t_{\text{dt,ZVS}}$, the ΔV yields zero. Once ΔV is obtained, the dissipated energy related to ΔV is calculated with (3.21).

$$E_{\text{dis.,iZVS}} = [E_{\text{oss}}(\Delta V) + (Q_{\text{oss}}(V_{\text{d}}) - Q_{\text{oss}}(V_{\text{d}} - \Delta V)) \cdot V_{\text{d}}$$
$$+ E_{\text{oss}}(\Delta V) - E_{\text{oss}}(V_{\text{d}} - \Delta V)] \cdot N_{\text{p}}$$

(3.21)

Hence, a trade-off between $I_{\text{on,ZVS}}$ and $t_{\text{dt,ZVS}}$ needs to be considered. Figure 3.25 shows how the higher $t_{\text{dt,ZVS}}$ the lower $I_{\text{on,ZVS}}$ is needed in order to achieve ZVS transitions.

3.4.3 Power losses model

The power losses of semiconductors are calculated with the characteristics presented in Section 2.2 and considering the topology waveforms
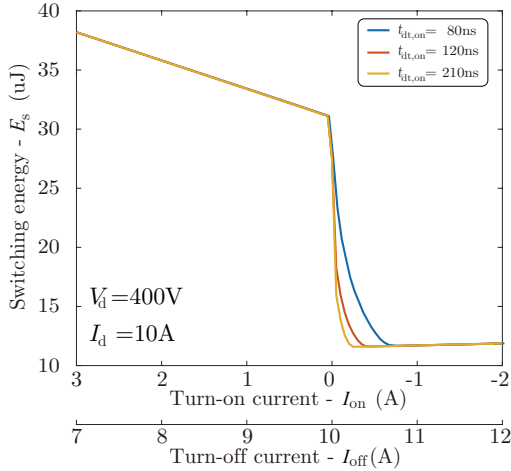
Figure 3.25: Switching losses for different turn-on currents within various dead-times, achieving ZVS.

(see Figure 3.26). Semiconductor conduction, switching and gate characteristics are obtained from SPICE simulations, as it is analyzed in Section 2.2. Then, design parameters such as the Δi, f_s, N_p and dead-time are considered in order to calculate the losses. Moreover, a ZVS model defined in Section 2.2 will be validated when operating at high Δi.
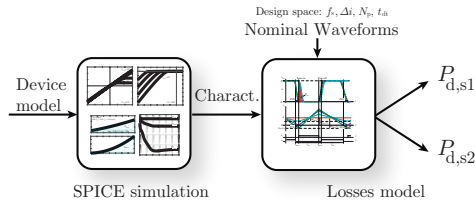
Figure 3.26: Power losses estimation procedure applied to GaN devices in half-bridge configuration.

Conduction losses

Conduction losses are related to conduction resistance $R_{\mathrm{ds,on}}$ and the Root Means Square (RMS) current through high-side (s_1) and low-side (s_2) devices (see Figure 3.19). For the total conduction losses the current can be approximated to the RMS current of the output inductor L

$$I_{\mathrm{rms}} = \sqrt{I_{\mathrm{o}}^2 + (I_{\mathrm{o}} \cdot \Delta i)^2 / 3} \qquad (3.22)$$

Moreover, it is a well-known fact that conduction losses are scaled down with N_{p} number of switches connected in parallel, resulting in lower conduction losses according to (3.23).

$$
\begin{aligned}
P_{\mathrm{c}} &= I_{\mathrm{rms}}^2 \cdot R_{\mathrm{ds,on}}(T_{\mathrm{j}})/N_{\mathrm{p}} \\
&= R_{\mathrm{ds,on}}(T_{\mathrm{j}}) \cdot (1 + \frac{\Delta i^2}{3}) \cdot \frac{I_{\mathrm{o}}^2}{N_{\mathrm{p}}}
\end{aligned}
\qquad (3.23)
$$

where $R_{\mathrm{ds,on}}$ is dependent on T_{j} and I_{d} as it is shown in Figure 2.3(b). However, as $R_{\mathrm{ds,on}}$ presents a weak variation with respect to I_{d}, this effect is not considered, simplifying the analysis.

Dead-time losses

In a half-bridge configuration a minimum dead-time was selected to prevent simultaneous conduction of both switches, also known as shoot-through (see Section 2.3). Two conduction instances are differenced, as it is depicted in Figure 3.27: turn-on dead-time ($t_{\mathrm{dt,on}}$) and turn-off dead-time ($t_{\mathrm{dt,off}}$). Dead-time losses of these transients are obtained from the free-wheeling reverse conduction characteristic [see Figure 2.4(b)] and the ratio between conduction times ($t_{\mathrm{dt,on}}, t_{\mathrm{dt,off}}$) and switching period ($1/f_{\mathrm{s}}$).

$$
\begin{aligned}
P_{\mathrm{dt}} &= \underbrace{\frac{[V_{\mathrm{SD,on}} \cdot I_{\mathrm{on}} \cdot t_{\mathrm{dt,on}} + V_{\mathrm{SD,off}} \cdot I_{\mathrm{off}} \cdot t_{\mathrm{dt,off}}]}{N_{\mathrm{p}}}}_{E_{\mathrm{dt}}} \cdot f_{\mathrm{s}} \\
&= \frac{V_{\mathrm{SD,on}} \cdot t_{\mathrm{dt,on}} \cdot (1 - \Delta i) + V_{\mathrm{SD,off}} \cdot t_{\mathrm{dt,off}} \cdot (1 + \Delta i)}{N_{\mathrm{p}}} \cdot I_{\mathrm{o}} \cdot f_{\mathrm{s}}
\end{aligned}
\qquad (3.24)
$$

where $V_{\mathrm{SD,on}}$ and $V_{\mathrm{SD,off}}$ are the reverse drain-to-source voltage drop for the switching currents I_{on} and I_{off}, respectively.
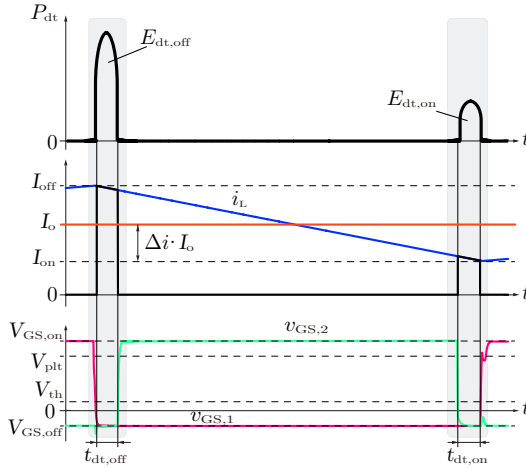
Figure 3.27: Dead-time conduction instances and energy (E_{dt}) on a synchronous buck converter, being s_1 high side switch and s_2 low side switch).

Figure 3.27 shows the conduction energy related to dead-time instances. These losses will be relevant at high $t_{dt} \cdot f_s$ ratio for devices with high V_{SD}, such as GaN devices (see Figure 2.4). Besides, a negative gate-to-source turn-off voltage ($V_{GS,off} < 0\,\text{V}$) is preferred for GaN devices in order to avoid false turn-on as it was analyzed in Section 2.5. However, the use of negative turn-off voltage increases the V_{SD} (2.3), resulting in higher dead-time losses.

Moreover, the impact of dead-time control strategies is shown in Figure 3.28. Large dead-times are required in most cases for ZVS. As it is previously analyzed in Section 3.4.2, a trade-off between $I_{on,ZVS}$ and $t_{dt,ZVS}$ needs to be considered in order to achieve ZVS transition (3.17). For the analyzed buck converter dead-time $t_{dt,ZVS}$ is related to $t_{dt,on}$ while $I_{on,ZVS}$ is related to Δi (3.26).

Then, different dead-time control strategies are defined depending on the current ripple. For low current ripples ($\Delta i \leq 1$), symmetrical minimum dead-time is selected, maintaining the minimum dead-time calculated with (3.19) for both transients. However, for ZVS operation ($\Delta i > 1$) only turn-on dead-time is increased to achieve ZVS operation, as it is depicted in Figure 3.28.

85
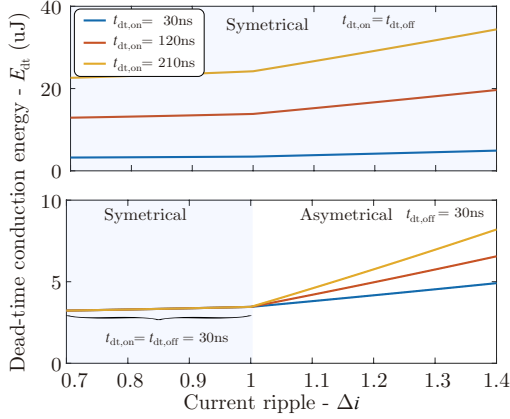
Figure 3.28: Symmetrical and asymmetrical dead-time control strategies for the reduction of dead-time losses impact.

Switching losses

Switching losses for a hard-switching transition consist of turn-on and turn-off losses, which are proportional to switching frequency f_s and can be scaled with the switched voltage V_d for a switching voltage reference $V_{d,ref}$ and T_j, derived from (3.9) and (3.10).

$$P_s(V_d) = [E_{on}(I_{on}, V_{d,ref}, 25°C) \cdot k_{gm} + E_{off}(I_{off}, V_{d,ref})] \cdot f_s \cdot \frac{V_d}{V_{d,ref}} \quad (3.25)$$

Considering the influence of T_j on turn-on energy, the energy at 25°C is multiplied by the factor k_{gm} obtained with (3.10). Besides, as occurs in all configurations with an inductive element connected to the midpoint of a half-bridge, ZVS transition can be achieved, if ZVS conditions are accomplished, as it is presented in Section 2.4.

3.4.4 Theoretical performance evaluation

The performance of these operation modes along with the impact of the design space needs to be analyzed in order to define GaN devices optimal operation conditions. Moreover, the impact of f_s, N_p and dead-times needs to be evaluated.

Considering the power losses breakdown evaluated in Section 3.4,

power losses of GaN devices are analyzed on a synchronous buck converter for the specifications and design space shown in Table 3.6.

Table 3.6: Synchronous buck electrical specifications.

Specifications	Value	
Input voltage - V_i	350	V
Output voltage - V_o	245	V
Output current - I_o	10	A
Junction temperature - T_j	120	℃
Design space		
Current ripple - Δi	0.2-1.2	
Switching frequency - f_s	10-1000	kHz
Number of devices in parallel - N_p	1 and 2	

Semiconductors losses are evaluated for junction temperature of 120 ℃. Switching energies presented in Figure 3.23, along with the analytical expressions for ZVS operation (3.21) are considered for switching losses estimation. Besides, asymmetrical dead-time control is performed with the minimum dead-time calculated with (3.19) (85 ns) for $\Delta i \leq 1$ and with (3.19) for ZVS operation, which depends on the inductor energy and the current ripple, among others. The current ripple and switching frequency influence is evaluated comparing single device with two parallel-connected devices.

Current ripple variation

For the current ripple analysis, a switching frequency of 100 kHz and an output current of 10 A with a duty cycle of 0.7 are considered. Figure 3.29 shows the losses breakdown in function of current ripple, number of devices and dead-time. Conduction losses increase with higher current ripples while switching losses reduce. The reduction of switching losses is mainly due to lower turn-on switching currents along with the great difference between turn-on and turn-off energy of GaN devices (see Figure 2.10).

Moreover, paralleling devices results on higher power losses for low current ripples, as a consequence of hard-switching operation. Nevertheless, the lower the relevance of switching losses is, the lower total power losses of paralleled-devices are in comparison with single devices

(see Figure 3.29). Regarding dead-time losses, the use of asymmetrical dead-time control results on low relevance of dead-time losses. In addition, minimum Δi is preferred, in order to avoid losses produced by high-current ripples. However, an excessive dead-time will be a key contributor on losses, as a consequence of the freewheeling conduction characteristic of GaN devices (see Figure 2.4). Thus, for ZVS operation, asymmetrical dead-time control with higher dead-time values is recommended in order to reduce total power losses, as it is shown in Figure 3.29.
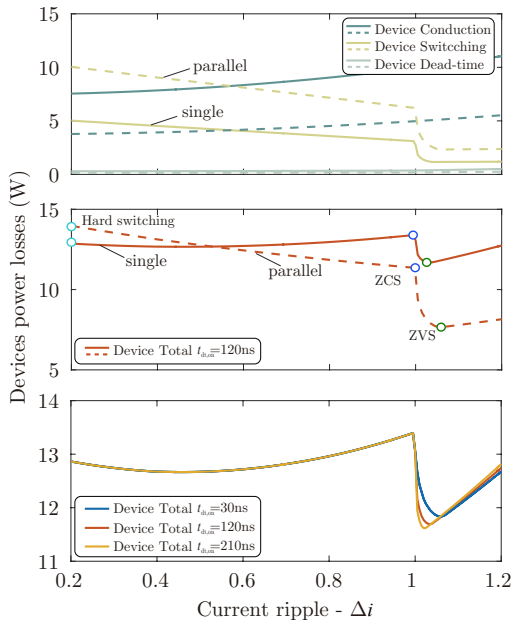
Figure 3.29: Analysis of devices power losses, comparing single (continuous lines) with parallel-connected (dashed lines) for different dead-times (t_{dt}) and varying the current ripple

Switching frequency variation

Switching frequency influence is also evaluated under the same operation conditions for the three current ripples which provide three different

operation modes: $\Delta i_{\text{hard}} = 0.2$, $\Delta i_{\text{ZCS}} = 1$ and $\Delta i_{\text{ZVS}} > 1$.

$$\Delta i_{\text{ZVS}} = 1 + \frac{|I_{\text{on,ZVS}}|}{I_{\text{o}}} \tag{3.26}$$

being $I_{\text{on,ZVS}}$ defined for achieving ZVS within $t_{\text{dt,ZVS}}$ (3.19).

Δi_{ZCS} presents similar performance than low current ripple for low switching frequencies and higher losses than Δi_{ZVS} for high switching frequencies (see Figure 3.30). Thus, only two current ripples will be considered for following analyses, i.e. 0.2 and Δi_{ZVS}. Moreover, Figure 3.30 shows that for low switching frequencies ($<20\,\text{kHz}$), hard-switching operation presents the lowest power losses due to low relevance of switching losses along with low current ripple. However, as the switching frequency increases, switching losses become relevant, being ZVS operation the most suitable solution.
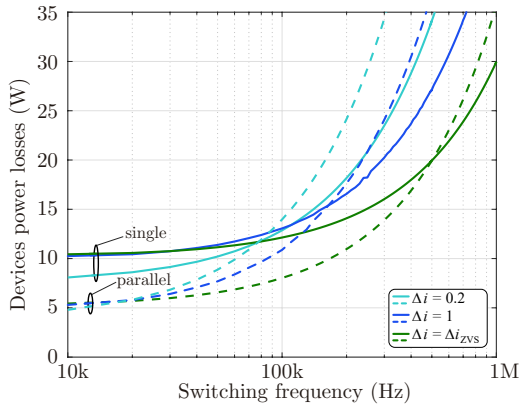
Figure 3.30: Analysis of devices power losses considering hard-switching (Δi=0.2), ZCS (Δi=1) and ZVS (Δi=Δi_{ZVS}), for various switching frequencies and comparing single (continuous lines) with parallel-connected (dashed lines).

In addition, paralleling devices results in lower power losses for high current ripple ($\Delta i > 1$) even for low switching frequencies. This is due to the relevance of conduction losses, which are reduced by the number of switches connected in parallel. Regarding parallelization for hard-switching operation, Figure 3.30 shows how for low switching frequencies ($f_{\text{s}} < 60\,\text{kHz}$) parallelization reduces devices losses. Nevertheless,

when operating at higher switching frequencies single devices results on
better performance.

Although obtained power losses are low, even for high-switching
frequencies, the thermal dissipation capability of GaN devices will play
a key roll when designing the whole power converter, as it is presented
in Section 3.3.

3.4.5 Power losses measurement

With the eruption of WBG devices, the performance of power convert-
ers is enhanced, reducing power losses. Hence, the exact determination
of power losses becomes more complex and relevant. Although different
methodologies have been proposed in the literature for accurate mea-
surement of power losses [128, 131, 132], in this work calorimetric test
at power converter level is presented.

Methods

The methods for the measurement of power losses are basically divided
in two groups: electrical and calorimetric (see Table 3.7). On the one
hand, electrical methods are based on measurement of voltage and cur-
rent of the Device Under Test (DUT). These methods, such as DPT
or input-output energy conservation analysis present the advantage of
reduced measurement time. For DPT, it is mandatory to use high-
precision probes. Special attention must be devoted to a precise align-
ment of probes due to high-switching speed of WBG devices [126]. It
has to be noted that measurement probes with bandwidths higher to
350 MHz are required for GaN devices, which present 5-30 ns rising and
falling times [126]. Moreover, the results obtained with this method
are questionable for soft-switching operation [128, 131]. Regarding the
energy conversion analysis other converter components losses have to
be subtracted from the total power losses, in order to obtain DUT
power losses. This procedure results in some cases in complex analy-
sis of converter losses [126]. Therefore, electrical measurements have
been demonstrated as low-medium accuracy measurements for WBG
devices, as it is analyzed in [131] for 10 kV SiC MOSFETs.

On the other hand, calorimetric methods determine the power losses
with the measurement of the dissipated heat on the DUT. Calorimet-
ric methods can be differed as steady-state-calorimetric and transient
calorimetric. Steady-state calorimetric methods present slow speed

in comparison with other methodologies. Moreover, with forced air cooling systems and air flow meters, the flow temperature difference is measured, obtaining 20-25 min./point speed [132]. However, the time consumed for this steady-state tests can not be compared to high speed measurements obtained by electrical measurements. Referring to transient-calorimetric, power losses are measured in a fast and accurate way. The method proposed in [131], achieves a low relative error even for soft-switching losses. However, special set-up is build along with brass block, which acts as thermal capacitance, neglecting the thermal resistance and therefore reducing the measuring time. Although both calorimetric methods present high accuracy, in most cases special set-ups were build in order to obtain these measurements.

Table 3.7: Comparison of different power losses measurement methods.

	Methods		Accuracy	Speed	Configuration
Elec.	DPT	[126]	Low	Fast	Half-bridge
	Energy conversion		Low	Fast	Converter
Calor.	Steady-State	[132]	High	Medium	Full-bridge + air flow
		[120]*	Medium	Medium	Converter
	Transient	[131]	High	Fast	Half-bridge + Brass block

* Proposed in this work

Converter level calorimetric method

In this work, a steady-state calorimetric measurement method is proposed for the experimental estimation of GaN switches power losses at power converter level. Heatsink and ambient temperatures are measured together with input and output power values [see Figure 3.13(a)]. As the heatsink has not a high thermal thermal constant ($\tau th = R_{\mathrm{th,hs}} \cdot C_{\mathrm{th,hs}}$) this measurement method is quite fast (20-30 min./point).

Devices power losses ($P_{\mathrm{d,loss}}$) are obtained from the thermal equivalent heatsink resistance $R_{\mathrm{th,hs}}$ and the measured heatsink-to-ambient temperature difference ($\triangle T_{\mathrm{hs}} = T_{\mathrm{hs}}$ - T_{a}) (3.27), when the thermal equilibrium is achieved.

$$P_{\mathrm{d,loss}} = \frac{\triangle T_{\mathrm{hs}}}{R_{\mathrm{th_{hs}}}} \tag{3.27}$$

Nevertheless, the measured point has to be calibrated by measurements in order to obtain the precise thermal resistance. This charac-

terization is similar to the one presented for the thermal limits eval-
uation in Section 3.3.2. A constant controlled current (I_d) is fed into
the power board, measuring $\triangle T_\mathrm{hs}$ for different controlled power levels.
Then, power losses for a measured $\triangle T_\mathrm{hs}$ are obtained [see Figure 3.31].
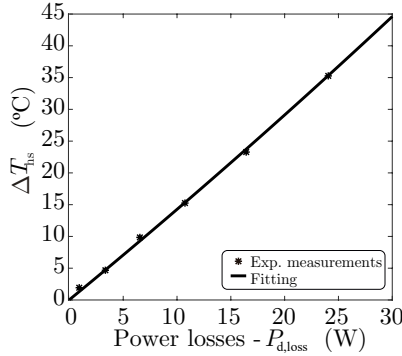
Figure 3.31: Experimental power losses measurement, relation between
the measured point temperature difference $\triangle T_\mathrm{hs}$ and power losses $P_\mathrm{d,loss}$.

The estimated $P_\mathrm{d,loss}$ consists of conduction P_c, switching P_s and P_dt
dead-time power losses. Measuring the RMS current of those switches
($I_\mathrm{d,rms}$) and with the $R_\mathrm{ds,on}(T_\mathrm{j})$, conduction losses are known and hence
the switching losses plus dead-time losses are obtained

$$P_\mathrm{s} + P_\mathrm{dt} = P_\mathrm{d,loss} - R_\mathrm{ds,on}(T_\mathrm{j}) \cdot I_\mathrm{d,rms}^2. \tag{3.28}$$

In addition, for the junction temperature T_j estimation, the on-
state resistance $[R_\mathrm{ds,on}(T_\mathrm{j})]$ will be used as TSEP, as it is proposed in
Section 3.3.2.

3.4.6 Experimental Results

In order to validate the theoretical analysis presented in Section 3.4.4,
the influence of different current ripples and switching frequencies on
power devices is experimentally measured. Moreover, the proposed
steady-state calorimetric method is validated.

Operation conditions

In Figure 3.32 the voltage of top device is depicted for three current ripples that achieve different operation modes: $\Delta i = 0.2$, $\Delta i = 1$ and $\Delta i > 1$. Low current ripple presents a hard-switching transition, as it is depicted in Figure 3.32(a). For the current ripple of 1 the switch-node voltage is not discharged and thus, a transition with ZCS is shown in Figure 3.32(b). On the contrary, for the ZVS current ripple, the depicted voltage v_{d1} shows up a complete soft-switching when ZVS conditions are accomplished [see Figure 3.32(c)].

The minimum $I_{on,ZVS}$ (3.18) and $t_{dt,ZVS}$ (3.19) are calculated for ZVS operation. Then, ZVS transition is fulfilled as it is shown in Figure 3.33. It is also demonstrated, that for lower dead-time an iZVS transition occurs as it is depicted in Figure 3.33(a). However, if dead-time increases up to $t_{dt,ZVS}$, complete ZVS is achieved [see Figure 3.33(b)].

GaN devices performance

Figure 3.34 shows a good match between theoretical and experimental measurements, considering the estimated junction temperature for each case. Power losses are evaluated at different junction temperatures and operation modes, resulting on a good agreement of conduction and switching losses with the ones obtained from the power losses model. Therefore, the considerations described in the power losses model (see Section 3.4.3) are validated. It has to be noted that experimental switching losses contain also dead-time losses.

Even for such low switching frequency (see Figure 3.34(a)- 20 kHz) the influence of the switching losses is reduced as the current ripple increases. However, the increase of the conduction losses leads to achieve similar power losses. Furthermore, when switching losses are more relevant (see Figure 3.34(a)- 40 kHz) the increase of the current ripple results on even lower power losses. Medium switching frequency operation (80 kHz) with reduced losses has been demonstrated even for hard-switching operation. It has to be noted that dead-time losses begin to be relevant at 80 kHz.

Thus, the possessed asymmetrical dead-time control strategy is validated for 80 kHz, achieving a reduction of power losses (see Figure 3.34(b)).
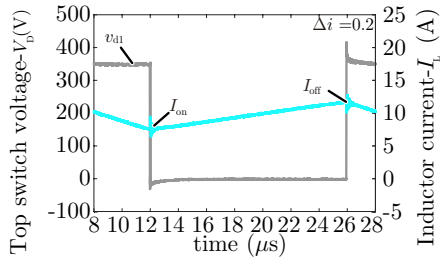
(a)
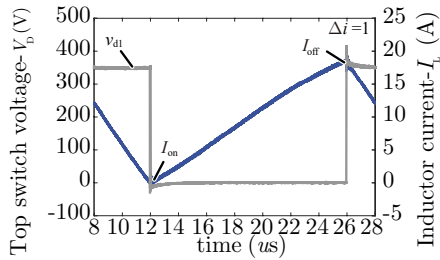
(b)
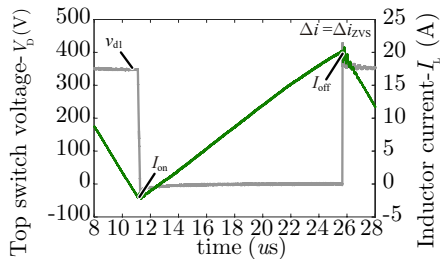
(c)

Figure 3.32: Experimental curves at different operation modes
(V_i=350 V and I_o=10 A): (a) hard-switching, (b) ZCS and ZVS.
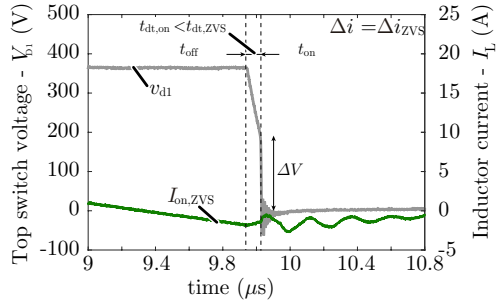
(a)
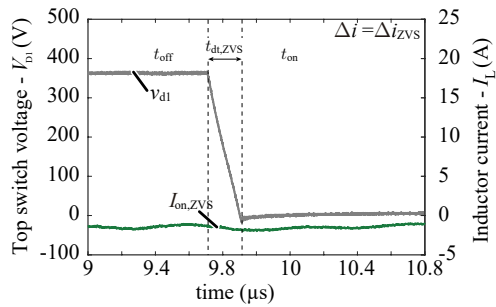
(b)

Figure 3.33: Experimental validation of ZVS condtions (V_i=350 V and I_o=10 A): (a) incomplete ZVS and (b) complete ZVS

(a)

(b)
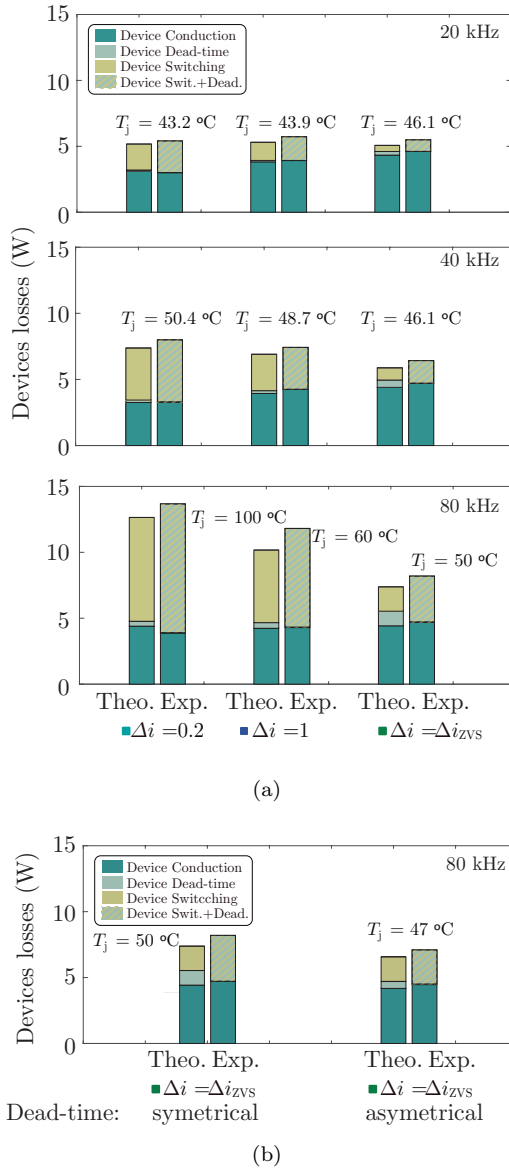
Figure 3.34:   Experimental validation of GaN devices performance
(V_i=350 V and I_o=10 A): (a) experimental distribution of devices power
losses compared to theoretical results and (b) dead-time control strategy
comparison for 80 kHz.

3.5 Conclusions

In this chapter, the benefits and limitations analyzed in Chapter 2 are evaluated and experimentally validated. First, design considerations related to driver, dead-time and parallelization are presented. Driver designs for the most commonly used GaN devices are proposed, i.e. insulated HEMT and non-insulated GIT. The presented designs result on reliable gate driver performance, without exceeding voltage safety margin and avoiding false turn-on. Regarding dead-time, the benefits of an asymmetrical dead-time control is evaluated, reducing dead-time losses when operating at high current ripples. Besides, the gate driver layout is analyzed for paralleling GaN devices. Symmetrical gate driver is presented, achieving an evenly shared current between devices.

Furthermore, considering the thermal cooling limitation of small size GaN devices, three cooling configurations are analyzed, including heat-spreading materials. Only comparing the thermal performance of both packages, top-side cooled device is better than bottom-side cooled one. However, the use of bottom cooled configuration with Cu inlay, increasing the thermal pad, and better TIM material improves the cooling performance in comparison with the top cooled configuration. As it was presented in Section 2.6, the use of parallel devices and heat-spreading materials overcome thermal cooling limitations of GaN devices. In Section 3.3, it is demonstrated that the use of heat-spreading material can increase the cooling capability by 56%. Hence, the use of heat-spreading materials to increase the dissipation area will be essential when designing GaN-based power converters.

Then, the performance of devices is evaluated at converter level with a general analytical model that can be adapted to different topologies. This model is based on the analytical expressions presented in Chapter 2. In this case, the analysis is centered on a well-known synchronous buck converter. The great difference between turn-on and turn-off energies, along with low conduction resistance of GaN devices leads to low power losses. Furthermore, the proposed asymmetrical dead-time control reduces the high impact of dead-time losses. The effect of operating at different current ripples and switching frequencies has been evaluated with paralleled devices.

On the one hand, the increase of the current ripple, ensuring ZVS, reduces power losses of semiconductors for high-switching frequencies ($>40\,\mathrm{kHz}$). Nevertheless, the relevance of GaN devices switching losses

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is low when considering full converter performance. Then, hard switching operation mode achieves lower overall losses than ZVS up to 40 kHz. On the other hand, the use of parallel devices results on lower power losses up to high switching frequency <150 kHz. These results are experimentally validated in Section 3.4.5 through calorimetric measurements.

All the analyses carried out in this chapter will be used during the GaN-based converter design process of Chapter 4 and defining potential solutions of GaN devices in Chapter 5.

Chapter 4

GaN-based Power Converters Performance

I<small>N</small> previous chapters, the operation of GaN devices at high switching frequency and with high current ripple has been demonstrated, due to their low conduction and switching losses (see Section 3.4.6). Hence, once operation conditions and limits of GaN devices have been evaluated, the performance at converter level is evaluated in this chapter.

For that purpose, an optimization routine is presented in Section 4.1. There is a clear tendency on improving power converters performance, increasing the efficiency, while reducing the converter overall size. Until recent years, the typical development process of a power converter consisted on a first prototype which performs the basic operation, and then the design was improved for next prototypes. However, thanks to computers with higher processing capability, huge amount of simulations can be performed with short computation times [133, 134]. Therefore, with the use of multiple simulations the optimal design can be obtained, before building experimental prototypes. This optimization routine is based on the power losses model presented in Section 3.4 and approximation models of Appendix A. The proposed approximation models are based on approximation equations related to commercial database and scaling laws. In this manner, the complexity and the computation time of the analysis is reduced. This procedure can be applied to different converter topologies in order to define the most optimal solution based on GaN devices.

Afterwards, the impact of the increase of switching frequency and current ripple on the components that conform a power converter is evaluated in Section 4.2. Finally, in Section 4.3 the main conclusions of this chapter are summarized.

4.1 Design and Optimization Routine

On the optimization procedure of a power converter multiple domains can be considered, such as thermal limitations, electric and/or electromagnetic behaviour. The optimal power converter design refers to the most suitable solution with respect to single or multiple performance indicators from all possible solutions.

In recent years several works related to multi-objective optimization applied to power electronics systems have been presented in the literature [15, 60, 119, 133–137]. Most of them have been applied for the evaluation of efficiency η and power density ρ of resonant converters [133], multi-level inverters [136], Power Electronic Transformers (PET) [134,135] and Inductive Power Transfer (IPT) [137], among other power electronic solutions. Moreover, [15, 134] evaluate the influence of the cost on the converter design for a more industrial solutions, where the cost is a limiting factor. In this section, a design routine based on power losses model presented in Section 3.4 and approximation models of Appendix A is presented, achieving low computation time. The proposed optimization routine defines the most optimal solution in terms of η and ρ.

The flow chart of the optimization routine is depicted in Figure 4.1. The inputs required for the proposed optimization includes system specifications, design constraints and parameters. Regarding system specifications the minimum required efficiency and/or power density is specified, while design constraints and parameters are more related to the electrical and thermal characteristics of the system. Then, the design space is defined and optimization procedure begins. The steps depicted in Figure 4.1 are described below. From the design space definition until the optimal designs.

4.1.1 Design space

The design space is related to the variation of design parameters that have influence on the performance of the power converter. Then, the
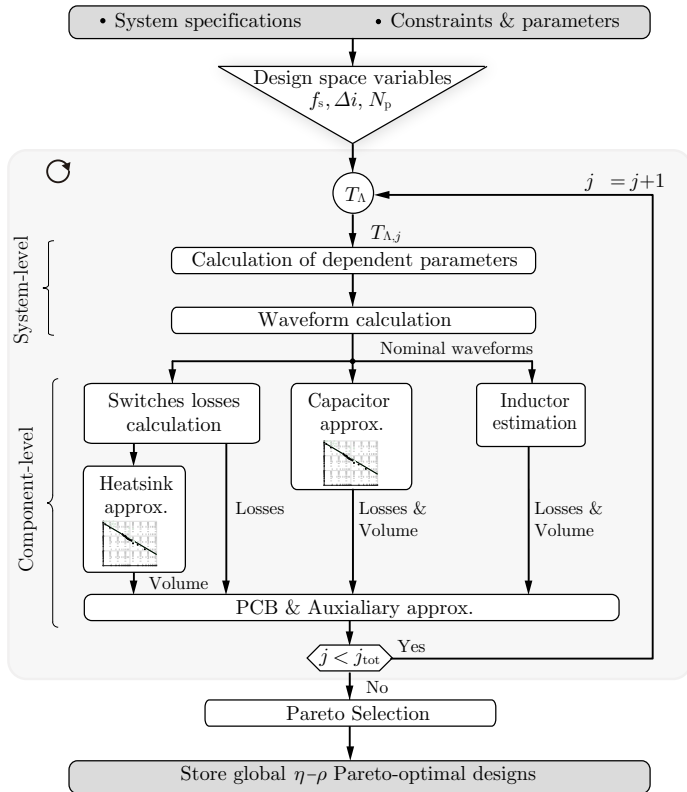
Figure 4.1: Proposed converter design optimization routine based on approximation models. The optimization routine performs the mapping of all possible designs defined by the design space. Then, the optimal Pareto Selection is done in terms of efficiency η and power density ρ.

possible number of designs is defined T_Λ. The mapping of entire options T_Λ is evaluated, for every single design $T_{\Lambda,j}$.

4.1.2 System-level

Once the global specifications are defined, calculation of parameters which are dependent on the design space is performed. Moreover, wave-

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forms related to the converter topology are theoretically obtained and validated by PLECS simulations. In this step, current and voltage waveforms of main components are obtained. In Figure 4.2 an example of theoretical calculation, which is validated by simulation, is depicted for a synchronous buck converter. Low error is obtained when comparing the RMS of each waveform. The use of theoretical calculations reduces computation time.
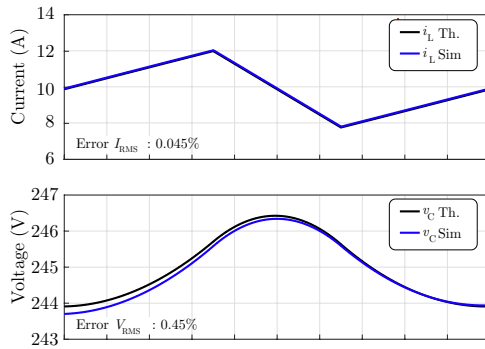
Figure 4.2: Validation of theoretical calculation of components waveforms: inductor current (i_L) and capacitor voltage v_c of a synchronous buck converter.

4.1.3   Component-level

Losses and volume of the components that conform a power converter are estimated, based on the defined specifications and calculated waveforms. Local design spaces are defined for the component level loops. These design spaces are defined for different component technologies, types and details. Power losses of switches are estimated with the model presented in Section 3.4, while other components performance is evaluated with approximation models presented in Appendix A. Hence, losses and/or volume of different components are obtained for a defined design space.

PCB and auxiliary

The losses related to the PCB are obtained from the conduction resistance ($R_{\mathrm{PCB}} = 0.08\,\mathrm{m\Omega}$) of the PCB for specified system current I_{in}. Auxiliary losses are obtained from additional supplies of the power board, such as, gate driver requirements P_{drv} (2.11), cooling system P_{cs}, control and measurements (P_{ctrl}=4 W). Moreover, these power losses are approximated with (4.1).

$$P_{\mathrm{AUX}} = \frac{1}{\eta_{\mathrm{aux}}} \cdot (P_{\mathrm{drv}} + P_{\mathrm{cs}} + P_{\mathrm{ctrl}}) \tag{4.1}$$

where an efficiency η_{aux}=75% is assumed for these auxiliary supplies [15].

Regarding the volume, 10-15% of the total volume is considered, as constant volume, based on experimental set-ups [120, 138].

4.1.4 Pareto selection

Besides, a *posteriori* method, i.e. Pareto-front optimization, is performed afterwards, selecting the optimal performance between all feasible solutions. This algorithm identifies the best performance point between two or more performance indicators (Pi_{i}) for all feasible solutions.

In Figure 4.3 a Pareto-Front example is depicted, where the Pareto-front is the line. Moreover, design limits are also considered when defining the Pareto-front line. Pareto-front line defines the most suitable solutions in terms of Pi_1 and Pi_2 performance indicators, between all feasible solutions (see Figure 4.3).

In this case, the most commonly selected countering performances, such as efficiency η and power density ρ, are evaluated. For these indicators a trade-off between η and ρ must be considered. Indeed, if a very efficient system is required the power density is reduced and *vice-versa*.

4.2 Performance of Components

In order to evaluate the impact of high-performance GaN devices on power converter components, the design space evaluated in Chapter 3 (N_{p}, Δi, f_{s}) is considered. Indeed, power losses and volume impact on cooling system technologies and passive components is evaluated for a dc-dc converter.
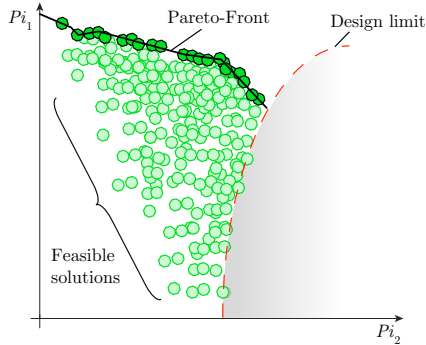
Figure 4.3: Pareto-front example with two performance indicators (Pi_1, Pi_2), considering the design limitations.

4.2.1 Cooling system

A trade-off between the power dissipation capability (2.36), power losses (see Section 3.4) and the system complexity has to be considered when defining a cooling system. Moreover, N_p number of devices and a $T_{j,max}$ design constraints need to be considered. The volume of the required heatsink increases with the power losses of devices (see Figure 4.4). Besides, as the increase of switching frequency results on higher semiconductor power losses, the volume of the heatsink also increases.

Considering GaN devices with small size package IGO60R070D1-[108] and the heatsink approximation models (see Appendix A), the volume of heatsink is evaluated in Figure 4.4. On the one hand, Figure 4.4(a) shows the volume impact of different cooling systems, for a bottom cooled system with Cu inlay but without spreading the heat along a wider area. Indeed, devices are connected to the heatsink through a Cu inlay thermal resistance of 0.5°C/W and a TIM Hi-Flow 300p, but just considering the active area of the device (13.5x5.9mm^2).

The use of N_p parallel connected increases the power dissipation capability, reducing the required volume [see Figure 4.4(a)]. However, the impact of TIM resistance limits the thermal cooling capability for every cooling technology, as it has been analyzed in Section 2.6.

On the other hand, the bottom cooling configuration presented in Section 3.3 is considered for different heatsink technologies. Figure 4.4(b) shows an improvement of cooling capability, reducing the required thermal resistance and thus the heatsink volume. In addition,
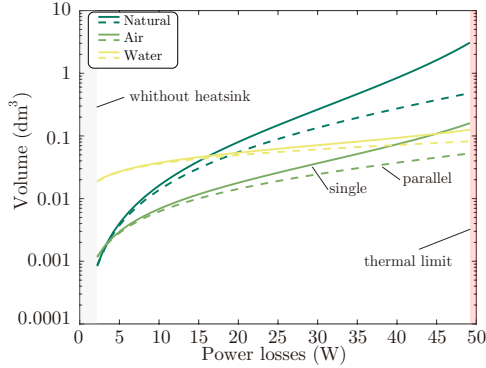
(a)
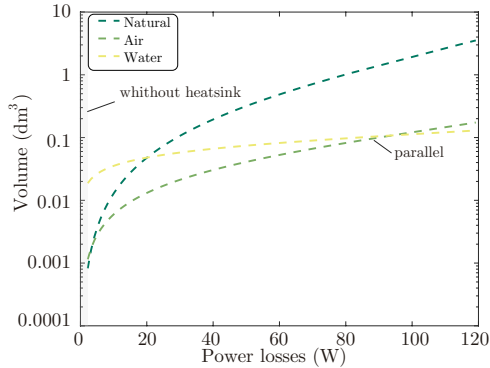
(b)

Figure 4.4: Analysis of the thermal dissipation limit ($P_{d,lim}$) for natural-convection, forced-air and water cooling configurations: (a) Cu inlay considering only the active area of the device (b) Cu inlay with heat-spreading.

the use of air-forced cooling solutions result on a lower volume even for medium power losses ($>20\,W$). The use of water cooling solutions will be interesting for higher power losses ($>90\,W$). In this case, the thermal limit is determined by the cooling system technology, defined in Appendix A.

Therefore, it is demonstrated that the use of heat spreading materials and parallelization is essential to increase thermal cooling capability of GaN devices. Moreover, for medium-high power converters based on

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bottom side cooling with heat-spreading, the use of air-forcer heatsinks is presented as the most suitable solution for power losses lower than $\approx$90 W [see Figure 4.4(b)].

4.2.2 Capacitor

Considering the general capacitance definition (A.8) and a fixed voltage ripple $\Delta v_c = 0.2$ the volume is evaluated for the previously defined design space and different technologies. Figure 4.5 shows how the use of ceramic or film capacitors supposes an increase on the converter volume in comparison to aluminum capacitors. However, the use of aluminum capacitors implies power losses, while power losses of ceramic and film capacitors are negligible. Power losses and volume increases with the current ripple, as it is shown in Figure 4.5 comparing low (Δi=0.2) and high current ripples (Δi=1.2).
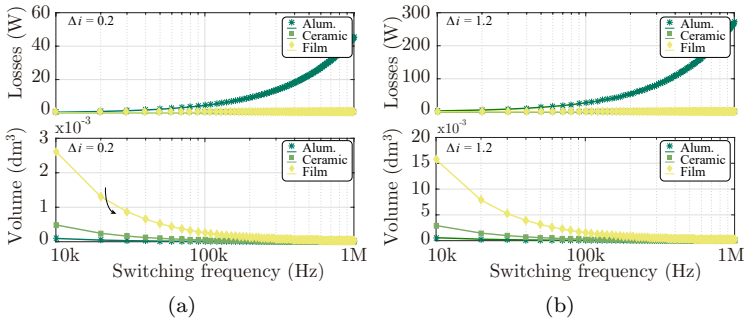
Figure 4.5: Impact of design parameters on capacitor performance, i.e. volume and losses, for 350 V and 10 A and different capacitor technologies: (a) Δi=0.2 and (b) Δi=1.2.

Hence, for high-frequency operation ceramic capacitors are recommended, as a result of negligible losses with similar volume impact as aluminum capacitors (see Figure 4.5).

4.2.3 Inductors

In this work E-type ferrite core N87 is chosen for the analyzed frequency range (10 kHz-1 MHz). Besides, an standard litz wire of (35 μm x 32) is selected. Figure 4.6 shows the impact of switching frequency on the

inductor performance for three current ripples, considering (A.14) and a dc current with a ripple Δi.
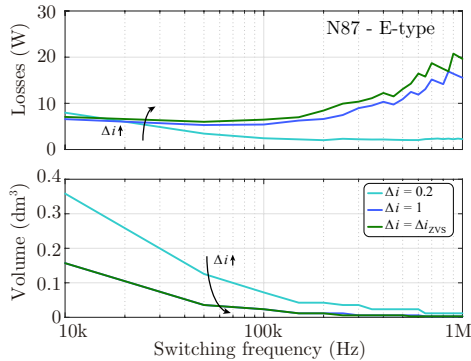
Figure 4.6: Impact of design parameters Δi and f_s on inductor performance, i.e. volume and losses, for 350 V and 10 A.

The increase of the current ripple results on expected higher losses but lower volume, as a consequence of lower required inductance (see Figure 4.6). High current ripples result on higher losses, mainly for high-switching frequencies. On the contrary, for low current ripples power losses are reduced while switching frequency increases. In addition, the inductor volume is reduced while the switching frequency increases. However, the higher switching frequency is ($f_s > 100$ kHz), the lower impact on the volume has, as it is depicted in Figure 4.6.

4.3   Conclusions

In previous chapters the high performance of GaN devices operating at high-switching frequency or/and high current ripple has been demonstrated, along with the benefits of paralleling semiconductors. However, it is not straightforward to determine the benefits of applying these operating conditions, when evaluating the overall converter performance. Therefore, this chapter analyzes the impact of switching frequency, current ripple and parallel connected devices on other components of converter.

Then, the impact of operating conditions on the volume and losses of these components is evaluated, based on the approximation models

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presented in Appendix A. Regarding power dissipation capability, the volume requirement is only related to semiconductors losses. As low power losses are expected for GaN devices, naturally cooled or air-forced cooled solutions are presented as the most suitable solutions, with reduced heatsink size. Besides, for implementing GaN devices at higher power levels, with power losses higher than $\approx 90\,\mathrm{W}$ water cooled solutions are preferred. In addition, inductor and capacitors volume reduces as the switching frequency increases. However, as the volume of the cooling solution increases with the switching frequency, a trade-off between switching frequency and volume has to be considered. Besides, for the analyzed design considerations it is not expected a clear reduction of the converter size for extremely high switching frequencies ($>500\,\mathrm{kHz}$).

Therefore, the benefits and limits of GaN semiconductors are presented in Chapter 2-3 and the impact of operating with high-performance GaN devices on converter overall losses and volume is introduced in this chapter. Then, how GaN devices can or cannot improve the performance of different topologies is evaluated in Chapter 5.

Chapter 5

GaN Devices Topological Evaluation

ENHANCEMENTS introduced by the use of GaN devices have been analyzed in previous chapters, resulting on high-switching frequency operation with relatively low losses and reducing converter size. However, it is not evident how these benefits and limitations affect to different system requirements. In this chapter, advantages and disadvantages of implementing GaN devices on power converters are evaluated with different topologies. For this study, power losses model presented in Section 3.4 and design optimization routine of Section 4.1 are used. Furthermore, the presented results are experimentally validated on GaN-based power converters. Indeed, design considerations, benefits and limitations of operating with high-performance GaN devices, presented in previous chapters are applied to different power electronics solutions. Hence, potential topologies and applications where GaN devices appear as a suitable solution are evaluated during this chapter.

First, in Section 5.1, different topologies are analyzed, differing between single-cell and multi-cell topologies. Regarding single-cell topologies, two main groups are identified: non-isolated, and isolated. Section 5.2 evaluates the performance of a non-isolated GaN-based buck converter. Besides, isolated resonant converters are analyzed in Section 5.3. The performance of a series-series resonant IPT is evaluated, identifying benefits of GaN devices working on resonant operation. This analysis is an extended version of the work presented in [138, 139].

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In addition, multi-cell topologies are analyzed considering Low Voltage (LV) and High Voltage (HV) applications. On the one hand, the performance of HV GaN-based Modular Multilevel Converter (MMC) is presented in Section 5.4 [140]. The influence of switching frequency on the converter is analyzed, defining the advantages and issues of implementing it with GaN semiconductors. On the other hand, the use GaN semiconductors on LV multi-cell applications is evaluated in Section 5.5. In this context, novel topology Multi-cell Multi-port Bidirectional Flyback (M2BF) is proposed, achieving high controllability and low power losses.

Finally, conclusions related to the implementation of GaN devices on power electronics are summarized in Section 5.6.

5.1 Potential Topologies

Figure 5.1 shows a general overview of power converter topologies. These configurations are distributed considering the number of cells. On the one hand, power solutions based on single-cell converters are the most commonly used configurations for low/medium power range due to the simplicity of its implementation. On the other hand, multi-cell converters are presented as a suitable solution for medium/high power converters [141]. In addition, in last decade, the use of multi-cell configurations has also been demonstrated as a competitive solution, increasing reliability and controllability of systems in low/medium power range [110]. Hence, the characteristics of these topologies are analyzed in order to define the most suitable configurations for previously analyzed GaN semiconductors

These two main groups are divided into different categories, highlighting the operation mode of each converter topology, i.e. hard-switching and/or soft-switching. Furthermore, the main relevant characteristics and configurations of each converter are summarized in Figure 5.1: number of active devices; configuration possibilities, dc-dc, dc-ac, ac-dc or ac-ac, and switching modes, soft-switching and/or hard-switching.

Figure 5.1: Topological analysis differing between single-cell and multi-cell configurations.

5.1.1 Single-cell

Single-cell converters can be divided in accordance to isolation requirement, as it is depicted in Figure 5.1: isolated and non-isolated converters. In addition, converters can be grouped depending on output levels: two-level or multilevel. In this case, only two-level converters are evaluated for single-cell converters. Multi-level concept will be analyzed for the case of multi-cell converters.

Non-Isolated

These converters can be operated in hard or soft switching mode, depending on the system requirements, i.e. output current ripple. In this group, most commonly used converters such as buck, boost or buck-boost appears. Besides, bidirectional operation can be achieved including synchronous switch to the half-bridge configuration of these converters. In addition, Cuk converter appears also as a suitable topology, but with negative to positive voltage conversion. Nevertheless, the connection between input and output is one of the main drawbacks of these topologies, as some applications require an isolation between input and output.

Synchronous buck converter is selected in order to evaluate its performance when using GaN devices. Then, the performance improvements added due to the use of GaN devices are evaluated, in terms of efficiency and power density.

Isolated

Regarding isolated converters, the main difference in comparison to non-isolated ones is the transformer, which provides isolation. On the one hand, topologies such as flyback, forward or push-pull, are controlled similar to non-isolated converters [142]. Moreover, these converters can be operated in hard or soft-switching operation mode. On the other hand, isolated resonant converters are generally used for dc-dc applications. Most of them consist of an inverter, high frequency transformer and a rectifier. Besides these converters are classified depending on active bridges: Single Active Bridge (SAB) or DAB. Resonant converters include a resonant network, which can be formed by different inductor (L) and capacitor (C) configurations, e.g. LC or LLC, in order to facilitate soft-switching operation, such as the GaN-based LLC Converter

presented in [143].

In this case, the potentiality of GaN devices working on a resonant converter is evaluated. For that purpose, IPT based on GaN devices is analyzed, as an extended and more detailed analysis of the work presented in [138].

5.1.2 Multi-cell

Multi-cell topologies are commonly defined as converter systems formed by two or more subsystems that are connected in one of the following configurations: input-series output-parallel, input-series output-series, input-parallel output-series or input-parallel output-parallel. Moreover, systems with two or more input or/and outputs are known as multi-port systems with different possibilities: single-input multiple-output, multiple input single-output and multiple-input multiple-output.

Therefore, the use of Multi-cell Multi-port (MCMP) results on configurable systems with high controllability. In addition, semiconductors with better performance can be used because the total power is fractioned between the number of cells. In this context, GaN devices appears as an interesting solution for this application requirements mainly due to low conduction losses and high switching performance (see Section 2.2). Besides, it has to be noted that GaN devices present remarkable benefits for MCMP systems, as a consequence of low driver requirements (Section 2.2.3). That is an important factor due to the higher number of devices used on MCMP. In addition, the use of multi-level topology enables the operation at higher voltages (>650 V), than the rated for current available devices (see Figure 2.2).

MCMP systems have been established primarily in medium- to high-voltage high-power applications [141, 144]. However, in recent years, versatility of MCMP systems have also been demonstrated for lower power range [110]. Then, multi-cell topologies have been analyzed for HV (>600 V) and LV (<400 V) applications.

High-voltage applications

Commercial GaN devices have relatively low blocking voltages (650V up to date) making difficult the use of these devices on medium/high voltage applications. However, thanks to the use multi-cell topologies, GaN devices can be used in applications where higher blocking voltages

are required, connecting cells in series. Considering HV application requirements the cascaded H-bridge Cascaded H-Bridge (CHB) topology has gained attention and has been applied in different kind of solutions, such as in railway applications [145]. Moreover, multi-cell topologies are also implemented in order to increase the reliability of the system, e.g. Multi-cell DAB (MDAB) presented in [146].

In addition, MMC has gained significant interest, especially in the area of High Voltage Direct Current (HVDC) converters [147], Flexible AC Transmission Systems, and Medium Voltage Drive (MVD) [148]. This topology was introduced in 2003 by *Lesnicar and Marquardt* [149], and it combines multilevel concept with modular structure by the use of cascaded Sub-Module (SM) or cells, allowing the use of low voltage blocking devices.

In this work, the performance benefits and limitations of GaN-based MMC are analyzed in Section 5.4.

Low-voltage applications

The use of MCMP architecture will be interesting also for lower power applications. DC Power Distribution Systems (DC-PDS) [150] or distributed Energy Storage Systems (ESS) [151, 152] have been analyzed among others. Indeed, the use of LV GaN devices ($<400\,\text{V}$) clearly improves the performance of the converter [152, 153]. For these specifications, normally multiple single-cell converters are connected in series or parallel, e.g. input-series output-parallel single phase power supply presented in [153]. Furthermore, Flying Capacitor Converter (FCC) which is commonly used for HV applications, presents high-efficiency ($>97\%$) with a reduced size ($0.14\,\text{dm}^3$) based on LV GaN switches [154].

These applications require multiple sources with a full control of delivered power, providing isolation in some cases. In this context a novel M2BF is proposed, allowing either dc or ac sources as inputs. In this work, only dc-dc configuration is presented. This architecture enables a bidirectional power flow with an individual control of each cell due to four quadrant switches. Besides, M2BF adds the possibility of configuring the number of connected cells according to system requirements. This results on a very versatile and configurable system, being suitable for many different applications, as it is shown in Figure 5.2 for different dc-dc solutions.
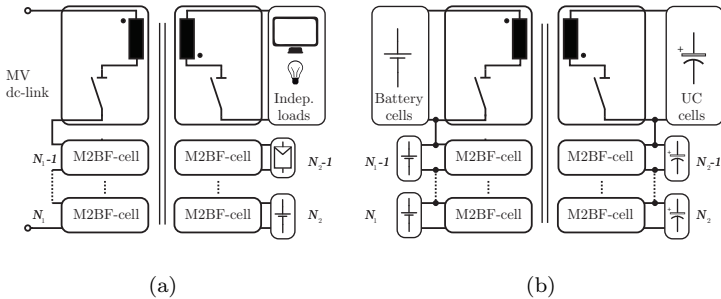
Figure 5.2: M2BF potential dc-dc applications: (a) DC-PDS with medium-voltage (MV) primary side and independent secondary sides and (b) hybrid ESS based on battery and ultra capacitors (UC) cells.

5.2 Single-cell Non-isolated: Buck dc-dc

Buck converter is evaluated in order to define the impact of high-performance GaN devices on an already well-known topology. In Section 3.4 power losses of devices for three operation modes are analyzed, defining the most suitable operation mode for each conditions, i.e. hard-switching, ZCS and ZVS. Then, in this section, power losses and volume impact at power converter level are evaluated for different current ripples, number of devices and switching frequencies. Indeed, the influence of design space parameters that have been previously used for GaN devices performance analysis in Section 3.4 are considered for the optimal design of GaN-based synchronous buck converter. Indeed, benefits and limitations of GaN-based non-isolated power converters are defined.

Figure 5.3 shows the analyzed synchronous buck converter, along with the output inductor (L) and input and output capacitors (C_i and C_o).

5.2.1 Operation principles

Following, different aspects of the synchronous buck converter are defined, in order to evaluate the performance of the converter:

▶ *Passive components sizing*: Design space parameters define the reactive components that conform a buck converter, i.e. C_i, L and output C_o.

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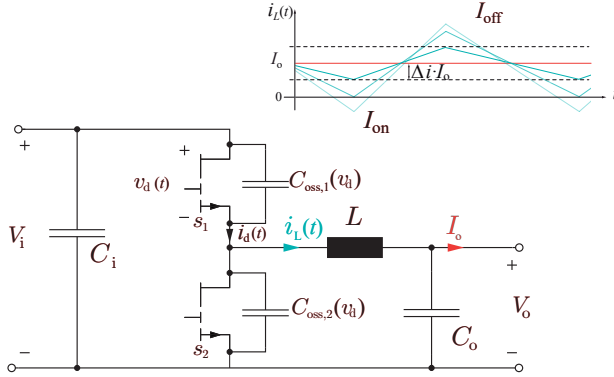
Figure 5.3: Synchronous buck converter based on GaN devices, with asymmetrical dead-time control.

▶ *Cooling limits*: The required cooling system is defined in accordance to losses distribution of semiconductors, which is presented in Section 3.4. Cooling system is defined, analyzing the power losses distribution between semiconductors that conform the buck converter.

▶ *Control strategy*: Benefits of operating the synchronous buck in soft-switching are presented in Section 3.4, being possible to achieve high switching frequency operation with relatevily low power losses. However, this ZVS conditions are defined at nominal operating conditions, being not possible to achieve ZVS in the whole output load. Hence, Quasi Square Waveform (QSW)-ZVS control strategy is described in order to achieve ZVS over the whole output load. Thus, ZVS condition can be ensured independently to the load.

Passive components

The output capacitance of a buck converter is defined for an output voltage ripple per unit Δv_o

$$C_\mathrm{o} = \frac{\Delta i \cdot I_\mathrm{o}}{4 \cdot \Delta v_\mathrm{o} \cdot V_\mathrm{o} \cdot f_\mathrm{s}}. \tag{5.1}$$

being I_o output current.

Besides, the input capacitance C_i is defined with (5.2) and the input voltage ripple requirement Δv_i.

$$C_i = \frac{I_o \cdot (1 - \delta) \cdot \delta}{\Delta v_i \cdot V_i \cdot f_s}. \tag{5.2}$$

Regarding the magnetics, the output inductance is given by (5.3) for a duty cycle δ,

$$L = \frac{V_i \cdot (1 - \delta) \cdot \delta}{2 \cdot \Delta i \cdot I_o \cdot f_s} \tag{5.3}$$

where V_i is the input voltage.

Cooling system

Regarding cooling configuration, the power losses are obtained for different operating conditions (see Section 3.4) and then the required $R_{th,hs}$ is defined with (A.1), for a specified T_j and TIM. Moreover, the losses distribution needs to be considered when defining $R_{th,hs}$ (A.1).

Power losses are distributed as follows (5.4), for the synchronous buck converter high-side (s_1) and low-side (s_2) devices with positive output current.

$$P_{d,s1} = P_c \cdot \delta + P_s + P_{dt,on} (\text{if} \quad \Delta i > 1)$$
$$P_{d,s2} = P_c \cdot (1 - \delta) + P_{dt,off} + P_{dt,on} (\text{if} \quad \Delta i \leq 1) \tag{5.4}$$

being conduction losses distributed with δ, switching losses related to s_1 and dead-time losses depends on the current ripple.

It has to be noted that for high current ripples ($\Delta i > 1$), part of dead-time losses, i.e. turn-on dead-time losses, are related to s_1, while turn-off dead-time losses are produced in s_2. Moreover, for negative output current the losses distribution between devices is the contrary. Then, the power losses limitation per device is the maximum of both devices, as it is analyzed in Section A.0.1.

QSW-ZVS control strategy

In order to achieve ZVS transition on a synchronous buck converter, the inductor is defined with (5.3) for a current ripple that provides ZVS (Δi_{ZVS}) within a dead-time $t_{dt,ZVS}$ (see Section 3.4.2). However, the sizing of the inductor is performed for nominal operating conditions.

Therefore, the switching frequency needs to be varied in order to maintain ZVS transition with large current ripple [155], when working with different output load. Hence, a frequency variable control is performed, achieving ZVS transitions even for low output power, as it is depicted in Figure 5.4. In this manner, Δi_{ZVS} is ensured for the whole operating range, which provides ZVS transition.
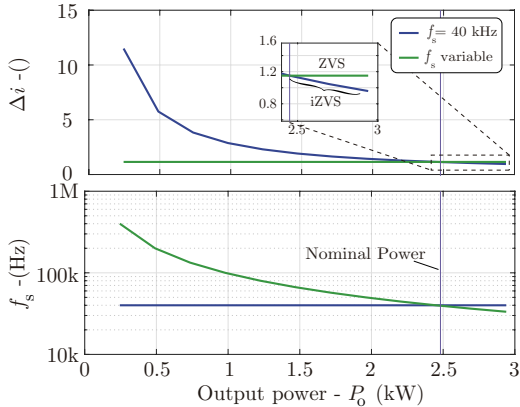
Figure 5.4: Impact of variable switching frequency control on the output current ripple (Δi) of a synchronous buck converter.

5.2.2 Performance evaluation

For this analysis, specifications and design space presented in Table 3.6 are considered, i.e. 2.45 kW and 350 V input voltage. An asymmetrical dead-time control is implemented when operating with $\Delta i > 1$.

Converter level losses and volume

The impact of design space parameters on the whole converter performance is evaluated for the previously defined design space, considering ceramic capacitors with negligible for input and output capacitors, for this first approach. Besides, forced-air cooling solutions are only considered, as appears as the most suitable solutions for this operation power range (see Section 4.2).

On the one hand, Figure 5.5(a) shows power losses distribution for different current ripples and a switching frequency of 100 kHz. Induc-

tor losses increase with the current ripple as it occurs with conduction losses of semiconductors. On the other hand, the impact of switching frequency is evaluated in Figure 5.5(b). Low current ripple (hard-switching) and high current ripple (ZVS) are only considered, as ZCS presents an intermediate performance (see Figure 3.30). Figure 5.5(b) shows how hard-switching operation mode presents lower losses than ZVS up to high-switching frequency (<110 kHz). This value is higher than when analyzing only GaN devices losses (see Figure 3.30). This is mainly due to the higher impact of losses related to the increase of the current ripple [see Figure 5.5(a)] and the low impact of switching losses on GaN devices.

When analyzing the volume impact, the size of inductor and capacitor reduces while increasing the switching frequency (see Figure 4.5-4.6). Nevertheless, the volume of the heatsink increases with the switching frequency, limiting the reduction of converter overall size as it is shown in Figure 5.6(a) for low current ripples. In addition, high current ripple results on lower volume than low current ripple, as it is compared for two current ripples in Figure 5.6(b). The increase of switching frequency reduces power converter volume for switching frequencies lower than 300 kHz [see Figure 5.6(b)]. Paralleling devices reduces converter losses (see Figure 5.5), maintaining almost the same volume reduction as it is shown in Figure 5.6(b).

Therefore, the increase of switching frequency reduces converter overall size even for hard-switching or ZVS operation modes. However, an excessive increase of the switching frequency, i.e. >300 kHz, does not result on a reduction of the converter overall volume. Moreover, it is demonstrated that the use of multiple devices will be essential for medium-high power converters based on GaN devices, increasing power losses limit and maintaining similar converter volume. Then, considering these results, optimization routine (see Section 4.1) is applied to GaN-based synchronous converter, defining the most optimal solution in terms of efficiency and power density, for a 2.45 kW power converter.

Optimization results

Once the impact of design parameters on the power converter are evaluated, the optimal GaN-based power converter designs are obtained among all feasible solutions. In this case, only forced-air cooling configurations are analyzed, as it has been previously presented as the most suitable solution for the analyzed design space [see Figure 4.4(b)]. More-
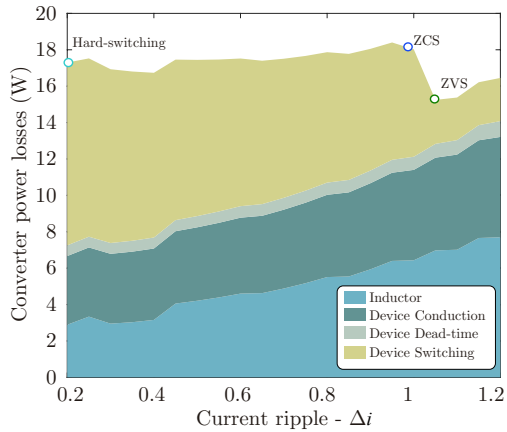
(a)
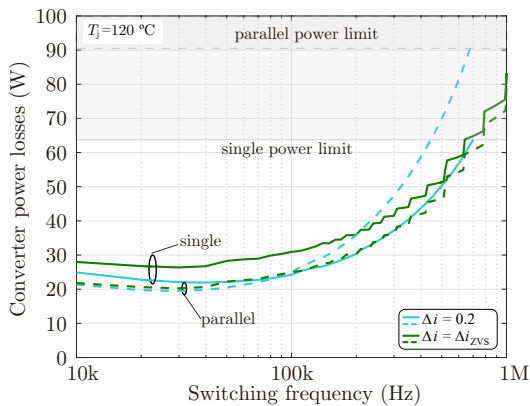
(b)

Figure 5.5: Power converter performance analysis for V_i =350 V and I_o =10 A: (a) distribution of power losses for different current ripples (f_s=100 kHz) and (b) comparison of buck converter power losses, varying the switching frequency for hard-switching and ZVS operation modes.

over, aluminum and ceramic capacitors are only considered because film capacitors present worse performance than ceramic capacitors in terms of power losses and higher volume impact than aluminum [see Figure 4.5]. Figure 5.7 shows designs of power converters with high power
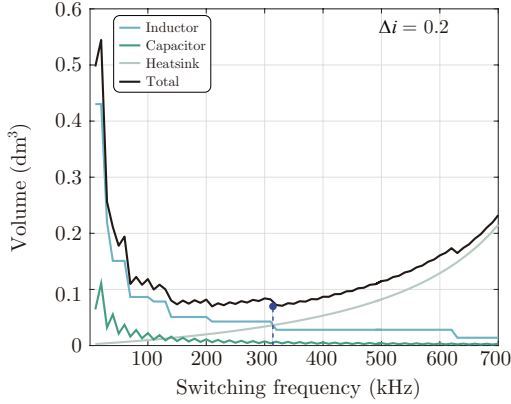
(a)
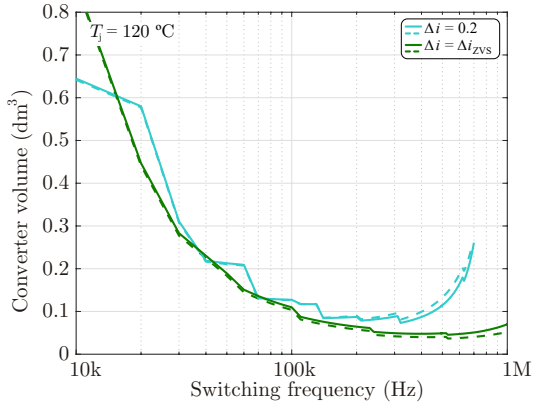
(b)

Figure 5.6: Power converter performance analysis: (a) heatsink, inductor, capacitor and total volume versus switching frequency (Δi=0.2 and N_p=1) and (b) comparison of buck converter volume, varying the switching frequency for hard-switching and ZVS operation modes.

density maintaining high efficiency (>97.5%) either for hard-switching operation or ZVS. Besides, Pareto selection is highlighted defining optimal solutions, for single device converters and converters with two devices connected in parallel. On the one hand, converters operated in hard-switching mode appears as the most suitable solution for ex-

tremely high-efficient systems (>99%), allowing also high power density (≈10 kW/l). On the other hand, when the power density is the most restrictive design constrain, soft-switching operation mode is preferred, achieving the highest power density when paralleling devices.

In addition, it has to be noted that for the specifications presented in Table 3.6 two parallel connected devices appears as the most suitable solution in terms of efficiency and power density.
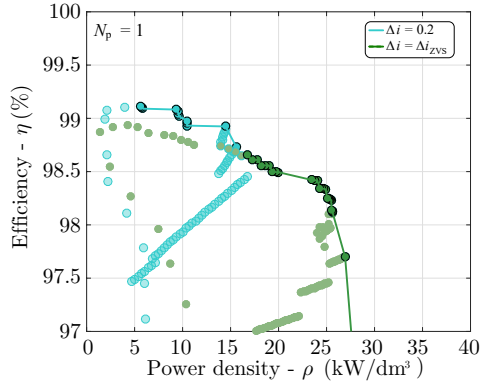
(a)
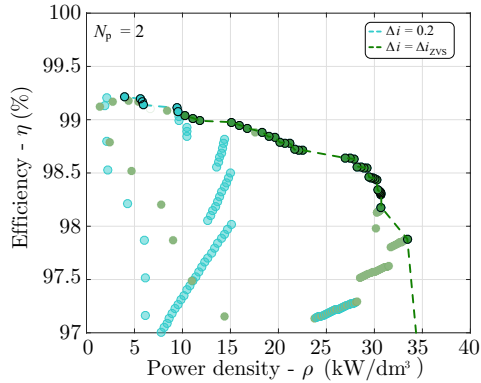
(b)

Figure 5.7: GaN-based optimal designs in terms of efficiency η and power density ρ (350 V/10 A) for Low current ripple (hard-switching) and high current ripple (ZVS operation mode): (a)single device and (b) parallel-connected devices.

5.2.3 Experimental measurements

Power losses of GaN devices operating a synchronous buck converter for different operating conditions has been already validated in Section 3.4.6. Thus, in this section the converter overall efficiency is evaluated for different operating conditions. In addition, the impact of the

QSW control strategy are experimentally validated on the converter performance, for the test set-up presented Figure 5.8. The used power inductor is not optimized, as it has been adapted for different operating conditions.
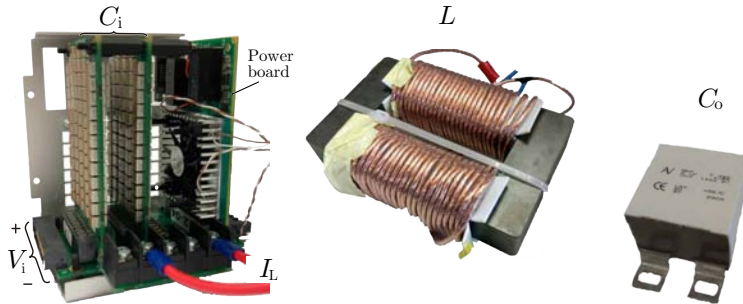
Figure 5.8: Synchronous buck experimental set-up based on GaN power modules, $2\,\mu$C ceramic capacitor (C_o) and $1\,$mH inductor (L).

The efficiency at converter level for a variable load is evaluated, as in some applications it is relevant to provide a high-efficiency over a wide power range. The obtained efficiencies are shown mainly for comparison purposes, as the output inductor has not been optimized for each operating point. Indeed, with an optimized inductor the efficiency could be increased.

Both current ripples that provide hard-switching and ZVS operation modes are compared in Figure 5.9. In the case of ZVS current ripple, a variable switching frequency control is implemented in order to maintain ZVS over the full operating range. It is validated that 20% current ripple achieves higher efficiency than Δi_{ZVS} operating at $20\,$kHz, as a consequence of low impact of GaN devices switching losses.

Therefore, it is demonstrated that the use of GaN devices increases the optimal operation range of hard-switching mode. Indeed, due to the low impact of GaN devices switching losses, hard-switching operation mode presents a better performance than ZVS for higher switching frequencies, as it is shown in Figure 5.5(b) and experimentally validated in Figure 5.9.
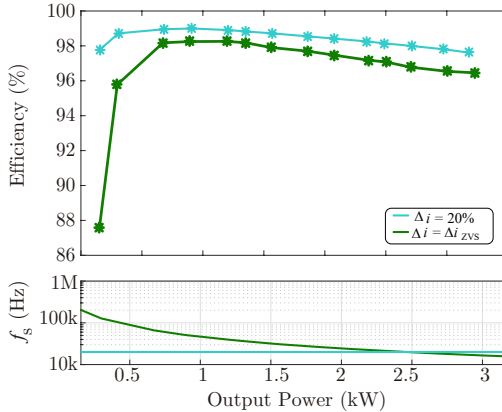
Figure 5.9: Experimental analysis of converter efficiency over a wide power range. Comparison of hard and soft switching current ripples.

5.3 Single-cell Isolated: Resonant IPT

An IPT resonant stage, used for a single-phase contactless battery charger is analyzed, evaluating the operation of GaN semiconductors with resonant waveforms. The use of contactless battery charging by IPT has been widely discussed as a charging system for PHEV/EV [139, 156–158]. Single-phase contactless battery charger system performs distinct tasks divided in two sides and different stages: rectification (R), input current shaping (CS) and PFC, current transfer (CT) and output voltage regulation (VR), as it is depicted in Figure 5.10 [139].

The presented analysis is mainly focused on the resonant stage, considering a SAB. The SAB appears as a very suitable and robust solution when unidirectional power flow is required. Besides, as in PHEV/EV applications the coupling coefficient k may vary drastically (from 0.2 to 0.5) a series-series (SS) compensation was chosen [157] (see Figure 5.10).

5.3.1 Operation principles

In this section, the most differential aspects related to IPT system are presented. A detailed analysis of IPT operation principles are described in [138]. The main advantage of contactless solution in comparison with conductive one is that the charging process is simplified, without the

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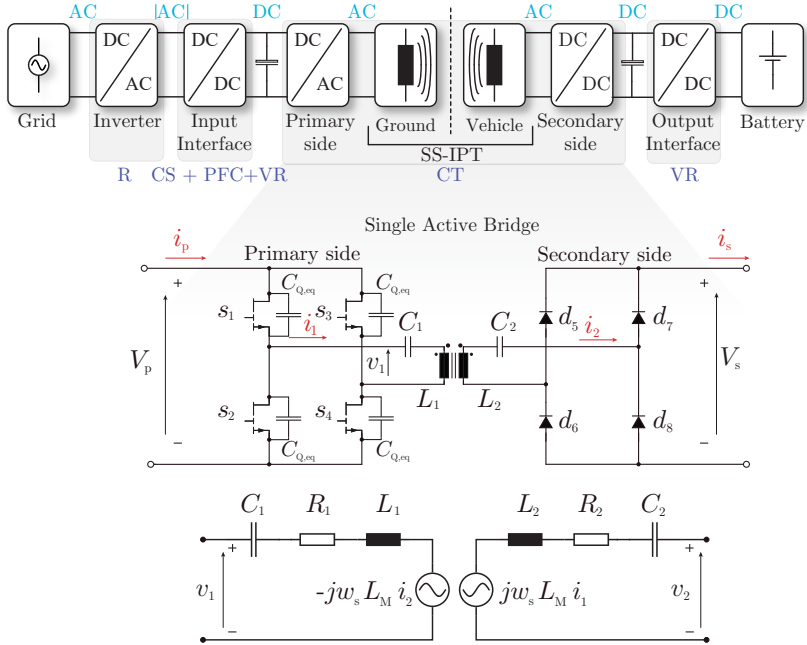
Figure 5.10: Unidirectional single-phase contactless battery charger, performing PFC on the primary side.

need of any physical connection between the vehicle and the charging point. However, in IPT systems, the coupling coefficient is usually very low ($k < 0.5$) compared to transformers ($k > 0.95$).

Design considerations

Figure 5.10 shows the equivalent circuit of the analyzed system. As a consequence of low k the relation between leakage inductances (L_σ) and mutual inductance (L_M) is changed, as it can be deduced from (5.5)

$$k = \frac{L_M}{\sqrt{L_1 \cdot L_2}}$$

(5.5)

being $L_1 = L_{\sigma,1} + L_M$ and $L_2 = L_{\sigma,2} + L_M$ self inductances of primary and secondary sides, considering a unity transformation ratio.

Moreover, the secondary side current (i_2) depends on the primary side induced voltages (v_1) and the reverse is also true. Then, the output power P_o can be derived [156].

$$P_o = \frac{8}{\pi^2} \cdot \frac{V_1 \cdot V_2}{\omega_s \cdot L_M} \tag{5.6}$$

In order to keep the commutation losses to the minimum, the switching frequency is set constant near to the resonance frequency, and it is not used as a control parameter. In this way, the resonance frequency is independent of the load and the output power can be adjusted by either V_1 or V_2.

When analyzing resonant converters, the input impedance ($|Z_{in}|\angle\phi$) is analyzed. Z_{in} represents the relation between v_1 and its current i_1, being ϕ the angle difference between voltage and current. Analyzing the $Z_{in}|\angle\phi$ different switching modes are identified. Figure 5.11 shows an example of input impedance of an IPT system for different coupling factors. Therefore, it is relevant to analyze different switching modes and the impact on GaN devices performance.
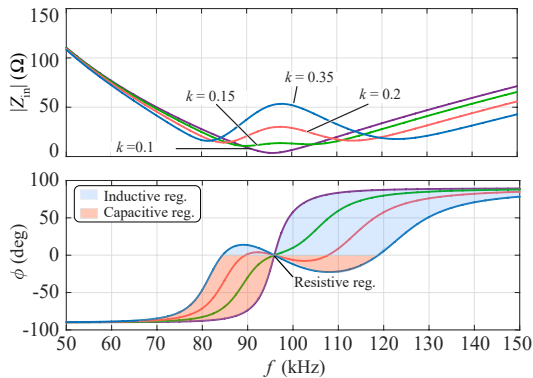
Figure 5.11: Input impedance $|Z_{in}|$ and its phase ϕ for various coupling factors (k), showing different switching modes. Switching in the inductive region results in soft-switching while the capacitive region leads to hard-switching operation. Moreover, the pole-splitting or bifurcation phenomena is also shown.

Switching modes

Depending on the angle ϕ three different zones are defined: inductive region, where $\phi > 0°$; resistive region, where $\phi = 0°$; and capacitive region, where $\phi < 0°$, as it is depicted in Figure 5.11.

Analyzing three operation zones, in Figure 5.12 three switching modes are depicted. Resistive and inductive switching modes, reduces the impact of turn-on losses with ZCS for resistive zone [see Figure 5.12(a)] and being possible to achieve ZVS turn-on when operating in the inductive zone. On the contrary, Figure 5.12(c), i.e. capacitive switching mode, presents hard turn-on losses and no turn-off losses.
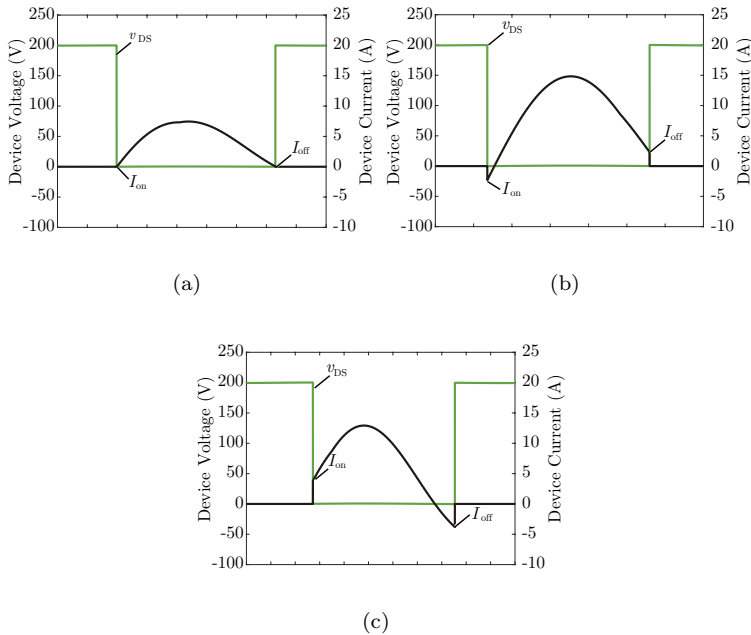
Figure 5.12: Simulation waveforms of IPT system operating in three different zones: (a) resistive, (b) inductive and (b) capacitive region.

In isolated resonant converters operating in ZVS condition, it is really important to work in the inductive region close to the resistive one. This way, there will only be turn-off losses, avoiding turn-on ones, as it is depicted in Figure 5.12(b). In dc–dc converters, using a transformer

with a high coupling factor is relatively easy to determine the capacitive and inductive regions. However, these regions are not so clear in IPT, since they depend on many factors, such as the coupling factor (see Figure 5.11) or the transferred power [159]. Thus, system with more than one pole can happen, known as pole splitting or bifurcation [138] (see Figure 5.11).

Although designers usually try to design systems without bifurcation, depending on the application requirements and system features it is not always possible. Thus, bifurcation or pole-splitting can result in an unwanted switching mode.

ZVS operation

For ZVS transition the secondary side has practically no effect, as in IPT systems the coupling is very low [137]. Thus, the equivalent circuit can be simplified into a LC system. Then, ZVS conditions presented in Section 3.4.2 can be applied but considering the equivalent capacitance formed by parasitic capacitances of semiconductors ($C_{Q,eq}$) and primary side series compensation (C_1) (5.7).

$$C_{eq} = \frac{2 \cdot C_{Q,eq} + C_1}{2 \cdot C_{Q,eq} \cdot C_1} \tag{5.7}$$

Besides, with the obtained equivalent capacitance and primary side inductance L_1, required current $I_{on,ZVS}$ (3.18), during dead-time $t_{dt,ZVS}$ (3.19) is defined in order to achieve ZVS transition. Considering this definition, different operation modes of the resonant stage with pole-splitting are analyzed for a SAB converter based on GaN devices.

5.3.2 Performance evaluation

In this section the performance of GaN-based IPT resonant stage is evaluated, considering the specifications presented in Table 5.1. The parameters of Table 5.1, correspond to the inductive pads designed in [157].

A distance of 50 mm is selected, resulting on a bifurcated system, as it is depicted in Figure 5.13(a). The presented analysis is performed varying the switching frequency in order to evaluate different operation modes and conditions. Figure 5.13(b) shows how the output power

Table 5.1: Contactless battery charger specifications.

Specifications	Value	Unit
Input voltage - V_{p}	200	V
Switching frequency voltage - f_{s}	70-130	kHz
Load resistance - R_{o}	13.2	Ω
Inductive pads parameters [157]	**Value**	**Unit**
Transmitter self inductance - L_{p}	122.5	μH
Receiver self inductance - L_{s}	62.27	μH
Coupling coefficient - k	0.37	
Transmitter resonance capacitor - C_{p}	20.95	nF
Receiver resonance capacitor - C_{s}	43.51	nF
Transmitter wire resistance - R_{p}	0.36	Ω
Receiver wire resistance - R_{s}	0.14	Ω
Transmitter resonance frequency - $f_{\mathrm{r,1}}$	95.88	kHz
Receiver resonance frequency - $f_{\mathrm{r,2}}$	96.69	kHz

varies with the switching frequency. Moreover, experimental measurements of the analyzed IPT system are included in Figure 5.13 achieving a good agreement with theoretical analysis.

In Figure 5.13(a) three different zones can be identified: capacitive, inductive iZVS and inductive ZVS. Inductive iZVS is defined as a consequence of not enough current or dead-time to achieve complete ZVS transition. In addition, power losses are estimated using the model presented in Section 3.4, with the waveforms of the IPT system obtained by PLECS simulations. ZVS conditions are calculated with the model of Section 3.4.2, but considering the equivalent capacitor (5.7). The distribution of power losses related to GaN devices are shown in Figure 5.14. Conduction losses are related to the delivered power (see Figure 5.13). Switching losses, however, not only depends on the output power but also on the switching mode defined by the equivalent impedance Z_{in} [see Figure 5.13(a)]. Figure 5.14 shows power losses distribution of GaN devices for different operation points, defined with switching frequency. Capacitive region presents turn-on losses. However, the impact of these losses for such low current are not relevant, even operating at medium switching frequency ($>70\,\mathrm{kHz}$). Besides, inductive iZVS zone also present low switching losses. Nevertheless, ZVS inductive zone shows up the lower switching losses, even at higher
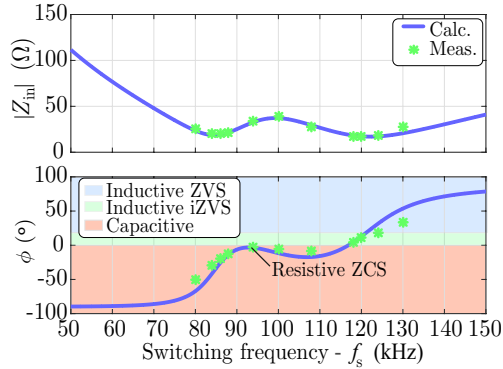
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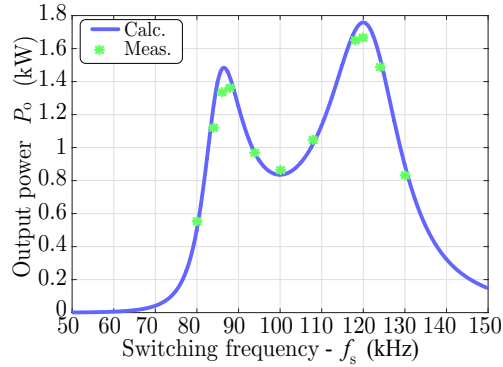
(b)

Figure 5.13: Theoretical (Calc.) and experimental measurements (Meas.) of characteristics of the contactless battery charger in terms of the switching frequency: (a) equivalent primary side converter impedance and (b) transferred power.

switching frequency (>110 kHz). In addition, it has to be noted, that dead-time losses need to be considered when operating at high switching frequencies (>120 kHz), as it is depicted in Figure 5.14.

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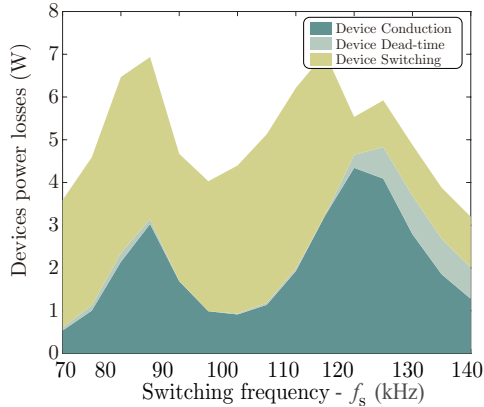
Figure 5.14: Power switches losses of the contactless battery charger in terms of the switching frequency. The distribution of power losses is presented differing between conduction, switching and dead-time losses.

5.3.3 Experimental measurements

The inductive pads presented in [157] are used for experimental measurements, along with the GaN-based power boards presented in [54] (see Figure 5.15). Two power boards with parallel connected GaN devices are used forming a full-bridge. Afterwards, the results presented in Figure 5.13 are validated through experimental measurements. Figure 5.13 shows a good agreement between theoretical analysis and experimental results. Moreover, different operation modes are evaluated in order to validate power losses of GaN devices for a resonant system.

In Figure 5.17 primary side voltage and current are depicted for three operation modes: capacitive (hard-switching), resistive (ZCS), incomplete inductive (iZVS) and inductive (ZVS).

For the estimation of power losses at the operation points presented in Figure 5.17, the calorimetric method proposed in Section 3.4.5 is used, measuring the heatsink temperature of both power boards. A good approximation of power losses is obtained for every operation mode (see Figure 5.16).

Therefore, it is demonstrated that the use of GaN devices reduces turn-on power losses in the capacitive region, limiting the uncertainty caused by the bifurcation phenomena. However, it is relevant to ensure an inductive region operation ZVS, if devices with relevant turn-on
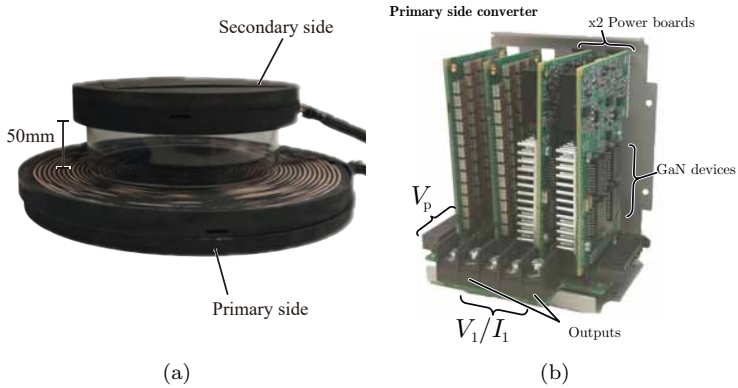
Figure 5.15: Experimental validation set-up of the IPT system: (a) photograph of the developed primary and secondary inductive pads with compensation described in [157] (b) GaN-based converter presented in [54] in full-bridge configuration.
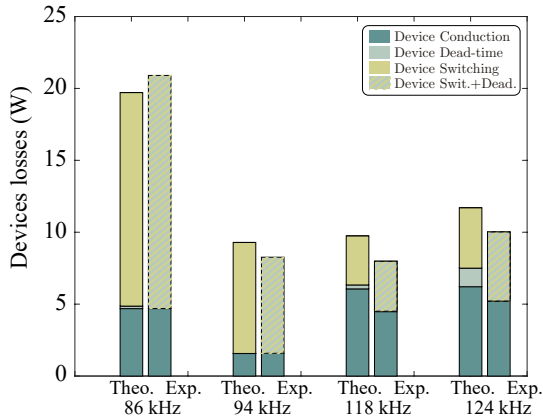
Figure 5.16: Experimental validation of GaN devices performance operating an IPT system. Experimental distribution of devices power losses compared to theoretical results (V_{in}=200 V).

losses, such as Si Super-Junction devices are used as it is analyzed in [138] comparing Si and GaN devices. Moreover, for an excessive switching frequency increase, dead-time losses relevance is higher, as it

(a)

(b)

(c)

(d)
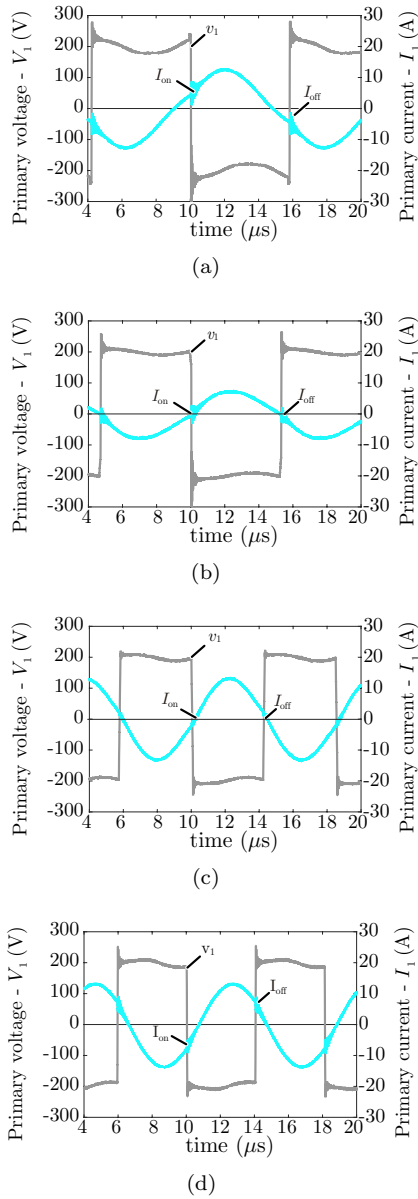
Figure 5.17: Experimental curves at different operation modes (V_i=200 V): (a) 84 kHz hard-switching, (b) 94 kHz ZCS, (c) 118 kHz iZVS and (d) 124 kHz ZVS.

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is depicted in Figure 5.16. This is a consequence of higher switching currents and higher switching frequency (see Figure 5.17).

5.4 Multi-cell HV: MMC

It is a well-known fact that the increase of operation frequency usually reduces the volume of magnetic elements (see Appendix A.0.3), something already analyzed for medium/low-power applications in this work (Section 5.2, 5.3). Furthermore, this fact is becoming a reality in high-power applications due to the use of multilevel configurations, such as the MMC. The benefits and limitations of MMC are analyzed with the aim of taking advantage of high-frequency devices on high-power applications. The main advantages of MMC in medium and high-voltage applications are: its scalability, modularity and redundancy due to the series connection of cells; the possibility to operate without output filters or transformers and its good dynamic characteristics thanks to the increase of the switching frequency [149]. Figure 5.18 shows a three phase MMC with N_{sm} number of SM per arm, while two arms conform a leg or phase. Although there are other configurations presented in the literature, the most commonly used is the half-bridge SM [160].

The main aspects to consider during the design and control of a MMC, together with a frequency analysis is presented in following subsections. Furthermore, power losses distribution and volume impact of different components are evaluated.

5.4.1 Operation principles

SMs of a MMC work as small dc sources, connecting/disconnecting each capacitor C_{sm} to the arm. Whenever the arm voltage increases, more SMs are going to be inserted into the system; in contrast, the capacitors will be bypassed when the voltage level must be reduced. Nevertheless, when capacitors are connected/disconnected from the system they suffer a charging/discharging process, which could derive into an instability problem. To overcome this issue, different controls related to capacitor voltage balancing are implemented. The voltage across the SM (V_{sm}) is defined considering the number of SMs N_{sm} and dc-link voltage (V_{dc}):

$$V_{sm} = \frac{V_{dc}}{N_{sm}} \tag{5.8}$$

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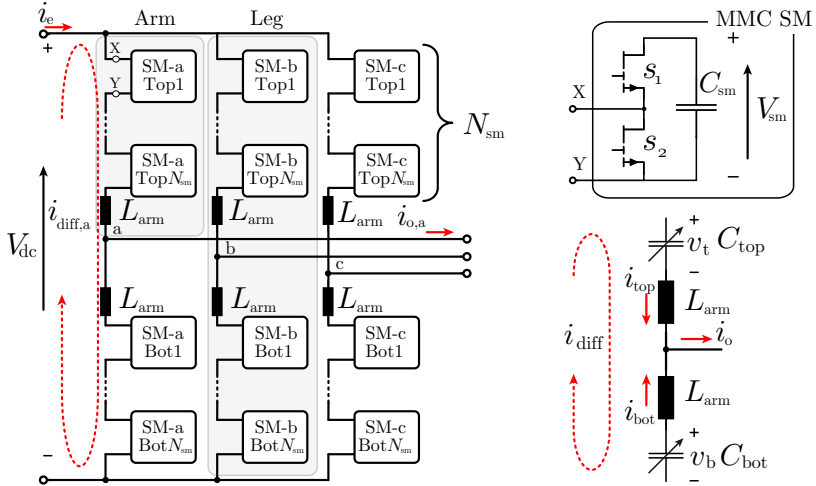
Figure 5.18: MMC based on GaN devices with N_{sm} number of SMs with a half-bridge configuration.

Figure 5.18 shows the equivalent circuit of one MMC leg. The analysis is focused on a single MMC leg, but all the arguments can be directly extended to two or three phase systems. It is assumed that the dc-link is connected to two controlled variable capacitors (C_{top} and C_{bot}); which capacitance evolves sinusoidally. Each of these equivalent capacitors represents one arm of the converter. Two different currents flow through the circuit, as it is depicted in Figure 5.18. On the one hand, the circulating or differential current (I_{diff}), which charges or discharges the voltage of the capacitors, and is created by the unbalance between the dc-link and the sum of both arm voltages. On the other hand, the output current (I_o), which is, theoretically, equally shared between both arms of the same leg, if equal internal resistance of the controllable capacitors and equal line impedances (L_{arm}) are assumed:

$$I_o = I_{top} - I_{bot}$$
$$\text{being} \quad I_{top} = \frac{I_o}{2} + I_{diff}, \quad I_{bot} = -\frac{I_o}{2} + I_{diff} \tag{5.9}$$

Therefore, the most important parameters during the design of a MMC are: the voltage (5.8) and current ratings (5.9) of power devices

and the design of SM capacitors C_{sm} and arm inductors L_{arm}. In addition, the control of the MMC needs to be especially considered in order to achieve a balanced system.

Reactive components

The sizing of C_{sm} and L_{arm} are key factors during the design of a MMC, since they largely define the weight and the size of the overall system. The tendency of these reductions is relatively clear in some power converters with a unique operation frequency, such as dc-dc converters (Section 5.2), but the impact of frequencies on reactive components of a MMC is not so evident, and further analysis is required.

The capacitor of each SM (C_{sm}) must be large enough to limit the voltage ripple and satisfy the voltage requirements of all components. Considering that the sum of all cells that conform an arm can be modeled as an equivalent capacitor, and knowing that the arm current is sinusoidal (about the half of the output current), it can be deduced that the C_{sm} depends on the transferred power and the fundamental frequency f_o. The value of the minimum C_{sm} to obtain a certain voltage ripple (Δv_c) can be calculated using (5.10) [140, 149]:

$$C_{sm} \geq \frac{P_o \cdot \cos \phi}{3 \cdot N_{sm} \cdot \Delta v_c \cdot V_{sm}^2 \cdot m_a \cdot \omega} \cdot \sqrt{\left[1 - \left(\frac{m \cdot \cos \phi}{2} \right)^2 \right]^3} \quad (5.10)$$

where P_o is the transferred power by the converter, V_{sm} the capacitor mean voltage value, m_a the modulation index, ω_o the angular output frequency and ϕ the angular displacement of the load.

The L_{arm} of a MMC has three main tasks. First, it serves as a link inductor, limiting the arm current in each commutation and making possible exchanging energy between the converter and the ac system. Second, it limits the currents in case of faults. And third, it is used to reduce the circulating currents and their resonance among arms [140]. In this context, the inductor value depends on the switching frequency, and its value can be deduced with (5.11) [140]:

$$L_{arm} \geq \frac{V_{dc}}{8 \cdot N_{sm}^2 \cdot f_s \cdot \Delta i \cdot I_{diff}} \quad (5.11)$$

being $\Delta i \cdot I_{diff}$ the maximum current ripple.

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Control strategy

The MMC topology needs multiple control techniques, in order to regulate current and voltage values within the safe operation area. Control strategy of this work contains: current control, total voltage balancing, differential voltage balancing, differential current suppressing and capacitor voltage balancing. This control strategy is analyzed in detail in [140]. With the implemented control strategy, voltages of SMs are balanced, as it is depicted in Figure 5.19(a). Moreover, the differential current $I_{\mathrm{diff},j}$ is reduced [see Figure 5.19(b)].

(a)   (b)
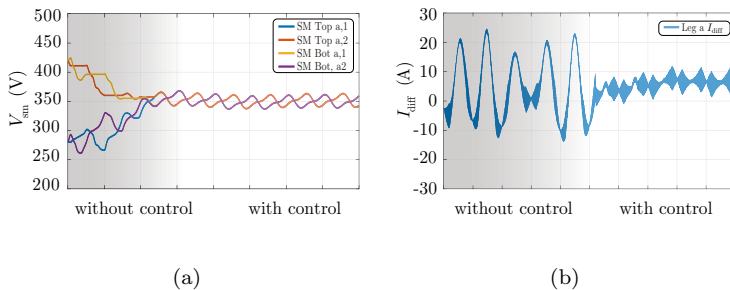
Figure 5.19: Implemented control strategy response: (a) voltage balancing of each SM and (b) differential current reduction.

Frequency influence analysis

Figure 5.20 shows the differential current of each leg ($I_{\mathrm{diff},j}$) together with the amount of SM voltages ($V_{\mathrm{c},j}$) for different frequency combinations. For this analysis fixed value of C_{sm} and L_{arm} are considered, in order to evaluate the impact of frequencies on current and voltage ripples [140].

It is demonstrated that the impact of the fundamental frequency only affects to the capacitor, and it is inversely proportional to the required capacitive value. Moreover, the inductor current ripple ($\Delta i \cdot I_{\mathrm{diff}}$) depends on the switching frequency (see Figure 5.20) (5.11).
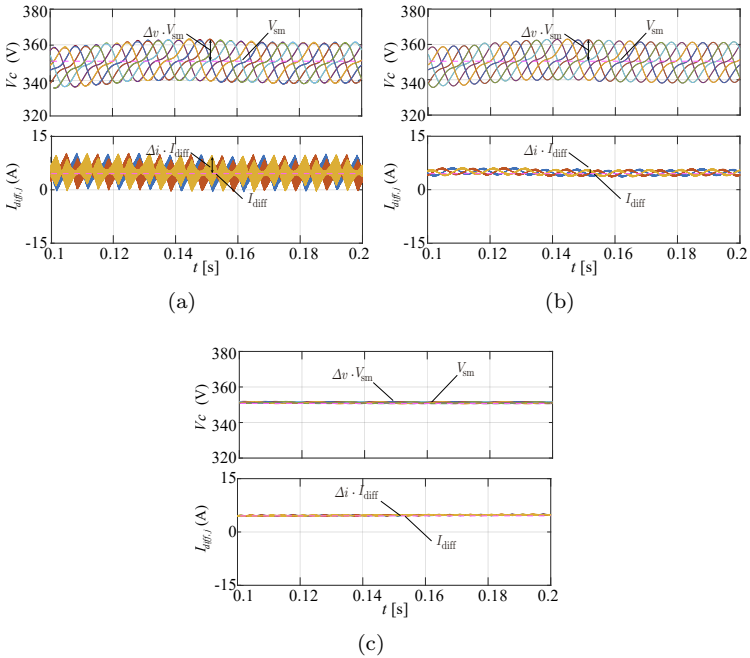
Figure 5.20: Fundamental and switching frequency impact on the voltage and current ripple ($C_{sm} = 1\text{mF}/L_{arm} = 1\,\text{mH}$). Voltage of SMs ($V_{c,j}$) and three-phase differential current $I_{diff,j}$ for different frequencies: (a) $f_o = 50\,\text{Hz}$, $f_s = 10\,\text{kHz}$, (b) $f_o = 50\,\text{Hz}$, $f_s = 200\,\text{kHz}$ and (c) $f_o = 1\,\text{kHz}$, $f_s = 200\,\text{kHz}$.

Power switches

Current and voltage switching waveforms at sub-module level are analyzed in order to define the requirements of semiconductors. Considering N_{sm}, it is clear that the switching voltage is the voltage that each SM withstands (5.8). Regarding the current, each arm conducts the half of output current (5.9). Figure 5.21 shows dc-link voltage and output current along with the voltage and current of a SM-switch. The switching current is the half of the output current with an offset related to the differential current, as it is depicted in Figure 5.21(a).

In addition, switching losses are obtained analyzing switching energies of each switching instance, during a fundamental period [see Fig-

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(a)

(b)
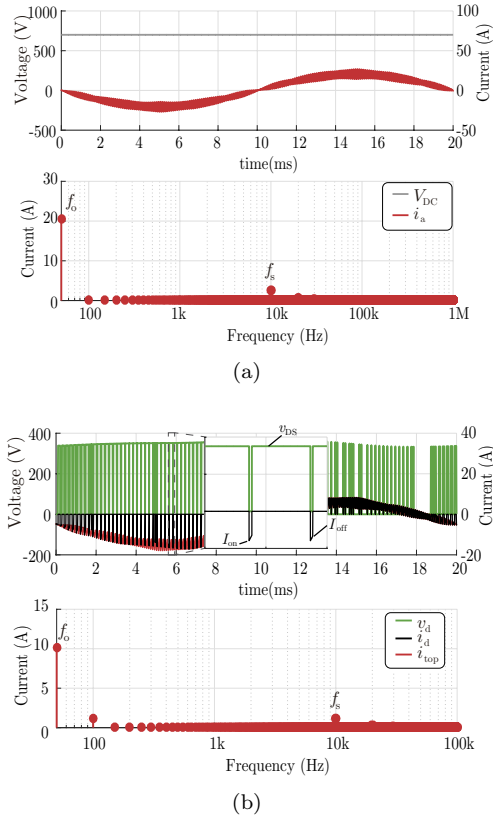
Figure 5.21:   Key waveforms of a MMC working with 2 SMs
(V_{dc}=700 V/$I_{o,RMS}$=16 A): (a) input dc-link and output current, and (b)
switching voltage and current of the SM, along with the arm current (i_{top}).

ure 5.21(a)]. Then, the average switching energy is obtained, dividing
the sum of total energy by the number of switching instances (5.12).

$$P_s = \frac{f_{s,n}}{n_{sw}} \cdot \sum_{i=1}^{n_{sw}} E_{s,i} \tag{5.12}$$

where the average natural switching frequency $f_{s,n}$ is obtained consid-
ering the fundamental frequency f_o and number of switching instances

n_{sw}

$$f_{\text{s,n}} = \frac{n_{\text{sw}}}{f_{\text{o}}} \approx \frac{f_{\text{s}}}{N_{\text{sm}}} \tag{5.13}$$

being the natural switching frequency approximated to the switching frequency divided by the number of SMs.

This is a consequence of the implemented balancing control that toggles between the number of SMs in order to balance the voltage of each cell. Thus, the impact of switching losses related to power devices is reduced, as it will be analyzed in following sections.

5.4.2 Performance evaluation

For this analysis, the MMC is configured as a three-phase MVD. In this manner, the impact of frequencies is evaluated as both frequencies can vary, i.e. switching frequency and fundamental frequency. Considering the specifications presented in Table 5.2, an analysis of GaN-based MMC is presented in this section, as a more detailed extension of the analysis presented in [140]. MMC-MVD is evaluated considering the proposed control strategy (Section 5.4.1) and devices presented in Chapter 2 (IGO60R070D1 [108]). The control strategy is developed in Matlab-Simulink, while for the power stage PLECS simulation tool is used. The presented results can be scaled for N_{sm} number of SMs.

Table 5.2: Scaled MVD specifications, for a MMC.

Specifications	Value	
Input HVDC voltage - V_{dc}	700	V
Output ac phase RMS voltage - V_{ac}	230	V
Output ac frequency - f_{o}	50-1k	Hz
Switching frequency - f_{s}	10k-200k	Hz
Output power - P_{o}	10	kW
Cell capacitor voltage - V_{sm}	350	V
Number of cell per arm - N_{sm}	2	
Arm current ripple - Δi	0.3	
Cell voltage ripple - Δv	0.1	

The influence of the switching and fundamental frequencies on the performance of the MMC is evaluated, considering the design of reactive components (5.10), (5.11). Moreover, power losses at SM level are analyzed, evaluating the impact of GaN devices on the performance.

Then, power losses and volume of whole converter are shown, considering the approximation models presented in Chapter 3. Thus, the benefits and limitations of working with high-performance GaN devices are evaluated.

GaN devices performance

Once the effect of system frequencies on converter response are analyzed in Section 5.4.1, power losses distribution related to GaN devices is analyzed considering the specifications presented in Table 5.2. Power losses of the SM are evaluated for switching frequencies combinations presented in Figure 5.20. The power losses distribution for a balanced MMC presents low difference among every SM, as it is evaluated in [140]. Therefore, power losses at SM level are analyzed. Figure 5.22 shows the high relevance of conduction losses, even when operating with high switching frequencies. Then, parallel connected devices are preferred, resulting in lower power losses [see Figure 5.22]. Moreover, as it is expected fundamental frequency does not affect to power losses of devices, as can be deduced from Figure 5.22.
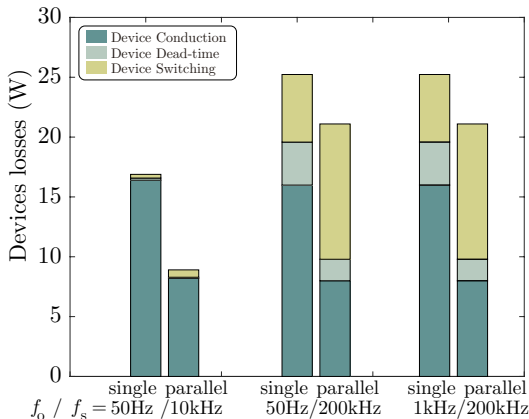
Figure 5.22: Analytical power loss distribution analysis of GaN-based SMs. Conduction losses (P_c), dead-time losses (P_s) and switching losses (P_s) for different frequencies: $f_o = 50\,\text{Hz}$, $f_s = 10\,\text{kHz}$; $f_o = 50\,\text{Hz}$, $f_s = 200\,\text{kHz}$ and $f_o = 1\,\text{kHz}$, $f_s = 200\,\text{kHz}$.

In addition, power losses of the SM are evaluated for various switching frequencies and number of SMs. Figure 5.23(a) shows the effect

of number of SM on semiconductors power losses. The use of more SMs reduces especially switching losses, as a result of lower blocking voltage and lower natural switching frequency of each cell. However, the number of semiconductors increases by $N_{sm} \cdot 4$, when analyzing overall converter losses. Thus, losses related to semiconductors increases, when the same semiconductor is used, as it presented in Figure 5.23(b). However, when semiconductor blocking voltage is reduced until 150 V, LV GaN devices can be used [161]. In this manner, overall power losses of power switches are reduced, as it is shown in Figure 5.23(b) for N_{sm}=6. This is a consequence of lower conduction an better switching capability of LV devices [161]. Thus, a trade-off between losses and system complexity needs to be analyzed. In this case N_{sm}=2 is selected for the sake of simplicity.

Converter performance

Regarding the performance at converter level, power losses and volume distribution is presented in Figure 5.24 for the specifications presented in Table 5.2. Ceramic capacitors are considered for this analysis.

Figure 5.24(a) shows the impact of switching frequency on semiconductors and inductor losses. Furthermore, Figure 5.24(b) shows the low impact of switching frequency on the converter overall volume, as a consequence of higher relevance of the volume of capacitors in comparison with inductors.

Indeed, low switching frequency is preferred, resulting in ultra-high efficient system, when operating with low fundamental frequency. Instead, it will be interesting to operate at high switching frequency only for high fundamental frequency systems, i.e. high speed MVD [140]. In this case, the volume of the converter is considerable reduced. However, it has to be noted that modular multi-cell converters, such as MMC, rarely achieve better power density features than single-cell converters. Nevertheless, modular multi-level structure allows the connection of the power converter to a high-voltage terminals (much higher that the devices voltage rating) by means of the boxes series connection. In this manner, high performance devices such as GaN devices can be used, resulting in low power losses. Moreover, depending on the input voltage value, the number of boxes could be increased. Besides, redundancy of modules could increase the availability and reliability of the system.

Therefore, the use of GaN devices results on MMC with low power losses, being possible to achieve high efficiency. However, the increase

(a)

(b)
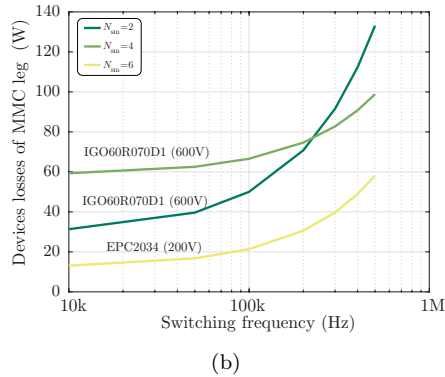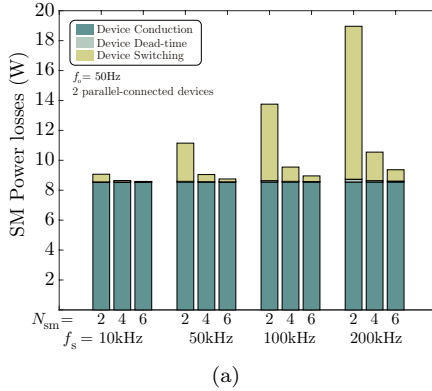
Figure 5.23: Power losses analysis of GaN devices for different number of SMs and switching frequencies: (a) distribution of each SM and (b) total losses of GaN devices.

of switching frequency has not a clear benefit for applications with low fundamental frequency. These results are experimentally validated.

(a)

(b)
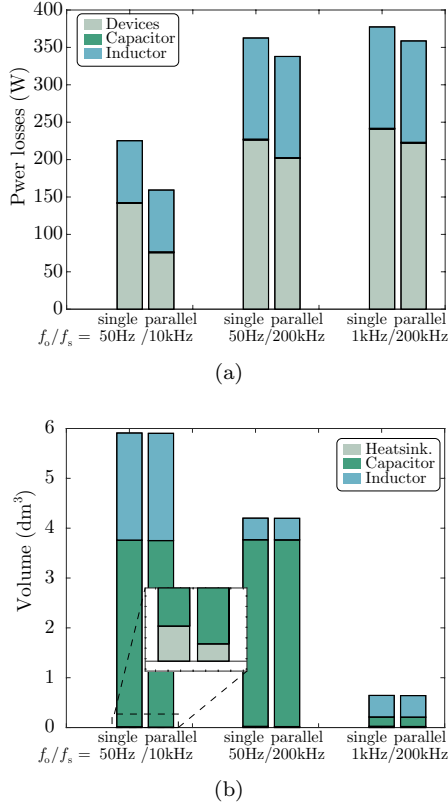
Figure 5.24: Performance analysis of MMC converter for various switching and fundamental frequencies: (a) losses distribution and (b) volume distribution, without considering control and housing.

5.4.3 Experimental measurements

Power boards depicted in Figure 3.3 are used in half-bridge configuration, forming a three-phase MMC (see Figure 5.25). Each module contains the power board based on GaN devices and C_{sm}. The MMC is analyzed for the specifications presented in Table 5.2 for a switching frequency of 20 kHz and a fundamental of 50 Hz.

The control strategy is validated achieving a balanced system, as it is depicted in Figure 5.26(a) for the capacitor voltages of one leg.

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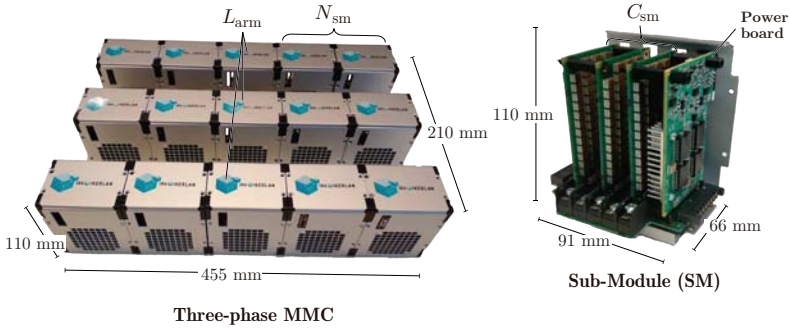
Figure 5.25: MMC experimental set-up based on GaN power modules, $980\,\mu\text{C}$ ceramic capacitors (C_{sm}) and $1\,\text{mH}$ inductors (L_{arm}).

Besides, Figure 5.26(b) shows the achieved low output current, working at nominal operation point.
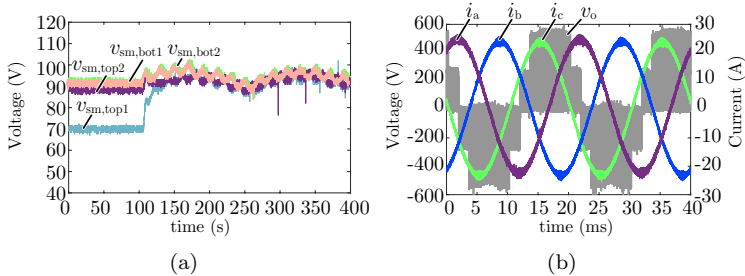
Figure 5.26: Experimental waveforms of the GaN-based MMC: (a) capacitor voltage balancing and (b) three-phase output currents with one line-to-line voltage at nominal operation ($10\,\text{kW}$).

Then, the performance of the converter is evaluated at different loads, achieving high efficiency, as it is shown in Figure 5.27(a). Moreover, high efficiency is achieved over the whole output load range. Regarding the volume distribution, the high impact of capacitors on the overall volume is demonstrated, as a consequence of low fundamental frequency [see Figure 5.27(b)].
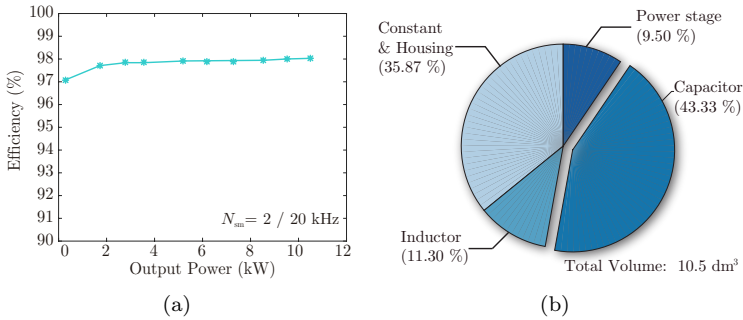
Figure 5.27: Experimental performance analysis of the MMC converter: (a) efficiency and losses for various output load and (b) volume distribution without considering the control board.

5.5 Multi-cell LV: M2BF

The proposed multi-cell flyback configuration has a modular structure with N_a primary and N_b secondary side number of cells, as it is depicted in Figure 5.28. The main switch is four quadrant switch, in order to connect/disconnect cells in accordance to system requirements. In addition, auxiliary windings with a diode are included for safety reasons, as it will be analyzed in Section 5.5.1.
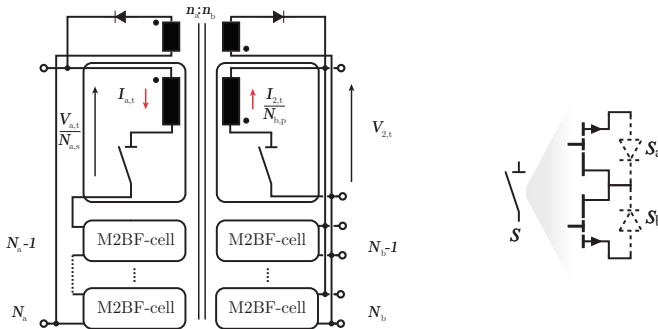
Figure 5.28: M2BF concept configured with input-series and output-parallel cells.

One of the main drawbacks of a flyback is that it requires semi-

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conductors with higher voltage and current capability than other conventional converters. This is a consequence of induced voltages and currents [162]. Multi-cell systems results on either distribute the voltage between N_s series-connected cells or share the current along N_p parallel-connected cells. The proposed architecture allows to configure cells in order to reduce maximum voltage (5.14) and current (5.15) requirements of primary or secondary sides.

$$
\begin{aligned}
V_{a,i} &\approx \frac{V_{1,t}}{N_{a,s}} + \frac{V_{2,t} \cdot n}{N_{2,s}}, \\
V_{b,i} &\approx \frac{V_{1,t}}{N_{1,s} \cdot n} + \frac{V_{2,t}}{N_{2,s}}
\end{aligned}
\tag{5.14}
$$

$$
\begin{aligned}
I_{a,i} &\approx \frac{I_{1,t}}{N_{1,p}}, \\
I_{b,i} &\approx \frac{I_{2,t}}{N_{2,p}}
\end{aligned}
\tag{5.15}
$$

where n is the transformer ratio (n_1/n_2) and $V_{1,t}$, $I_{1,t}$ and $V_{2,t}$, $I_{2,t}$ are the total voltage and current of primary and secondary sides, respectively. Figure 5.28 presents an input-series output-parallel configuration reducing the voltage requirement of primary side cells (N_1) and the current of secondary side cells (N_2).

5.5.1   Operation principles

The most differential characteristics and control strategy of the M2BF are presented in this section. The power delivery of M2BF is similar to a conventional flyback, but considering the number of connected cells and a bidirectional power flow control. The power delivery can be divided into two intervals: magnetizing and demagnetizing process. Assuming a current flowing from primary to secondary side, the magnetizing process begins with the turn-on of primary side main switch $s_{1,i}$, storing the energy on the transformer. Then, when turning-off $s_{1,i}$, the energy stored in the transformer is discharged on the secondary side, as it is shown in Figure 5.29(a) with two connected cells on each side.

On the contrary, considering a current flowing from secondary to primary side, magnetizing period is performed on the secondary side while demagnetizing occurs at primary side [see Figure 5.29(b)].
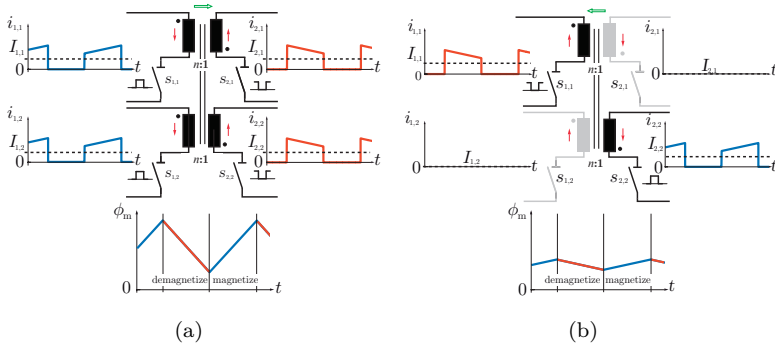
Figure 5.29: M2BF concept along with magnetic flux (ϕ), primary ($i_{1,\text{i}}$) and secondary ($i_{2,\text{i}}$) side currents for different configurations: (a) primary to secondary power flow with two connected cells on each side and (b) secondary to primary flow with one active cell on each side.

Furthermore, the magnetic flux of the transformer (ϕ_{m}) is proportional to the sum of primary and secondary side currents. Thus, in the M2BF, ϕ_{m} changes according to the sum of the current generated on each cell (5.16). Figure 5.29(b) shows how ϕ_{m} is decreased when enabling only one cell of each side in comparison with the configuration presented in Figure 5.29(a).

$$\phi_{\text{m}} = \left(\sum_{i=1}^{N_1} \frac{i_{1,\text{i}}}{n_1} + \sum_{i=1}^{N_2} \frac{i_{2,\text{i}}}{n_2} \right) \cdot L_{\text{m}} \tag{5.16}$$

being L_{m} the magnetizing inductance.

Design considerations

Regarding the sizing of converter components, it is similar to a conventional flyback, being the main difference related to the multi-winding transformer. Multi-winding transformer with $N_1 + N_2 + 2$ number of windings is required. Two of these windings are known as auxiliary windings. These auxiliary windings are connected with diodes to primary and secondary sides as it is depicted in Figure 5.28. These windings do not operate at normal operating conditions. These auxiliary windings only operate in case of system-failure providing a discharging path for the current. Moreover, they are designed with a transformer

relation of $n/n_{\text{aux}} > 1$, but close to the unity in order to avoid excessive induced overvoltage, in case of failure.

Analyzing the equivalent circuit of a transformer depicted in Figure **??**, the magnetizing inductance is defined with (5.17) for a certain current ripple Δi and switching frequency f_{s} [162]. The Δi defines the operation mode of a flyback. In this case, a continuous conduction mode is considered, avoiding excessive conduction losses produced by high current ripple operation modes.

$$L_{\text{m}} = \frac{V_{\text{in}} \cdot \delta}{2 \cdot f_{\text{s}} \cdot \Delta i \cdot I_{\text{Lm}}} \tag{5.17}$$

being δ the voltage conversion ratio and I_{Lm} the magnetizing current defined as follows:

$$\delta = \frac{n \cdot V_{\text{o,i}}}{n \cdot V_{\text{o,i}} + V_{\text{in,i}}} \tag{5.18}$$

$$I_{\text{Lm}} = \sum_{i=1}^{N_1} \frac{P_{\text{o,i}}}{\eta \cdot V_{\text{in,i}}} + \sum_{i=1}^{N_2} \frac{I_{\text{o,i}}}{n} \tag{5.19}$$

being n the transformer conversion ratio, $P_{\text{o,i}}$ output power, $V_{\text{o,i}}$ output voltage and $V_{\text{in,i}}$ input voltage of cell i. The maximum current I_{Lm} is a result of the sum of all cells currents.

Then, considering the worst case scenario, i.e. the minimum δ and the peak magnetizing current, L_{m} is defined. Moreover, the transformer is designed to have a reduced leakage inductance L_{lk} $(3 - 5\% \cdot L_{\text{m}})$ to reduce the overvoltage generated on the main switch.

Every coil of multi-winding transformer is formed by its own inductance and the mutual impedance between coils divided into two sides (p primary and s secondary). Then, the equivalent inductance matrix is defined with (5.20) for i number of windings.

$$\begin{bmatrix} L_{\text{1p,1p}} & L_{\text{1p,1s}} & \dots & L_{\text{1p},is} \\ L_{\text{1s,1p}} & L_{\text{1s,1s}} & \dots & L_{\text{1s},ip} \\ \vdots & \vdots & \vdots & \vdots \\ L_{is,\text{1p}} & L_{ip,\text{1s}} & \dots & L_{is,is} \end{bmatrix} \tag{5.20}$$

where $L_{\text{1p,1s}}$ corresponds to the mutual inductance between first primary and first secondary coils.

The multi-winding coils are distributed in a symmetrical way, in order to reduce the leakage inductance of each module. Moreover, primary

and secondary windings are interleaved, as it is shown in Figure 5.30 for six winding transformer: four main coils and two auxiliary. The diameter of the wire of auxiliary windings is reduced as these coils only operate in case of system failure. More details on the design of the transformer are included in [163].
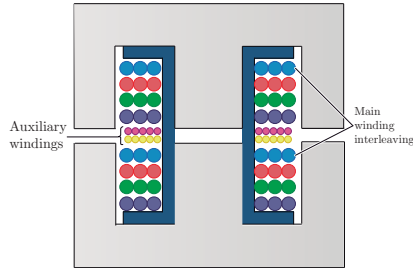
Figure 5.30: Winding distribution of the multi-winding flyback transformer for a reduced leakage inductance.

In addtion, flyback cells are operated with an active clamp circuit, in order to reduce switching losses. Active clamp is implemented in both sides due to the bidirectional operation of the converter. Considering the leakage inductance, clamp capacitor C_{r} is selected to be in resonance with L_{lk} at a switching frequency f_{s} (A.9). Besides, devices output capacitances are not considered as GaN devices present negligible C_{oss} in comparison to C_{r}.

$$C_{\mathrm{r}} = \frac{1}{(2 \cdot \pi \cdot f_{\mathrm{s}})^2 \cdot L_{\mathrm{lk}}}. \tag{5.21}$$

Bidirectional switch

Four quadrant flyback is proposed, based on two anti-series semiconductors for primary and secondary sides. Figure 5.31(a) shows how $s_{\mathrm{b1,2}}$ blocks the current on the primary side ($i_{1,2} = 0$) and $s_{\mathrm{b2,1}}$ on the secondary side ($i_{2,1} = 0$), when the current is flowing from primary

to secondary side. Conversely, considering a current flowing from secondary to primary side, $i_{2,1}$ yields to zero due to the blocking capability of $s_{a2,1}$ while the same is true for $s_{a1,2}$ device on the primary side [see Figure 5.31(b)]. Hence, bidirectional voltage and/or current conduction and blocking capability is achieved. However, the implementation
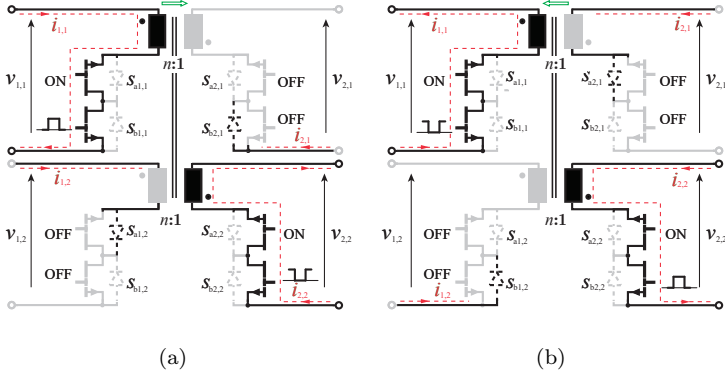
Figure 5.31: Bidirectional switches based on GaN devices with "body diode" (dashed lines): (a) current flowing from primary to secondary side and (b) current flowing from secondary to primary side.

of bidirectional switch results on higher number of semiconductors than for a conventional flyback and consequently higher conduction losses. Therefore, devices with low conduction resistance, such as GaN semiconductors, are presented as the most suitable solution. Besides, in near future, monolithically integrated bidirectional GaN devices will overcome this limitations with significantly lower conduction losses [164]. The lateral structure of GaN devices (see Figure 2.1), allows to include a second gate near the drain, achieving a bidirectional power semiconductor without an increase of the conduction resistance [165].

Control strategy

Figure 5.32 shows the implemented control strategy. Current control is performed measuring current ($i_{1,i}, i_{2,i}$) of each cell. Besides, peak current detector is implemented by hardware and then calibrated to obtain the relation between peak current and delivered current. Moreover, the voltage of each cell is measured, in order to obtain the power of every cell.
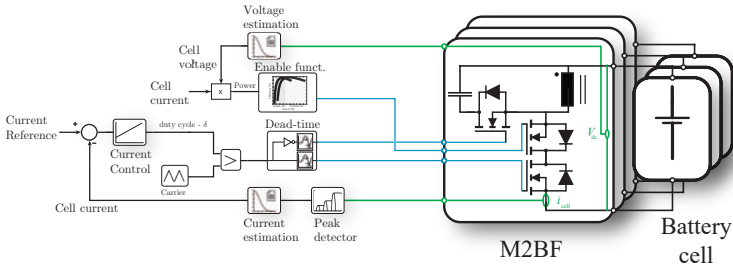
Figure 5.32: M2BF converter control scheme.

In addition, control signals of switches are enabled or not depending on the power flow and the enable function. In this first control strategy approach, an enable function that results on the highest efficiency is implemented. Thus, the number of connected cells is selected in terms of the required power. The impact of number of cells on the system efficiency is analyzed hereafter.

It has to be noted that the enable function can be defined for different system parameters. Indeed, multiple loads and sources can be controlled independently, as for DC-PDS systems [see Figure 5.2(a)]. Moreover, in the case of ESS operating with series connected cells [see Figure 5.2(b)], enable function is designed in terms of the State of charge (SoC), being possible to perform an integrated active balancing of cells, as in the active equalizer presented in [166].

5.5.2 Performance evaluation

Once the M2BF architecture is described, power converter performance is evaluated for the specifications of Table 5.3. Figure 5.33(a) shows a dc-dc M2BF with active clamp switches ($s_{c1,i}$, $s_{c2,i}$) and clamping capacitors (C_r). The same switches configuration is implemented in both sides as the power can be delivered in both directions.

Figure 5.33(b) shows the voltage that C_r has to withstand and the current of the primary side ($i_{1,i}$). Negative leakage current is allowed on the primary side, due to clamping circuit.

Moreover, considering primary to secondary power flow, switching transitions of power switches are analyzed in Figure 5.34. ZVS of primary switch $s_{a1,1}$ is achieved due to active clamp. Besides, Figure 5.34

Table 5.3: M2BF cell electrical specifications.

Description	Value	Unit
Input voltage - $V_{1,\text{i}}$	24	V
Output voltage - $V_{2,\text{i}}$	24	V
Output current - $I_{2,\text{i}}$	5	A
Current ripple - Δi	0.2	
Transformer ratio -n	1	
Transformer auxiliary ratio -n_{aux}	1.2	
Switching frequency - f_{s}	300	kHz
Semiconductor characteristics	**Value**	**Unit**
Case-to-heat-sink resistance $R_{th,c-h}$	4.5	°C/W
Junction-to-case resistance $R_{th,j-c}$	0.3	°C/W
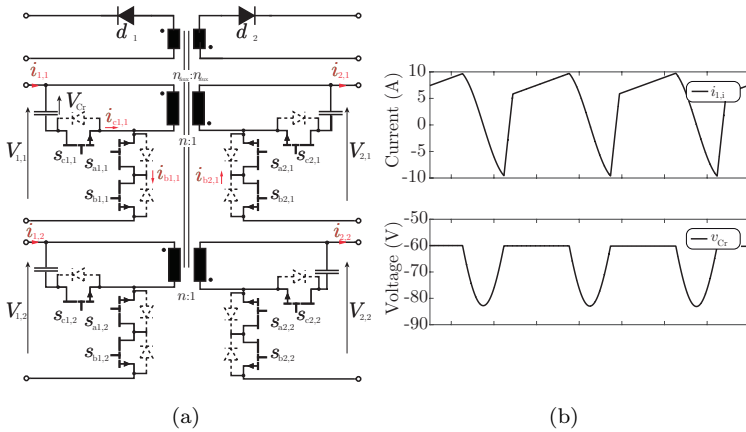
Figure 5.33: M2BF converter based on GaN devices, with two primary and secondary side cells and active clamp: (a) topology scheme and (b) key waveforms, C_{r} voltage and L_{lk} current.

shows the switches control signals considering a power flow from primary to secondary side and enabling only one cell on each side.

Primary main switch $s_{\text{b1},1}$ is switching with a duty δ while switch $s_{\text{b2},1}$ and clamping switch $s_{\text{c1},1}$ toggles complementary to $s_{\text{b1},1}$ with a defined dead-time t_{dt}. A minimum dead-time of 45 ns is defined, considering the analysis presented in Section 2.3, characteristics of the selected
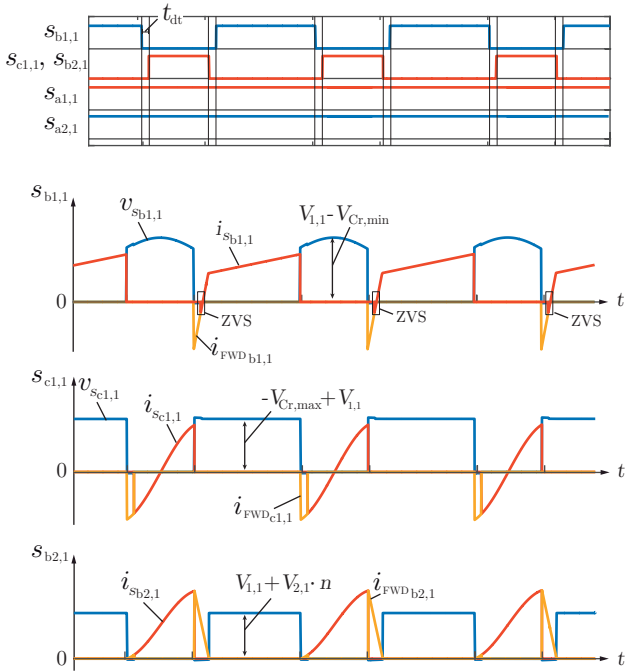
Figure 5.34: Power switches transitions of M2BF, including its "body diodes" conduction instances.

LV GaN devices (EPC2034 [161]) and driver delay times. Besides, anti-series switches $s_{a1,1}$ and $s_{a2,1}$ are continuously conducting according to enable function due to the free-wheeling conduction instances. The same control sequence of anti-series switches is applied if the current is flowing from secondary to primary side, i.e. switching with $s_{b2,i}$ and continuously with $s_{a2,i}$.

GaN devices performance

Power losses distribution is evaluated, adapting the power losses estimation method proposed in Section 3.4 to flyback switching waveforms. Figure 5.34 shows switching waveforms of each switch that conform the M2BF. Soft-switching operation is achieved operating near to resonance frequency f_r. ZVS operation of main switches of primary and secondary

sides is achieved along with soft turn-on of clamping switches. In addition, conduction instances of the "body diode", i.e. dead-time, have to be also considered.

Figure 5.35 shows the power losses distribution of each switch. Assuming a power flow from primary to secondary side, primary side presents main switch, auxiliary switch and clamp switch losses. On the contrary, secondary side cell only presents main switch and auxiliary switch losses. The use of active clamp reduces switching losses relevance, being negligible even operating at 300 kHz, as a consequence of reduced turn-off losses.

It is worth to pointing out that the use of two anti-series device as main switch increases total conduction power losses. In near future monolithically integrated GaN devices will be possible, with significantly lower on-state resistance than two devices in anti-series [165], reducing conduction losses.

The use of GaN devices in this topology allows to reduce conduction losses and switching losses, due to the low turn-off losses. However, dead-time losses of synchronous devices needs to be considered, as an important part of synchronous device losses.

In addition, Figure 5.35 compares power losses distribution of a M2BF operating with single cell and two cells, for a primary to secondary power flow of 120 W. Comparing both variants, conduction and dead-time losses are reduced while switching losses increase when considering two connected cells. Then, depending on the impact of conduction, dead-time and switching losses, the optimal number of connected cells will be different. Thus, the performance in terms of power losses of the converter is experimentally evaluated, in order to define the optimal number of connected cells for various load currents.

5.5.3 Experimental validation

This section presents the power cells of the GaN-based M2BF. The power cell is composed of a power board and a conditioning board, as it is depicted in Figure 5.36. The power converter is based on LV GaN devices resulting in a power module with reduced size.

The presented power module is configured to operate as a synchronous buck converter, in order to validate the performance of LV GaN devices operating at high-switching frequency. The analysis presented in Section 2.5 is used to define gate driver circuit, achieving
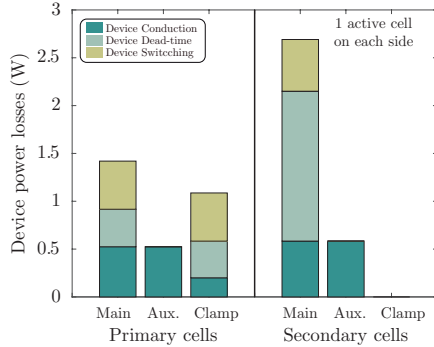
(a)
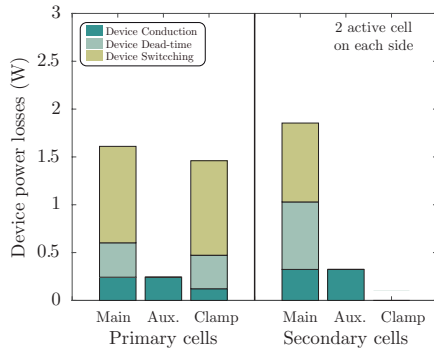
(b)

Figure 5.35: M2BF cell power losses distribution based on GaN devices (120 W): (a) connecting one cell on each side and (b) connecting two cells on each side.

a V_{GS} without exceeding maximum allowed voltage and without false turn-on [see Figure 5.37(a)].

The buck converter operates in hard-switching mode, with reduced current ripple, as it is depicted in Figure 5.37(b). Experimental measurements of power losses are presented in Figure 5.38, achieving a good agreement between theoretical and experimental measurements. Low switching losses are achieved, even operating in hard-switching mode. Moreover, although anti-series switch is implemented, the use of GaN devices results on low conduction losses. However, dead-time losses im-
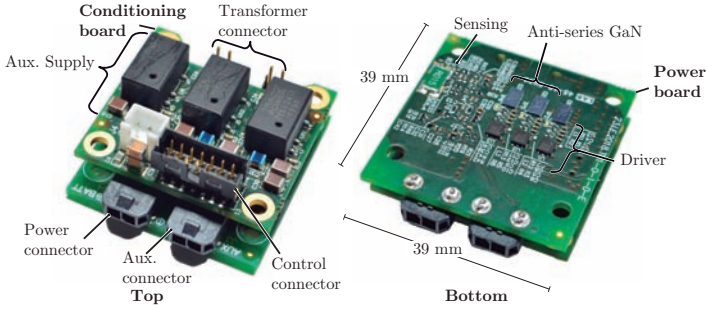
Figure 5.36: GaN-based M2BF power cell consisting of power and conditioning board.
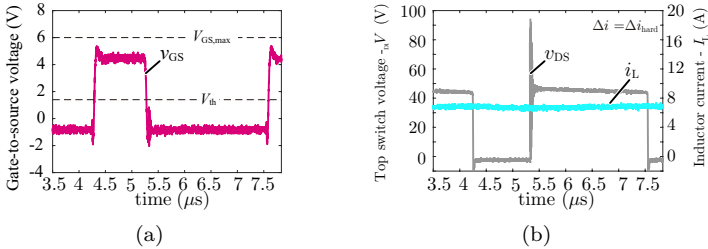
Figure 5.37: Experimental waveforms of LV GaN devices working at high-switching frequency in hard-switching mode (300 kHz/6 A: (a) gate-to-source voltage (V_{GS}) and (b) drain-to-source voltage and inductor current (I_{L}).

pact is higher, due to high-switching frequency. Therefore, it is crucial to reduce dead-time conduction instances. Once the performance of the power module has been evaluated working as buck converter, the performance working in M2BF configuration will be presented in future works [163].
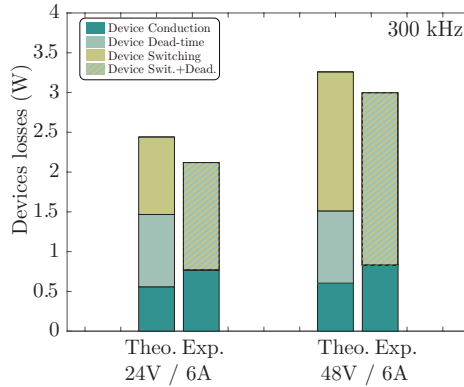
Figure 5.38: Experimental validation of LV GaN devices performance working at high-switching frequency in hard-switching mode (300 kHz/6 A).

5.6 Conclusions

Design optimization routine presented in Chapter 4 and power losses model of Section 3.4 are applied to different power converter topologies, in order to evaluate the application of GaN devices. Single-cell and multi-cell topologies are analyzed working at different operation modes.

Regarding single-cell, synchronous buck converter is evaluated, defining the most optimal design for medium power range (2.5 kW). The use of GaN devices for commonly used synchronous buck converter, results on ultra-efficient solutions operating in hard-switching (>99%). Besides, when power density is the most restrictive design aspect, GaN-based converters allow to reduce power converter size (>20 kW/l).

In addition, resonant operation of GaN devices is analyzed. Different operation regions of the resonant converter are evaluated. Capacitive region presents low power losses even operating at hard-switching. The impact of switching losses for such low current are not relevant for GaN devices at medium switching frequency (>70 kHz). Inductive zone present iZVS and ZVS zones. In these zones, GaN devices losses are reduced. However, it has to be noted, that dead-time losses need to be considered when operating at high switching frequencies (>120 kHz).

Referring to multi-cell converters, HV and LV applications are evaluated, on a MMC and on the novel M2BF. However, in the case of the MMC it is not a clear benefit of working with GaN devices at

high switching frequencies for low fundamental frequency. The increase of the switching frequency does not result on a reduction of the converter volume. Moreover, when working at lower switching frequencies it has been demonstrated that GaN achieves similar performance than Si. Nevertheless, when operating at higher fundamental frequency, such as for high-speed MVD, GaN devices will reduce the switching losses impact. On the contrary, M2BF appears as a suitable topology for GaN devices characteristics. The low conduction losses of GaN devices and the low impact of turn-off losses result on high efficiency even for high switching frequency (300 kHz).

Chapter 6

Conclusions

6.1 Conclusions and Contributions

Considering the novelty of GaN semiconductors and the challenges of implementing this technology on power electronics, the most suitable operation conditions of GaN-based power converters are presented in this thesis. The presented results are verified by simulations or/and experimental measurements for a variety of conditions.

For that purpose, the most differential characteristics of GaN devices have been defined, proposing different solutions for implementing GaN-based power converters. Gate driver circuit has been analyzed along with the dead-time control strategy and thermal limits. In the following step, this analysis has been applied to a GaN-based power converter, evaluating different operating conditions. Moreover, a general power losses model has been proposed, with a ZVS losses estimation. The analysis is experimentally validated, achieving a good agreement between experimental and theoretical results.

Once the performance of GaN devices has been evaluated, the impact of operating with GaN devices has been analyzed at power converter level. Indeed, design optimization routine has been presented, analyzing the impact of design variables, such as switching frequency or current ripple. The objective of this optimization has been to define the most efficient and compact solution. Thus, different cooling systems have been evaluated, along with capacitors and inductors. Then, this analysis is applied to various topologies, in order to analyze the

potentiality of GaN devices operating at different configurations.

The performance of GaN-based power converters has been evaluated for single-cell and multi-cell converters. On the one hand, single-cell non-isolated synchronous buck has been analyzed, obtaining high power density ($>20\,\text{kW/l}$), maintaining high efficiencies ($>98\%$). Moreover, isolated resonant converter has been also evaluated, achieving low power losses even operating in capacitive region, i.e. hard turn-on. On the other hand, high-voltage and low-voltage multi-cell systems are analyzed. For the high-voltage application a GaN-based MMC is analyzed, achieving a high efficiency over a wide output load. Regarding low-voltage multi-cell converter, a novel concept of mutli-port flyback has been proposed, i.e. M2BF. This topology presents high controllability, being possible to connect/disconnect cells depending on system requirements. Therefore, the high performance of GaN devices on this application range has been demonstrated.

The conclusions and contributions of this work are divided between main and other contributions.

MAIN CONTRIBUTIONS:

▶ **Comprehensive analysis of GaN semiconductors characteristics, that define the design considerations and challenges.**
Refer to publications: [a].

GaN semiconductors present lower overall conduction resistance even compared to Si Super-junction devices in the range of $600\,\text{V}$. Moreover, GaN has lower output capacitance along with lower gate charge requirement than its counterparts. These characteristics results on lower switching and driver losses.

However, special attention must be devoted when designing the gate driver to avoid false turn-on and exceeding the maximum allowable gate voltage. The gate driver is analyzed defining the gate resistances and voltages for a suitable operation of GaN devices. Considering the diode like gate behaviour of some GaN devices, current controlled gate driver design is also analyzed.

In addition, even if GaN devices have a negligible reverse recovery free-wheeling conduction, power losses generated in these conduction instances are higher than for Si or SiC MOSFETs. Therefore, dead-time conduction instances are analyzed, defining the minimum dead-time in order to reduce losses related to free-wheeling

conduction periods. Furthermore, an asymmetrical dead-time control is proposed reducing the high impact of dead-time losses.

▶ **Detailed analysis of hard- and soft-switching operation, including the losses of incomplete soft-switching transitions.**
Refer to publications: [a] and [f].

The performance of semiconductors is evaluated with a general analytical model that can be adapted to different topologies. In this case, the analysis is focused on a well-known synchronous buck converter. The great difference between turn-on and turn-off energies, along with low conduction resistance of GaN devices leads to low power losses, even for hard-switching operation mode. The effect of operating at different current ripples and switching frequencies has been evaluated for a 2.45 kW power converter with parallel-connected devices.

On the one hand, the increase of the current ripple, ensuring ZVS, reduces power losses of semiconductors for high-switching frequencies (>40 kHz). Nevertheless, the relevance of GaN devices switching losses is low when considering full converter performance. On the other hand, the use of parallel devices results on lower power losses up to high switching frequency <150 kHz.

▶ **Thermal limits improvement based on heat-spreading materials and parallelization of various devices.**
Refer to publications: [b],[g] and [h].

Thermal cooling limits are analyzed and the use of heat-spreading materials is proposed. The increase of thermal pad through high thermal conductivity heat-spreading materials results on the enhancement of cooling capability. Besides, paralleling GaN devices will be essential for medium/high power converters, in order to distribute power losses through larger dissipation area.

Furthermore, considering the thermal cooling limitation of small size GaN devices, three cooling configurations are analyzed, for two different packages and including heat-spreading materials. Only comparing the thermal performance of both packages, top side cooled device is better than bottom side cooled one. However, the use of bottom cooled configuration with Cu inlay, increasing

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the thermal pad, and better TIM material improves the cooling performance in comparison with the top cooled configuration. The use of parallel devices and heat-spreading materials overcome thermal cooling limitations of GaN devices. It is demonstrated that the use of heat-spreading material can increase cooling capability by 56%. Hence, the use of heat-spreading materials will be essential when designing GaN-based power converters to increase the dissipation capability of GaN semiconductors.

▶ **The potentiality of GaN devices is analyzed in detail for various applications. This analysis includes single-cell and multi-cell topologies, defining the enhancement and limitations of implementing them with GaN devices.**
Refer to publications: [c],[e], [i], [j] and [k].

Single-cell and multi-cell topologies are analyzed working at different operation modes. Regarding single-cell, a synchronous buck converter is evaluated, defining the most optimal design for medium power range (2.5 kW). It is demonstrated that the use of GaN devices for a commonly used synchronous buck converter, results on ultra-efficient solutions operating in hard-switching (>99%). Besides, when power density is the most restrictive design aspect, GaN-based converters allow reducing power converter size (>20 kW/l).

In addition, GaN devices performance is analyzed operating in resonant converters. Different operation regions of the resonant converter are evaluated. As the impact of switching losses for low current is not relevant for GaN devices at medium switching frequency (>70 kHz), low power losses are achieved even operating in the capacitive region, i.e. hard-switching turn-on. Otherwise, inductive zone presents soft-switching turn-on. In these modes, GaN devices losses are reduced. However, it has to be noted, that the impact of dead-time losses need to be considered when operating at high switching frequencies (>120 kHz).

Referring to multi-cell converters, HV and LV applications are evaluated, on a MMC and a M2BF. In the case of the MMC, there is not a clear benefit on working with GaN devices at high switching frequencies when operating with low fundamental frequency. The increase of the switching frequency does not result on a reduction of the converter volume, as a consequence of the

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high impact of the capacitor size of each sub-module. Nevertheless, when operating at higher fundamental frequency, such as for high-speed medium voltage drives, GaN devices will reduce the switching losses impact. On the contrary, M2BF appears as a suitable topology for GaN devices characteristics. M2BF provides high controllability of multiple inputs and outputs, being possible to adapt the number of connected cells to the requirements of the system. It has been demonstrated that the low conduction losses of GaN devices and the low impact of turn-off losses result on high efficiency even for high switching frequency (300 kHz), achieving a reduced size.

OTHER CONTRIBUTIONS:

▶ **Power losses model and experimental measurement method are proposed and validated.**

Considering the characteristics of semiconductors, power losses are estimated and thermally measured on an experimental prototype. A steady-state calorimetric measurement method is proposed for the experimental estimation of GaN switches power losses at power converter level.

▶ **Design optimization routine for analyzing different operation conditions in order to define the optimal converter design for GaN semiconductors.**

Approximation models of cooling systems, capacitors and inductors are presented. Then, the impact of operating conditions on the volume and losses of these components is evaluated, defining the most optimal solutions in terms of efficiency and power density.

▶ **New common-mode modulation techniques are evaluated for three-phase inverters with dc-link referenced to output filter.**
Refer to publications: [d].

List of Publications

Within this research project, several scientific contributions to the literature were published. These are listed below.

JOURNAL ARTICLES:

a **A. Avila**, A. Garcia-Bediaga, A. Rodriguez, L. Mir, A. Rujas, *Evaluation of Operation Conditions for the Design of GaN-based Power Converters*, submitted to IEEE Journal of Emerging and Selected Topics in Power Electronics, 2019.

b **A. Avila**, A. Garcia-Bediaga, A. Rodriguez, L. Mir, A. Rujas, *Evaluation of thermal management for GaN-based power converters*, submitted to IET Power Electronics, 2019.

c **A. Avila**, A. Garcia-Bediaga, U. Iruretagoyena, I. Villar, A. Rujas, *Comparative evaluation of front and back end PFC IPT systems for a contactless battery charger*, IEEE Transactions on Industry Applications, 2018. pp. 4842-4850.
DOI: 10.1109/TIA.2018.2839096

d M. Antivachis, D. Bortis, **A. Avila**, and J. W. Kolar *New optimal common-mode modulation for three-phase inverters with dc-link referenced output filter*, IEEE CPSS Transactions on Power Electronics and Applications, 2017, pp. 331-340.
DOI: 10.24295/CPSSTPEA.2017.00030

INTERNATIONAL CONFERENCE ARTICLES:

e **A. Avila**, A. García-Bediaga, A. Rodriguez, L. Mir, A. Rujas *Multi-cell Multi-port Bidirectional Flyback based on GaN devices*, in 11th Annual IEEE Energy Conversion Congress & Exposition (ECCE) Baltimore, 2019 (Accepted).

f **A. Avila**, A. García-Bediaga, A. Rodriguez, L. Mir, A. Rujas *Analysis of Optimal Operation Conditions for GaN-based Power Converters*, in 10th Annual IEEE Energy Conversion Congress & Exposition (ECCE), Portland, 2018.
DOI: 10.1109/ECCE.2018.8557476

g X. Jordà, X. Perpiñà, A. Garcia-Bediaga, **A. Avila**, M. Vellvehi *Analysis of natural convection cooling solutions for GaN HEMT transistors*, in 20th European Conference on Power Electronics and Applications, (EPE'18 ECCE Europe), Riga, 2018.

h **A. Avila**, A. Garcia-Bediaga, F. Gonzalez X. Jordà, X. Perpiñà, A. Rujas *Thermal performance analysis of GaN-based high-power converters*, in 20th European Conference on Power Electronics and Applications, (EPE'18 ECCE Europe), Riga, 2018.

i **A. Avila**, A. Garcia-Bediaga, U. Iruretagoyena, I. Villar, A. Rujas, *Comparative evaluation of front and back end PFC IPT systems for a contactless battery charger*, in: IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, 2017.
DOI: 10.1109/ECCE.2017.8095770

j **A. Avila**, A. Garcia-Bediaga, O. Onederra, A. Rodríguez, A. Rujas, *Comparative analysis of GaN HEMT vs. Si CoolMOS for a High-Frequency MMC Topology*, in: 19th European Conference on Power Electronics and Applications, (EPE'17 ECCE Europe), Warsaw, 2017.
DOI: 10.23919/EPE17ECCEEurope.2017.8099334

NATIONAL CONFERENCE ARTICLES:

k **A. Avila**, A. Garcia-Bediaga, A. Rodríguez, A. Rujas, H. Gaztanaga, *Análisis de las Ventajas de la Alta Frecuencia y el Nitruro de Galio (GaN) en un Convertidor Multinivel Modular*, in: Seminario Anual de Automática, Electrónica industrial e Instrumentación (SAAEI), Elche, 2016.

6.2 Future Work

During this thesis, the potential applications of GaN devices have been defined, modeling the performance of components that conform a power converter and validating these results experimentally. However, there are some issues and interesting research works to perform related to GaN devices and GaN-based power converters:

► *High-bandwidth instrumentation*: During this thesis, the measurement of current and voltages was a controversy when validating the performance of power converters. It would be interesting to analyze different measurement strategies, achieving high-accuracy with low distortion and high-bandwidth.

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▶ *High-speed protections*: Considering the high-switching capability of GaN devices, the use of high-speed protections will be interesting. Moreover, when opening the system in case of failure the high free-wheeling conduction losses need to be considered.

▶ *High-frequency magnetics*: In this work approximations and simplifications related to inductor design have been applied. However, with a more detailed analysis of the design of high-frequency magnetics lower converter overall volume will be achieved.

▶ *Megahertz operation range*: One of the most interesting work will be the evaluation of the accuracy of the presented model on MHz operation range. In this switching frequency range, the impact of dynamic on-resistance, dead-time losses and output capacitance losses plays a key role as addressed in [167].

▶ *Bidirectional switches*: The performance analysis and design issues of bidirectional GaN devices could be an interesting work for near future research works. As it has been previously mentioned, the lateral structure of GaN devices allows to develop bidirectional switches without an excessive increase of the conduction resistance. This characteristic will be interesting for different topologies, such as for Neutral-Point Clamped Converter (NPC) or the proposed M2BF.

Chapter 7

Conclusiones

7.1   Conclusiones y Contribuciones

Debido a la novedad de los semiconductores de GaN y los retos que supone implementar esta tecnología en la electrónica de potencia, en este trabajo se presentan cuáles son las condiciones óptimas en las que aprovechar al máximo las ventajas de estos dispositivos. Los resultados que se presentan han sido verificados mediante simulación y validados experimentalmente para diferentes condiciones de trabajo.

Para ello, las principales características de los dispositivos de GaN han sido subrayadas, proponiendo métodos de diseño. Se ha analizado el diseño del driver, junto con la elección del tiempo muerto y los límites térmicos. Este análisis se ha aplicado a un caso de estudio concreto en el que se han evaluado diferentes modos de operación. Además, se presenta un modelo de perdidas completo para estimar el rendimiento de los semiconductores incluso operando en ZVS. Este modelo se valida experimentalmente, obteniendo poca diferencia entre los resultados del modelo y los obtenidos experimentalmente.

Una vez se ha analizado el rendimiento de los dispositivos de GaN, se analiza el impacto de estos a nivel convertidor. Ciertamente, se ha propuesto una rutina de optimización para analizar cómo afectan los diferentes parámetros de diseño al rendimiento del convertidor. El objetivo de esta rutina es la de obtener la mejor solución en términos de densidad de potencia y eficiencia. Se analizan además diferentes sistemas de refrigeración, capacidades e inductores.

Por consiguiente, este análisis de aplica a diferentes topologías, definiendo la potencialidad del GaN para diferentes configuraciones. Se analiza el rendimiento de los convertidores basados en semiconductores de GaN considerando convertidores de una sola celda y multiceldas. Para los de una sola celda se obtiene alta densidad de potencia ($20\,\text{kW/l}$), manteniendo altas eficiencias, para un convertidor reductor. Además, se analiza el rendimiento de los dispositivos de GaN trabajando en resonancia, obteniendo reducidas pérdidas incluso operando en la zona capacitiva (encendido en conmutación dura). En cuanto las topologías multicelda, se analiza un MMC para aplicaciones de media/alta tensión ($>600\,\text{V}$), consiguiendo alta eficiencia incluso a baja potencia. Por otro lado, se analizan los beneficios de utilizar convertidores multicelda en aplicaciones de menos tensión. Para ello se propone la topología M2BF, que permite una alta controlabilidad. El rendimiento de esta topología basada en semiconductores de GaN resulta en reducidas pérdidas de conmutación, incluso trabajando a $300\,\text{kHz}$. Las contribuciones y conclusiones de este trabajo se dividen entre las contribuciones principales principales y otras contribuciones.

CONTRIBUCIONES PRINCIPALES:

▶ **Análisis exhaustivo de las características de los semiconductores de GaN, definiendo los retos de implementar esta tecnología.**
Ver publicación: [a].

Los semiconductores de GaN presentan una menor resistencia de conducción, incluso comparándolos con los semiconductores de Si en el rango de $600\,\text{V}$. Además, los GaN tienen menor capacidad parásita de salida junto con menos requerimientos de puerta que sus competidores, en el rango de $600\,\text{V}$. Estas características resultan en menos pérdidas de conducción, conmutación y de driver.

A la hora de diseñar el circuito del drive se ha de prestar especial atención en la tensión máxima permitida por puerta y evitar falsos encendidos. Se analiza el circuito de driver, definiendo una selección optima de resistencias de puerta y tensiones apropiadas para los dispositivos de GaN. Asimismo, se analizan tanto drivers controlados en tensión como en corriente.

Por otro lado, a pesar de que los semiconductores de GaN no tienen un diodo en antiparalelo en su estructura, permiten la conducción inversa en abierto con un recubrimiento inverso de-

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spreciable. Sin embargo, las pérdidas generadas por conducción inversa son relevantes. Por lo tanto, se analiza cómo reducir estas pérdidas reduciendo el tiempo muerto al mínimo y proponiendo un control del tiempo muerto asimétrico.

▶ **Análisis detallado de los modos de operación duro y suave, incluyendo las pérdidas de la conmutación dulce incompleta.**
Ver publicaciones: [a] y [f].

EL rendimiento de los semiconductores es evaluado a nivel convertidor con la propuesta de un modelo general que se puede adaptar a diferentes topologías. En este caso en particular, el análisis se valida en un convertidor reductor síncrono. La gran diferencia entre perdidas de encendido y de apagado junto con la baja resistencia de conducción de los dispositivos de GaN resulta en reducidas perdidas globales. Se analiza el efecto de trabajar con diferentes rizados y frecuencias de conmutación paralelando dispositivos en un convertidor de 2.45 kW.

Por un lado, el aumento del rizado, asegurando ZVS, reduce las pérdidas totales para frecuencias de conmutación superiores a los 40 kHz. Por otro lado, el uso de dispositivos en paralelo permite reducir las pérdidas hasta frecuencias inferiores a 150 kHz.

▶ **Mejora de los límites térmicos de los semiconductores de GaN usando materiales de alta conductividad térmica y el paralelado de varios dispositivos.**
Ver publicaciones: [b],[g] y [h].

Se analizan los límites térmicos y se propone el uso de materiales de alta conductividad térmica. El aumento del área de disipación de los dispositivos de GaN, mediante estos materiales permite una mejora considerable de la capacidad de disipación. Además, el uso de dispositivos en paralelo resulta esencial para convertidores de media/alta potencia, para poder distribuir las pérdidas sobre un área mayor.

Además, considerando las limitaciones del reducido tamaño de los dispositivos de GaN, se analizan tres métodos de disipación diferentes para dos empaquetados distintos. Solo comparando los empaquetados, el dispositivo que se refrigera por arriba presenta

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una solución mejor que la del dispositivo que se refrigera por debajo. Sin embargo, el uso de una configuración refrigerada por debajo que incorpora cobre en las capas interiores del PCB (Cu inlay), permite aumentar el área de disipación reduciendo el impacto del reducido tamaño de los dispositivos de GaN. Por otro lado, se demuestra que el uso de materiales de alta conductividad térmica para mejorar el sistema de refrigeración aumenta la capacidad térmica en un 56% para las soluciones analizadas. Por lo tanto, se demuestra que el uso de dispositivos en paralelo junto con materiales de alta conductividad térmica resulta indispensable para mejorar el diseño de convertidores basados en GaN.

▶ **La potencialidad del uso de dispositivos de GaN es analizada. Este análisis incluye topologías de una sola celda y múltasela, definiendo las mejoras que aportan los semiconductores de GaN.**
Ver publicaciones: [c],[e], [i], [j] y [k].

En cuanto a los convertidores de una celda, se aplica la rutina de diseño a un convertidor reductor convencional, para definir claramente los beneficios de implementarlo con semiconductores de GaN. Se demuestra que el uso del GaN permite trabajar a frecuencias más altas consiguiendo altas eficiencias (>99%). Además, cuando el requerimiento de diseño más restrictivo es el tamaño, el uso del GaN permite conseguir altas densidades de potencia (20 kW/l)

Por otro lado, se ha analizado el rendimiento de los semiconductores de GaN trabajando en un sistema resonante, evaluando diferentes zonas de operación. Como el impacto de las pérdidas de conmutación es reducido, trabajando en frecuencias de conmutación en torno a los 70 kHz se consiguen pérdidas bajas a pesar de trabajar en modo capacitivo, es decir conmutación dura. De lo contrario la zona inductiva presenta iZVS y ZVS. En estos modos de operación las pérdidas se reducen pero al trabajar a mayor frecuencia de conmutación (>120 kHz) las pérdidas del tiempo muerto cogen mayor impacto.

En cuanto a los sistemas multicelda, se analizan aplicaciones de alta (>600 V) y baja tensión (<200 V), en un MMC y el M2BF, respectivamente. Em el caso del MMC, no esta claro que los dispositivos de GaN aporten un gran beneficio. El trabajar a

alta frecuencia no supone un gran beneficio para el MMC, ya que si se trabaja con una frecuencia fundamental baja (50 Hz) el impacto del volumen de los condensadores de cada submódulo es el más relevante. En cambio, en aplicaciones que trabajan con una frecuencia fundamental alta, como los motores de alta velocidad, aumentar la frecuencia de conmutación si que sería interesante y los semiconductores de GaN reducirían el impacto de las pérdidas de conmutación.

Por otro lado, se propone el convertidor M2BF, con el que se consigue alta controlabilidad de múltiples entradas/salidas. Se demuestra que las reducidas pérdidas de conducción y conmutación de los dispositivos de GaN permiten una alta eficiencia incluso para aplicaciones multicelda de baja tensión trabajando a alta frecuencia de conmutación (>300 kHz). Además, el trabajar a alta frecuencia de conmutación con reducidas pérdidas resulta en un convertidor compacto.

OTRAS CONTRIBUCIONES:

► **Modelado de pérdidas y metodología de medida validada experimentalmente.** Considerando las características de los semiconductores, se estiman las pérdidas y se mide el salto de temperatura en el prototipo experimental. Se propone un método de medida de régimen permanente que mide la diferencia de temperatura entre el radiador y el ambiente.

► **Rutina de optimización analizando diferentes modos de operación, definiendo el convertidor optimo basado en dispositivos de GaN.**

Se utilizan modelos de aproximación para diferentes sistemas de refrigeración, capacidades e inductancias. Con estos modelos se analiza el impacto del volumen y las pérdidas de los diferentes componentes definiendo así la solución más eficiente y de mayor densidad de potencia.

► **Nueva técnica de modulación aplicada a inversores trifásicos con el dc-link referenciado al filtro de salida.**
Ver publication: [d].

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Lista de Publicaciones

Durante este proyecto de investigación, se han relizado contribuciones científicas a la literatura:

ARTÍCULOS DE REVISTA:

a **A. Avila**, A. Garcia-Bediaga, A. Rodriguez, L. Mir, A. Rujas, *Evaluation of Operation Conditions for the Design of GaN-based Power Converters*, submitted to IEEE Journal of Emerging and Selected Topics in Power Electronics, 2019.

b **A. Avila**, A. Garcia-Bediaga, A. Rodriguez, L. Mir, A. Rujas, *Evaluation of thermal management for GaN-based power converters*, submitted to IET Power Electronics, 2019.

c **A. Avila**, A. Garcia-Bediaga, U. Iruretagoyena, I. Villar, A. Rujas, *Comparative evaluation of front and back end PFC IPT systems for a contactless battery charger*, IEEE Transactions on Industry Applications, 2018. pp. 4842-4850.
DOI: 10.1109/TIA.2018.2839096

d M. Antivachis, D. Bortis, **A. Avila**, and J. W. Kolar *New optimal common-mode modulation for three-phase inverters with dc-link referenced output filter*, IEEE CPSS Transactions on Power Electronics and Applications, 2017, pp. 331-340.
DOI: 10.24295/CPSSTPEA.2017.00030

CONFERENCIAS INTERNACIONALES:

e **A. Avila**, A. García-Bediaga, A. Rodriguez, L. Mir, A. Rujas *Multi-cell Multi-port Bidirectional Flyback based on GaN devices*, in 11th Annual IEEE Energy Conversion Congress & Exposition (ECCE) Baltimore, 2019 (Accepted).

f **A. Avila**, A. García-Bediaga, A. Rodriguez, L. Mir, A. Rujas *Analysis of Optimal Operation Conditions for GaN-based Power Converters*, in 10th Annual IEEE Energy Conversion Congress & Exposition (ECCE), Portland, 2018.
DOI: 10.1109/ECCE.2018.8557476

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g X. Jordà, X. Perpiñà, A. Garcia-Bediaga, **A. Avila**, M. Vellvehi *Analysis of natural convection cooling solutions for GaN HEMT transistors*, in 20th European Conference on Power Electronics and Applications, (EPE'18 ECCE Europe), Riga, 2018.

h **A. Avila**, A. Garcia-Bediaga, F. Gonzalez X. Jordà, X. Perpiñà, A. Rujas *Thermal performance analysis of GaN-based high-power converters*, in 20th European Conference on Power Electronics and Applications, (EPE'18 ECCE Europe), Riga, 2018.

i **A. Avila**, A. Garcia-Bediaga, U. Iruretagoyena, I. Villar, A. Rujas, *Comparative evaluation of front and back end PFC IPT systems for a contactless battery charger*, in: IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, 2017. DOI: 10.1109/ECCE.2017.8095770

j **A. Avila**, A. Garcia-Bediaga, O. Onederra, A. Rodríguez, A. Rujas, *Comparative analysis of GaN HEMT vs. Si CoolMOS for a High-Frequency MMC Topology*, in: 19th European Conference on Power Electronics and Applications, (EPE'17 ECCE Europe), Warsaw, 2017. DOI: 10.23919/EPE17ECCEEurope.2017.8099334

CONFERENCIAS NACIONALES:

k **A. Avila**, A. Garcia-Bediaga, A. Rodríguez, A. Rujas, H. Gaztanaga, *Análisis de las Ventajas de la Alta Frecuencia y el Nitruro de Galio (GaN) en un Convertidor Multinivel Modular*, in: Seminario Anual de Automática, Electrónica industrial e Instrumentación (SAAEI), Elche, 2016.

7.2   Trabajo Futuro

Durante esta tesis, se han definido las aplicaciones potenciales de los semiconductores de GaN, mediante modelado del rendimeinto de los componentes que forman un convertidor de potencia, validando estos resultados experimentalmente. Sin embargo, existen ciertas areas de investigación interesantes a explorar relacionadas con los dispositivos de GaN y los convertidores basados en GaN

▶ *Intrumentación con alto ancho de banda.* La medida de tensión y corriente de los convertidores basados en GaN ha supuesto ciertos problemas, a la hora de validar el rendimeinto de los convertidores. Sería interesante analizar diferentes metodos de medida, consiguiendo alta precisión, con poca distosión y alto ancho de banda.

▶ *Proteciones de alta velocidad.* Considerando la capacidad de conmutación a alta velocidad de los dispostivos de GaN, resulta imprescindible el uso de protecciones de alta velocidad, en caso de necesitar protecciones. Además, a la hora de abrir el sistema en caso de fallo, se ha de analizar el impacto de la conducción por el "diodo" en antiparalelo.

▶ *Magnéticos de alta frecuencia.* En este trabajo se aplican aproximaciones y simplicaciones relacionadas con el diseño de inductancias. Sin embargo, se precisa de un análisis más detallado del diseño de magnéticos de alta frecuencia pudiendo conseguir redcuir el tamaño del convertidor.

▶ *Operación en el rango de megahercios.* Uno de los trabajos más interesantes a realizar seróa evaluar la precisión de los modelos presentados trabajando en el rango de megahercios. Para altas

frecuencias de trabajo, el impacto de la resistencia dinámica, el tiempo muerto y las pérdidas de la capacidad de salida aumenta [167].

► *Semiconductores bidirecionales.* El uso de dipostivos bidirecionales de GaN puede ser un punto de interes para futuras investigaciones. Cómo se ha mencionado en este documento, la estructura lateral de los dispostivos de GaN, permite desarrollar dispositivos de GaN bidirecionales con una resistencia de conducción reducida. Esta característica es interesante para el desarrollo de convertidores como el NPC o el M2BF propuesto en este trabajo.

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Appendix A

Approximation models

Approximation models are proposed based on updated commercial data, identifying the benefits of working with high performance GaN devices. The presented approximation models are suitable for general optimization routines, reducing long convergence times as it is proposed in [134] for medium frequency high-power converters.

Figure A.1 shows a general flow chart applied to approximation models. First the commercial database is loaded, differing between different technologies or types of devices. Then, the design space is defined according to the characteristics of the components, obtaining D_Λ number of design options. Once the design space is identified the mapping of entire solutions is performed obtaining the losses and volume of each possible configuration. Finally, approximation models of the most suitable Pareto selection is performed in terms of losses or/and volume. In Section 4.1.4 the Pareto selection procedure is explained in more detail.

This approximation procedure is applied to cooling solutions and capacitors, while inductors are obtained from scaling laws presented in the literature [168]. Although the presented models are based on simplifications, they are accurate enough to describe the performance at power converter level.

A.0.1   Cooling system

Cooling system sizing is dependent on power losses. In this case, losses of power switches are obtained from the model presented in Section 3.4 for a half-bridge configuration. Then, the required heatsink thermal
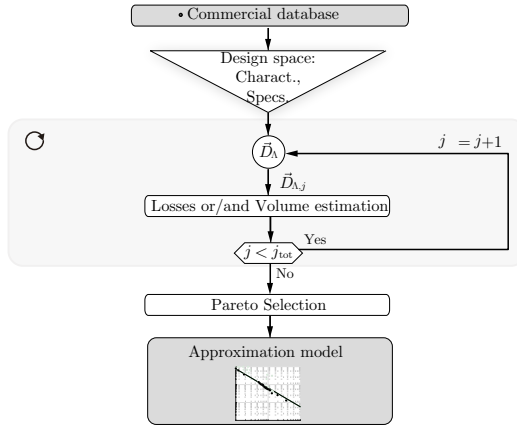
Figure A.1: Proposed general approximation model applied to commercial database of different components that conform a power converter.

resistance $R_{\mathrm{th,hs}}$ can be calculated as follows:

$$R_{\mathrm{th,hs}} = (T_{\mathrm{hs}} - T_{\mathrm{a}})/P_{\mathrm{d,T}}$$
$$\text{being} \quad T_{\mathrm{hs}} = T_{\mathrm{j,max}} - (R_{\mathrm{th_{j-c}}} + R_{\mathrm{th_{c-hs}}}) \cdot P_{\mathrm{d,1}} \tag{A.1}$$

where $P_{\mathrm{d,1}}$ is related to power losses across a single device, thermal network resistances are obtained with (2.34) and total power losses are calculated in Section 3.4.

Besides, total losses $P_{\mathrm{d,T}}$ are distributed between high-side and low-side switches for the half-bridge configuration. Thus, for the half-bridge configuration both devices losses need to be considered in order to obtain the maximum $P_{\mathrm{d,1}}$

$$P_{\mathrm{d,1}} = \max(P_{\mathrm{d,s1}}, P_{\mathrm{d,s2}}). \tag{A.2}$$

Thus, two limits are defined: the maximum losses related to a single device and total power losses. Then, the heatsink volume is approximated based on commercial database and $R_{\mathrm{th,hs}}$. A relation between the volume and required $R_{\mathrm{th,hs}}$ is obtained for different cooling technologies.

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Natural convection model

Database of natural convection heatsinks depicted in Figure A.2 is considered. The approximation model is obtained from the solutions with the lower volume and $R_{\text{th,hs}}$ relation. This work adapts the equation presented in [169] for cooling system volume estimation, which results in

$$\text{Vol}_{\text{hs,nat.}} = 0.728 \cdot R_{\text{th,hs}}^{-1.72} \quad [\text{dm}^3].\tag{A.3}$$
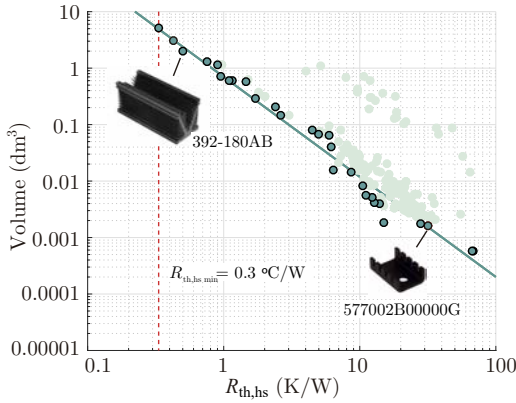
Figure A.2: Thermal resistance versus volume of commercially available natural convection cooling heatsinks, with a minimum achievable resistance $R_{\text{th,hs,min}}$=0.3℃/W .

A good correlation related to best heatsinks is achieved as it is shown in Figure A.2.

Forced-air model

As in the case of natural convection heatsinks, the volume is estimated with the approximation (A.4), based on the curve fitting applied to commercial database of forced-air cooling solutions.

$$\text{Vol}_{\text{hs,air}} = 0.055 \cdot R_{\text{th,hs}}^{-1.14} \quad [\text{dm}^3]\tag{A.4}$$

Figure A.3 shows that the correlation fits with commercial data even for different fan configurations: external fan (LA 9/200 24V) and integrated
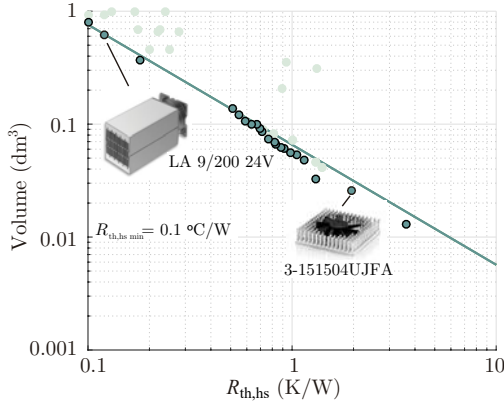
Figure A.3: Thermal resistance versus volume of commercially available forced-air cooling heatsinks, with a minimum achievable resistance $R_{\text{th,hs,min}}$=0.1℃/W .

fan (3-151504UFJA), among others. Integrated fan solutions, mainly used for consumer electronics, are presented as compact solution with relatevily low $R_{\text{th,hs}}$ for compact GaN-based solutions.

Liquid cooling model

In the case of liquid cooling heatsinks, equation (A.5) is obtained from database information to estimate their volume.

$$\text{Vol}_{\text{hs,liq.}} = 0.0894 \cdot R_{\text{th,hs}}^{-0.41} \quad [\text{dm}^3] \tag{A.5}$$

Commonly, for this configuration custom solutions are designed. Hence, in this case less commercial liquid cooling solutions are found, in comparison to other cooling configurations. However, good fitting is achieved, as it is depicted in Figure A.4.

Therefore, one of these commonly used cooling technologies is selected depending on the required $R_{\text{th,hs}}$, system complexity and volume constrain.

A.0.2 Capacitors

Capacitors are used in power converters with mainly two different objectives: dc-link or output filter, and resonant capacitors. The required
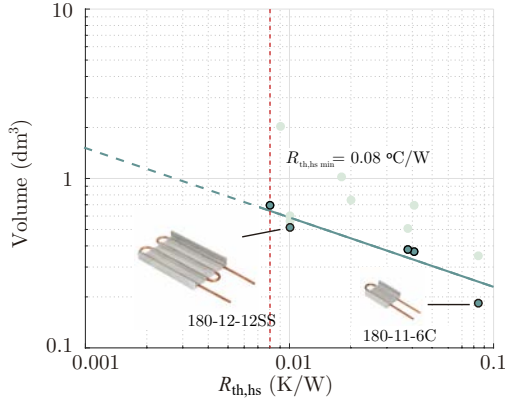
Figure A.4: Thermal resistance versus volume of commercially available liquid cooling heatsinks, with a minimum achievable resistance $R_{\mathrm{th,hs,min}}=0.08°C/W$.

capacitance for each variant is defined:

▶ *Dc-link or filter capacitors:* Power converters usually need dc-link and filter capacitors in order to regulate and maintain a constant voltage. Considering specifications of power converters, such as maximum allowed voltage variation or the attenuated frequency, the required capacitance can be defined. Solving the general capacitor current formula (A.6) the minimum capacitance is calculated with (A.7), which fulfills voltage ripple (Δv_{c}), expressed as per-unit.

$$i_{\mathrm{c}}(t) = C \cdot \frac{dv_{\mathrm{c}}}{dt} \tag{A.6}$$

$$C = \frac{\int i_{\mathrm{c}}(t)}{\Delta v_{\mathrm{c}} \cdot V_{\mathrm{c}}} \tag{A.7}$$

being $i_{\mathrm{c}}(t)$ the capacitor current which is related to the converter topology.

Then, the capacitance can be defined for the maximum allowable current on the capacitor I_{c} for a period $1/f$

$$C > \frac{I_{\mathrm{c}}}{\Delta v_{\mathrm{c}} \cdot V_{\mathrm{c}} \cdot f} \tag{A.8}$$

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▶ *Resonant capacitors:* In resonant converters capacitors are used to conform the resonance tank in order to reach soft-switching operation. Thus, the capacitance is defined by the resonance frequency f_r and resonant elements, e.g. $L - C$. Considering a series-resonant converter with an inductor L_r, the capacitance C_r is obtained with

$$C_r = \frac{1}{4 \cdot \pi^2 \cdot f_r^2 \cdot L_r}. \tag{A.9}$$

In addition, a second condition, related to the capacitor peak voltage (V_{C_r}) is defined in [134], as there are infinite combinations of L_r and C_r. The peak voltage is obtained developing the integral of a sinusoidal current from the general capacitor current expression (A.6).

$$V_{C_r} = \frac{I_{c,peak}}{\omega_r \cdot C_r}. \tag{A.10}$$

being $I_{c,peak}$ the peak current and ω_r its pulsation. High capacitance values are preferred in order to reduce the stress of magnetics components [142].

Technologies

Mainly three capacitor technologies are predominant in power electronics [170, 171]: aluminum electrolytic, film and ceramic. Table A.1 summarizes a comparison of these capacitor technologies, identifying the most relevant characteristics of each technology.

▶ *Aluminum electrolytic capacitors:* These capacitors present reduced cost and large capacitance per unit volume. However, the commercially available voltage rating of this technology is limited to lower than 650 V [170] and they present relatively high losses in comparison with other variants [170]. These features make then attractive for high-current and low frequency applications.

▶ *Film capacitors:* One of the most beneficial characteristic of this technology is the reduced internal resistance (ESR) and low parasitic inductances (ESL) but the energy density is much smaller than for electrolytic capacitors [171]. Hence, the losses related to film capacitors can be neglected but the volume has a great impact on the converter performance. Thus, film capacitors are suitable for applications with high surge currents, e.g. snubber,

or/and high-frequency applications, with an availability for any voltage range [170]. However, the internal structure of these devices can result on a great variation of the capacitance with the frequency [171].

► *Ceramic capacitors:* Ceramic capacitors feature high energy density and low losses but with high cost per stored energy. Moreover, they often present a reduction of the capacitance with respect to frequency and voltage, as occurs for film capacitors. Nevertheless, novel capacitors with low capacitance variation have been recently presented [172]. Then, ceramic capacitors are suitable for high-frequency applications and are also available in almost any voltage rating.

Table A.1: Comparison between aluminum electrolytic, film and ceramic capacitors

Characteristics	Aluminum	Film	Ceramic
Capacitance	**High**	Medium	Low
Ripple current	Medium	**High**	**High**
ESR	High $10x,15x$ ESR of Films	**Low** $<2\,\mathrm{m\Omega}$	Medium $2x$ ESR of Films
Frequency	Low	High	High
Energy/Volume	High $475.65\,\mathrm{J/dm^3}$	**Low** $0.68\,\mathrm{J/dm^3}$	Medium $2.52\,\mathrm{J/dm^3}$
Energy/Cost	**Low** $0.54\,\mathrm{J/€}$	High $13.68\,\mu\mathrm{J/€}$	Medium $0.29\,\mu\mathrm{J/€}$

Losses and Volume models

Considering characteristics presented in Table A.1, models of capacitors are defined for each technology. Power losses are obtained with (A.11) for the ESR characteristic of different technologies, neglecting these losses for ceramic capacitors, as a consequence of relativeily small ESR.

$$P_{\mathrm{Cap}} = \mathrm{ESR} \cdot I_{\mathrm{c,rms}} \tag{A.11}$$

where the ESR is obtained from the lower ESR of the analyzed data aluminum electrolytic capacitors, as it is depicted in Figure A.5.
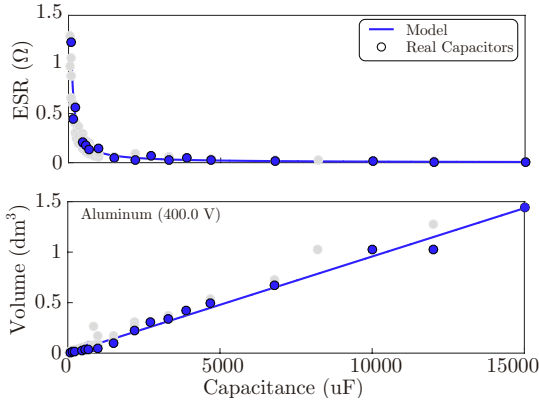
Figure A.5: Aluminum capacitor data of ESR and volume (gray) and considering best performance data (blue) for the model.

Regarding the capacitor volume, data of different capacitor technologies is evaluated considering the most optimal capacitors for the approximation model. Then, the volume of capacitors can be approximated as a function of the capacitor energy $(1/2 \cdot C \cdot V^2)$ with (A.12), which is obtained from data of real capacitors presented in Figure A.6.

$$\text{Vol}_{\text{Cap}} = \alpha_2 \cdot C^2 + \alpha_1 \cdot C + \beta_1 \cdot V + \gamma \cdot C \cdot V + \gamma_0 \qquad \text{(A.12)}$$

being α, β and γ the constants related to the voltage and capacitance. This approximation serves as scaling approximation when higher energy is required.

A.0.3 Inductors

Besides power losses of semiconductors and its impact on thermal management, the inductive components are the main cause for losses in converters. Regarding inductors, they are mainly employed to limit the current ripple $(\Delta i \cdot I_{\text{L}})$ and for resonant circuits. Moreover, inductors storage energy (A.13) between different operation modes.

$$E = \frac{1}{2} \cdot L \cdot I^2 \qquad \text{(A.13)}$$
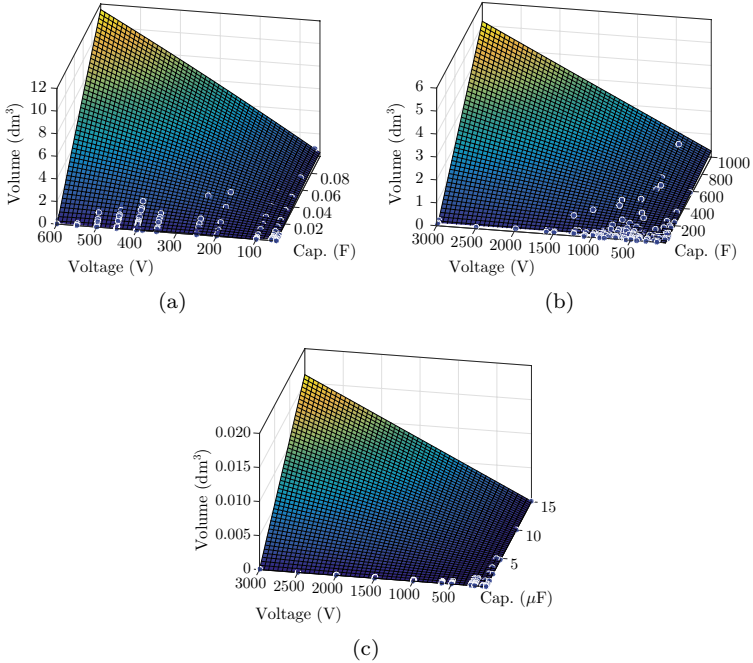
Figure A.6: Capacitor volume approximation constant for various capacitor technologies: (a) aluminum, (b) film and (c) ceramic.

Therefore, considering the general equation of an inductor voltage ($v_{\mathrm{L}} = L \cdot \mathrm{d}i/\mathrm{d}t$), the inductance L can be defined for an inductor voltage V_{L}, a Δi, a switching frequency f_{s} and a current I

$$L > \frac{V_{\mathrm{L}}}{\Delta i \cdot I_{\mathrm{L}} \cdot f_{\mathrm{s}}} \tag{A.14}$$

In addition, the resonant inductance L_{r} is obtained for the resonance frequency f_{r}, considering and LC resonance tank (A.9).

An inductor is typically constructed with a core where wires are bounded, as it is depicted in Figure A.7. Different core and winding technologies are described briefly in order to define the most suitable configuration for GaN-based power converters.

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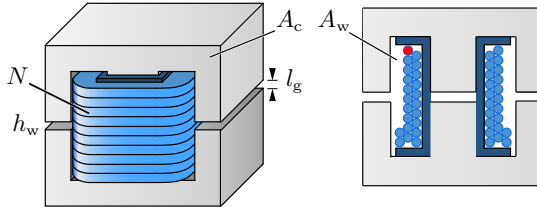
Figure A.7: Example of inductor geometry for an E-type core.

Core

Soft magnetic materials are widely used in power electronics, such as ferrite, iron powder and amorphous or noncrystalline soft magnetic alloys [168]. Amorphous and nanocrystalline alloys present the higher saturation flux density, along with relatively low hysteresis losses in the case of nanoncrystalline. However, amorphous alloys present high hysteresis losses. Besides, the availability in terms of shapes and sizes of these cores is very limited in comparison with ferrite or iron powder. Ferrite shows low flux density with low losses while iron powder presents high flux density with high losses.

Regarding ferrite cores, different materials are preferred depending on the switching frequency [173]. In this case, the core for operating at switching frequency from 10 kHz to 1 MHz is selected, i.e. N87 core [173].

Winding

The most commonly used winding materials for power inductors are solid cooper, litz wire and foil windings. The selection of winding technology can be determinant regarding high-frequency losses but it is outside the scope of this thesis. Then, a low processing time approximation model is used for the estimation of losses and volume impact, based on high frequency litz wires.

Losses and Volume model

In the literature inductor design has been widely discussed defining models with high complexity [15]. However, simplified models based on scaling laws proposed in [168,174] have been adapted during this work for a first approximation of inductor characteristics.

Inductor volume (Vol_L) can be approximated considering the area product AP, which is related to the core geometry: window winding area A_w and core cross-sectional area A_c [168] (see Figure A.7).

$$AP = A_\text{c} \cdot A_\text{w}$$
$$\text{where} \quad AP = \left(\frac{L \cdot I_\text{rms} \cdot I_\text{pk}}{B_\text{max} \cdot K_t \cdot \sqrt{k_\text{u} \cdot \Delta T}} \right)^{8/7} \tag{A.15}$$

where B_max is the maximum flux density in the inductor core; K_t is $48.2{\cdot}10^3$, based on typical values of different core types and sizes [168]; k_u is the winding factor (0.6-0.8) and ΔT is chosen as 60℃.

Then, Vol_L is obtained from (A.15) and k_L inductor volume constant, which is derived from the inductor geometry [168].

$$\text{Vol}_\text{L} = AP^{\frac{3}{4}} \cdot k_\text{L} \tag{A.16}$$

being k_L related to the core geometry [168]. Moreover, other inductor design parameters such as the core volume V_c and inductor surface area A_t can be obtained from AP approximations presented in [168].

Considering the calculated AP, the core with the higher AP value closest to the calculated with (A.15) is selected from manufacturer database [173]. After selection of the core, the required air-gap l_g in the magnetic flux path is obtained considering the energy stored at the inductor E_L (A.13):

$$l_\text{g} = \frac{E_\text{L} \cdot \mu_0}{B_\text{max}^2 \cdot A_\text{c}} \tag{A.17}$$

where the reluctance of the magnetic path is calculated, assuming that the permeability of the core is much higher than vacuum:

$$R = \frac{l_\text{g}}{A_\text{c} \cdot \mu_0} \tag{A.18}$$

Then, inductor losses are estimated, obtaining core and winding losses for the required number of turns ($N = \sqrt{L \cdot R}$). On the one hand,

the improved General Steinmetz Equation (iGSE) is used in order to calculate core losses per unit of volume (W/m^3)(A.19)

$$P_{\text{core}} = k_{\text{i}} \cdot |\Delta B|^{\beta} \cdot f_{\text{s}}^{\alpha} \cdot \left[\delta^{1-\alpha} + (1-\delta)^{1-\alpha}\right] \tag{A.19}$$

where δ the duty cycle, ΔB is the peak-to-peak flux density (A.20) for a voltage V_{i}, α, β are Steinmetz parameters and k_{i} is approximated as it is presented in [168].

$$\Delta B = \frac{V_{\text{i}} \cdot \delta}{f_{\text{s}} \cdot N \cdot A_{\text{c}}} \tag{A.20}$$

Analyzing P_{core} losses, tendencies can be deduced, based on Steinmetz parameters for fixed V_{i}, A_{c} and δ:

$$P_{\text{core}} \approx |\Delta B|^{\beta} \cdot f_{\text{s}}^{\alpha} \approx N^{-\beta} \cdot f_{\text{s}}^{\alpha-\beta} \tag{A.21}$$

where the core losses are reduced while switching frequency increases for $\alpha < \beta$. Moreover, core losses reduce with N number of turns.

On the other hand, winding losses are estimated with (A.22), for a high-frequency litz wire.

$$P_{\text{wd}} = I_{\text{rms}}^2 \cdot \frac{4 \cdot \rho_{\text{w}} \cdot l_{\text{w}}}{\pi \cdot d_{\text{w}}^2 \cdot n_{\text{p}}} \tag{A.22}$$

being l_{w} winding length related to core geometry, d_{w} diameter, n_{p} number of wires in parallel, and ρ_{w} the resistivity of the conductor at the operation temperature [168].

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Bibliography

[1] B. K. Bose, "Global Warming: Energy, Environmental Pollution, and the Impact of Power Electronics," *IEEE Industrial Electronics Magazine*, vol. 4, no. 1, pp. 6–17, Jan. 2010.

[2] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Muhlethaler, T. Nussbaumer, and J. Minibock, "Extreme efficiency power electronics," in *Conference on Integrated Power Electronics Systems (CIPS)*, 2012.

[3] N. Kaminski, "State of the Art and the Future of Wide Band-Gap Devices," in *IEEE European Conference on Power Electronics and Applications (EPE)*, 2009.

[4] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[5] T. P. Chow, "Wide Bandgap Semiconductor Power Devices for Energy Efficient Systems," in *IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015.

[6] A. Krings, A. Boglietti, A. Cavagnino, and S. Sprague, "Soft Magnetic Material Status and Trends in Electric Machines," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 2405–2414, 2017.

[7] DataBank, "Renewable energy consumption (% of total final energy consumption)," 2015. [Online]. Available: https://data.worldbank.org/indicator/eg.fec.rnew.zs?end=2015{&}start=1990{&}view=chart

[8] I. E. Agency, "Global EV Outlook 2016." [Online]. Available: https://www.iea.org/publications/freepublications/publication/Global_EV_Outlook_2016.pdf

[9] A. M. Andwari, A. Pesiridis, S. Rajoo, R. Martinez-Botas, and V. Esfahanian, "A review of Battery Electric Vehicle technology and readiness levels ," *Renewable and Sustainable Energy Reviews*, vol. 78, pp. 414–430, 2017.

[10] S. Manzetti and F. Mariasiu, "Electric vehicle battery technologies: From present state to future systems," *Renewable and Sustainable Energy Reviews*, vol. 51, pp. 1004–1012, 2015.

[11] J. Choi, D. Tsukiyama, Y. Tsuruda, and J. Rivas, "13 . 56 MHz 1 . 3 kW Resonant Converter with GaN FET for Wireless Power Transfer," in *Wireless Power Transfer Conference (WPTC)*, 2015.

[12] B. Burger and D. Kranzer, "Extreme high efficiency PV-power converters," *IEEE European Conference on Power Electronics (EPE)*, 2009.

[13] X. Dan Gumera, A. Caberos, and S. Huang, "Design and Implementation of a High Efficiency Cost Effective EV Charger Using LLC Resonant Converter," in *Asian Conference on Energy, Power and Transportation Electrification (ACEPT)*, 2017.

[14] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner, "Performance trends and limitations of power electronic systems," in *International Conference on Integrated Power Electronics Systems*, 2010.

[15] R. Burkart, "Advanced Modeling and Multi-Objective Optimization of Power Electronic Converter Systems," Ph.D. dissertation, ETH, Zurich, 2016.

[16] C. E. Mullett, "A 5-year power technology roadmap," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2004.

[17] Jong-Pil Lee, Byung-Duk Min, Dong-Wook Yoo, Tae-Jin Kim, and Ji-Yoon Yoo, "A new topology for PV DC/DC converter with high efficiency under wide load range," in *IEEE European Conference on Power Electronics (EPE)*, 2007.

[18] J. A. Anderson, E. J. Hanak, L. Schrittwieser, M. Guacci, J. W. Kolar, and G. Deboy, "All-silicon 99.35% efficient three-phase seven-level hybrid neutral point clamped/flying capacitor inverter," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 1, pp. 50–61, Jan. 2019.

[19] H. Lin, "Market and Technology Trends in WBG Materials for Power Electronics Applications," in *CS MANTECH*, 2015.

[20] P. Gueguen, "Market & Technology trends in Wide BandGap power packaging," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015.

[21] G. Deboy, M. Treu, O. Haeberlen, and D. Neumayr, "Si, SiC and GaN power devices: An unbiased view on key performance indicators," in *IEEE International Electron Devices Meeting (IEDM)*, 2016.

[22] K. Shirabe, M. Swamy, J. Kang, M. Hisatsune, M. Das, R. Callanan, and H. Lin, "Design of 400V class inverter drive using SiC 6-in-1 power module," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2013.

[23] R. Togashi, Y. Inoue, S. Morimoto, and M. Sanada, "Performance improvement of ultra-high-speed PMSM drive system based on DTC by using SiC inverter," in *International Power Electronics Conference (IPEC)*, 2014.

[24] S. Haghbin, "Design considerations of a 50 kW compact fast charger stations using nanocrystalline magnetic materials and SiC modules," in *Ecological Vehicles and Renewable Energies (EVER)*, 2016.

[25] A. Rujas, V. M. López, A. García-Bediaga, A. Berasategi, and T. Nieva, "Influence of SiC technology in a railway traction DC-DC converter design evolution," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017.

[26] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99% Efficient 10 kV SiC-Based 7 kV/400 V DC Transformer for Future Data Centers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 753–767, 2019.

[27] E. A. Jones, F. Wang, and B. Ozpineci, "Application-based review of GaN HFETs," in *IEEE Workshop on Wide Bandgap Power Devices and Applications (WIPDA)*, 2014.

[28] S. Chowdhury, B. L. Swenson, and U. K. Mishra, "Enhancement and Depletion Mode AlGaN/GaN CAVET With Mg-Ion-Implanted GaN as Current Blocking Layer," *IEEE Electron Device Letters*, vol. 29, no. 6, pp. 543–545, Jun. 2008.

[29] T. Kachi, M. Kanechika, and T. Uesugi, "Automotive Applications of GaN Power Devices," in *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2011.

[30] Y. Wu and K. Smith, "Progress of GaN Transistors for Automotive Applications," 2015.

[31] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707–719, Sep. 2016.

[32] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, "A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 6, pp. 1764–1783, Jun. 2012.

[33] M. W. Lee, Y. S. Lee, and Y. H. Jeong, "A high-efficiency GaN HEMT hybrid class-E power amplifier for 3.5 GHz WiMAX applications," in *European Microwave Conference (EuMC)*, 2008.

[34] IP, "IP2010 - High Frequency GaN-Based Integrated Power Stage," 2010. [Online]. Available: http://www.irf.com/product-info/datasheets/data/ip2010pbf.pdf

[35] EPC, "EPC2010 Enhancement Mode Power Transistor – Preliminary Datasheet," 2010. [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2010_datasheet.pdf

[36] Infineon, "Infineon Technologies AG successfully acquires International Rectifier - Infineon Technologies." [Online]. Available: http://www.infineon.com/cms/en/about-infineon/press/press-releases/2015/INFXX201501-020.html

[37] ——, "Infineon and Panasonic Will Establish Dual Sourcing for Normally-Off 600V GaN Power Devices." [Online]. Available: http://www.infineon.com/cms/en/about-infineon/press/press-releases/2015/INFPMM201503-041.html

[38] Furukawa, "Licensing agreement reached with Transphorm, Inc. : FURUKAWA ELECTRIC CO., LTD." [Online]. Available: https://www.furukawa.co.jp/english/what/2014/kei_140514.htm

[39] Semiconductor Today, "Power GaN device IP dynamics heralds future ramp-up of market," 2015. [Online]. Available: http://www.semiconductor-today.com/news_items/2015/oct/yole_211015.shtml

[40] KnowMade, "GaN Devices for Power Electronics Patent Investigation," 2016. [Online]. Available: http://www.knowmade.com/downloads/gan-devices-for-power-electronics-patent-investigation/

[41] "HiPoSwitch GaN-based normally-off high power switching transistor for efficient power converters," 2015. [Online]. Available: http://www.hiposwitch.eu/

[42] "PowerBase-Enhanced substrates and GaN pilot lines enabling compact power applications," 2015. [Online]. Available: http://www.powerbase-project.eu/

[43] UltimateGaN, "UltimateGaN - Research for GaN technologies, devices and applications to address the challenges of the future GaN roadmap." [Online]. Available: http://www.ultimategan.eu/

[44] D. Reusch and J. Strydom, "Understanding the effect of PCB layout on circuit performance in a high-frequency gallium-nitride-based point of load converter," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 2008–2015, Apr. 2014.

[45] Transphorm, "Designing Hard-switched Bridges with GaN," 2014. [Online]. Available: http://www.transphormusa.com/wp-content/uploads/2016/02/AN-0004_0.pdf

[46] G. Systems, "App. Note - How to Drive GaN Enhancement Mode Power Switching Transistors," 2014. [Online]. Available: https://www.mouser.com/catalog/additional/GaNSystems_GN001AppNote2014-10-21.pdf

207

[47] J. S. Glaser and D. Reusch, "Comparison of deadtime effects on the performance of DC-DC converters with GaN FETs and silicon MOSFETs," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016. [Online]. Available: http://ieeexplore.ieee.org/document/7854939/

[48] N. Badawi, O. Hilt, E. Behat-treidel, J. Böcker, J. Würfl, and S. Dieckerhoff, "Investigation of the Dynamic On-State Resistance of 600V Normally-off and Normally-on GaN HEMTs," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015.

[49] T. Cappello, A. Santarelli, and C. Florian, "Dynamic RON Characterization Technique for the Evaluation of Thermal and Off-State Voltage Stress of GaN Switches," *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 3386–3398, Apr. 2018.

[50] Infineon, "Reliability and qualification of CoolGaN™ Technology and devices," 2018. [Online]. Available: https://www.infineon.com/dgdl/Infineon-2_WhitePaper_Reliability_and_qualification_of_CoolGaN_EN-WP-v01_00-EN.pdf?fileId=5546d46266a498f50166c9bebef322aa

[51] W. Kangping, M. Huan, L. Hongchang, G. Yixuan, Y. Xu, Z. Xiangjun, and Y. Xiaoling, "An Optimized Layout with Low Parasitic Inductances for GaN HEMTs Based DC-DC Converter," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015.

[52] F. Luo, Z. Chen, L. Xue, P. Mattavelli, D. Boroyevich, and B. Hughes, "Design considerations for GaN HEMT multichip halfbridge module for high-frequency power converters," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2014.

[53] D. Reusch, J. Strydom, and A. Lidow, "Thermal Evaluation of Chip-Scale Packaged Gallium Nitride Transistors," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 738–746, Mar. 2016.

[54] A. Avila, A. Garcia-Bediaga, F. Gonzalez, X. Jorda, X. Perpina, and A. Rujas, "Thermal Performance Analysis of GaN-Based High-Power Converters," in *IEEE European Conference on Power Electronics and Applications (EPE)*, 2018.

[55] L. Xue, Z. Shen, M. Mu, D. Boroyevich, R. Burgos, B. Hughes, and P. Mattavelli, "Bi-directional PHEV battery charger based on normally-off GaN-on-Si multi-chip module," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2014.

[56] B. Sun, R. Burgos, D. Boroyevich, S. Bala, and J. Xu, "10 kW High Efficiency Compact GaN-Based DC/DC Converter Design," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018.

[57] Eric Persson, "Professional Education Seminar S17 GaN HEMTs in Power Electronics," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015.

[58] F. Guo, L. Fu, H. Li, and M. Alsolami, "A Dual-Input Full-Bridge Current-Source Isolated DC / DC Converter Based on Quasi-Switched- Capacitor Circuit for Photovoltaic Systems with Energy Storage," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015.

[59] O. Bomboir, P. Bleus, F. Milstein, T. Joannès, P. Stassain, and C. Geuzaine, "Red Electrical Devils by CE+T Technical Approach Document," 2015. [Online]. Available: https://www.littleboxchallenge.com/pdf/finalists/56568-Tech.pdf

[60] J. W. Kolar, "Approaches to Overcome the Google/IEEE Little-Box Challenges," in *Keynote Presentation at the International Telecommunications Energy Conference (INTELEC)*, 2015.

[61] Y. Wu, "Paralleling high-speed GaN power HEMTs for quadrupled power output," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013.

[62] R. Ramachandran and M. Nymand, "Experimental Demonstration of a 98.8% Efficient Isolated DC-DC GaN Converter," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9104 – 9113, 2016.

[63] Z. Wang, Y. Wu, J. Honea, and L. Zhou, "Paralleling GaN HEMTs for Diode-free Bridge Power Converters," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015.

209

[64] J. S. Lai, C.-y. Lin, Y.-c. Liu, L. Zhang, and X. Zhao, "Design Optimization for Ultrahigh Efficiency Buck Regulator using Wide Bandgap Devices," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015.

[65] D. Derix, R. Freiche, C. Schöner, and A. Hensel, "Comparison of continuous and transition mode in a PV-booster with GaN-transistors and switching frequencies up to 250 kHz Keywords," in *IEEE European Conference on Power Electronics and Applications (EPE)*, 2015.

[66] H. Li, X. Zhang, and Z. Zhang, "Design of a 10 kW GaN-Based High Power Density Three-Phase Inverter," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016.

[67] J. W. Kolar, D. Neumayr, and D. Bortis, "The Google Little Box Challenge - Ultra-Compact GaN- or SiC-Based Single-Phase DC/AC Power Conversion." Warsaw, 2017: Tutorial at the 19th European Conference on Power Electronics and Applications (EPE - ECCE Europe).

[68] CE+T Power, "Little Box Challenge by CE+T Power." [Online]. Available: http://littleboxchallengecetpower.com/{#}effy

[69] A. Taylor, J. Lu, L. Zhu, K. . Bai, M. McAmmond, and A. Brown, "Comparison of SiC MOSFET-based and GaN HEMT-based high-efficiency high-power-density 7.2kW EV battery chargers," *IET Power Electronics*, vol. 11, no. 11, pp. 1849–1857, Nov. 2018.

[70] A. Cai, A. Pereira, Y. K. Tan, and L. Siek, "A High Frequency , High Efficiency GaN HFET Based Inductive Power Transfer System," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015.

[71] S. Wall, X. Hong, L. Sha, and J. Xie, "High-efficiency PV inverter with SiC technology," *IET Renewable Power Generation*, vol. 12, no. 2, pp. 149–156, Feb. 2018.

[72] "Market Analysis of Wideband Gap Devices in Car Power Electronics - IEEE Transportation Electrification Community Web Portal," 2015. [Online]. Available: https://tec.ieee.org/newsletter/november-december-2014/market-analysis-of-wideband-gap-devices-in-car-power-electronics

[73] PowerPulse, "GaN Enables 1600W Titanium Power Supply for Gamers," 2018. [Online]. Available: http://powerpulse.net/gan-enables-1600w-titanium-power-supply-for-gamers/

[74] ——, "GaN Power ICs Deliver 45W Travel Adapter in 14mm Profile," 2018. [Online]. Available: http://powerpulse.net/gan-power-ics-deliver-45w-travel-adapter-in-14mm-profile/

[75] Solar Power Europe, "Global Market Outlook - For Solar Power 2018-2020," Tech. Rep. [Online]. Available: http://www.solarpowereurope.org/wp-content/uploads/2018/09/Global-Market-Outlook-2018-2022.pdf

[76] C. Sintamarean, E. Eni, F. Blaabjerg, R. Teodorescu, and H. Wang, "Wide-band gap devices in PV systems - opportunities and challenges," in *International Power Electronics Conference (IPEC)*, 2014.

[77] F. Guo, L. Fu, H. Li, M. Alsolami, X. Zhang, J. Wang, and J. Zhang, "A full-bridge current-source isolated DC/DC converter with reduced number of switches and voltage stresses for photovoltaic applications," in *IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2014.

[78] S. Srdic and Z. Despotovic, "A Buck-Boost Converter Modified to Utilize 600V GaN Power Devices in a PV Application Requiring 1200V Devices," *Advances in Electrical and Computer Engineering*, vol. 15, no. 3, pp. 59–64, Mar. 2015.

[79] A. Hensel, C. Wilhelm, and D. Kranzer, "Application of a new 600 V GaN transistor in power electronics for PV systems," 2012.

[80] E. Gurpinar and A. Castellazzi, "SiC and GaN Based BSNPC Inverter for Photovoltaic Systems Keywords Bi-directional Switched Neutral Point Clamped Inverter," in *IEEE European Conference on Power Electronics (EPE)*, 2015.

[81] C. Sintamarean, F. Blaabjerg, and H. Wang, "Comprehensive evaluation on efficiency and thermal loading of associated Si and SiC based PV inverter applications," in *IEEE Industrial Electronics Society (IECON)*, Nov. 2013.

211

[82] "Mitsubishi Shows 'World's 1st' SiC-based PV Inverter," 2014. [Online]. Available: https://tech.nikkeibp.co.jp/dm/english/NEWS_EN/20140731/368247/?ST=msbe

[83] "Solar inverters get smaller, more efficient thanks to exotic semiconductors." [Online]. Available: http://www.solarpowerworldonline.com/2015/07/solar_inverters_get_smaller_more_efficient_thanks_to_exotic_semiconductors/

[84] Y. Zhou, L. Liu, and H. Li, "A High-Performance Photovoltaic Module-Integrated Converter (MIC) Based on Cascaded Quasi-Z-Source Inverters (qZSI) Using eGaN FETs," *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2727–2738, Jun. 2013.

[85] M. Kasper, M. Ritz, D. Bortis, and J. W. Kolar, "PV Panel-Integrated High Step-Up High Efficiency Isolated GaN DC-DC Boost Converter," in *IEEE International Telecommunications Energy Conference (INTELEC)*, 2013.

[86] L. Garcia-Rodriguez, V. Jones, J. C. Balda, E. Lindstrom, A. Oliva, and J. Gonzalez-Llorente, "Design of a GaN-based microinverter for photovoltaic systems," in *International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2014.

[87] G. Patterson, "The Automotive Market Opportunity for GaN," in *Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM)*, 2015.

[88] K. Itoh, S. Inoue, M. Ishigaki, T. Sugiyama, M. Sugai, and A. Port, "Loss Estimation of an Isolated Three-port DC-DC Converter for Automotive Applications," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015.

[89] T. Kikkawa, T. Hosoda, K. Imanishi, and E. al., "600 V JEDEC-qualified highly reliable GaN HEMTs on Si substrates," in *International Electron Devices Meeting*, 2014.

[90] D. Americas, "Delta Awarded DOE Grant to Develop a High-efficiency Compact GaN-based On-board Charger for Plug-in Electric Vehicles." [Online]. Available: http://www.delta-americas.com/news/pressDetail.aspx?secID=3{&}pID=1{&}typeID=2{&}itemID=5168{&}tid=0{&}hl=en-US

[91] M. Su, C. Chen, L. Chen, M. Esposto, and S. Rajan, "Challenges in the automotive application of GaN power switching devices," in *Compound Semiconductor Manufacturing Technology (CS MAN-TECH)*, 2012.

[92] T. Kachi, "Recent progress of GaN power devices for automotive applications Recent progress of GaN power devices for automotive applications," *Japanese Journal of Applied Physics*, vol. 53, pp. 100–210, Sept. 2014.

[93] T. Kachi and T. Uesugi, "Evaluation of GaN Substrate for Vertical GaN Power Device Applications," *Sensors and Materials*, vol. 25, no. 3, pp. 219–227, Jan. 2013.

[94] T. Kachi, D. Kikuta, and T. Uesugi, "GaN power device and reliability for automotive applications," in *International Reliability Physics Symposium (IRPS)*, 2012.

[95] K. Peng, S. Eskandari, and E. Santi, "Characterization and Modeling of a Gallium Nitride Power HEMT," *IEEE Transactions on Industry Applications*, vol. 52, no. 6, pp. 4965–4975, Nov. 2016.

[96] N. Korada, Z. Yu, and R. Ayyanar, "Loss Characterization and Analysis of High Voltage E-mode GaN HEMT in Soft-switching Application," in *IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2018.

[97] European Passive Components Institute, "SiC and GaN Created Buzz at APEC, but there was Plenty of Capacitor News, Too," 2016. [Online]. Available: https://passive_components.eu/sic_and_gan_created_buzz_at_apec_but_there_was_plenty_of_capacitor_news_too/

[98] I. Electronics360, "EPC Claims GaN Power Win Over Silicon."

[99] M. Asif Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson, "High electron mobility transistor based on a GaN-AlGaN heterojunction," *Applied Physics Letters*, vol. 63, no. 9, p. 1214, Jun. 1993.

[100] Panasonic, "600V GaN power transistor," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013. [Online]. Available: http://www.semicon.panasonic.co.jp/en/news/contents/2013/apec/panel/APEC2013_GaN_FPD_WEB.pdf

[101] Rongming Chu, A. Corrion, M. Chen, Ray Li, D. Wong, D. Zehnder, B. Hughes, and K. Boutros, "1200-V Normally Off GaN-on-Si Field-Effect Transistors With Low Dynamic on -Resistance," *IEEE Electron Device Letters*, vol. 32, no. 5, pp. 632–634, May 2011.

[102] Transphorm, "900V GaN (Galium Nitride) FET TP90H180PS - Transphorm." [Online]. Available: https://www.transphormusa.com/en/product/tp90h180ps-2/

[103] T. LaBella, B. York, C. Hutchens, and J.-S. Lai, "Dead time optimization through loss analysis of an active-clamp flyback converter utilizing GaN devices," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012.

[104] A. Hariya, K. Matsuura, H. Yanagi, S. Tomioka, Y. Ishizuka, and T. Ninomiya, "High frequency PWM-controlled current-mode resonant DC-DC converter with boost conversion," in *IEEE European Conference on Power Electronics and Applications (EPE)*, 2013.

[105] L. L. Jenkins, J. M. Aggas, B. K. Rhea, W. E. Abell, C. G. Wilson, and R. N. Dean, "Design and implementation of planar inductors for low voltage GaN-based power converters," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015.

[106] Infineon, "650V CoolMOS™ C7 PowerTransistor IPZ65R065C7 - Datasheet," Tech. Rep. [Online]. Available: https://www.infineon.com/dgdl/Infineon-IPZ65R065C7-DS-v02_01-en.pdf?fileId=db3a304341e0aed001420440a1011443

[107] Rohm, "SCT3060AL N-channel SiC power MOSFET - Datasheet," Tech. Rep. [Online]. Available: https://www.rohm.com/datasheet/SCT3060AL

[108] Infineon, "IGO60R070D1 - 600V CoolGaN™ enhancement-mode Power Transistor," 2018. [Online]. Available: https://www.infineon.com/dgdl/Infineon-IGO60R070D1-DS-v02_01-EN.pdf?fileId=5546d46265f064ff016685f053216514

[109] E. A. Jones, F. Wang, D. Costinett, Z. Zhang, B. Guo, B. Liu, and R. Ren, "Characterization of an Enhancement-Mode 650-V GaN

HFET," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015.

[110] M. Kasper, R. Burkat, F. Deboy, and J. Kolar, "ZVS of Power MOSFETs Revisited," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, Dic.. 2016.

[111] M. Danilovic, Z. Chen, R. Wang, F. Luo, D. Boroyevich, and P. Mattavelli, "Evaluation of the switching characteristics of a gallium-nitride transistor," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2011.

[112] R. Xie, H. Wang, G. Tang, X. Yang, and K. J. Chen, "An analytical model for false turn-on evaluation of GaN transistor in bridge-leg configuration," *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016.

[113] D. Han and B. Sarlioglu, "Deadtime Effect on GaN-Based Synchronous Boost Converter and Analytical Model for Optimal Deadtime Selection," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 601–612, Jan. 2016.

[114] M. Rodríguez, A. Rodríguez, P. F. Miaja, D. G. Lamar, and J. S. Zúniga, "An insight into the switching process of power MOSFETs: An improved analytical losses model," *IEEE Transactions on Power Electronics*, vol. 25, no. 6, pp. 1626–1640, Jun. 2010.

[115] O. Kreutzer, B. Eckardt, and M. Maerz, "Optimum gate driver design to reach SiC-MOSFET's full potential — Speeding up to 200 kV/μs," in *IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015.

[116] R. Khanna, A. Amrhein, W. Stanchina, G. Reed, and Z.-H. Mao, "An analytical model for evaluating the influence of device parasitics on Cdv/dt induced false turn-on in SiC MOSFETs," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013.

[117] Bernhard Zojer, "Infineon App. note - Driving 600 V CoolGaN™ high electron mobility transistors," 2018. [Online]. Available: https://www.infineon.com/dgdl/Infineon-ApplicationNote%7B_%7DCoolGaN%7B_%7D600V%7B_%7Demode%7B_

%7DHEMTs%7B_%7D-Driving%7B_%7DCoolGaN%
7B_%7Dhigh%7B_%7Delectron%7B_%7Dmobility%7B_
%7Dtransistors%7B_%7Dwith%7B_%7DEiceDRIVER%7B_
%7D%201EDI%7B_%7DCompact-AN-v01%

[118] S. Lee, S. Song, V. Au, and K. P. Moran, "Constriction/spreading resistance model for electronics packaging," in *Thermal Engineering Conference (ASME/JSME)*, 1995.

[119] C. Gammeter, "Multi-Objective Optimization of Power Electronics and Generators of Airborne Wind Turbines," Ph.D. dissertation, ETH, Zurich, 2017.

[120] A. Avila, A. Garcia-Bediaga, A. Rodriguez, L. Mir, and A. Rujas, "Analysis of Optimal Operation Conditions for GaN-based Power Converters," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018.

[121] GaN Systems, "GS66516T Top-side cooled 650 V E-mode GaN transistor," GaN Systems, Tech. Rep., 2016. [Online]. Available: https://gansystems.com/wp-content/uploads/2018/04/GS66516T-DS-Rev-180422.pdf

[122] GaNSystems, "GS66516T Top-side cooled 650 V E-mode GaN transistor," 2015. [Online]. Available: http://www.gansystems.com/datasheets/GS66516TDSRev160318.pdf

[123] J. L. Lu and D. Chen, "Paralleling GaN E-HEMTs in 10kW–100kW systems," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2017, pp. 3049–3056.

[124] M. De Rooij, "White Paper: Paralleling eGan FETs," 2012. [Online]. Available: http://www.digikey.com.mx/WebExport/SupplierContent/EfficientPowerConversion_917/PDF/epc-wp-wp005.pdf

[125] I. Rectifier, "Application Note: AN-941 PARALLELING POWER MOSFETs." [Online]. Available: http://www.irf.com/technical-info/appnotes/an-941.pdf

[126] S. Zhang, E. Laboure, D. Labrousse, and S. Lefebvre, "Thermal management for GaN power devices mounted on PCB substrates," in *International Workshop On Integrated Power Packaging (IWIPP)*, 2017.

[127] W. Burr, N. Pearne, and F. Stern, "Printed circuit board technologies for thermal management," *Circuit World*, vol. 39, no. 1, pp. 9–12, Feb. 2013.

[128] Y. Zhang and P. E. Bagnoli, "A modeling methodology for thermal analysis of the PCB structure," *Microelectronics Journal*, vol. 45, no. 8, pp. 1033–1052, 2014.

[129] X. Jorda and X. Perpina and M. Vellvehi and D. Sanchez and A. Garcia and A. Avila, "Analysis of Natural Convection Cooling Solutions for GaN HEMT Transistors," in *IEEE European Conference on Power Electronics (EPE)*, 2018.

[130] K. Wang, X. Yang, H. Li, H. Ma, X. Zeng, and W. Chen, "An Analytical Switching Process Model of Low-Voltage eGaN HEMTs for Loss Calculation," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 635–647, Jan. 2016.

[131] D. Rothmund, D. Bortis, and J. W. Kolar, "Accurate transient calorimetric measurement of soft-switching losses of 10kV SiC MOSFETs," in *International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2016.

[132] J. A. Anderson, C. Gammeter, L. Schrittwieser, and J. W. Kolar, "Accurate Calorimetric Switching Loss Measurement for 900 V 10 mOhm SiC mosfets," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 8963–8968, Dic. 2017.

[133] X. Fang, H. Hu, F. Chen, U. Somani, E. Auadisian, J. Shen, and I. Batarseh, "Efficiency-Oriented Optimal Design of the LLC Resonant Converter Based on Peak Gain Placement," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2285–2296, May 2013.

[134] A. Garcia-Bediaga, "Optimal Design of Medium Frequency High Power Converters," Ph.D. dissertation, Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, 2014.

[135] M. Mogorovic and D. Dujic, "Medium frequency transformer design and optimization," in *Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM)*, 2017.

217

[136] E. Gurpinar and A. Castellazzi, "Tradeoff Study of Heat Sink and Output Filter Volume in a GaN HEMT Based Single-Phase Inverter," *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5226–5239, Jun. 2018.

[137] U. Iruretagoyena Alustiza, "Design and Optimization of a Three Phase Inductive Power Transfer System," Ph.D. dissertation, Universidad del Pais Vasco (UPV/EHU), Donostia, 2018.

[138] A. Avila, A. Garcia-Bediaga, U. Iruretagoyena, I. Villar, and A. Rujas, "Comparative Evaluation of Front- and Back-End PFC IPT Systems for a Contactless Battery Charger," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 4842–4850, Sep. 2018.

[139] ——, "Comparative evaluation of front and back end PFC IPT systems for a contactless battery charger," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017.

[140] A. Avila, A. Garcia-Bediaga, O. Onederra, A. Rujas, and A. Rodriguez, "Comparative analysis of GaN HEMT vs. Si CoolMOS for a high-frequency MMC topology," in *IEEE European Conference on Power Electronics and Applications (EPE)*, 2017.

[141] D. Dujic, F. Kieferndorf, F. Canales, and U. Drofenik, "Power electronic traction transformer technology," in *International Power Electronics and Motion Control Conference*, 2012.

[142] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, Intergovernmental Panel on Climate Change, Ed. Springer US, 2001.

[143] Y. Hayashi, H. Toyoda, T. Ise, and A. Matsumoto, "Contactless DC Connector Based on GaN LLC Converter for Next-Generation Data Centers," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3244–3253, Apr. 2015.

[144] S. Inoue and H. Akagi, "A Bidirectional Isolated DC–DC Converter as a Core Circuit of the Next-Generation Medium-Voltage Power Conversion System," *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 535–542, Mar. 2007.

[145] M. Steiner and H. Reinold, "Medium frequency topology in railway applications," in *IEEE European Conference on Power Electronics and Applications (EPE))*, 2007.

[146] H. R. Mamede, W. M. dos Santos, R. F. Coelho, and D. C. Martins, "A multicell Dual-Active Bridge converter for increasing the reliability of power supply in a DC microgrid," in *IEEE First International Conference on DC Microgrids (ICDCM)*, 2015.

[147] J. Dorn, H. Gambach, J. Strauss, T. Westerweller, and J. Alligan, "Trans Bay Cable – A Breakthrough of VSC Multilevel Converters in HVDC Transmission," in *CIGRE San Francisco Colloq.*, 2012. [Online]. Available: http://scholar.google.com/scholar?hl=en{&}btnG=Search{&}q=intitle:Trans+Bay+Cable+?+A+Breakthrough+of+VSC+Multilevel+Converters+in+HVDC+Transmission{#}0

[148] M. a. Perez, D. Arancibia, S. Kouro, and J. Rodriguez, "Modular Multilevel Converter with Integrated Storage for Solar Photovoltaic Applications," in *Industrial Electronics Society (IECON)*, 2013.

[149] A. Lesnicar and R. Marquardt, "An Innovative Modular Multilevel Converter Topology Suitable for a Wide Power Range," in *PowerTech Conference*, 2003.

[150] D. Boroyevich, I. Cvetkovic, D. Dong, R. Burgos, F. Wang, and F. Lee, "Future electronic power distribution systems a contemplative view," in *International Conference on Optimization of Electrical and Electronic Equipment*, 2010.

[151] Jian Cao and A. Emadi, "A New Battery/UltraCapacitor Hybrid Energy Storage System for Electric, Hybrid, and Plug-In Hybrid Electric Vehicles," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 122–132, Jan. 2012.

[152] M. Guacci, D. Bortis, and J. W. Kolar, "High-Efficiency Weight-Optimized Fault-Tolerant Modular Multi-Cell Three-Phase GaN Inverter for Next Generation Aerospace Applications," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018.

219

[153] M. Antivachis, M. Kasper, D. Bortis, and J. W. Kolar, "Analysis of capacitive power transfer GaN ISOP multi-cell DC/DC converter systems for single-phase telecom power supply modules," in *IEEE Industrial Electronics Society IECON*, 2016.

[154] A. Stillwell and R. C. N. Pilawa-Podgurski, "A Five-Level Flying Capacitor Multilevel Converter With Integrated Auxiliary Power Supply and Start-Up," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2900–2913, Mar. 2019.

[155] D. Maksimovic, "Design of the zero-voltage-switching quasi-square-wave resonant switch," in *Power Electronics Specialist Conference - (PESC)*, 1993.

[156] C.-S. Wang, O. Stielau, and G. Covic, "Design Considerations for a Contactless Electric Vehicle Battery Charger," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 5, pp. 1308–1314, 2005.

[157] I. Villar, U. Iruretagoyena, A. Rujas, A. Garcia-Bediaga, and I. P. de Arenaza, "Design and implementation of a SiC based contactless battery charger for electric vehicles," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015.

[158] R. Bosshard and J. W. Kolar, "Inductive power transfer for electric vehicle charging: Technical challenges and tradeoffs," *IEEE Power Electronics Magazine*, vol. 3, no. 3, pp. 22–30, Sep. 2016.

[159] U. Iruretagoyena, A. Garcia-Bediaga, L. Mir, H. Camblong, and I. Villar, "Bifurcation phenomenon limits for three phase IPT systems with constant coupling coefficient," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017.

[160] M. a. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4–17, Jan. 2015. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6757004

[161] EPC, "EPC2034 – Enhancement Mode Power Transistor," 2019. [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2034_datasheet.pdf

[162] X. Huang, J. Feng, W. Du, F. C. Lee, and Q. Li, "Design consideration of MHz active clamp flyback converter with GaN devices for low power adapter application," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016.

[163] A. Avila, A. Garcia-Bediaga, A. Rodriguez, L. Mir, and A. Rujas, "Multi-cell Multi-port Bidirectional Flyback based on GaN devices," in *(Digest Accepted) IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019.

[164] T. Morita, M. Yanagihara, H. Ishida, M. Hikita, K. Kaibara, H. Matsuo, Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, "650 V 3.1 mOhmcm2GaN-based monolithic bidirectional switch using normally-off gate injection transistor," in *IEEE International Electron Devices Meeting*, 2007.

[165] C. Kuring, O. Hilt, J. Bocker, M. Wolf, S. Dieckerhoff, and J. Wurfl, "Novel monolithically integrated bidirectional GaN HEMT," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018.

[166] T. Mizuno, T. Inoue, K. Iwasawa, and H. Koizumi, "A voltage equalizer using flyback converter with active clamp," in *Asia Pacific Conference on Circuits and Systems*, 2012.

[167] M. Guacci, M. Heller, D. Neumayr, D. Bortis, J. W. Kolar, G. Deboy, C. Ostermaier, and O. Häberlen, "On the Origin of the Coss Losses in Soft-Switching GaN-on-Si Power HEMTs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 679–694, 2019.

[168] W. G. Hurley and W. H. Wölfle, *Transformers and Inductors for Power Electronics.* John Wiley & Sons, Ltd, 2013.

[169] Y. Louvrier, "Étude et optimisation d'un convertisseur dc/dc à canaux multiples entrelaces," Ph.D. dissertation, Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, 2010.

[170] KEMET, "Electronic Components Capacitor Selection Guide." [Online]. Available: http://www.kemet.com/Lists/FileStore/ Capacitor

[171] TDK, "Capacitors Selection Guide | Tech Notes | Capacitors | TDK Product Center." [Online]. Available: https://product.tdk.com/info/en/products/capacitor/technote/selection-guide.html

[172] KEMET, "KEMET KC-LINK™ for Fast Switching Semiconductor Applications DC Link, Snubber, Resonator Capacitor, 150°C." [Online]. Available: http://www.kemet.com/Lists/ProductCatalog/Attachments/744/KEM_C1039_KC-LINK_C0G.pdf

[173] TDK, "Ferrite Materials - Ferrites and Accessories (EPCOS)," 2017. [Online]. Available: https://www.tdk-electronics.tdk.com/en/529404/products/product-catalog/ferrites-and-accessories/epcos-ferrites-and-accessories/ferrite-materials

[174] J. Biela and J. W. Kolar, "Pareto-optimal design and performance mapping of telecom rectifier concepts," in *Power Conversion and Intelligent Motion Conference, Shanghai, China*, 2010.