Self-Powering High Frequency Modulated SiC Power MOSFET Isolated Gate Driver

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***Abstract*—A novel implementation of an isolated gate driver for power switches is proposed in this work. The driver is bespoke designed for SiC power MOSFETs. The proposal achieves the main driver characteristics - isolation capability, gate switching command and power transfer to the secondary side- by using a unique magnetic transformer. The resulting simple circuitry enables the integration of the driver into the power cell, achieving theoretical higher power density values of the final system. The principle of operation of the driver is described in detail. The original PWM signal is modulated with a pure AC square waveform under a two-level modulation scheme, that guarantees no saturation of the magnetic core. The signal is then magnetically coupled to the secondary side, where it is rectified and reconstructed to effectively drive the target device. In addition, the steps needed to provide a suitable design taking into account the parameters of the target power switch are also detailed. The resulting driver is characterized and a prototype of the driver is built and tested. The main results of the driver performance on a SiC MOSFET based prototype are presented. Based on the analysis of these results, this work demonstrates experimentally the feasibility of the proposal.**

***Index Terms*—Gate Driver, SiC MOSFET, Wide Band Gap devices**

I. Introduction

RECENT developments on wide-bandgap (WBG) power transistors make these devices the preferred option for an increasing number of applications. These devices withstand higher operating temperatures than standard solutions, allowing for the implementation of specific heat removal techniques that enable the miniaturization of the full system [1], [2]. In addition, WBG transistors present higher operating voltage and switching frequency ratings than the silicon-based counterparts, thus increasing the design and applicability limitations of power electronic converters. Still, these developments put forward specific challenges in the system, such as optimization of the reactive components for higher frequency and temperature operation, development of protecting circuitry, packaging, and so on [1], [3]–[5]. A major issue among these challenges is the design of the driver required for a proper command of the power device. There is a need for reliable, high power density, high frequency (HF), isolated gate drivers for full-range PWM duty ratio operation of the power devices [1], [3], [4], [6]–[8].

Some authors focus on specific drivers that address the main drawbacks of switching silicon-carbide (SiC) MOSFETs due to their specific characteristics. Active gate drivers vary the gate resistance of the driver, and are one of the most promising techniques for WBG drivers [9]. [10], [11] explore dynamic gate resistance modulation techniques to keep the SiC-device within its safe operating limits while maintaining a low switching loss with minimum voltage and current overshoots. The work in [12] proposes the variation of the drive voltage to decrease the effect of large dV/dt and dI/dt that imply overshoots, oscillations and EMI problems. The use of integrated drivers on SiC MOSFETS to decrease the effect of parasitic inductances in the gating path is explored in [13]. The effect of dead times in the general performance of the driver-power switch device is also assessed in [14]. [15] discusses the requirements of gate drivers for gallium nitride (GaN) WBG devices.

About the structure of isolated drivers, the most general solution is to use an optocoupler device to transfer the command pulses, together with a dedicated isolated DC-DC converter to supply the power device side of the driver [16]–[19]. This solution generally implies relatively large PCB footprint areas, thus penalizing the power density of the final solution. In addition, the relatively large parasitic elements of both the DC-DC converter and the optocoupler imply low dV/dt immunity and large harmful circulating currents, which in the long term also results in reliability concerns [16], [17], [20]. However, there is a significant research in this kind of structure to cope with these limitations [21]–[23]. Some other solutions based on pulse transformers ensure a saturation-free operation only for narrow duty ratio ranges, preventing the use in general applications [20], [24], [25]. In order to extend the duty ratio range,

a series capacitor might be included, to account for the DC component of the PWM signal; however, this limits the bandwidth of the driver, as fast changes in the duty ratio will imply large transients due to the large capacitance value of the blocking capacitor. The transient waveforms at the secondary side of the transformer when implementing such blocking capacitor, largely depend on a manifold of parameters in the design, some of them parasitic components that present a high-sensibility to design and implementation parameters. In fact, the design is generally carried out as a trade-off between the LF saturation avoidance feature and HF dynamic constraints in the driver. Other solutions based on symmetrical on-off pulses that avoid saturation [26]–[29] will not allow for a full duty ratio range, nor for a continuous on-off operation.

Several implementations of HF modulated gate drivers have been reported in the literature [30]–[33]. These proposals use high frequencies from hundreds of kHz up to tens of MHz for modulating the switching signal. In the case of targeting several MHz as modulating frequency, the solutions employ resonant techniques to generate the transformer waveforms. This results in complex control schemes to ensure resonant operation regardless of variations in the parameters of the circuit elements, due to various aspects such as temperature dependence, ageing, manufacturing tolerances, etc. Special care must be taken to cope with synchronization issues between the modulating and modulated waveforms in the PWM transitions. Indeed, this might lead to harmful glitches at the reconstructed waveform in the power device gate. These glitches might provoke, in extreme cases, undesired turn-on/off of the power device. Also, the turn-on/off dV/dt is limited to the slew rate of the resonant waveforms, that might not be enough depending on the application and device technology.

To cope with this limitation in dV/dt, square waveforms can be used as modulating signals; however, the frequency of these waveforms is limited to hundreds of kHz to few MHz, due to the losses caused by the hard switching at the oscillator stage. Moreover, the synchronization effect is even worse than in the resonant case. These solutions make use of a series-blocking capacitor to solve the saturation issue; however it results again in bandwidth limitations in the duty ratio command, as previously explained. In all cases, the power transfer is limited when operating at low duty ratio conditions, therefore constraining the operation range of the driver. To overcome these issues, this work proposes a new isolated gate driver for SiC Power MOSFETs, based on a dual level HF Amplitude Modulation (AM) scheme, applied to a single magnetic transformer. This single device provides simultaneously the triggering turn-on and off signals for the target device, but also the amount of power required to effectively drive the gate at the secondary side. A preliminary version of this proposal was introduced in [34], parting from a previous idea developed in [35]. The present work describes more in detail the characteristics and operating principles of the proposed drivers, shows the operating waveforms after a re-design to solve initial issues shown in [34], shows the full dimming range operation through experimental results, and validates the design through experimental results.

The paper is organized as follows. Section II describes the operating principle of the driver, shows the different functional blocks of the device, and describes the theoretical waveforms expected. After that, Section III discusses some design aspects, including a preliminary verification of the operation assessed through simulations. Later, Section IV presents the built prototypes of the driver, and shows the characteristic waveforms that validate the proposed operating principle. Section V shows the performance of two drivers implemented on the power switches of a built converter, and finally Section VI discusses the main conclusions of the research and proposes future developments.

II. Description of the Proposed Driver

Asymmetric turn-on and off voltage values are commonly used for driving such devices [1], [3], [7], [36], to ensure adequate turn on and off sates of the power devices.

For these WBG devices, high switching frequencies, of 100 kHz and above, can be considered without a significant increase in the corresponding switching losses. However, in practical converter designs, other aspects such as fulfillment of EMI regulations or implementation of reactive elements at such frequencies become a major issue, therefore limiting the design parameters [37], [38]. For this work, the target switching frequency for the SiC MOSFETs is selected to be 100 kHz. However, as it will be described in detail, the principle of operation is valid also for higher switching frequencies. As an example, a switching frequency of 200 kHz operation will also be explored. The modulation frequency for gate signal and power transfer is selected to be 1 MHz. It will be shown how the selection of such a low modulation index is not a problem for the conceived modulation strategy. Also, it will be shown how the system is able to provide full range duty ratio 0%-100%.

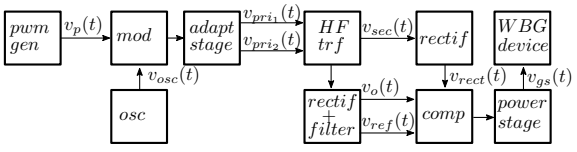


Fig. 1: System block diagram.

Fig. 1 shows a block diagram of the proposed circuit. The original pulse waveform, $v_p(t)$, ranges from 0 V to the high value at the digital controller, in this case 3.3 V. This signal is modulated with a square wave HF signal $v_{osc}(t)$, coming from an analog oscillator. As both the modulating and the oscillator waveforms are square waves, also the output of the modulator will be a square waveform, regardless of the duty ratio of the gating signal. In order to achieve a suitable waveform for the transformer (i.e. no DC component to avoid saturation), two different modulated waveforms in a complementary scheme with a 180 degree phase shift, are generated. Each of these waveforms, $v_{pri_1}(t)$ and $v_{pri_2}(t)$, depicted in Fig. 2 is applied to one of the terminals at the primary side of the transformer. Given the 180° phase shift of both signals, the effective voltage supplied to the primary side of the transformer, $v_{pri}(t)$, is a symmetrical bipolar voltage, and therefore it inherently avoids core saturation. Fig. 3 shows a detailed block diagram of this complementary modulator scheme.

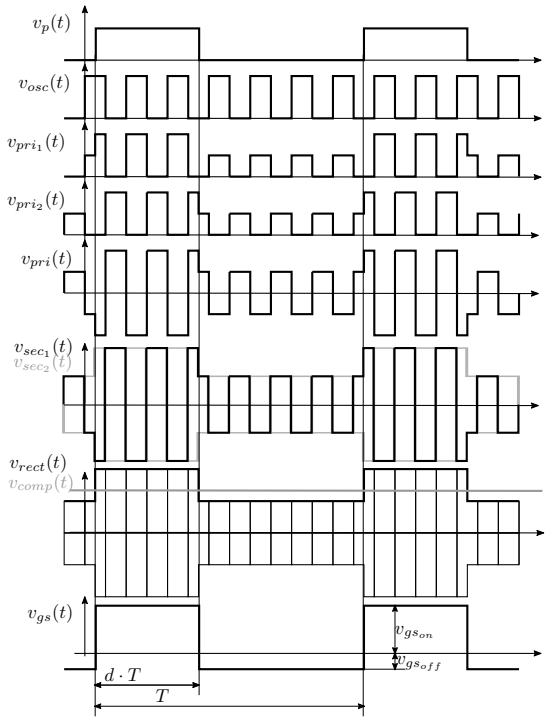


Fig. 2: Main theoretical waveforms at the driver. $v_p(t)$: Initial PWM signal. $v_{osc}(t)$: HF oscillator square waveform. $v_{pri_1}(t)$ and $v_{pri_2}(t)$: complementary modulated waveforms. $v_{pri}(t)$: Effective modulated waveform. $v_{rect}(t)$: Rectified waveform (black filled line). $v_{gs}(t)$: Gate-to-Source voltage.

Therefore, the resulting $v_{pri}(t)$ signal is a pure AC signal for any duty ratio value in the original PWM waveform. It must be noticed how the resolution of the duty ratio in the driver is limited by the digital controller only, independently of the modulation index used in the driver. As it can be seen in Fig. 2, signal $v_{pri}(t)$ has the envelope of the original pulsed signal, $v_p(t)$, no matter at which time instant the change of modulation amplitudes takes place. Thus, provided that the signal keeps the characteristic voltage fast variations between the limit values, the original PWM signal can be easily reconstructed by means of a simple diode rectifier.

The effective way to transfer the signal to the target device is to connect the v_{pri}(t) signal to the primary side of the transformer Tr. Again, this waveform can be understood as a HF modulated signal, with two different amplitude levels, one for turn-on and the other for turn-off intervals. On one side, this signal has no DC component, and therefore core saturation is avoided at any case of operation. But in addition, there will always be an input waveform at the transformer, even for 0% duty ratio, what allows for effective power transfer at every duty ratio, and thus sustained 0% duty ratio operation can be applied to the WBG device.

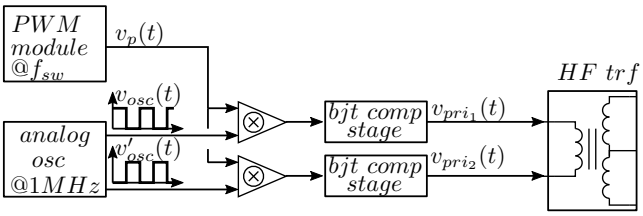


Fig. 3: Complementary modulator scheme at the primary side of the driver.

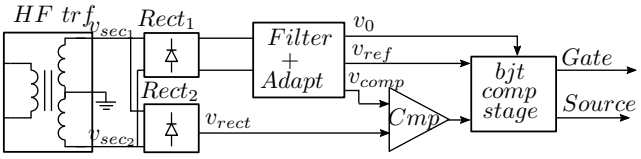


Fig. 4: Secondary side and output stages at the driver.

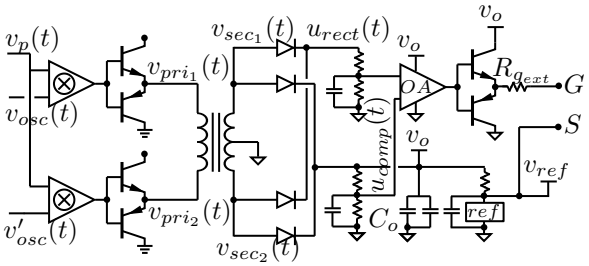


Fig. 5: Detailed schematics of the self-powered circuit.

At the secondary side, a diode rectifying stage provides the required output voltage, $v_o(t)$, needed to supply all the remaining stages, by charging the output bulk capacitor C_o. A block diagram of this scheme is shown in Fig. 4, while Fig. 5 shows a more detailed circuit. In order to achieve a proper operation, the effects of the parasitic elements in the driver must be kept under control. A secondary side based in a two-winding scheme has been used in order to decrease the effect of the diode capacitances in the rectifier. A fixed reference signal, $v_{ref}(t)$ is also generated to attain the negative turn-off voltage. Also from the secondary terminals of the transformer, the control signal is reconstructed by means of an additional diode rectifying stage, yielding to signal $v_{rect}(t)$. Fig. 2 shows the theoretical waveforms involved. This signal enters into a final block formed by a comparator plus a power stage based on a complementary scheme of two BJTs. This power stage, that is supplied by the output voltage $v_o(t)$, provides the final gate-to-source voltage, $v_{gs}(t)$, to the target power MOSFET. The reference voltage $v_{ref}(t)$ ensures the required recommended gate voltage values for SiC MOSFET, i.e. +20 V and -5 V for turn-on and turn-off, respectively.

III. Design of the Proposed Driver

The driver is designed to supply C2M0080120D SiC MOSFETs from $Wolfspeed$ ($V_{ds} = 1200V$, $I_{D@25^\circ} = 36A$, $R_{ds_{(on)}} = 80m\Omega$, $Q_g = 62nC$, $G_{gs} = 950pF$, $G_{gd} = 7.6pF$). The main driver parameters are stated in Table I

TABLE I: Main parameters of the driver

Parameter	Symbol	Value
Switching frequency	f_s	100 kHz
Modulating frequency	f_m	1 MHz
Duty ratio range	d	0%-100%
Gate-Source turn-on voltage	u_{gsON}	+20V
Gate-Source turn-off voltage	u_{gsOFF}	-5V

The blocks at Fig. 1 have been designed and simulated in $LTSpice$, considering the complete models of every part, including estimated parasitic components. The oscillator and adaptation stages have been implemented using a commercial operational amplifier LM6172, from TI. The transformer has been implemented in a ring core of 3E5 magnetic material (TX10/6/4 core size from $Ferroxcube$). The diode rectifiers at the secondary side have been implemented using PMEG6020 Schottky diodes from NXP. The output comparator has been implemented also with the LM6172, and the output power stage has been implemented using ZXTN25040 and ZXTP25040 BJTs from $ZETEX$. It must be noticed that the input BJT complementary stages in Fig. 5 have different voltage and current ratings, and therefore they could be implemented with different part references. Fig. 6 shows the simulated waveforms of the designed gate driver. As it can be seen, the driver provides the desired output waveforms. However, in the simulation, some distortion appears in the waveforms, compared to the ideal theoretical ones sketched in Fig. 2. This mismatch is due to parasitic elements in the circuit, such as the magnetizing and dispersion inductances or the winding resistances in the transformer, the BJT complementary stage output impedances, or the internal equivalent circuits of the operational Amplifiers.

In particular, the time delays in the turn-on and turn-off pulses of the PWM waveform from the original $v_p(t)$ voltage to the output $v_{gs}(t)$ voltage is a combination of the propagation delays caused by the subsequent stages (mainly the comparators ICs, but also due to the complementary BJT stages), plus the contribution of the charging transient of the charging RC rectified voltage that reconstructs the PWM waveform at the secondary side. The effect of these delays will be discussed in the next section.

IV. Built Prototype and Implementation Issues

The next stage in the design is to build a prototype of the proposed gate driver. Fig 7 shows two working prototypes of the proposed design, used for the experimental test presented ahead. The operation of the prototype has been characterized and presented in Fig. 8 with the main actual waveforms in the driver, for f_m=1 MHz, and for a PWM signal of f_s=100 kHz and a duty ratio of 50%. The driver has been tested at full duty ratio range, showing adequate operation, therefore showing the expected behavior. The measurements have been taken on a DLM2000 Mixed Signal Oscilloscope from $Yokogawa$. The csv files obtained from the digital oscilloscope plots have been represented using $MATLAB$.

In addition to the approach presented in Fig. 1, a synchronization block between HF and LF signals has been implemented to avoid glitches. Fig. 9 shows both the oscillator block and the synchronization stage. In this scheme, the synchronization stage takes place at the falling edge of the original PWM signal. This can be noticed as a slightly larger turn-off time in the oscillator 1MHz waveform at the falling edges of the PWM signal, in CH2 at Fig. 8. However, this has no practical effect in the operation of the driver.

Due to all the stages and parasitic elements involved, a given delay exists between the PWM original signal, v_o, and the output v_{gs} waveform. These delays are shown in Fig. 10. In this plot, two complementary PWM signals,

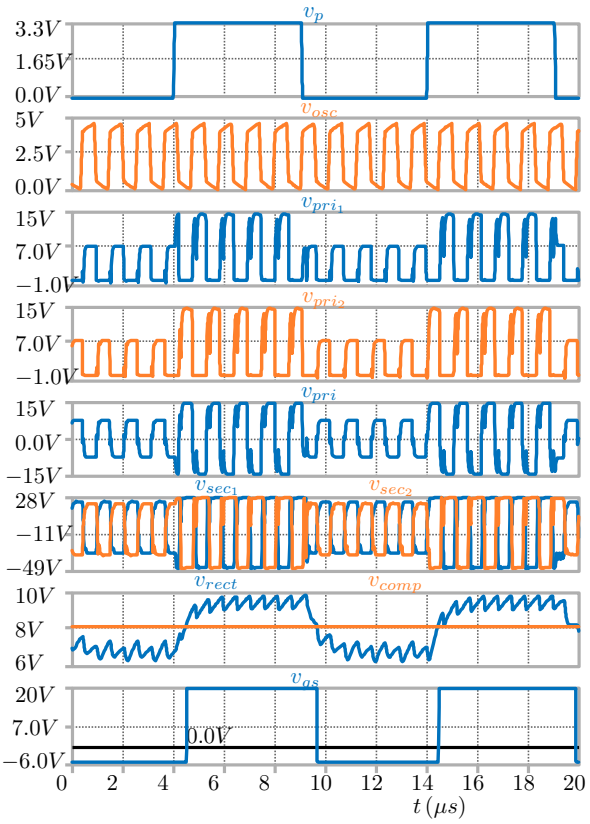


Fig. 6: Simulation waveforms of the proposed driver. $v_p(t)$: Original PWM signal. $v_{osc}(t)$: HF oscillator square waveform. $v_{pri_1}(t)$ and $v_{pri_2}(t)$: complementary modulated waveforms at each terminal of the primary transformer. $v_{pri}(t)$: Resulting modulated waveform at the primary side of the transformer. $v_{sec_1}(t)$ and $v_{sec_2}(t)$: Waveforms at both secondary side windings. $v_{rect}(t)$: Rectified and filtered waveform. $v_{gs}(t)$: Gate-to-Source voltage.

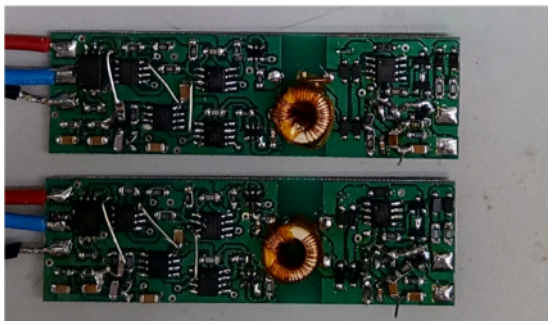


Fig. 7: Prototype of the proposed drivers (PCB dimensions 80x24 mm each)

$v_{o_A}(t)$ and $v_{o_B}(t)$, have been provided to the actual drivers shown previously. A dead time of 200ns has been programed between signals. It can be seen how the output signals, $v_{gs_A}(t)$ and $v_{gs_B}(t)$, track the original PWM waveforms, with a given delay of around 500ns each. However, this delay is kept constant and it is symmetric, therefore not affecting the operation of the

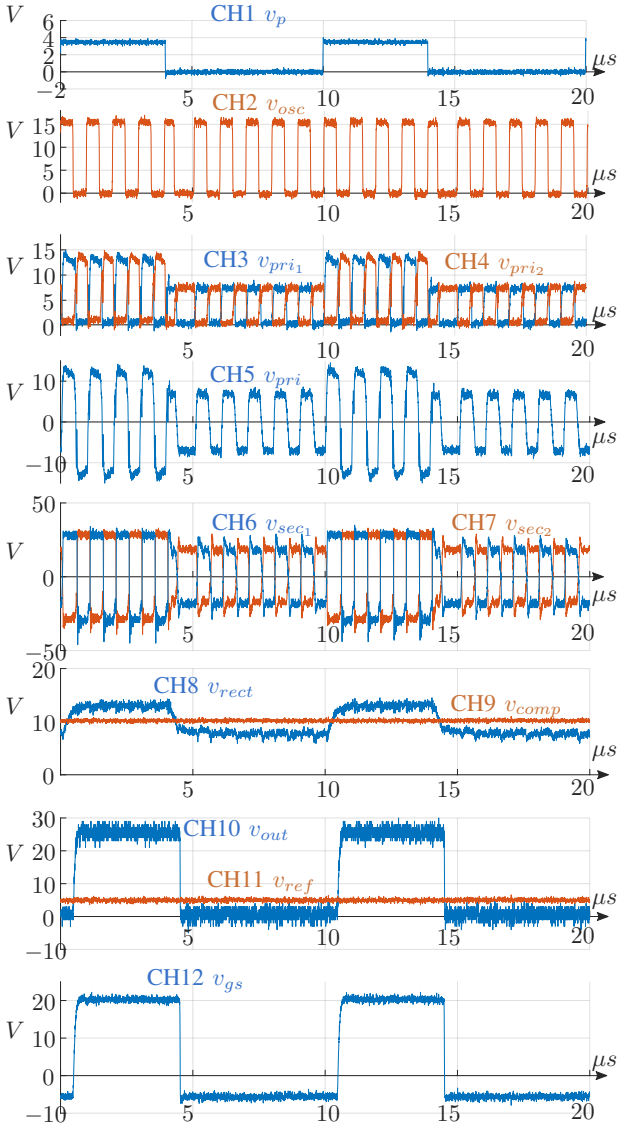


Fig. 8: Experimental waveforms of the built prototype. CH1: $v_p(t)$, original PWM signal. CH2: $v_{osc}(t)$, oscillator signal. CH3 and CH4: $v_{pri_1}(t)$ and $v_{pri_2}(t)$, complementary modulated waveforms at the primary terminals. CH5: $v_{pri}(t)$, resulting waveform at the primary side of the transformer. CH6 and CH7: $v_{sec_1}(t)$ and $v_{sec_2}(t)$, secondary side voltages. CH8: $v_{rect}(t)$, rectified voltage at the secondary side. CH9: $v_{comp}(t)$, comparison value. CH10: $v_{out}(t)$, output of the secondary comparator. CH11: $v_{ref}(t)$, reference value for turn-off level. CH12: $v_{gs}(t)$, gate-to-source voltage value.

driver. The reference design driver from the manufacturer [39] is based on a combination of an optocoupler and a pulse power amplifying IC. The combined final delay for the standard solution is around 350ns. This is in the same range of the values measured in the proposed demonstrator. It must also be noticed that the performance of the proposed solution largely depends on the specific comparator selected, and that a large room for optimization is expected in an eventual pre-industrialization optimizing stage of the design.

Fig. 11 shows detailed turn-on and off switching transients, to assess how the delays and dead times are maintained in the original and in the v_{gs} waveforms. Given that these delays are constant and symmetric at turn-on and turn-off, the effect can be included in the control schemes if required.

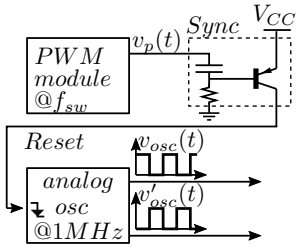


Fig. 9: Oscillator block and synchronization block (sync) schematics of the proposed driver

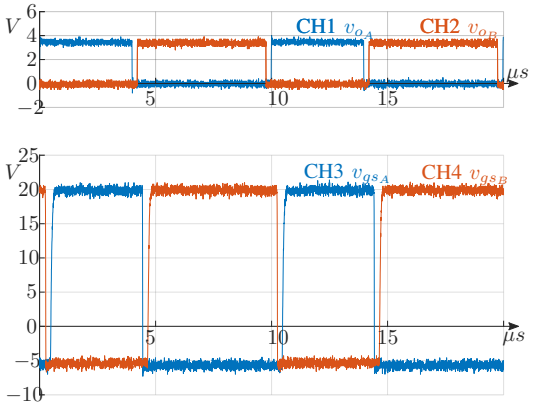
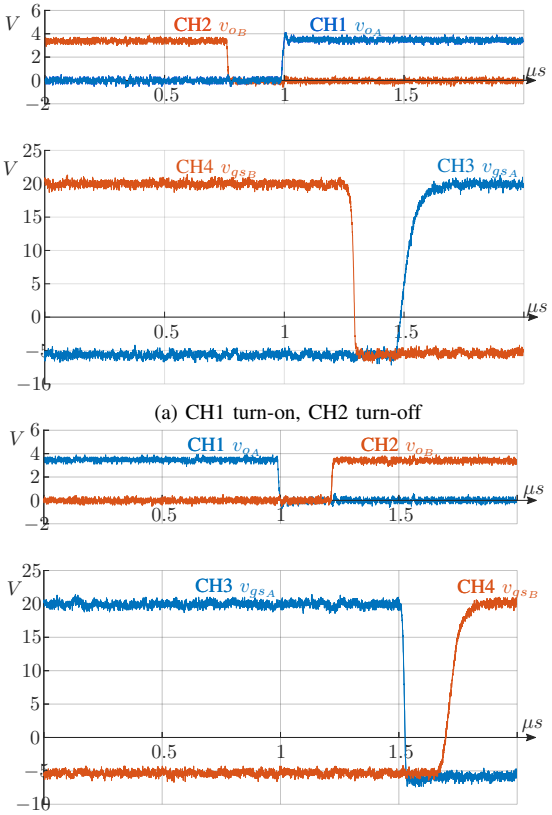


Fig. 10: CH1 and CH2: original PWM complementary signals, v_{o_A} and v_{o_B} (with a dead time of 200 ns). CH3 and CH4: Power switch gate-to-source voltage complementary signal, v_{gs_A} and v_{gs_B}.

In order to demonstrate the performance of the driver for different duty ratio values of the original waveform, but also to assess that the delays and dead times are ensured within all the PWM range, Fig. 12, shows a set of plots with duty ratios of 10%, 30%, 50%, 70% and 90% for the signal v_o. The complementary PWM



(a) CH1 turn-on, CH2 turn-off

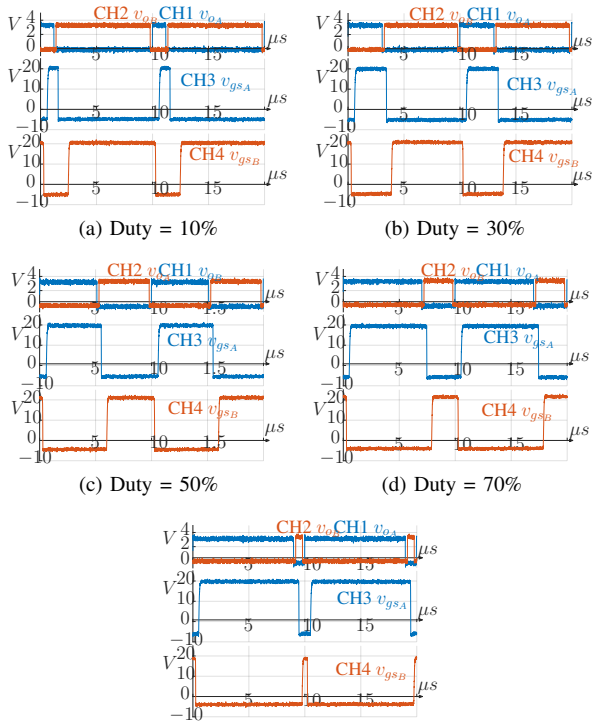
(b) CH1 turn-off, CH2 turn-on

Fig. 11: CH1 and CH2: original complementary signals, v_{o_A} and v_{o_B} (with a dead time of 200 ns). CH3 and CH4: Power switch gate-to-source voltage complementary signal, v_{gs_A} and v_{gs_B}.

signal, as well as the gate-to-source resulting waveforms of both drivers are also shown. As it can be seen, the driver performs adequately within all the PWM range. The critical part to ensure both galvanic isolation, correct signal transfer and Common Mode Immunity (CMI) is the transformer. The built transformer has been characterized, and Table II shows the main transformer parameters measured at 1 MHz. The equivalent circuit is shown in Fig. 13

From Table II, it can be seen that the parasitic coupling capacitor between primary and secondary side, C_C presents a small value, below 3 pF. This value is much smaller than the typical values available in commercial DC/DC isolated sources, usually around 10 times larger [40]. Such reduction in the capacitance implies high immunity CMI.

In order to verify the effect of the output resistor R_{dr_o} on the driver waveforms, a specific characterization has been carried out. It must be noticed that this output resistor is the addition of the external gate resistor, depicted in Fig. 5 as $R_{g_{ext}}$, plus the internal gate resistor



(a) Duty = 10%

(b) Duty = 30%

(c) Duty = 50%

(d) Duty = 70%

(e) Duty = 90%

Fig. 12: CH1 and CH2: original complementary signals, v_{o_A} and v_{o_B} (with a dead time of 200 ns). CH3 and CH4: Power switch gate-to-source voltage complementary signal, v_{gs_A} and v_{gs_B}.

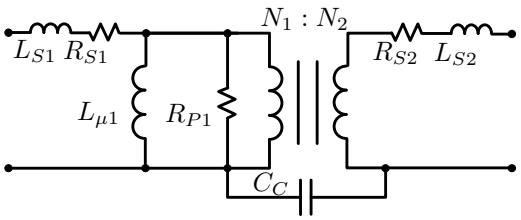
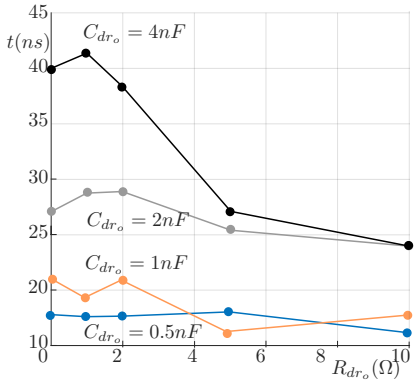


Fig. 13: Equivalent circuit of the transformer.

of the device, $R_{g_{int}}$. Fig. 14 shows the rise and fall times at the output waveform of the driver, v_{gs}, testing the circuit with a standard RC load. This circuit is formed by the given resistor R_{dr_o} when a capacitor, C_{dr_o}, is connected as load in the driver. The rise and fall times have been measured as the interval between the instants in which the waveform reaches 10% and 90% of the final value. It can be seen how the output pulse characteristics depend on the RC combination, and therefore a given optimal value of the external resistor might be calculated for each power device, as a function of the internal values of the gate resistor, $R_{g_{int}}$, and the internal input capacitance, C_{iss}.

TABLE II: Main parameters of the transformer

Parameter	Symbol	Value
Series Resistor at Primary Side	R_{S1}	54 mΩ
Leakage Inductance at Primary Side	L_{S1}	250 nH
Magnetizing Inductance from Prim. Side	$L_{\mu 1}$	440 μH
Turns Ratio	$N_1 : N_2$	10:22
Series Resistor at Secondary Side	R_{S2}	330 mΩ
Leakage inductance at Secondary Side	L_{S2}	1.70 μH
Parallel Resistor from Primary Side	R_{P1}	1.2 kΩ
Capacitance measured between windings	C_C	2.13 pF



(a) Rise time

(b) Fall time

Fig. 14: Rise and fall times for v_{gs}, as a function of R_{dr_o} for different C_{dr_o} values.

V. Experimental Validation and Discussion of the Results

Two driver prototypes have been tested in a 400 V-2 kW DC-DC synchronous buck-boost converter, implemented with C2M0080120D SiC MOSFETs from *Wolfspeed*, as previously stated. This device comes in a standard TO-247 package. Fig. 15 shows the power topology, both switches (S_1 and S_2) and the drivers (DS_1 and DS_2). Fig. 16 depicts experimental waveforms of

the converter, at 300 V input voltage and 3 A input current, showing the drain-to-source voltage of switch S_1 (the switch connected to the input source) and the gate-to-source voltage waveforms of both transistors, at 100 kHz switching frequency and 50% duty ratio. As it can be seen, both switches are driven in a complementary scheme. As early mentioned, the operation at higher frequencies has also been assessed. Fig. 17 shows the performance of the driver when the switching frequency is increased up to 200 kHz.

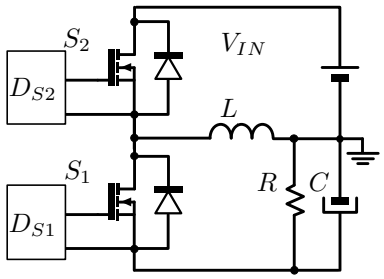


Fig. 15: Power topology used for device testing (DC-DC synchronous buck-boost converter)

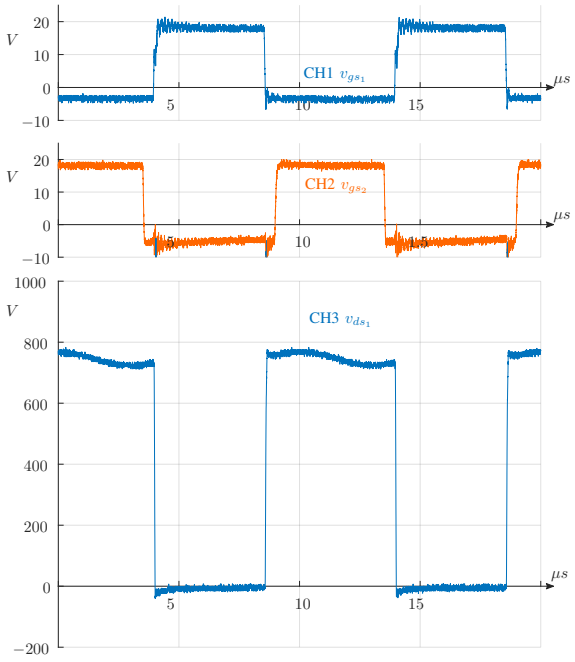


Fig. 16: Experimental waveforms at the converter, for 100 kHz switching frequency. CH1: v_{gs_1} of switch S_1. CH2: v_{gs_1} of switch S_2. CH3: v_{ds_1} of switch S_1.

The external gate resistance $R_{g_{ext}}$ has been chosen to be 5Ω, in order to find an acceptable trade-off between rise and fall times (considering Fig. 5) and the v_{gs} ringing, as it will be explained in the following paragraphs.

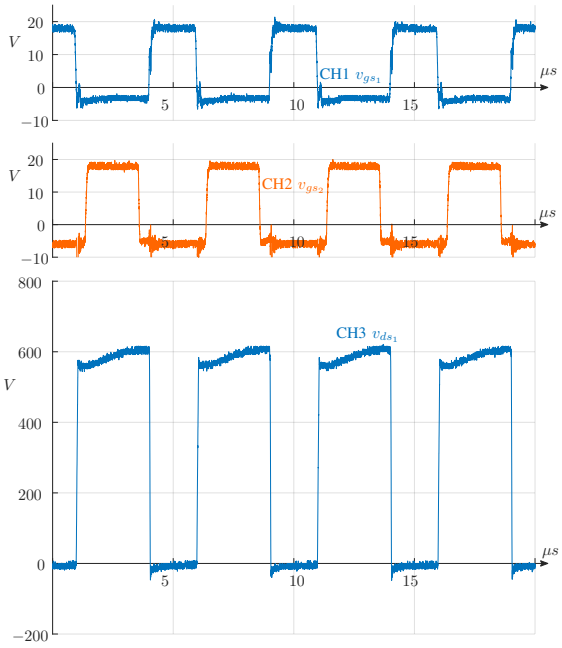


Fig. 17: Experimental waveforms at the converter, for 200 kHz switching frequency. CH1: v_{gs_1} of switch S_1. CH2: v_{gs_2} of switch S_2. CH3: v_{ds_1} of switch S_1.

Details of the turn-on and turn-off switching waveforms of switch S1 are depicted at Figs. 18 and 19, respectively. These plots show the effects at the gate-to-source voltage waveforms at S_2 of the switching in S_1. The ringing due to the large dV/dt in the driver waveforms can be seen. However, this voltage does not reach values close the threshold levels, therefore ensuring immunity to this switching.

In addition, these plots also show the rise and fall time at the drain-to-source waveforms (55 ns and 40 ns, respectively) at 600V dc link voltage. Fig. 20 shows the rise and fall times of the drain-to-source voltage in the power switch for several dc link voltages, already shown in [35]. Regarding drain-to-source dV/dt values, it can be seen how, on average, the v_{ds} rising slope reaches over $50V/\mu s$, while the falling slope stays around $40V/\mu s$. It must be noticed that the relatively low rise and fall time values have been increased in order to decrease this ringing in the gate waveforms. These time values are considered as admissible, given that the scope of this work is intended to demonstrate the feasibility of the proposed scheme. This also helps in keeping EMI issues in reasonable levels. Nevertheless, if these values are found to be excessively low for faster SiC or even GaN devices, it must be noticed that the switching performance could be enhanced, by optimizing the redesign of the driver. The main challenges with faster

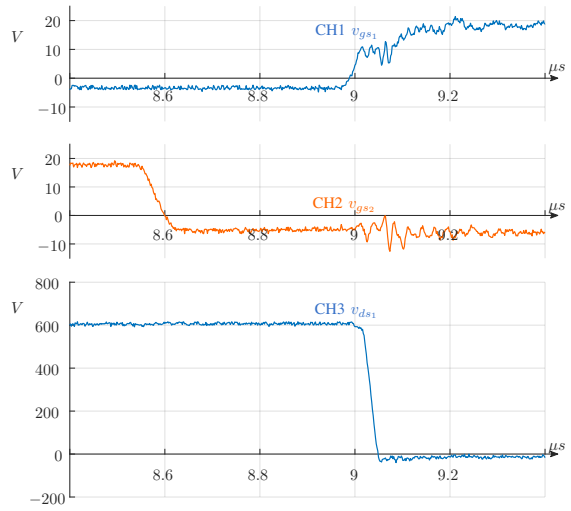


Fig. 18: Detail of the switching waveforms at the converter, at switch S_1 turn-on. CH1: v_{gs_1} of switch S_1. CH2: v_{gs_2} of switch S_2. CH3: v_{ds_1} of switch S_1.

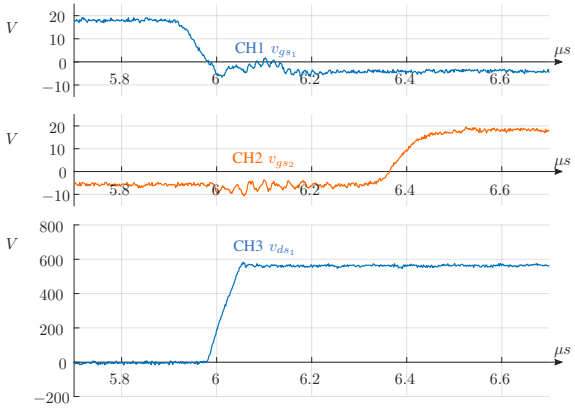


Fig. 19: Detail of the switching waveforms at the converter, at switch S_1 turn-off. CH1: v_{gs_1} of switch S_1. CH2: v_{gs_2} of switch S_2. CH3: v_{ds_1} of switch S_1.

switching times can be resolved with faster comparators and complementary BJT stages, and re-designing the PCB layout of the gate loop. These measures will tend to decrease the effect of the parasitic gate inductance and the output stage impedance in the switching sequence. In fact, this is considered as a future development of this work, considering an eventual design optimization process in a pre-industrial implementation of the concept.

In the technical literature about SiC MOSFETs, considering the dV/dt values presented in this paper, the most common way to avoid dV/dt issues is to ensure an ultra-low coupling capacitance between the control

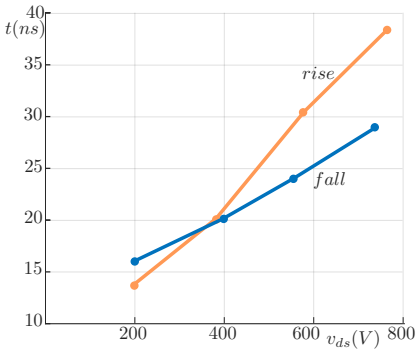


Fig. 20: Experimental values of rise and fall times in the v_{ds} waveform as a function of the DC link values.

signal generation side and the power device side together with an adequate driver layout, but simultaneously ensuring that the driver is able to withstand a high isolation voltage between both sides [41], [42]. Regarding the coupling capacitor, the implemented toroidal core provides a capacitance value (few nF) significantly smaller than the values found in alternate solutions [40]. But in addition, it is particularly critical to minimize the effect of any common mode current path in the circuit [41]. This is an issue in standard drivers, where the parasitic capacitance of the DC-DC power converter used to supply the secondary side of the driver couples with the parasitic capacitance of the optical/magnetic signal transmission subcircuit. In the proposed converter, the common mode path problem is less relevant, as only one element (the transformer) is used to couple the sides of the control and power device. This contributes to decrease dV/dt effects, yet still a careful design of the routing and winding strategies is required, in order to avoid these common mode issues.

The observed ringing around the Miller plateau shown in Fig. 18 is caused by the resonance between the parasitic inductor of the gate driver, SiC MOSFET package and the gate capacitance [43]. However, this ringing does not provide any crosstalk phenomenon, as the gate voltage does not reach the threshold levels of the devices. Generally speaking, the threshold voltage instability of SiC devices can be greater than those of standard silicon devices [44]. When discussing on the effect of the temperature alone, several references can be found that state the typical variations of the threshold voltage vs. temperature in WBG devices [45]–[47]. In the particular SiC device used, the decrease of the threshold voltage vs. temperature, from room temperature up to 150°C is of 0.5V, roughly around 20% of the initial value, in line with the aforementioned variations referred [48]. In any case, given that the nominal turn-on and off voltages provided by the driver are the recommended operational

values obtained from the manufacturers datasheet for the device, no effect on the switching operation is expected with regards to this variation. It must also be noticed that these values are the standard ones for this power rating devices, even from different manufacturers. Hence, a redesign of the driver could easily be carried out in order to tune these parameters for other desired values if required.

The variation of the oscillation amplitude at the Miller Plateau as a function of the temperature, is generally considered minimal in these devices [49]. However, any potential cross-talk risk comes from the decrease of the threshold voltage with increased temperature discussed in previous paragraphs. But the combined effect of selecting adequate gate driver output resistors for turn on and off, together with the use of the recommended negative turn-off voltage, ensure adequate operation of the driver.

Given that the propagation delays in digital circuits tend to increase with higher temperatures, in general it is expected a slight increase on the driver dead time as temperature rises [50]. However, using high performance extended temperature range comparators, ensures that this variation is low enough. In the case of the implemented parts, the slew rate is practically constant with the temperature, however the propagation delay increases with temperature around 10% from ambient temperature up to 125°C. This variation is assumed as reasonable for the driver under consideration.

Finally, Figs. 21 and 22 show the evolution of the power consumption in the driver. Fig. 21 represents the power consumption of a single driver, at full load of the converter, for a $f_{sw} = 100kHz$ and a modulating frequency $f_{mod} = 1MHz$, as a function of the duty ratio D. The power consumption is roughly around 2.5W, increasing slightly towards high duty ratio values. It must also be remarked that this value is a clear minimization target for future versions of the driver. On the other hand, Fig. 22 shows the power consumption per driver, again at full load of the converter, keeping unchanged the $f_{sw} = 100kHz$ and $D = 50\%$ values, but as a function now of the modulating frequencies, f_{mod}. As it can be seen, an increase of the modulating frequency would yield to higher power losses in the driver.

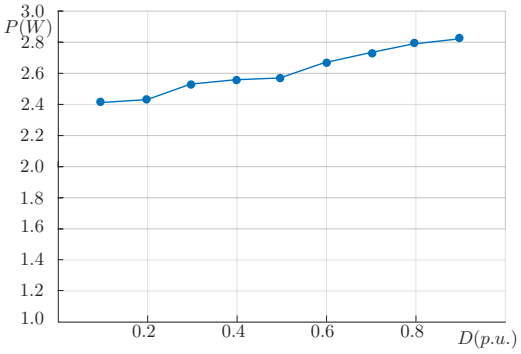


Fig. 21: Power consumption of a single driver as a function of the duty ratio D, at $f_{SW} = 100kHz$ and $f_{mod} = 1MHz$

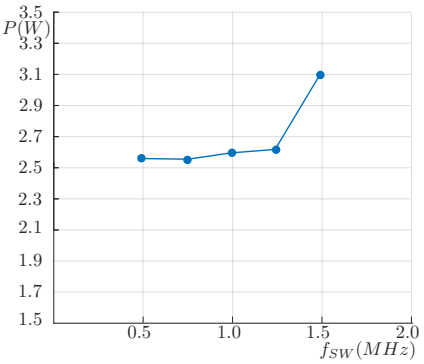


Fig. 22: Power consumption of a single driver as a function of the modulating frequency f_{mod}, at duty ratio $D = 50\%$ and $f_{SW} = 100kHz$.

VI. Conclusions and Future Developments

In this paper, a new isolated gate driver for SiC MOSFETs has been proposed, designed and experimentally tested. The operation of the driver has been analysed and explained. A prototype of the driver, designed for a modulation frequency of 1 MHz and a switching frequency of 100 kHz has been experimentally verified. The operation of the driver prototype has been discussed against the simulation results obtained with the full component models of the $LTSpice$ environment. After that, the implementation issues of the design, such as the oscillator and PWM synchronization, the transformer design and the output comparator have been discussed. The performance of the driver has been demonstrated for the full PWM range, and experimental waveforms are given to characterize and assess the operating principle of the driver. Finally, preliminary results on a DC-DC converter show the feasibility of this approach. The performance at a switching frequency up to 200 kHz has also been verified through experimental results. It must be noticed how, by using a square waveform modulating scheme, the driver signal can take any value in the full PWM range, and it is not limited by the modulation index.

The main contribution of the proposed work is the use of the square waveform bi-level amplitude modulation scheme generated through a simple circuit, implemented with standard components. The bi-level scheme allows for a 0% to 100% duty ratio operation at the desired

turn-on and turn-off voltage values of the design (in this case +20 V and -5 V, respectively). The simple approach allows for a compact design, suitable when high integration and high power density is required. Considering that the shown prototype has been built in a single layer PCB with standard surface mount components in SMD1206 packages, a final commercial design can easily reach a size smaller by a factor of 2 to 3 and even more. Considering solely the isolation block scheme in both the conventional and proposed driver respective areas, then an initial comparison can be carried out. In the conventional solution, the joint area of the DC-DC converter plus the optocoupler IC is around 220 mm^2 [40]. However, the transformer area of the proposed converter is smaller than 100 mm^2. This increases the power density of the final power converter significantly. Provided that the implementation of the presented proof of concept of the driver does not require any external DC-DC switching converter for the secondary side of the driver, nor an optocoupler device, and given that the parts used for the demonstration include only simple elements (resistors and capacitors, signal diodes and BJT stages, comparators and a single transformer), the driver can be easily integrated with the power device in a single package, thus achieving a dramatic size reduction. Finally, and given the followed design approach, it is also worth mentioning that the proposed circuit can be easily adapted to other WBG families such as GaN, by simply changing key parameters in the design.

Future works include the optimization of the design for achieving higher dV/dt at the gate-to-source waveforms, a detailed characterization of the power consumption of the gate driver as a function of the different operating parameters (switching frequency, duty ratio, etc.) or the inclusion of protections. Regarding this last issue, a key aspect is the shortening of the time delay introduced by the driver, that can be carried out through the aforementioned design optimization. This optimizing process is based on selecting the best-performing parts for the specific design (considering specific voltage and current values at the input and at the power device together with the parasitic elements in key components); also on the optimization of the RC charging stage after rectifying the secondary side pulses (which reconstructs the original PWM waveform through the output comparator); and finally on a multilayer PCB routing strategy to minimize the gate-to-source path and the driver size. All these aspects jointly tackled are required to achieve a pre-industrial version of the proposal, that has been validated and demonstrated in this work as a proof of concept of the implementation.

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