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Optimization of a Series Converter for Low-Frequency Ripple Cancellation of an LED Driver

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Abstract: In this paper, the optimization of the power and control stages of a previously proposed topology for an off-line LED electronic driver is presented. The full system avoids the use of electrolytic capacitors at the *DC* link, therefore increasing the lifespan and reliability of the driver. As a consequence of having a relatively small capacitance, the *DC* link operates with a large Low-Frequency (*LF*) voltage ripple. This work presents a design optimization for the power and control stages of a current-fed bidirectional buck converter, operating as the LED current control stage. As this block processes only the *AC* power arising from the *LF* voltage ripple, it can increase the system efficiency against the typical two-stage solution. In the original proposal, the main drawback was the high inductor losses due to the resulting large inductor currents and large inductance value. The proposed optimization ensures an enhanced design of the inductor while keeping a constant current through the LEDs. A new optimization methodology is proposed and the theoretical results have been validated in a built prototype for a 40 W LED lamp.

Keywords: LED driver; lighting electronics; *LF* ripple cancellation; single-phase converter

1. Introduction

Presently, LED lighting systems are gaining more importance as they provide a tool for a more rational use of electrical energy on household, public lighting systems, transportation, commercial applications, etc. [1,2]. Therefore, one of the major power electronic development fields is related to the enhancement of efficient high-performance electronic lighting systems for LED lamps. The main features to consider when designing an LED driver are its *DC* voltage source behavior (a *DC* driving stage able to limit the LED current must be used), the long operating life (the driver must last at least as long as the LED itself), and the color variations (there are some parameters that affect the color such as the waveforms, the operating temperature, etc.).

For low requirement applications, simple, passive, or cost-effective solutions can be used to deal with the *DC* behavior of the LED lamp [3]. For instance, [4] presents a linear regulator integrated with an LED lamp that provides an optimal solution in terms of power density for single LED applications. But generally speaking, linear regulators are not recommended when the application requires a high number of LEDs (as the overall efficiency of the system turns more critical) or when high-performance control schemes are needed. In fact, the driver might also include additional features

such as dimming—either Amplitude Modulated (AM) dimming or Pulse Width Modulation (PWM) dimming—, current derating, etc. Linear regulators can be used for implementing AM dimming, but in case PWM dimming is required (to avoid color shift or stability problems at low power, as in higher power LED Lamps), switch-mode regulators are much more adequate. Also, the future deployment of DC grids will allow significant simplification in the LED driver topologies used for DC applications [5]. However, taking into account the regulations and standards that lighting equipment must fulfill, in most cases high-performance drivers are required. The LED driving system must provide not only AC-DC efficient conversion, but also LED current control, Power Factor Correction (PFC) and input current Total Harmonic Distortion (THD) control.

As the lifespan of the driver is expected to match that of the LED lamp [6], some constraints are derived for the design of the electronic stage [7]. For instance, large electrolytic capacitors usage is highly inadvisable, considering their shorter operating life compared to the life of the LED lamp [8]. Many recent works in the literature agree that large capacitance values for the power stage of LED drivers need to be avoided [9–15]. In order to achieve this goal, electrolytic capacitors must be discarded. Therefore, researchers have come up with novel control strategies [16–19] as well as optimized topologies [6,13,20–33] that imply smaller capacitances in the DC link, to overcome this issue.

Two-stage schemes are the most common approach when designing single-phase LED ballasts. A first active PFC stage controls the power factor and the line current harmonics content. Considering a power factor close to unity, the input power to this active stage pulsates at twice the line frequency. In order to guarantee the instant power balance, this input stage delivers the pulsating power to a second stage, interfaced through an energy storage device. This storage part is usually a capacitive device at the DC link. The main voltage ripple component at this capacitor, at twice the line frequency, is a function of the capacitance value, taking into account that higher capacitances mean smaller ripple amplitudes. To ensure proper operation of the system, and to effectively control the output power through the LEDs—and hence the emitted light—standard output stages require a low voltage ripple at the DC link. This guarantees a given constant DC current through the LEDs. These large capacitance values are implemented by means of electrolytic technology devices, which achieve such high capacitance values in reasonable component size.

In the conventional scheme, each of the stages processes the full amount of power, ensuring enough design flexibility as it decouples the input and the output constraints, allowing for simple solutions. However, this usually results in relatively low efficiencies, higher volume, and components count.

A second strategy divides the output power of the input stage in two different power flows. The largest share of this power is delivered directly to the LED lamp, while the rest of the power (including the AC part) is processed by a second stage. This ensures the AC power ripple cancellation at the load [29–32]. Upon careful design considerations, this scheme provides an overall system efficiency increase, as most of the power is processed only once.

The approach followed in this work delivers all the DC part of the output power of the input stage, and uses a second stage to process only the AC. Therefore, this bidirectional stage stores energy in some intervals and sends it back to the DC link in others. Provided that adequate management of the AC power is carried out, the resulting power through the LEDs will be pure DC, therefore allowing for higher ripples and smaller capacitances at the DC link. This capacitance reduction is the main purpose of the proposed topological scheme. Given that these low capacitance values can be achieved with technologies such as plastic film capacitors, thus avoiding the reliability problems derived from the use of electrolytic parts, therefore extending the lifespan of the system. In particular, this work improves the performance of the system presented in [33] but including a deeper analysis that allows for an optimal design strategy in terms of power density and efficiency.

The design of the second stage has one degree of freedom, which is related to the inductance value of an inductive energy storage device, L_{Sto}. Therefore, the performance of the output stage (size, weight, power losses, dynamic behavior, etc.) largely depends on this L_{Sto} value. In a first approach, the design of this inductor is carried out by analyzing the steady state, open loop operation of the circuit, for different L_{Sto} inductance values, considering two key dimensions of this performance. These two factors are losses on one hand (both copper and core losses), and size (and therefore weight) on the other hand. A trade-off between those two dimensions is initially achieved, although it is considered to be unfeasible, as it will be justified. After that, a novel closed-loop operation analysis of the output stage has been carried out, and as it will be shown, a smaller, yet more efficient design of the inductor L_{Sto} will be achieved, considering the same trade-off approach in terms of losses vs. size than in the steady-state analysis previously discussed. This work shows the detailed procedure of the optimization process, and demonstrates its feasibility through simulations and by experimental validation on a 40 W design example.

The paper is divided as follows. Section 2 deals with the considered LED driving strategy. Later, Section 3 presents and discusses the proposed topology and its basic operation. Sections 4 and 5 show the switching and dynamic equations of the open loop operation respectively, in order to obtain the transfer functions of the proposed scheme. A design example for open loop operation is given in Section 6, while Section 7 shows the simulation results obtained with this configuration. The control scheme implemented for closed-loop operation is discussed in Section 8, whereas Section 9 shows the experimental results of the closed-loop operation of the converter. Finally, Section 10 shows the main conclusions of this work as well as the future developments.

2. Bidirectional Output Stage for LED Drivers

To process the *AC* power at the *DC* link, two possibilities can be used, based on the connection of the stage and the LED lamp. Figure 1 depicts both cases, and as it can be seen, the equivalent circuit of the input PFC stage is modeled by a *DC* current source, I_{DC}, in parallel with an *AC* current source, I_{AC}, charging the *DC* link capacitor, *C*.

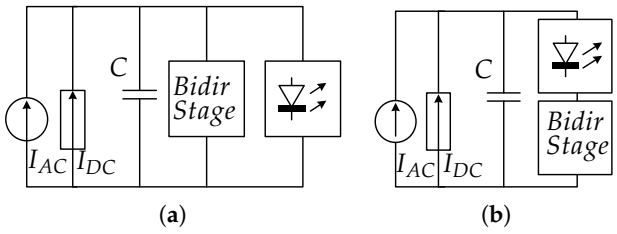


Figure 1. Connection options for bidirectional converter. (**a**) Parallel connection. (**b**) Series connection.

Figure 1a shows the parallel configuration that uses an additional capacitor as main storage device [13,32]. This work uses the series configuration proposed in [33] and depicted in Figure 1b. From this diagram, it can be understood that the voltage ratings in this stage are smaller than the *DC* link ratings, allowing for the use of low voltage components. Also, the proposed converter must allow single polarity current flow, but it must enable voltage blocking capability with both positive and negative polarities. Although it is out of the scope of this work, it must be commented that the series scheme has inherent *PWM* dimming capability, just by turning on and off the series stage. In terms of efficiency, the switches are rated for relatively low voltage values, which implies smaller parasitic elements in general terms, which provide expected benefits in switching and conduction losses. However, as it will be seen throughout the work, the most important concern is related to the losses at the storage inductor. This work presents a new design methodology for the control scheme of the bidirectional stage, targeting the optimization of this inductor. Thus, the full system efficiency is increased when compared to the previous design proposed in [33].

3. Proposed Topology

Figure 2 shows the block diagram of the full off-line High Frequency (*HF*) LED driver with the followed approach. After being rectified and filtered, the input voltage enters the input *PFC* stage, which processes the energy towards the *DC* link capacitor, C_{link}. However, the selection and proper design of this input stage is out of the scope of this work. The input of the second stage, u_{Cs}, is connected in series with the LEDs assembly. As a small capacitance value is selected for the capacitor C_{link}, in order to avoid electrolytic technologies, a significant *AC LF* ripple appears at the *DC* link voltage, u_{link}. Figure 2 also depicts the simplified waveforms in the expected operation of the system (pure *DC* voltage at u_{LEDs}, and pure *AC* voltage at u_{Cs} as well).

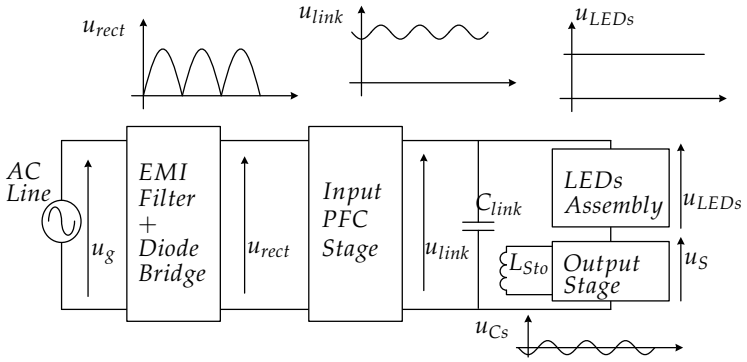
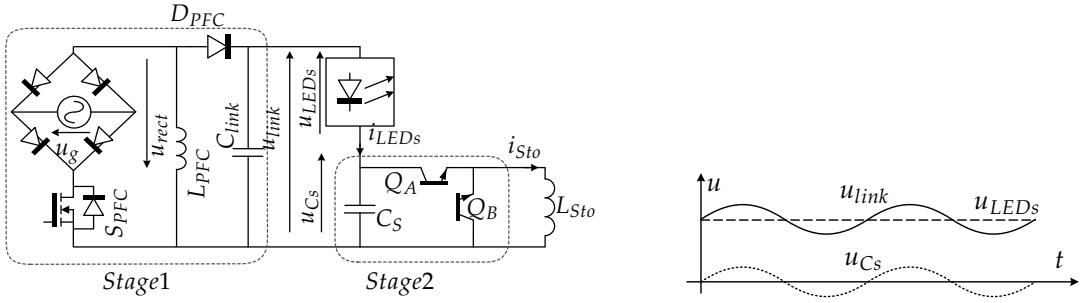


Figure 2. Proposed scheme. The second stage processes the small amount of *AC* power, thus keeping high efficiency and small LEDs current ripple.

Figure 3a details the topology of the system. A grid-side PFC stage is implemented by means of a Discontinuous Conduction Mode (*DCM*) buck-boost converter, in order to provide unity power factor with constant duty ratio. This input stage supplies power from the grid towards the *DC* link. Connected to this DC link, the proposed bidirectional series circuit can be seen. This stage is a current-fed bidirectional buck converter, formed by switches Q_A and Q_B, capacitor C_S and the storage inductor, L_{Sto}. The input of this stage is considered to be the LEDs current, i_{LEDs}, with the output variable being the current through the inductor L_{Sto}, i_{Sto}. Q_A and Q_B have been represented as bipolar transistors for simplicity, as they must be able to block reverse voltages. In the final prototype, they will be implemented by means of MOSFET transistors with a series blocking diode. Figure 3b depicts again the main *LF* voltage waveforms at the driver, sharing the time axis.



(**a**) Power Stages (**b**) Main Waveforms

Figure 3. Proposed Circuit, with the input *PFC* stage and the output buck stage delivering energy back to the *DC* link.

4. HF Analysis of the Proposed Topology

The *HF* and *LF* analysis of the basic topology for this application has already been presented in [33]. The most important conclusions to this analysis are reviewed in this work. The *HF* analysis

employs a fixed frequency control, denoting the switching period as T. The common HF analysis in power electronics is based on considering that the system operates in steady state. Therefore, the significant waveforms of the most relevant devices can be calculated for one switching period, keeping in mind that for any magnitude considered to be a function of time, $x(t)$, the following equation is fulfilled:

$$x(t) = x(t+T) \tag{1}$$

This is achieved through a power balance, as the circuit input power in one period equals the power delivered to the output stage. It must be taken into account that there is not an output load in the proposed stage able to dissipate active power. This implies that the input power in one switching period will not be dissipated. In turn, the energy will be stored within the storage inductor, L_{Sto}, by changing the electric parameters at this device. Therefore, the analysis cannot be based on considering steady state in a switching period, and (1) is not fulfilled anymore. Instead, this analysis must be focused on finding the variations of the capacitor voltage, $u_{Cs}(t)$, and the storage inductor current, $i_{Sto}(t)$, in a switching period, while the LEDs current remains constant. Figure 4a shows the voltage and current references considered during the analysis. Only complementary operation of switches Q_A and Q_B is considered. The duty ratio, D, is defined for switch Q_A. Given that the current through the storage inductor will flow either through Q_A or Q_B, thus:

$$i_A(t)|_T < i_{Sto}(t)|_T \tag{2}$$

where $i_A(t)$ is the forward current through Q_A (see Figure 4a, and the expression $x(t)|_T$ denotes the average value of a generic magnitude $x(t)$ in a switching period, T. Furthermore, (2) ultimately states that the current flowing through the storage inductor will always be greater than the LEDs current. The HF analysis considers two switching modes in a switching period. While Q_A is turned on and Q_B is turned off, i.e., $0 < t < D \cdot T$, the system operates in Mode I. On the other hand, for the complementary state of the switches, i.e., $D \cdot T < t < T$, the converter operates in Mode II. The full analysis of these modes is given in [33], and only the main statements are summarized here. At instant t_0, the values of the storage inductor current and the input capacitor are, respectively:

$$i_{Sto}(t_0) = i_{Sto0} \tag{3}$$

$$u_{Cs}(t_0) = u_{Cs0} \tag{4}$$

After a switching period T, the waveforms are expressed by:

$$i_{Sto}(t_0 + T) = i_{Sto0} + \Delta i_{Sto} \tag{5}$$

$$u_{Cs}(t_0 + T) = u_{Cs0} + \Delta u_{Cs} \tag{6}$$

After some calculations [33], the final expressions for these parameters can be expressed as:

$$u_{Cs}(t_0 + T) = u_{Cs0} + \frac{i_{LEDs}}{C_S} \cdot (1 - D) \cdot T \tag{7}$$

$$\Delta u_{Cs} = \frac{i_{LEDs}}{C_S} \cdot T - \frac{i_{Sto0}}{C_S} \cdot DT - \frac{\Delta i_{Sto}}{2 \cdot C_S} \cdot DT \tag{8}$$

$$\Delta i_{Sto} = \frac{u_{Cs0}}{L_{Sto}} \cdot DT + \frac{1}{2} \frac{u_{Cs}}{L_{Sto}} \cdot DT \tag{9}$$

Finally, from (8) and (9):

$$\Delta u_S = \frac{i_{LEDs} - i_{Sto} \cdot D - \dfrac{u_{Cs0}}{2L_{Sto}}}{C_S + \dfrac{D^2T^2}{4L_{Sto}}} \cdot T \tag{10}$$

$$\Delta i_{Sto} = \left[u_{Cs0} \cdot \frac{D}{L_{Sto}} \left(1 - \frac{D^2T^2}{4L^2 \left(C_S + \dfrac{D^2T^2}{4L_{Sto}} \right)} \right) + \left(\frac{DT\left(i_{LEDs} - i_{Sto0} \cdot D\right)}{2L_{Sto} \left(C_S + \dfrac{D^2T^2}{4L_{Sto}} \right)} \right) \right] T \tag{11}$$

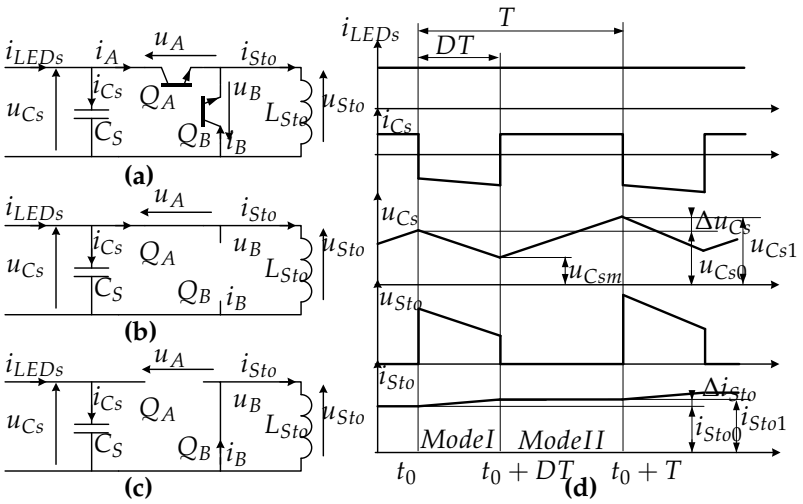


Figure 4. Switching modes of the proposed second stage. (**a**) Voltage and current references of the circuit. (**b**) Mode I, Q_A switched on, Q_B switched off. (**c**) Mode II, Q_A switched off, Q_B switched on. (**d**) Main theoretical waveforms of the output stage.

The expression of the *HF* current ripple through the LEDs can be calculated considering Mode II. In this interval, the capacitor current, i_{Cs}, equals the current through the LEDs. Considering that the *DC* link behaves as a voltage source at *HF*, then the resulting circuit for this subinterval can be seen in Figure 5, in which the LEDs assembly is modeled by a series connection of an ideal diode D_i, a dynamic resistor R_d, and a threshold voltage $V\gamma$. Therefore the *AC* ripple of the current through the LEDs can be calculated considering an exponential discharge through the dynamic resistance of the LEDs, R_d:

$$\Delta i_{LEDs} = \frac{\Delta u_{Cs}}{R_d} \tag{12}$$

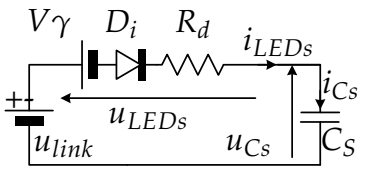


Figure 5. Subcircuit for *HF* LED ripple calculation, in Mode II. (Q_A switched off, Q_B switched on).

5. Dynamic Analysis of the Proposed Topology

The study of the *LF* average model of the main circuit magnitudes enables the dynamic analysis of the system, which in turn is required for designing the control system. Considering (10), (11),

and the waveforms in Figure 4d, the following expressions are found for the capacitor and the inductor waveforms, respectively:

$$C_S \cdot \frac{du_{Cs}(t)}{dt}|_{LF} = i_{LEDs}(t) - i_{Sto}(t) \cdot D \tag{13}$$

$$L_{Sto} \cdot \frac{di_{Sto}(t)}{dt}|_{LF} = D \cdot u_{Cs}(t) \tag{14}$$

These equations yield the *LF* equivalent circuit in Figure 6, for the second stage of the LED driver. The ideal transformer takes into account the effect of the switching of Q_A and Q_B with a duty ratio D for Q_A.

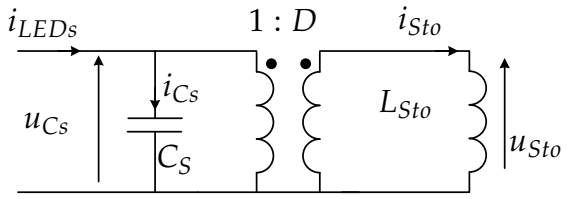


Figure 6. *LF* equivalent circuit of the proposed second stage converter.

6. Design Example for a 40 W LEDs Assembly

With the previous analysis, a design example is proposed for a XLamp® XR-E LED (part XREWHT-L1-0000-00D01) from Cree®, in a series connection assembly of 36 devices, accounting for a nominal power of 40 W. the design parameters of the input PFC stage can be seen in Table 1. The input values for the design are shown in Table 2. In order to design the power stage, both values of L_{Sto} and C_S must be calculated. A target value for the LEDs current ripple will be 10%, considering this parameter is equally split into a 5% at *HF* and a 5% at *LF*.

Table 1. Input PFC Stage Parameters.

Parameter	Symbol	Value
Input Grid Voltage	u_g	$110V_{RMS} - 60$ Hz
Input PFC Buck-Boost Inductor	L_{PFC}	90 µH
Switching Frequency	f_{PFC}	50 kHz
Nominal Duty Ratio	D_{PFC}	32%
DC Link Capacitor	C_{link}	100 µF

Table 2. Initial Design Parameters.

Parameter	Symbol	Value
LEDs nominal current	i_{LEDs}	0.35 A
LEDs voltage (series assembly of LEDs)	v_{LEDs}	121 V
LEDs dynamic resistance (series assembly of LEDs)	R_d	27 Ω
Switching Period	T	20 µs
Maximum *DC* bus peak-to-peak voltage ripple	Δu_{peak}	25 V
DC link ripple frequency	f_{RIPPLE}	100 Hz

The value of the *HF* voltage ripple at capacitor C_S is given by the capacitor charge when Q_A is turned off:

$$\Delta v_{Charge} = \frac{1}{C_S} \cdot (1 - D) \cdot i_{LEDs} \cdot T \tag{15}$$

Therefore, the *HF* current ripple through the LEDs will be:

$$\Delta i_{LEDs} = \frac{\Delta v_{Charge}}{R_d} \tag{16}$$

The worst case will be when $D \to 0$. Therefore, from (15), (16) and Table 2, for a 5% *HF* ripple in the output current, the *HF* current ripple through the LEDs will be:

$$C_S \geq \frac{i_{LEDs} \cdot T}{R_d \cdot \Delta i_{LEDs}} = 5.6\,\mu\text{F} \tag{17}$$

The value of the storage inductor, L_{Sto}, can be calculated considering the performance of the system. The first approach, taken into account in [33], is to supply the system in open loop, with a constant duty ratio, in this case $D = 0.1$, and check the evolution of the waveforms. Upon these conditions, the inductor is chosen as follows. From Figure 6, for a constant duty ratio, and after referring the inductance value to the primary side of the equivalent transformer, the expression for the current through the LEDs becomes:

$$\hat{i}_{LEDs} = \hat{u}_{LEDs} \cdot \frac{1 + s^2 \cdot C_S \cdot \frac{L_{Sto}}{D^2}}{s \cdot \frac{L_{Sto}}{D^2}} \tag{18}$$

This yields an expression of L_{Sto} given by:

$$L_{Sto} = \frac{\Delta u_{Cs} \cdot D^2}{2 \cdot \pi \cdot f_{RIPPLE}(\Delta i_{LEDs} + \Delta u_{Cs} \cdot 2 \cdot pi \cdot f_{RIPPLE} \cdot C_S)} \tag{19}$$

Therefore, the value of L_{Sto} depends on the selected fixed duty ratio, D. The design solution must be optimized in terms of size (core volume of the inductor) and efficiency (losses in the switches and in the inductor). A series of preliminary data has been calculated for four different duty ratio parameters. These figures are represented in Table 3:

Table 3. Preliminary Data for Different Duty Ratio Values.

Parameter	Symbol	Value			
Duty ratio (steady state)	D	0.2	0.1	0.05	0.025
Storage inductor	L_{Sto}	12 mH	3.0 mH	760 µH	190 µH
Nominal current (storage inductor)	I_{LSto}	1.75 A	3.5 A	7.0 A	14 A
HF ripple current (storage inductor)	ΔI_{LSto}	5 mA	10 mA	20 mA	30 mA

From Table 3, it can be seen how the larger the duty ratio, the larger the inductance, allowing for larger core sizes. However, this would imply smaller currents through the inductor, which in turn implies smaller losses. On the other hand, smaller duty ratios cause higher effects of non-linear aspects (switching times, etc.) and parasitic elements. In order to take a final decision, an optimal design of the inductor has been carried out for each of these duty ratio values. This design provides the sizes of the cores, the *AC* and *DC* losses in the inductors, the number of turns, air gap, etc. For simplicity, the core geometry has been restricted to the commercial *ETD* shape; however, the full series of size has been considered (from *ETD*29 to *ETD*59). These results are presented in Tables 4–7, for *ETD* cores, of 3*F*3 magnetic material. The proximity effect has been included within the losses while the skin effect skin-depth which limits the diameter in case it is too large.

Table 4. Main Inductor Design Outputs for $D = 0.2$ ($L_{Sto} = 12$ mH).

Core Size	ETD29	ETD34	ETD39	ETD44	ETD49	ETD54	ETD59
Wires Diam (wires × mm)	1 × 0.3	1 × 0.4	1 × 0.5	2 × 0.5	3 × 0.5	4 × 0.5	6 × 0.55
N of Turns	900	700	540	380	310	240	180
B_{MAX} (T)	0.32	0.32	0.32	0.32	0.32	0.32	0.32
Copper Losses (W)	27	14	7.7	3.3	2.1	1.1	0.61
Core Losses (mW)	0.66	0.94	1.4	2.4	3.3	4.5	6.8
Total L_{Sto} Losses (W)	27	14	7.7	3.3	2.1	1.1	0.62

Table 5. Main Inductor Design Outputs for $D = 0.1$ ($L_{Sto} = 3$ mH).

Core Size	ETD29	ETD34	ETD39	ETD44	ETD49	ETD54	ETD59
Wires Diam (wires × mm)	1 × 0.45	1 × 0.55	2 × 0.55	**3 × 0.55**	4 × 0.55	7 × 0.55	12 × 0.55
N of Turns	450	350	275	**200**	160	120	90
B_{MAX} (T)	0.32	0.32	0.32	**0.32**	0.32	0.32	0.32
Copper Losses (W)	24	15	7.3	**5.1**	2.3	1.2	0.58
Core Losses (mW)	0.66	0.94	1.4	**2.1**	3.0	4.5	6.8
Total L_{Sto} Losses (W)	24	15	7.3	**5.1**	2.3	1.2	0.59

Table 6. Main Inductor Design Outputs for $D = 0.05$ ($L_{Sto} = 760$ µH).

Core Size	ETD29	ETD34	ETD39	ETD44	ETD49	ETD54	ETD59
Wires Diam (wires × mm)	2 × 0.4	2 × 0.55	3 × 0.55	5 × 0.55	8 × 0.55	13 × 0.55	24 × 0.55
N of Turns	230	180	140	100	82	62	47
B_{MAX} (T)	0.32	0.32	0.32	0.32	0.32	0.32	0.32
Copper Losses (W)	28	16	8.3	4.0	2.4	1.2	0.61
Core Losses (mW)	0.65	0.90	1.4	2.2	2.9	4.3	6.3
Total L_{Sto} Losses (W)	28	16	8.3	4.0	2.4	1.2	0.62

Table 7. Main Inductor Design Outputs for $D = 0.025$ ($L_{Sto} = 190$ µH).

Core Size	ETD29	ETD34	ETD39	ETD44	ETD49	ETD54	ETD59
Wires Diam (wires × mm)	3 × 0.5	4 × 0.55	6 × 0.55	11 × 0.55	17 × 0.55	24 × 0.55	44 × 0.55
N of Turns	115	88	70	50	41	31	24
B_{MAX} (T)	0.32	0.32	0.32	0.32	0.32	0.32	0.32
Copper Losses (W)	28	15	8.4	3.9	2.1	1.3	0.63
Core Losses (mW)	0.64	0.96	1.4	2.2	2.9	4.3	5.9
Total L_{Sto} Losses (W)	28	15	8.4	3.9	2.1	1.3	0.64

As an initial guess, a 10% duty ratio has been selected as the minimum value allowing proper operation of the converter. Assuming the total losses in the inductor of around 10% of the output power levels, then from (19) and Table 3:

$$L_{Sto} = 3\,\text{mH} \tag{20}$$

$$D = 0.1 \tag{21}$$

$$I_{LSto} = 3.5\,\text{A} \tag{22}$$

For this inductance choice, Table 5 shows the different coil designs that minimize losses for each ETD size considered. Aiming to balance the size and the losses, the ETD44 size has been selected, and it is represented in bold characters.

7. Validation of the Open Loop Approach

To validate this approach, a simulation has been carried out with the system parameters stated above. The simulation simplified schematics file for *PSIM* can be seen in Figure 7. However,

the simulation results shown in Figure 8 take also into account the parasitic components of the elements in Figure 7.

In Figure 8a, the *LF* evolutions of *DC* link voltage, the capacitor C_S voltage, and the LEDs voltage are shown. As it can be seen, all the *AC* voltage of the *DC* link is held by C_S, and thus the LEDs voltage is a *DC* voltage. The resulting LEDs current can also be seen, still presenting a 100 Hz ripple, although for requirement applications it could be considered acceptable, as some directives allow relatively high HF harmonics levels [34]. Figure 8b shows the *HF* switching system waveforms at 50 kHz, again at full power level. Even though the design provides good results in terms of ripple cancellation and efficiency, the overall size (*ETD*44 for a 40 W converter) results too high, implying an unfeasible solution. In order to achieve a smaller core size, an analysis of the closed-loop control of the system will be carried out, and, as it will be demonstrated, results in a smaller inductor value for the same *LF* current ripple cancellation levels.

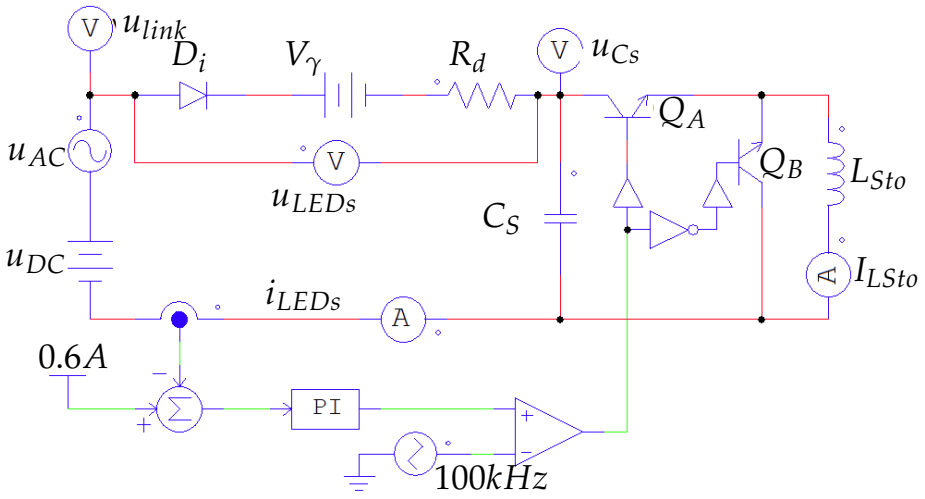
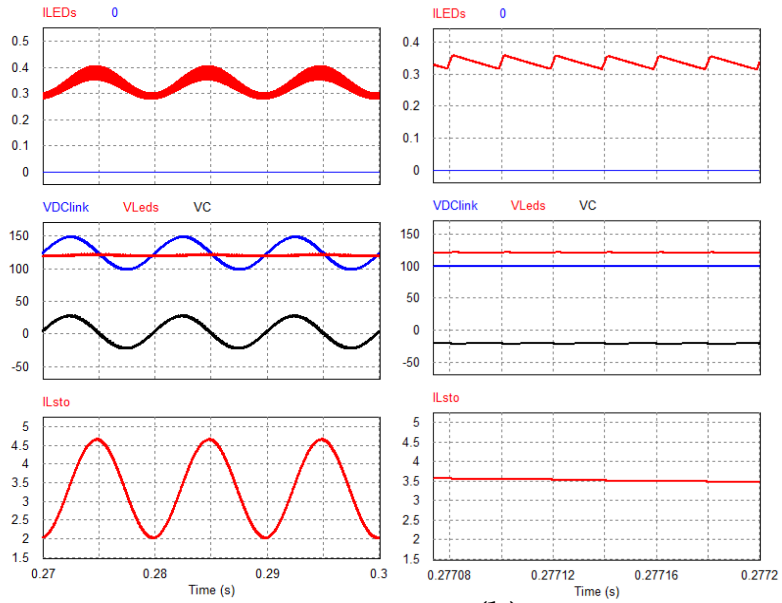


Figure 7. *PSIM* schematics diagram of the proposed topology.



(a) *LF evolution* **(b)** *HF evolution*

Figure 8. Simulation results for full power operation in open loop ($L = 3$ mH).

8. Closed-Loop Control of the Proposed Topology

Figure 9a depicts the equivalent *LF* model of the second stage including the LEDs assembly. The u_{link} voltage source models the output voltage behavior of the input *PFC* stage, including both the *DC* and the *LF AC* ripple voltage components at the *DC* link capacitor. As in the previous discussion, the equivalent circuit that models the LEDs assembly is formed by an ideal diode, D_i, in series with a *DC* source, $V\gamma$, and a resistor, R_d. $V\gamma$ and R_d account for the total threshold voltage and the total dynamic resistor of the LEDs setup, respectively. After following a small-signal analysis approach (linearize and perturb) [33], the final small-signal *AC* model of the circuit is shown in Figure 9b. After some calculations, the transfer functions of the system are finally given by:

$$G_{id}(s) = \frac{\hat{i}_{LEDs}(s)}{\hat{d}(s)} = \frac{U_{Cs}}{D \cdot R_d} \cdot \frac{s \cdot \frac{I_{Sto} \cdot L_{Sto}}{U_{Cs} \cdot D} + 1}{s^2 \cdot \frac{L_{Sto} \cdot C_S}{D^2} + s \cdot \frac{L_{Sto}}{D^2 \cdot R_d} + 1} \tag{23}$$

$$G_{iu}(s) = \frac{\hat{i}_{LEDs}(s)}{\hat{u_{Cs}}(s)} = \frac{1}{R_d} \cdot \frac{s^2 \cdot \frac{L_{Sto} \cdot C_S}{D^2} + 1}{s^2 \cdot \frac{L_{Sto} \cdot C_S}{D^2} + s \cdot \frac{L_{Sto}}{D^2 \cdot R_d} + 1} \tag{24}$$

where G_{id} is the transfer function representing the duty ratio, $\hat{d}$, to the LEDs current, $\hat{i}_{LEDs}$, and G_{iu} is the transfer function representing the voltage across the capacitor, $\hat{u}_S$, also to $\hat{i}_{LEDs}$. Capital letters represent steady-state parameters, while lower case letters with the symbol ˆ represent small-signal variables.

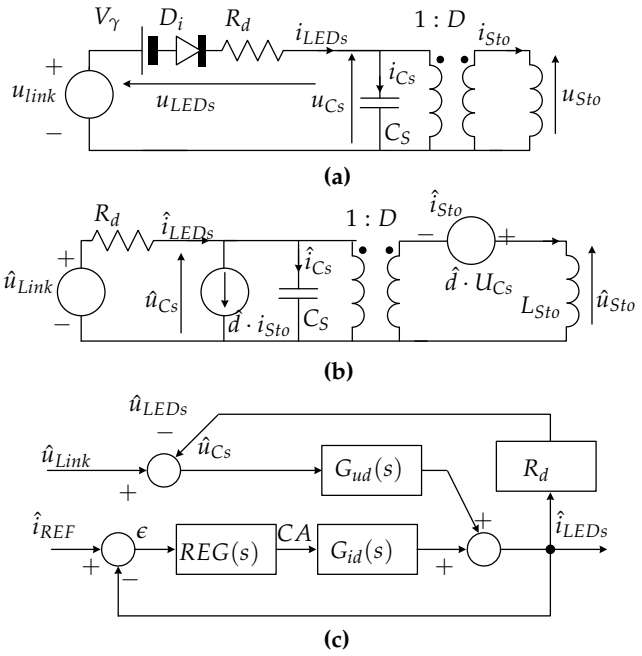


Figure 9. *LF* equivalent circuit of proposed topology.

Figure 9c shows the system block diagram that depicts the current control scheme implemented in the LEDs driver. The current error, ϵ, is the input of the regulator block, $REG(s)$. The output of this block is the control action, CA, that corresponds to the duty ratio of switch Q_A. From (23), it can be seen that the open loop transfer function is a second order system. A PI controller, with a bandwidth

of 1 kHz and a phase margin of 45° has been tuned using *SISOTool* of *MATLAB*, resulting in the following parameters:

$$REG(s) = K_p \cdot \left(1 + \frac{1}{s \cdot T_I}\right) = 8.1 \cdot 10^{-12} \cdot \left(1 + \frac{1}{s \cdot 2.9 \cdot 10^{-5}}\right) \tag{25}$$

Figure 10 depicts some simulation waveforms of the closed-loop system with such a controller. As it can be seen, the *LF* ripple results in a much smaller value than the obtained in open loop. Nevertheless, given that the perturbation represented by the *DC* link voltage ripple, $\hat{u}_{link}$, is continuously changing at twice the grid reference, a complete error cancellation is not possible with a PI regulator. In fact, this error, $G_{LFCR}(s)$, can be calculated as:

$$G_{LFCR}(s) = \frac{\hat{i}_{LEDs}(s)}{\hat{u}_{Link}(s)}|_{\hat{i}_{LEDs}} = \frac{G_{iu}(s)}{1 + REG(s) \cdot G_{id}(s) + R_d \cdot G_{iu}(s)} \tag{26}$$

The value of this error is a function of the storage inductor, L_{Sto}, and of the parameters of the regulator. This opens an interesting option, which is to optimize the design (including the inductance value and the regulator parameters) for a given target parameter. In this case, the target will be to decrease the inductance value, keeping constant the control parameters (bandwidth and phase margin), and ensuring that the *LF* ripple is equal or smaller than in the open loop case. Table 8 shows a set of designs for different inductor values, along with the resulting control parameters that ensure relatively similar dynamic performance.

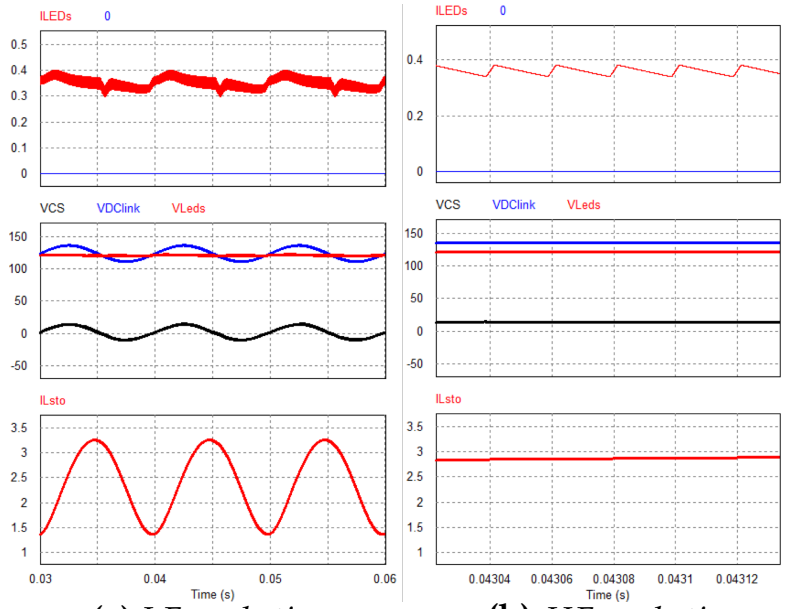


Figure 10. Simulation results for full power operation in closed loop ($L = 3$ mH).

Table 8. Control Parameters Design for Closed-Loop Operation with Different Inductor Values.

Inductance (μH)	**30**	**90**	**300**	**900**	**3000**
K_p	0.004	0.104	**0.079**	0.057	0.081
T_i	2.5×10^{-6}	6.5×10^{-6}	$\mathbf{3.7 \times 10^{-6}}$	2.5×10^{-6}	2.9×10^{-6}
$\lvert G_{LFCR}$(@100 kHz)$\rvert$(dB)	−50	−50	**−54**	−60	−78
V_{DC} offset (V)	–	23	**14**	8.3	3.5
η_{MAX} (%)	–	86%	**90%**	95%	98.5%
Losses (W)	–	7.0	**4.3**	2.6	1.0

To make a decision, the design solution must be optimized in terms of size (core volume of the inductor), efficiency (losses in the switches and in the inductor) and implementation (allowing enough control margins in the control action variable). For very small L_{Sto} values, the control action gets too high, and the control loop is unable to operate properly in the carried-out simulations. On the other hand, very high values of L_{Sto} yield large size cores, which result in non-practical design values. Thus, the optimal solution has been chosen as $L_{Sto} = 300$ µH (highlighted in bold characters in Table 8). For this new value of the inductor, a new design is given in Table 9. Again, and in order to balance the size and the losses in the core, the ETD34 size has now been selected, and it is represented in bold characters in Table 9.

Table 9. Main Inductor Design Outputs for ($L_{Sto} = 300$ µH).

Core Size	ETD29	ETD34	ETD39	ETD44	ETD49	ETD54	ETD59
Wires Diam (wires × mm)	3 × 0.5	**4 × 0.55**	6 × 0.55	8 × 0.55	10 × 0.55	13 × 0.55	24 × 0.55
N of Turns	90	**70**	54	39	32	24	19
B_{MAX} (T)	0.32	**0.32**	0.32	0.32	0.32	0.32	0.32
Copper Losses (W)	6.9	**3.1**	1.6	1.0	0.94	0.88	0.79
Core Losses (mW)	0.65	**0.94**	1.4	2.2	2.9	4.5	5.8
Total L_{Sto} Losses (W)	6.9	**3.1**	1.6	1.0	0.94	0.88	0.80

Comparing Tables 5 and 9, a theoretical 2 W power losses decrease in the total inductor losses can be achieved, accounting for around a 5% efficiency gain. This is obtained even moving to an $ETD34$ core size, significantly smaller than the first guess, and much more adequate for a 40 W design. The system has been again simulated for the PI controller selected from Table 8. Figure 11 shows the simulated behavior of the system. As it can be seen, the resulting LEDs current ripple has also a smaller value, therefore the design has been optimized in terms of inductor size. However, as the real inductor is much smaller, the inductor average current and LF current ripple is larger. As the system needs to avoid the current to evolve to negative values (as switches Q_A and Q_B cannot withstand negative currents), the capacitor C_S voltage presents a DC offset. This ensures low ripple in the LEDs current, but unfortunately provides a decrease in the system efficiency. These losses are represented, for the inductor values considered, in the last row of Table 8.

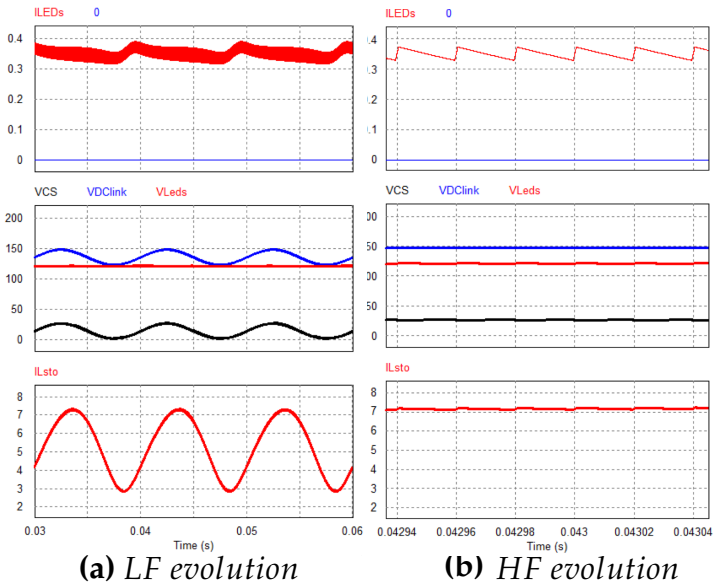


Figure 11. Simulation results for full power operation in closed loop ($L = 300$ µH).

Therefore, with the new inductor, there is an increase of 4.3 W in the system power losses due the capacitance offset required for proper operation of the output stage. However, from Tables 5 and 9,

a saving of 2.1 W is obtained in the inductor L_{Sto} (as its inductance decreases by a factor of ten). Therefore, considering the power balance, the global loss increase is around 2.2 W for this solution, but significantly decreasing the size of the inductor (from $ETD44$ to $ETD34$). Depending on the particular application considered, a trade-off must be carried out, in order to select the optimal size of the inductor.

9. Experimental Results of the Closed-Loop Operation

To validate the design, a prototype of the proposed second stage has been built and tested. This prototype is shown in Figure 12, along with the LED Lamp and the digital controller.

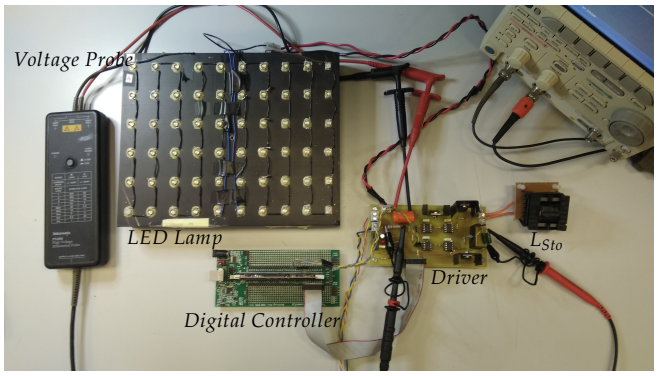


Figure 12. Experimental setup of the built prototype.

The built LED driver is intended for a lamp with the specifications given in Section 6 and Table 2. The system is operating with the optimal inductor from Table 9 (i.e., $ETD34$, $L = 300$ µH), for a steady-state operation at a nominal current of 350 mA. The PI controller of the current loop has the parameters defined in Table 8 for this inductance value. The input of the setup is a programmable DC voltage source $HP6812A$, in order to control the average and ripple values of the DC link voltage. The switches have been implemented connecting in series a $BYW29200G$ diode from $OnSemi$ and an $IRF640$ from IR. Figure 13 shows the steady-state operation of the system. As it can be seen, the steady-state operation is similar to the one depicted in the simulations at Figure 11.

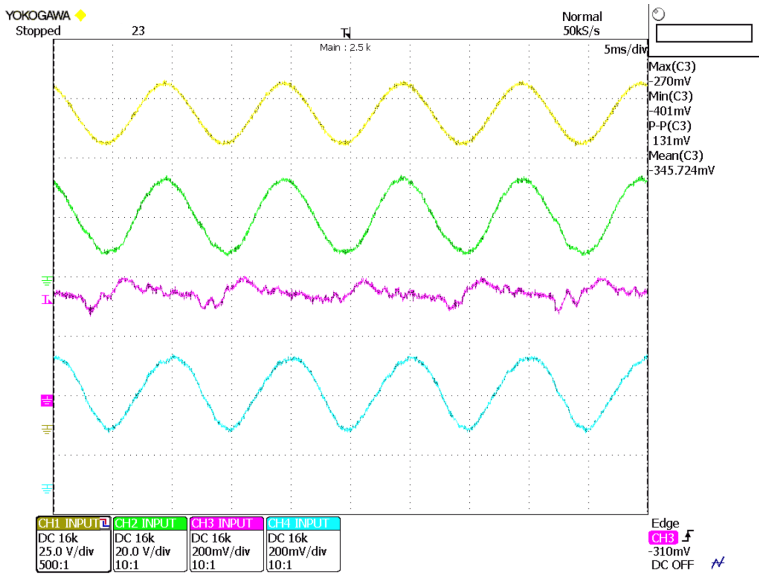


Figure 13. Experimental results of the closed-loop system (5 ms/div). CH1 (yellow): u_{link} (25 V/div). CH2 (green): u_{Cs}, (20 V/div). CH3 (magenta): I_{LEDs} (200 mA/div). CH4 (blue): I_{Lsto} (200 mA/div).

The final power losses at the output stage are 6.4 W, allowing for a final efficiency of this secondary stage of 87%. It can be noted how in this particular design, the primary goal is the size reduction of the converter; higher efficiencies can be achieved at the cost of increasing the core size. Figure 14 finally shows the dynamic performance of the controller, upon a current step from 350 mA to 300 mA. As it can be seen, the system reaches the new steady state in less than half a line frequency cycle.

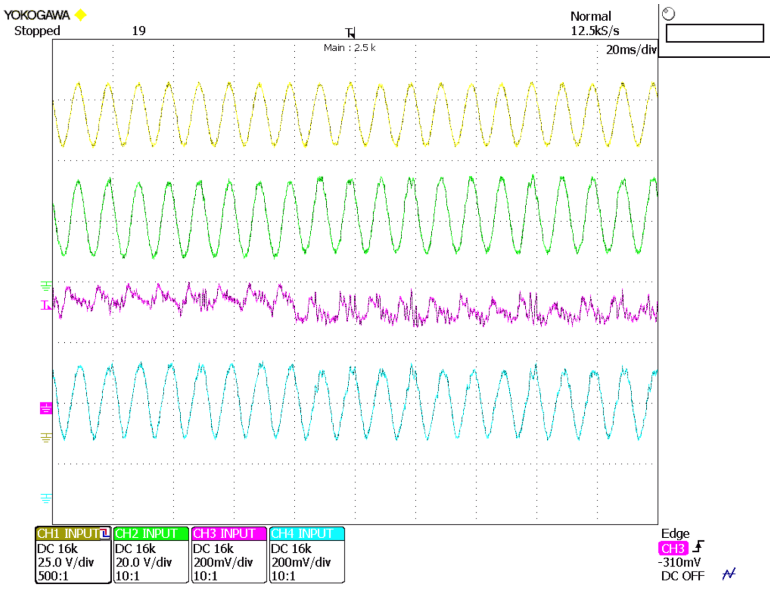


Figure 14. Experimental results of the closed-loop system (20 ms/*div*). CH1 (yellow): V_{DClink} (25 V/*div*). CH2 (green): V_{Cs}, (20 V/*div*). CH3 (magenta): I_{LEDs} (200 mA/*div*). CH4 (blue): I_{Lsto} (200 mA/*div*).

10. Conclusions and Future Developments

The LED driver topology proposed in [33] for the output stage of an electronic driver for power LEDs has been deeply analyzed, and a new design methodology for optimizing the converter size has been proposed. This methodology has been validated both by simulations and experimentally. The advantages of this improved methodology are mainly two: first, the optimization of the inductor design which implies that the resulting inductor value can be built in an *ETD*34 core, and secondly, the dynamics of the controller are improved allowing for comparably faster performance which implies that the proposed series scheme is suitable for *LF PWM* dimming control.

The main drawbacks of the proposed driver are the number of components (two extra switches, which in addition must be driven with isolated drivers, as well as the reactive elements C_S and L_{Sto}), plus the mandatory current control loop (including sensor, microcontroller, etc.). Comparing the closed-loop control schemes, in standard LED drivers, the *DC* link voltage control is mandatory, while the LED current control can be achieved without a dedicated closed loop (for instance, in open loop by means of a peak current control through the LEDs); however, with the proposed series output stage, the LED current control is also necessary to attain proper operation of the stage. Future developments of the work include the design of a full off-line driver, also considering the input *PFC* stage in the control system, as well as the experimental validation of the system operating under *PWM* dimming scheme. Also, alternative control methods such as peak current control or resonant current control can be explored.

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Abbreviations

The following abbreviations are used in this manuscript:

MDPI	Multidisciplinary Digital Publishing Institute
DOAJ	Directory of open access journals
TLA	Three letter acronym
LD	linear dichroism

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