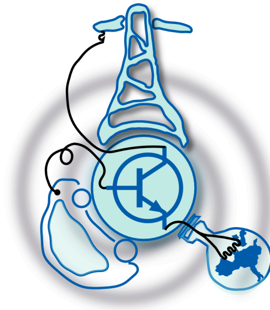
Simulative and Experimental Characterization of 650V GaN High Electron Mobility Transistors

by
Rand Bassam AL Mdanat



Submitted to the Department of Electrical Engineering, Electronics, Computers and Systems
in partial fulfillment of the requirements for the degree of
Erasmus Mundus Joint Master Degree in Sustainable Transportation and Electrical Power Systems
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Abstract

The Gallium Nitride High Electron Mobility Transistors (GaN HEMT) based on field-effect transistors came out as new promising candidates for the high-frequency high-voltage applications, due to their unique capabilities of achieving higher current density, higher breakdown voltage, higher operating temperatures and higher frequencies compared to conventional silicon (Si) transistors.

In this thesis, these novel transistors will be studied to understand their material properties and their main electrical characteristics. Then, a double pulse test will be carried out to study the switching behaviour of these transistors. Since the double pulse test is a practical method of characterizing the transient performance of semiconductors transistors under hard switching. The test will be performed experimentally and in simulation under different operating conditions to have the ability to understand the difference in the transistor behaviour under these different operating points. To do so, an evaluation kit from GaN Systems will be employed, as well as a Digital Signal Processor (DSP) of Texas Instruments. A PCB will be designed as an interface between the evaluation kit and the DSP to allow the control and the communication between them. While for the simulation, it will be implemented using LTSpice software, since GaN Systems provides an LTSpice model for their devices, which allows the evaluation of the device performance.

Finally, the obtained results will be presented, commented and compared to identify the particularities of these devices.

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Chapter 1

Introduction

1.1 Introduction

Since the invention of the world's first electronic device, power electronics appeared as an attractive subject area in electrical engineering. This is mainly due to its ability to make significant contributions towards modern technological growth [13]. Power electronics has developed continuously over the years and is finding increasing applications, nevertheless, recently it started to face some challenges in order to meet the requirements of new technologies. The continuous growth in renewable energy systems, energy storage applications, and electric vehicles require power devices with a significantly high efficiency. Moreover, the upsurge of wireless communication technologies (satellite communications, TV broadcasting, broadband wireless internet connection) and military applications created the need for high power high-frequency power devices. These applications need to become more rigid, as faster and higher capacity wireless data transfer over long distances is becoming a common need for both military and commercial applications [14].

Semiconductor materials are the core of power electronics devices. Silicon (Si) has been the basic and dominant material for these devices for the last half century. Because it was more reliable, easier, and cheaper to use. All these advantages are the result of the basic physical properties of silicon, in addition to the huge investment in manufacturing infrastructure and engineering [4, 12, 15]. This technology became more mature over the past 30 years. Silicon technology is rapidly approaching its

theoretical limits imposed by the intrinsic material proprieties, which suffers from limitations regarding blocking voltage capability, operating temperature, and switching frequency. These inevitable physical limits reduce the capability and the efficiency of the power semiconductor system. Unfortunately, these limitations will prevent silicon power devices to stay as the dominant material in the power electronics market for future applications [1, 16, 17].

As a consequence of these limitations and the need for high power high-frequency devices, a new semiconductor material drew the attention of researchers as it is showing some promising results which could lead to a new generation of power devices. This new material has the capabilities to satisfy the future needs for high operating frequencies, high output power, and high operating voltages. Wide bandgap (WBG) semiconductors, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), can be defined by their larger-than-Si bandgap, typically between two and four electron volts (eV). They have the potential to meet future needs due to their superior material properties, as they feature higher blocking voltage capabilities, faster-switching speeds, high-temperature operation, and lower on-state resistance when compared to (Si). The high voltage breakdown will be beneficial in high voltage applications (i.e. grid) and in increasing the efficiency of the existing power conversion. Moreover, faster switching yields to higher power density. As a result, (WBG) devices will improve the efficiency of the power conversion, as well as reducing the device switching losses which will lead to the reduction of the cooling system requirements hence improving the size and saving the cost [17–21].

Figure 1-1 compares between the relevant material properties for Si, SiC and GaN which include the energy gap, (breakdown) electric field, thermal conductivity, electron velocity, and melting point. The high electric field and the wide energy gap allow operation at high voltages. The high saturation electron velocity allows operation at a high switching frequency.

From Figure 1-1, it is clear that the WBG devices increase the capabilities of power electronics devices and can be used in applications which Si devices could not cover. SiC will be the preferred choice for high-temperature applications since GaN presents a lower thermal conductivity. On the other hand, GaN is considered an outstanding material for high-frequency and high-voltage operation.

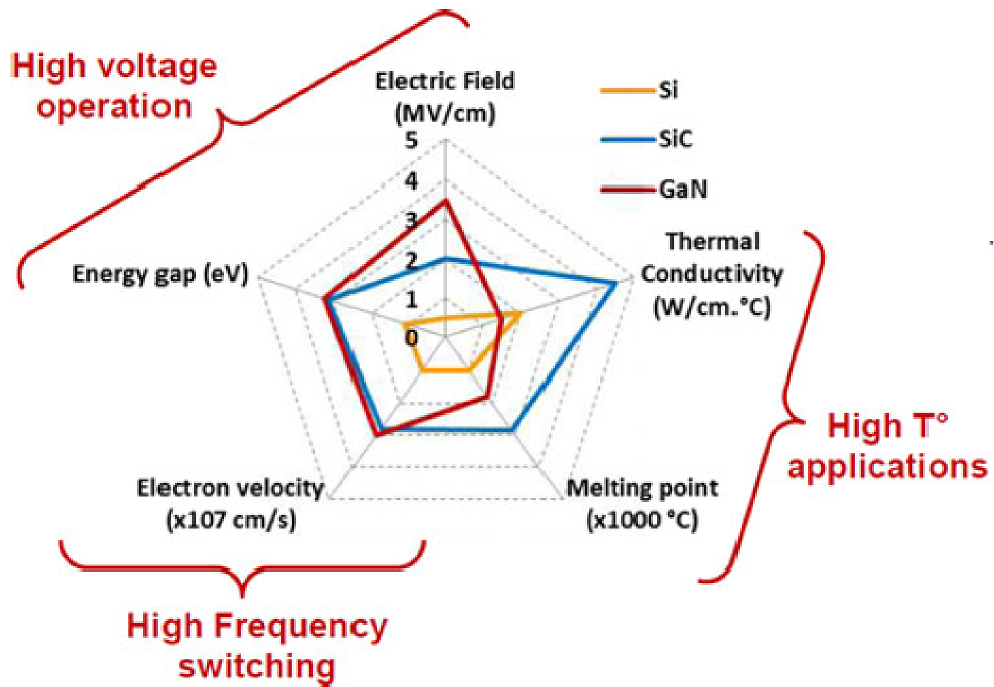


Figure 1-1: Comparison between Silicon, Silicon Carbide and Gallium Nitride based on their physical properties [1]

Gallium nitride high electron mobility transistor (GaN HEMTs) have more advantages among their competitors. The high electron mobility and ability of GaN to form heterojunctions put GaN devices in front of SiC and Si. These devices have a high current density and low channel resistance, which are suitable for high frequency operation and power switching applications. Furthermore, the operation at high voltage due to its high breakdown electric field provides the potential to obtain high efficiency and fewer power losses, as well as better noise performance [18, 22, 23].

These novel power devices represent a real breakthrough in power electronics although many developments are still required, and this is the reason for this work. This thesis is the first step towards the design of GaN based converters; possible converters would be dc-dc converters for dc microgirds, dc-ac low voltage grid-interface inverters and automotive traction inverters.

1.2 Objectives

Since Gallium Nitride technology is showing promising results for future semiconductors. The central theme of this thesis is to study and analyze the switching behaviors of Gallium Nitride (GaN) transistors through the double pulse test. To do so the high-power Insulated Metal Substrate (IMS) Evaluation Platform (from GaN Systems) and its corresponding motherboard GSP65HB-EVB were used. The fundamental objectives guiding the work process can thus be listed to

- Deep theoretical analysis of GaN transistor material properties and electrical characteristics.
- Theoretical overview of the double pulse test, its constraints and, measurements techniques.
- Design of the control interface hardware required for measuring all the required magnitudes, and detecting possible faults (PCB design).
- Simulation of the double pulse test using GaN LTspice model.
- Implementation and testing the PCB.
- Generating a double pulse signal from Texas instrument DSP.
- Assembling the double pulse setup.
- Experimental validation.
- Analysis and comparing experimental results with simulations.

1.3 Thesis Structure

After the current chapter 1 which introduces the motivation of the work, objectives and structure, Chapter 2 does a deep theoretical study of the main characteristics of the GaN high electron mobility transistors. The theoretical analyses will include the basics and main material properties of GaN devices and then compare them with other semiconductor materials. The basic structure of GaN transistors, its electrical characteristics and finally the gate driving constraints will be introduced as well.

Later, a detailed explanation about the test carried out to study the switching characteristic of the GaN device is done in Chapter 3. The theoretical overview double pulse test will be explained, besides the test constraints and the measurement techniques that should be used to get the best results from this test. Moreover, the design main requirements will be addressed such as the experimental evaluation kit, the GaN transistor that had been used in the experimental test.

After that, Chapter 4 will include the software design of the double pulse test circuit, which was done using LTSpice software, the second half of this chapter will discuss the implementation of the test setup. In this section, the design of the printed circuit board used in the setup will be explained in details, the method to generate the double pulse test signal using a microcontroller, and finally this section will show the complete setup of the test.

In Chapter 5 the results of the experimental and stimulation tests will be presented, commented and compared, the test was done under different electrical parameters to be able to achieve a clear understanding of the device performance. The analysed voltages were: V_{in} = 50V; 100V;150V; 200V; 250V; 250V. The analysed currents for each voltage level were: I = 5A; 10A; 15A; 20A; 25A; 30A, and this chapter will show some of these results. Moreover, anlayazing the switching losses using LTSpice software will be addressed in this chapter. Finally, Chapter 6 will include the conclusion of the project and the future work.

Chapter 2

Gallium Nitride Transistors Overview

Gallium nitride (GaN) power devices are a new technology that is drawing attention. This new technology enables the design of converters at higher frequencies and efficiencies than those achievable with conventional Si devices. Gallium Nitride (GaN) based on high electron mobility transistors (HEMTs) is a field effect transistor in which two layers of different bandgap and polarization field are grown upon each other, creating the Two Dimensional Electron Gas (2DEG) chanel, which is one of the main advantages of GaN HEMT devices. In this chapter a deep theoretical study will be carried out, discussing the main material properties of GaN with comparison to other competitor devices and the electrical characterises showing that GaN HEMT devices are the best candidate for high power high frequency applications.

2.1 Gallium Nitride Basics

2.1.1 Gallium Nitride Material Properties

High power high frequency requirements for nowadays applications are becoming more stringent and a common need. And as Si-based devices could not satisfy these requirements because of material limitations, as mentioned in section 1.1, Wide Bandgap (WBG) devices appeared as a technology to enable applications with these requirements, Gallium Nitride semiconductor devices seem to superior semiconduc-

tors for high power high frequency applications due to their material properties.

Table 2.1 [22, 24–26] shows a comparison between the material properties of different semiconductor devices, these properties improved the ability of GaN devices to compete in the future and to fulfill the requirements of the new applications.

Table 2.1: Material Properties of Silicon, GaN, and SiC

Property		**Si**	**GaN**	**SiC**
Bandgap E_g	eV	1.1	3.4	3.26
Critical Field E_{Crit}	MV/cm	0.3	3.3	2.2
Electron Mobility μ_n	$cm^2/V.s$	1300	1500	950
Electron Saturation Velocity v_{sat}	$10^7 cm/s$	1.0	2.5	2.0
Thermal Conductivity λ	W/cm.K	1.5	1.3	4.9
Permittivity ε_r		11.8	9.0	9.7

To compare these power devices using their material properties, the only way is to calculate their theoretical performance. Taking into consideration that the most important characteristics in power conversion systems nowadays are: conduction efficiency (on-resistance), breakdown voltage, size, switching efficiency, and cost. [4]

Bandgap E_g

The bandgap represents the minimum energy required to excite an electron up to a state in the conduction band where it can participate in conduction. So, the stronger the chemical bonds between the atoms in the lattice means the harder it is for an electron to jump from one site to the next one.

As seen from Table 2.1 the bandgap of GaN and SiC is three times more than the Si. Wide bandgap gives the semiconductor the advantage of operating at high-temperature. Because when the temperature increases, the thermal energy of the electrons in the valence increases. And at a certain temperature, their energy will be enough to let them move to the conduction band. This uncontrolled conduction must be avoided. But for WBG semiconductors, the bandgap energy is high; so, electrons need more thermal energy to move to the conduction band. Therefore, the higher

the bandgap, the higher temperature that semiconductors can operate at [27] and the lower intrinsic leakage currents [4].

Critical Field $\mathbf{E}_{Crit}$

In Table 2.1 it is observed that GaN and SiC have critical field ten times higher than Si. High bandgap means high electric field; thus, higher breakdown voltages will result in power devices because of the higher electric field. The voltage at which the device breaks down V_{BR} can be approximated with the formula [15]:

$$V_{BR} = \frac{1}{2} w_{drift} E_{crit} \tag{2.1}$$

From this equation, the breakdown voltage of a device (V_{BR}) is proportional to the width of the drift region (w_{drift}). Hence, in the case of SiC and GaN, the drift region can be ten times smaller than Si for the same breakdown voltage. As increasing electric breakdown field will increase the doping levels; therefore, device layers can be made thinner at the same breakdown voltage levels. The resulting WBG-semiconductor-based power devices are thinner than their Si-based devices and have smaller on resistances [28].

On-resistance $\mathbf{R}_{DS_{on}}$

One of the main characteristics of power devices is the on-resistance of an active device which defines conduction losses during on-state operation. It can be calculated using this formula [14]:

$$R_{on} = \frac{4.V_{BR}^2}{\epsilon_s.\mu_n.E_{crit}^3} \tag{2.2}$$

where:

V_{BR} = Break down voltage
E_{crit} = Electric field
ϵ_s = Permittivity
μ_n = Electron mobility

The calculation results for on-resistance are plotted in Figure 2-1 with respect to the breakdown voltage of the device.

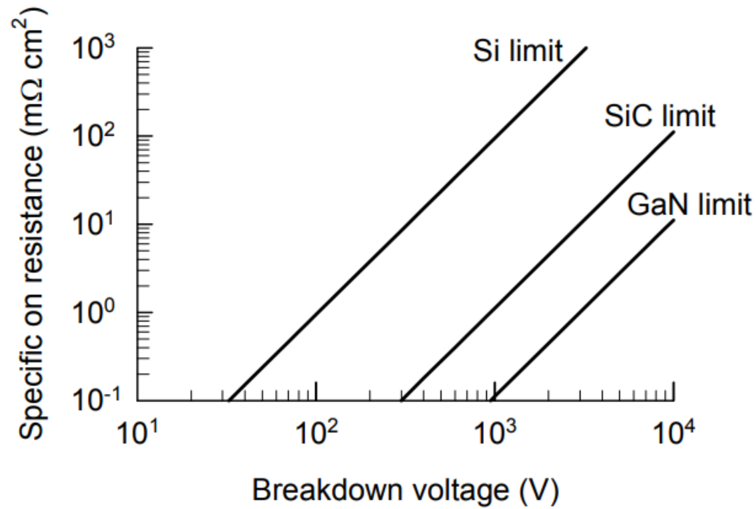


Figure 2-1: On resistance versus breakdown voltage for silicon, SiC, and GaN [2]

From Figure 2-1 it can be seen that for the same breakdown voltage, WBG devices offer a significantly smaller on-resistance, GaN devices have the smallest among all, which will reduce on-state losses and allow higher-frequency operation. That is why on-resistance is a very important parameter for power capacity and efficiency criteria.

Electron Mobility μ_n

The electron mobility of the GaN devices is higher than the Si and SiC, and this is another advantage added to the GaN devices, as electron mobility is a key parameter that affects the access resistances as seen in equation 2.2. Furthermore, larger drain currents can be achieved due to this high electron mobility which can be greater than 1A/mm. A high current density and low channel resistance are very important for high-frequency operation and power switching applications.

Electron Saturated Velocity

The drift velocity of a semiconductor material can result in the frequency switching capabilities, the higher the drift velocity the higher switching frequencies can be reached. And since SiC and GaN have more than twice the drift velocity of Si, they are expected to switch at higher frequencies.

The result of the combination of high-field and high electron velocity in GaN-

based semiconductors enable the potential to increase output power densities since high current densities and high voltages would be achieved at the same time [3].

2.1.2 Figures of Merit

In addition to the material properties, for a comparison between these devices, different figures of merit were proposed as a benchmark to evaluate the performance of the semiconductor materials for a given application, the higher number the figure of merit reaches the better the performance will be.

The most common figures of merits are Johnson's Figure of Merit (JFOM) and Baliga's Figure of Merit (BFOM). JFOM is a measure of the ultimate high-frequency capability of the material which gives an idea of suitability for high frequency and high power application, can be calculated using this equation [29]:

$$JFOM = \frac{E_c.v_{sat}}{2.\pi} \tag{2.3}$$

where E_c is the critical electric field for the breakdown in the semiconductor and v_{sat} is the saturated drift velocity.

While BFOM is a measure of the specific on-resistance of the drift region of a vertical field effect transistor, can be calculated using this equation [30]:

$$BFOM = \epsilon_r.\mu.E_g^2 \tag{2.4}$$

where μ is the electron mobility and ε_r is the dielectric constant of the semiconductor. Table 2.2 compares these figures of merit for the possible high-power and high-frequency performance of GaN relative to Si and SiC. This table shows that GaN is an excellent candidate for high-frequency power applications.

Table 2.2: Figures of merit of Si, GaN and SiC [12].

FOM	**Si**	**GaN**	**SiC**
JFOM	1	270-480	324-400
BFOM	1	17-34	6-12

2.1.3 The Two-Dimensional Electron Gas

The high electron mobility transistor (HEMT) is a field-effect transistor (FET) in which two layers of different bandgaps and polarization fields are grown upon one another. One of the main advantages of GaN-based devices such as AlGaN/GaN high electron mobility transistors (HEMTs) is the ability to form a two-dimensional electron gas (2DEG) channel at the interface of the heterostructure. This 2DEG at the hetero-junction works as the conductive channel for large drain currents due to high electron mobility and high electron sheet charge density, and it can be controlled by the gate of the device.

The main structure of crystalline gallium nitride is a hexagonal structure named "wurtzite". This structure is very chemically stable, it is mechanically robust and can withstand high temperatures without decomposition [4]. Beside this, it possesses a built-in polarization field named the spontaneous polarization (P_{SP}). This field is caused due to the ionic nature of the gallium-nitrogen bond and the lack of inversion symmetry within some planes within the crystal [31, 32].

Moreover, this crystal structure gives GaN piezoelectric properties, which means when an external electric field is applied to piezoelectric materials, they mechanically deform. Conversely, these materials generate an electric field in response to an applied mechanical stress/strain, the higher the strain, the greater the electric field. So, when growing two materials with a different lattice constant upon each other, at certain conditions the above layer will stretch or shrink so that its lattice constant matches the layer upon which it is grown. This stretch/strain will generate a polarization field named piezoelectric polarization (P_{PE}).

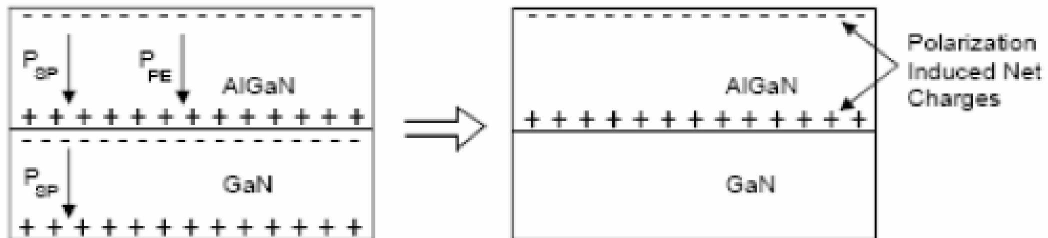


Figure 2-2: Illustration of piezoelectric and spontaneous polarization fields and sheet charges in AlGaN/GaN structure.

Thus, growing a thin layer of AlGaN on top of a GaN crystal, a strain will be created at the interface. This strain will generate a piezoelectric polarization in the AlGaN layer that has the same direction as the spontaneous polarization. So, the AlGaN layer ended up with a higher polarization field than the thick GaN layer as shown in Figure 2-2. As a result, the electric field becomes roughly discontinuous at the heterostructure interface which leads to a very high positive sheet charge density at AlGaN side. This will create a two-dimensional electron gas (2DEG) channel, which is a sheet of electrons at the GaN side of the interface [14,18]. In other words, this will give the GaN devices the ability to achieve very high conductivity compared with other semiconductor materials [4].

The polarization difference between the two materials plays an additional role in determining the band diagram. One of the semiconductors forming a heterostructure will have higher band-gap than the other (AlGaN is the high band-gap semiconductor and GaN is the smaller band-gap semiconductor). At an interface of the two semiconductors, there will be a band-gap discontinuity, the band-gap discontinuity can be separated to the conduction band offset ΔEc and the valence band offset ΔEv [33]. Check Figure 2-3(a).

The Fermi levels E_F is defined as the highest energy in a material that electron can at absolute zero temperature, which lies between the valence band and conduction band because at absolute zero temperature the electrons are all in the lowest energy state. The Fermi levels E_F of the two semiconductors do not match. This will lead

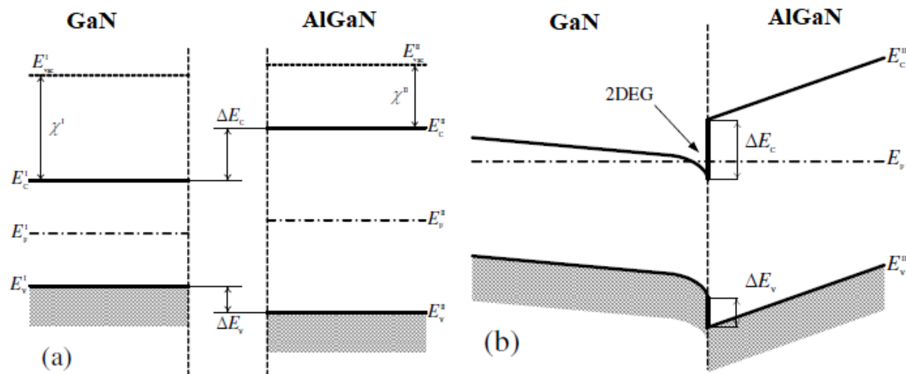


Figure 2-3: Band diagram of the AlGaN/GaN heterostructure and accumulated sheet charges in the system [3].

to a bending of the bands until the structure will have an equal Fermi level. The bandgap offset at the AlGaN/GaN interface forms a quantum well in the GaN under the AlGaN barrier layer. It will be filled with electrons diffused from AlGaN. Check Figure 2-3(b). The electrons in the quantum well form a two-dimensional electron gas (2DEG) channel. The term 2DEG refers to the condition in which electrons have quantized energy levels in one spatial directions but are free to move in both direction [3, 12, 24, 34].

This 2DEG is highly conductive because of the confinement of the electrons to a very small region at the interface. The high concentration of electrons with very high mobility is the basis for the high electron mobility transistor (HEMT).

2.2 The Basic GaN Transistor Structure

As mentioned in section 2.1.3, GaN transistors are high electron mobility transistors (HEMT) are field-effect transistors (FET). And as a FET, the basic depletion-mode GaN transistor structure consists of gate, drain and source electrodes. But unlike the MOSFET, there is no intended doping or p-n junction diode, due to the two-dimensional electron gas (2DEG) channel generated by the piezoelectric polarization at the hetero-junction between GaN and AlGaN.

The source and drain electrodes pass through the top AlGaN layer to form an ohmic contact with the 2DEG. So, a short circuit will occur between the source and

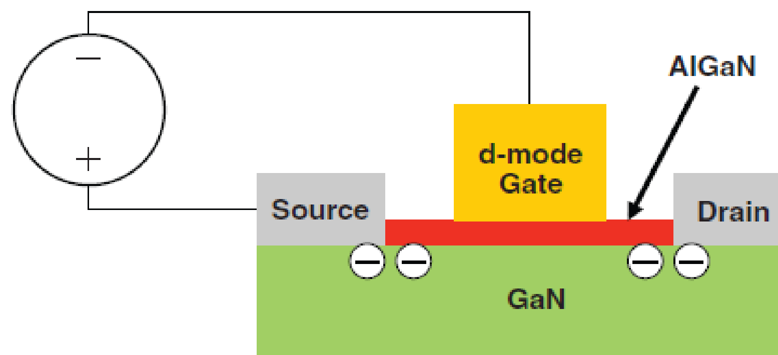


Figure 2-4: a depletion-mode (d-mode) GaN HEMT, with a negative voltage applied to the gate to deplete the electrons [4].

the drain, letting the current to conduct until the electrons in the 2DEG pool are completely depleted, in addition to that the semi-insulating GaN crystal can block the flow of current. The gate electrode is placed on top of the AlGaN layer to deplete the 2DEG. For this depletion in the 2DEG to happen, with a negative voltage relative to both drain and source must be applied to the gate, check Figure 2-4.

This is how GaN HEMT depletion mode is created which is the simplest GaN transistor structure. The drawback of this structure is a negative bias must be applied first to the devices to turn it off since this structure is normally turned on. Which means in power application this structure is not desirable as short circuits may happen [4, 5].

For this reason, other structures were designed that are turned off with zero bias on the gate (normally off), hence they will not turn on and current will not conduct until a positive voltage is applied to the gate. These are known as enhancement-mode (e-mode) devices. In this section, the main e-mode structures will be discussed.

2.2.1 Recessed Gate Enhancement-Mode Structure

This structure is created by growing a thin AlGaN layer on top of the 2DEG, as a result, the generated voltage caused by the piezoelectric field is decreased, check Figure 2-5. When the voltage generated is less than the built-in voltage of the Schottky gate metal, the 2DEG is eliminated with zero bias on the gate. While with a positive bias, electrons will get attracted to the AlGaN interface and complete the circuit between the source and the drain [35].

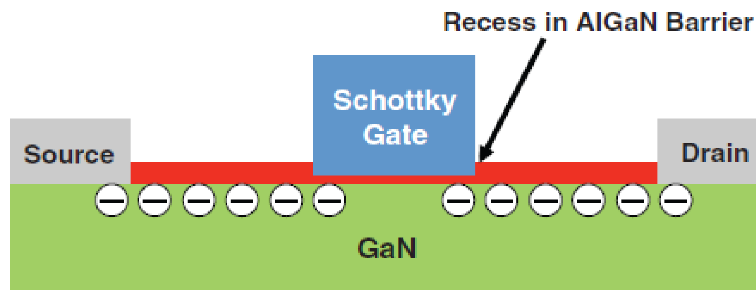


Figure 2-5: Recessed Gate Enhancement-Mode Structure [4].

2.2.2 Implanted Gate Enhancement-Mode Structure

This structure is created by implanting negative fluorine ions 19F+ in the AlGaN barrier layer as shown in Figure 2-6. The conduction band is raised in the region where fluorine is implanted, so the threshold voltage is positively shifted. When this shift is large enough, in a way that the threshold voltage reaches a positive value, these negative fixed charges will deplete the 2DEG in the channel. And then by adding a Schottky gate on top, e-mode HEMTs will be created [36, 37].

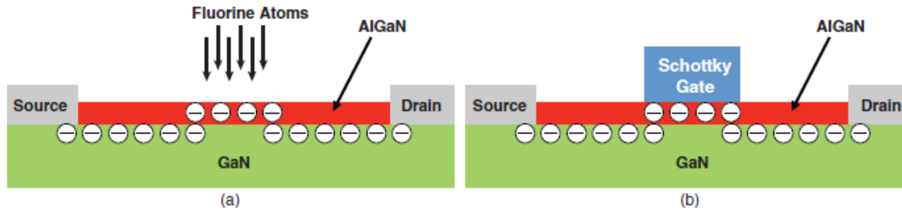


Figure 2-6: (a) Implanting fluorine atoms into the AlGaN barrier layer (b) A Schottky gate added on top [4].

2.2.3 pGaN Gate Enhancement-Mode Structure

In this structure, a pGaN layer is inserted between the gate and the AlGaN barrier. The built-in voltage in the positive charges in the pGaN layer is greater than the piezoelectric effect voltage, this will deplete the electrons in the 2DEG at zero volts on the gate and create an enhancement-mode structure [38], check Figure 2-7.

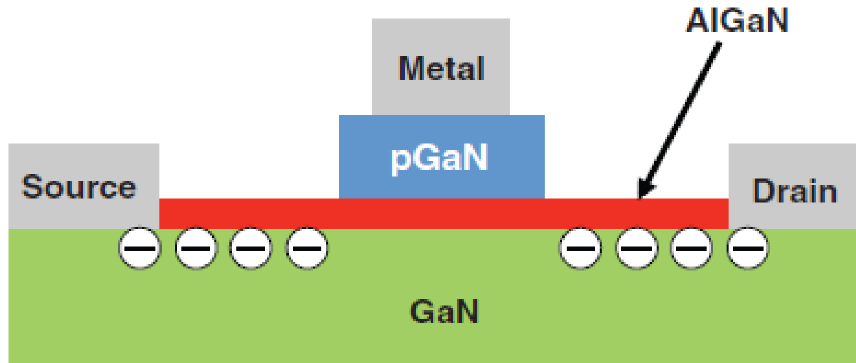


Figure 2-7: pGaN Gate Enhancement-Mode Structure [4].

2.2.4 Cascode Hybrid Enhancement-Mode Structure

Another solution to build a normally-off GaN device is by placing a low-voltage enhancement-mode Si MOSFET in series with a depletion-mode HEMT device. See Figure 2-8, the MOSFET is turned on and controlled by the positive voltage applied on the gate, and the output of the MOSFET goes to the depletion-mode GaN HEMT's gate input. When the applied voltage is close to zero volts the GaN transistor turns on. When the voltage on the MOSFET gate is removed, a negative voltage will occur between the depletion-mode GaN transistor gate and its source, which will turn the GaN device off [5].

The disadvantages of this structure are [5]:

- Cascode package parasitics are higher, even though the Si gate input is more rugged and easier to drive.
- The disability of direct control of the gate input to the depletion-mode GaN device because it is not accessible in the external cascode contacts.

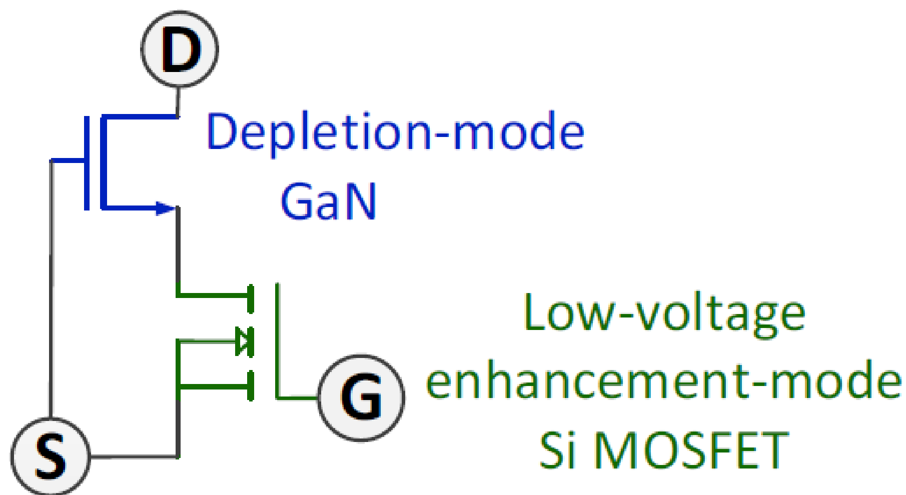


Figure 2-8: Cascode Hybrid Enhancement-Mode Structure [5]

2.3 GaN Transistor Electrical Characteristics

After studying the physical properties of GaN transistors, the important electrical characteristics to develop a power converter will be discussed based on the previous

properties. Breakdown voltage (BV_{DSS}), on-resistance ($R_{DS(on)}$), and threshold voltage ($VGS_{(th)}$) are the operating parameters that give the engineer the important information about the device to analyse and design a system. Moreover, to understand how the device behaves during switching on and off, which is the core idea of this thesis, capacitance and reverse conduction characteristics will be commented, beside the thermal characterises.

2.3.1 Breakdown voltage (BV_{DSS})

Starting with the breakdown voltage which is defined as the maximum reversed voltage that can be applied across a semiconductor before it becomes electrically conductive. The breakdown voltage between the source and the drain terminals for GaN HEMT device is affected by many factors: The critical field E_{Crit}, the design of the device, the specifics of the heterostructure, the internal insulating layers in the device structure above the gate, source, and drain electrodes, and the underlying substrate material properties [39].

Higher electric fields appear near the drain and the gate. When their field at any location of any device structure exceeds the critical field E_{Crit} the power device will break down and start conducting current.

Another factor that can cause the device to break down is the metal layers used in the device. When the device is in the blocking state, and one of these layers is connected to the source potential while another neighbouring layer is connected to drain potential, the break down will occur if the E_{Crit} of the dielectric material separating these two layers is exceeded. To avoid this, the separation between the layers can be increased or switch to an insulating layer with a higher E_{Crit} [4].

If a HEMT device suffers from breakdown, the results will be destructive. The dielectric material will face a physical rupture, in the case insulating layers exceed the critical electric field. The closer the electric field approaches to E_{Crit}, the sooner the rupture will occur [40]. Moreover, another factor that can cause the device failure, because of the excess in the GaN layer above the E_{Crit} thus a breakdown in the GaN or Al GaN regions, is the distortion of the 2DEG channel because of the generated electrons, as a result the on-resistance of the device will increase dramatically [41].

When the device is operating in the blocking state, a small current will still flow

between terminals, this current is known as the leakage current I_{DSS}, which varies with temperature. In HEMT devices it can flow from drain to the source, from drain to gate, or from drain to the substrate. The total sum of these leakage currents will be the total I_{DSS} measured between drain and source in a circuit. I_{DSS} is considered one of the serious sources of power loss in power conversion systems. Specifically, in the very low power applications, the amount of loss due to the leakage current is considered not acceptable [4].

2.3.2 On-resistance ($R_{DS(on)}$)

As it was defined in section 2.1.1, $R_{DS(on)}$ is the conduction losses during the on-state operation for an active device. Hence, it is a key variable when considering the conduction losses [42], power capacity and efficiency criteria [14].

The on-resistance of a transistor consist of the sum of all the resistance elements in the device. Check Figure 2-9, the source and drain metals should be connected to the 2DEG through the AlGaN barrier. This resistance component is called the contact resistance (R_C). Then the electrons flow in the 2DEG channel with a resistance R_{2DEG}, which can be expressed as bellow [43]:

$$R_{2DEG} = \frac{L_{2DEG}}{q.\mu_{2DEG}.N_{2DEG}.W_{2DEG}} \tag{2.5}$$

where:

L_{2DEG} = The distance the electrons have to travel
μ_{2DEG} = The mobility of the electrons
N_{2DEG} = The number of electrons created by the 2DEG
W_{2DEG} = the width of the 2DEG
q = The universal charge constant (1.6×10^{19} coulombs).

Generally, the electrons under the gate have less concentration than the region between the gate and the drain. This electron concentration depends on the type of gate, the particular process used, and the heterostructure deployed. It depends also on the voltage applied to the gate. A fully enhanced gate will have a higher electron concentration. This resistance can be approximated and calculated as [4]:

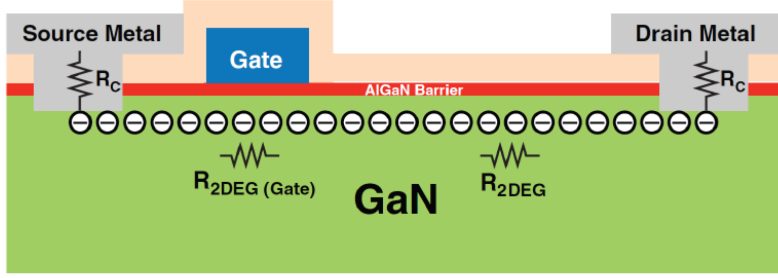


Figure 2-9: Major components of $R_{DS(on)}$ in GaN HEMT [4]

$$R_{HEMT} = 2 \times (R_C + R_{2DEG} + R_{2DEG(Gate)}) \tag{2.6}$$

The last resistance component is the parasitic resistance ($R_{parasitic}$) which is a metal resistance coming from the several metal buses that conduct the current. The conduction losses are a significant issue in power conversion systems, and that is the reason why $R_{DS(on)}$ is important. It can be expressed as:

$$R_{DS(on)} = R_{HEMT} + R_{parasitic} \tag{2.7}$$

$R_{DS(on)}$ is dependent on temperature it can increase significantly as the temperature increases, each of the $R_{DS(on)}$ components can vary with the temperature differently, based on their resistivity temperature coefficients, but mainly the temperature variation will depend on the design of the device: how much of the $R_{DS(on)}$ comes from 2DEG, contact resistance, or parasitic metal resistance [4]. Therefore for efficient power switching, GaN-based HEMTs must have low on-state resistance and ability to operate in high temperatures [3].

2.3.3 Threshold Voltage (V_{th})

The threshold voltage is the voltage at which the power device will start conducting, it is applied between the gate and the source that's why it is known as V_{GS}. In other words, it can be defined as the voltage below which the device is off as the current will be locked from conducting between the drain and the source electrodes. Threshold voltage occurs when the 2DEG channel, formed underneath the gate, got fully depleted due to the voltage generated by the gate electrode [44]. For GaN power

devices, it happens when the gate voltage got balanced with the voltage generated by the piezoelectric strain in the AlGaN/GaN barrier.

Moreover, a positive threshold voltage is needed to turn the enhancement-mode device on, while a negative voltage is required to turn on the depletion-mode device. Threshold voltage consists of two types: the first one is the voltage applied externally to the gate (defined as V_{th}) and the second one is the built-in voltage due to the material of the gate.

Since the strain in the AlGaN barrier is independent of temperature variation, as well as the voltage generated by the gate internal material, the threshold voltage in GaN devices is completely independent of temperature variation and roughly stays constant.

2.3.4 Parasitic Capacitance

Gating characterization and switching loss characterization are two major concern for the transistor application [45]. Thus the transistor capacitance is considered as an important parameter since it determines the lost energy during switching on and off. The capacitance (C) determines the amount of charge (Q) that needs to be supplied to devise terminal to change the voltage across them. The faster this charge is supplied, the faster the device will change voltage.

There are three basic elements of capacitance related to a FET, check Figure 2-10:

1. gate-to-source capacitance (C_{GS})

2. gate-to-drain capacitance (C_{GD})

3. drain-to-source capacitance (C_{DS})

The total capacitance is seen at the input terminals ($C_{ISS} = C_{GD} + C_{GS}$) which decides the gating characterization, and the total capacitance at output terminals ($C_{OSS} = C_{GD} + C_{DS}$) which decides the switching loss characterization [46]. Furthermore, the device switching speed is determined by the gate-to-source (Q_{GS}) and gate-to-drain (Q_{GD}) charges. An important ratio to determine the point at which the device might turn on due to the voltage transient applied across the drain to source is called the Miller ratio ($Q_{GS} \backslash Q_{GD}$). GaN devices switch much faster than Si devices

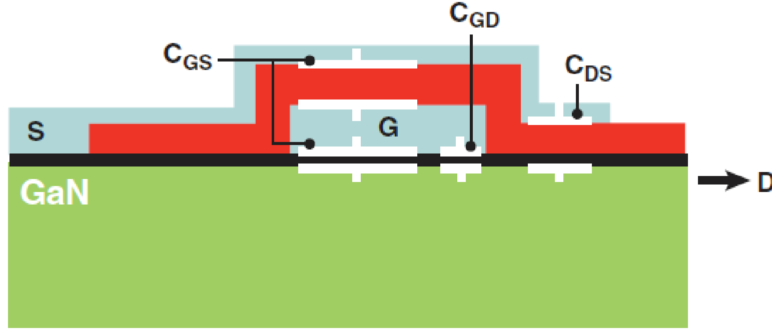


Figure 2-10: Capacitive sources in GaN Transistor [4]

with similar voltage and current ratings. The input capacitance C_{ISS} and gate charge Q_g are lower for GaN HFMTs than Si MOSFETs [28].

2.3.5 Reverse conduction

When voltage is applied from source to drain, the reverse direction of the normal forward conduction, a voltage drop V_{SD} will appear across the transistor. It is known that in the conventional Si MOSFET there is a p-n junction that creates a diode from the body of the channel to the drain of the transistor. On the other hand, e-mode GaN HEMT transistors do not have this p-n diode at all, but they do conduct in the reverse direction using a mechanism sometimes called self-commutated reverse conduction or diode-like behaviour [28]. The key to this mechanism is the symmetry of the device, as this body diode is formed by turning the 2DEG in the reverse direction. e-mode GaN transistor will conduct in reverse direction when the gate–source voltage V_{GS} exceeds its threshold, $V_{GS_{th}}$ and it will also turn on when the gate–drain voltage V_{Gd} exceeds its threshold voltage, $V_{GD_{th}}$.In the reverse-biased the gate–drain voltage will be [28]:

$$V_{GD} = V_{GS} - V_{DS}. \quad (2.8)$$

Thus, if this voltage surpasses the threshold voltage $V_{GD_{th}}$, which is similar to the specified $V_{GS_{th}}$, the e-mode GaN HEMT device channel will turn on and current will conduct in the reverse direction. And the device will have a channel resistance similar to $R_{DS(ON)}$, which can be modelled as the "body diode" but with higher

forward voltage drop and no reverse recovery charge. This resistance will vary with temperature in the same way as the $R_{DS(ON)}$ varies with temperature in forward conduction. Thus, the voltage drop V_{SD} will vary with temperature as well [4,28,42].

Q_{RR} is a charge element related to the amount of charge in a body diode is turned off, this charge is caused by the minority carriers leftover during diode conduction in Si MOSFET. This will make the Si MOSFET suffer under the hard switching mode, especially under relatively high switching frequency. while, there is no p-n diode in e-mode GaN HEMT, there will be no minority carriers. So, no reverse recovery losses in e-mode GaN devices and QRR will be zero. Because of this excellent reverse recovery, the current I_d waveform will be clean [47], and it enables the GaN-based devices to do hard-switching at a relatively high switching frequency, such as half-bridge hard switching [48] which requires hard commutation (higher efficiency and more robust without body diode).

2.3.6 Thermal resistance

It is important to understand how the device transfer heat to the surrounding environment since the consumed power in the transistor is wasted in form of heat. The main two-component elements that specify the heat transfer are junction-to-case thermal resistance ($R_{\theta JC}$) and junction-to-ambient thermal resistance ($R_{\theta JA}$). If the device is double-sided and can be cooled from the top and the bottom surfaces, a third parameter will be added which is junction-to-board ($R_{\theta JB}$). The larger the area of the transistor, the lower ($R_{\theta JC}$) resistance. The thicker the case, the longer the thermal path to the heat sink and the higher ($R_{\theta JC}$) will become [4].

The top-side thermal pad provides a path of low thermal resistance for attaching a heat sink. To improve the heat transfer, a thermal interface material (TIM) should be added between the device's thermal pad and the external heat sink. The thermal resistance through the TIM is ($R_{\theta TIM}$) and the thermal resistance from the interface with the heat sink to the ambient is ($R_{\theta HSA}$). The TIM improves the heat transfer by filling the air gap between the device and the heat sink. Heat Sink Considerations are thermal conductivity, heat sink size, weight and Heat convection path. While TIM Considerations are: thermal conductivity, contact Resistance, thickness, phase and electrical Isolation [6,49].

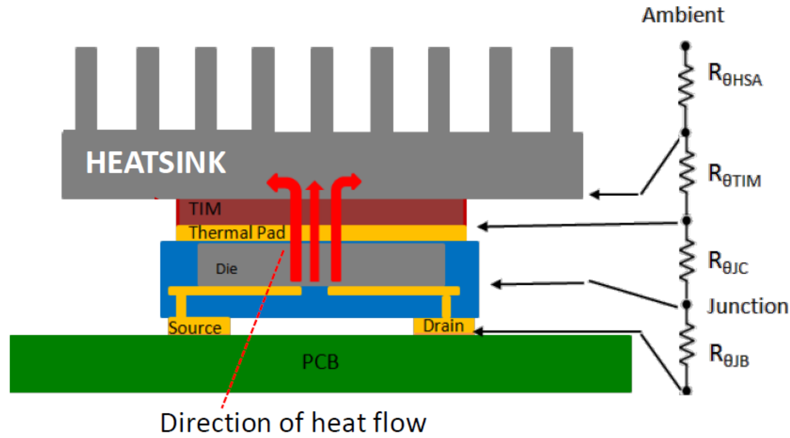


Figure 2-11: Cross-section view of GaN device and thermal dissipation path [6]

Figure 2-11, shows the thermal dissipation and all the thermal resistance elements, the sum of these three is the thermal resistance from the junction to the ambient ($R_{\theta JA}$).

$$R_{\theta JA} = R_{\theta JC} + R_{\theta JB} + R_{\theta TIM} + R_{\theta HSA} \tag{2.9}$$

2.4 Driving GaN Transistors

A great advantage of e-mode GaN HEMT devices is their switching speed. On the other hand, a layout with less parasitic capacitance, resistance, and inductance will be needed. So more considerations for the gate driver will occur. The GaN Devices are controlled by applying or removing the gate voltage from the gate electrode. Gate drive design for cascode device is identical to the Si MOSFET. However, driving e-mode devices is more complicated and needs special requirements. The main constrains of devices are [50]:

1. Low threshold gate voltage
2. Very small margin of allowed gate voltage
3. dv/dt and di/dt constraints
4. Parasitic issues
5. Layout considerations

The threshold voltage of an e-mode GaN HEMT is typically 1–2 V and the maximum gate to source voltage is normally less than 6 V but the devices can switch on with 3 to 4 Volts, resulting in a small margin. The recommended driving voltage is typically around 5 V. This only allows a few volts of ringing before spurious switching events occur, during both turn-on and turn-off transients and it may cause incident switch on when the device is working under high dv/dt applications, as a small gate voltage overshoot may destroy the device. Gate rupture is also a known issue with e-mode GaN devices [4, 50].

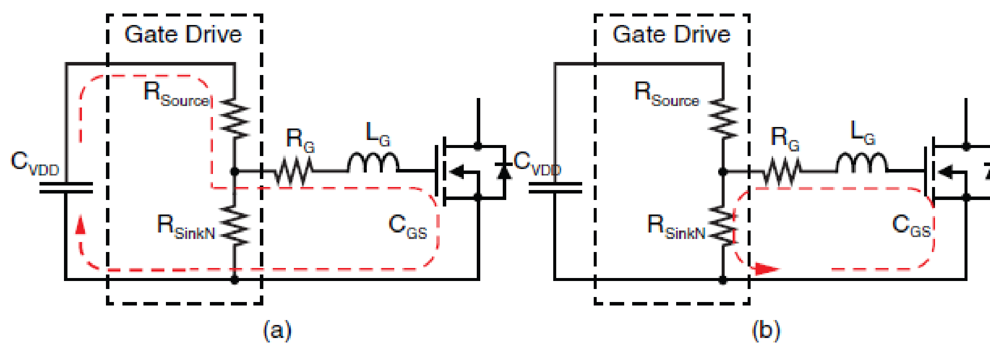


Figure 2-12: Resonant loop formed between the gate driver and eGaN FET during (a) turn-on and (b) turn-off [4]

As shown in Figure 2-12, an LCR-series resonant tank is formed by the gate driver, the transistor, the gate drive bypass capacitor (C_{VDD}), and the inductance of the interconnections between them (L_G). The equivalent resistance value includes the transistor gate resistance R_G, gate drive pull-up resistance R_{source}, the high-frequency interconnect resistance between the components, as well as the equivalent series resistance of the gate driver supply capacitor.

The gate voltage requirements can be fulfilled by critical damping of this gate drive turn-on switching power loop. To achieve this, the gate loop resistance R_G must be enlarged enough by reducing the gate loop inductance and adjusting the series gate resistance to limit overshoot. While for the gate drive voltage falling edge, there are no practical limitations. Therefore, at turn-off mode, the GaN device can drive much faster with some negative ringing [4].

As the damping requirements are different between the turn-on and turn-off of the device, the minimum gate loop resistance will have different values as well. It is

better separated the pull-up and pull-down resistance at the driver output to allow the best performance of the device, and adjust the turn-on and turn-off gate loop damping independently.

2.4.1 dv/dt Immunity & di/dt Immunity

dv/dt Immunity

As mentioned before, GaN power devices have a high voltage and current slew rates, which can influence the transistor performance. So, these conditions should be understood well.

In hard- and soft-switching applications, a very high voltage slew rate (dv/dt) on the drain can take a place in e-mode GaN device. And it is known for its quick charging of the device's capacitances. During this dv/dt event, the drain-source capacitance (C_{DS}) is charged. As well as, the gate-drain (C_{GD}) and gate-source (C_{GS}) capacitors in series are charged. A problem may occur if the charging current passing through the C_{GD} will flow through and charge C_{GS} beyond threshold voltage,

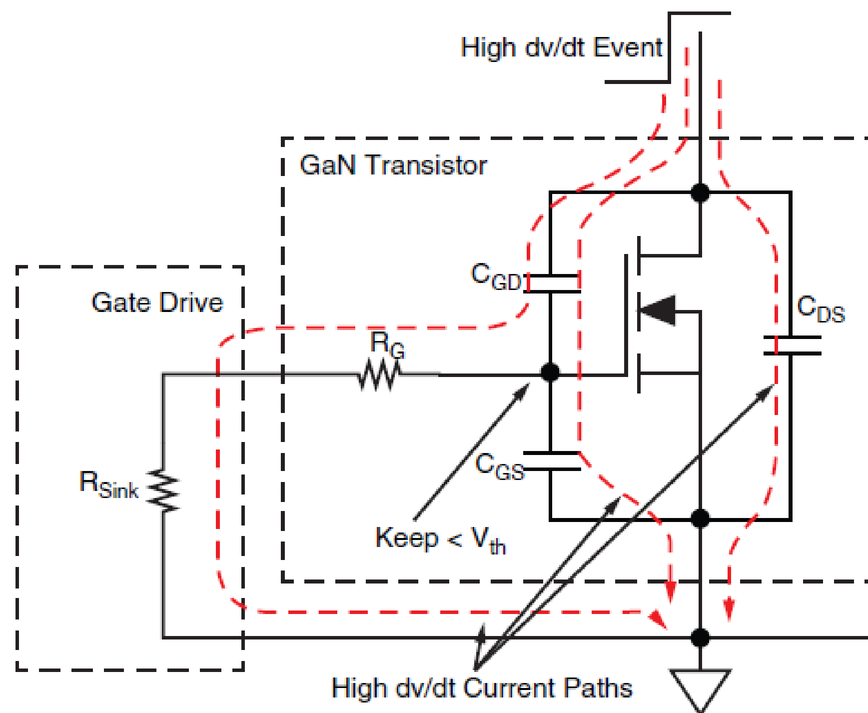


Figure 2-13: Effect of dv/dt on a device in the off state [7]

hence turn the device on. This event is known as Miller turn-on. See Figure 2-13.

This unneeded turn on can be avoided by designing a different path parallel to C_{GS}, so that the C_{GD} charging current can flow through. With this additional path that has a low pull-down resistor the charging current of C_{GD} will be transferred to the series gate resistor (R_G) to the gate driver pull-down resistor (R_{Sink}), which will allow the device to operate efficiently.

According to [51] the turn on Miller can be prevented in many ways such as using a negative gate driver, which will increase noise immunity against miller turn-on it is recommended to for this voltage to be between -2 to -3V. As a result, the turn-off loss will be reduced but the reverse conduction losses will be higher.

di/dt Immunity

A step voltage across the common-source inductance (CSI) will be induced by the rising current through the device. This common source inductance is defined as the inductance on the source side of the device that is common to both the power loop (drain-to-source current) and the gate drive loop (gate-to-source current) [4]. Check Figure 2-14.

This positive voltage step will stimulate an opposite voltage across C_{GS}. For a rising current, it causes a negative voltage to be applied to the gate with not enough damping of the off-state gate loop LCR resonant tank. This negative voltage will induce a positive ringing which may cause an unplanned turn on and shoot through.

To avoid this a sufficient damping for the gate turn-on loop is needed, but increasing the gate turn-off power loop damping through an increase in gate pull-down resistance will have a negative effect on dv/dt immunity. Thus, this solution alone may not be enough to avoid di/dt and/or dv/dt turn-on.

The other good solution is the reduce the size of the CSI by improving package design and device layout. This is done by separating the gate and power loops to be as close as possible to the GaN device and reducing the internal source inductance of the GaN device, which will remain common to both loops. Moreover, reducing CSI is also beneficial for hard-switching performance [4].

In conclusion, the gate voltages for e-mode GaN systems is lower than other devices, which will make the gate drive design more complicated and add many require-

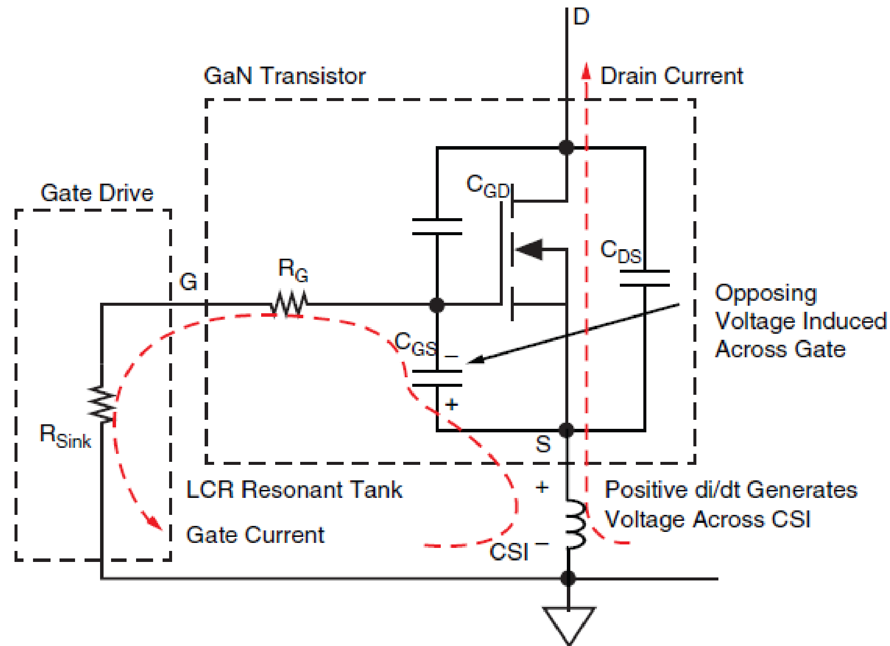


Figure 2-14: Impact of a positive di/dt of an off-state device with common-source inductance [7]

ments to the design. Driving the GaN will require separated pins for the turn-on and turn-off to get the best performance, moreover decreasing the common source loop inductance by improving the GaN system design will improve the performance in hard switching applications. Negative gate voltage can help in preventing the Miller turn-on phenomena to happen.

Chapter 3

Characterization of GaN Device

Chapter 2 showed the intrinsic material properties of the GaN devices, and due to these properties, GaN HEMT devices are showing promising results in high voltage high-frequency applications. This chapter will discuss the test that will be carried out to study the switching characteristic of the GaN device, the constraints of this test will be mention as well, besides the main design requirements to build the test.

3.1 Double Pulse Test

3.1.1 Theoretical Overview

Since the GaN devices are enabling high-frequency applications, it is important to study and understand its behaviour under these conditions. When switching frequency increases, the switch will turn on and off more times over a specific period. Knowing that switching losses are related to the change of the switch state from on to off, increasing the frequency will increase these losses. Reducing the switching losses in a power device will become essential importance of system design. Therefore, understanding the behaviour of the switch during each transition, and quantifying the losses related to these events, have become a key expectation of any power supply designer [52].

Double pulse test provides a good method for characterizing the transient performance of semiconductor transistor [46], as it allows easy evaluation of the device switching behaviour at high voltage/current without the need to run the system at

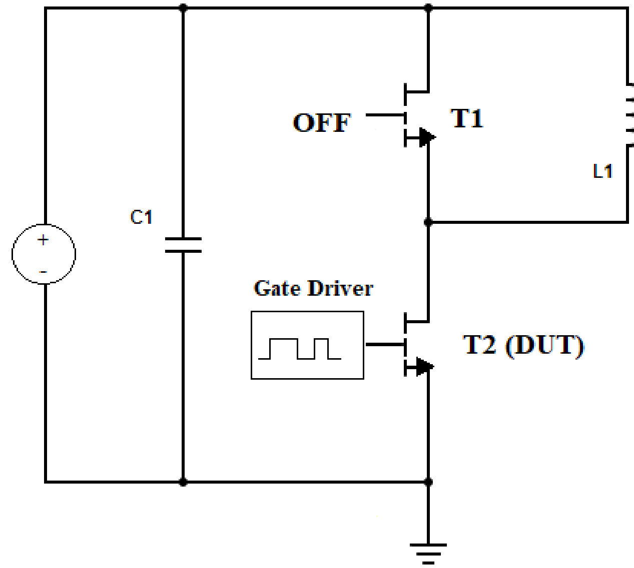


Figure 3-1: Double-pulse Test Circuit

high power ratings. Moreover, this test provides the switching loss (Eon/Eoff) measurements, and other switching characterization parameters [53]. On the other hand, the test result accuracy depends a lot on the gate loop and the power loop in the printed circuit board PCB, as well as the measurement techniques.

A double pulse test (DPT) consists of a half-bridge structure with an inductive load, a simplified schematic is shown in Figure 3-1. The main power loop in the test will start when the device under test (DUT) turns, the current will flow from the capacitors to charge the inductor and then flow through the DUT. When the DUT turns off, a freewheeling loop will occur and the inductor will circulate current through the upper transistor and force it to conduct in reverse direction. The gate drive circuit consists of the gate driver, turn-on resistor, turn-off resistor.

This test gives the possibility to test flexibly the DUT under varying voltage and current conditions. Figure 3-2 illustrates the double pulse signal. At t_0 when DUT is switched on, the inductor starts t_0 charge and current starts to increase linearly until t_1. Changing this period will allow the test current to be adjusted easily. The width is adjusted for the desired test current, the period of first pulse T_{on1} defines the switching current $I_{SW} = (V_{DS} \times T_{on1})/L$. At t_1 DUT will turn off, there will be a delay between first and second pulse, this delay should be long enough for the voltage and

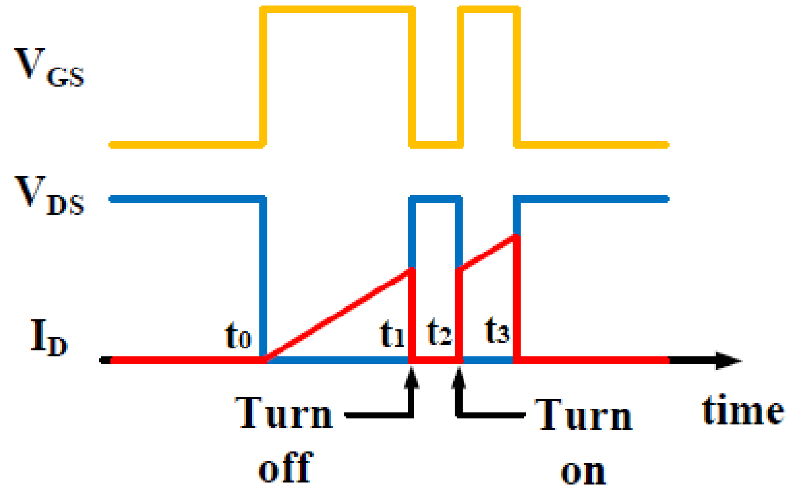


Figure 3-2: Double-pulse Test Signals [8]

current to reach the steady-state and might be changed during the test to ensure that the waveforms are settled out. Between this period (t_1-t_2) the freewheeling period will start and the inductor current I_L will force T_1 to conduct in reverse direction. This transition is used to measure the device turn-off characteristics [54].

At the beginning of the second pulse at t_2 the DUT will turn on, keeping in mind that the inductor current still at the same level, and the current will move from the free wheeling circuit to flow again in DUT. This transition is used to measure the device turn-on characteristics. Since the test is done with two short pulses the DUT junction temperature will stay almost constant during the test.

The double pulse signal can be generated using a programmable signal generator or microcontroller/DSP board. As this test involves high switching stress and high current, it is preferred to do the double pulse test one time by setting the gate signal on single trigger mode or use long repetition period (for example 50-100ms) to avoid stress on the switches. The upper transistor T_1 can be kept turned off during the whole test.

In conclusion, the t_1 (turn-off) and t_2 (turn-on) points are the intervals of interest of the test as they are the hard switching transients for the half-bridge circuit when DUT is under high switching stress.

3.1.2 Test Constraints

As mentioned before the test result accuracy might be affected so much by the gate loop and the power loop printed circuit board (PCB). Increasing the switching frequency will let the parasitic inductances, resulting from PCB of the evaluation platform layout and device package, to influence the switching performance by creating overshoots and ringing, and they may oscillate with parasitic capacitances of the device [55]. All of this will affect the gate drive stability, high ringing may cause a false turn-on event, also cause damage to the device. The undesired voltage spikes can potentially exceed the device's voltage ratings and can have a huge impact on the safe operation of fast switching devices [56].

There are many reasons of ringing that should be considered while designing the GaN device package, the power loop circuit and the gate loop, these reasons can be: The common-source inductance L_{cs} may couple the high di/dt from the power loop into the lower voltage gate loop. The voltage drop across L_{cs} will reduce the applied gate voltage during turn-on event and will increase it during the turn-off event, as a result switching transients will be slowed down and the switching losses will get worse. Gate loop inductance may cause an over/ undershoot and ringing, as well as it may turn on the miller effect. Drain-to-gate coupling capacitance can cause some noise. The effect of the power loop inductances such as L_{drain} and L_{source} will appear as drain voltage overshoot and current/voltage ringing [28, 48, 51].

To reduce the parasitic element effects care must be taken in designing the gate and power loop of the device, like power loop inductances effect can be reduced by minimising the power loop length and placing decoupling capacitors. While for gate loop inductance it is recommended to minimize the gate drive loop area and length by placing the gate driver as close as possible to the gate electrode, selecting the right gate resistance will tune the turn-on slew rate as well. Reducing the common source inductance can be done by using the kelvin source connection [48, 51].

3.1.3 Measurements Techniques

GaN E-HEMTs have a short delay, a fast switching speed and higher frequencies than Si. The high dv/dt or di/dt variation made the measurements during the switch

transitions a challenge [55]. Conventional measurement equipment does not have the ability any longer to measure these high-frequency signals, due to their limited bandwidth and dynamic frequency response limitations. Moreover, the interface between the high dv/dt or di/dt signals and the measurements equipment (oscilloscopes and probes) may add some deviations. Hence, accurate measurements are becoming more difficult as frequency is being pushed higher [57]. To determine the switching power characteristics and losses of the power switches accurately, high-performance voltage and current measurement equipment must be used.

In this section, an overview of proper voltage measurement technique is presented for obtaining test results that accurately reflect the performance of GaN devices. The voltage measurements are required to study the switching characterization of a power switch at the gate-source voltage V_{gs} and the drain-source voltage V_{ds}.

Since GaN HEMT devices are significantly fast switches, they require an increase in the bandwidth of the measurement equipment used. To get acceptable accurate results in fall/rise time measurements, the bandwidth of the measurements system (Oscilloscope and probe) must be from 3 to 5 higher than the maximum frequency of the measured signal [58].

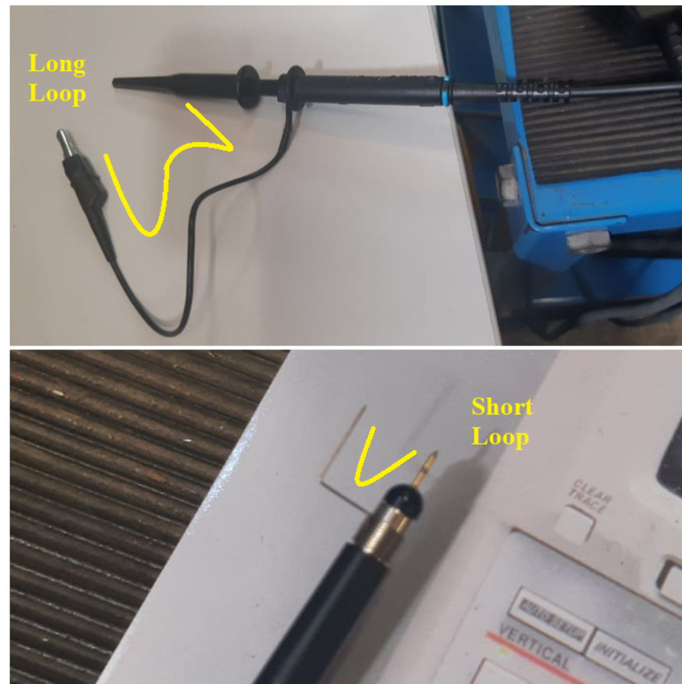
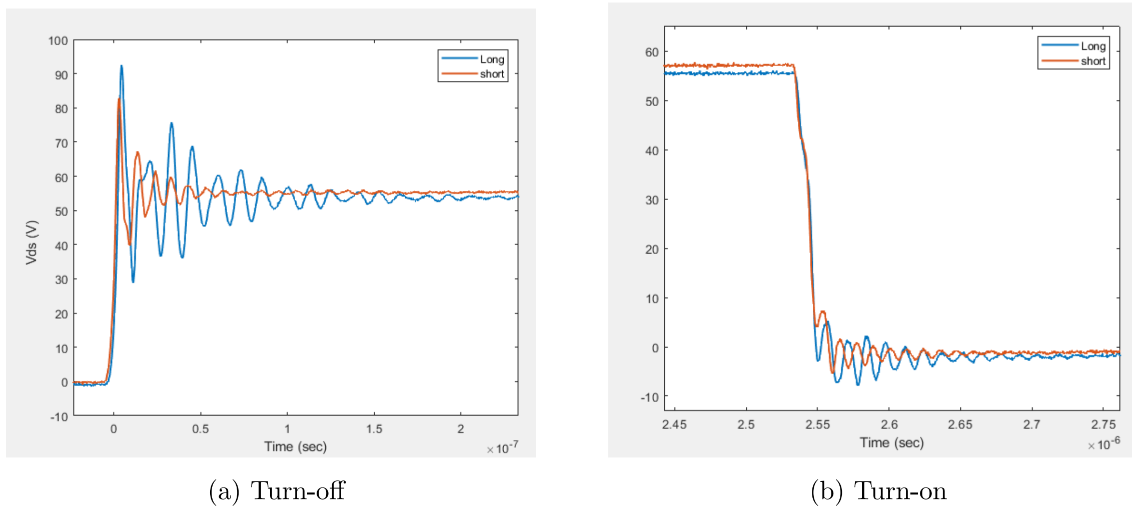


Figure 3-3: Different Probe for Voltage Measurements

Other than choosing the right oscilloscope, care must be taken when choosing the probe to measure the voltage as the parasitic elements introduced by these probes can overshadow the GaN device parameters and lead to incorrect measurement results. Figure 3-3 shows different options of probes, one with short ground loop and the other with a long ground loop.

The long ground wire will insert unwanted parasitic inductance into the probe measurement path. Consequently, overshoot and ringing associated with the rising and falling edges of the signals will result due to this unwanted parasitic. For GaN E-HEMTs it is significantly essential to minimize the length of the ground loop, as their fast rise/fall times can get affected by the probe's ground inductance, which will lead to incorrect analyses of the device switching characteristics. So, for accurate measurement results, use a scope probe with the shortest ground clip [59]. Furthermore, it is so important to place the probe as close to the required measurement point as possible, to have more accurate results.

Figure 3-4 represents the differences between using the long ground loop of the probe and the short one to measure the measure V_{ds} under a double pulse test with 50 VDC and 30 Amps. As seen from the figure, the unwanted inductance that the long loop probe had inserted to the circuit gave incorrect and inaccurate voltage measurements, as it had induced higher overshoot in the turn-on event. The long



(a) Turn-off

(b) Turn-on

Figure 3-4: Difference in using the long loop probe and the short loop one to measure V_{ds}

loop probe signal had more ringing than the short loop probe signal in both events (turn-on and turn-off), and took more time to reach the steady-state. These erroneous measurement results (Using the long loop probe) gave an inaccurate determination of the switching losses. So, characterizing the fast switching GaN E-HEMTs accurately needs attention to test methodologies.

3.2 Design Requirements

In this section, the main parts of the double pulse setup that will be used in this work will be discussed. The features of the used experimental kit and the GaN device will be explained briefly, in addition to other important requirements.

3.2.1 Experimental Evaluation Kit

The high power insulated metal substrate (IMS) evaluation platform (from GaN Systems) and its corresponding motherboard GSP65HB-EVB was used to carry out the double pulse test. This IMS evaluation platform provides a low-cost solution to transfer heat, increase the power density and cut off the system cost. Which is known as Metal Core/Aluminum PCB and it is used to cool down the GaN Systems' bottom-side cooled transistors. Many application used this platform successfully, such as Automotive applications(3.3kW-22kW onboard charger, DC/DC), photovoltaic inverters and energy storage systems [9].

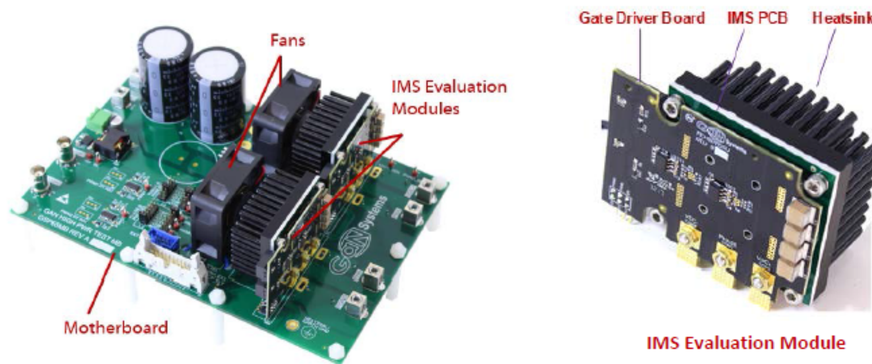


Figure 3-5: Experimental Evaluation Kit: GSP65RxxHB evaluation motherboard and 650V high power insulated metal substrate (IMS) evaluation modules [9]

Figure 3-5 shows the IMS evaluation board and its corresponding motherboard, this high-power motherboard is offered by GaN systems it is used to evaluate the IMS evaluation module in any half or full-bridge topology. The IMS evaluation module is designed with the newest and highest power E-HEMT from GaN Systems. The GS66516B is a bottom-side cooled E-HEMT, rated at 650V/25mΩ, it will be discussed in details later. With this platform, it is possible to evaluate the e-mode GaN HEMT in high-power and high-efficiency applications.

The IMS evaluation module is a two-board assembly consists of GaN E-HEMTs, gate drivers, isolated DC/DC supply, DC bus decoupling capacitors and a heatsink to form a fully functional half-bridge power stage. The IMS board is populated with the GaN E-HEMTs. While a gate driver board was designed to be so close to the IMS board. It provides the gate drivers for the half-bridge GaN E-HEMTs and DC link decoupling capacitors. It allows the IMS board to be mounted vertically for high power density design.

The functional block diagram of the IMC evaluation board is illustrated in Figure 3-6. The three power pins are CON1: VDC+, Input DC Bus voltage, CON2: Phase,

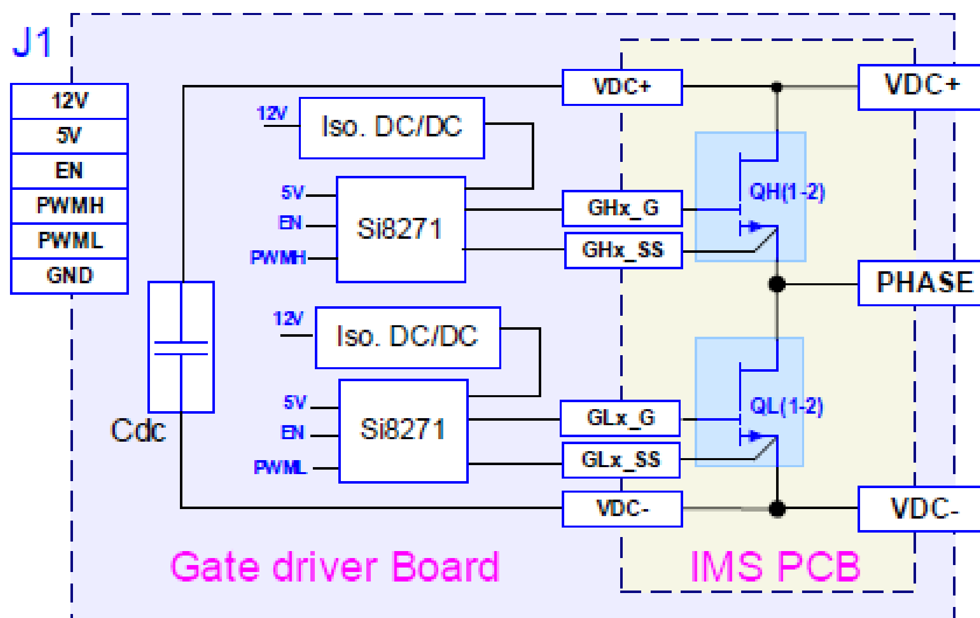


Figure 3-6: GSP65RxxHB-EVB Functional Block Diagram [9]

Switching node/phase output, CON3: VDC- Input DC bus voltage ground return. Notice that control ground GND on J1 is isolated from VDC- on CON3. The 12V PIN in the control pins side feeds the input of two isolated DC/DC (12V-9V) to generate isolated +6/-3V gate drive bias, by using a 6V Zener diode. While the 5V pin is used to power the gate driver IC.

The gate driver used in this evaluation platform is Si8271 from Silicon Labs, this driver is ideal for driving power switches, it is used in a wide variety of power supply, inverter, and motor control applications. This driver comes with a separate pull up and pull down outputs for slew rate control. An external gate resistor is used to control the switching speed and slew rate. Low turn-off gate resistance 1Ω. While The turn-on gate resistor is 10Ω. The DC coupling capacitors are mounted on the on multi-layer gate driver board, they are designed to create a balanced and low inductance power loop path for high-frequency current across the half bridge.

The motherboard (GSP65MB-EVB) has the fans to cool the IMS evaluation board, the DC link capacitors, and the inputs for the PWM signals, this mother-board is power by 12V, an on-board voltage regulator will provide 5V for the IMS evaluation modules and control logic circuit, while 12V is used to power the fans. Figure 3-7 shows all the details of the evaluation board.

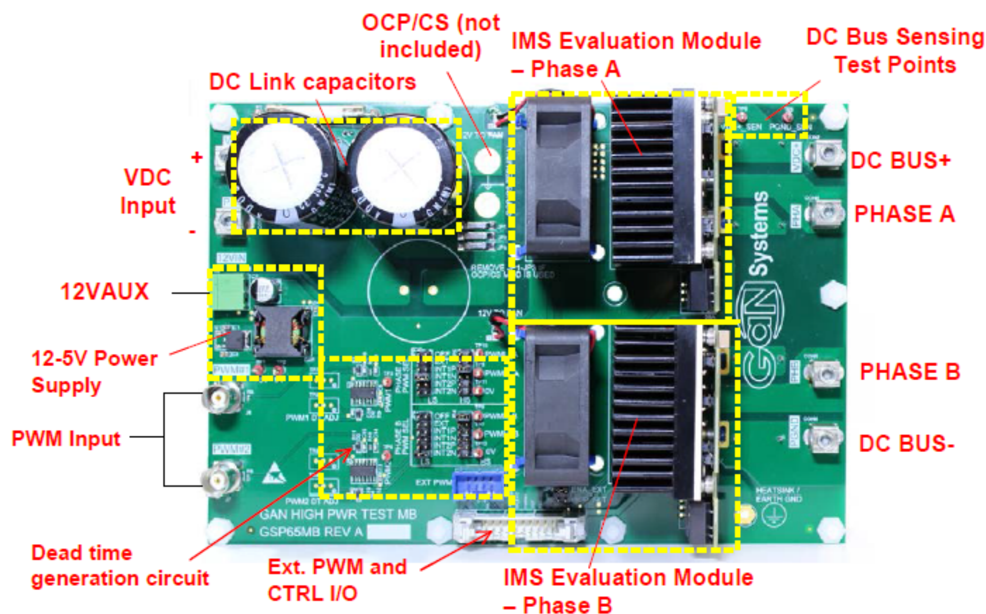


Figure 3-7: GSP65MB Evaluation Board [9]

The PWM generation can be done in two different ways, as shown in Figure 3-7. First one using PWM Inputs which can send the PWM signals to the power dower device using a signal generator source. For these pins the motherboard has an integrated circuit for the dead-time generation between transistors of the same leg, the default dead time is 100ns. The duration of the dead-times in this case is controlled by RC delay circuit, potentiometers are provided to let fine adjustment of the dead time. The second way is by using the external PWM pins, which can send the PWM signals to the power device using an external DSP.

These evaluation board can be configured into any of 12 different topologies, architectures and operating modes. This board allows the voltage measurements of V_{GS} and V_{DS}, but unfortunately, it does not have any access to allow measuring the switch current.

3.2.2 E-mode GS66516B GaN Transistor

As commented before the IMS evaluation module is populated with the newest and highest power E-HEMT from GaN Systems, Figure 3-8. The GS66516B is an enhancement-mode gallium nitride (GaN) on silicon power transistor bottom side cooled, rated at 650V/25mΩ. The properties of GaN allow for high current, high voltage breakdown and high switching frequency [10]. The transistor's SMD package has the following features [9]:

- Dual symmetrical gate and source sense (kelvin source) for flexible PCB layout and paralleling.
- Large power source/thermal pad for improved thermal dissipation.

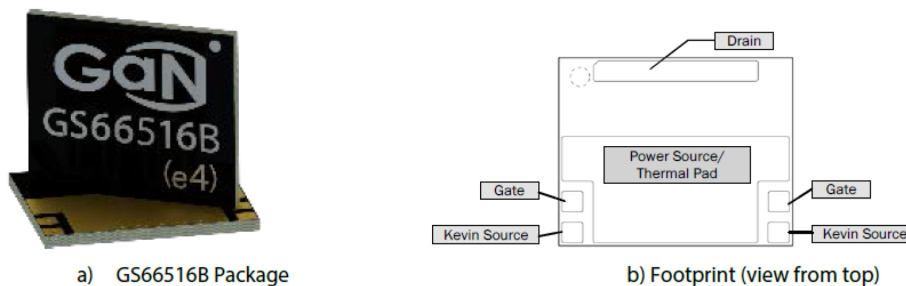


Figure 3-8: GS66516B GaNPX® SMD Package [10]

- Bottom-side cooled packaging for conventional PCB or advanced IMS/Cu inlay thermal design.

- Ultra-low inductance for high-frequency switching.

The properties of GaN allow for high current, high voltage breakdown and high switching frequency. These features combine to provide very high-efficiency power switching. Table 3.1 shows the main features of the GS66516B transistor, as e-mode GaN HEMT device, it has fast and controllable fall and rise times, the capability of conducting current in reverse direction and zero reverse recovery loss.

Table 3.1: Features of GS66516B Transistor [10]

Parameter	**Value**
Rated Voltage [V]	650
Rated current $I_{DS(max)}$ [A]	60
$R_{DS(ON)}$ [mΩ]	25
Transient tolerant gate drive [V]	-20/10
Switching freq [MHz]	$>$ 100
Small PCB footprint [mm^2]	11×9

As observed from the table the transistor has a very small PCB footprint thanks to GaNPX® packaging design, which enables low inductance and low thermal resistance in a small package. The GS66516B is a bottom-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high-efficiency power switching [10]. Packaging design is very important for the device performance, as package parasitics, such as drain parasitic inductance, source parasitic inductance, and gate inductance, can worsen the ringing that occurs during and after the switching transient, which will limit the switching speed and may cause damage to the device [28].

This transistor can be used in many applications, such as high-efficiency power conversion, high-density power conversion, AC/DC converters, synchronous buck or boost converters, half-bridge topologies, industrial motor drives, DC-DC converters, solar and wind power, fast battery charging, traction drives, etc.

Gate Drive

For optimal $R_{DS(ON)}$ and long life, it is recommended to use gate drive voltage from 0V to +6V. The maximum gate to source voltage rating is +7V, the gate drive can tolerate transients up to +10 V and – 20 V for pulses up to 1 µs. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) gets fully enhanced and reaches its optimal efficiency point. GaN Systems E-HEMT does not require negative gate bias to turn off, but as commented in Chapter 2, negative gate bias improves the voltage spike on the gate and ensures the safe operation, however it increases the reverse conduction loss.

Blocking Voltage

The blocking voltage rating BV_{DS} is defined by the drain leakage current. The hard breakdown voltage is approximately 30% higher than the rated BV_{DS}. The maximum drain-to-source rating is 650V and does not vary with negative gate voltage. A transient drain-to-source voltage of 750V for 1 µs is acceptable.

Source Sensing

The GS66516B has two dedicated source sense pads. The used package utilizes no wire bonds so the source connection is very low inductance. The source sense pin will improve the performance of the device by reducing the value of the common source inductance, by creating a gate drive signal kelvin connection. This can be achieved by connecting the gate drive signal from the driver to the gate pad on the GS66516B and returning from the source sense pad on the GS66516B to the driver ground reference.

Reverse Conduction

Because of the material properties, GaN Systems enhancement-mode HEMTs are capable of reverse conduction without the need for the body diode, thus zero reverse recovery charge. Figure 3-9 depicts the GS66516B Reverse Conduction Characteristics.

On-state conduction (V_{GS} = +6V): The reverse conduction characteristics in on-state is similar to that of the Si MOSFET, with the I-V curve symmetrical about the

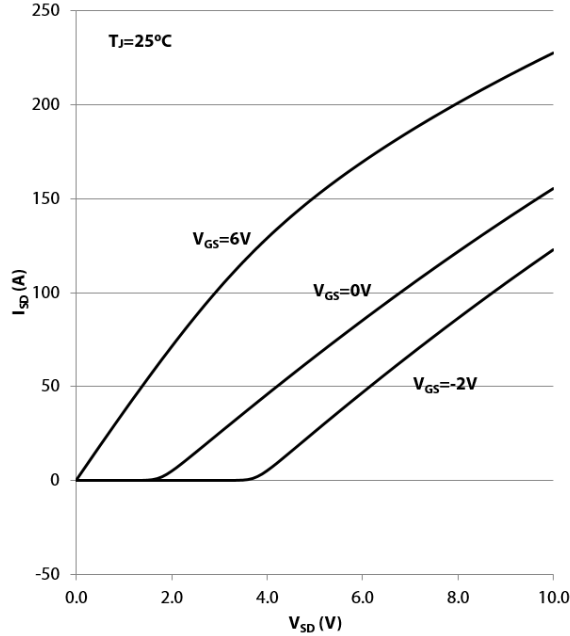


Figure 3-9: GS66516B Reverse Conduction Characteristics: Typical I_{SD} vs. V_{SD} [10]

origin, providing a similar $_{DS(on)}$ than the forward conduction operation.

Off-state condition ($V_{GS} \leq 0$V): The reverse conduction characteristics in the off-state are different from silicon MOSFETs because the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, V_{GD}, exceeds the gate threshold voltage. At this point, the device exhibits a channel resistance. This condition can be modelled as a "body diode" with a bit higher V_F and no reverse recovery charge.

To use the negative gate voltage in the off-state, the source-drain voltage must be higher than $V_{GS(th)}$+$V_{GS(off)}$ to turn the device on. Therefore, the reverse conduction loss will increase, as a result of the negative gate voltage that will add to the reverse voltage drop V_F.

3.2.3 Other Requirements

The Delfino F28379D controlCARD (TMDSCNCD28379D) from Texas Instruments (TI) will be used to send the DPT signal, and it can be used to send PWMs and control the power devices. This 180-pin controlCARD is intended to provide a

well-filtered robust design that is capable of working in most environments.

The oscilloscope HDO6104A-MS provided by Teledyne LeCroy, is a good choice to measure the voltages and inductor current. It allows to capture and display the signals with 16 times more resolution than other oscilloscopes. Waveforms captured and displayed are cleaner and crisper. Signal details often lost in the noise on other oscilloscopes are visible and easy to distinguish.

Main key features of HDO6104A-MS:

- 4 input channels
- 16 digital channels (with –MS models)
- 12-bit ADC resolution, up to 15 bits with enhanced resolution
- Up to 10 GS/s with Enhanced Sample Rate
- 1 GHz bandwidths

Chapter 4

Design and Implementation

In this chapter, the first part is a simulation design of a half-bridge double pulse test circuit was simulated in LTSpiceis to evaluate switching of GaN E-mode HEMT performance under different conditions. The second part is the implementation of the test setup, a printed board circuit (PCB) was designed as an interface between the evaluation platform and the micro-control, this design was made to control the platform in all possible configuration high/low power and full bridge and half-bridge. The DPT signal was generated by Texas Instruments (TI) Microcontroller F28379D controlCARD using the integrated development environment software Code Composer Studio that supports TI's Microcontroller.

4.1 Simulation Design

GaN Systems provides Pspice/ LTSpice simulation models for GaN E-mode HEMT as a development aid tool to evaluate the device performance and to ensure first-pass design success [60]. The model describes the characteristics of typical devices, but it does not represent all of the specifications and operating characteristics of the semiconductor product to which the model relates, and they cannot exact the device performance under all conditions. However, it is a good tool to start and get familiar with the GaN devices switching characteristics.

4.1.1 LTspice Model

GaN systems provides three different levels of models for GaN E-HEMT transistors. The first level focus on simulation speed, it allows general electrical simulations on application/converter level circuits. The second one is similar to the first but includes a thermal model. Self-heating temperature rise is also taken into account. While the third one has an added feature, which is including the package stray inductance. The model structure and symbol are shown in Figure 4-1. The Tc terminal is (case temperature) and Tj terminal is (junction temperature). The model is calibrated to include the temperature dependence of the saturation current and drain-to-source resistance. The connection for the thermal network should be separated from the electrical one.

Figure 4-1: Structure and Symbol of the 3-level of GaN systems LTspice model [11]

4.1.2 Double Pulse Test File

GaN systems provides an LTSpice® simulation file of a half-bridge double pulse test circuit which is used as the test bench to evaluate switching performance under different electrical parameters, it can be found in [61]. The power electronics software PSIM® has the same file as well using the LTSpice model and this is possible due to the interface connection between the two softwares. The results of both softwares were compared, and they were the same. In the end, LTspice software was chosen to do all the tests and to compare its results with the experimental lab results. The circuit is shown in Figure 4-2.

Some of the test parameters were modified to match with the evaluation board used in the experimental part. The junction temperature at which the tests were performed was assumed to be 30°C; as in the experimental tests, the environmental

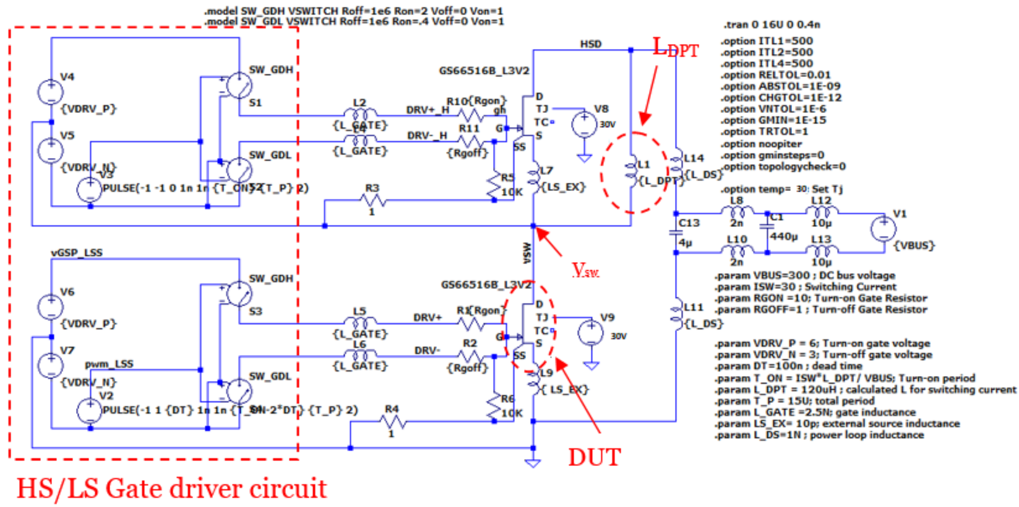


Figure 4-2: Half-Bridge Double Pulse Test bench circuit in LTSpice

temperature was about 30°C and due to the very fast nature of the tests and to the cooling system, it is expected that the junction temperature did not increase too much beyond the room temperature. In addition to the test parameters, parasitic inductances can be found in the file, for their important role in affecting the device switching behaviour and to make the simulation results as realistic as possible. These

Table 4.1: The Simulation Parameters

	Parameter		Value
	V_{Bus}	[V]	50-400
	I_{SW}	[A]	5-30
Switching parameters	L_{DPT}	[μH]	120
	R_{Gon}	[Ω]	10
	R_{Goff}	[Ω]	1
	V_G	[V]	-3/6
	L_{Gate}	[nH]	2.5
Parasitic parameters	$L_{S_{EX}}$	[pH]	10
	L_{DS}	[nH]	1

parasitic inductances were modified after doing the experimental test to match the simulation results with the lab results. The simulation parameters are described in Table 4.1.

4.2 Implementation

4.2.1 PCB Design

As explained in the previous chapters, GaN devices are very fast switches, any parasitic elements can affect their switching behaviour severely, in a way that may damage the device. So, attention should be drawn while building the setup of any topology using the IMS platform to prevent adding more parasitic elements to the system that may come from wires and create high nose signals. And since the F28379D controlCARD from Texas Instruments will be used in generating the double pulse signal and controlling any other topology, design of printed board circuit (PCB) was the best solution to interface between the DSP and the IMS board.

The DSP will be mounted directly on the PCB, so no wires between the DSP and the PCB, thus better performance and less noise. Moreover, the PCB was designed to be mounted directly in a vertical way on the evaluation platform through the external PWM and control I/O connector, check Figure 3-7.

This connector has 20 pins, part of these pins will be used in the PCB design, such as 5V pin to power the PCB, the ground pins to connect between the evaluation

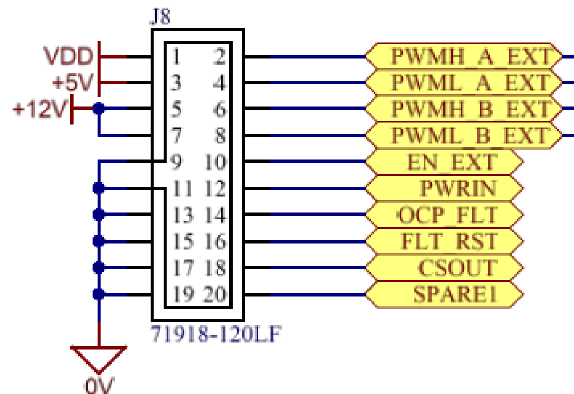


Figure 4-3: Schematic of the external PWM and control I/O connector [9]

board ground and the PCB ground, and the external PWM pins to be able to send the signals from the DSP to the gate driver. While the rest of the pins will not be connected to the PCB, pin number 10 is an enable input, logic low disables all the gate drive outputs, but it is not used and left to its default statues will is high logic. In the designed PCB there will be a switch to disable the gate drive signals. Figure 4-3 shows the schematic of the external PWM and control I/O connector, which is the connection point between the PCB and the evaluation board.

The PCB design was done using Altuim® software. As mentioned before the PCB was designed to give the ability of full control of the evaluation board switches in any possible topology. The PCB design was separated into three main parts: Voltage and current adapting stage, fault triggering and PWM signal buffering. Figure 4-4 shows a block diagram for the PCB interface with the evaluation board.

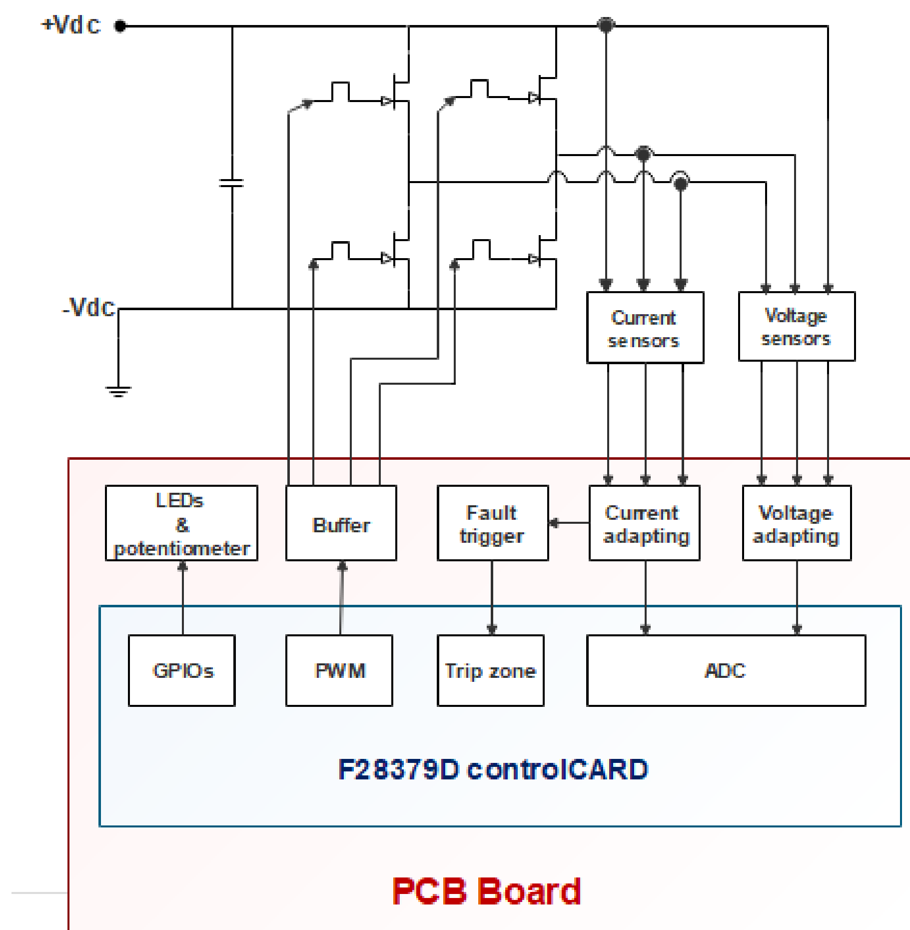
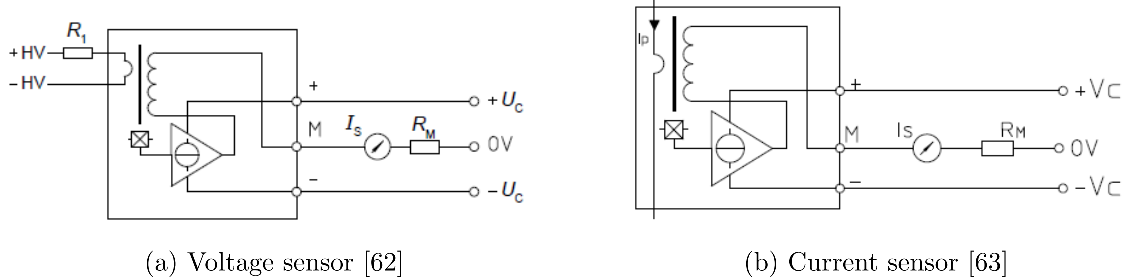


Figure 4-4: Block diagram for PCB interface with the evaluation board

Voltage and Current Adapting Stage

In this section, the adapting stage design for the measured voltages and currents will be explained clearly. The voltages and currents of Phase A (first leg), Phase B (second leg) and the DC input will be measured, these values are measured for controlling the system, they are analog signals which will be sent to the DSP through the analog to digital conversion pins (ADC). This adapting stage is needed to allow the communication and the interface between the DSP and the power stage since the ADC pins can handle a voltage range from 0V to 3V, while output from the measurement tools can exceed these limits. Before explaining the design of the adapting stage, the sensors to get the measurements values of the voltages and currents should be explained, as the output of the sensor is the signal that will enter the adapting stage.

Voltage Transducer LV 25/P [62] and Current Transducer LA 55-P/SP1m [63] are used to measure the voltage and the current, both sensors are hall effect sensors, check Figure 4-5 that explains the equivalent circuit of both sensors. The sensors are based on a current transformer which means that the output of both of them is a current, the signal that will enter the adapting stage is the voltage across the R_m, the design was made to have equal output voltage at the secondary side (1.5V) from both sensors, so in this case one adapting stage design will be required.



(a) Voltage sensor [62]

(b) Current sensor [63]

Figure 4-5: Equivalent circuit for voltage and current sensors

The voltage sensor transformer ratio is 2.5, and the circuit was designed to allow the maximum voltage input which is V_P=600V, R_1=66kΩ, and the calculation to find R_m is as below:

$$I_P = \frac{V_P}{R_1} = \frac{600}{66} = 0.009A \tag{4.1}$$

$$I_S = I_P \times 2.5 = 0.009 \times 2.5 = 0.0225A \tag{4.2}$$

$$R_m = \frac{V_S}{I_S} = \frac{1.5}{0.0225} = 66.6\Omega \tag{4.3}$$

While for the current sensor the transformer ratio is 1/2000, the circuit was designed with a maximum current equal to 50 A, and R_m for the current sensor will be calculated as below:

$$I_S = I_P \times \frac{1}{2000} = \frac{50}{2000} = 0.025A \tag{4.4}$$

$$R_m = \frac{V_S}{I_S} = \frac{1.5}{0.025} = 60\Omega \tag{4.5}$$

As mentioned before the output of these sensors will be imported to the DSP through the analog to digital pins, which can handle voltage input between 0-3 volts only. The design of the adapting stage is done using the operational amplifiers, it was designed to satisfy these conditions:

1. V_{out}=0 if V_{in}= 1.5

2. V_{out}=3 if V_{in}= -1.5

Check Figure 4-6 it shows the adapting stage design, The V_{in} is the signal coming out from the sensor, while V_{out} is the output of the adapting stage and the input to ADC pins. The amplifier is rail to rail amplifier with supply voltage from 0V to 5V, which is not that critical for DSP. The chosen voltage reference is 0.75V, and with

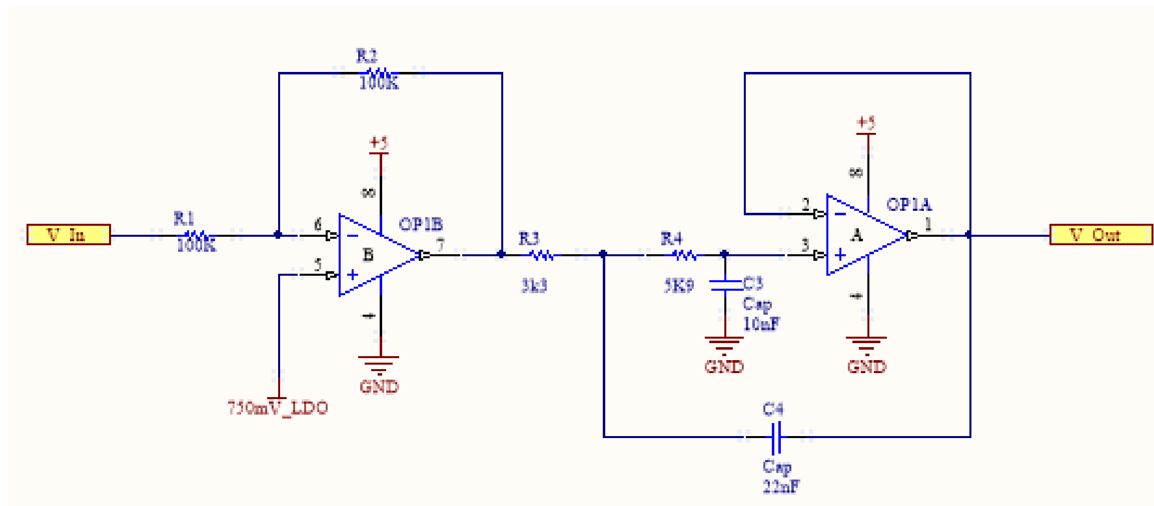


Figure 4-6: Adapting stage design

resistors values shown in Figure 4-6 we can satisfy the conditions mentioned before using Equation 4.6. The next step of adapting stage is filtering the signal using a second-order filter to filter the signal from the noise before it goes to the DSP. The V_{in} is the signal coming out from the sensor it is assumed here to be a sinusoidal wave to make sure that the adapting stages are correct for all point.

$$\begin{aligned} V_{out} &= 0.75 \times (1 + \frac{R_1}{R_2}) - V_{in} \times \frac{R_1}{R_2} \\ &= 0.75 \times (1 + \frac{100}{100}) - V_{in} \times \frac{100}{100} \\ &= 1.5 - V_{in} \end{aligned} \tag{4.6}$$

This circuit was simulated using Tina software provided by Texas Instruments, Figure4-7 shows the input voltage signal and adapted output voltage, from the figure, it can be seen that at zero volts at the input, the output will be 1.5V, and when the input is -1.5V the output is 3V, while when input is 1.5, output is zero volts.

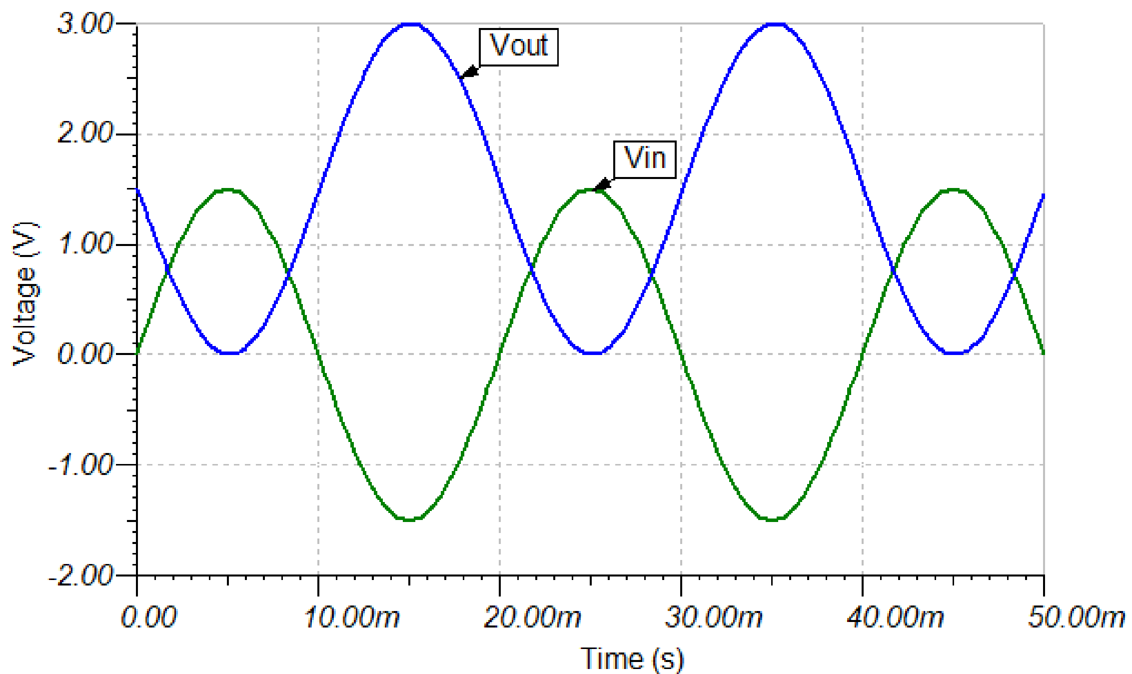


Figure 4-7: Adapting Stage Signal

Fault Signal Triggering

Unfortunately, this evaluation board does not send to the user any signal to indicate a fault state. To protect the system from any faults and high currents, a design should be implemented to notify the user that high currents are passing through the circuit and disable the gate driver, especially that the evaluation board is design to handle currents up to 30A.

Triggering the faults is done by sending a signal to the DSP through the trip zone pins, at zero volts this signal can trigger the trip zone indicating that a fault happened. And through the control algorithm, the PWM generation can be interrupted and stop commanding the gate driver and switches will open if a fault occurred. Thus the fault triggering circuit should be designed to give a zero volt when the unwanted event happens.

Since the evaluation board cannot handle currents higher than 30A, the fault circuit design will limit any current that may exceed 25A, or go below -25A to protect the evaluation board. To do so a rail to rail amplifier with 0-5V input supply will be

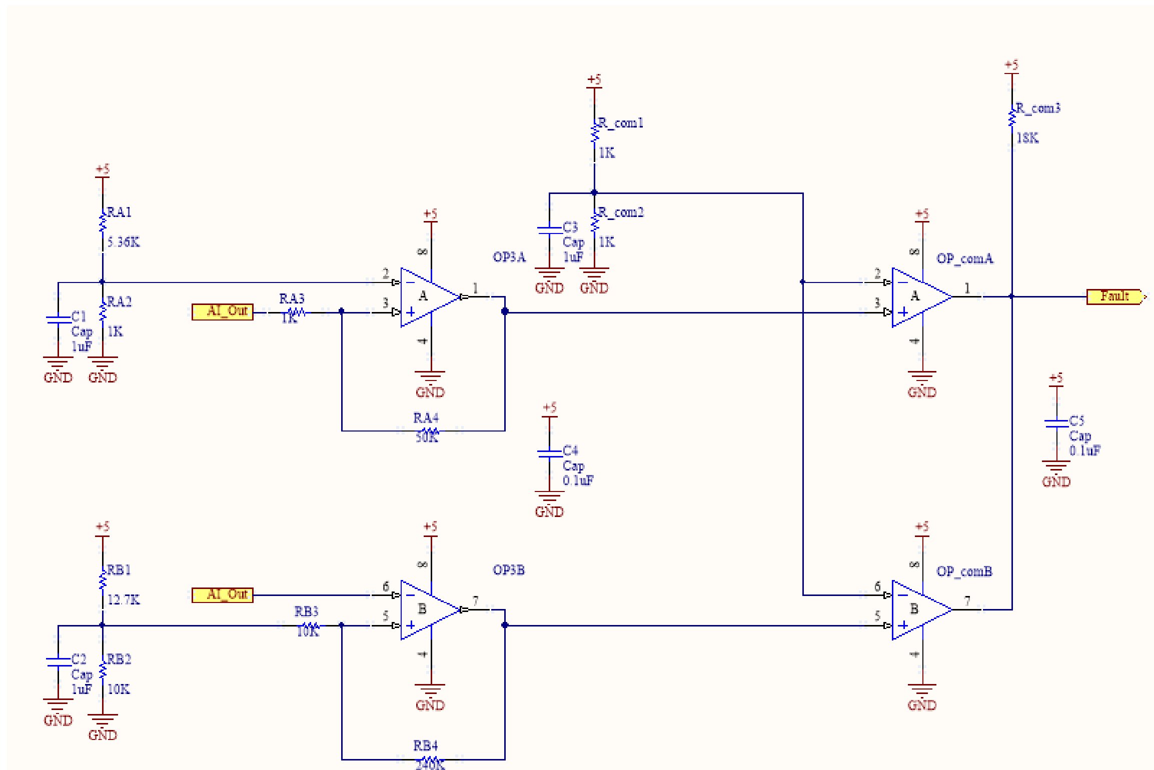


Figure 4-8: Fault Triggering Circuit Design

used to limit this range, by comparing the input signal to a reference voltage. Since noise or signal variation at the comparison threshold can cause multiple transitions, a certain tolerance introduced by hysteresis was designed to solve this problem. The concept of hysteresis is to set an upper and lower threshold to eliminate the multiple transitions caused by noise [64], more explanation and examples can be found in [64].

The schematic of the design is shown in Figure 4-8, the input signal to the fault triggering circuit is the current signal coming from the output of the adapting stage, which will pass to two different amplifiers as shown in the figure. The upper part will check if the current exceeds 25A, while the lower one will check if it goes lower than -25A.

Since the input of the fault circuit is the output of the adapting stage, 2.3V from the adapting stage will represent the -25A, while 0.7 will represent the 25A. So acceptable range of [-25A,25A] will be equivalent to 2.3V descending to 0.7V and 0.7V to 2.3V ascending at the output of adapting stage. As shown in Figure 4-9, the accepted range includes all values between the red line and the blue on, such as the highlighted example, remember here that the V_{in} is the signal coming out from the sensor, while V_{out} is the output of the adapting stage.

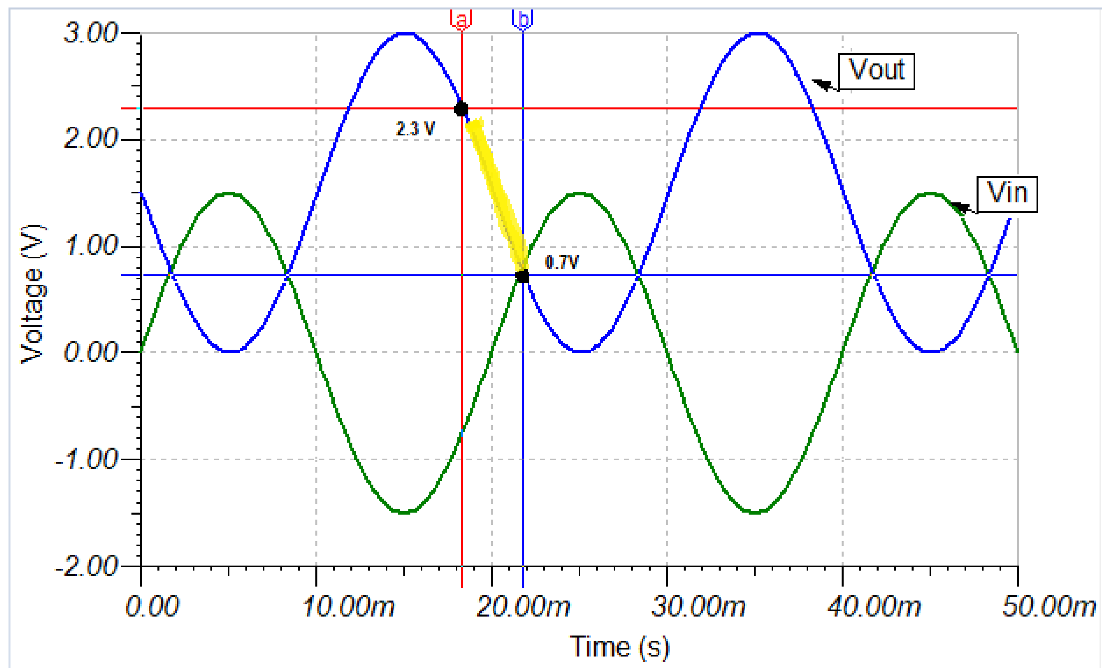


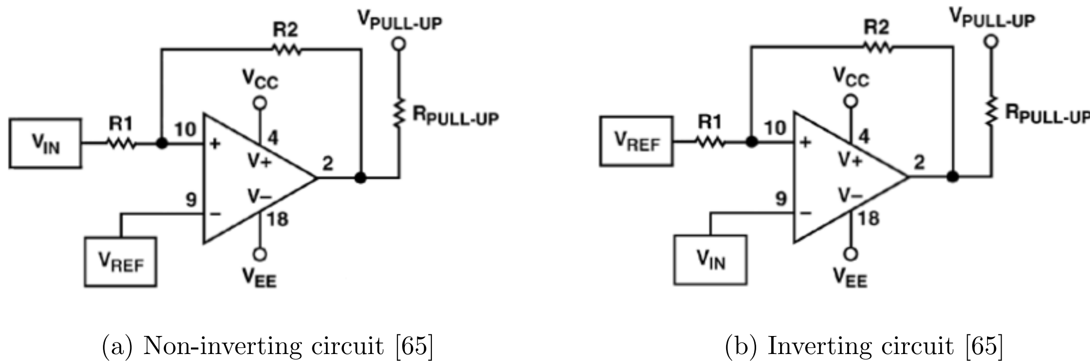
Figure 4-9: Accepted range for current signal

So in other words, there are two critical points to check these limits:

A) I< I_{max} —> V_{ADC} > V_1=0.7V

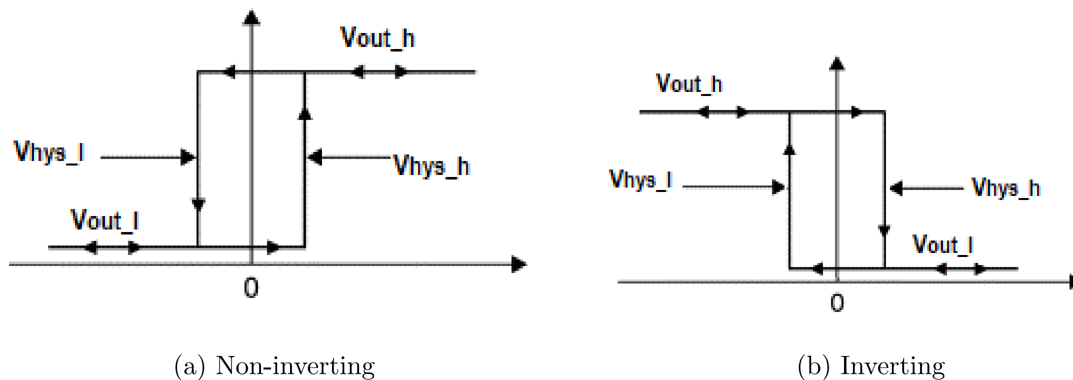
B) I> I_{min} —> V_{ADC} < V_1=2.3V

The hysteresis circuit design has two types: an inverting or noninverting configuration [65], check Figure 4-10. Both configurations will be used and combined together to get the intersection between their outputs, for case A a noninverting configuration will be used which will let the signals higher than 0.7V to pass, while case B an inverting configuration will be used, which allows signals under 2.3V to pass only. Figure 4-11 shows the transfer function for the different configurations. The output voltages in the figure are the values of the supply input for the amplifier, which is 0V and 5V in this design, while the other voltages shown in the figure are the hysteresis



(a) Non-inverting circuit [65] (b) Inverting circuit [65]

Figure 4-10: Different hysteresis configurations



(a) Non-inverting (b) Inverting

Figure 4-11: Transfer function of the different hysteresis configuration

threshold higher and lower limits to protect from multiple transitions. In case A the lower limit will be 0.7V and the higher limit 0.8V, for case B the lower limit will be 2.1V and the higher will be 2.3V.

The design for an inverting hysteresis was done using these equations [65]:

$$HYST = V_{hysh} - V_{hysl} \tag{4.7}$$

$$HYST = R_1 \times \frac{(V_{Outh} - V_{Outl})}{(R_1 + R_2)} \tag{4.8}$$

$$V_{hysl} = \frac{((R_2 \times V_{REF}) + (R_1 \times V_{Outl}))}{(R_1 + R_2)} \tag{4.9}$$

$$V_{hysh} = \frac{((R_2 \times V_{REF}) + (R_1 \times V_{Outh}))}{(R_1 + R_2)} \tag{4.10}$$

The design for a noninverting hysteresis was done using these equations [65]:

$$HYST = V_{hysh} - V_{hysl} \tag{4.11}$$

$$HYST = R_1 \times \frac{(V_{Outh} - V_{Outl})}{R_2} \tag{4.12}$$

$$V_{hysl} = \frac{(((R_1 + R_2) \times V_{REF}) + (R_1 \times V_{Outl}))}{R_2} \tag{4.13}$$

$$V_{hysh} = \frac{(((R_1 + R_2) \times V_{REF}) + (R_1 \times V_{Outh}))}{R_2} \tag{4.14}$$

To get the intersection between the two signals coming from case A and B, two comparators will be used to compare the previous signals with a voltage reference equals to 2.5V, one comparator will have noninverting configuration and the other one will have inverting one, as seen in Figure 4-8. In other words, these two comparators will do the same job as an or gate.

Figure 4-12 shows the signal output of each stage, VS1_A is the signal output from case A, as shown whenever the value of the adapting stage signal (VAI_out) is above 0.7, VS1_A will be 5 volts, and when it is less than this it will be zero. While VS1_B is the signal output of case B, which will give high voltage whenever the value of the adapting stage is less than 2.3V and it will be zero if the value is higher. And VS2 is the output signal after the intersection stage.

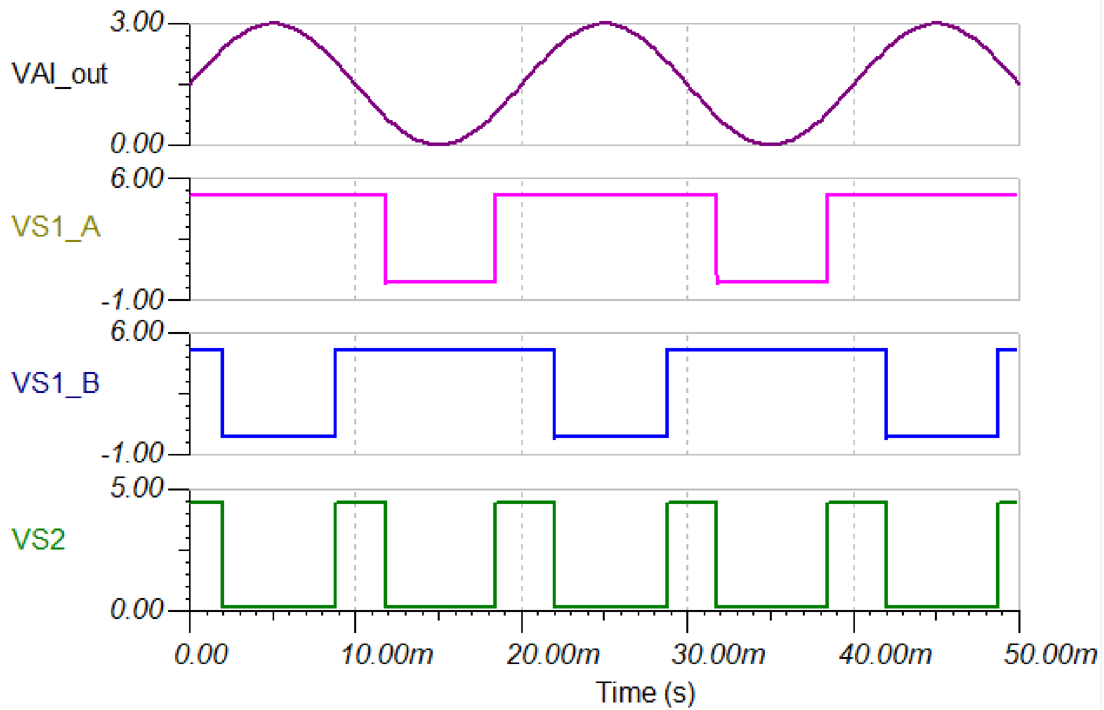


Figure 4-12: The signal output for each stage of the fault circuit design

As mentioned before, the output signal of the second stage will be sent to the DSP to trigger the trip zone, but the DSP trip zone pins cannot handle 5V, thus 5V must be adjusted to be 3.3V. To do so, the fault signal after the intersection stage (VS2) will be connected to the base of an NPN transistor, as shown in Figure 4-13, the collector is connected to 3.3V and the emitter output will be sent to the trip zone.

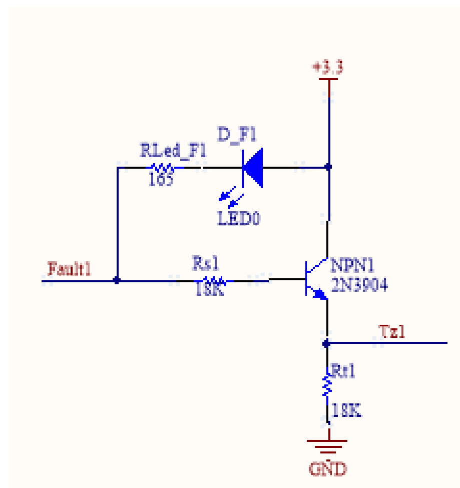


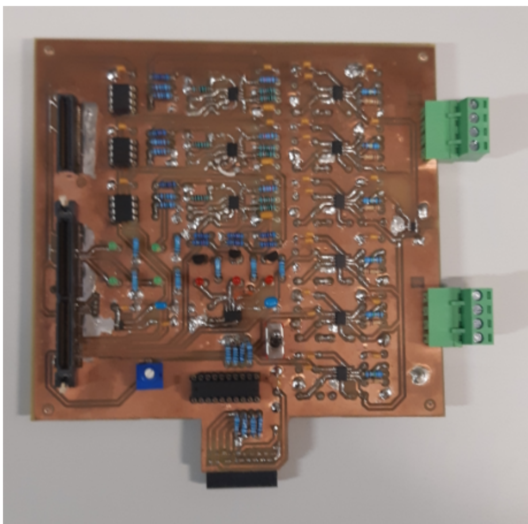
Figure 4-13: Adjusting the fault signal

When the fault signal is 5V the signal at the emitter will be 3.3v and nothing happens, since the trip zone not triggered. But when a fault signal has zero volts, the signal at the emitter will be zero volts, and the trip zone will be triggered, which will stop the generation of the PWM signals. An LED is connected between collector and base. At the event of a fault, the base has zero volts and the collector has 3.3V, so the LED will turn on, notifying the user about the fault.

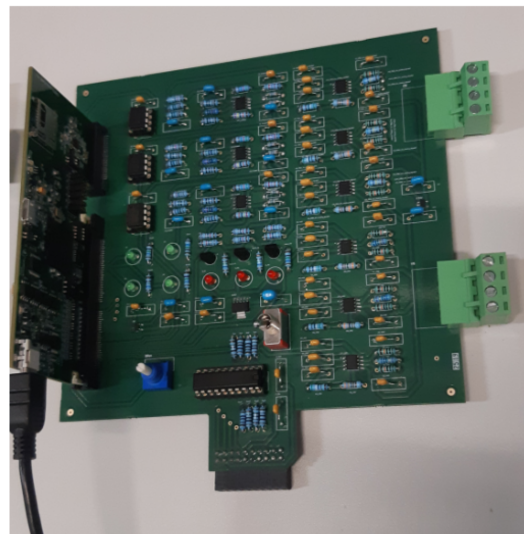
PWM Signals

The DSP generates PWM signals with 3.3V, although the gate driver used in the IMS evaluation board is compatible with 3.3V and 5V, it was preferred to use a buffer to increase the voltage to 5V, a switch is connected to the enable pin of the buffer, which can stop transferring the PWM signals to the gate driver. So if the user saw the fault LED turned on, he can interfere immediately by changing the switch state, thus stop transferring the PWM signals to the gate driver.

In addition to all the part mentioned before, the PCB has potentiometer and LEDs connected to General Purpose Input/Output (GPIOs) pins for general use and easier interface, as well a green LED is used in the PCB to indicate that the PCB is power.



(a) Version 1



(b) Version 2

Figure 4-14: Different versions of the PCB

The PCB was printed twice in different versions, the first one was hand made and not very good quality, there were some problems with soldering some components of the fault circuit, so faults where not triggered, and user cannot get notified with any high current passing through the system, moreover because of the poor quality the DPT signal had a bit of noise at the output of the PCB. On the other hand, the second version was printed in a professional way, and after testing all parts, it was working perfectly. Figure 4-14 shows the two versions of the PCB.

4.2.2 Double Pulse Test Signal Generation

As mentioned before the PWM signals will be generated using a microcontroller F28379D mounted on the PCB directly, check Figure 4-14 (b). The DSP model F28379D together with the C2000 DIMM100 Experimenter's Kit will allow generating signals to command the driver. Texas Instruments gives the ability to choose the qualification needed for each pin.

The PWM pins that are used to generate the signal and connected to the PCB are 49, 51, 53 ,55. The signal of the double pulse test can be generated using the normal General-Purpose Input/Output (GPIOs) pins, so the same pins mentioned before can be changed from ePWM mode to GPIO mode. For the test, the higher switch will be turned off all the time no need to command the driver at all, because of the 2DEG which allows the reverse conduction. The interest is to study the switching characteristics of the lower device, so the pulses will command its driver.

The software used to program the DSP was Code Composer Studio (CCS - Version9), which is based on C programming language. To generate the DPT signals the first thing to do is to set the required GPIO as an output, the first pulse will be generated by setting this pin to high-state for the required amount of time, then to turn off the transistor set the GPIO to low state for a small amount of time, good enough to catch all transients at the hard switching off event. the second pulse is generated again by setting the GPIO to high-state for a short period of time, then set it back to low.

To control the period of time to set the GPIO high and low a delay function provided by CCS called delayUS was used. As mention in Section 3.1.1, it is preferred to run the test one time or to have a use long repetition period. A variable called

start was created in the code for this purpose to allow the generation of the pulses and to run the code whenever the user sets its value to one, so when "start" equals 0 the code will do nothing, and when it is changed to 1 the code will run and will generate the double pulse test signal. At the end of the code, its value will be cleared and returned to be zero, thus preventing the short period repetition of the test. Figure 4-15 illustrates the flow chart of the program to generate a double pulse test signal.

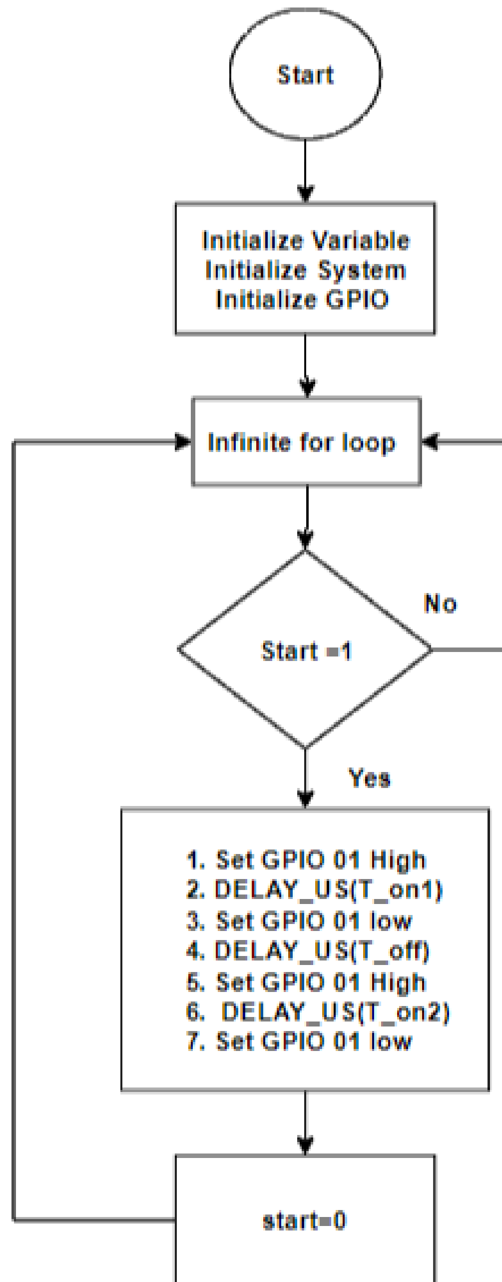
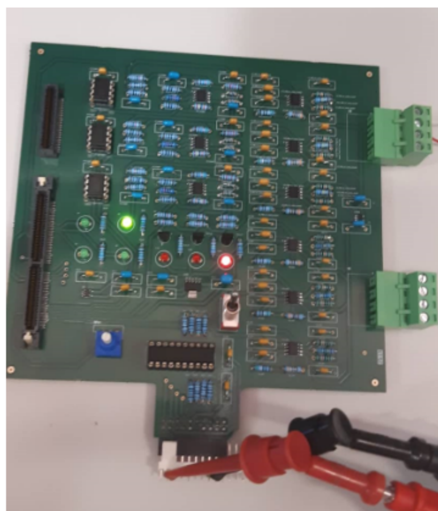


Figure 4-15: Flow chart for generating double pulse test signal

4.2.3 Double Pulse Test Setup

To build the setup many checks were made before connecting all components together. The DPT signal was checked in the beginning using TMDSDOCK28379D Experimenter's Kit, to make sure that the code will generate the required pulses and that the delay function is accurate enough to give the exact delay.

When the first PCB was tested, it gave results as expected for adapting stage and PWM signal buffering. Thus, it covers the requirements to do the double pulse test, The only issue was a small amount of noise appeared in the signal. And as mentioned before the fault triggering circuit was not working because of soldering and mounting issues. The second version of the PCB gave good results for adapting the signals, triggering high current, and adjusting the PWM signals. The communication between the DSP and the computer was tested, to see if the computer is able to recognize the DSP, as The DSP will be powered by the PCB, which is powered by the evaluation board. During first test, the DSP was not powered and the computer could not recognize, since there was no sufficient current from the voltage source 12V that powers the evaluation board. After increasing the current the CCS was able to connect to the DSP and debug the code, thus pulses were generated. Figure 4-16 (a) is showing how user will be notified from PCB of high current passing through the system. Figure 4-16 (b) shows the DSP powered by the PCB.



(a)

(b)

Figure 4-16: Parts of the testing steps before implementing the DPT setup

The next step after test the PCB and the DSP, making sure that they work and cooperate well together, was to assemble and connect with other parts of the setup. The DPT inductor value is 120 μH, the power voltage supply can give voltage up to 300V. The oscilloscope HDO6104A-MS provided by Teledyne LeCroy was used to measure the inductor current, V_{DS} and V_{GS}. Figure 4-17 shows the complete setup of the double pulse test.

Figure 4-17: Double pulse test setup

Chapter 5

Double Pulse Test Experimental and Simulation Results

In this chapter, the experimental and the simulation results of the double pulse test will be presented, analyzed and compared in the first part, while in the second part the switching losses will be analyzed using LTSpice software. Analyzing the switching transient behaviour is very important because it is an efficient way to evaluate the performance of the transistor together with the parasitic elements in the power loop [15, 46]. The test was done under different electrical parameters in order to be able to achieve a clear understanding of the device performance. The analysed voltages were: V_{in} = 50V; 100V; 150V; 200V; 250V; 250V. The analysed currents for each voltage level were: I = 5A; 10A; 15A; 20A; 25A; 30A.

The GaN transistor was not able to switch with voltages higher than 70V in previous tests which were using different experimental setup. This is due to the high ringing in the switching waveforms caused by the noise and extra parasitic elements coming from the test setup. On the other hand, using the setup design mentioned in the previous chapter, it was possible to run the test under 300V and 30A which are the maximum ratings that can be achieved with the currently available lab equipment with no problem in switching the device. Figure 5-1 represents the drain-to-source voltage and inductor current of the DPT performed experimentally with V_{in}=300V and I=5A. As shown in the figure below, the GaN transistor under the test was able to switch on and off smoothly under high voltage and high current, with acceptable

overshoots and transients.

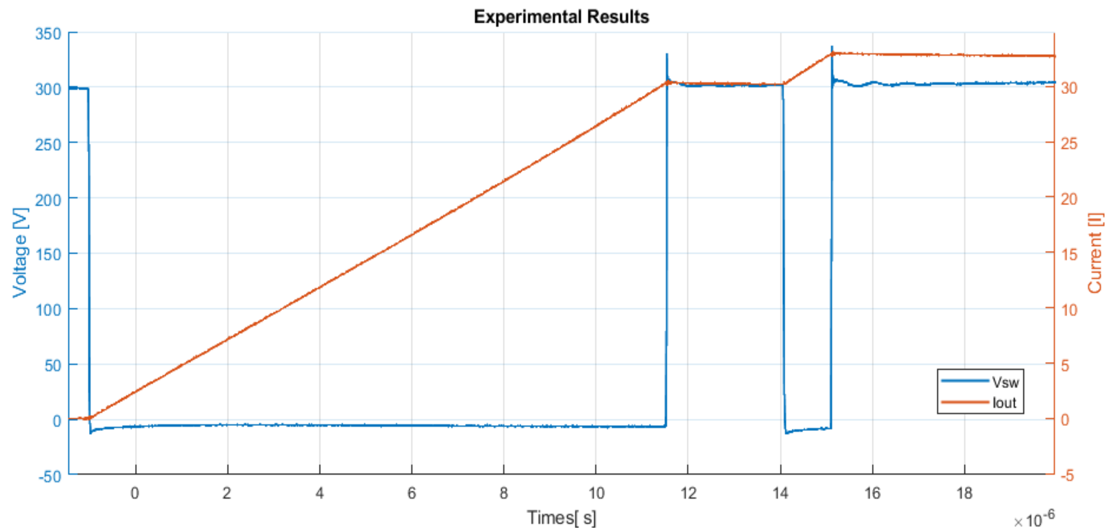


Figure 5-1: DPT Experimental Waveforms with V_{in}=300V & I=30A

5.1 Switching Transient Analysis

In this section, the experimental switching waveforms of the DPT will be analyzed and compared to the simulation waveforms for the turn-on and turn-off events. The only waveforms that will be analyzed are the drain-to-source voltage and the gate-to-source voltage, since the experimental evaluation board does not allow the accessibility to measure the switch current. However, with these voltages waveforms, it is possible to obtain large information, such as a comparison of the transient response between simulation and experiments, the overshoot voltage, the dV/dt, rise time, fall time, oscillation frequencies, etc [66]. All this information will be analyzed..

The test was done under many different conditions as mentioned before and presenting the results of all of them in this study will require many figures, and thus only some chosen results will be presented in this section. These results are good enough to cover the transistor behaviour under different conditions. The chosen conditions are 50V, 150V and 300V, with 5A, 15A and 30A. These conditions are sufficient to display the behaviour of the GaN transistor under the minimum and the maximum ratings for both voltage and current.

5.1.1 Turn-off Event

Figure 5-2 represents the experimental and the simulation waveform of the drain to source voltage transients at the turn off event when V_{in}=50V with different current levels. It is clear from the figure that there is a significant increase in the overshoot and the ringing when the the switch turns off at higher current values in both experimental and simulation tests. Nevertheless, increasing the current will increase the dv/dt, thus the transistor will have a faster response. When comparing the simulation results to the experimental ones, it can be observed clearly that the oscillations occur more in the simulations, while the overshoots are higher in the experimental test for all the current ratings. It can also be noted that the voltage at the steady state period is

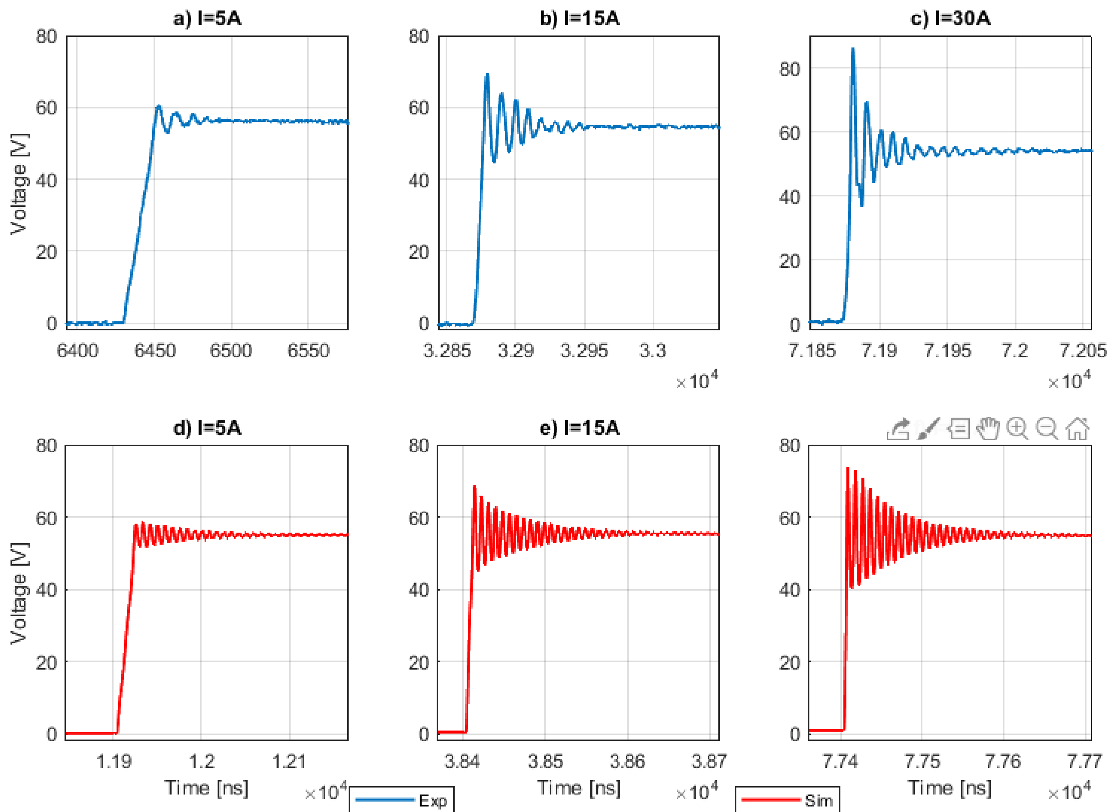


Figure 5-2: Drain-to-source (V_{DS}) voltage transients produced at the turn-off for different current levels at V_{in}=50V: (a) Experimental at 5A; (b) Experimental at 15A (c) Experimental at 30A; (d) Simulation at 5A; (e) Simulation at 15A; (f) Simulation at 30A.

higher than 50V and almost 55V. This is due to the voltage drop across the source and the drain at the revered conduction by looking at Figure 3-9, it can be noted that since the gate is turned off by -3V, the voltage across the source and the drain V_{SD} will be around 5V, which explains the 5V increase in the V_{DS}.

Figure 5-3 represents the experimental and the simulation waveform of the gate to source voltage transients at the turn off event when V_{in}=50V with different current levels. Similar to the drain to source voltage, the ringing at low currents is much lower than the ringing at high currents. In addition to this, the simulation signals had more transients and ringing than the experimental results, as at 5A the simulation signal had an undershoot close to 27% while the experimental signal had an undershoot equal

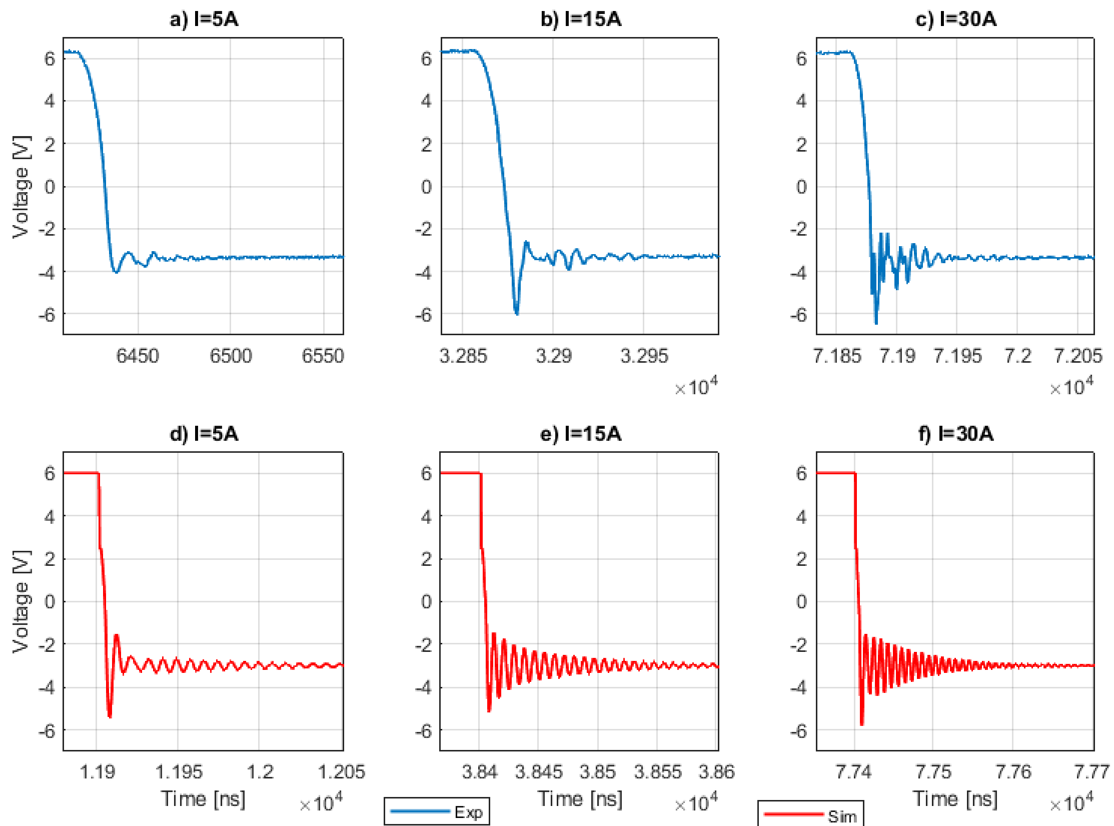


Figure 5-3: Gate-to-source (V_{GS}) voltage transients produced at the turn-off for different current levels at V_{in}=50V: (a) Experimental at 5A; (b) Experimental at 15A (c) Experimental at 30A; (d) Simulation at 5A; (e) Simulation at 15A; (f) Simulation at 30A.

to 9%. Furthermore, the gate switching speed was much higher in the simulation test than in the experimental test, but the switching speed was not affected too much by the increase in the current levels.

Figure 5-4 represents the experimental and the simulation waveform of the drain to source voltage transients at the turn off event when V_{in}=150V with different current levels. By comparing this figure to the previous one, it can be seen that a better turn off response by increasing the voltage of the transistor was achieved. There is a significant drop in the overshoot between operating at 50V and 150V, especially at high currents. Moreover at higher voltages the slew rate is higher for all currents, thus the transistor is switching faster at 150V. Similarly, it can be seen from the previous

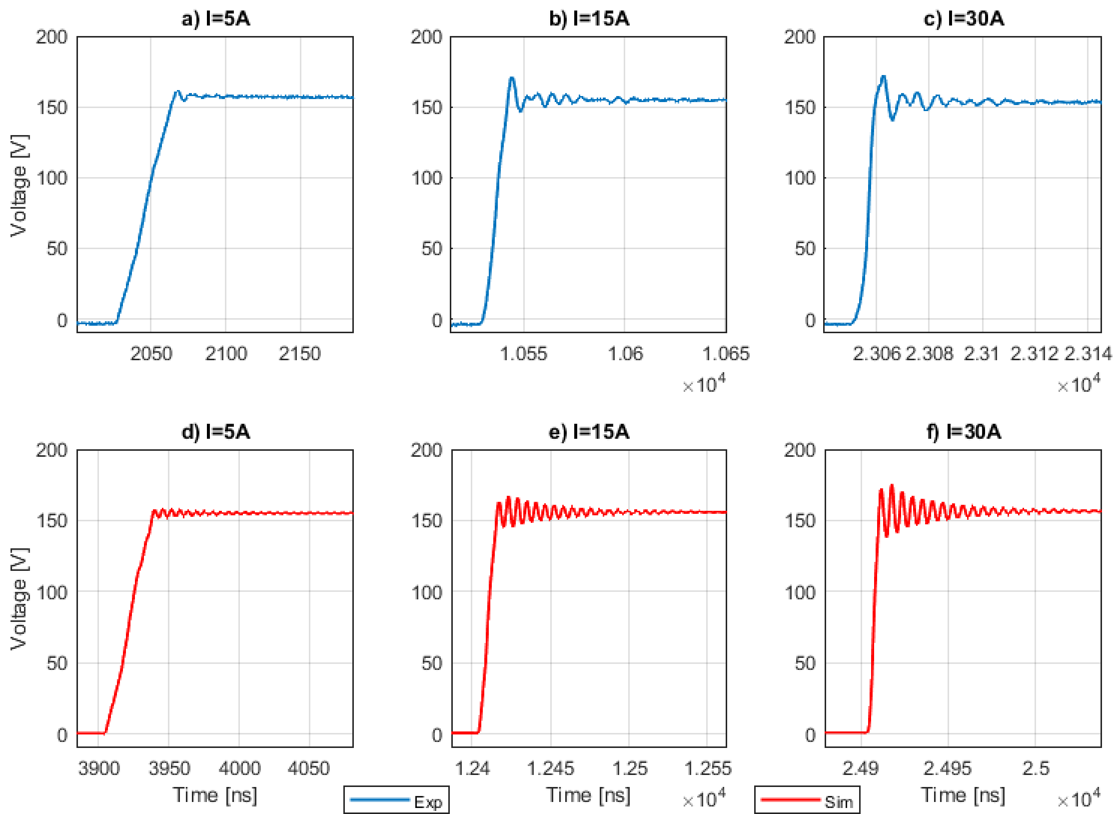


Figure 5-4: Drain-to-source (V_{DS}) voltage transients produced at the turn-off for different current levels at V_{in}=150V: (a) Experimental at 5A; (b) Experimental at 15A; (c) Experimental at 30A; (d) Simulation at 5A; (e) Simulation at 15A; (f) Simulation at 30A.

test that increasing the current for the same voltage level results in a higher overshoot. The difference can be seen in Figure 5-4 (a), Figure 5-4 (b), 5-4 (d) and Figure 5-4 (f). However, at higher currents, the transistor switches faster as the slew rate is bigger. Lastly, it can noted from the figure that the results from the simulations matched the experimental ones in a better way.

Figure 5-5 represents the experimental and the simulation waveform of the gate to source voltage transients at the turn off event when V_{in}=150V with different current levels. As it can be observed, at this voltage level the simulation transients do not match the experimental ones. The reason for this is that the oscillations are increasing in the experimental test by increasing the current level, while in the simulation test,

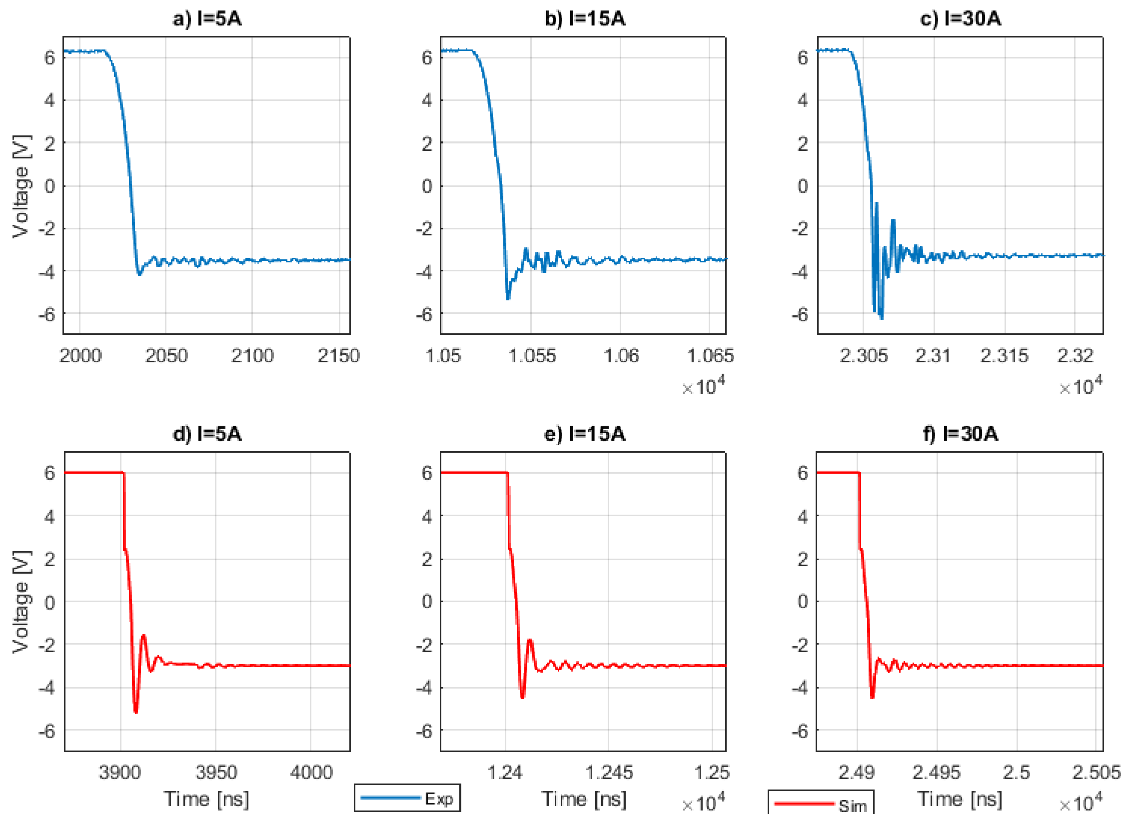


Figure 5-5: Gate-to-source (V_{GS}) voltage transients produced at the turn-off for different current levels at V_{in}=150V: (a) Experimental at 5A; (b) Experimental at 15A (c) Experimental at 30A; (d) Simulation at 5A; (e) Simulation at 15A; (f) Simulation at 30A.

the oscillations are disappearing and the signal becomes more clean and smooth. Similar to the previous case, the gate switches at a higher speed in the simulation test than in the experimental test. On the other hand, the switching speed was not affected by the increase of the current level.

Figure 5-6 represents the experimental and the simulation waveform of the drain to source voltage transients at the turn off event when V_{in}=300V with different current levels. At 300V there is a quite good match between the simulation results and the experimental results, even though a bit more oscillations occur in the simulations wavefroms. At 5A, there is a very small overshoot in the signal. In general, the overshoot for all current ratings decreased significantly when comparing this test to the

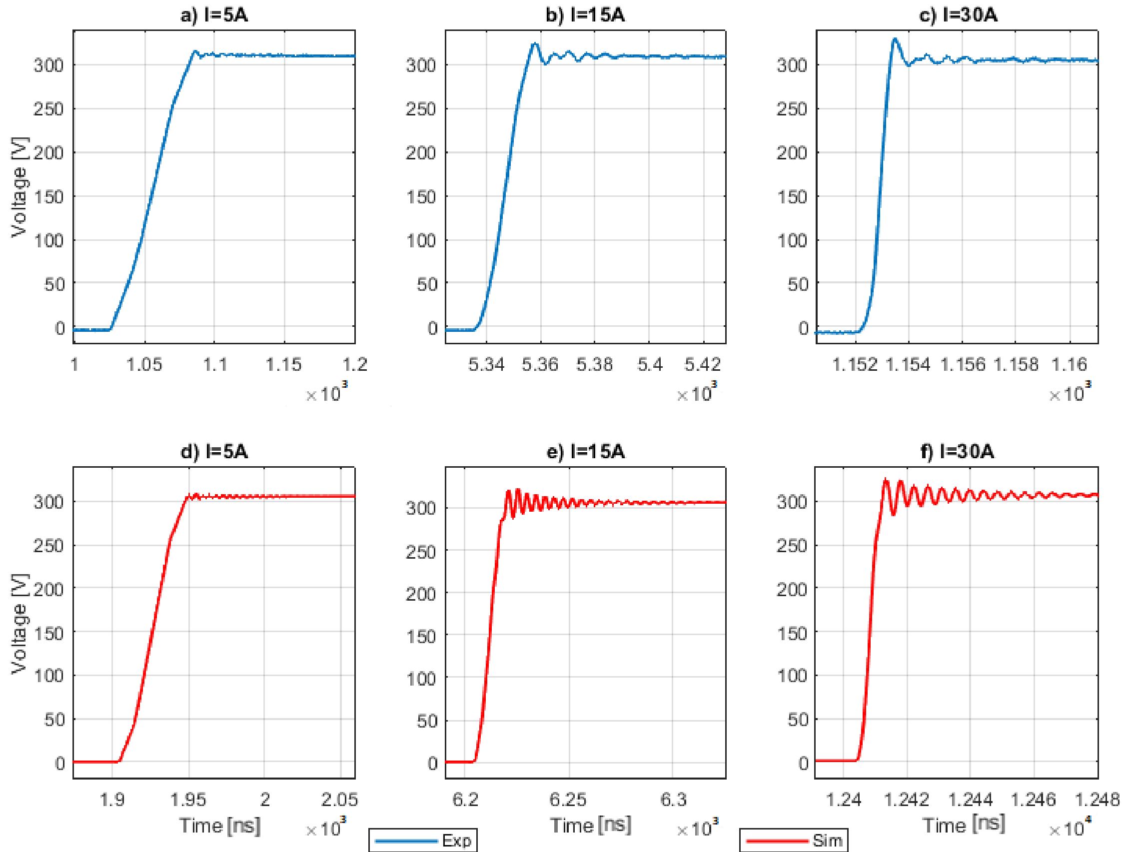


Figure 5-6: Drain-to-source (V_{DS}) voltage transients produced at the turn-off for different current levels at V_{in}=300V: (a) Experimental at 5A; (b) Experimental at 15A; (c) Experimental at 30A; (d) Simulation at 5A; (e) Simulation at 15A; (f) Simulation at 30A.

first one. As mentioned before, the transistor switches faster at higher voltage input and thus GaN transistors are an outstanding solution for high voltage applications.

Figure 5-7 represents the experimental and the simulation waveform of the gate to source voltage transients at the turn off event when V_{in}=300V with different current levels. The results of the test at this level are pretty similar to the previous one as the oscillations are increasing in the experimental test when the current level is increasing, while the simulation tests showed opposite results. And again the simulation gate switching speed is faster than the experimental gate switching speed, and it is not affected by the increase of the current levels neither the increase of the voltage level.

Table 5.1 analyses the previous waveforms in numbers by calculating the slew-rate

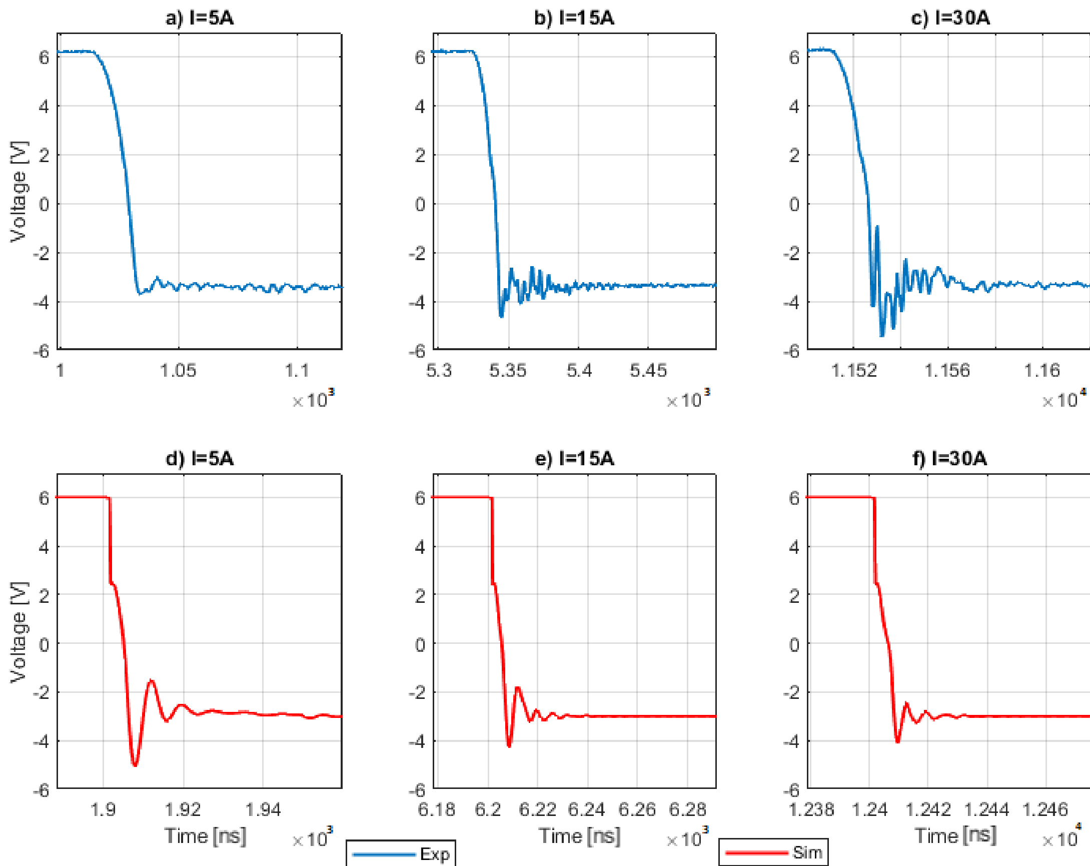


Figure 5-7: Gate-to-source (V_{GS}) voltage transients produced at the turn-off for different current levels at V_{in}=300V: (a) Experimental at 5A; (b) Experimental at 15A (c) Experimental at 30A; (d) Simulation at 5A; (e) Simulation at 15A; (f) Simulation at 30A.

(dv/dt) and the overshoot percentage, and comparing the experimental results with the simulation results. From this table it can be observed that there is a dramatic decrease in the overshoot percentage when the voltage increases, especially at the case of 30A, as it has decreased from 76.5% at 50V to 9.9% at 300V in the experimental work. Another key point to realize is the increase in the variation rate of the voltage with respect to the time dv/dt when voltages and currents are increasing, as for the tests with same voltage 150V for instance, it increased when the current increased from 4.24 V/ns to 25.25 V/ns in the experimental test, and it increased from 4.6V/ns to 27.7 V/ns in the simulation test. Additionally, increasing the voltage for the same current value 30A for example, increased the dv/dt from 10 V/ns at 50V to 36.79V/ns at 300V in the experimental test, and from 19V/ns to 45V/ns in the simulation test for the same voltages.

Table 5.1: Turn-off V_{DS} Transients Analysis

Voltage[V]	Current[A]	Experimental Results		Simulation Results	
		dv/dt [V/ns]	Overshoot	dv/dt [V/ns]	Overshoot
50	5	2.63	8.14%	2.66	5.97%
	15	7.15	33.26%	6.74	25.32 %
	30	10	76.50%	19	35.4 %
150	5	4.24	8%	4.6	1.56%
	15	13.45	13.7%	13.9	7.14 %
	30	25.25	14.7%	27.7	11.9%
300	5	5	5.8%	7.96	1.53%
	15	18.75	7.77%	25	5.85 %
	30	36.79	9.9%	45	5.85%

Although the transistor current was inaccessible, and impossible to be measured with the provided evaluation board, it is important to have an idea about the current transients under different operating conditions. Thus, the simulation results for the current transient at the turn of event are presented in Figure 5-8.

From the figure, it can be seen that by increasing the current level and keeping the

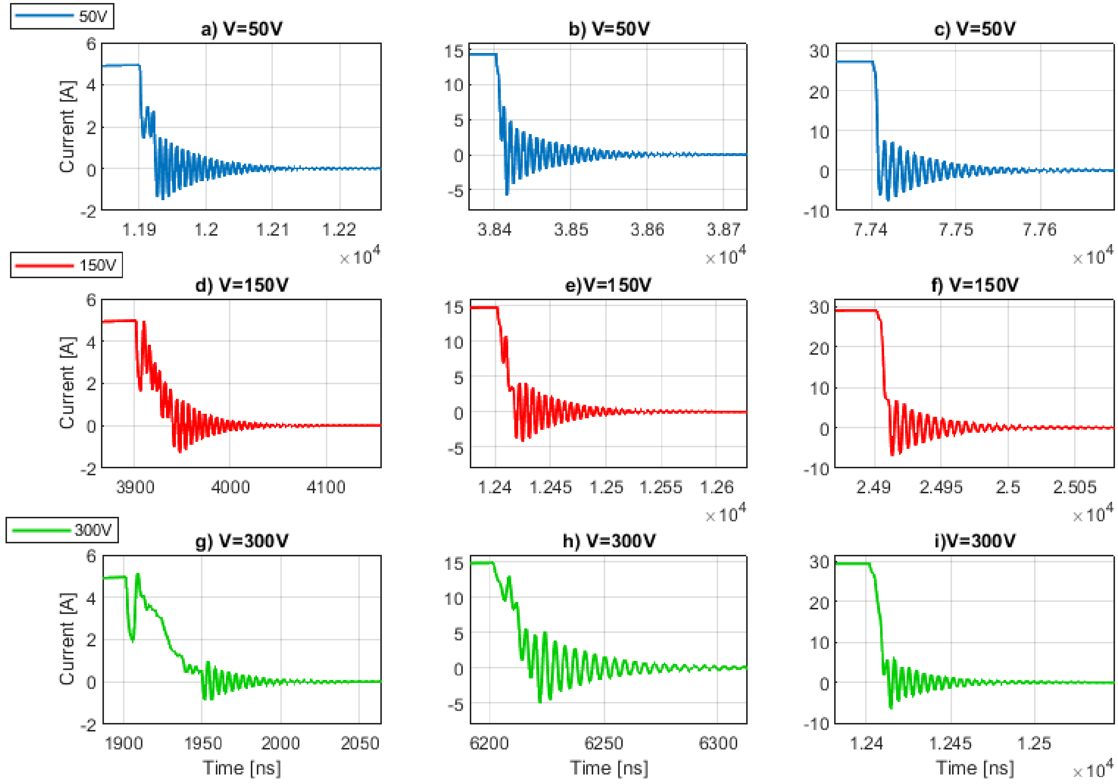


Figure 5-8: Simulation results for the transistor current transients produced at the turn-off for different voltage levels: (a) 5A at V=50; (b) 15A at V=50; (c) 30A at V=50; (d) 5A at V=150; (e) 15A at V=150; (f) 3A at V=150; (g) 5A at V=300; (h) 15A at V=300; (i) 30A at V=300

voltage at the same level, the current undershoots are increasing as well. While increasing the voltage for the same current level will result in less ringing and smoother switching, which matches with the analysis obtained from the V$_{DS}$ transients. Moreover the slewrate di/dt is increasing as well when the voltage increases which means faster switching at high voltages. Notice that at 5A for all the voltage levels there is a strange oscillations appearing along the fall edge, which is fading away with the current level increase, and it is clear that the cleanest and the smoothest signal was the one with 300V input voltage and 30A. It is expected that the real will have less ringing in the experimental tests, since the V$_{DS}$ signal had less ringing and oscillations in the experimental test than the simulation.

5.1.2 Turn-on Events

Figure 5-9 represents the experimental and the simulation waveform of the drain to source voltage transients at the turn on event when V_{in}=50V with different current levels. At this low voltage increasing the current did not show a clear difference between the waveforms, as the overshoot had increased slightly and almost stayed the same when the current was higher. While the dv/dt had dropped a little bit when the test was done at a higher current. There is a good match between the simulation and the experimental results at the turn on event, yet the experimental waveform has higher overshoots than the simulation waveform. Notice there is a dip occurred in the waveform when the current increased, specifically at 30A, this dip

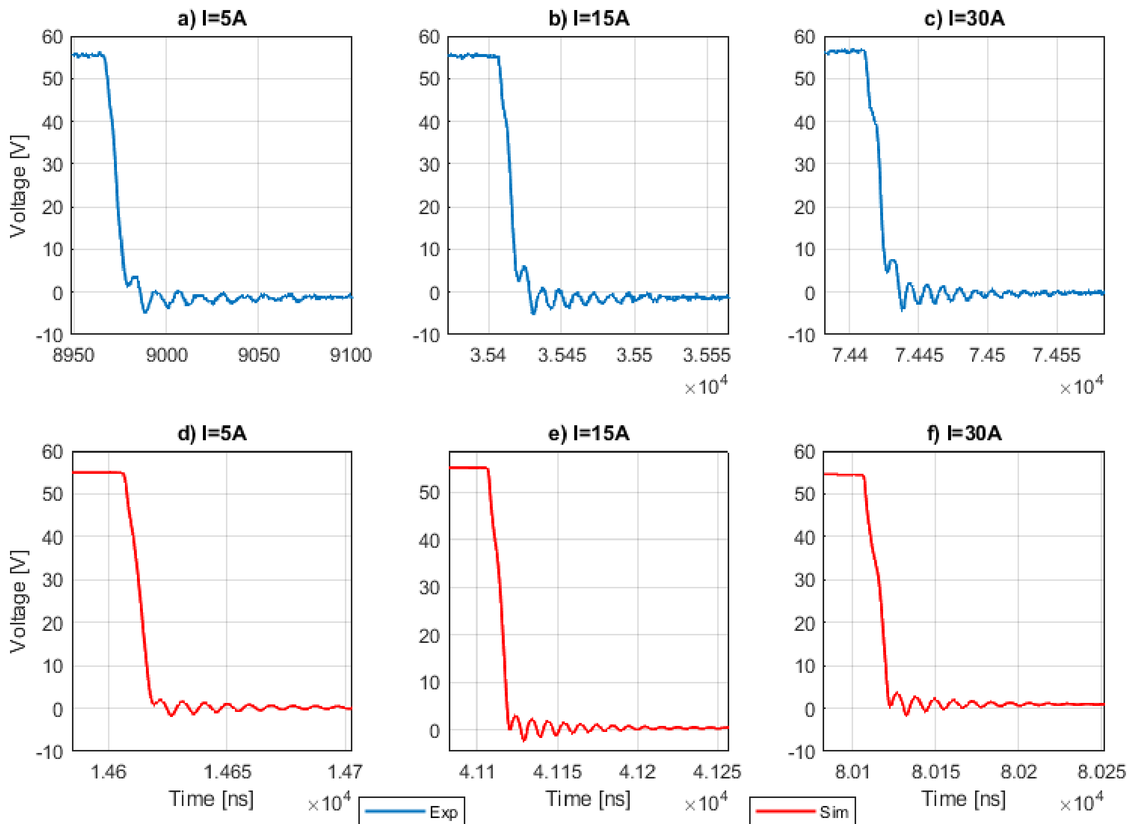


Figure 5-9: Drain-to-source (V_{DS}) voltage transients produced at the turn-on for different current levels at V_{in}=50V: (a) Experimental at 5A; (b) Experimental at 15A; (c) Experimental at 30A; (d) Simulation at 5A; (e) Simulation at 15A; (f) Simulation at 30A.

is caused by the loop inductance which is equals to ($\Delta V = L_p \times di/dt$) [48], the loop inductance effect will be seen clearly later at higher voltage levels.

Figure 5-10 represents the experimental and the simulation waveform of the gate to source voltage transients at the turn-on event when V_{in}=50V with different current levels. For the turn-on event the gate voltage was almost similar in experimental and simulation tests, but the experimental test had a bit more oscillations, and as shown in the figure the gate voltage at the turn on was similar for all current levels. Notice the oscillation that occurred in the middle of the signal while the voltage was increasing, this is due to the fact that gate current charges the gate to source capacitance C_{GS}. At the time the gate voltage reaches the threshold voltage V_{th}, the transistor starts

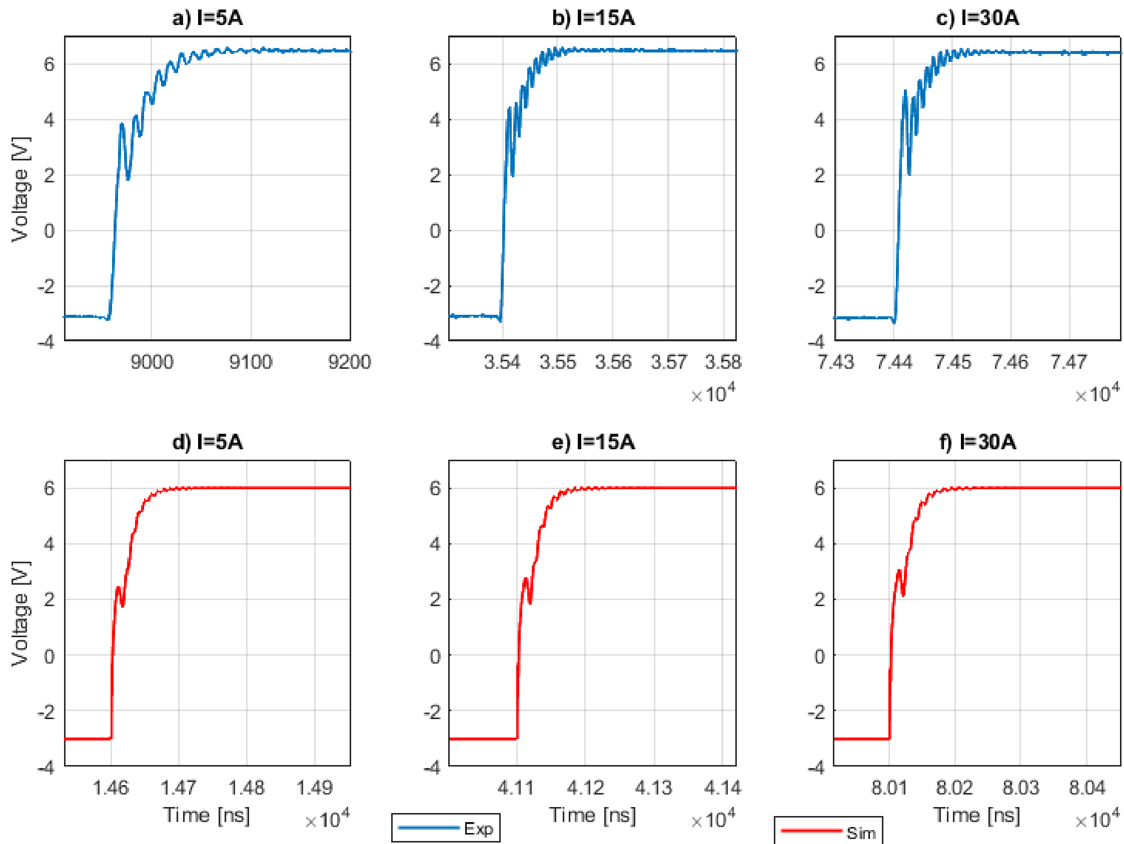


Figure 5-10: Gate-to-source (V_{GS}) voltage transients produced at the turn-on for different current levels at V_{in}=50V: (a) Experimental at 5A; (b) Experimental at 15A (c) Experimental at 30A; (d) Simulation at 5A; (e) Simulation at 15A; (f) Simulation at 30A.

to partially gate on. After that, the gate to drain capacitance C_{GD} starts to discharge through the drain to source channel, creating a plateau called Miller Plateau. During this period the gate voltage will stay constant, until the C_{GD} is fully discharged and the drain voltage reaches to zero. After that, the gate voltage start to increase again to reach its final value. Note that C_{GD} capacitance, despite being usually small, it has probably the greatest effect on the crossover time, because of the fact that it directly injects current from a high switching voltage node (drain) on to the gate [52].

Figure 5-11 represents the experimental and the simulation waveform of the drain to source voltage transients at the turn on event when V_{in}=150V with different current levels. Comparing the results of this figures with the previous one, the overshoots had a decreased and close to be negligible, again as mentioned before the increase in the

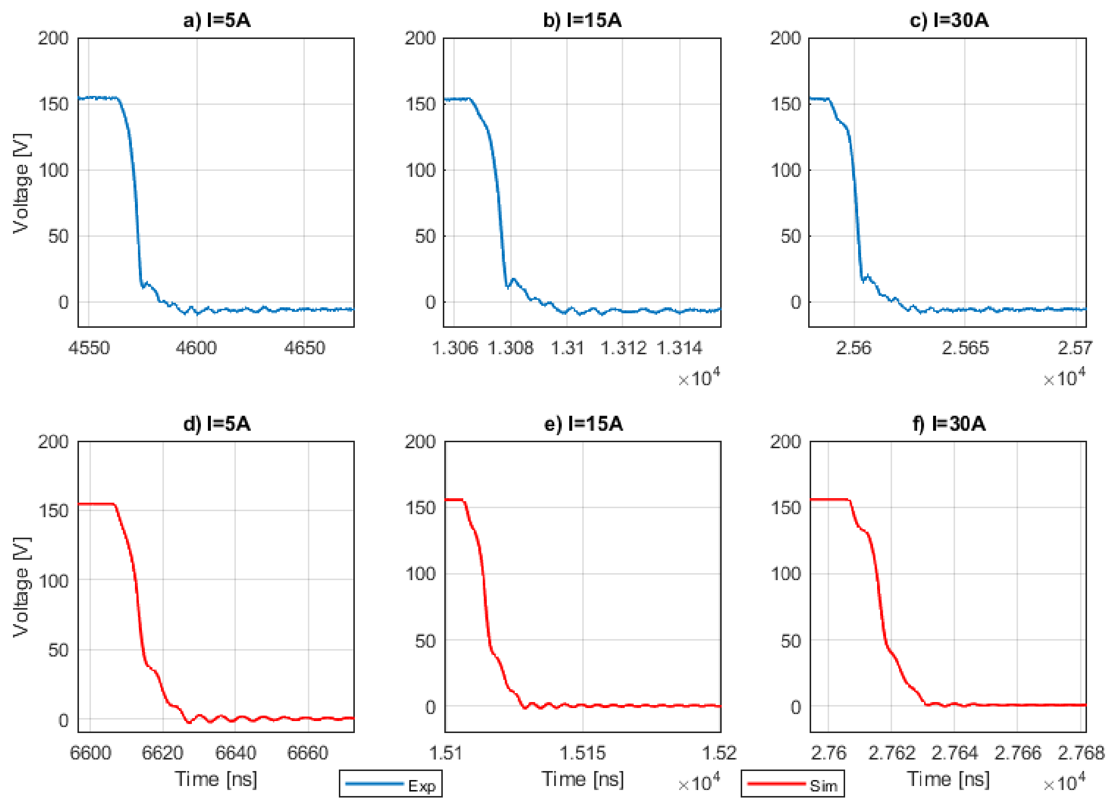


Figure 5-11: Drain-to-source (V_{DS}) voltage transients produced at the turn-on for different current levels at V_{in}=150V: (a) Experimental at 5A; (b) Experimental at 15A; (c) Experimental at 30A; (d) Simulation at 5A; (e) Simulation at 15A; (f) Simulation at 30A.

current ratings did not have a noticeable effect on the turn-on transients. Moreover, the switching response is faster at 150V than 50V, but there is no huge difference in the variation rate of the voltage with respect to the time dv/dt for different current levels with the same input voltage. Notice that at 30A, the dip caused by the loop inductance appears more clearly than the previous test conditions.

Figure 5-12 represents the experimental and the simulation waveform of the gate to source voltage transients at the turn-on event when V_{in}=150V with different current levels. In this figure the Miller Plateau appears more clear than the previous case, especially in the simulation test, and this is due to the fact that the interval in which the gate voltage stays constant depends on the value of C_{GD}, which changes significantly with the Drain to source voltage. And increasing the current levels did

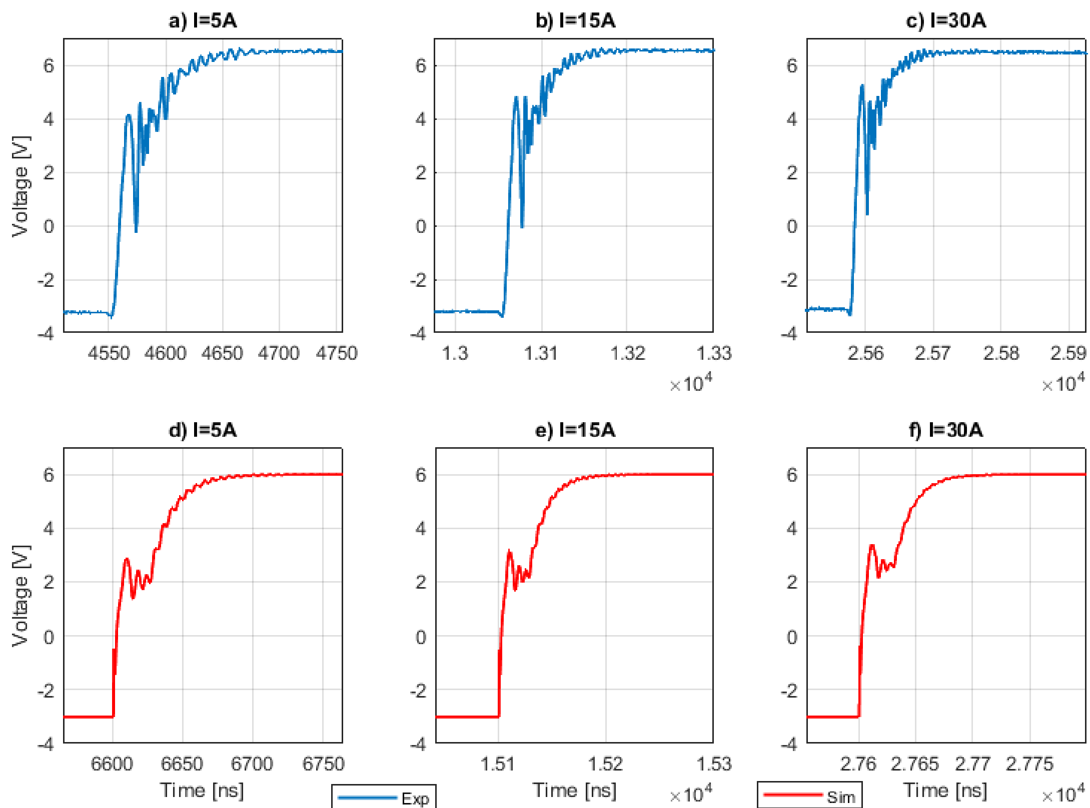


Figure 5-12: Gate-to-source (V_{GS}) voltage transients produced at the turn-on for different current levels at V_{in}=150V: (a) Experimental at 5A; (b) Experimental at 15A (c) Experimental at 30A; (d) Simulation at 5A; (e) Simulation at 15A; (f) Simulation at 30A.

not cause any difference in the gate voltage signal.

Figure 5-13 represents the experimental and the simulation waveform of the drain to source voltage transients at the turn on event when V_{in}=300V with different current levels. At this voltage level, the turn-on event had no overshoots or ringing in the signal, the signal was clean and smooth for all voltage ratings and in both simulation tests and experimental tests. Besides that, the dv/dt did not change much from the 150V input voltage case. Notice that in the experimental results in all cases, especially 150V and 300V, the voltage goes beyond the zero volts, this is due to the voltage drop across the transistor, while in simulation the transistor is very ideal that there is no voltage drop across it, and the voltage is equals to zero volts.

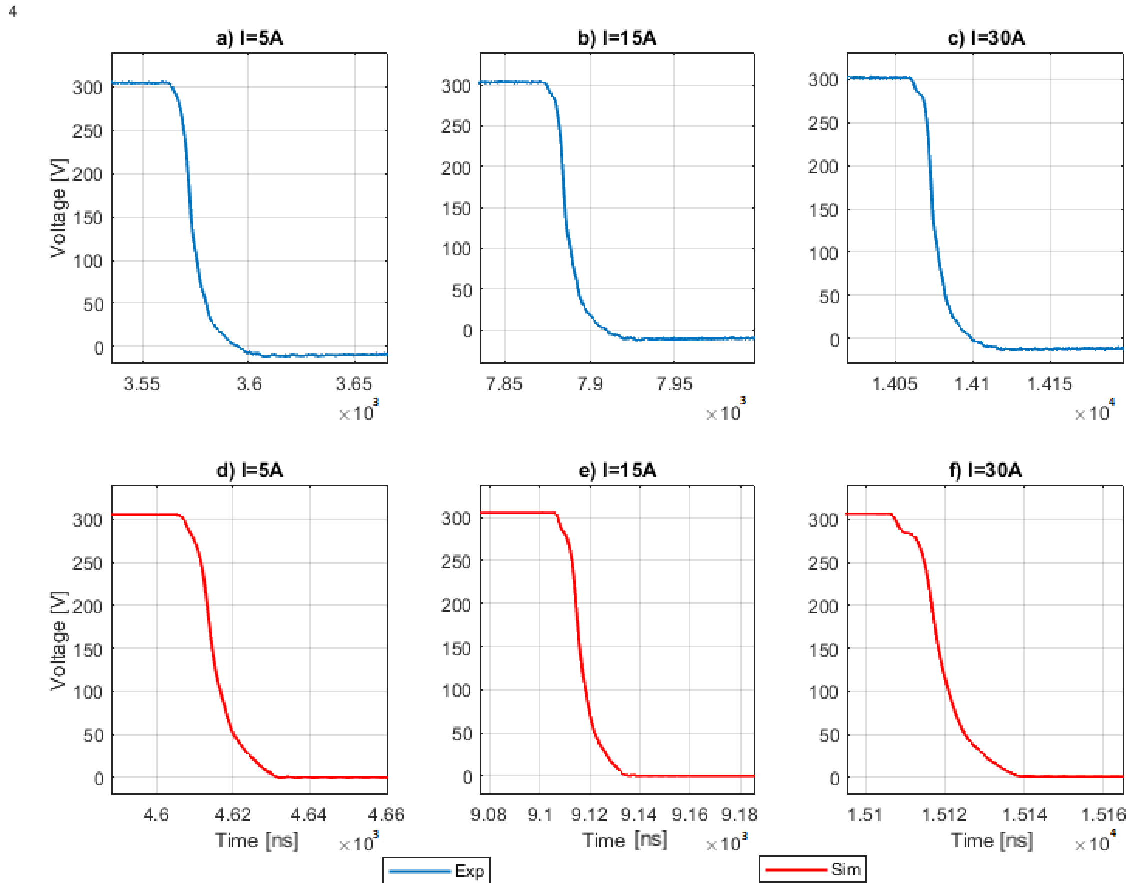


Figure 5-13: Drain-to-source (V_{DS}) voltage transients produced at the turn-on for different current levels at V_{in}=300V: (a) Experimental at 5A; (b) Experimental at 15A; (c) Experimental at 30A; (d) Simulation at 5A; (e) Simulation at 15A; (f) Simulation at 30A.

Figure 5-14 represents the experimental and the simulation waveform of the gate to source voltage transients at the turn-on event when V_{in}=300V with different current levels. At this voltage level the results are similar to the previous case, as Miller Plateau effect appears clearly, nevertheless the voltage peack overshoots at this voltage level is higher than the one at 150V. Increasing the current limit did not have a huge influence on the gate voltage signal but it enabled the gate to turn on faster at higher current level.

Table 5.2 summarize the previous analysis in numbers, as it can be observed increasing the current for the same voltage level did not have any noticeable changes the dv/dt and the overshoot values for both experimental and simulation tests. Nev-

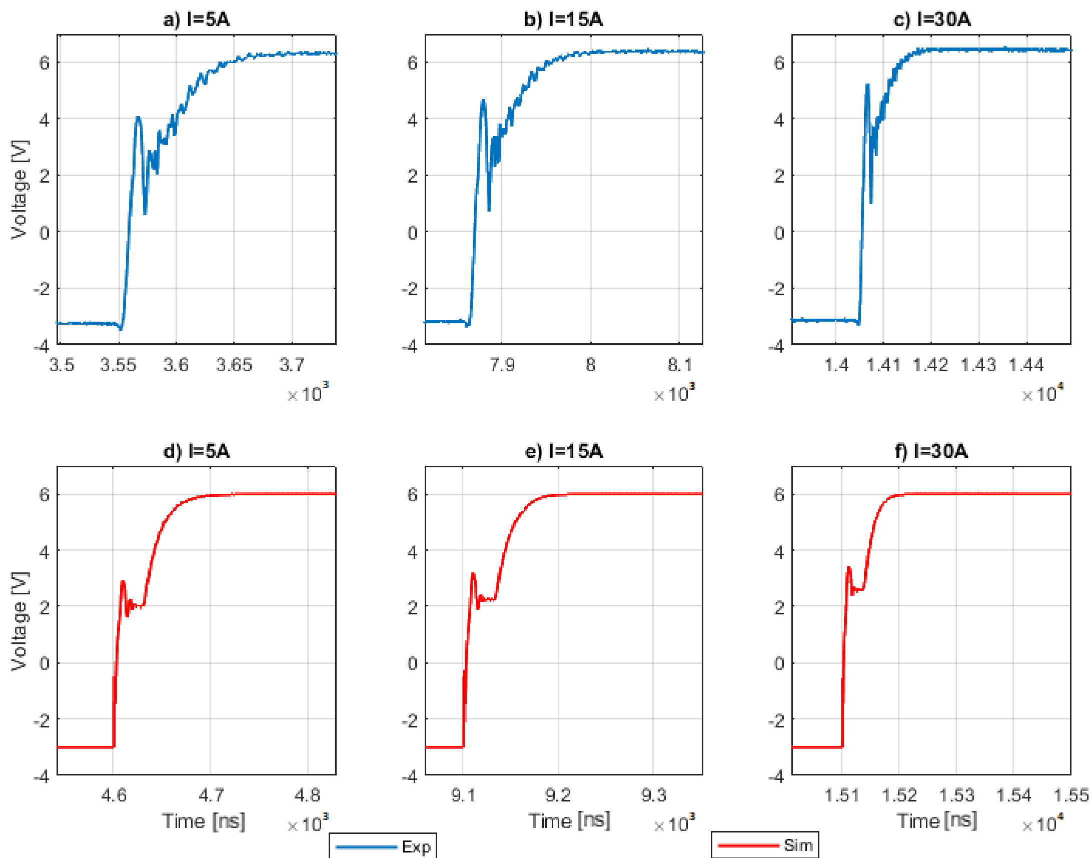


Figure 5-14: Gate-to-source (V_{GS}) voltage transients produced at the turn-on for different current levels at V_{in}=300V: (a) Experimental at 5A; (b) Experimental at 15A (c) Experimental at 30A; (d) Simulation at 5A; (e) Simulation at 15A; (f) Simulation at 30A.

ertheless, the switching speed is faster at the higher voltages when it is compared to the low voltage level, as it has increased from 5V/ns at 50V and 5A test, to 17.16 V/ns at 150V and 5A. The overshoots it is very low for all the test, but can be completely ignored in the 300V input voltage level, as in the experimental tests id did not reach 3%, while in the simulation tests did not reach 1%. The switching speed of the transistor at the turn-on event is much lower than the switching speed at the turn-off event as it reached 36.79% in the turn-off event, while in the turn-on event the best case was 17.16% for the experimental tests.

Table 5.2: Turn-on V_{DS} Transients Analysis

Voltage[V]	Current[A]	Experimental Results		Simulation Results	
		dv/dt [V/ns]	Overshoot	dv/dt [V/ns]	Overshoot
50	5	5	8.92%	4.7	2.71%
	15	4.2	9.70%	4.21	4.54 %
	30	3.26	8.33%	3.4	3.47 %
150	5	17.16	3.93%	10.2	1.56%
	15	15.72	4.166%	9	1.37 %
	30	8	2.68%	7.3	0.52%
300	5	15.49	1.51%	18.58	0.34%
	15	14.62	2.77%	17.3	0.11 %
	30	13.6	2.87%	15.4	0%

Figure 5-15 shows the transistor current behaviour during the turning on event. It is clear from the figure that increasing the voltage for the same current level, will cause a high overshoot in the signal, but on the other hand smoother and more clean signal with less ringing. Moreover increasing the voltage will let the device to switch on faster as the di/dt increases with the increase of the voltage. For the same voltage level increasing the current will decrease the overshoot percentage significantly as at 50V, the overshoot was 120% at 5A and it dropped to 41% at 30A. So, it can be concluded that these devices are suitable for high-current applications.

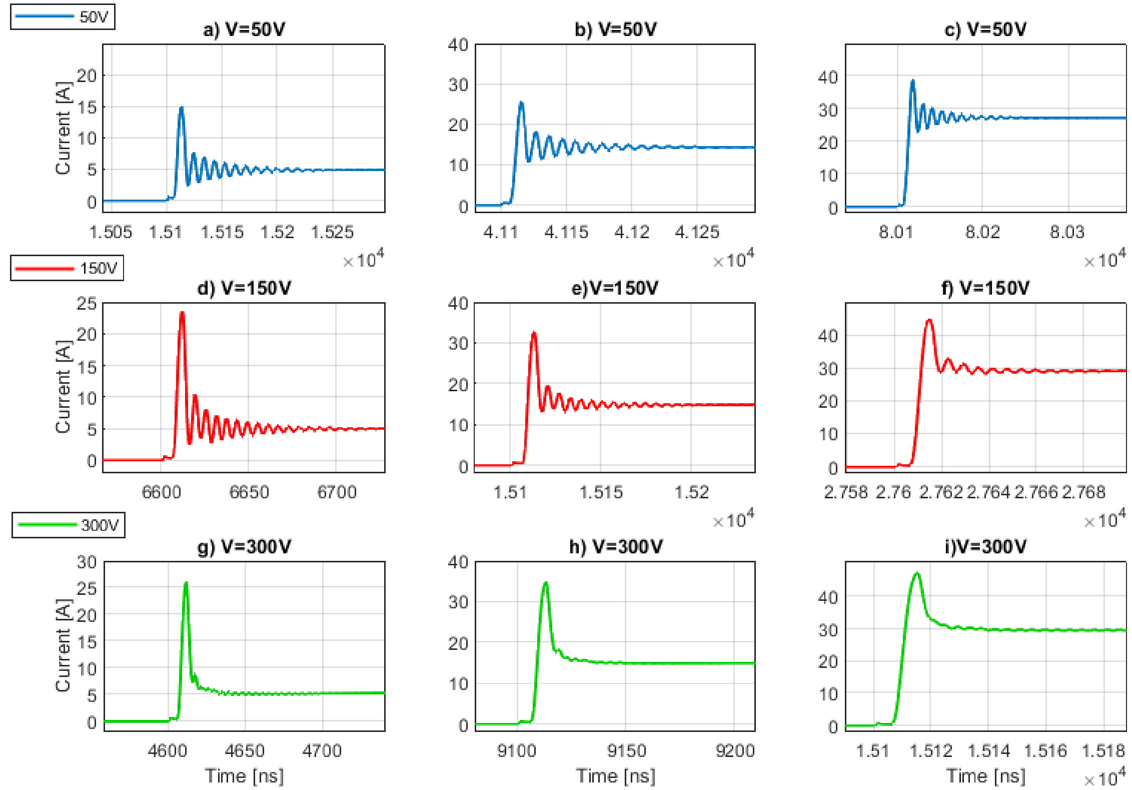


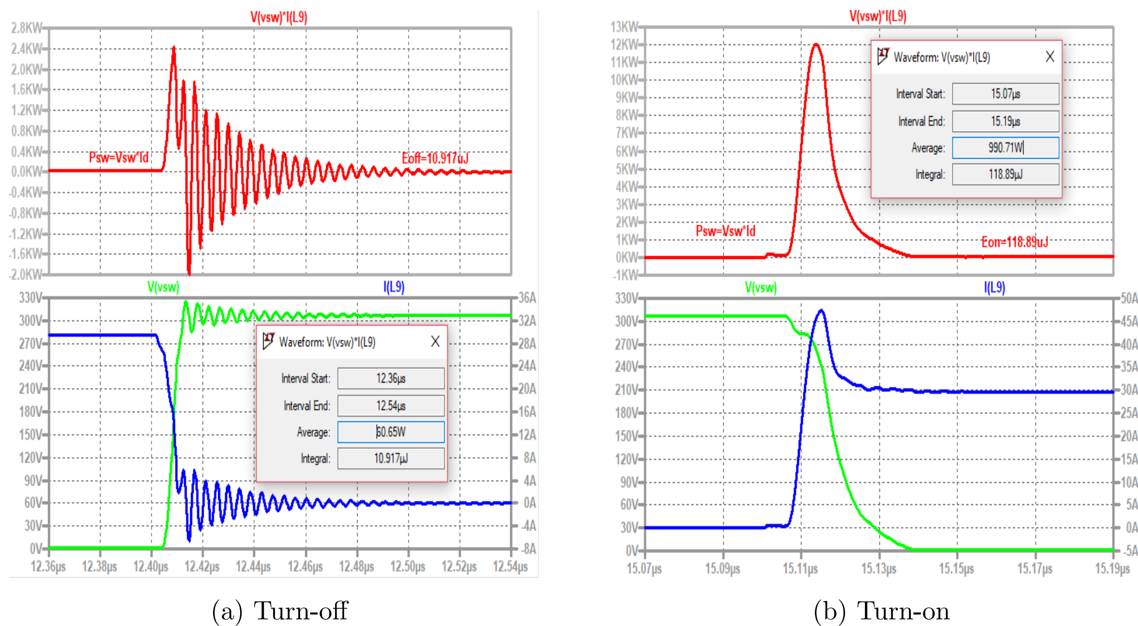
Figure 5-15: Simulation results for the transistor current transients produced at the turn-on for different voltage levels: (a) 5A at V=50; (b) 15A at V=50; (c) 30A at V=50; (d) 5A at V=150; (e) 15A at V=150; (f) 3A at V=150; (g) 5A at V=300; (h) 15A at V=300; (i) 30A at V=300

5.2 Switching Losses Analysis Using LTSpice

High electron mobility transistor (HEMT) has the advantage of fast switching capability, low power loss. In this section the switching losses will be analyzed through the simulation tests using LTSpice software, since the switch current could not be measure in the experimental work and as there was a good match between the experimental and the simulation results the switching losses obtained from the simulation can give a brief idea about the real losses. Switching loss characterization is decided by the transistor output capacitor (C_{oss}=C_{DS}+C_{GD}). Since GaN HEMT has a lower parasitic capacitor and lower conduction resistance than their Silicon counterparts, it has a fast switching capabilities and low switching loss [67].

LTSpice gives the ability to calculate the switching losses, by integrating the power

over a period of time so in this way the turn-off and the turn-on switching losses can be calculated as shown in Figure 5-16, which represent the turn-off and the turn-on losses for GaN device switching at 300V and 30A. From the figure it is clear to see that the turning off losses are much lower than the turning on.



(a) Turn-off (b) Turn-on

Figure 5-16: Calculating the turn-off and turn-on switching losses of the GaN device at 300V and 30A using LTSpice

Figure 5-17 shows the switching losses $E_{on}+E_{off}$ for different voltage and current levels. It can be observed in this figure that the increase in the voltage can increase the total power losses across the device, as well as increasing the current levels has the same influence, so the maximum loss was at 300V and 30A which is equal to 129.807 µJ. Anyway this results is pretty close to the values mentioned in the device datasheet [10], which indicates that at 400V and 20A the E_{on} will be equal to 134.1 µand the E_{off} will be equal to 14.7 µJ, so the total losses 148.8 µJ and it is higher than the simulation result because it is measured at higher voltage. Keeping in mind that the junction temperature at which the tests were performed is assumed to be around 30°C; and due to the very fast nature of the tests and to the cooling system, it is expected that the junction temperature did not increase too much beyond the room temperature. As the switching losses may increase with the junction temperature increase because the consumed energy by the device is dependent on the device temperature.

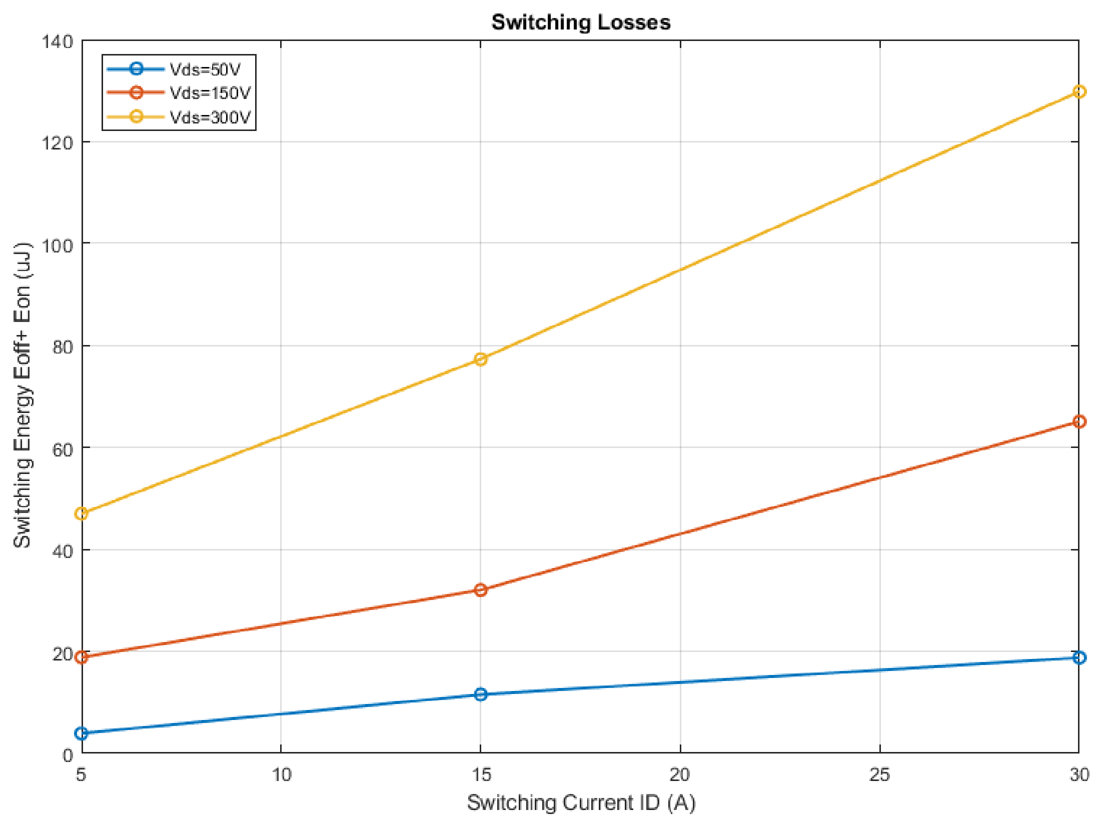


Figure 5-17: Switching losses for different voltage levels

Chapter 6

Conclusion and Future Work

6.1 Conclusion

Due to its superior material properties, GaN-based technology is expected to become the dominant semiconductor in high-power and high-speed applications. With the high field strength offered by GaN devices and the high mobility caused by the two dimensional-electron-gas (2DEG), this device can achieve a high breakdown voltage with a low on state resistance overtaking the limitation of conventional silicon devices. Since the power switching applications strongly demand normally-off operation, several normally-off structures have been proposed such as recessed gate structures, Fluorine ion treatment, p-GaN gate structures, as the conventional depletion mode HEMTs has a channel populated with electrons at zero gate voltage making them normally-on. However these novel transistors did not reach their maturity yet, and still there are many features that can be improved, and a lot of research to be done. In this work a stimulative and experimental characterization of 650V GaN HEMT has been performed using a double pulse test. With the mentioned setup design, the test succeeded to run under high current and high voltage levels with remarkable results.

During this work, it was addressed that these fast switching transistors are so sensitive towards the parasitic elements coming from the packaging design and the PCB design of the gate loop and the power loop. Therefore, these designs should be done carefully to avoid high ringing during the switching events that may lead to false turning on or off. Using The GS66516B enhancement mode gallium nitride (GaN)

transistor from GaN Systems, which is designed by GaNPX®, achieving getting low inductance and low thermal resistance in the small SMD package.

Since GaN transistors are fast switches, conventional measurement equipment does not have the ability any more to measure these high-frequency signals due to their limited bandwidth and dynamic frequency response limitations. Therefore, in order to determine the switching power characteristics and the losses of the power switches accurately, high-performance voltage and current measurement equipment must be used. Other than choosing the right oscilloscope, care must be taken when choosing the probe to measure the voltage as the parasitic elements introduced by these probes can lead to incorrect measurement results, and thus wrong analysis for the transistor switching characteristics, as it was proved in Chapter 3.

Moreover, the double pulse test setup should be designed in a way to prevent adding extra parasitic elements to the loop that may occur for example from the connection between the PWM generator (DSP or signal generator) and the experimental kit evaluation board. This may in turn cause high noise in the signal and as a result affecting the switching behaviour severely during the hard switching. To surpass these constraints, a PCB was designed as a solution and interface between the evaluation board and the DSP. This PCB was designed for general use to control the GaN transistors of the evaluation board for any topology. It was designed with the DSP mounted on it and it had a connector to allow the direct vertical connection with the evaluation board without the need for any wires as it was shown in Chapter 4, thus decreasing the parasitic elements as much as possible.

An LTSpice simulation of the half-bridge double pulse test circuit including the parasitics of the circuit and GaN device model from GaN Systems was used in order to determine the switching characteristics.A reasonably good agreement was achieved between the simulation model and measurement data after comparing the results from both. Keeping in mind that real world measurements can be affected by many factors.

In both cases, the experimental and stimulative tests, the overshoot produced during the turn-off and turn-on events was considerably decreasing while increasing the input voltage. It can be noticed from the obtained results that the transient response and the overshoot percentage were quite dependant on the test current level at the turn-off events. This means that increasing the current produced larger over-

shoot when compared to lower current levels for the same test voltage. So the worst turn-off scenario appeared at the lowest voltage level (50V) with the highest current level (30A). On the other hand, at the turn-on events the the transient response was independent of the current, so the increase in the current level did not have a notable effect for all the evaluated voltages.

For the voltage derivative (dV/dt), it was increasing with the increase of test voltage and current levels during the turn-off events, thus the fastest switching response appeared at 300V with 30A. Nevertheless, during the turn-on analyses the voltage derivative was controlled by the gate turn-on resistor, so since the turn-on speed is controlled by the gate resistor, there was a small reduction in the dv/dt with an increase in the test current for the same voltage level. In general, GaN transistor can turn-off faster than turning on.

In conclusion all the objectives of the test listed earlier were fulfilled. Namely, the theoretical analysis of GaN transistors was covered in chapter 2, while the overview of the double pulse test and its constraints were addressed in chapter 3. The design of the PCB as a control interface to enable the control of the GaN devices of the experimental kit and the detection of any possible faults was successfully achieved. The double pulse test signal was generated using DSP as planned. After testing the PCB, the setup of the test was built and tested, if all parts are able to work together. Moreover, the simulation design of the double pulse test using LTSpice gave matching results to the experimental ones, these results were analyzed and compared in Chapter 5.

6.2 Future Work

After analyzing the behaviour of the GaN HEMT transistors under hard switching events, more research and work can be done depending on these analysis, moreover there is still more improvements can be done to achieve more accurate analysis, so the future work that can be implemented are listed as bellow:

- First, it is very important to measure the drain current and to analyze the transient response of its single, as this information gives the possibility to extend the knowledge of the switching characteristics, in addition to calculate the power

losses of the device. So, another design can be done of the experimental kit that allows the access to measure the current switch.

- A thermal analysis can be performed to measure the heat distribution in the GaN device, to be able to analyze the behaviour of the switch during the temperature variations and improve the thermal management of this design.

- Another topologies can be used to analyze the behaviour of the switches in such as half-bridge, full-bridge and DC-DC converters for high-power fast-switching applications.

- An experimental and stimulative comparison with similar ranging SiC transistors to analyze the main differences between both WBG devices and to know the advantages and disadvantages (overshoots, peak voltages, dV/dt, power losses, thermal resistance, efficiency, etc.) of both power devices in DPTs and other converter topologies.

- PCB design including thermal and EMC aspects.

- Construction of a three phase inverter and dc-dc converters for automotive applications or low voltage microgrids.

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