



performance and even stability can be compromised.

This paper analyzes the design and implementation of synchronous PI current regulators for AC drives. Influence of machine characteristics, effects due to the discrete implementation of the controller and operation under voltage constraints (saturation) will be considered. The paper is organized as follows. Modeling of three-phase AC systems is presented in Section 2, both scalar and complex vector notation being used. Inverter operation and voltage limits are discussed in Section 3. Design and tuning of synchronous PI current regulators is discussed in Section 4. Discretization and operation under voltage constraints are covered in Section 5. Conclusions are summarized in Section 6.

## 2 Modeling of three-phase AC systems

Representation of AC systems and machines, and consequently the analysis of their current regulators can be addressed using both scalar and complex vector notation [1], [3], [6]-[9]. Although eventually both notations can provide the same results, each notation provides different insight into the control problem. The standard  $d$ - $q$  scalar notation results in multiple-input/multiple-output systems (and controllers), requiring the use of matrix algebra. The use of complex vector notation simplifies the model of an AC machine from a multiple-input/multiple-output system to an equivalent single-input/single-output complex vector system, it also reduces the order of the system by two, enabling the use of powerful analysis methods [7]. However, complex vector modeling requires that the AC system is symmetric (same parameters in the  $d$ - and  $q$ -axis). It is not suitable therefore for salient machines as interior permanent magnet machines or synchronous reluctance machines. Both scalar and complex vector notation will be used through the paper for the analysis of AC systems and their current control problem.

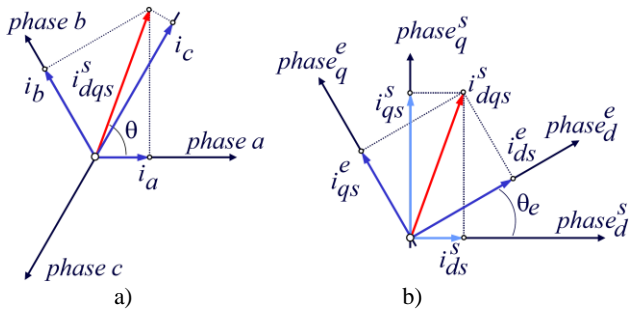


Fig. 2: Reference coordinate systems and coordinate rotations. a) three-phase quantities; b)  $d$ - $q$  plane in the stationary and synchronous reference frames.

### 2.1 Three-phase variables, two phase equivalent variables and complex vectors

#### A) Three-phase to $d$ - $q$ transformation and complex vectors

Given a set of three-phase currents, the linear transformation in (1) is used to transform the variables to an orthogonal  $d$ - $q$  coordinate system [1], [8].

$$\begin{bmatrix} i_{0s} \\ i_{ds}^s \\ i_{qs}^s \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1/2 & 1/2 & 1/2 \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (1)$$

The  $i_{0s}$  component is the average of the three phase currents, and is equal to zero for the common case of machines with an isolated neutral connection.

Three-phase variables can also be modeled using complex notation, the transformation being (2) [1], [8].

$$i_{dqs}^s = i_{ds}^s + j i_{qs}^s = \frac{2}{3} (i_a + i_b e^{j2\pi/3} + i_c e^{j4\pi/3}) \quad (2)$$

Transformations in (1) and (2) can be visualized as the currents  $i_a$ ,  $i_b$  and  $i_c$  aligned with three axes shifted  $120^\circ$  from each other being transformed to an orthogonal  $d$ - $q$  reference frame, as shown in Fig. 2.

#### B) Coordinates transformations

The  $d$ - $q$  reference frame defined by (1) and (2) is fixed in space and will be referred to as a *stationary reference frame*. Variables referred to this reference frame will be denoted by a superscript “ $s$ ”. The two-phase components defined by (1) and (2) can be referred to an arbitrary reference frame forming an angle  $\theta_e$  with the stationary reference frame, as shown in Fig. 2. This transformation is defined by (3) and (4) for the case of scalar and complex vector notation respectively. Variables referred to this reference frame are denoted by a superscript “ $e$ ”. This transformation is especially important when the reference frame rotates at the electrical frequency  $\omega_e$  of the electromagnetic variables (currents, voltages, flux-linkages) (5). This rotating reference frame is referred as *synchronous reference frame*.

$$\begin{bmatrix} i_{ds}^e \\ i_{qs}^e \end{bmatrix} = \begin{bmatrix} \cos(\theta_e) & \sin(\theta_e) \\ -\sin(\theta_e) & \cos(\theta_e) \end{bmatrix} \begin{bmatrix} i_{ds}^s \\ i_{qs}^s \end{bmatrix} \quad (3)$$

$$i_{dqs}^e = i_{ds}^e + j i_{qs}^e = i_{dqs}^s e^{-j\theta_e} \quad (4)$$

$$\omega_e = \frac{d\theta_e}{dt} \quad (5)$$

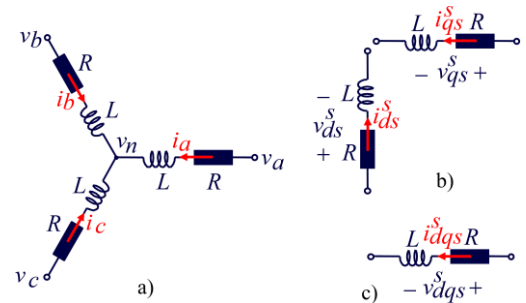


Fig. 3: a) Three-phase RL load; b) equivalent  $d$ - $q$  system; c) equivalent complex vector system.

## 2.2 Modeling of three-phase loads

$D$ - $q$  models play a major role in the analysis of three-phase systems, including electric AC machines. Though scalar and complex vector representations can be used for this purpose and will eventually provide the same results, each has its own advantages and disadvantages. Following a three-phase RL load will be used to discuss the different options and to analyze the current regulation problem in Section 3. Similarities between the current control problem of a three-phase RL load and a three-phase electric machines will be shown in Section 2.2C.

### A) Scalar model of symmetric RL load

The current to voltage relationship of a three-phase, symmetric RL load with isolated neutral connection (Fig. 3a), is described using matrix notation by (6). Since the neutral of the RL load is isolated (7) must hold.

$$\frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = R \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (6)$$

$$i_a + i_b + i_c = 0 \quad (7)$$

Applying (1) to both the currents and the voltages in (6) the two-phase equivalent system (8) is obtained. The reduction from three to two dimensions just recognizes the fact that the three-phase currents are not independent (7). The equivalent circuit is shown in Fig. 3b [8].

$$\begin{bmatrix} v_{ds}^s \\ v_{qs}^s \end{bmatrix} = R \begin{bmatrix} i_{ds}^s \\ i_{qs}^s \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_{ds}^s \\ i_{qs}^s \end{bmatrix} \quad (8)$$

It is useful from a modeling and control perspective to transform (8) to a synchronous reference frame. This is done by applying (3) to both the current and the voltages in (8), with (9) being obtained (the corresponding block diagram can be found in the right side of Fig. 10). It is observed that in the synchronous reference frame there is cross-coupling between  $d$ - and  $q$ -axis ( $\omega_e L$  terms).

$$\begin{bmatrix} v_{ds}^e \\ v_{qs}^e \end{bmatrix} = \begin{bmatrix} R & -\omega_e L \\ \omega_e L & R \end{bmatrix} \begin{bmatrix} i_{ds}^e \\ i_{qs}^e \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_{ds}^e \\ i_{qs}^e \end{bmatrix} \quad (9)$$

### B) Complex vector model of a symmetric RL load

The complex vector transfer function describing an RL load in the stationary reference frame (10) is obtained by taking the Laplace Transform after (2) to currents and voltages in (8) [8], where  $Y^s(s)$  corresponds to the stator admittance.

$$\frac{i_{dqs}^s}{v_{dqs}^s} = \frac{1}{Ls + R} = Y^s(s) \quad (10)$$

This transfer function can be referred to a synchronous reference frame (12) using (4), (5) and considering (11) [7]. The equivalent circuit is shown in Fig. 3c, the corresponding block diagram being shown on the right side of Fig. 9.

$$\frac{di_{dqs}^s}{dt} = \frac{d(i_{dqs}^e e^{j\omega_e t})}{dt} = \frac{di_{dqs}^e e^{j\omega_e t}}{dt} + j\omega_e i_{dqs}^e e^{j\omega_e t} \quad (11)$$

$$\frac{i_{dqs}^e}{v_{dqs}^e} = \frac{1}{L(s + j\omega_e) + R} = Y^e(s) \quad (12)$$

Comparing (8) and (9) with (10) and (12) is observed that the complex vector representation reduces both the order of the system and the number of inputs and outputs from two to one. It is also seen from (12) that poles (and zeros) in complex transfer functions do not need to exist in conjugate pairs as opposed to the scalar representation.

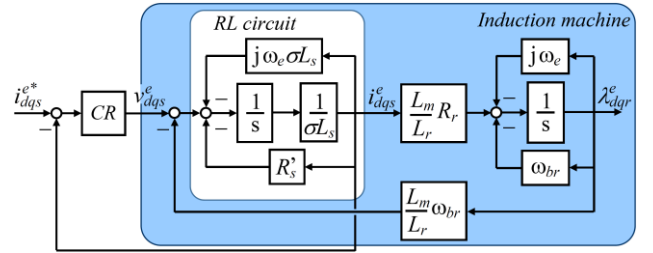


Fig. 4: Complex-vector block diagram of a current regulated three-phase induction machine.

### C) Complex vector model of an induction machine

For the sake of simplicity, an RL load has been chosen in Section 2.2 to introduce scalar and complex vector models of three-phase AC systems. However, the main target of this work is the study of current regulators for electric drives. Regardless of the significant differences between an electric machine and an RL load, they share some key properties, meaning that most of the conclusions reached for the current regulation of an RL load apply to the electric machine case. The induction machine will be used to illustrate this.

The nonlinear state equations in the synchronous reference frame governing the electrical and electromagnetic behavior of an induction motor using complex vector notation, with the stator current and the rotor flux as the state variables are (13) and (14), [7]. The corresponding block diagram is shown in Fig. 4.

$$\sigma L_s s i_{dqs}^e = v_{dqs}^e - (R_s' + j\sigma L_s \omega_e) i_{dqs}^e + \frac{L_m}{L_r} \omega_{br} \lambda_{dqr}^e \quad (13)$$

$$s \lambda_{dqr}^e = \frac{L_m}{L_r} R_r i_{dqs}^e - (\omega_{br} + j\omega_e) \lambda_{dqr}^e \quad (14)$$

$$\sigma = 1 - \frac{L_m^2}{L_s L_r}; \quad R_s' = R_s + \left( \frac{L_m}{L_r} \right)^2 R_r; \quad \omega_{br} = \frac{R_r}{L_r} - j\omega_r$$

The last term in (13) is the back-emf. Comparing (13) and (12) it is observed that the induction machine is equivalent to an RL load with the back-emf behaving as a disturbance voltage (see Fig. 4). Two different approaches can be followed for the extension of the RL load analysis to the electric machine case. The back-emf for the second case can be decoupled, the resulting system then coinciding with (12). Alternatively, the behavior of the induction

machine can be studied from the response of an RL load to a disturbance (back-emf) voltage [3]. This is further discussed in Section 4.

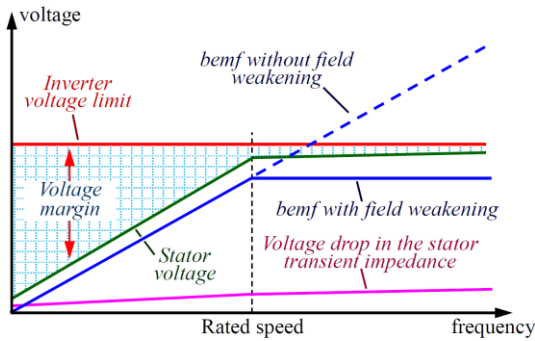


Fig. 5: Schematic representation of the voltage vs. speed characteristics of an induction machine in steady state. *Voltage margin* accounts for the voltage available to the current regulator for transient operation.

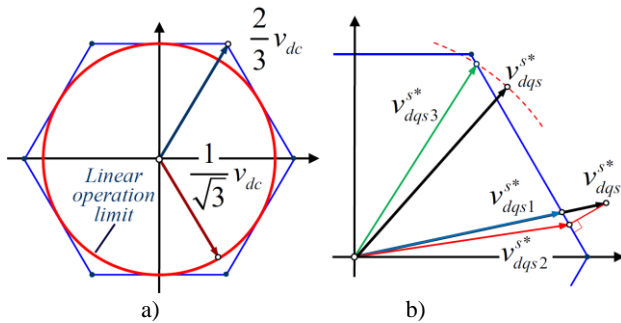


Fig. 6: a) voltage limits for a two level inverter; b) overmodulation strategies. Subscripts 1, 2 and 3 correspond to *minimum phase error*, *minimum distance* and *constant magnitude*.

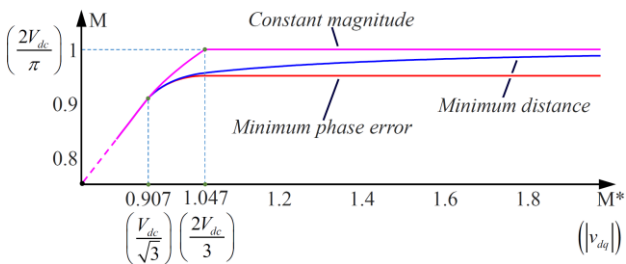


Fig. 7: Fundamental component of the output vs. reference voltage for different overmodulation strategies. Modulation index  $M=1$  corresponds to the maximum fundamental voltage that can be supplied by then inverter, which occurs for six-step operation.

### 3 Voltage needs and limits

The current regulator provides the voltage command to the three-phase inverter feeding the machine. Understanding inverter behavior and limits will be key for proper current regulator design and drive operation.

#### 3.1 Voltage needs

Fig. 5 shows a schematic representation of the stator voltage vs. frequency for an induction machine. It is noted that the discussion following also applies for other types of AC machines. When the machine is operating in steady

state, the difference between the stator voltage and the inverter voltage limit is the voltage margin available for the current regulator transient operation. This margin reduces as the frequency increases mainly due to the back-emf (last term in the right side of (13)), eventually affecting to the current regulator performance. Some relevant aspects must be considered in this case:

- Selection of current commands to produce the desired torque depends on the strategy used by outer control loops (field weakening, MTPA, ...) [10]. Discussion of this issue is beyond the scope of this paper. Independent of the strategy being used, current commands must be chosen such that in steady state there is enough voltage to produce the desired currents.
- Voltage margin reduction at high speeds will unavoidably penalize the current regulator transient response. It is critical to guarantee that this does not jeopardize system integrity due e.g. to current overshoots or even instability of the current loop.
- When the current regulator operates with a reduced voltage margin, it is important to ensure that the current regulator utilizes all the available DC link voltage [3], [10], [11], [12]. This involves both proper current regulator design and inverter modulation strategy.

DC link voltage utilization is discussed in the next subsection, transient operation of the current regulator under transient constraints being discussed in section 5.

TABLE I. MODES OF OPERATION OF THE INVERTER

	<i>Linear</i>	<i>Hexagon</i>	<i>Six-step</i>
Fundamental Voltage	$\leq \frac{1}{\sqrt{3}} V_{dc}^*$	$\frac{V_{dc}}{\sqrt{3}} \leq V_{max} \leq \frac{2V_{dc}}{\pi}$	$\frac{2}{\pi} V_{dc}$
Harmonic content	Lowest**	Increases with modulation index	Highest
Switching losses	Highest**	Decreases with modulation index	Lowest

\* For Space Vector Modulation or sine-triangle modulation with homopolar voltage injection [13]

\*\* Discontinuous modes of operation in the inverter reduce switching losses and increase the harmonic content

#### 3.2 Inverter operation and voltage limits

Fig. 6a shows the voltage limits in the  $d-q$  plane for a three-phase, two-level inverter. The maximum fundamental voltage component that can be supplied by the inverter is determined by the DC bus voltage and the modulation strategy. Operation of the inverter when the fundamental voltage is constrained to the inscribed circle is commonly referred as linear operation. It is possible to increase the fundamental voltage further by allowing the voltage command to move on the hexagon limits, which is referred as overmodulation. The maximum fundamental output voltage corresponds to six-step operation. In this mode the voltage vector remains on each corner of the hexagon for one sixth of the fundamental cycle [3], [14]-[17].

It is up to the designer to constrain the voltage command to the linear region or to use overmodulation. Choosing one option of the other involves a trade-off among: 1) the



maximum fundamental voltage (and consequently current and torque); 2) voltage (and consequently current) harmonic content, which will affect to torque *quality*; and 3) inverter switching losses. Table I summarizes the main properties for different modes of operation of the inverter.

A relevant issue in drives configured to operate in overmodulation or even six-step is the transition among the different modes. Voltage commands coming from the current regulator which are outside the hexagon (see Fig. 1) cannot be produced physically by the inverter and must be limited, several methods have been proposed for this. Using the intersection between the commanded voltage and the hexagon is likely the most intuitive solution, it is referred as *Minimum phase error* in Fig. 6b [11], [13]. A concern with this method is that the increase of the fundamental component of the output voltage vs. commanded voltage in the overmodulation region is modest (see Fig. 7) and cannot provide six-step. *Minimum distance* (see Fig. 6b) projects the original voltage command on the hexagon [11], [13]. Though this strategy produces a larger fundamental voltage, it cannot provide six-step either unless the voltage command becomes infinite. In the method proposed in [14] (*Constant magnitude* in Fig. 6b) the voltage command is rotated until it intersects the hexagon. An appealing property of this method is that it quickly produces six-step (whenever  $|v_{dqs}^*| \geq 2V_{dc}/3$ , see Fig. 7). Discussion on transition between different modes of operation of the inverter and the reconfiguration of the control loops can be found in [11].

### 3.3 PWM update and current sampling

Since synchronous PI current regulators are always implemented digitally, different strategies can be used for the PWM update and current sampling. The discussion following assumes that the PWM uses a triangular carrier but also applies for Space Vector Modulation. *Symmetric PWM* (Fig. 8-left) updates the voltage command once per cycle of the triangular carrier, while *Asymmetric PWM* (Fig. 8-right) updates the voltage command twice per switching period [3]. In both cases, updates must occur at the peaks of the carrier. *Asymmetric PWM* is preferred as it reduces by two the delay intrinsic to the PWM operation, enabling higher current regulator bandwidths. This can be of great interest in drives operating at low switching frequencies, but is at the price of doubling the computational burden of the current regulator.

Sampling the currents at the peaks of the triangular carrier (commonly known as synchronous sampling, see Fig. 8c) is the preferred strategy in AC drives [18]. Synchronous sampling is easy to implement and is claimed to provide the mean value of the current over the switching period, getting rid therefore of switching harmonics without the use of an anti-aliasing filters, which otherwise would compromise the current regulator bandwidth.

It is finally noted that traces shown in Fig. 8 use a constant switching frequency. Modulation strategies using variable switching frequency have also been proposed, as synchronized PWM [1], [3] and random PWM [19], which are of common use e.g. in electric traction.

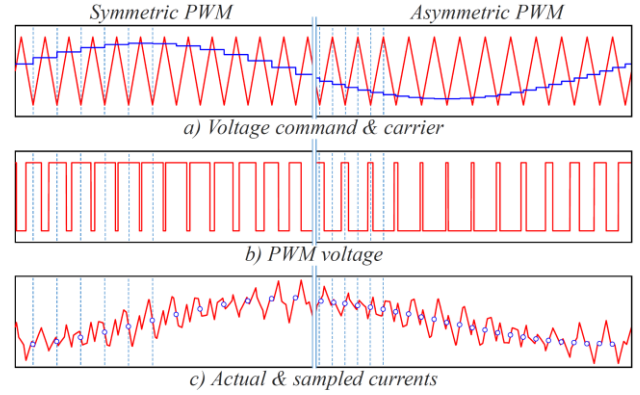


Fig. 8: Waveforms and current sampling for the case of symmetric and asymmetric PWM.

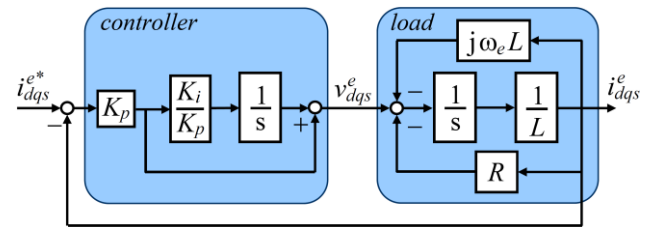


Fig. 9: Complex vector block diagram of a current regulated RL load using a classical synchronous PI current regulator, shown in a synchronous reference frame.

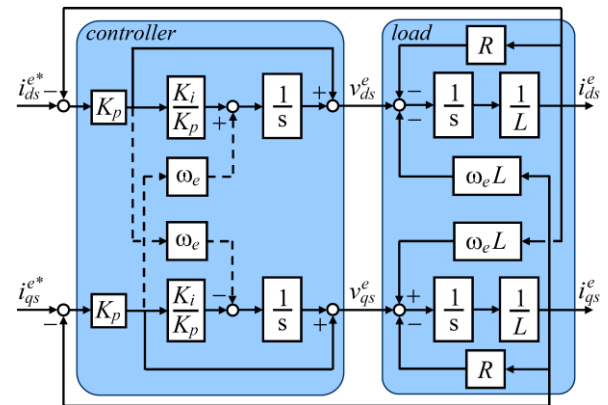


Fig. 10: Scalar block diagram of a current regulated RL load using a classical synchronous PI current regulator, shown in a synchronous reference frame. Dashed lines correspond the complex vector PI current regulator in Fig. 16.

## 4 Synchronous PI current regulators

The transformation of three phase loads to a reference frame rotating synchronously with the excitation frequency was already shown to have the appealing property of transforming sinusoidal signals into dc signals. A PI regulator implemented in this reference frame should therefore provide zero steady-state error, independent of the excitation frequency. This form of controller is denoted a synchronous PI current regulator and can be considered the standard in current controlled AC drives [5], [6].

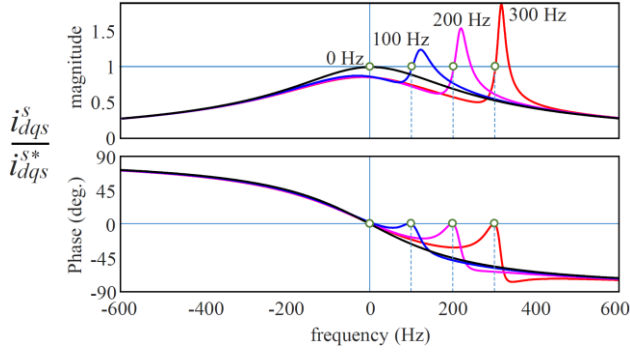


Fig. 11: Classical synchronous PI current regulator FRF for different fundamental frequencies. Current regulator was tuned for 200 Hz bandwidth.

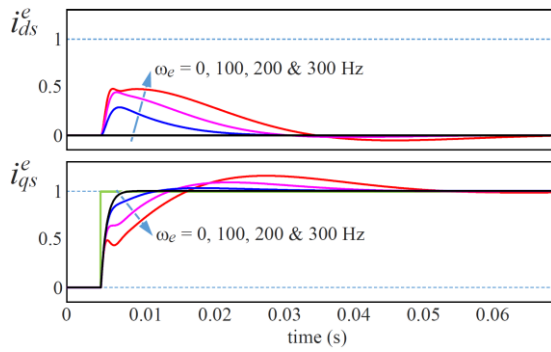


Fig. 12: Classical synchronous PI current regulator time response, shown in a synchronous reference frame, to a step-like command in the  $q$ -axis for different fundamental frequencies

#### 4.1 Classical synchronous PI current regulators

In its simplest implementation, the PI current regulator shown in the synchronous reference frame is given by (15), its block diagram is shown in the left side of Fig. 9.

$$\frac{v_{dqs}^{e*}}{\mathcal{E}_{dqs}^e} = K_p \frac{s + K_i/K_p}{s} ; \mathcal{E}_{dqs}^e = i_{dqs}^{e*} - i_{dqs}^e \quad (15)$$

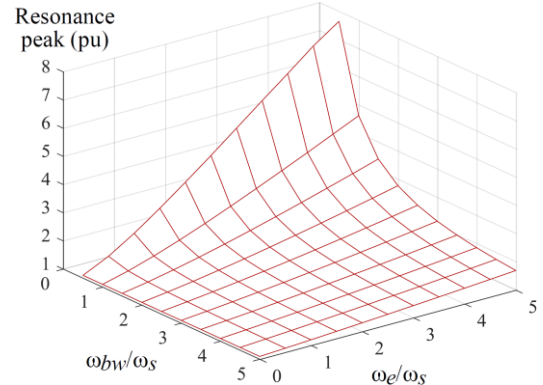
The scalar representation of this controller can be seen in the left side of Fig. 10 (without dashed lines). The regulator can be transformed into a stationary reference frame using (4) and (11), (16) being obtained.

$$\frac{v_{dqs}^{s*}}{\mathcal{E}_{dqs}^s} = K_p \frac{(s - j\omega_e) + K_i/K_p}{(s - j\omega_e)} \quad (16)$$

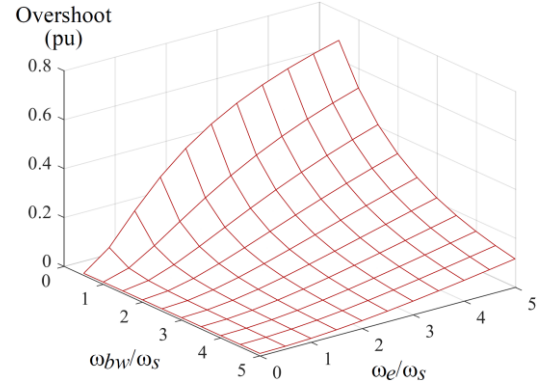
An effective way to tune the current regulator gains is zero-pole cancellation. The controller zero  $K_i/K_p$  is selected to be equal to the (estimated) cut-off frequency of the RL load,  $\omega_s$  (17). The proportional gain  $K_p$  is then selected to obtain the desired closed-loop bandwidth  $\omega_{bw}$  (in rad/s).

$$\frac{K_i}{K_p} = \frac{R}{L} = \omega_s ; K_p = \omega_{bw} \cdot L \quad (17)$$

The closed-loop transfer function in the stationary reference frame obtained from (10) and (16) is (18).



a) Resonance peak of the FRF



b) Overshoot of the time response (step input)

Fig. 13: a) resonance peak and b) overshoot in the time response of the FRF vs. bandwidth and synchronous frequency of a classical synchronous PI current regulator. Bandwidth and synchronous frequency are normalized to p.u. by dividing by the system bandwidth  $\omega_s = R/L$

$$\frac{i_{dqs}^s}{i_{dqs}^{s*}} = \frac{K_p s + K_i - jK_p \omega_e}{L s^2 + (K_p + R - j\omega_e L) s + K_i - j\omega_e (K_p + R)} \quad (18)$$

A suitable tool to evaluate the behavior of the closed loop system in (18) is the *Frequency Response Function* (FRF), which is obtained by making  $s = j\omega$  [7], [8]. Fig. 11 shows the FRF for the transfer function in (18). It is noted that as complex vectors can rotate both forwards (positive frequencies) and backwards (negative frequencies), the FRF must include both positive and negative frequencies. Furthermore, use of a logarithmic frequency scale is not possible unless some trick is implemented to avoid the frequency zero crossing. Two important facts are noticed from Fig. 11.

- In all the cases the FRF has a unity gain and zero phase shift at the synchronous frequency. This means that the current regulator guarantees perfect tracking (no error) in steady state. This holds for any synchronous frequency, regardless of current regulator bandwidth.
- A *resonance* in the FRF occurs near the synchronous frequency whenever the synchronous frequency is different from zero. This resonance increases as the synchronous frequency increases.

Transients in the current will excite the resonances shown in Fig. 11, eventually resulting in a degradation of

the current regulator dynamic response. Fig. 12 shows the time response of the synchronous PI current regulator to a step-like  $q$ -axis current command for different values of the synchronous frequency. As the synchronous frequency increases, current control degradation (overshoot, increased settling time and cross-coupling between  $d$ - and  $q$ -axis) is readily visible.

The results shown in Fig. 12 were obtained for certain values of the system pole and current regulator bandwidth. The behavior of the closed-loop system depends on the synchronous frequency  $\omega_e$  and closed-loop bandwidth  $\omega_{bw}$  vs. load cut-off frequency  $\omega_s$  (17). Fig. 13a shows the resonance peak of the FRF, while Fig. 13b shows the overshoot of the time response to a step-like command, as a function of the synchronous frequency and closed-loop bandwidth, normalized in p.u. of the system cut-off frequency  $\omega_s$ . The risks of operating at (relative) high synchronous frequencies with (relative) low current regulator bandwidths are evident from this figure.

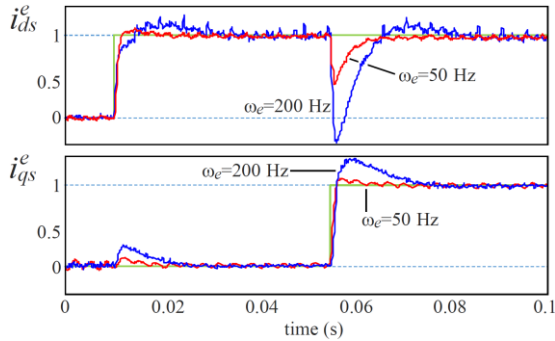


Fig. 14: Experimental results for an RL load ( $R=1.1 \Omega$ ,  $L=3.7$  mH). Classical synchronous PI current regulator time response, shown in a synchronous reference frame, to a step-like command in the  $d$ - and  $q$ -axis for two different fundamental frequencies.  $\omega_{bw}=200 \cdot 2 \pi$  rad/s.

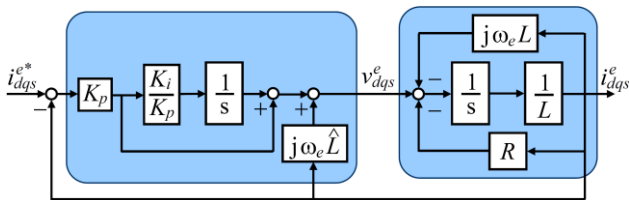


Fig. 15: Current regulated RL load using a classical synchronous PI current regulator with cross-coupling decoupling, shown in a synchronous reference frame.

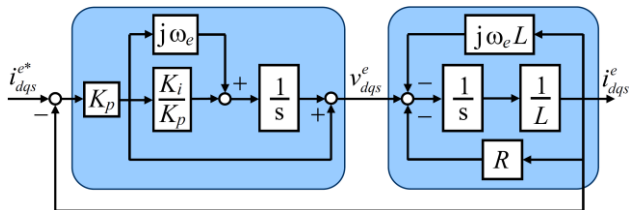


Fig. 16: Current regulated RL load using a complex vector PI current regulator, shown in a synchronous reference frame.

Experimental results showing the response of the synchronous PI current regulator to step-like commands in

the  $q$  and  $d$  axis current for two synchronous frequencies of 50 and 200 Hz are shown in Fig. 14. These results confirm the deterioration (overshoot, cross-coupling) of the current regulator response as the synchronous frequency increases.

An ideal synchronous PI current regulator should show a response independent of the synchronous frequency when viewed in a synchronous reference frame. Two different approaches to achieve this are discussed in the next subsections: 1) cross-coupling decoupling and 2) the complex-vector PI current regulator [7], [8]. This last one is equivalent to the internal model control discussed in [9].

#### 4.2 Synchronous PI current regulators with cross-coupling decoupling

A behavior independent of the synchronous frequency can be achieved using the scheme shown in Fig. 15. The current controller is seen to include a gain equal  $j\omega_e L$  in the feedback path which compensates the effect of the load cross-coupling. It is noted that the decoupling block implemented by the controller uses an estimation of the load inductance,  $\hat{L}$  which will differ from the actual value. The effects of the inductance estimation errors must therefore be considered [7], [8]. It is also noted that there is no error in the fundamental frequency  $\omega_e$ , as this frequency is set by the digital signal processor implementing the control.

#### 4.3 Complex-vector synchronous PI current regulator (internal model control)

The idea behind the complex-vector synchronous PI current regulator is to use the controller zero to cancel the system pole. This is in principle the same concept discussed in Section 4.1. However, the cancellation discussed in Section 4.1 was only effective for the case of a fundamental frequency equal to zero. The complex-vector synchronous PI current regulator (19) considers for the zero placement the displacement of the load pole with the fundamental frequency. This design is shown in Fig. 16.

$$\frac{v_{dqs}^{e*}}{\mathcal{E}_{dqs}^e} = K_p \frac{s + j\omega_e + K_i/K_p}{s} \quad (19)$$

Assuming exact zero-pole cancellation (17), the closed-loop transfer function in the stationary reference frame is equal to (20), which in a synchronous reference frame transforms to (21).

$$\frac{i_{dqs}^s}{i_{dqs}^{s*}} = \frac{K_p}{L(s + j\omega_e) + K_p} = \frac{\omega_{bw}}{(s + j\omega_e) + \omega_{bw}} \quad (20)$$

$$\frac{i_{dqs}^e}{i_{dqs}^{e*}} = \frac{K_p}{Ls + K_p} = \frac{\omega_{bw}}{s + \omega_{bw}} \quad (21)$$

Fig. 17 shows the FRF for both the synchronous PI current regulator with cross-coupling decoupling in Fig. 15 and the complex vector synchronous PI current regulator in Fig. 16, obtained making  $s = j\omega$  in (20). Perfect matching between system and controller parameters (17)

is assumed. The FRF shifts with the fundamental frequency, but its *shape* remains invariant, contrary to the FRF shown in Fig. 11 for the classical synchronous PI current regulator. In a synchronous reference frame, the closed-loop transfer function (21) is seen to be that of a first-order system with the desired bandwidth  $\omega_{bw}$  and independent of the synchronous frequency.

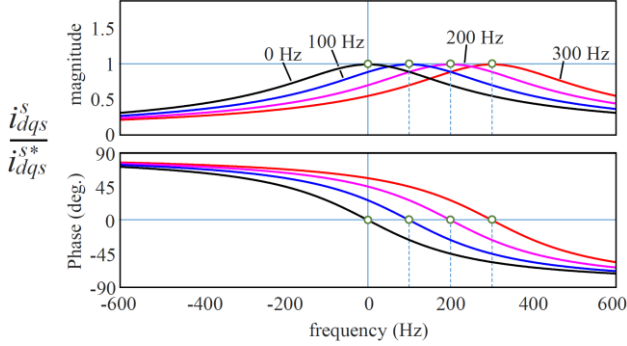


Fig. 17: Synchronous PI current regulator with cross-coupling decoupling and complex vector PI current regulator FRF for different fundamental frequencies. Current regulator was tuned for 200 Hz bandwidth.

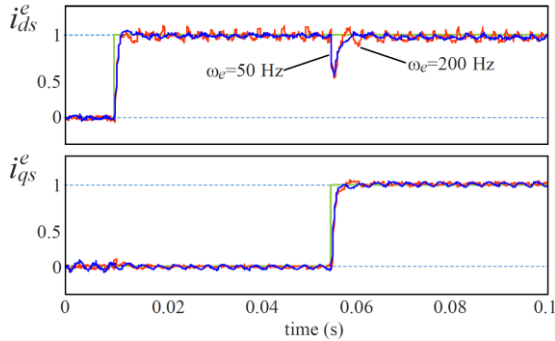


Fig. 18: Experimental results for an RL load ( $R=1.1 \Omega$ ,  $L=3.7$  mH). Complex vector synchronous PI current regulator time response, shown in a synchronous reference frame, to a step-like command in the  $d$ - and  $q$ -axis for two different fundamental frequencies.  $\omega_{bw} = 200 \cdot 2\pi$  rad/s.

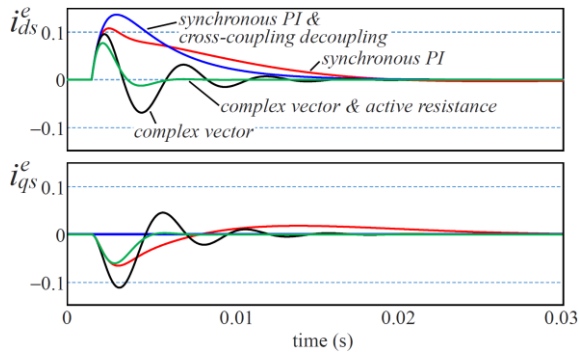


Fig. 19: Simulated response of different current regulator designs to a step-like disturbance voltage, shown in a synchronous reference frame.  $\omega_{bw} = \omega_e = 200 \cdot 2\pi$  rad/s;  $R_a = 2R$  for the active resistance case.

Experimental results showing the response of the complex vector synchronous PI current regulator to step

changes in the  $d$ - and  $q$ - axis current commands are shown in Fig. 18, for two synchronous frequencies of 50 and 200 Hz. These results confirm that the response of the current regulator is not affected by the synchronous frequency. The synchronous PI current regulator with cross-coupling decoupling provides similar performance, the results are not included due to space constraints.

It is finally noted that while both the synchronous PI current regulator with cross-coupling decoupling and the complex vector design provide the same performance ideally, the second is more robust against errors in the system parameters (i.e. incorrect zero-pole cancellation (17)) [8].

#### 4.4 Back-emf effects and compensation

As discussed in Section 2.2C, an electric machine can be modeled as an equivalent RL load with the back-emf acting as a disturbance (see Fig. 4). Back-emf occurs at the synchronous frequency and is proportional to the rotor speed and the flux linkage. On the other hand, it is observed from Fig. 5 that the voltage drop in the stator transient impedance, i.e. the voltage requested by the current regulator to inject the desired current into the equivalent RL load, is relatively small. Therefore, at medium-high speeds the back-emf can be viewed as large disturbance interfering with a small control signal.

The effects due to the back-emf can be analyzed using the transfer function between output current and back-emf voltage. These can be readily obtained from (12), (15) and (19), being (22) for the synchronous PI, (23) for the synchronous PI with cross-coupling decoupling and (24) for the complex vector synchronous PI current regulators.

$$\frac{i_{dqs}^e}{v_{bemf}^e} = \frac{s}{Ls^2 + (j\omega_e L + R + K_p)s + K_i} \quad (22)$$

$$\frac{i_{dqs}^e}{v_{bemf}^e} = \frac{s}{Ls^2 + (K_p + R)s + K_i} \quad (23)$$

$$\frac{i_{dqs}^e}{v_{bemf}^e} = \frac{s}{Ls^2 + (j\omega_e L + R + K_p)s + K_i + K_p j\omega_e} \quad (24)$$

Fig. 19 shows an example of the response of the different current regulator designs to a step-like change of the back-emf voltage. Several conclusions are reached:

- The DC gain is always zero, meaning that in steady state the disturbance voltage is fully compensated by the current regulator. This was expected as disturbance rejection to DC signals in steady state is inherent to the PI controller. The settling time is similar for all the designs.
- The back-emf voltage  $v_{bemf}^e$  is a function of the rotor flux and the speed. In many applications speed dynamics are significantly slower than current regulator dynamics, while flux will either remain constant or will vary according to speed (field weakening). Consequently  $v_{bemf}^e$  will change slowly. Its effects are therefore easily compensated by the current regulator.
- An exception can be servo drives with low mechanical inertia, for which speed dynamics might not be negligible compared to current dynamics. Back-emf



decoupling can be used in this case.

- The use of *active resistance* in the feed-back path (see in Fig. 20) is an effective mechanism to increase the stiffness of the current regulator against  $v_{bemf}^e$ . This *fictitious* resistance adds to the physical resistance but without consuming power [7]. Current regulator (25) and gain selection (26) are easily deduced from (19) and (17) respectively. The active resistance is selected as  $R_a = \omega_{bw}L - R$  in [12], [21].

$$v_{dqs}^{e*} = \varepsilon_{dqs}^e \left( K_p \frac{s + j\omega_e + K_i/K_p}{s} \right) - i_{dqs}^e R_a \quad (25)$$

$$K_i = \omega_{bw}(R + R_a) ; K_p = \omega_{bw} \cdot L \quad (26)$$

Benefits of *active resistance* can be observed in Fig. 19.

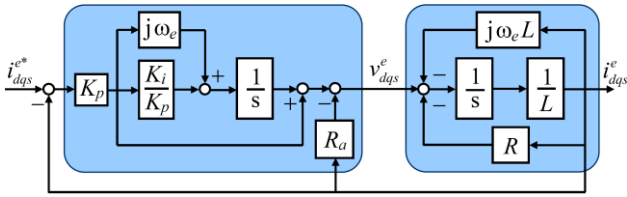


Fig. 20: Current regulated RL load using a complex vector PI current regulator with *active resistance*  $R_a$ , shown in a synchronous reference frame.

#### 4.5 Current regulator representation using a state-feedback structure

The synchronous current regulator (25) can be represented as a state-feedback regulator, augmented with integral action and the reference feedforward [20], [21], where  $K_i$  is the reference-feedforward gain,  $K_i$  is the integral gain, and  $K_i$  is the state-feedback gain. In a general case, the gains are complex, which is marked with boldface symbols.

$$v_{dqs}^{e*} = K_i i_{dqs}^{e*} + \frac{K_i}{s} (i_{dqs}^{e*} - i_{dqs}^e) - K_i i_{dqs}^e \quad (27)$$

This structure, illustrated in Fig. 21, is useful for better understanding the direct discrete-time design in Section 5.

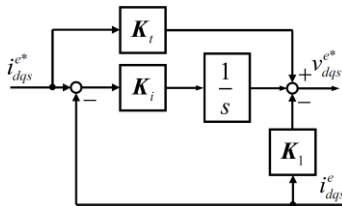


Fig. 21: Synchronous current regulator in the form of state-feedback regulator.

Using (12) and (27) with the assumption  $v_{dqs}^{e*} = v_{dqs}^e$  the closed loop response is obtained,

$$\frac{i_{dqs}^e}{i_{dqs}^{e*}} = \frac{(K_i s + K_i) / L}{s^2 + [(K_i + R) / L + j\omega_e] s + K_i / L} \quad (28)$$

The two closed-loop poles can be arbitrarily placed by means of  $K_i$  and  $K_i$  and the one zero by means of  $K_i$

[21]. Choosing the gains (29) makes the regulator in (27) mathematically equivalent to the regulator (25) with the gain selection in (26).

$$K_i = \omega_{bw} L; K_i = \omega_{bw} (R + R_a + j\omega_e L); K_i = \omega_{bw} L + R_a \quad (29)$$

## 5 Digital implementation

As explained before, synchronous current regulators are implemented digitally. The implementation can be based on 1) approximation of the continuous-time design; or 2) direct discrete-time design.

The first approach is more straightforward to apply. The continuous-time design is simply discretized by means of the Euler (or Tustin) method and the angular errors due to the computational delay and the PWM are compensated for in the coordinate transformation. However, the sampling frequency should be at least 10–20 higher than the closed-loop bandwidth and the maximum synchronous frequency. If this requirement is not fulfilled, the actual closed-loop system deviates significantly from the desired one due to discretization errors, leading to the cross-coupling between the axes, oscillations, and even instability.

In the direct discrete-time design, the exact sampled-data model of the system (including the sampling and hold effects) is first developed and the regulator is then designed directly in the discrete-time domain. The system delays can be properly taken into account, which enables significantly better performance and robustness at low sampling frequencies.

In the following, discrete-time regulators resulting from these two fundamentally different approaches are presented using the same regulator structure. The sampled-data model of the system to be controlled is first developed and a discrete-time control algorithm is then defined. The gains resulting from the two approaches are then given.

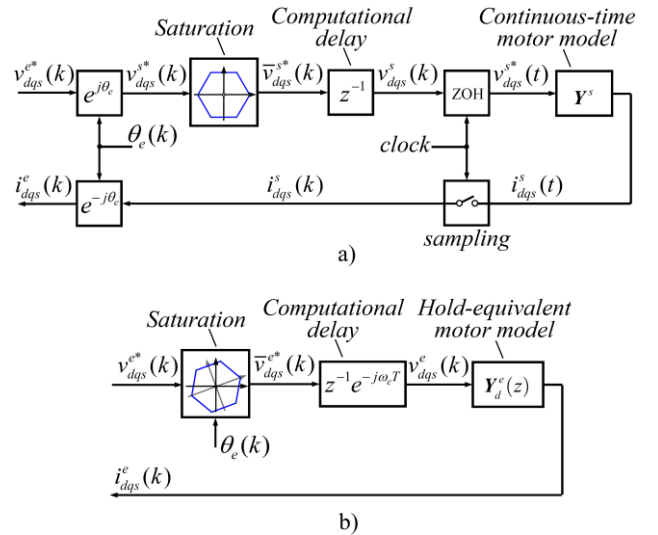


Fig. 22 (a) System seen by the digital current regulator operating in synchronous coordinates. (b) Corresponding sampled-data model. The PWM is modeled with the ZOH in stator coordinates. An inherent computational delay  $z^{-1}$  of the digital processor and the inverter voltage saturation are taken into account.

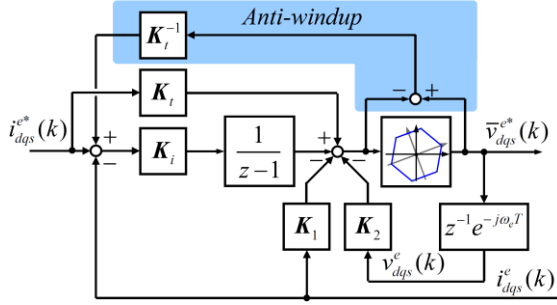


Fig. 23 Discrete-time synchronous current regulator. The anti-windup mechanism based on the realizable reference is also included.

### 5.1 Voltage saturation and sampled-data model

Fig. 22(a) shows the system seen by the digital current regulator [21]-[23]. This model includes the following important phenomena:

- The phase currents are sampled in synchronism with the PWM (cf. Fig. 8). Therefore, the switching-cycle-averaged models and quantities can be used in modeling and control design.
- The PWM is modeled using the zero-order hold (ZOH) in stator coordinates [21], [22], i.e., the actual stator voltage  $v_{dqs}^s(t)$  in stator coordinates is piecewise constant between two consecutive sampling instants.
- The inverter voltage is limited, cf. Fig. 6. The limited (realizable) voltage reference is denoted by  $\bar{v}_{dqs}^{s*}$ . If the voltage reference  $v_{dqs}^{s*}$  is inside the voltage hexagon,  $\bar{v}_{dqs}^{s*} = v_{dqs}^{s*}$  holds.
- The computation of the new voltage command takes finite time, typically less than one sampling period. The new voltage command is applied in the beginning of the next sampling period, which causes one sampling-period delay in the control system. This computational delay should be considered in the control design, unless the sampling frequency is very high compared to the bandwidth and to the synchronous frequency.

Fig. 22(b) shows a sampled-data model equivalent to Fig. 22(a). The development of the model is briefly explained in the following. In stator coordinates, the sampled current is (30), where the pulse-transfer function (31) is obtained from (10) as [20].

$$\mathbf{i}_{dqs}^s(z) = \mathbf{Y}_d^s(z) v_{dqs}^s(z) \quad (30)$$

$$\mathbf{Y}_d^s(z) = \frac{z-1}{z} \mathcal{Z} \left\{ \mathcal{L}^{-1} \left\{ \frac{\mathbf{Y}^s(s)}{s} \right\} \right\} \Bigg|_{t=kT} = \frac{1}{R} \frac{1-a}{z-a}; \quad a = e^{-(R/L)T} \quad (31)$$

Transforming this model to synchronous coordinates leads to

$$\mathbf{i}_{dqs}^e(z) = \mathbf{Y}_d^e(z) v_{dqs}^e(z) = \frac{\gamma}{z-\phi} v_{dqs}^e(z) \quad (32)$$

where  $\phi = e^{-(R/L+j\omega_e T)}$  and  $\gamma = (e^{-j\omega_e T} - \phi)/R$ . The effect of the computational delay, transformed to synchronous coordinates, is [21]-[23]

$$v_{dqs}^e(z) = z^{-1} e^{-j\omega_e T} \bar{v}_{dqs}^{e*}(z) \quad (33)$$

The model in Fig. 22(b) is directly applicable to nonsalient permanent magnet synchronous machines and to induction machines. Using the above-mentioned assumptions, the closed-form sampled-data model for salient synchronous machines is derived in [21]. The nonlinear saturation characteristics can also be included in the model [24]. The hold-equivalent models can also be expressed using the series expansions [20], [21].

### 5.2 Control algorithm

The discrete-time state-feedback control algorithm, analogous to (27), is considered

$$v_{dqi}^e(k+1) = v_{dqi}^e(k) + \mathbf{K}_i \left[ \mathbf{i}_{dqs}^{e*}(k) - \mathbf{i}_{dqs}^e(k) \right] \quad (34)$$

$$v_{dqs}^{e*}(k) = \mathbf{K}_t \mathbf{i}_{dqs}^{e*}(k) - \mathbf{K}_1 \mathbf{i}_{dqs}^e(k) - \mathbf{K}_2 v_{dqs}^e(k) + v_{dqi}^e(k) \quad (35)$$

where  $v_{dqi}^e$  is the integral state,  $\mathbf{K}_i$  is the integral gain,  $\mathbf{K}_t$  is the feedforward gain, and  $\mathbf{K}_1$  and  $\mathbf{K}_2$  are the state-feedback gains. Fig. 23 shows the corresponding block diagram, where also the anti-windup mechanism is included and it will be discussed in Section 5.6.

The computational delay increases the order of the discrete-time system as compared to the continuous-time system. However, the full-state feedback can still be easily realized using (33) and the gain  $\mathbf{K}_2$  in (35). The realizable voltage reference needed in (33) can be obtained from the PWM or it can be calculated from the simple geometry of the voltage hexagon [17], [24]. Naturally, the proper coordinate transformations between stator and synchronous coordinates are needed in both cases.

It is also worth noticing that the control algorithm given in (34)-(35) can be used for approximating the continuous-time designs, as will be further discussed in Section 5.4.

### 5.3 Closed-loop system

Using (32)-(35), the closed-loop response of the system is obtained

$$\mathbf{i}_{dqs}^e(z) = \frac{\mathbf{b}_1 z + \mathbf{b}_0}{z^3 + \mathbf{a}_2 z^2 + \mathbf{a}_1 z + \mathbf{a}_0} \mathbf{i}_{dqs}^{e*}(z) \quad (36)$$

where the coefficients depend on the motor parameters and the controller gains

$$\mathbf{a}_0 = \mathbf{K}_2 e^{-j\omega_e T} \phi + (\mathbf{K}_i - \mathbf{K}_1) \gamma e^{-j\omega_e T} \quad (37)$$

$$\mathbf{a}_1 = \phi + \mathbf{K}_1 \gamma e^{-j\omega_e T} - (1 + \phi) \mathbf{K}_2 e^{-j\omega_e T} \quad (38)$$

$$\mathbf{a}_2 = \mathbf{K}_2 e^{-j\omega_e T} - 1 - \phi \quad (39)$$

$$\mathbf{b}_0 = (\mathbf{K}_i - \mathbf{K}_1) \gamma e^{-j\omega_e T} \quad (40)$$

$$\mathbf{b}_1 = \mathbf{K}_t \gamma e^{-j\omega_e T} \quad (41)$$

The model in (36) can be used for analysis of the closed-loop response as well as the pole and zero locations

resulting from different gain selections.

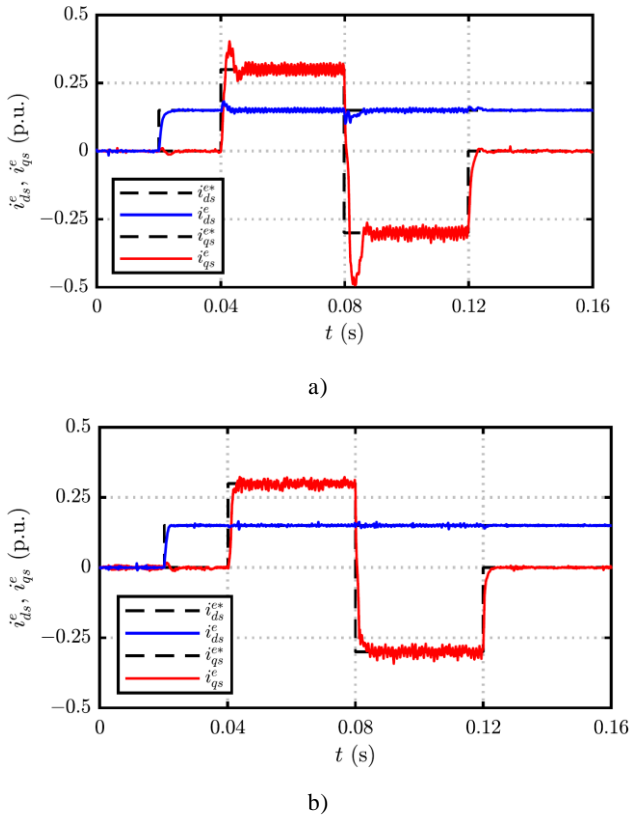


Fig. 24. Experimental results for a 6.7-kW synchronous reluctance motor drive rotating at  $\omega_e = 160 \cdot 2\pi$  rad/s: (a) continuous-time design (42)-(45) with  $\omega_{bw} = 200 \cdot 2\pi$  rad/s; (b) discrete-time design (46)-(49) with  $\omega_{bw} = 500 \cdot 2\pi$  rad/s.

#### 5.4 Approximation of the continuous time design

The gains of the discrete-time regulator (34)-(35) can be determined based on the continuous-time regulator design. When approximating continuous-time designs, the angular error of  $3/2 \omega_e T$  caused by the ZOH and computational delays should also be compensated for [25]. Embedding this compensation into the gains given in (29) yields

$$\mathbf{K}_i = \omega_{bw} L e^{j(3/2)\omega_e T} \quad (42)$$

$$\mathbf{K}_i = T \omega_{bw} (R + R_a + j\omega_e L) e^{j(3/2)\omega_e T} \quad (43)$$

$$\mathbf{K}_1 = (\omega_{bw} L + R_a) e^{j(3/2)\omega_e T} \quad (44)$$

$$\mathbf{K}_2 = 0 \quad (45)$$

When these gains are used in (35), the continuous-time integrator is approximated with the Euler method, but the control performance would be essentially the same for the Tustin method as well. The problems at low sampling frequencies originate from the delays, which are omitted in the continuous-time designs; only the angular error of the delay is compensated for in (42)-(45).

Fig. 24(a) shows example results, measured using a 6.7-kW synchronous reluctance motor drive [24]. Even if

the load is different, essentially the same design principles are used as in this paper. The cross-coupling and overshoot seen in the response originate mainly from the digital delays, even if the sampling frequency is 25 times the closed-loop bandwidth and about 30 times the synchronous speed. If the sampling frequency were increased, the response would better match the designed one.

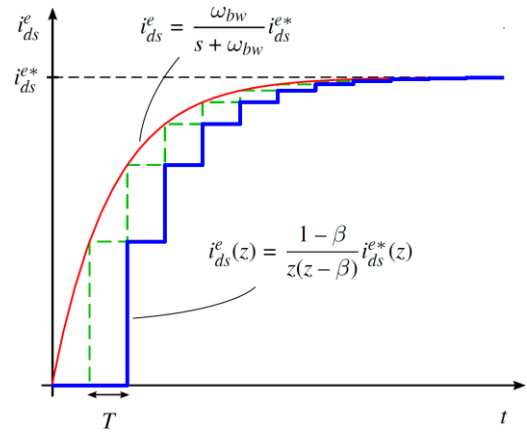


Fig. 25. Step responses of the continuous-time system (21) and the discrete-time system (51), where  $\beta = e^{-\omega_{bw} T}$ . The green dashed line shows the response of the discrete-time system without the computational delay.

#### 5.5 Direct discrete-time design

For the direct discrete-time design, the gains can be solved from (37)-(41) as

$$\mathbf{K}_i = \mathbf{b}_1 e^{j\omega_e T} / \gamma \quad (46)$$

$$\mathbf{K}_i = (1 + \mathbf{a}_0 + \mathbf{a}_1 + \mathbf{a}_2) e^{j\omega_e T} / \gamma \quad (47)$$

$$\mathbf{K}_1 = [1 + \mathbf{a}_1 + \mathbf{a}_2 + \phi(1 + \phi + \mathbf{a}_2)] e^{j\omega_e T} / \gamma \quad (48)$$

$$\mathbf{K}_2 = (1 + \mathbf{a}_2 + \phi) e^{j\omega_e T} \quad (49)$$

Due to the full-state feedback, the poles can be arbitrarily placed by choosing the characteristic coefficients  $\mathbf{a}_0$ ,  $\mathbf{a}_1$  and  $\mathbf{a}_2$ . The open-loop pole  $z = 0$ , originating from the computational delay in (33), is already in the optimal location, thus it is feasible to choose  $\mathbf{a}_0 = 0$ . The direct discrete-time equivalent of the regulator (25) is obtained by choosing the other coefficients as [21]:

$$\mathbf{a}_1 = \beta \rho \phi; \mathbf{a}_2 = -\beta - \rho \phi; \mathbf{b}_1 = 1 - \beta \quad (50)$$

where the constants  $\beta = e^{-\omega_{bw} T}$  and  $\rho = e^{-(R_a/L)T}$  are used for the exact mappings of the desired continuous-time pole locations in the discrete-time domain. This choice leads to the closed-loop response in (51). Poles are placed at (52), the last one being cancelled with the corresponding zero.

$$i_{dq_s}^e(z) = \frac{(1 - \beta)(z - \rho \phi)}{z(z - \beta)(z - \rho \phi)} i_{dq_s}^{e*}(z) = \frac{(1 - \beta)}{z(z - \beta)} i_{dq_s}^{e*}(z) \quad (51)$$

$$z = 0; \quad z = \beta; \quad z = \rho \phi = e^{-((R+R_a)/L+j\omega_e)T} \quad (52)$$

The step responses corresponding to (21) and (51) are compared in Fig. 25. Setting  $\beta = 0$  (or, equivalently, setting  $\omega_{bw}$  to infinity) would give the dead-beat response. This choice is not recommended, however, due to high sensitivity to the model parameters.

The tuning of the control system is simple, i.e., the same input parameters are needed as in the continuous-time design:  $L, R, R_a$  and  $\omega_{bw}$ . It can also be realized that the computationally complexity resulting from the direct discrete-time design (46)-(49) is not much more than that of the continuous-time design (42)-(45). Naturally, the computational efficiency of the algorithm can be optimized in the both cases as compared to the representation shown in Fig. 23.

Fig. 24(b) shows example results, measured using the discrete time design with the 6.7-kW synchronous reluctance motor drive. It can be seen that the control response matches very well the designed one. If desired, the sampling frequency could be lowered.

### 5.6 Anti-windup based on the realizable references

The current regulator should implement mechanisms for guaranteeing proper operation under voltage constraints. If the voltage reference  $v_{dqs}^{e*}$  is outside the voltage hexagon, cf. Fig. 6, the control loop becomes nonlinear. The voltage reference may exceed the limit for large current reference steps, especially at large speeds (cf. Fig. 7). This inverter voltage saturation will cause the integral state of the regulator to wind up unless some suitable anti-windup mechanism is applied.

The anti-windup mechanism can be designed based on the concept of realizable references [9], [12], [13], [26]. The unlimited (ideal) voltage reference  $v_{dqs}^{e*}$  is given by (35). If the realizable current reference  $\bar{i}_{dqs}^{e*}$  were applied to the regulator instead of  $i_{dqs}^{e*}$ , the unlimited voltage would equal the realizable voltage reference  $\bar{v}_{dqs}^{e*}$ , i.e.,

$$\bar{v}_{dqs}^{e*}(k) = \mathbf{K}_t \bar{i}_{dqs}^{e*}(k) - \mathbf{K}_1 i_{dqs}^e(k) - \mathbf{K}_2 v_{dqs}^e(k) + v_{dq1}^e(k) \quad (53)$$

The realizable current reference (54) can be solved from (35) and (53).

$$\bar{i}_{dqs}^{e*}(k) = i_{dqs}^e(k) + \frac{\bar{v}_{dqs}^{e*}(k) - v_{dqs}^{e*}(k)}{\mathbf{K}_t} \quad (54)$$

which is applied for the integrator according to Fig. 23. This mechanism has no effect in the linear modulation range where  $\bar{v}_{dqs}^{e*} = v_{dqs}^{e*}$  holds.

## 6 Conclusions

Design and implementation of synchronous PI current regulators for AC drives has been addressed in this paper. Both complex vector and state feedback approaches have been used. Tuning methodology, effects due to discretization and the associated delays, and effects due to voltage constraints have also been considered. It is

concluded that if, properly designed and tuned, synchronous current regulators can provide excellent performance even under adverse conditions (low switching frequency vs. fundamental frequency ratio). On the contrary, ignoring aspects as cross-coupling, the delays intrinsic to digital control systems, or the existence of severe voltage constraints when the drive operates at high speeds, can produce a serious degradation of the control, and even compromise its stability.

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