Realizable references anti-windup implementation for parallel controllers in multiple reference frames

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***Abstract*—Parallel controller structures are often used for the control of harmonic components in those power converters including harmonic compensation functions. The harmonic compensation can be distorted during saturation of the power converter output. This paper proposes an implementation of the realizable references anti-windup technique suitable for parallel controllers in multiple reference frames. The proposed implementation does not require a particular type of controllers nor special formulations. It allows canceling individual controller outputs during steady-state saturation to improve the waveform quality. Different saturation options are analyzed.**

I. Introduction

There is a continuous increment of non-linear loads connected to the grid in present days. Distributed power generation systems (DPGSs) have increased their presence in the grid, specially those based on renewable energies, as solar or wind energy [1]. In addition, microgrids are also increasing in size and quantity and they also feed a high percentage of non-linear loads [2]. Since the connection to the grid is realized using power converters, harmonic compensation has gained increasing importance. In addition, requirements for grid quality have been toughen in an attempt of improving general power quality [3]. This harmonic compensation can be done by means of dedicated units, as passive filters or centralized active filters [4], [5]. These add extra cost to the system. Alternatively, the distributed generation units that are connected to the grid can provide ancillary services as compensating part of these harmonics. This is possible because almost all include a power converter interface to the grid where grid voltage and currents are already measured [5]. Harmonic compensation increases the controller complexity requiring parallel structures [1]. There are different approaches to harmonic compensation. The most used are those based on proportional-resonant (PR) controllers [6], and those based on synchronous and or stationary reference-frame proportional-integral (PI) controllers [7], [8].

Despite the controller design there is always a maximum voltage available for compensation. Due to this, the controller output can exceed the maximum available voltage under heavy load conditions or if there is a sudden change of power demand. During saturated state, two problems can arise: controller wind-up and harmonic distortion.

The controller wind-up can be avoided by saturating the parallel controllers to different preset values [9]. However, this solution does not ensure an efficient voltage utilization and correct transition from saturate to non-saturate state. A back-tracking algorithm with proportionally assigned gains for each controller has been also proposed [10]. Again, the need of gain tuning makes the solution inefficient in a general case. A conditional cancelation of the multiple reference frame parallel controller integrators is proposed in [11]. It requires tuning of a voltage threshold to disable the integrators as well as calculation of the control signal derivative to enable and disable the cancelation of the different controllers. The slow dynamic response of this solution makes it inefficient for continuously varying conditions. In addition, it requires a particular controller structure. An effective realizable references anti-windup technique has been recently presented for stationary reference frame parallel controllers [12]. The implementation requires a special formulation for the controller since the controller is efficiently implemented as a single transfer function. Unfortunately, this prevents from manipulation of the individual parallel controllers outputs, which can be used to minimize harmonic distortion. Moreover, the solution cannot be used when different types of controllers are used.

Along with the windup problem, saturation also produces harmonic distortion. A trajectory analyzer is proposed in [13], [14] to limit the controller output in case of saturation and avoid harmonic injection. This analyzer is used to adapt the output voltage in stationary reference frame. The main drawback is that due to its complexity it is limited to the saturation of the fundamental and negative sequence harmonic; the compensation strategy being not injecting additional harmonics during saturation. That is not generally the case in harmonic compensation schemes. A back-tracking scheme is proposed in [15], [16] for a parallel structure based on reduced-order generalized integrators (ROGI) in multiple reference frames. When output saturation is produced, the different voltage components are adjusted following a pre-commissioned gain

This work was supported in part by the Research, Technological Development and Innovation of the Spanish Ministry Economy and Competitiveness, under grant MINECO-17-ENE2016-80047-R and by the FEDER INTERCONNECTA 2015 program under grant ITC20151130.

adjustment algorithm in such a way the less priority harmonics are removed from compensation. The main drawbacks of this method are that it requires a particular controller structure, the complex tuning process, and the dynamic performance since the gain adjustment is driven by an integral controller.

This paper proposes an universal implementation of the instantaneous realizable-references algorithm. The implementation allows to work in multiple reference frames and cancel the compensation of lower priority harmonics during saturation. Any parallel controller can be easily disabled by just setting to zero its output. The proposed implementation is not restricted to a special type of controllers, allowing to develop new controller types and combine different controllers in different reference frames. The paper also analyzes different options for the selection of the saturated voltage to minimize harmonic distortion, proposing one specially suited for grid-forming applications.

II. Realizable references for parallel controllers

A. Basic concept

The transfer function of a discrete-time controller can be expressed as (1), assuming it has the same number n of poles as zeroes.

$$D(z) = \frac{u(z)}{e(z)} = \frac{b_0 + b_1 z^{-1} + \cdots + b_n z^{-n}}{1 + a_1 z^{-1} + \cdots + a_n z^{-n}} \tag{1}$$

where u is the controller output (i.e. inverter output voltage in a current controller); e is the error signal (i.e. current error in a current controller); and b_i and a_i ($i = 1, 2, ...n$) are the polynomial coefficients. u and e can be either scalar or complex vector quantities, as well as the polynomial coefficients.

The assumption of having the same number of poles as zeroes is not very restrictive provided that all continuous-time controllers discretized using the bilinear (Tustin), matched pole-zero, first-order hold, or backward Euler approximations will meet this condition. For the zero-hold, forward euler, or modified matched pole-zero approximations this condition is not necessarily met, resulting in discrete-time transfer functions that may have one more pole than zeroes. This can be circumvented by adding $\frac{T}{2}(z+1)$ to the numerator controller, where T is the sampling period; the new controller exhibiting a very similar response. Nevertheless, the discussion will be later extended to the case the controller transfer function might have different number of poles than zeroes.

The difference equation needed for computer (e.g. microcontroller) implementation can be easily obtained (2)

$$u[k] = \sum_{i=0}^{n} b_i e[k-i] - \sum_{i=1}^{n} a_i u[k-i] \tag{2}$$

The controller output must be limited to the actuator operating range to avoid controller windup. In case of scalar output (i.e. using DC power source) a maximum and minimum voltage will be easily set (3).

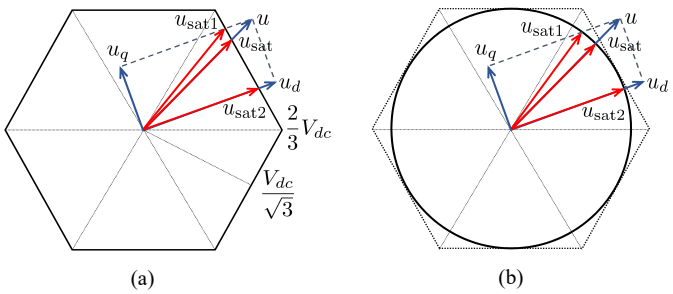

Fig. 1. Complex vector voltage limits. (a) Hexagon saturation. (b) Circle saturation.

$$u[k] = u_{\text{sat}} = \begin{cases} u_{\max}, \text{if } u[k] > u_{\max} \\ u_{\min}, \text{if } u[k] < u_{\min} \end{cases} \tag{3}$$

In case of a complex vector output (i.e. using a three-phase inverter) more complicated expressions apply. Fig. 1(a) shows the maximum allowable voltage range using a three-phase inverter. It is given by an hexagon which a circumscribed circle of radius $\frac{2}{3}V_{dc}$ and apothem $\frac{V_{dc}}{\sqrt{3}}$, being V_{dc} the DC-link voltage. When the amplitude of a voltage command u surpasses the voltage hexagon limits, its amplitude must be limited or its phase distorted. In this case, multiple options exist. The most commonly used are shown in Fig. 1(a): u_{sat} keeps the original vector angle; u_{sat1} maximizes $q-$axis component; and u_{sat2} maximizes the $d-$axis component. The hexagon limitation maximizes the inverter voltage utilization but brings implementation complexity, reference frame dependence, and the injection of additional harmonics when the voltage moves along the hexagon sides. To avoid this, the hexagon inner circle seen in Fig. 1(b) is often selected as voltage limit.

Limitation of the digital controller output to the actuator limits prevents from windup, but does not ensure a correct controller operation during the saturation state and a fast transition to normal operation when the saturation cause ceases. There exist different anti-windup mechanisms, as described in the introduction; the back-calculation or realizable references method being the most effective and straightforward for digital implementation. It consists of calculating the error signal that would have made the controller to calculate the saturated output (4). This value will be used as the previous step error signal in the next control period. This makes the controller always operate in the linear region, even under output saturation.

$$e_{\text{sat}} = \frac{1}{b_0}\left(u_{\text{sat}} - \sum_{i=1}^{n} b_i e[k-i] + \sum_{i=1}^{n} a_i u[k-i]\right) \tag{4}$$

Calculation of e_{sat} requires to recalculate the last two terms on the right side of (4), or storage of those values during the controller computation. A simpler implementation is proposed next for later extension to parallel controllers.

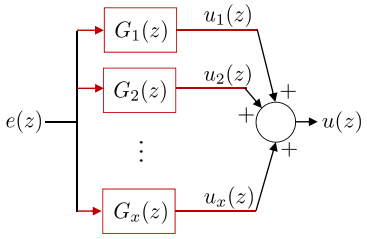

Fig. 2. Block diagram of a stationary reference frame parallel controllers' structure.

B. Efficient implementation

The controller difference equation seen in (2) can be rewritten by extracting the first polynomial coefficient out of the summation, as seen in (5).

$$u[k] = b_0 e[k] + \sum_{i=1}^{n} b_i e[k-i] - \sum_{i=1}^{n} a_i u[k-i] \tag{5}$$

In case of saturation, the saturated controller output as a function of the realizable error (i.e. realizable reference minus actual output) can be calculated as (6).

$$u_{\text{sat}} = b_0 e_{\text{sat}} + \sum_{i=1}^{n} b_i e[k-i] - \sum_{i=1}^{n} a_i u[k-i] \tag{6}$$

By subtracting (5) from (6) a simpler expression only dependent on the last terms can be obtained (7). Therefore, the realizable error can be easily calculated by only using the actual period input and output of the controller (8).

$$u_{\text{sat}} - u[k] = b_0 \left(e_{\text{sat}} - e[k]\right) \tag{7}$$

$$e_{\text{sat}} = e[k] + \frac{1}{b_0} \left(u_{\text{sat}} - u[k]\right) \tag{8}$$

C. Parallel controllers in stationary reference frame

In grid-forming, grid-connected or active filter inverters, parallel controllers are often use for the control of the fundamental current (or voltage) and its harmonics. A structure using stationary reference frame parallel controllers can be seen in Fig. 2. A back calculation or realizable reference anti-windup implementation has been proposed for a parallel structure composed of a proportional plus resonant harmonic controllers [12]. The implementation in [12] allows an independent design of the fundamental and harmonic controllers and a straightforward anti-windup computation. The drawbacks are: 1) It requires a special arrangement of the controllers; 2) The structure is fixed to proportional plus resonant controllers; 3) Individual controller outputs cannot be analyzed or limited; 4) It is only intended for controllers implemented in stationary reference frame. The anti-windup implementation proposed in this paper overcomes those limitations.

The difference equation for the individual controllers can be seen in (9). They are computed as x independent controllers, where $u_j (j = 1, 2, \cdots, x)$ are the controller outputs, and $b_{j,i}$ and $a_{j,i} (i = 1, 2, \cdots, n)$, are the discrete-time controllers' coefficients. Please, note the error signal is common for all of them.

$$u_1[k] = b_{1,0}\, e[k] + \sum_{i=1}^{n_1} b_{1,i}\, e[k-i] - \sum_{i=1}^{n_1} a_{1,i}\, u_1[k-i] \tag{9a}$$

$$u_2[k] = b_{2,0}\, e[k] + \sum_{i=1}^{n_2} b_{2,i}\, e[k-i] - \sum_{i=1}^{n_2} a_{2,i}\, u_2[k-i] \tag{9b}$$

$$\vdots$$

$$u_x[k] = b_{x,0}\, e[k] + \sum_{i=1}^{n_x} b_{x,i}\, e[k-i] - \sum_{i=1}^{n_x} a_{x,i}\, u_x[k-i] \tag{9c}$$

The total controller output is the sum of the individual controller outputs (10). An identical result is obtained by summing the controllers' difference equations in (9), resulting in the expression (11).

$$u_T[k] = \sum_{i=1}^{x} u_i[k] \tag{10}$$

$$u_T[k] = \sum_{l=1}^{x} b_{l,0}\, e[k] + \sum_{l=1}^{x}\sum_{i=1}^{n_l} b_{l,i}\, e[k-i] - \sum_{l=1}^{x}\sum_{i=1}^{n_l} a_{l,i}\, u_l[k-i] \tag{11}$$

Similarly to the single controller case, by replacing the actual output and error signal by their saturated counterparts, (12) is obtained.

$$u_{\text{sat}} = \sum_{l=1}^{x} b_{l,0}\, e_{\text{sat}} + \sum_{l=1}^{x}\sum_{i=1}^{n_l} b_{l,i}\, e[k-i] - \sum_{l=1}^{x}\sum_{i=1}^{n_l} a_{l,i}\, u_l[k-i] \tag{12}$$

Finally, by subtracting (11) from (12), and after clearing e_{sat}, (13) is obtained. The obtained result shows the error back-calculation process is as simple as for the single controller. It must be remarked that (11) does not need to be computed; the parallel implementation, (9) and (10), being used instead. Finally, the fraction of saturation voltage corresponding to each parallel controller must be calculated (14).

$$e_{\text{sat}} = e[k] + \frac{1}{\sum_{l=1}^{x} b_{l,0}} \left(u_{\text{sat}} - u_T[k]\right) \tag{13}$$

$$u_{l\_\text{sat}} = u_l[k] + b_{l,0} \left(e_{\text{sat}} - e[k]\right) \text{ for } l = 1, 2, ..., x \tag{14}$$

This implementation is advantageous since it allows disabling some harmonic controllers in case of saturation as it will be discussed in section III. Moreover, it mitigates numeric rounding errors that can arise in a single controller implementation. In a general case, the parallel controllers can be designed and implemented in different reference frames. Therefore, a realizable references anti-windup implementation for multiple reference frames will be described next.

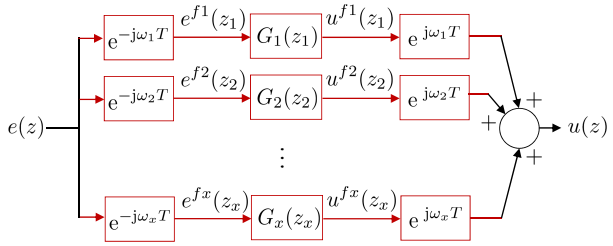

Fig. 3. Block diagram of a multiple reference frame parallel controllers' structure.

D. Parallel controllers in multiple reference frames

Different reference frames can be used for the design and implementation of the different controllers in the parallel structure as can be seen in Fig. 3. The error signal is first transformed into the multiple reference frames. Each controller produces an output in its own reference frame ; and finally, the outputs are transformed into a common reference frame (i.e. stationary) and added up. Superscript fl $(l = 1, 2, \cdots, x)$ is used to specify the different reference frames for the parallel controllers. The difference equations for the parallel controllers can be expressed as (15). After computation of the parallel controllers, the total output can be easily obtained (16).

$$u_1^{f1}[k] = b_{1,0}\, e^{f1}[k] + \sum_{i=1}^{n_1} b_{1,i}\, e^{f1}[k-i] - \sum_{i=1}^{n_1} a_{1,i}\, u_1^{f1}[k-i] \tag{15a}$$

$$u_2^{f2}[k] = b_{2,0}\, e^{f2}[k] + \sum_{i=1}^{n_2} b_{2,i}\, e^{f2}[k-i] - \sum_{i=1}^{n_2} a_{2,i}\, u_2^{f2}[k-i] \tag{15b}$$

$$\vdots$$

$$u_x^{fx}[k] = b_{x,0}\, e^{fx}[k] + \sum_{i=1}^{n_x} b_{x,i}\, e^{fx}[k-i] - \sum_{i=1}^{n_x} a_{x,i}\, u_x^{fx}[k-i] \tag{15c}$$

$$u_T[k] = \sum_{i=1}^{x} u_i[k] = \sum_{i=1}^{x} u_i^{fi}[k]\, \mathrm{e}^{\,j\theta_i[k]} \tag{16}$$

By summing the difference equations in (15) after transforming them to a stationary reference frame, (17) can be obtained.

$$\begin{aligned} u_T[k] = &\sum_{l=1}^{x} b_{l,0}\, e^{fl}[k] \mathrm{e}^{\,j\theta_l[k]} + \sum_{l=1}^{x} \left(\sum_{i=1}^{n_l} b_{l,i}\, e^{fl}[k-i] \right) \mathrm{e}^{\,j\theta_l[k]} \\ &- \sum_{l=1}^{x} \left(\sum_{i=1}^{n_l} a_{l,i}\, u_l^{fl}[k-i] \right) \mathrm{e}^{\,j\theta_l[k]} \end{aligned} \tag{17}$$

By writing the synchronous reference frame error signal in (17) in terms of the stationary reference frame error signal (18), equation (19) is obtained. This expression contains both the total controller output and the actual sample error signal in stationary reference frame.

$$e^{fl}[k] = e[k] \mathrm{e}^{-\,j\theta_l[k]} \tag{18}$$

$$\begin{aligned} u_T[k] = &\sum_{l=1}^{x} b_{l,0}\, e[k] + \sum_{l=1}^{x} \left(\sum_{i=1}^{n_l} b_{l,i}\, e^{fl}[k-i] \right) \mathrm{e}^{\,j\theta_l[k]} \\ &- \sum_{l=1}^{x} \left(\sum_{i=1}^{n_l} a_{l,i}\, u_l^{fl}[k-i] \right) \mathrm{e}^{\,j\theta_l[k]} \end{aligned} \tag{19}$$

Following the same thought process as in stationary reference frame, both the actual voltage and error signal can be replaced by the saturated versions (20). By substracting (19) from (20), and after clearing e_{sat}, equation (13) is again obtained. Therefore, there is not difference in the calculation of the realizable error signal between the implementation in stationary or multiple reference frames. However, a final step is required in this case to provide the realizable error signal in each of the multiple reference frames (21).

$$\begin{aligned} u_{\mathrm{sat}} = &\sum_{l=1}^{x} b_{l,0}\, e_{\mathrm{sat}} + \sum_{l=1}^{x} \left(\sum_{i=1}^{n_l} b_{l,i}\, e^{fl}[k-i] \right) \mathrm{e}^{\,j\theta_l[k]} \\ &- \sum_{l=1}^{x} \left(\sum_{i=1}^{n_l} a_{l,i}\, u_l^{fl}[k-i] \right) \mathrm{e}^{\,j\theta_l[k]} \end{aligned} \tag{20}$$

$$e_{\mathrm{sat}}^{fl} = e_{\mathrm{sat}}\, \mathrm{e}^{-\,j\theta_l[k]} \text{ for } l = 1, 2, ..., x \tag{21}$$

The saturation voltage corresponding to each controller in the parallel structure can be then calculated similarly to the stationary reference frame case (22).

$$u_{l\_\mathrm{sat}}^{fl} = u_l^{fl}[k] + b_{l,0} \left(e_{\mathrm{sat}}^{fl} - e^{fl}[k] \right) \text{ for } l = 1, 2, ..., x \tag{22}$$

E. Controllers with different number of poles and zeroes

The former expressions assume each controller discrete-time transfer function has the same number of poles as number of zeroes. Please, note this does not mean all the controllers in the parallel structure must have the same number of poles. However, similar results can be obtained if the controllers have different number of poles than zeroes while all of them have the same pole/zero difference (23). Otherwise, a more complex and unpractical saturation scheme should be derived.

$$n_1 - m_1 = n_2 - m_2 = \cdots = n_x - m_x \tag{23}$$

where m_l are the number of zeroes of controllers $l = 1, 2, ..., x$.

III. Saturation strategies

The previous section has demonstrated the realizable references anti-windup technique can be easily implemented in case of parallel controllers with independence of the reference frame. This technique ensures a fast transition from saturated to non saturated state. However, this does not imply a correct harmonic compensation during the saturated state. As it was described in the introduction, several researchers [13], [14],

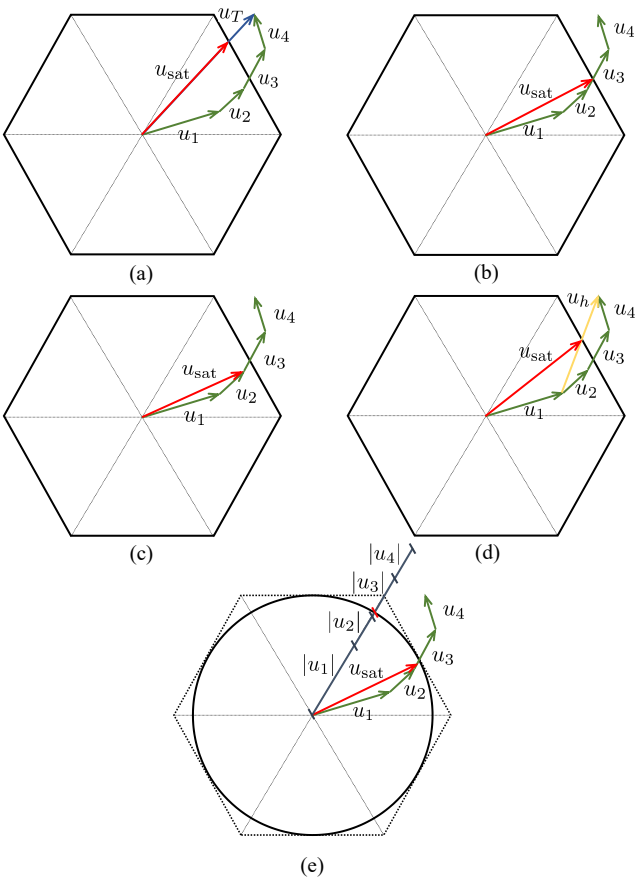

Fig. 4. Saturation options analyzed: (a) Global saturation. (b) Incremental saturation 1. (c) Incremental saturation 2. (d) Group saturation. (e) Magnitude-based saturation.

[15], [16] have dealt with the problem of harmonic distortion during saturation. The use of the realizable references technique will further simplify the introduction of compensation mechanisms but the harmonic distortion will depend on the selection of the saturated complex vector. As it was seen in Fig. 1, multiple saturation options exist when the controller output magnitude exceeds the hexagon limits. In case of parallel controllers, increased number of options exist. Fig. 4 shows the options analyzed in this paper. It is considered that four parallel controllers would provide four voltage commands to exemplify the different analyzed options. The controllers are sorted (and numbered) in order of importance regarding the harmonic compensation, being u_1 the fundamental component.

Fig. 4(a) shows the first option. In this case, the resulting vector addition of the parallel controllers is compared with the hexagon limits. Since the magnitude exceeds the limits, the output voltage will be limited to the hexagon but keeping the original angle. This is expected to generate significant harmonic distortion during saturation, but it is taken as reference since is the simplest approach and offers the best voltage utilization.

Fig. 4(b) shows another option in which the saturated voltage is calculated from the first component crossing the hexagon limit. The remaining voltage components are disregarded. A modified version is shown in Fig. 4(c). The same idea applies, but the saturated vector is calculated also rejecting the component crossing the hexagon limit. These solutions can be seen as instantaneous versions of those proposed in the literature [11], [15], [16] where the harmonic controllers are dynamically disabled when saturation is detected.

A fourth approach can be seen in Fig. 4(d). The different components are grouped in two: the fundamental u_1 and the vector addition of the remaining voltages u_h. A similar saturation technique to that described for Fig. 4(b) is then applied. This and the previous methods will be also tested using the hexagon inner circle as voltage limit.

The last approach, seen in Fig. 4(e), offers the worst voltage utilization, but it is included since it offers a similar philosophy to those methods that decrease the harmonic controller gains when saturation is detected. In this case the magnitude of the voltage components coming from the controllers are summed and compared with the hexagon inner circle. The magnitude of the first voltage component crossing the inner circle will be limited, and the higher order or less important components disregarded. This solution theoretically eliminates any inter-modulation issue during saturation at steady-state.

Once the saturated vector is calculated following one of the proposed methods, no special treatment must be done to the controllers which outputs are disregarded, since the back-calculation method described in the previous section will automatically disable them in practice.

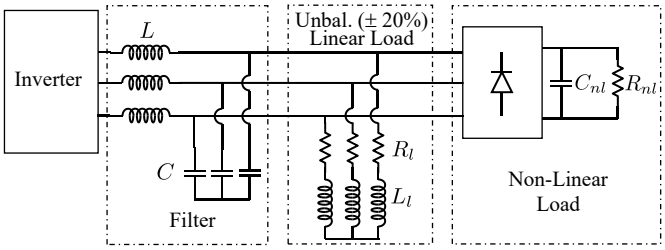

Fig. 5. Test system.

IV. System under test

The distortion introduced by the different methods will depend both on the saturation level and on the type of loads present in the system. A grid forming scenario has been used to test the described alternatives. Fig. 5 shows a three-phase inverter with an output LC filter, an unbalanced three-phase linear load, and a non-linear load. The main system parameters can be found in Table I. The linear and non-linear loads draw about 40 % and 35 % of the rated power respectively.

The inverter control goal is to obtain a balanced three-phase voltage at the filter output. The necessary current to achieve this goal can be easily calculated by replacing the inverter and the filter inductor L by an ideal three-phase source. Fig. 6(a) shows the current needed to obtain the voltage trajectory at the filter capacitor shown in Fig. 6(c). It is also possible to

TABLE I
SYSTEM PARAMETERS

Rated voltage	V_r	400 V_{rms}
Rated current	I_r	144 A_{rms}
Filter	L	260 µH
Filter	C	270 µF
Linear load	R_l	3.36 Ω
Linear load	L_l	6.6 mH
Linear load	Unbalance	±20%
Non-linear load	C_{nl}	1 mF
Non-linear load	R_{nl}	8.35 Ω

calculate the inverter voltage trajectory to achieve both the inverter current and the capacitor voltage, as seen in Fig. 6(b).

To produce the trajectories seen in Fig. 6(a)-(c) an unrealistic bandwidth would be needed for the current controller. Assuming a parallel controller structure composed of a fundamental current controller, a negative sequence current controller, and five harmonic controllers the trajectories seen in Fig. 6(d)-(f) are considered. They include the fundamental voltage at 50 Hz and harmonics at -250, 350, -50, -550, 650, -850 Hz in decreasing order of magnitude. The resulting capacitor voltage shown in Fig. 6(f) shows a small total harmonic distortion (THD) of 0.74 %.

If voltage saturation is produced the previous trajectories will be distorted. The following sections will analyze the resulting capacitor voltage trajectory when the different methods described in previous section are used. First, open-loop tests using the voltage trajectory seen in Fig. 6(e) will be carried out. This avoids the interaction on the current controller and the time to recover from saturation to better understand the different saturation options. Later, closed-loop current control will be enabled to analyze the interaction of the current controller and the validity of the proposed realizable references implementation. Three levels of saturation are imposed assuming DC-link voltages of 600, 570, and 540 V. The corresponding hexagon limits can be seen in Fig. 7.

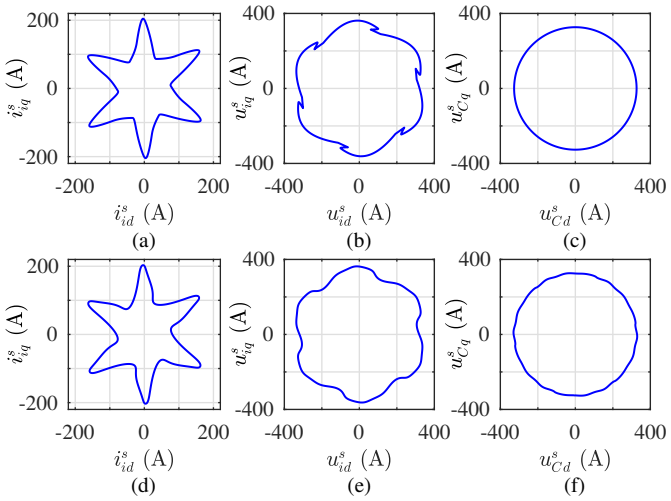

Fig. 6. Current and voltage trajectories for the system under test. (a),(d): Inverter current. (b),(e): Inverter voltage. (c),(f): Capacitor voltage. (a)-(c): Unlimited bandwidth. (d)-(f): Considering fundamental a six main harmonics.

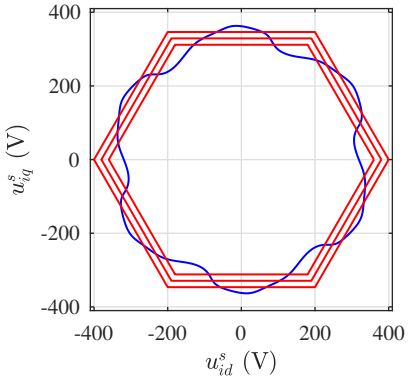

Fig. 7. Non-saturated inverter voltage trajectory and voltage limits.

V. Open-loop tests

The different saturation strategies described in section III are tested in simulation. The inverter seen in Fig. 5 is simplified using a linear voltage source to speed up the simulations assuming a sampling frequency of 10 kHz. The voltage trajectory seen in Fig. 7 is the inverter voltage command before saturation. The measured capacitor voltage total harmonic distortion (THD), fundamental voltage magnitude error, and the voltage phase angle are taken as figures of merit for the different methods. The phase angle is given in respect to the non-saturated case, which its trajectory seen in Fig. 6(f).

Table II summarizes the obtained results. It can be seen that the "Group" strategy proposed in this paper [see Fig. 4(d)] gives the best (i.e. smallest values) results. Using the circle as the voltage limit provides a slightly better THD but an increased magnitude error than with the hexagon. The angle difference respect to the non-saturated case is negligible in all cases. The "Global" strategy [see Fig. 4(a)] offers the second best results for both the circle and hexagon limits, and it has the benefit of being the simplest for computer implementation. The "Incremental" strategies [see Fig. 4(b,c)] do not provide good results; this, in addition to their increased complexity makes them to be discarded for the closed-loop tests. The "Magnitude-based" strategy [see Fig. 4(e)], despite its simplicity, does not offer good results and it is also disregarded. It is noted that the discarded methods are the most similar to those reported in the literature [15], [16], [11].

VI. Closed-loop tests

The validity of the proposed anti-windup algorithm is analyzed in combination with some of the described saturation strategies. The current trajectory seen in Fig. 6(c) is commanded to a current controller following a parallel structure composed of seven complex vector synchronous frame PI controllers [17] for the fundamental, negative sequence and main five harmonic components. Each controller is independently tuned in its own reference frame. In addition, the measured ca-

TABLE II
CAPACITOR VOLTAGE DISTORTION USING DIFFERENT SATURATION STRATEGIES FOR OPEN-LOOP INVERTER VOLTAGE INJECTION.

	600 V			570 V			540 V		
Method	THD (%)	Mag. Error (%)	Angle (deg)	THD (%)	Mag. Error (%)	Angle (deg)	THD (%)	Mag. Error (%)	Angle (deg)
Global (circle)	2.14	1.27	0	2.98	4.34	0	3.84	8.45	-0.01
Global (hexagon)	2.17	0.99	0	4.1	3.25	0.01	5.04	6.43	0
Incremental 1 (circle)	4.47	1.27	0.32	3.35	4.34	0.53	6.32	8.44	0.13
Incremental 1 (hexagon)	4.01	1.02	0.22	3.68	3.20	0.41	5.9	5.61	0.41
Incremental 2 (circle)	3.04	1.96	0.28	3.35	4.34	0.53	6.32	8.44	0.13
Incremental 2 (hexagon)	3.39	1.63	0.22	3.62	3.22	0.44	5.9	6.22	0.43
Group (circle)	1.87	1.26	0.25	2.59	4.57	0.57	2.54	10.06	0.61
Group (hexagon)	2.04	0.91	0.14	3.71	3.18	0.47	4.94	6.47	0.59
Magnitude	3.03	1.53	0.4	3.35	4.34	0.53	6.32	8.44	0.13

TABLE III
CAPACITOR VOLTAGE DISTORTION USING DIFFERENT SATURATION STRATEGIES FOR CLOSED-LOOP INVERTER CURRENT INJECTION.

	600 V			570 V			540 V		
Method	THD (%)	Mag. Error (%)	Angle (deg)	THD (%)	Mag. Error (%)	Angle (deg)	THD (%)	Mag. Error (%)	Angle (deg)
Global (circle)	2.99	2.16	-0.19	5.85	6.8	-1.17	7.48	11.15	-2.38
Global (hexagon)	3.01	1.54	-0.05	6.25	6.24	-0.56	9.45	10.82	-1.53
Group (circle)	1.99	2	0.93	4.27	6.23	0.93	7.49	10.39	-0.64
Group (hexagon)	2.21	1.48	0.669	4.22	5.21	2.14	6.33	9.26	2.45
No real. references	5.78	-0.36	2.34	7.18	4.52	-4.59	5.78	8.78	-5.73
No state saturation	5.11	2.89	1.42	15.66	11.68	3.25		Unstable	

pacitor voltage is used as feedforward term. This feedforward signal and the output of the fundamental current controller will be considered as the fundamental voltage component for the saturation strategy implementation. It is noted the feedforward term can also contain harmonic content during transients and in steady-state if a low harmonic distortion is not achieved.

The capacitor voltage THD using this controller and assuming no saturation is 0.92 %, and the fundamental voltage component magnitude error is 0.1 %. When inverter voltage saturation is present the results shown in Table III are obtained.

Slightly increased values compared to those obtained for the open-loop inverter voltage are obtained. This is explained by both the controller bandwidth and the time to recover from saturation even when the realizable references technique is implemented. Nevertheless, the comparative results are similar to the case of open-loop inverter voltage injection. The "Group" strategy using the hexagon limit has been found again to provide excellent results.

To prove the validity of the described anti-wind up technique the "Group" hexagon saturation strategy was also implemented without any anti-windup algorithm in two cases. One, calculating the individual output voltages after saturation according to the given strategy (see "No real. references" in Table III); the second, limiting only the global controller output according to the same strategy but not calculating the individual outputs (see "No state saturation" in Table III). The results are clearly worst than for the case in which the anti-windup technique is enabled. However, the THD and magnitude error for the particular case of 540 V are better in case of only state saturation ("No real. references"). This is explained by the largely increased capacitor voltage phase delay. It will be next seen how the injected current also contains an increased delay respect to the case in which the anti-windup is enabled. This would provide poor results in case a capacitor voltage control loop were used.

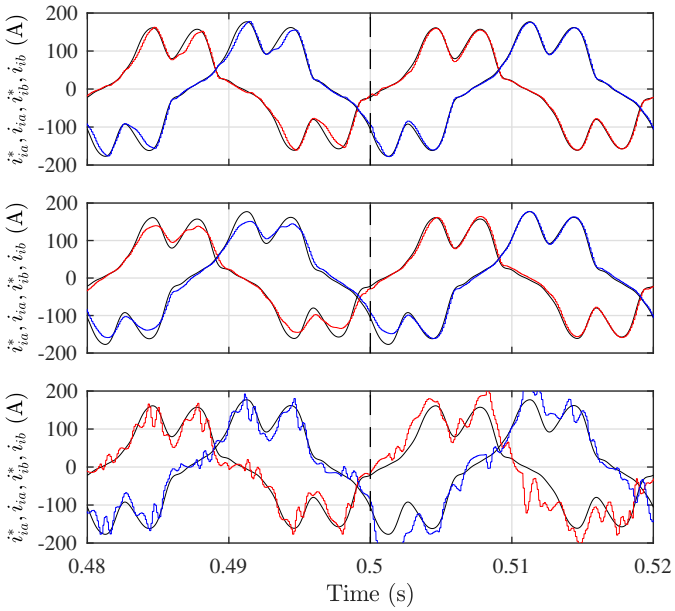

Fig. 8. Inverter phase a and b currents showing the transition from 570 V DC-link (saturation) to 700 V DC-link (no saturation) at 0.5 s using the "group" hexagon saturation strategy. Top: Realizable references. Middle.: individual controller state saturation. Bottom: Global output saturation. Black: current commands. Red: Phase-a current. Blue: Phase-b current.

Despite the selection of the saturation method, the proposed realizable references implementation for parallel controller structures makes straightforward the correct operation of the controller during saturation.

Fig. 8 shows the phase-a and b currents during the transition from a DC-link voltage of 570 V (i.e. saturation) to 700 V (i.e. no saturation) at 0.5 s when the proposed anti-windup

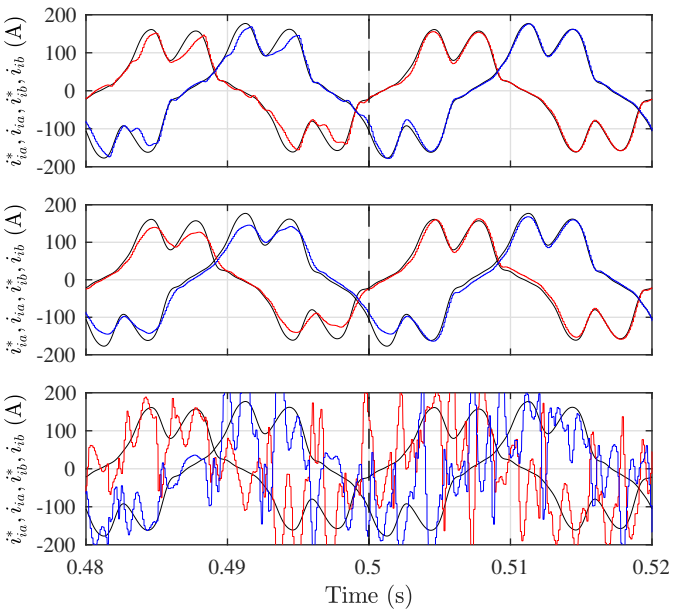

Fig. 9. Inverter phase a- and b- currents showing the transition from 540 V DC-link (saturation) to 700 V DC-link (no saturation) at 0.5 s using the "group" hexagon saturation strategy. Top: Realizable references. Middle: individual controller state saturation. Bottom: Global output saturation. Black: current commands. Red: Phase-a current. Blue: Phase-b current.

technique is enabled (top), when only the output voltage of each parallel controller is calculated (middle), and when only the global output saturation voltage is computed (bottom). It can be seen that during saturation (before 0.5 s) the realizable reference algorithm provides the best current tracking. Saturating only the individual controllers produces higher tracking error. Oscillations are noticeable is case of only limiting the total controller output. Once the DC-link voltage increases the realizable references algorithm provides the fastest transition to the non-saturated state. The transition time is higher, but acceptable, in case of individual controller output limitation, and extremely long (> 0.4 s, not seen in Fig. 8) in case of global output limitation.

In case of a higher saturation this results become more apparent. Fig. 9 shows the transition from a reduced DC-link of 540 V to 700 V showing the same signals as in Fig. 8. In this case the same comments can be made, but the global saturation case makes the current control unstable. Moreover, the system cannot recover from the unstable state once the DC-link voltage increases. It is also noted the better tracking performance of the realizable reference algorithm during saturation although the resulting delayed and smoother current waveform of the individual controller saturation case results in the lower capacitor voltage THD reported in Table III. This fact opens opportunities to new saturation strategies that need to be further investigated.

VII. Conclusion

This paper develops and demonstrates a simple way of implementing the realizable references anti-windup technique for parallel controllers in multiple reference frames. The proposed implementation allows to use any kind of controller and, if required, natural modification of single controller outputs during saturation. Different saturation options are available. Grouping the harmonic controllers outputs shows excellent results. Simulation results demonstrate the feasibility and performance of the proposed anti-windup implementation.

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