UNIVERSITY OF OVIEDO

Department of Electrical Engineering

Ph.D. Programme in Energy and Process Control

Ph.D. THESIS DISSERTATION

Topologies and Control Strategies of Multiport Modular Multilevel Converters

Mario López Medina

December 2018

UNIVERSIDAD DE OVIEDO

Departamento de Ingeniería Eléctrica, Electrónica, de Computadores y Sistemas

Programa de Doctorado en Energía y Control de Procesos

TESIS DOCTORAL

Topologías y Estrategias de Control de Convertidores Modulares Multinivel Multipuerto

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Dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy at the University of Oviedo

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Gijón, December 2018

Acknowledgements

First of all, I would like to express my gratitude to my supervisor Prof. Fernando Briz for his continuous support and advice during the development of this thesis. Without his help, infinite patience and knowledge, this work would not have been possible.

I would like to address my thanks to the Power Electronics, Machines and Control group from the University of Nottingham and in particular to the head of group Prof. Jon Clare and my co-supervisor, Dr. Ralph Feldman, for giving me the opportunity to stay and work in their group. I would also like to thank other members of the group for their friendly welcome.

Furthermore, I wish to show my sincere thanks to all my friends and colleagues in the lab, Chema, Enrique, Mariam, Carlos, Alberto, for their continuous and unconditional support. They know this has not been an easy path and without their help, I would not be writing these words right now.

Finally, I would like to thank my parents and my close friends for their patience, encouragement and understanding. This work is somehow theirs as well.

Abstract

Reducing the dependence on conventional fossil fuels has become a priority for industrialized countries due to environmental concerns, limited resources and the progressive increase of their cost. This scenario has pushed the penetration of renewable energies in the existing electric power system. However, massive integration of renewable energy into the existing and future grids poses major challenges, as a significant part of the installed capacity will be connected to the distribution levels. Innovative solutions based on high-power, high-voltage electronic power converters, like High Voltage Direct Current (HVDC), Flexible AC Transmission Systems (FACTS) and Solid State Transformers (SST) have the potential to cope with these challenges.

Multilevel converters are well suited for medium-high voltage and power ranges which are required for electronic power converters connected to medium voltage electrical grids. Among these, Modular Multilevel Converters (MMCs) appear as a promising topology for applications requiring a high voltage DC port. MMCs, which was first introduced one decade ago [47]-[49], realizes a bidirectional DC/AC power conversion. It shares those advantages intrinsic to multilevel converters, but adds some additional attractive features, such as modularity, scalability and distributed energy storage, therefore eliminating the need of a bulk DC capacitor.

This thesis covers both the MMC topology and Solid State Transformers mainly derived from MMC topology. Operational features such as modulation strategies, capacitor voltage balancing methods and control of the converter are covered. A thorough analysis and classification of existing circulating current control strategies is presented. Additionally, the MMC converter is also studied under abnormal operating conditions affecting to its voltage margins, such us transients in the DC or the AC ports voltages, or failures of one or more cells. Under these circumstances, the MMC can be forced to operate in the overmodulation region. Voltage limits and overmodulation techniques are discussed in this work.

Conventional MMCs use cells consisting of a half-bridge and a capacitor. Control and modulation strategies developed for MMCs are aimed to balance the power between the AC and DC ports, which is needed to maintain the average voltage of the cells capacitors at its target value. It is possible however to transfer (absorb or deliver) power through the MMC cells. This enables new potential features, including distributed energy storage; integration of distributed energy resources (DER) at the cell level; and multiport multilevel power converters combining different low/high AC/DC ports, eventually leading to an MMC-based Solid State Transformer topology.

This work proposes the modification of conventional cells in the Modular Multilevel Converter to provide power transfer capability and thus, the transformation of this topology into the so-called MMC-based multiport power converter. Such multiport power converter can be asymmetric and symmetric, depending on the number and location of cells transferring power. Both options are covered in this thesis including their analysis, control strategies and limits of operation.

Glossary

Acronyms

AC	Alternating current
ADC	Analog-to-digital converter
ARM	Acorn RISC machine
Btu	British thermal unit
CHB	Cascaded H-bridge converter
CS	Current sensor
DAB	Dual active bridge
DC	Direct current
DER	Distributed energy resources
DSBC	Double star bridge cells
DSCC	Double star chopper cells
DSP	Digital signal processor
EMI	Electromagnetic interference
EV	Electric vehicle
FACTS	Flexible AC transmission system
FB	Full bridge
FC	Flying capacitor converter
FPGA	Field-programmable gate array
HB	Half bridge
HF	High frequency
HV	High voltage
HVAC	High voltage alternating current
HVDC	High voltage direct current
IGBT	Insulated gate bipolar transistor
IPD	In-phase disposition

I/O	Input/Output
LF	Low frequency
LFT	Line frequency transformer
LV	Low voltage
LVAC	Low voltage alternating current
LVDC	Low voltage direct current
MMC	Modular multilevel converter
M2C	Modular multilevel converter
MMCC	Modular multilevel cascade converter
MOSFET	Metal-oxide semiconductor field-effect transistor
MV	Medium voltage
MVDC	Medium voltage direct current
NSF	National science foundation
NPC	Neutral point clamped converter
OF	Optical fiber
PET	Power electronic transformer
PHEV	Plug-in hybrid electric vehicle
POD	Phase-opposite disposition
PWM	Pulse width modulation
RISC	Reduced instruction set computing
RMS	Root mean square
SDBC	Single delta bridge cells
SiC	Silicon carbide
SoC	System on a chip
SSBC	Single star bridge cells
SST	Solid state transformer
STATCOM	Static synchronous compensator
SVM	Space vector modulation
THD	Total harmonic distortion
UPFC	Unified power flow controller
UPS	Uninterruptible power supply
VS	Voltage sensor
ZVS	Zero voltage switching

Nomenclature

C_{cell}	Cell capacitance
$cos\phi$	Power factor
d_{xjT}	Top arm cell j ($j = 1 : N_{MMC}$) duty cycle in phase x (x=u,v,w)
d_{xjB}	Bottom arm cell j ($j = 1 : N_{MMC}$) duty cycle in phase x (x=u,v,w)
d	DAB phase shift in pu
k	Number of voltage levels between two output phases
i_{dc}	DC-port current
i_i	Input current in the DAB
i_o	Output current in the DAB
i_{LK}	Current through the DAB leakage inductance
i_{cu}	Circulating current flowing through phase u
i_{cv}	Circulating current flowing through phase v
i_{cw}	Circulating current flowing through phase w
i_{uT}	Top arm current in phase u
i_{vT}	Top arm current in phase v
i_{wT}	Top arm current in phase w
i_{uB}	Bottom arm current in phase u
i_{vB}	Bottom arm current in phase v
i_{wB}	Bottom arm current in phase w
i_u	AC-port phase u current
i_v	AC-port phase v current
i_w	AC-port phase w current
i_{ac}	AC-port current complex vector
${i_{ac}}^*$	AC-port current complex vector conjugate
i_T	Top arm current complex vector
i_B	Bottom arm current complex vector
i_c	Circulating current complex vector
i_{cDC}	DC component of circulating current complex vector
i_d	d-axis component of AC port current vector
i_q	q-axis component of AC port current vector
i_{cell}	Current entering the cell from DAB
L_{arm}	Arm inductance

M	Relation between output and input voltage in DAB
M_f	Number of faulty cells per arm in MMC
M_t	Number of cells transferring power per arm
m	Number of voltage levels in any phase of the converter with respect to the middle point of the DC bus
m_i	Modulation index
N	Middle point in the DC bus
N_{CHB}	Number of submodules per phase in CHB
N_{MMC}	Number of submodules per arm in MMC
n	Transformer turns ratio
P_T	Top arms power
P_B	Bottom arms power
P_{dc}	DC-port active power
P_{ac}	AC-port active power
P_u	Cells power in phase u
P_v	Cells power in phase v
P_w	Cells power in phase w
P_{uT}	Top arm cells power in phase u
P_{uB}	Bottom arm cells power in phase u
P_{vT}	Top arm cells power in phase v
P_{vB}	Bottom arm cells power in phase v
P_{wT}	Top arm cells power in phase w
P_{wB}	Bottom arm cells power in phase w
P_{jT}	Top arm cell j ($j = 1 : N_{MMC}$) active power
P_{jB}	Bottom arm cell j ($j = 1 : N_{MMC}$) active power
$P_{celljxT}$	Power from cell j ($j = 1 : N_{MMC}$) in top arm of phase x (x=u,v,w)
$P_{celljxB}$	Power from cell j ($j = 1 : N_{MMC}$) in bottom arm of phase x (x=u,v,w)
P_{dc1T}	DC power from all cells that transfer power in top arm
P_{dc2T}	DC power from conventional cells in top arm
P_{dc1B}	DC power from all cells that transfer power in bottom arm
P_{dc2B}	DC power from conventional cells in bottom arm
P_{ac1T}	AC power from all cells that transfer power in top arm
P_{ac2T}	AC power from conventional cells in top arm
P_{ac1B}	AC power from all cells that transfer power in bottom arm

P_{ac2B}	AC power from conventional cells in bottom arm
P_{cell1T}	Power from all cells that transfer power in top arm
P_{cell2T}	Power from conventional cells in top arm
P_{cell1B}	Power from all cells that transfer power in bottom arm
P_{cell2B}	Power from conventional cells in bottom arm
P_{cell}	Power transferred by a complex vector cell including top and bottom arms
$P_{cell-total}$	Total power transferred by the cells
P_{DAB}	Power transferred by the DABs
P_{DABj}	Power transferred by an individual DAB
Q_{ac}	AC-port reactive power
R_{arm}	Arm resistance
R_x	Ratio between AC port and DC port voltage
v_{cell}	Cell capacitor voltage
$v_{celljxT}$	Top arm cell j ($j = 1 : N_{MMC}$) capacitor voltage in phase x (x=u,v,w)
$v_{celljxB}$	Bottom arm cell j ($j = 1 : N_{MMC}$) capacitor voltage in phase x (x=u,v,w)
v_{celljx}	Cell j ($j = 1 : 2N_{MMC}$) capacitor voltage in phase x (x=u,v,w)
v_{dc}	DC-port voltage
v_{LK}	Voltage drop in the DAB leakage inductance
v_i	Input voltage in the DAB
v_o	Output voltage in the DAB
v_{uT}	Top arm cells voltage in phase u
v_{vT}	Top arm cells voltage in phase v
v_{wT}	Top arm cells voltage in phase w
v_{uB}	Bottom arm cells voltage in phase u
v_{vB}	Bottom arm cells voltage in phase v
v_{wB}	Bottom arm cells voltage in phase w
v_u	AC-port phase u voltage
v_v	AC-port phase v voltage
v_w	AC-port phase w voltage
v_{jxT}	Top arm cell j ($j = 1 : N_{MMC}$) voltage in phase x (x=u,v,w)
v_{jxB}	Bottom arm cell j ($j = 1 : N_{MMC}$) voltage in phase x (x=u,v,w)
v_n	Voltage applied to the neutral star point in CHB

v_{ac}	AC-port voltage complex vector
v_T	Top arm complex vector cells voltage
v_B	Bottom arm complex vector cells voltage
v_{grid}	Grid voltage complex vector
v_L	Arm inductance voltage complex vector
v_{Lx}	Arm inductance voltage in phase x (x=u,v,w)
v_{jT}	Top arm cell j ($j = 1 : N_{MMC}$) voltage complex vector
v_{jB}	Bottom arm cell j ($j = 1 : N_{MMC}$) voltage complex vector
v_d	d-axis component of AC port voltage vector
v_q	q-axis component of AC port voltage vector
v_{dc1T}	DC voltage from all cells that transfer power in top arm
v_{dc2T}	DC voltage from conventional cells in top arm
v_{dc1B}	DC voltage from all cells that transfer power in bottom arm
v_{dc2B}	DC voltage from conventional cells in bottom arm
v_{ac1T}	AC complex voltage vector from all cells that transfer power in top arm
v_{ac2T}	AC complex voltage vector from conventional cells in top arm
v_{ac1B}	AC complex voltage vector from all cells that transfer power in bottom arm
v_{ac2B}	AC complex voltage vector from conventional cells in bottom arm
v_{acT}	AC complex voltage vector from all cells in top arm
v_{acB}	AC complex voltage vector from all cells in bottom arm
v_{dcT}	DC voltage from all cells in top arm
v_{dcB}	DC voltage from all cells in bottom arm
v_{acTd}	Real part of AC complex voltage vector from all cells in top arm
v_{ac1Td}	Real part of AC complex voltage vector from all cells that transfer power in top arm
v_{ac2Td}	Real part of AC complex voltage vector from conventional cells in top arm
v_{acTq}	Imaginary part of AC complex voltage vector from all cells in top arm
v_{1T}	Complex cell voltage accounting for all cells that transfer power in top arm
v_{2T}	Complex cell voltage accounting for conventional cells in top arm

v_{1B}	Complex cell voltage accounting for all cells that transfer power in top arm
v_{2B}	Complex cell voltage accounting for conventional cells in bottom arm
v_{acjxT}	Top arm cell j ($j = 1 : N_{MMC}$) AC voltage in phase x (x=u,v,w)
v_{acjxB}	Bottom arm cell j ($j = 1 : N_{MMC}$) AC voltage in phase x (x=u,v,w)
v_{jxT}	Top arm cell j ($j = 1 : N_{MMC}$) voltage in phase x (x=u,v,w)
v_{jxB}	Bottom arm cell j ($j = 1 : N_{MMC}$) voltage in phase x (x=u,v,w)
Δv_{dc}	DC voltage imbalance
Δv_{ac}	AC voltage vector imbalance
ΔP_{cell}	Variation in the power transferred by cells
$\Delta Re(v_{ac})$	Real part of AC voltage vector imbalance
Δv_{dc1T}	DC voltage imbalance from all cells that transfer power in top arm
$\Delta Re(v_{ac1T})$	Real part of AC voltage vector imbalance from all cells that transfer power in top arm
φ_{grid}	Grid voltage vector angle
φ	Angle between AC port voltage and current complex vectors
ω_e	Fundamental frequency

Superscripts

$\overline{x}$	DC component
x^*	Commanded value

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Chapter 1

Introduction

1.1 Background

The current energy scenario is suffering from a deep change. Reducing the dependence on conventional fossil fuels has become a priority for industrialized countries due to environmental concerns, limited resources and the progressive increase of their cost. This scenario has lead the governments to assign large resources in the seek for cleaner and cheaper energy sources as well as the maximum efficiency in every energy conversion process.

The increasing penetration of renewable energies, as well as more demanding requirements in terms of efficiency and reliability in the electrical network leads to a big challenge, as a significant part of the installed capacity will be connected to the distribution levels in the near future.

It is in this scenario where power power electronics makes its appearance. Innovative operational equipment based on power electronics and capable to be connected to the medium voltage grids, able to provide several functions to the power operator, such as controlling power flow, reduction in transmission losses and power quality improvement among others will be needed, example of this being HVDC and FACTS technologies.

Multilevel converters are well suited for medium-high voltage/power ranges which are required for electronic power converters connected to medium voltage electrical grids. Among the different multilevel topologies, the Modular Multilevel Converters (MMCs) appear as a promising topology for applications requiring a high voltage DC port (e.g. HVDC). While they share the appealing properties of other multilevel configurations, they offer some interesting and useful features. As a result of this, the MMC has become a

hot research topic nowadays.

The aim of this thesis has been focused on the study and analysis of the MMC topology, including topological, control and modulation aspects. In particular, the design of new topologies derived from the original MMC configuration aiming to achieve a multiport structure has been considered.

1.2 Framework

The content of this dissertation is framed within the research activities on multilevel power converters developed by the Electric Drives and Power Converters research group (AECP) of the Department of Electrical Engineering of University of Oviedo.

Design, modeling and control of electric machines has been the main topic of this research group, finding in sensorless control its main success. Supervision and diagnosis of electrical machines, flywheels based on magnetic bearings, microgrids and digital signal processing are or have also been research topics. The present thesis is born within a new line of research in the group regarding the design and control of multiport multilevel power converters.

The present work was supported in part by the Research, Technological Development and Innovation Programs of the Spanish Ministries of Science and Innovation and of Economy and Competitiveness, under grants MICINN-10-CSD2009-00046 and MINECO-13-ENE2013-48727-C2-1-R, and by the European Commission FP7 Large Project NMP3-LA-2013-604057, under grant UE-14-SPEED-604057

1.3 Objectives

The core of the this thesis is focused on the design of medium voltage multiport modular multilevel converter topologies and their control strategies. Specific objectives are defined as follows:

- Study and detailed analysis of the Modular Multilevel Converter topology: control and modulation strategies
- Study and analysis of Solid State Transformers
- Design of new topologies derived from the MMC. In particular, these

topologies will be based on the development of cells with power transfer capability

- Modification of conventional MMC topology into a multiport arrangement able to combine the medium/high voltage DC and AC ports of the MMC with low voltage DC and AC ports
- Design of control and modulation strategies for the MMC-based multiport topologies
- Application of the new multiport topologies and control strategies in Solid State Transformers
- Development of prototypes suitable for partial verification of the concepts developed in this thesis

1.4 Document structure

This thesis has been structured in five chapters and two appendices, as follows:

In chapter 1, an introduction to the work has been presented, including the main objectives and lines to be followed.

Chapter 2 is dedicated to the introduction of multilevel power converters and it highlights its importance in the current energy network scenario. Different multilevel converter topologies are presented and analyzed, also including both classical and novel approaches. It ends with the introduction of the Solid State Transformer concept, addressing a classification of these kind of converters and a brief study about the Dual Active Bridge (DAB) converter and its operation.

In chapter 3, state-of-the-art of Modular Multilevel Converters is addressed. Principles of operation, modeling and power balance equations of the MMC are analyzed in detail. Special focus is given to its distinguishing feature: the circulating current. Modulation strategies and capacitor voltage balancing methods are firstly studied and after that, control of the MMC is deeply covered, focusing on the different approaches for circulating current control. Operation of the MMC under voltage constraints and its use for variable-speed drive applications are also studied.

Chapter 4 addresses the modification of conventional cells in the Modular Multilevel Converter to provide power transfer capability and thus, the transformation of this converter into MMC-based multiport power converters, which are covered next. A classification of these converters is also

proposed attending to the number and location of cells transferring power. Limits of operation of cells with power transfer capability are studied in detail, including mathematical analysis and development of specific control strategies. The proposed methods are confirmed by means of simulation. A certain multiport modular multilevel converter topology is chosen as the basis for a Solid State Transformer arrangement. Practical implementation of the control for this topology is then included. To conclude, a comparative analysis between CHB and MMC-based multiport power electronic transformers is presented.

In chapter 5, the work developed along this thesis is summarized, including final conclusions, contributions and possible future work.

Finally, appendix A is dedicated to the experimental setups and the results of different tests while appendix B includes the publications derived from the work of this thesis.

Chapter 2

Multilevel Power Converters and Solid State Transformers

In this chapter, the need for novel power converter topologies in the current energy scenario is firstly introduced. Then, different multilevel converter topologies are presented and analyzed including both classical and novel approaches. To conclude, Solid State Transformers are also addressed, providing a deep background and a classification based on the number of energy conversion stages.

2.1 The new power-electronics-based energy network scenario

Primary energy consumption is continually growing every year (see Fig. 2.1). This fact eventually leads to an unavoidably change in the current energy scenario.The strong dependence on fossil fuels and the progressive increase of their cost is leading to the investment of huge amounts of resources, both economical and human, to develop new cheaper and cleaner energy resources, not directly related to fossil fuels [11] as well as to seek for the maximum efficiency in every energy conversion process. In this context, the electric power industry is undergoing deep technical, economical and organizational changes. Fig. 2.2 shows the installed power capacity in Spain during the period 2004-2018, with renewable energy sources as well as combined cycle power plants gaining an increased importance.

Traditionally, the electric power sector has been characterized by a vertical structure, with large power generation units, transmission/distribution

and trading [1]. The liberalization process has resulted in the unbundling of this organizational structure, where the different stages might be organized in separate business entities that can compete with each other. As a consequence, the stress on the electric system is considerably bigger than in the past, with many networks been pushed near their technical limits. The efficient use of the available infrastructure is therefore of prime interest to the network operator.

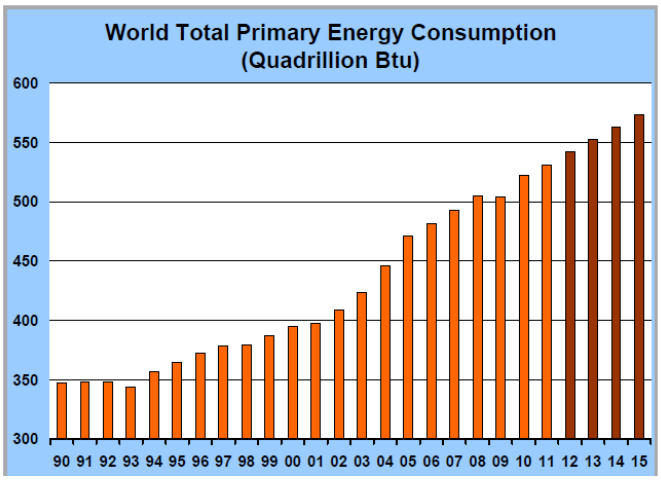

Figure 2.1: World total energy consumption expressed in Quadrillion Btu along the period from 1990-2015 [3]

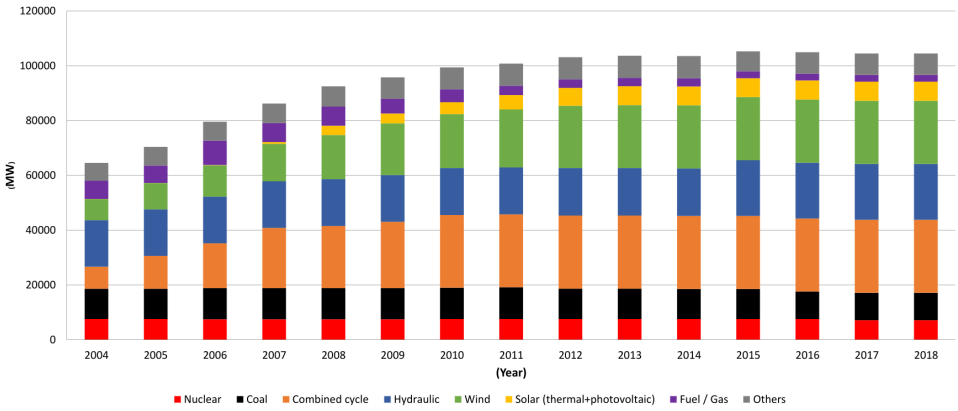

Figure 2.2: Installed power capacity in Spain (MW) during the period 2004-2018 distributed between different energy sources [4]

In this scenario, efficiency and renewable energy have both become of prime interest for the governments of developed countries. Fig. 2.3 shows the installed capacity of different renewable energy sources in Spain during the period between 2002 and 2016. As it can be observed, installed capacity,

especially wind energy, is continuously growing. Spanish government has set an installed generation capacity of renewable energy of 140000 GWh as an objective for year 2020 [5].

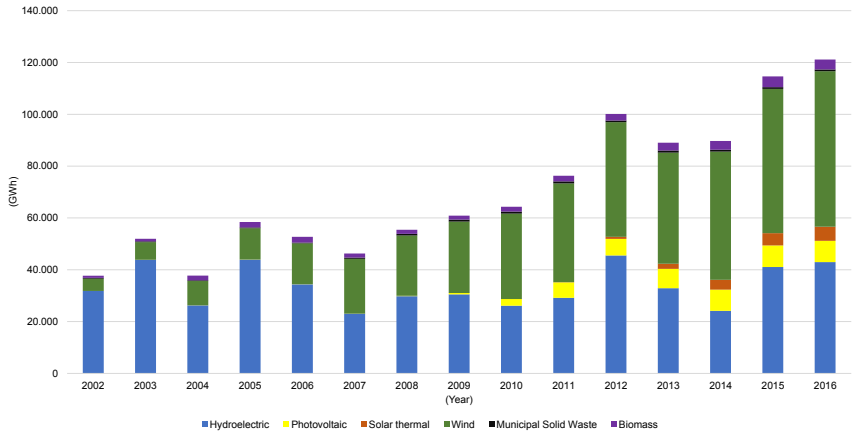

Figure 2.3: Renewable energy generation capacity in Spain (GWh) during the period 2002-2016 distributed between different energy sources [5]

This increase in renewable energy sources has forced the traditional planning approaches for power networks to go through a reinvention process. The long lasting experience with the power unidirectionally flowing from the power plants to the customers is no longer valid. Growing volatility and an increasing unpredictability of the system behavior, especially as the generation side due the massive use of renewable resources, requires innovative equipment to successfully handle such situations [1]. The introduction of distributed generation units close to the customers is changing the functionality and the requirements of the distribution networks. The grid operator is requested to provide access to the network to stakeholders in a transparent and non-discriminatory manner.

The necessity to design electric power networks, maximizing their power transfer capability, while minimizing the costs, leads to a great engineering challenge [1]. It is in this scenario where power electronics are called to play a key role. Innovative operational equipment based on power electronics can be present at all the stages in modern electric power networks:

- In the generation area, power electronics plays a key role in renewable generation systems. Photovoltaic generation require basically power conversion from DC to AC. Wind energy requires the use of variable speed drives to achieve the maximum efficiency in the wind energy capture process. Small hydrogenerators also obtain benefits from the use of variable speed drives. Also in the storage side, in the coming

decades, widespread use of various energy storage technologies is expected in the near future as capacitor, including batteries, flywheels, supercapacitors, superconducting magnet technologies and fuel cells [2]. All these technologies require the use of electronic power converters.

- In the transmission stage, modern applications of power electronics include High Voltage Direct Current transmission systems (HVDC) and Flexible AC Transmission Systems (FACTS). FACTS devices can be utilized to increase the transmission capacity, improve the stability and dynamic behavior of the electric grid, ensure better power quality and adequate interconnection of renewable and distributed generation and storage resources [1]. On the other hand, the main role of HVDC concerns the interconnection of electric grids in those cases in which the use of AC transmission reveals inadequate. This technology is mainly applied to submarine cables, long distance overhead transmission, underground transmission and connecting AC systems of different frequencies [2].

- In the distribution area, an exciting opportunity called "Custom Power" enables solutions to deliver reliable electric service to the industrial and commercial customers. This term comprises the whole area of power conditioning technology used by customers under the term of Power Quality. Uninterruptible power supplies (UPS) and voltage regulators represent a major growth area in power electronics [2]. On the other hand, the integration of battery electric vehicles into the grid draws a totally new scenario, in which the vehicles can provide grid support or even become a new player, able to buy or sell the energy stored in the batteries, according to the needs and price of the electricity.

- In the end-use side, use of power electronic converters has been steadily growing for more than two decades. Efficient lighting, computers, communications, lasers, visuals, sound, robots, medical tools, and of course variable speed drives are examples of applications in which electronic power converters are always present. Massive introduction of Electric Vehicles (EV) and Plug-In Hybrid Electric Vehicles (PHEV) will also lead to large consumptions that must be considered in the near future.

Additionally, the development of the smart grid concept should not be forgotten (see Fig.2.4). The smart power grid distributed energy system would contribute to the infrastructure required for the massive integration of distributed renewable sources. Smart grids are expected to improve the efficiency an reliability of metropolitan load centers, prevent the complete blackout of the interconnected power systems due to either man-made or

environmental events, and would provide the ability to separate the interconnected power systems into smaller clusters [7].

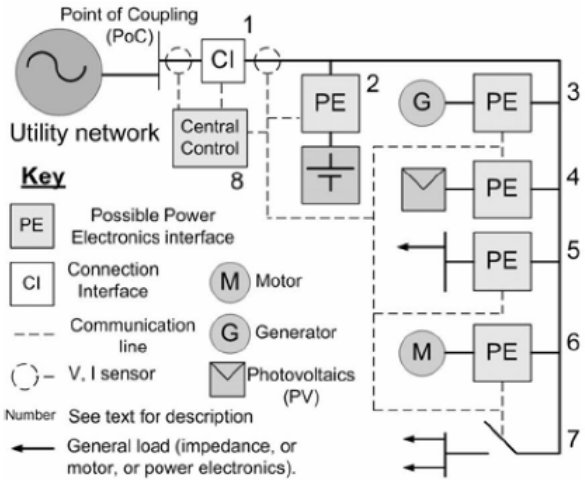

Figure 2.4: Potential Microgrid System Technologies [10]

In the aforementioned search for efficiency in power systems, the big industrial consumers must be taken into account. In fact, there is a remarkable place for efficiency improvement in the field of electric motor driven applications. The medium voltage (MV) drives cover power ratings from 0.4 MW to 40 MW at the medium voltage level of 2.3 to 13.8 kV. Most of the existing MV drives are in the 1 to 4 MW range with voltage ratings from 3.3 kV to 6.6 kV [8]. One of the major markets for the MV drive is precisely to retrofit existing applications with line connected machines, to improve the motor efficiency. It is reported that 97% of the currently installed MV motors operate at a fixed speed, i.e. only 3% of them are fed from variable speed drives [8]. When fans or pumps are driven by a fixed speed motor, the control of air or liquid flow is normally achieved by conventional mechanical methods, such as throttling control, inlet dampers, and flow control valves, resulting in a substantial efficiency decrease [8].

2.2 Multilevel Converters

The need of electronic power converters able to connect either to medium voltage grids, or to feed medium voltage motors or other medium voltage loads, has triggered the development of new power converter topologies as well as new semiconductors able to cope with such voltage levels. Design of such medium-high voltage power converters can be approached using classic power converter topologies and high-voltage semiconductors, or modular

converter topologies using low-medium voltage power devices [11], as shown in Fig. 2.5. It should be mentioned that Fig.2.5 not only refers to medium and high power semiconductors but also to medium and high voltage ones.

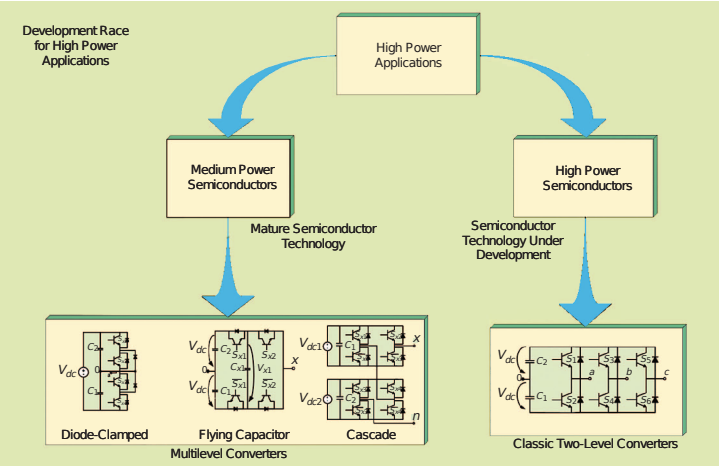

Figure 2.5: Two-level power converters versus most common multilevel power converters [11].

Generally speaking, any three-phase DC-AC power converter can be considered as "multilevel" when it is able to generate a phase-to-phase output phase voltage consisting of more than three levels [9]. In general, the number of voltage levels between two output phases (k) is given by (2.1), being m the number of voltage levels in any phase of the converter with respect to the middle point of the DC bus [9][15]. It is noted however that a physical DC bus might not exist for some types of multilevel topology (e.g. CHB converter).

$$k = 2 \cdot m - 1 \tag{2.1}$$

2.2.1 Motivation and Main Features of Multilevel Converters

Motivation for multilevel converters mainly responds to two different needs:

1. *High voltage (and high power) converters built using relatively low voltage power devices:*

   This first kind of converter appears to solve the problems related to a design based on using conventional circuits, serializing/parallelizing

power switches. The latter is difficult to implement practically, since voltage/current sharing between the devices often represents a challenging task. The main application field for high voltage/power converters is mainly centered on high power machine drives and power converters for grid applications such as HVDC, FACTS.

2. *High output frequency converters with low switching frequency power devices:*

   If a high output frequency converter is needed, a conventional 2-level solution has limited possibilities due to the device switching frequency imposes restrictions. On the contrary, for a multilevel converter, the effective switching frequency can be higher than the individual device switching frequency. Thus, it can produce low THD waveshapes with relatively low switching frequencies. High output frequency converters are appealing e.g. for very high speed motor drives, compressors, etc.

The most relevant features of multilevel power converters can be summarized as follows:

- Voltage sharing among devices will be handled automatically by the topology
- Multilevel waveform will lead to reduced harmonic distortion for a given switching frequency
- Increasing converter operating voltage (power rating) without the need of connecting devices in series
- Reduction of Electromagnetic Interference (EMI) due to smaller voltage steps and thus, lower filtering requirements and less insulation stress
- Generating smaller common-mode voltages, thus reducing the stress e.g. in the motor bearings for the case of electric drives[15]

2.2.2 Review of Multilevel Topologies

A patent search carried out in [15] showed that multilevel power converters have been around for more than 40 years. An early traceable patent appeared in 1975 [18], in which the cascaded inverter was first defined with a format that connects DC-sourced full-bridge cells in series to synthesize a staircase AC output voltage [15]. Through manipulation of the cascade

inverter, with diodes blocking the sources, the diode-clamped multilevel inverter was then derived.

The most popular multilevel converter topologies are the neutral point clamped converter (NPC), flying capacitor converter (FC) and cascaded H-bridge converter (CHB) [11], they are briefly described following.

2.2.2.1 Neutral Point Clamped (NPC) Converter

The diode-clamped converter, also called the neutral-point clamped converter, was first used in a three-level converter in which the mid-voltage level was defined as the neutral point [15]. In 1981, A. Nabae, I. Takahashi, and H. Akagi presented the first NPC pulse width modulation (PWM) converter [19].

This kind of converter is based on a modification of the classic two-level converter topology adding two new transistors and four diodes per phase, as shown in Fig. 2.6.

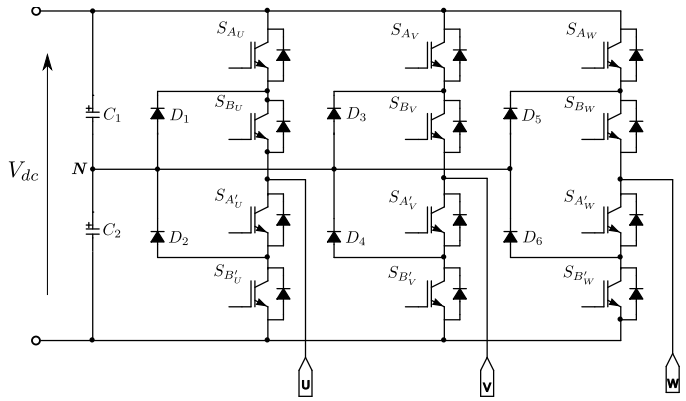

Figure 2.6: Three-level Neutral Point Clamped (NPC) converter

In this circuit, the DC bus voltage is split two halves by means of two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors (N) is taken as the neutral point. The three-level NPC in Fig. 2.6 is able therefore to produce an output voltage V_{xN} with three states: $V_{dc}/2$, 0 and $-V_{dc}/2$.

A significant difference of this topology with respect to the conventional 2-level converter are the diodes ($D_1 ... D_6$). Diodes of the same leg clamp the switch voltage to half the level of the DC bus voltage. E.g., when S_{AU} and S_{BU} are closed, D_2 balances the voltage sharing between S'_{AU} and S'_{BU} with S'_{AU} blocking the voltage across C_1 and S'_{BU} blocking the voltage across C_2.

Without the presence of these diodes, the output voltage levels would not be defined. Table 2.1 shows the different switching states for the three level output phase-to-neutral voltage.

V_{xN}	A	B	A'	B'
$V_{dc}/2$	1	1	0	0
0	0	1	1	0
$-V_{dc}/2$	0	0	1	1

Table 2.1: Switching states 3-level NPC converter.

The configuration shown in Fig.2.6 can be theoretically extended to any number of voltage levels. Fig.2.7 shows one phase of a five-level NPC converter.

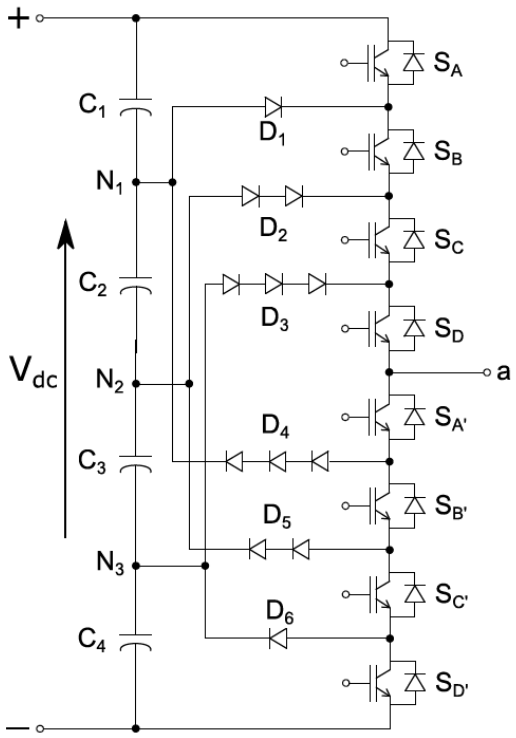

Figure 2.7: Five-level Neutral Point Clamped (NPC) converter. Phase a.

In this arrangement, the DC bus is split among four capacitors C_1,C_2,C_3 and C_4, each one withstanding $V_{DC}/4$. Thanks to the blocking diodes, each switching device just withstands the voltage corresponding to one capacitor. Unlike the three-level case, not all the diodes handle the same voltage. As the number of levels increases, some of them must withstand the voltage corresponding to several series-connected capacitors. If all the diodes are

identical, i.e. same blocking voltage, some of them must be consequently serialized.

Table 2.2 shows the different switching states for the five level output phase-to-neutral voltage. It is noted that there are four pair of switches with complementary switching states: (S_A, S'_A),(S_B, S'_B), (S_C, S'_C) and (S_D, S'_D).

Output voltage	A	B	C	D	A'	B'	C'	D'
$V_{aN_2} = V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{aN_2} = V_{dc}/4$	0	1	1	1	1	0	0	0
$V_{aN_2} = 0$	0	0	1	1	1	1	0	0
$V_{aN_2} = -V_{dc}/4$	0	0	0	1	1	1	1	0
$V_{aN_2} = -V_{dc}/2$	0	0	0	0	1	1	1	1

Table 2.2: Switching states 5-level NPC converter.

To conclude, NPC converters offer some attractive advantages, such as:

- This topology only requires one isolated DC supply.
- Unlike other multilevel topologies, it needs a reduced number of capacitive elements, simplifying therefore the control as there is less capacitor with voltage balancing requirements [21].

However, there are several aspects which need to be considered for its design and control:

- While for the case of the three-level NPC, capacitor voltages can be balanced by appropriate selection of switching patterns, this is not possible for topologies with more than 3 levels. Extra balancing circuitry is therefore needed in this case, or alternatively multiple DC supplies. In both cases the complexity and cost of the power converter significantly increases [9].
- As the number of levels increases, some diodes have to block large voltages. This situation makes the topology unattractive for more than 5 levels. Consequently, and assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be (m-1)x(m-2), being "m" the number of levels in the phase-to-neutral output voltage. This number represents a quadratic increase in m. When the number of levels increases, the number of diodes required will make the system impractical [15].

- This topology is not modular, i.e. increased voltage levels cannot be achieved by simply piling up identical modules.
- Asymmetry in its working conditions. Conduction times are unequal for the different devices leading to different losses and therefore, different temperature rises. This will add complexity to the cooling system design [12][9].

2.2.2.2 Capacitor-Clamped (Flying Capacitor) Converter

This topology was first proposed in 1992 for the medium voltage application range [22]. In this arrangement, the voltage sharing between the switches is not made by the diodes, but by means of capacitors (C_3, C_4 and C_5), i.e., independent capacitors clamp the device voltage to one capacitor voltage level. Fig. 2.8 shows a three-level flying capacitor topology. Similarly to the NPC converter, this topology is able to generate an output phase voltage consisting of three levels: $V_{dc}/2$, 0 and $-V_{dc}/2$.

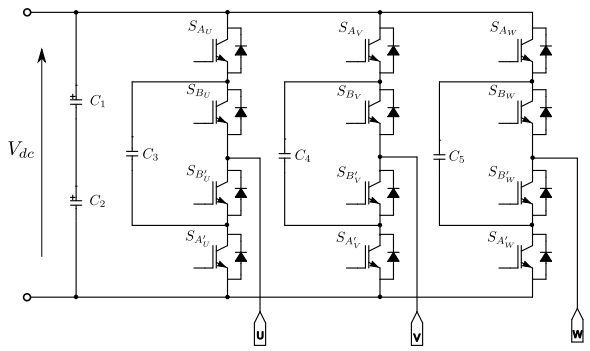

Figure 2.8: Three-level Flying Capacitor Converter.

Table 2.3 shows the different switching states for the three level case. Unlike the 3-level NPC topology, there are different switching states able to generate the zero voltage.

V_{xN}	A	B	B'	A
$V_{dc}/2$	1	1	0	0
0	1	0	1	0
0	0	1	0	1
$-V_{dc}/2$	0	0	1	1

Table 2.3: Switching states 3-level Flying Capacitor Converter.

A distinctive feature of this topology concerns the capacitors voltage balancing, which is absolutely necessary to assure a proper operation of

the converter. As an example in the 3-level arrangement, capacitor C_3 is charged when S_{AU} and $S_{B'U}$ are turned on, and it is discharged when S_{BU} and $S_{A'U}$. By proper selection of the 0-level switch combination, the charge of the capacitors can be controlled.

Similarly to the NPC topology, FC arrangement is not strictly modular. In order to increase the number of levels, there are no identical modules to be piled up. Depending on their place on the arrangement, capacitors will withstand different voltages, serialization being therefore needed (i.e. if identical capacitors are considered). Figure 2.9 shows a 5-level FC converter while Table2.4 includes the different switching states for the aforementioned topology. As it can be noticed, there are redundant states, i.e. multiple switching combinations produce the same output voltage. This feature is essential for capacitor voltage balancing [15].

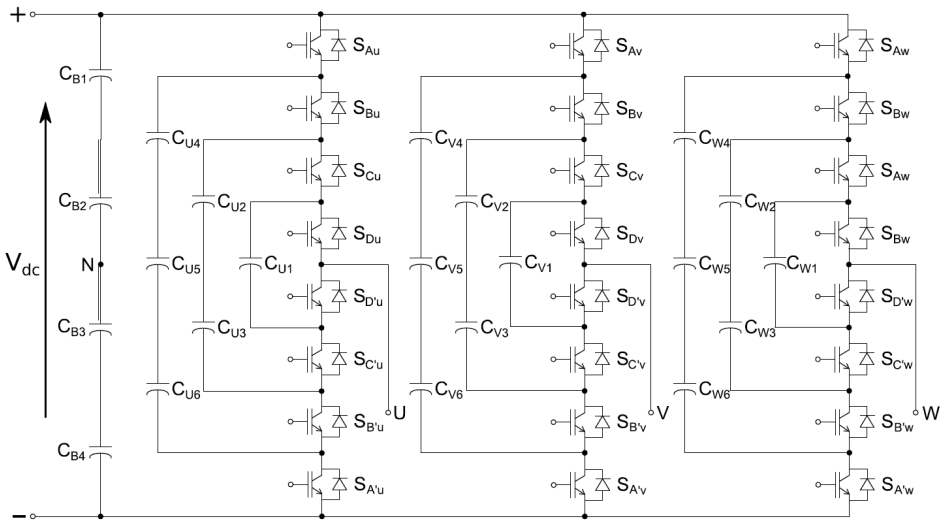

Figure 2.9: Five-level Flying Capacitor Converter.

To summarize, this topology presents some relevant advantages:

- Similar to the NPC case, only a single DC power supply is required
- The voltage sharing between the devices is guaranteed as long as the clamping capacitors are kept charged at the right voltage. Unlike the NPC topology, where high voltage diodes are eventually required, no high voltage silicon devices are needed in this case
- Redundant states offer great flexibility in the capacitor voltage balancing [15]

V_{xN}	A	B	C	D	A'	B'	C'	D'
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	1	1	1	0	0	0	0	1
$V_{dc}/4$	1	1	1	0	1	0	0	0
$V_{dc}/4$	1	0	1	1	0	1	0	0
0	1	1	0	0	0	0	1	1
0	0	0	1	1	1	1	0	0
0	1	0	1	0	0	1	0	1
0	1	0	0	1	0	1	1	0
0	0	1	0	1	1	0	1	0
0	0	1	1	0	1	0	0	1
$-V_{dc}/4$	1	0	0	0	0	1	1	1
$-V_{dc}/4$	0	0	0	1	1	1	1	0
$-V_{dc}/4$	0	0	1	0	1	0	1	1
$-V_{dc}/2$	0	0	0	0	1	1	1	1

Table 2.4: Switching states 5-level FC converter.

However, the following disadvantages can be mentioned:

- Clamping capacitors need to be pre-charged at a certain voltage
- The switching strategy has to consider the need of balancing the clamping capacitors voltage, meaning that some kind of feedback mechanism has to be implemented. It must be noted that capacitor voltage balancing is not possible when the load is purely reactive [17]
- As the number of level increases, the number of capacitors required increases near exponentially. Similar to diode clamping, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor is the same as that of the main power switch, a m-level converter will require a total of (m-1)x(m-2)/2 clamping capacitors per phase leg [15].
- Redundancy is difficult to be implemented since this topology is not fully modular. In order to increase the number of levels, modules being piled up are not identical. Depending on their place on the arrangement, capacitors will withstand different voltages, serialization of identical capacitors being therefore needed

2.2.2.3 Cascaded H-Bridge (CHB) Converter

The CHB converter is a particular case of a cascaded converter, based on the series connection of H-bridge cells [15] as those shown in Fig. 2.10-a, where (S_1,S_2) and (S_3,S_4) present complementary switching states. A five-level CHB converter is shown in Fig. 2.10-b.

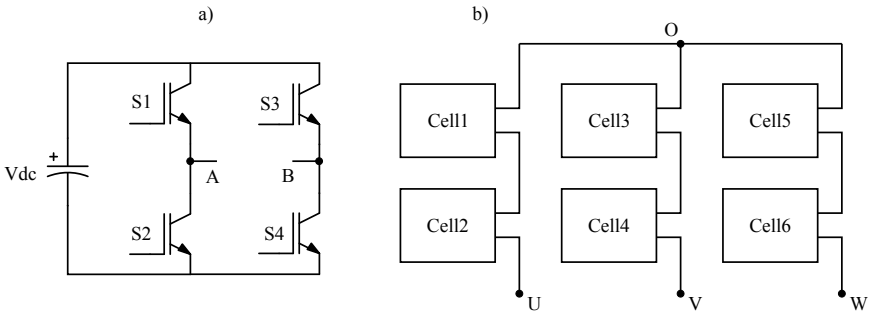

Figure 2.10: a) Individual H-Bridge cell. b) 5-level Cascaded H-Bridge converter

Each cell can produce three voltage levels of with values V_{dc}, 0 and $-V_{dc}$, the output phase voltage being the combined result of the voltage generated by all the cells in that phase. By series connection of N_{CHB} cells per phase, the output phase voltage (V_{U0}) presents $2N_{CHB}+1$ levels and the phase-to-phase voltage (V_{UV}) is made from $4N_{CHB}+1$ levels. In the case of Fig. 2.10, the output phase voltage can present the following voltage levels: $2V_{dc}$, V_{dc}, 0, $-V_{dc}$ and $-2V_{dc}$ [15].

Similarly to the NPC and FC topologies, Table 2.5 shows the switching states for the 5-level arrangement. For simplicity, only phase U has been shown. Subindexes c_1 and c_2 refers to the number of cell. It is noted that the complementary switching states from $S2$ and $S4$ have not been included.

As it can be observed, redundant states also exist in this topology. These states are very useful to keep the voltage balancing between the cell capacitors. These algorithms are in general based on choosing the adequate cell as a function of the required output phase voltage and the phase current direction.

Unlike the NPC and FC converters, CHB topology in its general representation is not a DC/AC converter, as it does not provide a high voltage DC link but it is distributed along the cells. The cell DC bus often consists of a capacitor with limited energy storage capabilities which eventually means that this kind of converter can not handle active power transfer but only reactive power and harmonics. The main application for this case is focused on active power filters. In case active power transfer is required, each cell must include an isolated DC supply which is usually obtained from an

V_{U0}	$S1_{c1}$	$S3_{c1}$	$S1_{c2}$	$S3_{c2}$
$2 \cdot V_{dc}$	0	1	0	1
V_{dc}	0	1	0	0
V_{dc}	0	0	0	1
V_{dc}	1	1	0	1
V_{dc}	0	1	1	1
0	1	1	1	1
0	0	0	0	0
0	0	1	1	0
0	1	0	0	1
0	1	1	0	0
0	0	0	1	1
$-V_{dc}$	1	0	0	0
$-V_{dc}$	1	0	1	1
$-V_{dc}$	0	0	1	0
$-V_{dc}$	1	1	1	0
$-2 \cdot V_{dc}$	1	0	1	0

Table 2.5: Switching states 5-level CHB converter. Phase u

isolated AC supply and a diode bridge. This usually leads to complex transformer arrangements (i.e. multipulse transformer arrangements) in order to reduce harmonic content in the input AC current [8].

To conclude, this topology provides some very attractive advantages:

- Voltage sharing between switching devices is intrinsic to the cell design and limited to the cell voltage
- Allows redundancy by simply using more cells per phase than it is actually required
- High voltage is achieved by just connecting identical cells
- The circuit is completely modular which represents an important advantage in terms of maintenance and manufacturing

Drawbacks of this topology are:

- Unlike the other topologies, each H-bridge cell needs an isolated DC supply if active power transfer is required. This leads often to some complex transformer based arrangements

- The capacitors placed in each cell can be relatively large. This is mainly due to the fact that each individual bridge operate in a single-phase, with the associated high power ripple

It is finally noted that many other circuits respond to the name of cascaded converters [12] [14] [15], such as diode-based rectifier cell topologies, asymmetric cascaded circuit topologies, cascaded converters with variable multilevel DC-link voltage, and the so-called Modular Multilevel Converters which will be covered in detail in Chapter 3.

2.2.3 Fields of Application of Multilevel Converter

Fields of application of multilevel converters are schematically summarized in Fig.2.11.

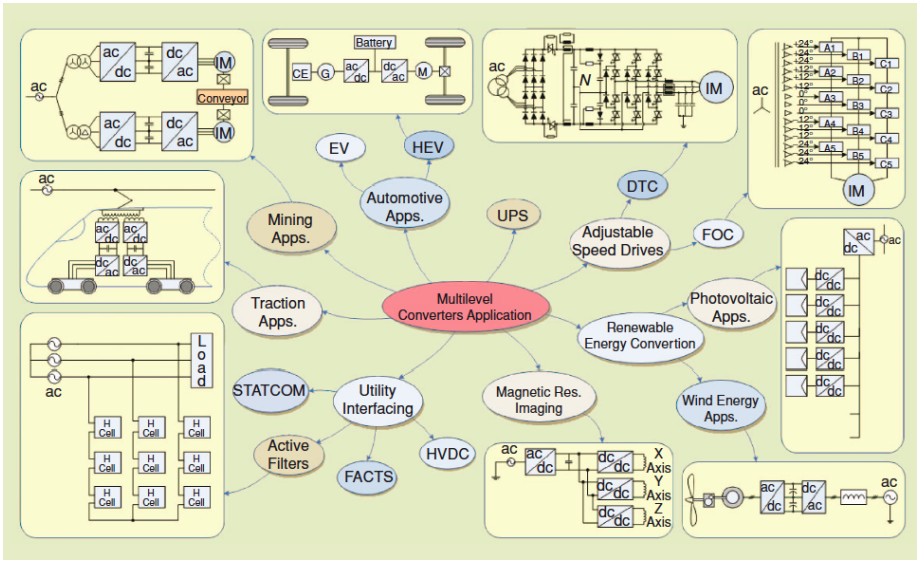

Figure 2.11: Multilevel Converter-based applications overview [11]

- Controlled rectifiers: the main purpose is to avoid the phase shift of transformers used in traditional multipulse rectifiers [15].
- Medium voltage motor drives. Particularly, the NPC converter is frequently found in high power AC motor drive applications like conveyors, pumps, fans and mills, among others [11]. In addition, the back-to-back configuration for regenerative applications has also been a major plus of this topology, used for example in regenerative conveyors for the mining industry or grid interfacing of renewable energy resources like wind power [11].

- In the field of power systems, both NPC and cascaded multilevel converters are especially suitable for harmonic and reactive power compensation [15] such as active filters, STATCOM. In fact, the first unified power flow controller (UPFC) in the world was based on a diode-clamped three-level inverter [20]. On the contrary, the capacitor-clamped converter cannot have balanced voltage for power conversion involving only reactive power, thus, it is not suited for reactive power compensation [15]. In general, applications interfacing the medium/high voltage grid are well suited for the use of a multilevel converter.

2.3 Solid State Transformers

During the initial years of electric distribution a so-called war of currents was waged between the defenders of alternating (AC) and direct (DC) currents.

The first electric generator was the direct current (DC) generator and hence, the first electric power transmission line was built with DC. The basic discoveries of Volta, Ohm and Ampere were also in the DC field. In addition, Thomas A. Edison built the first electric central station in the world in 1882, on the Pearl Street, in New York, which was also a DC power plant [23]. On the other side of the argument, AC, as advocated by Nicola Tesla and George Westinghouse, had the ability to transform high voltages, suitable for transmission over long distances, to lower voltage levels needed both at the generation side and for residential usage [30]. Although DC presented a dominant position, AC transmission systems finally won the battle and become the most popular way for energy transmission.

Since the introduction of AC systems in 1887, the magnetically coupled transformer had been used for both voltage transformation and galvanic isolation.The basic construction of the transformer did not change much during the last century [30]. Improvements in material processing and the creation of new alloys with higher magnetic saturation and low hysteresis losses gave rise to more efficient and reliable transformers.

Distribution transformers are fundamental components of the power distribution system and relatively inexpensive, highly reliable, and fairly efficient [38]. They can be considered therefore a mature technology. However, some of their characteristics do not fit well with the requirements of the future power grids [30],[38].

- Output voltage is a direct representation of the input. Any unwanted characteristics from the input, such as voltage dips or frequency variations, will show up at the output.
- As a consequence of the previous issue, voltage and/or current harmonics in one side will be transmitted to the other.
- In general, transformers are designed for maximum efficiency when they operate near to full load. This severely penalizes their efficient when they operate at no load or low load levels.
- There is a voltage drop when they are loaded that may require the use of some voltage compensation mechanisms, such as tap changer transformers.
- Require protections against system disruptions and overload.

Over the last century significant efforts have been done to overcome some of these negative effects. E.g. Many standards regulating the consumer behavior have been adopted e.g. to avoid the propagation of reactive power and harmonic currents through the grid. They use FACTS (Flexible AC Transmission Systems) in conjunction with line frequency transformers (LFTs has become very popular during the last decades to address these problems.

Solid-state transformers (SSTs) offer a different approach for the connection of two AC systems with galvanic isolation. SSTs make use of the fast switching characteristics of semiconductors, to replace the low frequency, iron based transformers by high frequency, lighter transformers.

There is no unanimous criteria concerning the first appearance of the SST concept. In [39] the first conceived SST is dated in the early seventies. This first form of AC/AC power electronic circuit with galvanic isolation and power flow control was presented by W. McMurray [40], it is shown in Fig. 2.12. This circuit consists of two four-quadrant switches on the primary side connected to a 1-phase grid while feeding the primary center-tapped higher-frequency transformer winding. On the secondary side, a similar structure comprising the required inductor and an output capacitor is used.

Other authors claim the first mention of this kind of power converter was in the eighties [30]. In 1980, US Navy researchers introduced the concept of "Solid State Transformer" as an alternative to the conventional transformer [37]. It consisted of an AC-AC buck converter aimed to reduce the input voltage to a lower level. Although the technology for the successful demonstration of the concept did not exist at the time, the advantages of that

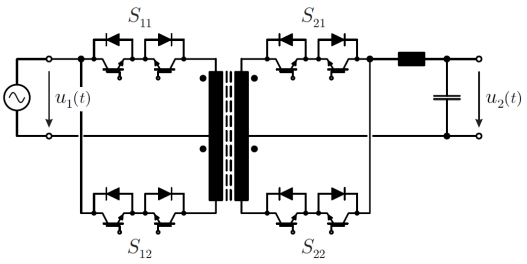

Figure 2.12: SST concept [40] based on four quadrant switches able to control output voltage and/or input current amplitude while providing galvanic isolation.

system were clearly stated. Further advancements in power semiconductors and in the understanding of multilevel converters, made the concept became viable, renewing the interest and boosting an intensive research activity in the topic [38].

Focusing on the modern Solid-State Transformer concept, it can be defined as a power electronic based device that replaces traditional 50/60Hz power transformers by a high frequency isolated AC/AC conversion stage, as shown in Fig.2.13. Galvanic isolation between the two ports or grids is still a requirement so some kind of transformer is therefore needed. Use of power semiconductors allows operation of this transformer at frequencies much higher than the grid frequency, enabling a significant reduction of transformer weight and volume. Additionally, controllability of power semiconductors enables the use of advance concepts especially suitable for high voltage/high power applications, as serialization (multilevel constructions) and/or paralelization of elements, modularity, redundancy, etc.

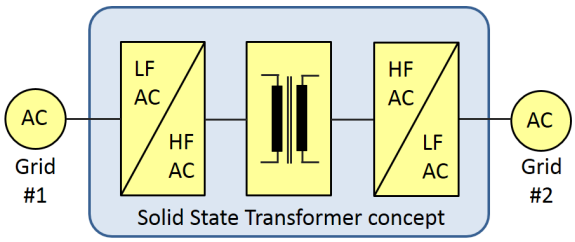

Figure 2.13: Solid State Transformer concept. Basic power conversion representation.

The solid state transformer can potentially overcome some of the problems experienced in distribution systems using traditional transformers, and can play a a major role for the development of the future smart electric system [36]. Potential advantages of the SST would include:

- Decreased volume and weight. The original motivation for the SST

was to develop lighter and smaller devices able to realize the AC/AC voltage transformation. This would have advantages in terms of volume, weight and cost of the installation, as well as it transportation and maintenance aspects.

- Reactive power compensation and harmonic filtering. The presence of the power electronic devices and storage elements (capacitors and inductors) can provide additional functionalities which do not involve active power handling, including reactive power compensation and/or harmonic elimination, at no cost.

- Controllability. Solid state transformers are able to control the power transferred almost independently from the features of the grid where they are connected to. Additionally, these converters can handle imbalances produced e.g. by single-phase or imbalanced loads, either absorbing them internally using the internal energy storage elements, and/or transferring the imbalance to other ports in a controlled manner.

- Micro grid integration. The microgrid concept, including both DC and AC microgrids, has been a hot research topic in the recent years. Solid State Transformers can be envisioned as a compact solution able to interface multiple microgrids of different nature [41].

- Disturbance suppression and fault isolation. Unlike the passive power transformer, SST embedded with advanced control functions may also provide disturbance suppression and fault isolation capabilities. For instance, the regulated output voltage of SST can compensate voltage sags in the input side. In addition, the Solid State Transformer may also have the capability of limiting the short-circuit fault current as well as providing reactive power compensation capability for transient-fault ride-through, similar to STATCOMs used e.g. in wind energy [36].

While SST could potentially replace conventional transformers in any application, there are certain fields or niches in which their advantages make them specially appealing. Examples of these are:

- On-board and sub-sea systems are clear examples of space-critical applications in which the improved performance and power density of SSTs can be of significant importance [39]. Increased power density can also be beneficial in boarded systems in ships and especially in railway applications, in which the low frequency (i.e. 50Hz or 16.6Hz) and single-phase nature of catenary voltage places further concerns for the use of conventional transformers.

- Future electric power system: the Smart Grid. This concept consists on an efficient distribution of electric energy which is based on flexible routing mechanisms and comprehensive information about the end-user's energy consumption, which ultimately facilitates the coordination and integration of renewable energy sources and energy storage systems into the current electrification network [39].

2.3.1 SST Topologies

A Solid State Transformer typically consists of three major blocks:

- One (or more) power converter stages to transform the low frequency (grid frequency) AC voltage into a high frequency AC voltage required by the HF transformer.
- An isolation stage using a high frequency transformer.
- One (or more) power converter stages to transform the high frequency AC voltage into a low frequency AC voltage.

Though there is no common agreement on the classification of SSTs topologies, this is often done based on the number of power conversion stages. According to this criteria, three-stage, two-stage and one-stage implementation have been proposed along the literature.

2.3.1.1 Three-stage SST

Three-stage SSTs typically use the following steps $AC_{MV-LF} - (DC - AC_{HF} - DC) - AC_{LV-LF}$, where MV and LV stand for Medium Voltage and Low Voltage, and LF and HF stand for low frequency (grid frequency) and high frequency respectively. It is noted that the high frequency transformation occurs at the AC_{HF} stage.

Three-stage configuration seems to be the most popular choice. This arrangement can be found multiple research projects, such as FP6 project UNIFLEX (Europe)[33], National Science Foundation (NSF) project FREEDM (USA) [31][32][41], and other projects in Japan [29][34].

Different three-stage SST arrangements can be seen at Fig.2.14. Left side will be referred as the MV-LF side, while right side is referred as the LV-LF side.

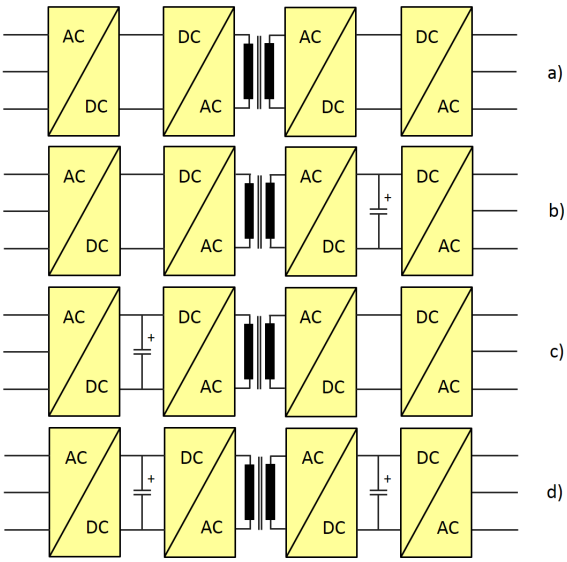

Figure 2.14: Three-Stage SST. a) MV-side indirect matrix converter/LV-side indirect matrix converter b) MV-side indirect matrix converter/LV-side DC-link back-to-back converter c) MV-side DC-link back-to-back converter/LV-side indirect matrix converter d) MV-side DC-link back-to-back converter/LV-side DC-link back-to-back converter

The first conversion stage (AC-DC) can either include a conventional DC link with a capacitor (see Fig.2.14-c)-d)) or avoid the DC capacitor link by means of an indirect matrix converter structure [39] (see Fig.2.14-a)-b)). Due to the high voltages in the HV-AC side of the SST, multilevel and/or modular topologies are normally required, examples of this can be found in [28],[29],[31]-[34].

For the central stage where the high frequency transformer is placed, Dual Active Bridge converter (DAB) is the most popular choice [29],[31]-[34] (the DAB is analyzed later in this chapter in subsection 2.3.2). This conversion step can be performed in several ways. Examples of this includes multilevel DC-DC converters without split DC link [28] and multiple DC-DC converters splitting the DC link [24][28].

The last conversion stage (DC-AC) can use the same arrangements as the first stage. It can use a conventional DC link capacitor structure (see Fig.2.14-b)-d)) or avoid the DC link by means of an indirect matrix converter [39] (see Fig.2.14-a)-c)). It must be noted however that significant differences exist between the left and right AC sides when the SST realizes a HV-AC to LV-AC transformation. Power converters in the left side must withstand high voltages, which often requires multilevel topologies and/or high voltage semiconductors. However, the current in this devices will be relatively small.

On the contrary, power devices in the right side must normally withstand much lower voltages, two level topologies using 1.2 kV or 1.7 kV power devices can be enough in this case. However, since the power must be the same in both sides (neglecting losses), the right side elements must carry much higher currents.

Symmetrical and asymmetrical arrangements between the HV-AC and LV-AC sides have been proposed. Examples of symmetrical arrangements using both modular and non-modular converters, can be found in [28][29][33][34]. An asymmetrical arrangement was proposed in the NSF FREEDM project. Its input stage consists of a modular arrangement and its output stage is based on a single inverter connected in parallel with all the individual cells in order to provide two single-phase outputs (see Fig.2.15) [27][31][32][35].

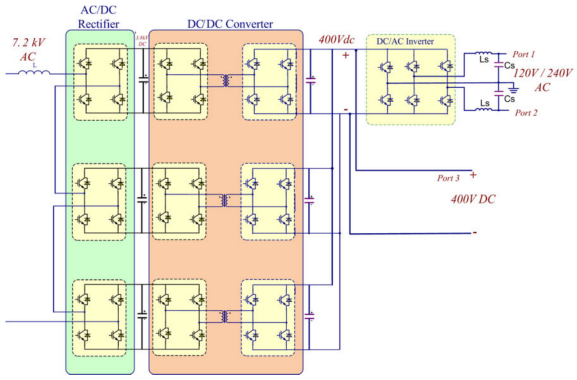

Figure 2.15: Topology of the proposed FREEDM SST topology [31].

2.3.1.2 Two-stage SST

Two-stage arrangements eliminate one power conversion stage. Thus, a direct AC-AC transformation is required, meaning that either a matrix converter or cycloconverter is needed [24][39], what normally increases cost and complexity and adds reliability concerns. Fig.2.16 shows some possible two-stage SST topologies. The conversion steps are typically $(AC_{MV-LF} - AC_{HF} - DC) - AC_{LV-LF}$.

The direct AC-AC conversion is performed by a direct matrix converter, which can be placed either on the HV side (Fig.2.16-a)-b)) or in the LV side (Fig.2.16-c)-d). Similarly to the previous three-stage configuration, the remaining (AC-DC) conversion can be based on a conventional DC link capacitor structure (Fig.2.16-b)-d)) or avoid the DC link by the use of an indirect matrix converter (Fig.2.16-a)-c)).

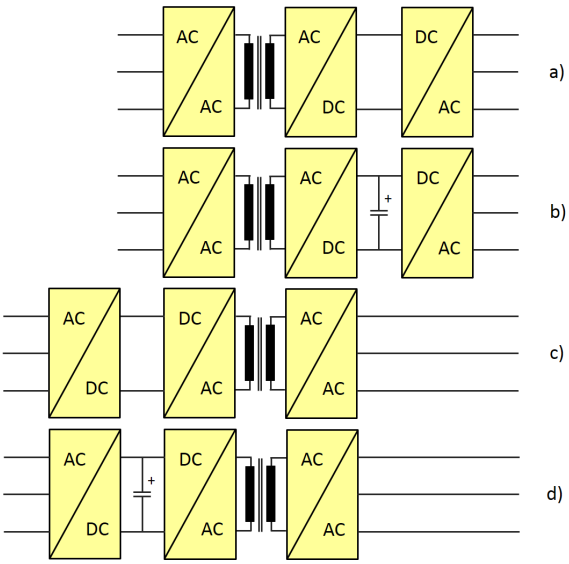

Figure 2.16: Two-Stage SST. a) MV-side direct matrix converter/LV-side indirect matrix converter b) MV-side direct matrix converter/LV-side DC-link back-to-back converter c) MV-side indirect matrix converter/LV-side direct matrix converter d) MV-side DC-link back-to-back converter/LV-side direct matrix converter

2.3.1.3 One-Stage SST

A one-stage SST topology will consist of a direct 3-phase matrix conversion (see Fig.2.17) [39]. The benefit of this type of solutions would basically be an increased power density as well as an increased robustness thanks to the elimination of DC link capacitors. However, new concerns arise mainly related to the switching strategies as well as with the extra components (either active or passive) needed for safe operation of the matrix converter.

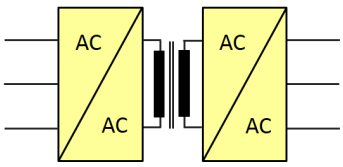

Figure 2.17: One-Stage SST. MV-side direct matrix converter/LV-side direct matrix converter

To conclude, the fully modular three-stage configuration appears to be the most popular choice. As it has been addressed, this topology realizes a double DC/AC transformation in the HV side and in the LV side respectively. Isolation between the HV and LV sides is provided by a DC/DC

stage using a HF transformer. A remarkable feature concerns the presence of DC links which offers notable advantages in terms of optimization in each conversion stage [39].

2.3.2 The Dual Active Bridge (DAB)

IT has been shown that the isolation stage in a SST is usually based on a DC-DC bidirectional converter with a medium-high frequency transformer. The DAB is likely the most popular topology to realize this transformation. Though the DAB is not a main topic for this thesis, its principles of operation and performance are discussed following, given its importance for the power converter topologies studied in this thesis.

2.3.2.1 Principles of operation

The Dual Active Bridge converter was originally proposed in [42][43], a detailed analysis can be found in [44]. The DAB is a bidirectional DC-DC converter which consists of two full bridges linked by a medium frequency transformer with turns ratio $1 : n$ (see Fig. 2.18).

The transformer leakage inductance (L_k in Fig. 2.18) will be a key parameter for the operation of this converter. This inductance corresponds to the leakage inductance of the high frequency transformer; nevertheless, an additional inductance connected in series with the high frequency transformer can be used when the leakage inductance of the high frequency transformer is too small. This is done to achieve Zero Voltage Switching (ZVS) conditions for operation at lower power levels (i.e. lower output current i_o). However, this will also limit the maximum power that can be transferred (see eq. (2.2)). ZVS operation condition is analyzed in Section 2.3.2.2.

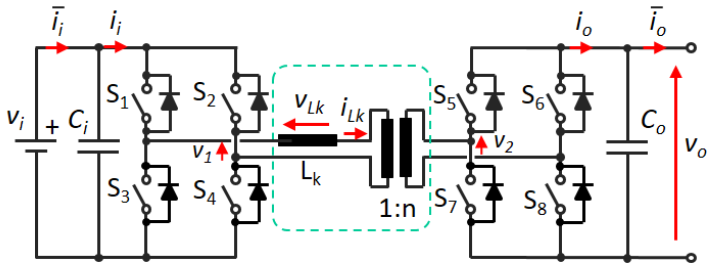

Figure 2.18: Schematic representation of DAB converter

A simple manner of controlling the DAB is using a constant duty cycle (50%) to generate a high frequency square voltage in both sides of the trans-

former ($\pm v_i, \pm v_o$). The resulting two square voltages generated by the full bridges must be adequately phase shifted to produce a voltage (v_{Lk}) along the transformer leakage inductance L_k, and consequently, a current will start to flow (i_{LK}). This current will depend on the phase shift applied between the two bridges and hence, power flow (both magnitude and direction) can be easily controlled by controlling the phase shift between the gate signals in both sides of the converter.

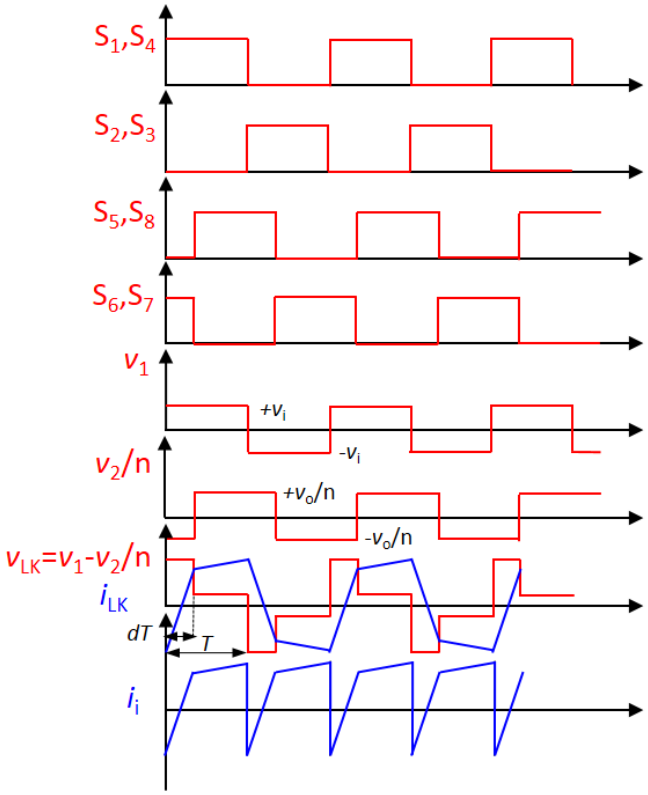

Figure 2.19: Waveforms of the DAB converter.

Figure 2.19 shows the waveforms of the DAB converter implementing this type of control. Primary side gating signals (S_1, S_2, S_3, S_4) have a 50% duty cycle. The operation of the primary-side full bridge produces a two-level square voltage waveform $\pm v_i$ in the transformer primary windings v_1. Similarly, secondary-side bridge generates a voltage v_2 with values $\pm v_o$ in the secondary-side transformer windings. Gating signals (S_5, S_8) are complementary to (S_6, S_7). Phase shift between the voltages applied to the transformer is controlled through the gating signals of both converters. This produces a differential voltage in the transformer leakage inductance ($v_{LK} = v_1 - v_2/n$), which results in a current i_{LK}.

As the structure of the converter is fully symmetric, power flow direction

is performed by selection of the phase shift sign. It is be observed from Fig.2.19 that input current i_i has a positive average value, power in this case is flowing from the left side to the right side.

Considering ideal components and neglecting losses in the passive elements, it is possible to obtain the average output current as (2.2), where T stands for the switching period, d deals with the relation between the phase shift and the switching period in v_{LK} (see Fig.2.19) and n stands for the HF transformer turns ratio.

$$\bar{i_o} = \frac{(1-d)dTv_i}{nL_K} \tag{2.2}$$

It is concluded from (2.2) that maximum power transfer is performed with a phase shift of $\pm 90^o$ ($d = 0.5$). Another important consideration regards the fact that power transfer is inversely proportional to the leakage inductance L_K, which can pose restrictions for the design of the medium frequency transformer. E.g. designs requiring high voltage isolation between the primary and the secondary, will require arrangements with and increased separation between the primary and secondary coils. This can result in and increased leakage inductance, eventually limiting the maximum power transfer capability of the DAB.

2.3.2.2 Performance Considerations

One of the main advantages of the DAB converter regards the fact that zero voltage switching (ZVS) is possible in all the devices forming the two full bridges, enabling efficient operation of the converter. In order to achieve ZVS, it is needed that the energy stored in the transformer leakage inductance is enough to charge and discharge all the parasitic capacitors placed at the output of the switching devices [43][44][45]. That is, during transition between S_3 closed and S_1 opened (see Fig.2.19), current through the leakage inductance (i_{Lk}) must be negative. That energy will depend on the leakage inductance value (L_k) and the transferred current (i_o). In general, higher leakage inductances (L_k) will achieve ZVS conditions at lower output current (i_o). However, this will limit the maximum power that can be transferred.

To illustrate ZVS concept, Fig.2.20 shows one branch (S_1 and S_3) of one full bridge of the DAB at three different switching states, while Fig.2.21 shows the gating signals (G_1 and G_3) and the voltage drop at the parasitic capacitors (v_{c1} and v_{c3}) for the same devices (S_1 and S_3).

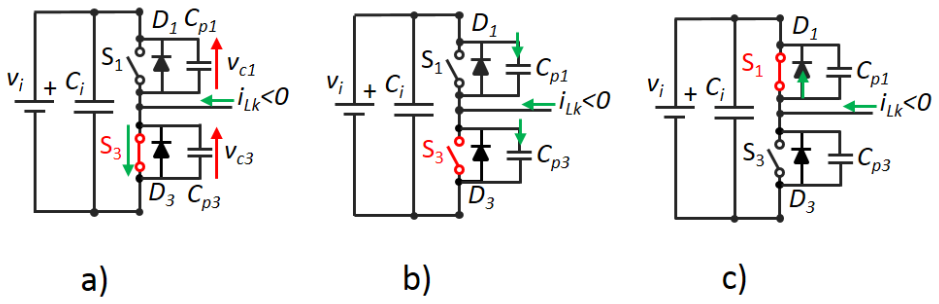

Figure 2.20: ZVS operation. Charging and discharging of the parasitic capacitors C_{p1},C_{p3} in one branch of the DAB during the switching process. a) S_1 is opened and S_3 is closed b) Dead time: both S_1 and S_3 are opened c) S_1 is closed and S_3 is opened

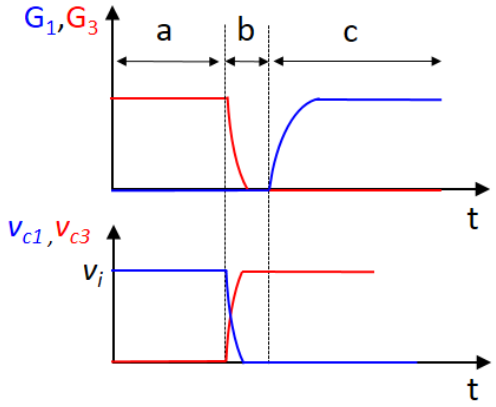

Figure 2.21: ZVS operation. Gate signals (G_1,G_3) and voltage at the parasitic capacitor (v_{c1},v_{c3}) in one branch of the DAB during the switching process. a,b,c represent periods of time with the circuit representation showed in Fig.2.20

When the branch is in state a) in Fig.2.20, current is flowing through device S_3, its parasitic capacitor being completely discharged ($v_{c3} = 0$). On the other hand, upper capacitor has been previously charged ($v_{c1} = v_i$). During the dead time, where both devices are opened (state b) in Fig.2.20), upper capacitor starts discharging while lower capacitor starts charging. Diode D_1 was inversely polarized. Once S_1 is closed and D_1 starts to conduct (branch in state c) in Fig.2.20), the parasitic capacitor was already discharged and the switching process occurred therefore with zero voltage. Previous discussion is also valid for the other full bridge.

Considering M (2.3) as the relation between the output voltage and the input voltage, it is possible to define the limits of operation in ZVS

conditions as a function of the phase shift d and M [43]. This is shown in Fig.2.22.

$$M = \frac{v_o}{v_i \cdot n} \tag{2.3}$$

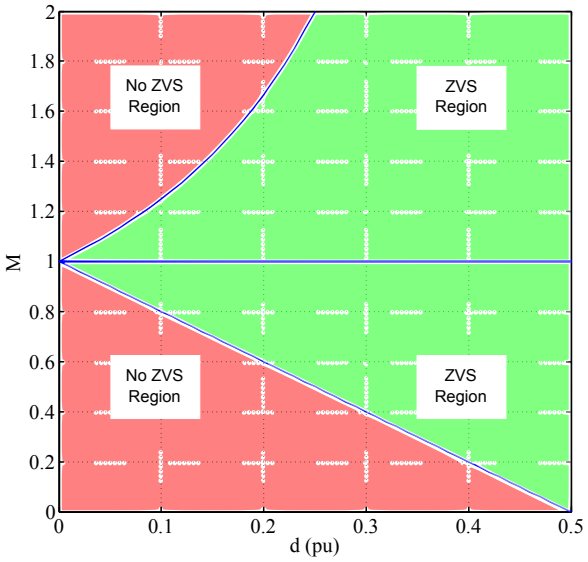

Figure 2.22: Limits of operation of the DAB in ZVS conditions as a function of the phase shift d and the ratio between output and input voltages M.

In case $M = 1$, it can be observed that ZVS is always possible, independent of the phase shift, i.e. of the power being transferred. Hence, the choice of input and output voltages with a conversion ratio that operates with $M = 1$ in rated conditions will in principle assure ZVS in all the working range of the converter. For values of M different from 1, ZVS conditions will fade away as the phase shift gets smaller, i.e. as the power being transferred decreases. This is one of the reasons why the design of the converter to operate with large phase shifts would be in principle the smarter strategy. However, the use of phase shifts d close to its maximum ($d = 0.5$) may have some major drawbacks:

- The relationship between the phase shift and the output current (and therefore of the power transferred) is linear for small values of the phase shifts, such linearity being lost as d approaches to its maximum ($d = 0.5$). This is readily deduced from (2.2), which shows the parabolic relationship between the phase shift and the current. Having a linear relationship between the phase shift and the power makes control easier limiting the phase shift to $d < 0.35$ is a common criteria to keep a good linearity [46].

- The use of large phase shifts leads to larger reactive current in the converter [45] (i.e. current that is not directly related to active power transfer), which may reduce the efficiency.

2.4 Summary

This chapter has firstly introduced the new energy network scenario and highlighted the importance of electronic power converters. Multilevel converters offer several advantages, including their capability to withstand high terminal voltages using power devices with relatively low voltage ratings and to provide high quality waveforms with relatively low switching frequencies and/or filter requirements. Both conventional and novel topologies have been discussed, ending with the introduction of the Solid State Transformer concept. Classification of these kind of converters as well as a brief study about the Dual Active Bridge converter (DAB) and its operation have been also covered.

Chapter 3

Modular Multilevel Converters (MMC/M2C)

This chapter firstly introduces the Modular Multilevel Converter (MMC) and analyzes its motivation. Then, principles of operation of the MMC are addressed and modeling based on complex vector notation is presented. Modulation strategies, capacitor voltage balancing methods and control of the MMC are deeply studied and analyzed. Especial emphasis is given to the circulating current, including a proposal for the classification of existing control strategies for the MMC based on this criteria. To conclude, operation of the MMC under voltage constraints and its use for variable-speed drive applications are studied.

3.1 Introduction

The Modular Multilevel Converter (MMC) is a DC to AC power converter that was first proposed one decade ago by Marquardt and Lesnicar [47]-[50].

It must be remarked that the same circuit using voltage sources instead of capacitors had already been proposed by Alesina et al. in 1981 [51]. Fig. 3.1 shows the basic configuration of this multilevel converter where each leg consists of two stacks of cells (or submodules) and two inductors (L_{arm}). The classic arrangement of the MMC uses submodules consisting of a half-bridge configuration, as shown in Fig. 3.2-b).

The MMC offers several features. Some of them are shared with the conventional multilevel topologies, while some others are quite different at

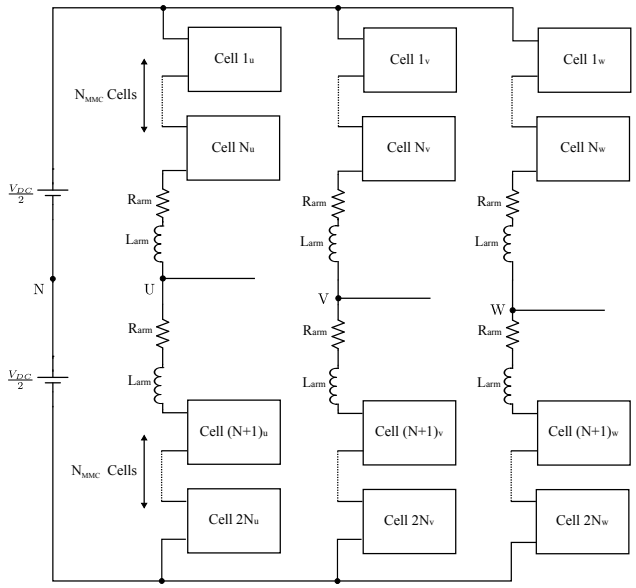

Figure 3.1: Circuit configuration of a three-phase MMC.

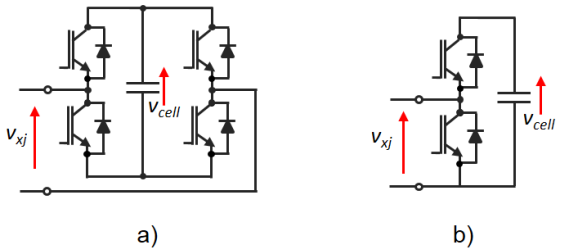

Figure 3.2: Submodule circuit configurations: a) Full bridge (Bridge cell) b) Half bridge (Chopper cell).

first glance and may seem strange when compared to other multilevel voltage source converter topologies [52]:

- In only requires one isolated DC supply. It is similar in this regard to conventional two-level DC to AC power converters.
- Similar as for other multilevel converter topologies, it combines low switching frequency and low harmonic content due to the reduced voltage steps in the output voltage. Low switching frequency results in reduced switching losses [53].
- It has modular realization, which is easily scalable to achieve the required voltage levels [47]. This is similar to the CHB topology.
- Redundancy can be easily achieved just by using more cells than

strictly needed. Faulty cells can be easily bypassed. This is also similar to the CHB topology.

- The internal arm currents are not chopped, but flow continuously [52].
- Protection chokes (L_{arm}) are inserted into the arms. However, they do not disturb operation or generate overvoltages in the semiconductors, since arm currents are not chopped. Moreover, the arm inductors limit the AC-current in the event of a DC-bus short-circuit (fault condition) [52].
- The submodules are two terminal devices. There is no need to supply their DC link capacitor from external DC voltage sources. This is true independent of whether the MMC is transferring active power between its DC and AC sides or it is only supplying reactive power in the AC side [52].
- Voltage balancing of the submodules does not depend on the timing of the pulses or the semiconductor switching times. It is actually performed by the converter control [52].
- No bulk DC capacitor is needed. The energy is distributed along the capacitors in each cell. This is an advantage compared to other multilevel topologies as can avoid catastrophic event e.g. in case of a fault (e.g. short-circuit in the DC link).

However, this circuit topology presents some drawbacks:

- The number of devices required for a given AC voltage is higher compared e.g. to the CHB option.
- As many capacitors as the number of required submodules are needed, which normally have a significant size. This is similar to the CHB topology.
- Individual control of the capacitor voltages in each cell may be needed, which leads to significant computational requirements.

Although the term "Modular Multilevel Converter" is normally used to describe the topology shown in Fig. 3.1 with the cells shown in Fig. 3.2-b), it can be considered as a member of a wider Modular Multilevel Cascade Converter (MMCC) family [54]. According to this classification, the MMCC family would consist of four main circuit configurations:

1. Single-Star Bridge-Cells (SSBC): It is based on single-phase full bridge cells with star connection of three clusters. This configuration has already been described as Cascade H-Bridge Converter (CHB) in Fig. 2.10.

2. Single-Delta Bridge-Cells (SDBC): This circuit configuration is based on single-phase full bridge cells with delta connection of three clusters. The mentioned topology is shown in Fig. 3.3.

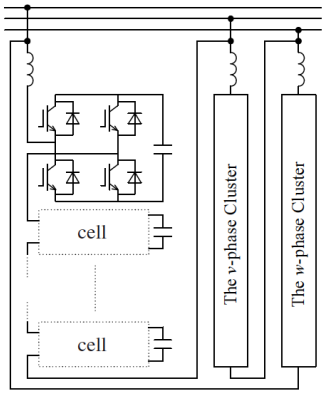

Figure 3.3: Circuit configuration of MMCC-SDBC [54].

3. Double-Star Chopper-Cells (DSCC): The Double-Star configuration is based either on the conventional topology presented in Fig. 3.1 with non coupled arm inductors or on the configuration shown in Fig. 3.4 with coupled arm inductors, but both using half-bridge cells as those shown in Fig. 3.2-b).

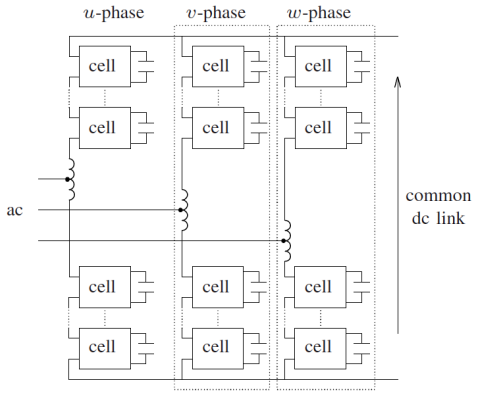

Figure 3.4: Circuit configuration of MMCC using coupled arm inductors [54].

The reason for the name is that DSCC is based on a couple of star-connected MMCCs in which the low voltage AC sides of multiple reversible choppers are cascaded to form each arm. It must be noticed

that the use of the coupled inductors leads to a smaller size and lighter weight than the total of the two non-coupled inductors [54].

4. Double-Star Bridge-Cells (DSBC): This topology is based on a couple of star-connected MMCCs in which the low voltage AC sides of multiple single-phase full-bridge voltage-source converters are cascaded to form each arm. The DSBC configuration includes both Fig. 3.1 and Fig. 3.4 with the cells shown in Fig. 3.2-a).

The term "Modular Multilevel Converter (MMC)" will be used hereafter to refer to the MMCC with Double-Star Chopper-Cells (DSCC) and non-coupled arm inductors.

MMC topology has found its main application in the field of high or medium voltage power converters [55]. This is mainly due to its attractive features such as modularity and scalability, as well as the lack of a high voltage DC-link capacitor, as the stored energy is distributed among the cell capacitors. All these reasons have made the MMC a very appealing topology for HVDC applications. In fact, this topology can be found in practical applications under the trade name of "HVDC-PLUS", produced by Siemens, for power ratings of 400 MVA, 200 kV DC link voltage and 200 cells [12][13].

Use of MMC for medium-voltage drives is currently receiving increased attention nowadays [57][58]. The multilevel nature contributes to reduce the motor current ripple and consequently the resulting torque ripple, as well as to mitigating effects due to common-mode voltages, like ground leakage current and bearing current [56]. It must be noticed however that, as the MMC converter produces AC-voltage fluctuations in the capacitors of each cell at the output frequency [56], this topology would not be suitable for applications which require high torque in the low speed region. Inadmissible fluctuations of the capacitor voltage would occur in this case, prohibitive values of the capacitance would be required otherwise.

3.2 Principles of Operation of the MMC

The basic circuit configuration of a three-phase Modular Multilevel Converter can be seen in Fig. 3.5. Each leg (or limb) of the converter consists of two stacks of cells (or submodules), with N_{MMC} being the number of submodules per arm, each leg will consisting therefore of $2N_{MMC}$ cells. The classic arrangement of the MMC uses two non-coupled inductors per leg (L_{arm}) as previously shown in Fig. 3.1. The submodules have a half-bridge configuration with a floating capacitor (see Fig. 3.2-b)).

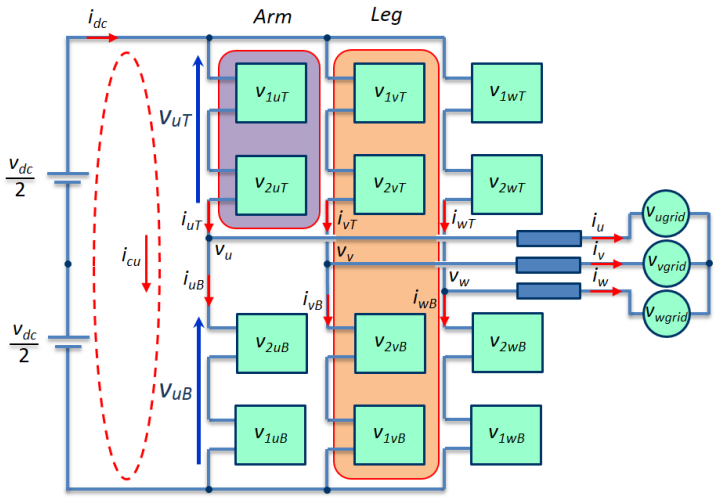

Figure 3.5: Schematic representation of a three-phase grid-connected MMC. Arm inductors are not shown for the sake of simplicity (see Fig. 3.1 for reference)

The goal of the arm inductors is twofold:

- They are necessary to handle the differential voltage the top and bottom sides of each arm. This differential voltage is used for current control purposes, as will be explained later.
- They limit the current in case of a fault (short-circuit).

The MMC control uses the differential voltage between the DC side (v_{dc}) and the overall DC component of the output voltage at the cells ($\sum v_{ju}$). This produces a circulating current (i_{cu}) per phase, which will be responsible of the power transfer between the DC and the AC sides of the converter. The differential voltage is achieved by proper control of the power devices at each cell, different control strategies could be used for this purpose. Independent of the control strategy being used, the average power transferred by each cell has to be equal to zero, which is the basic condition to maintain the average cell capacitor voltage constant. However, it is important to remark that the instantaneous power at each cell will have oscillations, as they are conducting an AC current component and withstanding a AC voltage component at their terminals, which produces power fluctuations at frequencies which are integer multiples of the fundamental frequency (ω_e). These power fluctuations will lead to oscillations in the cells capacitors voltage, which must be considered when designing the control strategies.

3.2.1 CHB vs. MMC

Motivation for the MMC topology can be seen a the need of an AC-DC bidirectional multilevel converter, such as NPC and FC topologies, but with a fully modular arrangement, similar to the CHB topology. It must be remarked that, on one hand, NPC and FC topologies are not fully modular, in the sense that increasing the number of levels is not as simple as adding identical cells. On the contrary, it places significant challenges regarding both the number of elements (diodes for the NPC, capacitors for the FC) that need to be serialized to withstand the increased voltages, as well as the control issues that are involved to balance the levels. It must be also highlighted that CHB, while being fully modular, only has an AC port, i.e. does not realize a power transfer, but can just supply reactive power and harmonics (STATCOM functionalities) due to its limited energy storage capability.

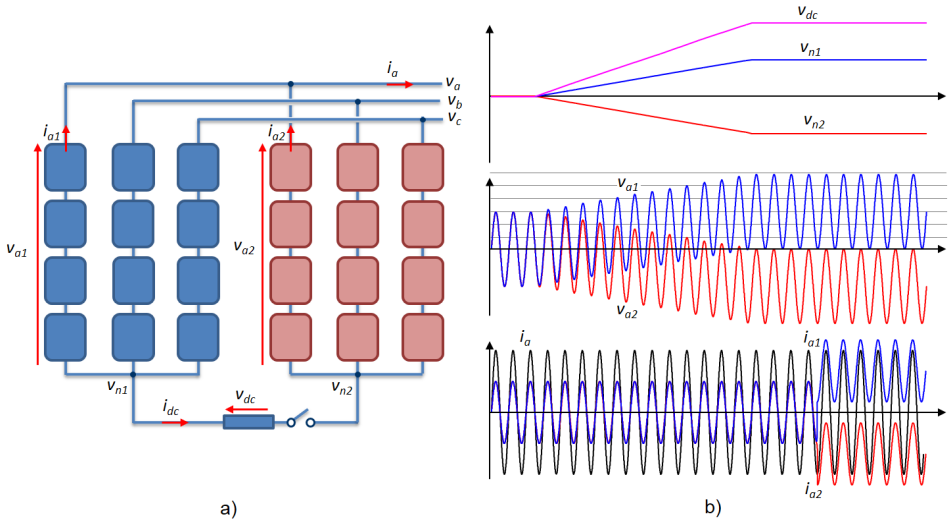

Figure 3.6: a- Two CHB converters parallel connected. Their neutral star-connection points are linked in order to generate a DC voltage. b- From top to bottom: Voltage applied to the neutral points v_{n1},v_{n2} and DC link voltage v_{dc}; Voltage generated by the cells of both converters v_{a1}, v_{a2}; Output phase "a" grid current i_a and arm currents i_{a1}, i_{a2}.

MMC topology can be viewed as a parallel connection of two CHB, as shown Fig. 3.6. Using the two CHBs in parallel connection as shown in Fig. 3.6-a), it is possible to create a differential DC voltage between the neutral of both converters ($v_{dc} = v_{n1} - v_{n2}$) by adding DC zero sequence voltage components to the voltage commands of the converters (see Fig. 3.6-b). If a load is then connected between both neutrals, a DC current (i_{dc}) will flow. Such DC current will add up to the existing AC currents (i_{a1}, i_{a2}), but will

circulate within the converter legs, i.e. will not show up at the grid, i.e. the output current i_a remains as pure AC. This DC current will be called *circulating current*. A DC voltage source instead of a load can be connected between the neutrals of the two CHB converters. In this case, the power flow in the DC link can be bidirectional. The arrangement with two CHB in parallel and a DC voltage source between its terminal corresponds to the MMC topology (see Fig. 3.7).

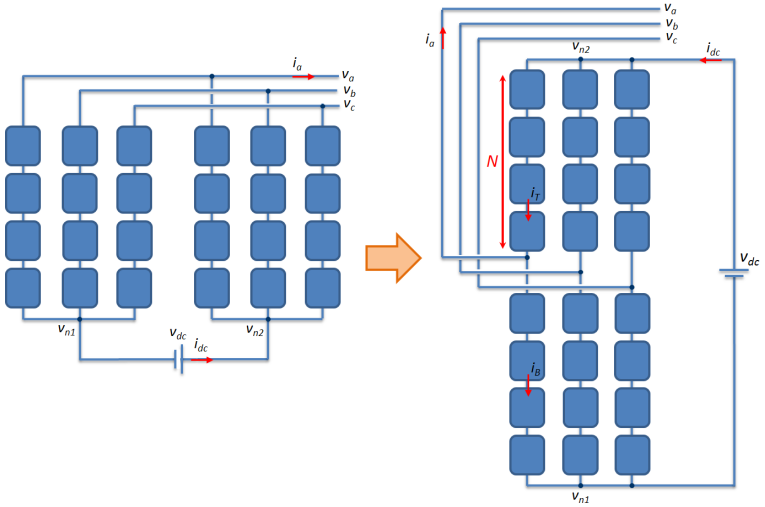

Figure 3.7: Transformation of two CHB converters parallel connected into an MMC. MMC is now able to generate a DC link.

Some interesting features can be extracted when comparing the CHB and the MMC:

- The MMC provides a DC link of $v_{dc} = v_{cell} \cdot N_{MMC}$ and realizes therefore a DC to AC power conversion. The CHB does not have such DC link voltage, so there is no power transfer between ports.

- For a given output voltage (v_a, v_b, v_c) and cell voltage (v_{cell}), the MMC requires twice the number of cells per arm, thus, four times the whole number of cells compared to the CHB. This is due to the need to create the DC link (see Fig. 3.7).

- The voltage produced by the CHB cells must be bipolar, full bridges being therefore required. On the contrary, the voltage produced by the MMC cells, due to the injection of the homopolar voltage, is unipolar (see Fig. 3.6-b). Hence, half bridges can be used in this case.

3.3 MMC modeling and power balance

The MMC realizes a bidirectional DC-AC power conversion. The AC side can be either single phase or three-phase, the analysis presented in this work is restricted to the three-phase case, as it has significantly more interest. For the case of three-phase systems, complex vector notation can be used to represent the AC variables as voltages (3.1) and currents vectors (3.2). The three phase MMC shown in Fig. 3.5 is simplified in this case to the scheme shown in Fig. 3.8. Each *complex vector cell* in this figure corresponds to three physical cells.

$$v_{ac} = \frac{2}{3}(v_u + v_v e^{j2\pi/3} + v_w e^{j4\pi/3}) \tag{3.1}$$

$$i_{ac} = \frac{2}{3}(i_u + i_v e^{j2\pi/3} + i_w e^{j4\pi/3}) \tag{3.2}$$

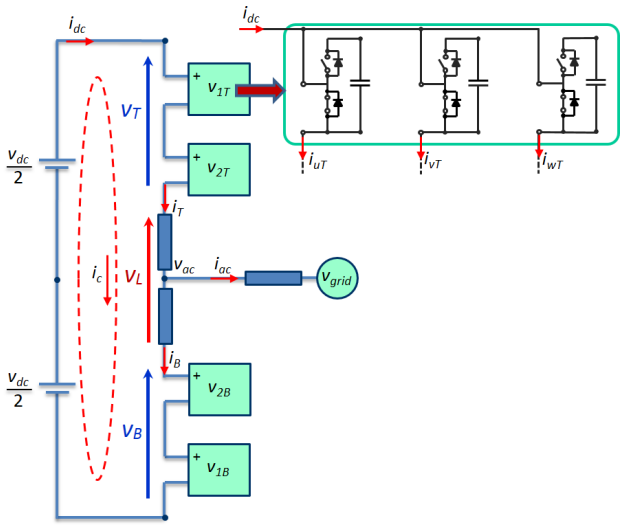

Figure 3.8: Left- *Complex vector* equivalent circuit of a three-phase MMC. Each *complex vector cell* corresponds to three conventional half-bridge cells.

The AC output current is split between the upper and lower arms, each carrying half of it (3.3)(3.4). The arm currents also includes a DC component i_c responsible of the power transfer between both sides of the converter. A relevant difference of the MMC with respect to conventional converter topologies, is that the arm currents (i_T, i_B) are not chopped, but flow continuously (i.e. they do not change between a positive or negative value to

zero depending on the switching state).

$$i_T = i_c + \frac{i_{ac}}{2} \tag{3.3}$$

$$i_B = i_c - \frac{i_{ac}}{2} \tag{3.4}$$

By adding the two previous expressions, the output AC currents are canceled out, the circulating current is then obtained (3.5):

$$i_c = \frac{i_T + i_B}{2} \tag{3.5}$$

This circulating current is an unique feature of this converter topology, it will be discussed in a subsequent section. Similarly to the arm currents, arm voltages also include DC and AC components, and are given by (3.6)(3.7).

$$v_T = \sum_{j=1}^{N_{MMC}} v_{jT} = \frac{v_{dc}}{2} - v_{ac} - \frac{v_L}{2} \tag{3.6}$$

$$v_B = \sum_{j=1}^{N_{MMC}} v_{jB} = \frac{v_{dc}}{2} + v_{ac} - \frac{v_L}{2} \tag{3.7}$$

The MMC is primarily a voltage source converter, aimed to produce a certain output voltage v_{ac}. The peak value of the AC output voltage is limited to $v_{dc}/2$ and $-v_{dc}/2$, assumed that no homopolar harmonics are added. To reach this limit, the capacitor voltage of each submodule (v_{cell}) must be charged to v_{dc}/N_{MMC}. Therefore, both upper and lower arms must handle the whole DC bus voltage. The output voltage equation can be expressed as (3.8). For the sake of simplicity, it has been assumed that the circulating current does not contain harmonics [57][59].

$$v_{ac} = \frac{1}{2}(v_B - v_T) - \frac{L_{arm}}{2}\frac{di_{ac}}{dt} - \frac{R_{arm}}{2}i_{ac} \tag{3.8}$$

Some conclusions can be derived from (3.8):

- The output AC voltage v_{ac} depends only on the output current i_{ac} and the difference between the arm voltages generated by the cells.

- The term proportional to the arm inductance can be removed by using the coupled arm inductors configuration (Fig. 3.4). Discussion of this concept can be found in [54][60][61].

- For current control purposes, half the arm inductance must be added to the output filter or load inductance.

The voltage drop along the arm impedance can be expressed as (3.9). It is seen that it is equal to the voltage difference between the DC bus and the sum of the upper and lower cells voltages. The circulating current depends on the DC bus voltage and the sum of the cell voltages. Therefore, adding or substracting the same voltage amount to/from the top and bottom arms, will affect to the circulating current but will have no effect on the AC side output voltage (see (3.8)). Consequently, v_L can be used to control the circulating current.

$$v_L = 2(L_{arm}\frac{di_c}{dt} + R_{arm}i_c) = v_{dc} - (v_B + v_T) \tag{3.9}$$

Upper and lower arm powers are given by (3.10) and (3.11) respectively, while combined and differential powers can be expressed as (3.12) and (3.13).

$$P_T = v_T \cdot i_T = \left(\frac{v_{dc}}{2} - v_{ac} - \frac{v_L}{2}\right) \cdot \left(i_c + \frac{i_{ac}}{2}\right) \tag{3.10}$$

$$P_B = v_B \cdot i_B = \left(\frac{v_{dc}}{2} + v_{ac} - \frac{v_L}{2}\right) \cdot \left(i_c - \frac{i_{ac}}{2}\right) \tag{3.11}$$

$$P_T + P_B = v_{dc} \cdot i_c - v_{ac} \cdot i_{ac} - v_L \cdot i_c \tag{3.12}$$

$$P_T - P_B = v_{dc} \cdot \frac{i_{ac}}{2} - 2 \cdot v_{ac} \cdot i_c - v_L \cdot \frac{i_{ac}}{2} \tag{3.13}$$

For the case of a three-phase MMC operating with balanced, perfectly sinusoidal voltages and currents in the AC port, both the DC and AC ports power, (P_{dc}) and (P_{ac}), are constant. However, the AC power in each phase will be pulsating. This is illustrated in Fig. 3.9.

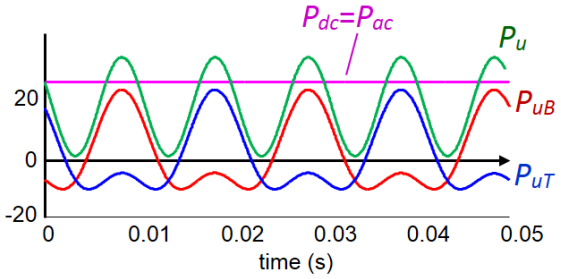

Figure 3.9: MMC powers wave shape representation. DC power P_{dc}, AC power P_{ac}, power generated by the top cells P_{uT}, power generated by the bottom cells P_{uB} and total power in the leg P_u. It has been particularized for phase u.

3.3.1 The Circulating Current

The circulating current is one of the distinguishing features of the MMC. The circulating current is defined by (3.5). If there is no harmonic content, the circulating current within each phase of the converter (see Fig. 3.5) will be a DC current of exactly one third of the total DC current, i.e. $i_{cu} = i_{cv} = i_{cw} = i_{dc}/3$. Considering that the combined arm power (3.12) (i.e. the net power balance in the converter) must be zero in order to avoid variations in the arm energy (i.e. cell capacitor voltages), and neglecting the voltage drop along the arm inductance (v_L), the circulating current can be derived from (3.12):

$$i_c = \frac{v_{ac} \cdot i_{ac}}{v_{dc}} \tag{3.14}$$

Particularizing the study for one individual cell (e.g $1T$), cell power must be equal to the capacitor power, in other words, cell power will directly affect to the variations of the energy stored in the cell capacitor (3.15), which are meant to be constant.

$$P_{1T} = v_{1T} \cdot i_T = v_{1T} \cdot (i_c + \frac{i_{ac}}{2}) = i_{cap1} \cdot v_{cell} = C_{cell} \cdot \frac{dv_{cell}}{dt} \cdot v_{cell} = 0 \tag{3.15}$$

Analyzing the general expression (3.14), it is noted that the circulating current must include a DC value and a harmonic component at twice the fundamental frequency, in order to keep the capacitors energies constant. Otherwise, the power oscillations will be reflected in the capacitor voltages. As a consequence of this, to preserve the net power balance of the converter, the control will need to trade off the oscillations of the capacitor voltages

and the harmonic content of the circulating current. I.e., balancing the cell capacitor voltages will naturally produce harmonics in the circulating current. Specific strategies can be used to control these harmonics. This issue will be analyzed in detail in Section 3.6.1.

3.3.2 Passive Elements Sizing

Control issues and behavior of the MMC can strongly depend on the sizing the of passive elements: arm inductors and cell capacitors.

Selection of the the arm inductors faces several goals: They are necessary to handle the voltage difference between the top and bottom side of the converter, and also help to limit the current in case of a DC-side short circuit. Also they can filter high-frequency harmonics of the circulating current. In the end, sizing of the arm inductors will depend on both filtering requirements (or circulating current control needs) and the short-circuit current limit [69].

Selection of the cell capacitors involves a trade-off between their size, cost and the voltage ripple that will exist in the cell voltage [69]. For a given permissible peak-to-peak cell capacitor voltage ripple $\delta v_{cap,pp}$, Lesnicar and Marquardt have proposed (3.16) to determine the required capacitance C_{cell}, where P is the real power transferred, v_{cell} is the nominal capacitor voltage, m_i is the modulation index, and $cos\phi$ is the power factor [49].

$$C_{cell} = \frac{P}{3N_{MMC}m_i v_{cap}\delta v_{cell,pp}\omega cos\phi}\left(1 - (\frac{m_i cos\phi}{2})^2\right)^{\frac{3}{2}} \tag{3.16}$$

Considering the unavoidable trade-off between the harmonic content of the circulating current and the oscillations in the capacitor voltages, the selection of the cell capacitor and arm inductor has been seen to have a significant impact on the performance provided by different control methods that have been proposed. To illustrate this, Table 3.1 summarizes some values used in experimental setups reported in the literature. The large dispersion in the sizing of the passives is remarkable. It is noted in this regard the difficulty to fairly compare the performance of those control methods due to this dispersion.

Table 3.1: Arm inductances and cell capacitances reported in the literature.

Arm inductance (H)	Cell Capacitance (mF)	Reference
$1e^{-3}$ (3.20%)	3 (10.6%)	[55]
$1e^{-3}$ (4%)	3.3 (9%)	[57]
$0.25e^{-3}$ (1.31%)	3.3 (23.9%)	[61]
$0.75e^{-3}$ (4%)	6.6 (11.9%)	[62][63]
$2e^{-3}$ (18.6%)	4.4 (21.4%)	[59]
$3.1e^{-3}$ (10.4%)	3.3 (10.2%)	[64][65]
$3.3e^{-3}$ (3.3%)	3.3 (3%)	[53]
$4.74e^{-3}$ (7.4%)	5.6 (50.5%)	[66]
$2e^{-3}$ (17.4%)	4.4 (20.1%)	[67]
$3.6e^{-3}$ (22.6%)	3.6 (58.1%)	[68]

3.4 Modulation Strategies

The primary goal of the modulation is to calculate the cell gate signals to obtain the desired output voltages. Table 3.2 summarizes the existing modulation strategies, N_{MMC} standing for the number of submodules per arm. The number of inserted cells determines the number of voltage levels applied to the arm inductors. If the number of inserted cells equals N_{MMC}, the voltage applied to the arm inductance is zero (see equation 3.9). If the number of inserted cells is $\neq N_{MMC}$, then a constant voltage is applied to the arm inductance, behaving as an inductive divider.

Similarly to other multilevel topologies, two carriers dispositions can be used (see Fig. 3.10): level-shifted and phase-shifted:

Level-shifted carriers can be placed in phase (*In-Phase-Disposition*), the output voltage can take then $2N_{MMC}+1$ voltage levels. On the other hand, level-shifted carriers can also be placed 180 degrees phase-shifted between top and bottom arms (*Phase-Opposite Disposition*). With this configuration, the number of voltage steps in the output voltage waveform is reduced to $N_{MMC}+1$ levels. In general, a reduced number of voltage levels leads to a reduced number of voltage steps in the arm inductance and consequently, a decrease in the circulating current switching ripple. However, the number of levels in the output voltage is also reduced, therefore increasing its harmonic distortion (see Table 3.2).

Phase-shifted carriers can also be used with MMCs. Carriers can be generated evenly spaced ($360°/2N_{MMC}$), which produces similar effects as level-shifted *Phase-Opposite Disposition*. On the other hand, carriers can be placed in an interleaved disposition where carriers in adjacent cells are shifted by $360°/N_{MMC}$. This provides similar results as the level-shifted *In-Phase-Disposition*.

Table 3.2: Modulation strategies and carriers disposition.

Carriers Disposition	*Output voltage levels*	*Inserted cells*
Phase-shifted		
Evenly spaced carriers	N_{MMC}+1	N_{MMC} ($v_L = 0$) [N_{MMC}+1,N_{MMC},N_{MMC}-1] ($v_L \neq 0$)
Interleaved carriers	$2N_{MMC}$+1	[N_{MMC}+1,N_{MMC},N_{MMC}-1]($v_L = 0$) [N_{MMC}+2,N_{MMC}+1,N_{MMC},N_{MMC}-1,N_{MMC}-2] ($v_L \neq 0$)
Level-shifted		
In-Phase-Disposition (IPD)	$2N_{MMC}$+1	[N_{MMC}+1,N_{MMC},N_{MMC}-1] ($v_L = 0$) [N_{MMC}+2,N_{MMC}+1,N_{MMC},N_{MMC}-1,N_{MMC}-2] ($v_L \neq 0$)
Phase-Opposite-Disposition (POD)	N_{MMC}+1	N_{MMC} ($v_L = 0$) [N_{MMC}+1,N_{MMC},N_{MMC}-1] ($v_L \neq 0$)

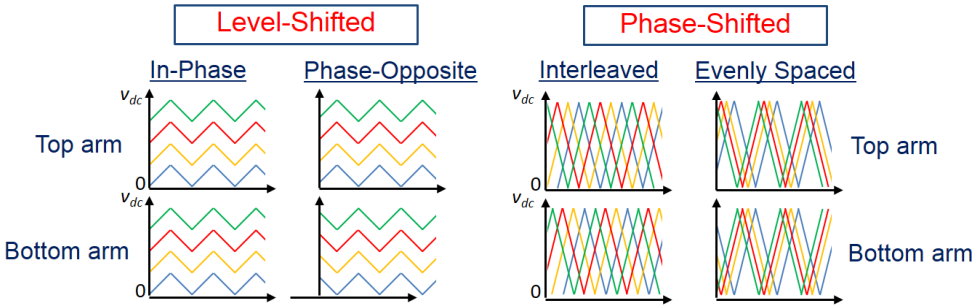

Figure 3.10: Modulation strategies. Left- Level-shifted. Right- Phase-shifted.

3.5 Capacitor Voltage Balancing Methods

For the modulation strategies covered in the previous section, for each switching period every carrier is linked to a certain submodule. If this carrier-submodule connection is permanent, i.e. remains unchanged for all the switching periods, some cells will be inserted more often than others. Since all the cells in the arm must carry the same current, this will inevitably produce unbalances in the capacitor voltages. Therefore, some kind of capacitor voltage balancing strategy must be implemented to prevent this to happen.

While the modulation strategy defines the number of submodules that must be inserted at any switching period, voltage balancing algorithm selects the specific cells that should be inserted/removed based on the capacitor

voltages and the sign of the arm current. In general, two different methods have been proposed, namely *sorting* and *individual voltage balancing*, they are discussed following. It is noted that the selection of the balancing strategy can be conditioned in some cases by the modulation method.

3.5.1 Sorting Algorithm

The number of cells to be inserted in the upper and lower arms to obtain the desired output voltage are decided by the carrier disposition. The fact that not all the cells in the arm need to be inserted normally, leaves some degree of freedom to select the inserted cells. This degree of freedom can be used to balance the capacitor voltages. Sorting algorithms sort the capacitor voltages and select the cells to be inserted based on the capacitor voltage needs and the direction of the arm currents.

To balance the capacitor voltages, three different actions can be carried out: increase, decrease the capacitor voltage or keep it constant. Fig. 3.11-a) shows the effect over the capacitor voltage when a cell is inserted. If the arm current flows in the positive direction (see Fig. 3.8), the capacitor will be charged, its voltage increasing. On the contrary, if the arm current is negative, the capacitor will be discharged, its voltage therefore decreasing. In case the cell is not inserted (i.e. bypassed), current arm will not flow through the capacitor, its voltage remaining constant (Fig. 3.11-b).

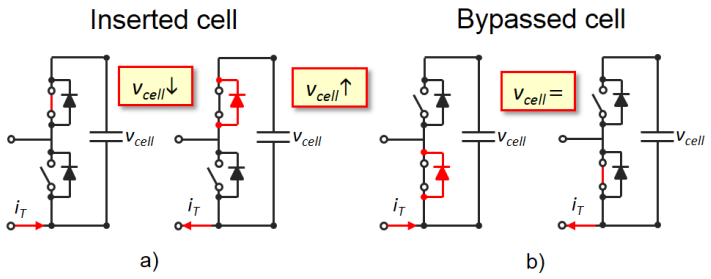

Figure 3.11: Submodule capacitor voltage balancing actions.

Fig. 3.12 illustrates the algorithm for phase u, the same applies for the other two phases.

Sorting algorithms can be used in principle with any carrier disposition. It must be noted however that this method may lead to unexpected commutations in the cells. Effectively, even if the total number of required submodules for two consecutive control periods does not change, it may happen that the sorting algorithm selects different submodules to be inserted/bypassed for the first and the second periods. This will results if an

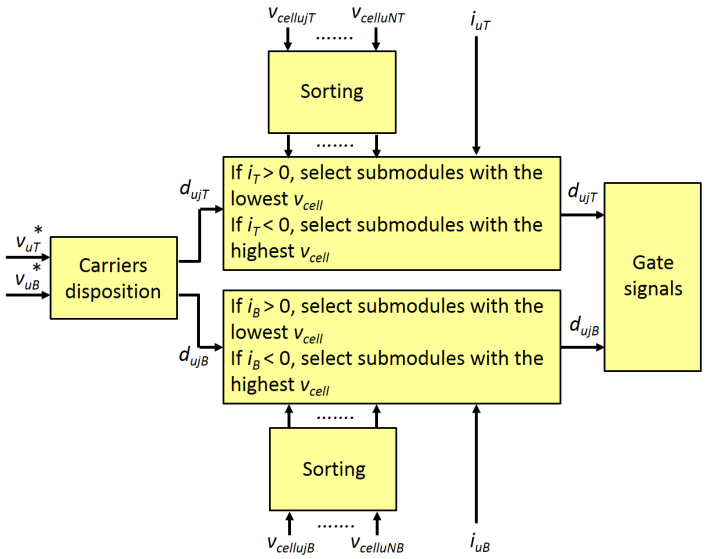

Figure 3.12: Block diagram including sorting algorithm approach.

undesirable increase of the commutations and consequently of the switching losses. Several methods have been proposed in the literature aiming to reduce the switching frequency when using sorting algorithms [70][71]. The lowest limit for the switching frequency occurs when all the cells switch once per cycle of the fundamental frequency, which is called *staircase modulation* [72][73].

3.5.2 Individual Capacitor Voltage Balancing

This approach was first proposed in [55], it is schematically shown in Fig. 3.13. An independent controller is assigned to each capacitor. If the capacitor voltage error is positive, i.e. the voltage is lower than the reference, and the arm current is positive, a positive voltage command will be generated. This voltage contribution will be added to the individual voltage reference for each cell coming from the overall arm voltage reference, which is common to all arm submodules. This positive voltage command increases the time that the cell is inserted (see Fig. 3.11). On the contrary, if the arm current is negative, the voltage contribution will be negative. This reduces the time that the cell is inserted, as inserting the cell in this case would reduce the capacitor voltage further.

A similar argumentation is used when the capacitor voltage error is negative, i.e the voltage is higher than the reference. In this case, the effects of a positive voltage command voltage will be positive when the arm cur-

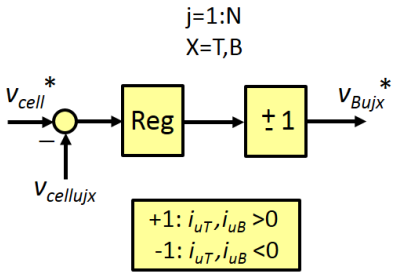

Figure 3.13: Individual capacitor voltage balancing.

rents are negative, as it increases the time that the cell is inserted, therefore discharging the capacitor.

It is finally noted that the use of individual capacitor voltage balancing poses restrictions on the modulation method, as it cannot be used with level-shifted modulation approaches. Unlike the sorting algorithm, the switching frequency is the same in all the cells since all of them commute each switching cycle. Obviously this will have an adverse effect on the switching losses and therefore on the overall efficiency of the MMC compared to sorting algorithms, which is considered a major drawback of the method.

Finally, it must be remarked that modulation and balancing strategies often cannot be selected independently. The choice of a certain modulation strategy determines the capacitor voltage balancing method that can be implemented. Level-shifted strategies require carriers covering the whole voltage range and cannot therefore be applied with individual voltage balancing methods (i.e. based on individual cell control). On the contrary, phase-shifted strategies can be used with individual cell references, allowing the use of the two balancing methods described above.

3.6 Control of the MMC

Control of the Modular Multilevel Converter is a challenging task, as multiple control objectives need to be satisfied simultaneously. They are listed below:

- AC-port active and reactive powers control. This is achieved through the control of the AC output voltage.
- DC cell voltage control.

- Circulating current control.
- Submodule capacitor voltage balancing.

A number of control strategies have been proposed. Intuitive *ad-hoc* approaches, are often used for the design and analysis of the control structure. Furthermore, the performance of a specific control configuration can be significantly affected by issues like the modulation strategy (see Section 3.4), the modes of operation of the MMC (e.g. constant AC voltage and frequency for the case of grid-connected MMC vs. variable voltage and frequency for the case of MMCs used in electric drives) and the sizing of the passive components (arm inductances and cell capacitors). To address these issues, a methodology for the analysis of the MMC control strategies is proposed in this thesis, mainly focused on the circulating current control and the relationship between modulation and capacitor voltage balancing methods.

3.6.1 Circulating Current Control Strategies

The circulating current is one of the distinguishing features of the MMC. A considerable number of strategies have been proposed for its control. Analysis and classification of the proposed methods is not trivial, as often the control of the circulating current is combined with balancing and modulation strategies.

Fig. 3.14 shows a generic block diagram for the circulating current control loop (per phase) and the different mechanisms that can be used to obtain the reference value. Different control actions can be combined to obtain the final arm voltage $v_{Lk}{}^*$. Switches S1 to S3 are used to indicate the actions that are selected, i.e. the control being used. The different strategies are discussed following, the brackets indicate which switches are open (S=0) or closed (S=1).

3.6.1.1 No circulating current control: Direct modulation

(S1=S2=S3=0) In this strategy there is no explicit control of the circulating current. The converter produces the commanded output voltage, which may come from outer current or power control loops. Capacitor voltage balancing is of course needed.

Though simple, this method has remarkable drawbacks. The circulating current contains a large component at $2\omega_e$, increasing the losses in the

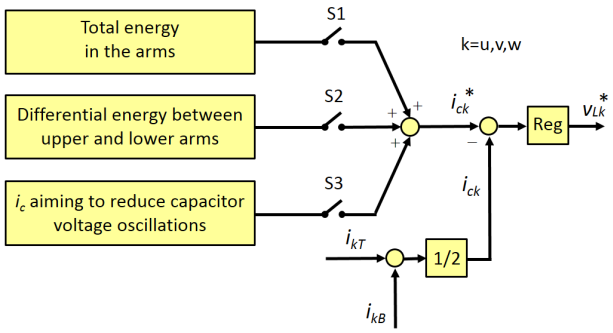

Figure 3.14: Circulating current control loop (per phase). k stands for u,v or w.

arm inductances and power devices, also producing large oscillations in the capacitor voltages. Moreover, the choice of the arm inductors and the cell capacitors can be critical due to potential resonance phenomena [92].

3.6.1.2 Suppression of the $2\omega_e$ component of the circulating current

(S1=S2=S3=0) A resonant controller is used to eliminate the $2\omega_e$ component of the circulating current. As for direct modulation, the DC component of the circulating current is not controlled, Fig. 3.14 therefore also applying in this case. This strategy is considered of little interest, as once a circulating current control loop is implemented, including the DC component in the control law would be straightforward.

3.6.1.3 Control of the DC component of the circulating current i_{cDC}

(S1=1, S2=S3=0) The combined arm power (3.12) reflects a power mismatch between the DC and AC sides. The last term in the right side of (3.12) can be neglected due to the small value of v_L. It is readily seen that the term $v_{ac} \cdot i_{ac}$ will produce two components in the arm power at DC and $2\omega_e$ respectively. The component at $2\omega_e$ will produce oscillations in the capacitor voltages, which can be acceptable. On the contrary, the DC component will produce an continuous increase/decrease of the capacitor voltage, which is obviously unacceptable. A DC circulating current i_c is then calculated and injected to make $v_{dc} \cdot i_c$ equal to the DC component of $v_{ac} \cdot i_{ac}$. The sum of all capacitor voltages can be used as the error signal to obtain the circulating current command which guarantees the power balance of the converter.

3.6.1.4 Control of the DC and $2\omega_e$ components of the circulating current: $i_{cDC} + 2\omega_e$

(S1=1, S2=S3=0) Also derived from (3.12), the circulating current can be used not only to balance the average power but also to reduce the $2\omega_e$ components of the capacitor voltage. This is done by injecting a circulating current of the form given by (3.14).

3.6.1.5 Control of the DC component and suppression of the $2\omega_e$ component of the circulating current

(S1=1, S2=S3=0) In this strategy, in addition to the control of the DC component of the circulating current, some type of current regulation strategy is implemented to cancel the $2\omega_e$ component of the circulating current. The goal of this strategy is to reduce the RMS value of the arm current, and therefore the losses in the arm inductors. However, this produces an increase of the $2\omega_e$ component of the capacitor voltage.

3.6.1.6 Control of the DC and ω_e components of the circulating current: $i_{cDC} + \omega_e$

(S1=1, S2=S3=0) Small power imbalances (3.13) can occur during the normal operation of the power converter between the upper and lower cells. As such imbalance cannot be compensated either by the DC or the $2\omega_e$ components of the circulating current, a component at ω_e in phase with the output voltage can be used for this purpose.

3.6.1.7 Circulating current control with high frequency circulating current injection (Motor drives)

(S1=1/0, S2=0, S3=1) A relatively new field of research is the use of the MMCs for medium voltage electric drives. The operation of the motor at low speed worsen the oscillations of the capacitors voltages. Strategies that have been proposed to solve this problem include control of the low frequency components and the modulation at high frequency of the circulating current. By doing this, the power oscillations in the cells are shifted to a higher frequency, significantly reducing the impact on the cells capacitor voltage. The desired circulating current reference includes both low and high frequency components (S3 in Fig. 3.14), different options have been proposed to obtain this current command (see references in Fig. 3.15).

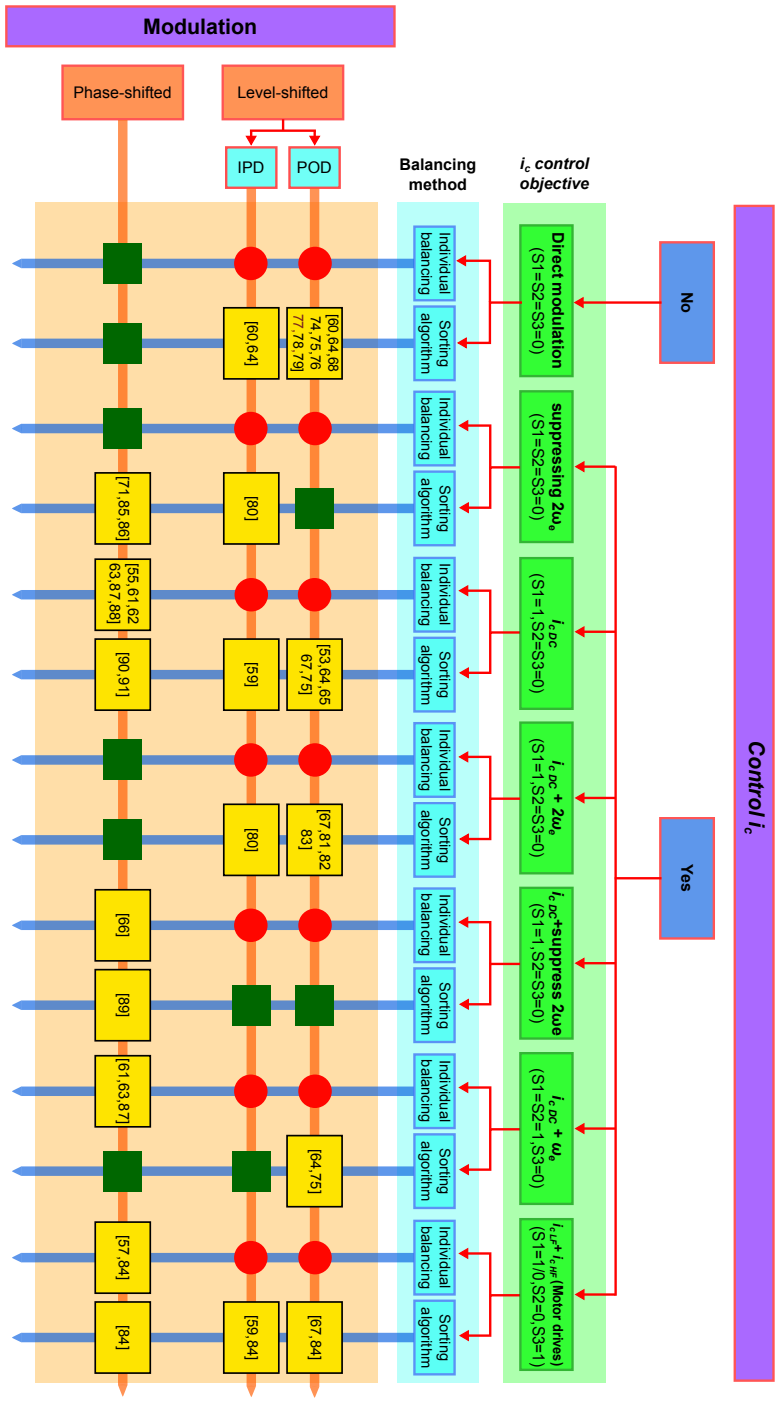

Figure 3.15: Classification of circulating current control and modulation methods for MMCs. References using *Phase-shifted* modulation in this figure implement *Interleaved carriers* (See Table 3.2).

Fig. 3.15 summarizes all the methods that have been discussed. Balancing and modulation strategies are also considered. Cells in green indicate configurations which though feasible, have not been reported in the literature. Cells in red indicate configurations which are not feasible.

To assess the differences in the performance of the aforementioned control methods, Fig. 3.16 shows the magnitude of the $2\omega_e$ component of both the circulating current and a capacitor voltage for four different control strategies. The magnitudes are shown in % of the worst case, which corresponds to direct modulation. It is readily observed the large magnitude of this harmonic both in the current and voltage for the direct modulation control strategy compared to any other method. By controlling the $2\omega_e$ component of the circulating current, this component as well as the oscillations of the capacitor voltage can be significantly reduced. However, as expected, suppression of the $2\omega_e$ component in the circulating current produces a slightly increase of the $2\omega_e$ component of the capacitor voltage.

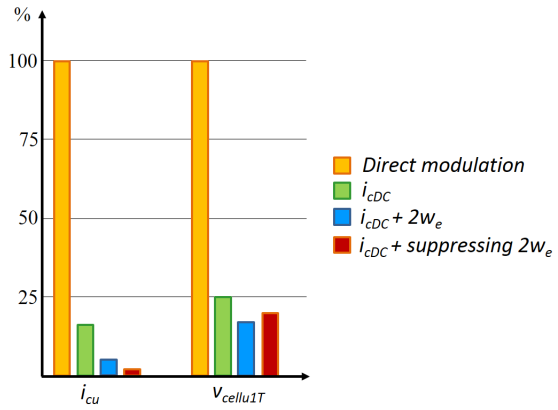

Figure 3.16: Simulation results. Magnitude of the $2\omega_e$ component of circulating current i_{cu} and a capacitor voltage $v_{cellu1T}$, for four different control strategies. Level-shifted POD modulation was used. The magnitudes are expressed in % of the worst case, which corresponds to direct modulation.

It is concluded from the previous analysis that direct modulation, though simple, leads to large $2\omega_e$ component of both circulating current (which implies increased losses in the arm inductances and power devices) and capacitor voltage (which can affect to the capacitors lifetime). Adding some type of circulating current control (especially the DC and $2\omega_e$ components) produces remarkable improvements, this option being normally preferred.

3.6.2 Overview of outer control loops

Unlike the control and modulation strategies discussed in previous sections, there is not a well established criteria concerning the general control structure for the Modular Multilevel Converter. Two schemes have been chosen as the most representative control structures for this kind of converters, they are shown in Fig. 3.17 and 3.18. It is noted that capacitor voltage balancing and modulation strategies are not fully independent and can require a coordinated design. Level-shifted approaches cannot be applied with individual voltage balancing methods, while phase-shifted options allow the use of both individual voltage balancing and sorting algorithm. Fig. 3.17 shows a overall control structure based on the sorting algorithm, which can be combined with any modulation scheme. Fig. 3.18 illustrates an equivalent structure but based on individual capacitor voltage balancing and phase-shifted modulation.

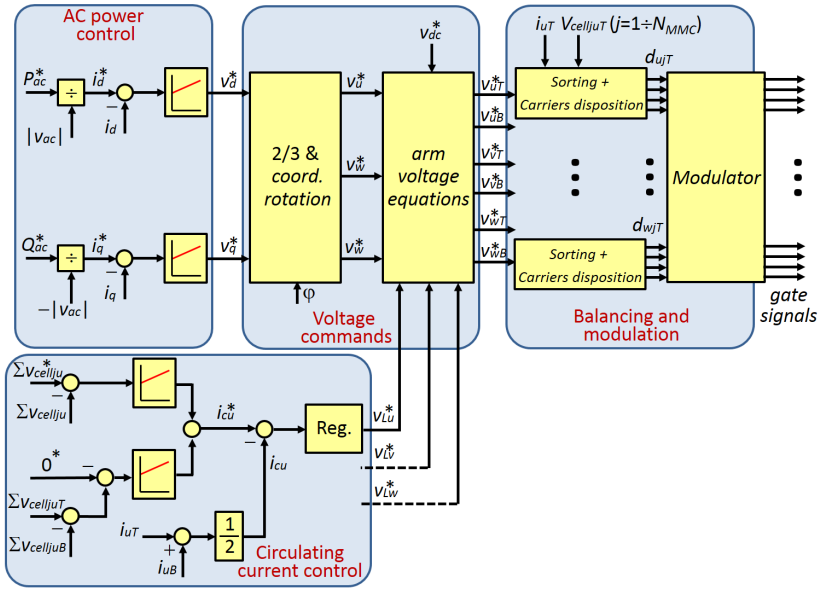

Figure 3.17: MMC overall control scheme based on sorting algorithm.

Some blocks are seen to be common to both structures:

AC-port power control: It is based on a conventional current vector control, in which d and q axis components are referred to a rotating reference frame aligned with the grid voltage vector (φ). d and q axis current commands may come from an outer active and reactive power control loop. Output of this block are the d and q AC voltage commands ($v_d{}^*$,$v_q{}^*$) to the modulation algorithms. Although not shown in the figure for shake of simplicity, d and q axis decoupling terms as well as feed-forward terms to

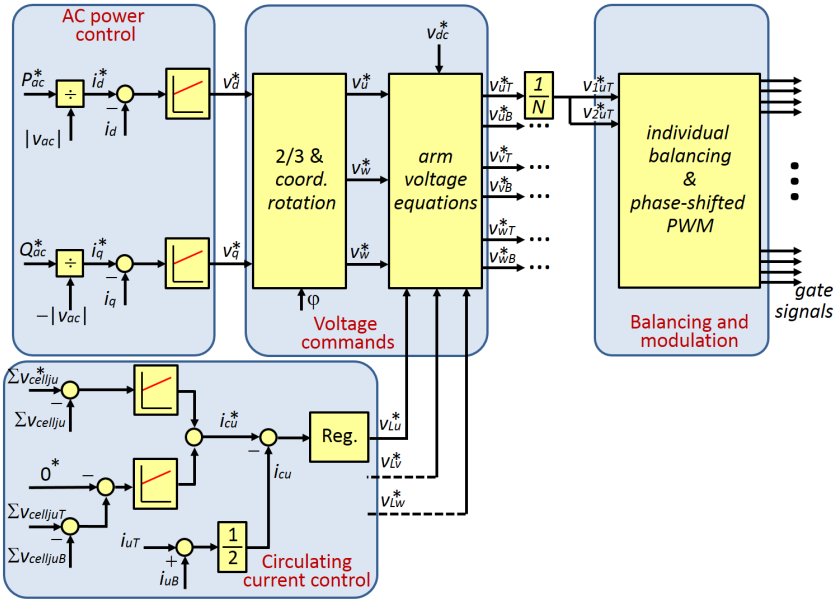

Figure 3.18: MMC overall control scheme based on individual capacitor voltage balancing.

compensate for the grid voltage can be included to improve the dynamic performance of the AC power control.

Voltage commands: AC voltage commands are rotated to a stationary reference frame and transformed into three-phase variables by means of Park transformation. AC voltage commands $(v_u{}^*, v_v{}^*, v_w{}^*)$, arm inductor voltage commands $(v_L u^*, v_L v^*, v_L w^*)$ and the command for the DC-port voltage $(v_{dc}{}^*)$ are combined using (3.6) and (3.7), to obtain the voltage commands for the submodules of top and bottom arms.

Circulating current control: Circulating current command can be implemented using different approaches (see Section 3.6.1). The sum of all capacitor voltages is used to keep the power balance of the converter ("Total energy in the arms" in Fig. 3.14), providing a current command with consist of two major components at DC and $2\omega_e$ respectively. An additional loop can be added aiming to cancel the voltage difference between the capacitors of top and bottom cells ("Differential energy between upper and lower arms" in Fig. 3.14), which produces a current command at the fundamental frequency ω_e. Finally, the control of the combined circulating current can be performed by different types of regulators, which normally operate in parallel; conventional PI controllers are used for the DC component and resonant controllers for specific AC components. The outputs of these controllers are combined to form the voltage to be applied to arm inductors.

Differences between both control structures mainly affect to the *balancing and modulation* block. Fig. 3.17 shows the sorting-algorithm-based structure. Arm voltage commands are converted into duty cycles by means of the specific carrier disposition and assigned to each individual submodule, according to the capacitor voltage balancing method based on the sorting algorithm. Finally, gate signals are produced. Fig. 3.18 shows a general control structure based on individual balancing. Unlike the previous approach, arm voltage commands are equally split among the cells. A certain voltage contribution is added to each individual voltage command in order to perform the capacitor voltage balancing (see Fig. 3.13). Finally, phase-shifted carriers must be used to generate the gate signals.

3.7 MMC Operation Under Voltage Constraints

MMCs are normally designed to operate in their AC side in the linear region. This fact constrains the peak-to-peak voltage in the AC port, which must be smaller than the DC port voltage. It is possible to increase the AC fundamental component of the voltage beyond this limit by using overmodulation strategies. However, this is at the price of an increase in the harmonic content (THD) of the voltages, and consequently of the currents and power. While this type of operation is not desired in principle, there are exceptional cases in which the MMC could be forced to operate in this mode. These would include transient conditions, e.g. temporary decrease of the DC port voltage below its rated value and temporary increase of the AC port voltage above its rated value, or quasi-permanent conditions, e.g. failure (and subsequent disconnection) of one or more cells in one or more arms of the MMC. Under these circumstances, the voltage margin between the DC and the AC port voltages required for the normal operation of the MMC might fade away. Consequently, the MMC will be forced to operate in the overmodulation region to maintain its power transfer capability, or be turned-off otherwise.

Voltage limits and the use of zero voltage sequence voltage components and overmodulation techniques applied to MMCs is discussed following.

3.7.1 AC vs. DC Voltage Ratio

A key aspect for the design and operation of the MMC, which is extensive in general to other three-phase converters, is the ratio between the DC link voltage and the AC port voltage. It is useful for analysis and comparison purposes to use the ratio between both voltages, as it indicates *how much*

of the available DC bus voltage is actually being used to produce the AC voltage. For a given v_{dc} and v_{ac}, this ratio is defined as (3.17) if triplen harmonics are added to the phase voltages, and increases to (3.18) (i.e. less margin between v_{dc} and v_{ac}) if triplen harmonics are not used.

$$R_{thi(pu)} = \frac{\sqrt{3} \cdot |v_{ac}|}{v_{dc}} \tag{3.17}$$

$$R_{no\ thi(pu)} = \frac{2 \cdot |v_{ac}|}{v_{dc}} \tag{3.18}$$

Fig. 3.19 shows the ratio R_{thi} (in %) vs. MMC power for already installed (or under development) MMCs that have been reported. It is interesting to note the dispersion of the data shown in this figure. Values of R_{thi} significantly lower than 100% means that the MMC has a large safety margin between its DC and AC ports voltages, and that therefore can likely operate within its voltage limits even in the event of anomalies, e.g. DC voltage lower than expected, or AC voltages larger than expected. Also this opens the opportunity to implement redundancy-based fault tolerant designs [94][95]. This would mean that it is possible to disconnect or by-pass faulty cells, without compromising the operation of the MMC. However, small values of R also implies a misuse of the power devices and of the cells in general, which obviously penalizes cost. On the contrary, for values of R closer to 100, a better use of the cells and power devices is made, but at the price of an increased risk of forcing the MMC to operate without the required safety voltage margin. Finally, values of $R > 100$ % will impede the normal operation of the MMC. Depending on the severity of this anomaly and its duration, these effects can be manageable by the MMC control algorithms, or can produce an inadmissible degradation of the voltages (and currents) or even unstable operation, and consequently, the disconnection of the MMC.

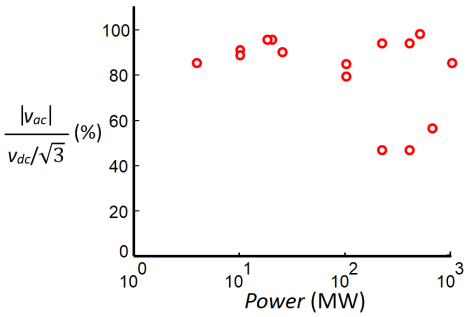

Figure 3.19: AC-to-DC voltage ratio R vs. power of already installed (or under development) MMC.

3.7.2 Voltage Limits of the MMC

For the discussion following, an MMC with four cells per arm ($N_{MMC} = 4$) is considered. It is noted that this does not imply any lost of generality. Fig. 3.20 shows the voltage vectors in the $d-q$ plane that can be produced by the MMC. Vertexes correspond to the voltage vectors that can be physically produced by the MMC, while the outer hexagon corresponds to the maximum voltage.

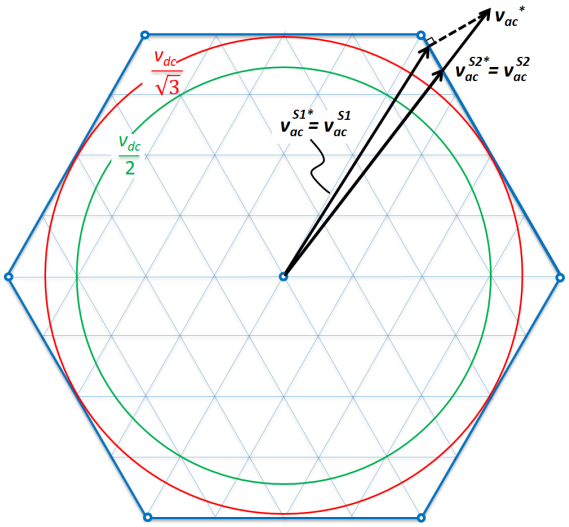

Figure 3.20: Voltage limits and overmodulation strategies for a grid-connected MMC with 4 cells per arm. Outer and inner circles correspond to the cases with and without zero sequence voltage (triplen harmonics) injection respectively.

As for other types of three-phase power converters, the maximum AC voltage that can be achieved will depend on whether zero sequence voltage components are used or not. The limits shown in Fig. 3.20 corresponds to the case when a zero sequence voltage (triplen harmonics) is added to the phase voltages, [93]. This corresponds to the physical voltage limit of the MMC in linear operation. The inner circle represents the voltage limit when triplen harmonics are not used. The use of triplen harmonics is seen to increase the voltage limit by an amount of $\approx 15\%$. However, this is at the price of injecting a zero sequence voltage between the DC port and the neutral voltage of the AC port. The peak value of the phase voltage in the AC side of the MMC is equal to the magnitude of the AC voltage complex vector (3.1), being limited to $v_{dc}/\sqrt{3}$ when triplen harmonics are added.

A difference regarding the use of zero sequence voltage components between conventional three-phase converters and the MMC, is that while for the first case the zero sequence voltage is applied to a set of three phase

voltages [93], for the MMC case there are six voltage references, i.e. top and bottom voltages (3.19)-(3.20) for phases u, v and w.

$$v_{kT}^{*} = \frac{v_{dc}}{2} - v_{k}^{*} - \frac{v_{Lk}^{*}}{2} \quad k = u, v, w \tag{3.19}$$

$$v_{kB}^{*} = \frac{v_{dc}}{2} + v_{k}^{*} - \frac{v_{Lk}^{*}}{2} \quad k = u, v, w \tag{3.20}$$

3.7.3 Overmodulation Strategies for MMCs

It is possible to increase the fundamental AC voltage supplied by the MMC with respect to the voltage limit in linear operation (outer circle in Fig. 3.20) by operating the MMC in the overmodulation region. This occurs whenever the commanded voltage vector is beyond the limit of $v_{dc}/\sqrt{3}$. Two different cases can be distinguished:

- Magnitude of the AC voltage vector command is larger than the voltage limit for linear operation, but smaller than the fundamental voltage obtained in six-step operation, i.e. $v_{dc}/\sqrt{3} \leq |v_{ac}^{*}| \leq v_{dc} \cdot 2/\pi$
- Magnitude of the AC voltage vector command is larger than the fundamental voltage achievable using six-step operation, i.e. $|v_{ac}^{*}| \geq v_{dc} \cdot 2/\pi$.

Voltage command v_{ac}^{*} in Fig. 3.20 is an example of this second case. Since this voltage command is permanently beyond the limits of the hexagon, it cannot be physically produced by the MMC. When this occurs, two different strategies are considered in this thesis to obtain a realizable voltage vector [93]:

Minimum phase error: With this approach, the magnitude is reduced to match the hexagon limits, the phase angle of the resulting voltage vector remaining unchanged. This corresponds to v_{ac}^{S2} in Fig. 3.20.

Minimum error: The vector command is projected on the hexagon, the resulting feasible voltage vector being v_{ac}^{S1}. It is noted that both magnitude and phase of the resulting voltage vector are modified with respect to the voltage vector command. This corresponds to v_{ac}^{S1} in Fig. 3.20.

Minimum phase error and *Minimum error* strategies allow to increase the fundamental component of the AC voltage vector beyond the limit of linear operation. However, this is at the price on an increase in the harmonic

content of the AC voltage, and consequently of the currents and power. The physical limit for the fundamental component of the AC voltage will occur when the MMC operates in a six-step mode, i.e. staying all the time at hexagon corners. The ratio R_{thi} can be increased with respect to the case of linear operation by an amount of $\approx 10\%$ in this case [96]. It is noted however that the six-step limit is unlikely to be used in practice, due both to power quality degradation as well as to MMC controllability issues.

It is finally noted that though space vector modulation representation has been used in the preceding discussion, sine-triangle modulators are often used in practical implementations. The DC-bus utilization by sine-triangle modulators can be increased to that of SVM through the use of zero sequence voltage components [93]. Centering the phase voltages with respect to the triangular carrier limits extends the maximum voltage in linear operation by $\approx 15\%$. After injecting the homopolar component, the modulator will come into overmodulation when two phase voltages touch the triangular carrier limits. This corresponds to touching the hexagon limit in Fig. 3.20, it is schematically shown in Fig. 3.21.

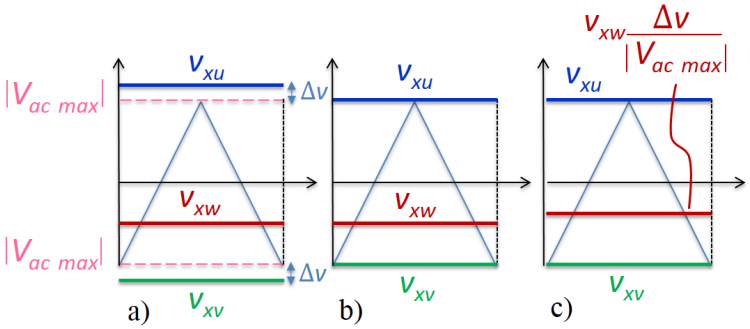

Figure 3.21: a) zero sequence voltage injection. Unlimited voltage vector; b) *Minimum error* (v_{ac}^{S1} in Fig. 3.20); c) *Minimum phase error* (v_{ac}^{S2} in Fig. 3.20).

If after injecting the homopolar component two phase voltages go outside the triangular carrier bounds (v_{xu} and v_{xv} in Fig. 3.21-a), they will be physically limited (v_{xu} and v_{xv} in Fig. 3.21-b and Fig. 3.21-c). If the third phase voltage remains unchanged (v_{xw} in Fig. 3.21-b), the resultant voltage vector will correspond to the minimum error SVM voltage vector. If it is reduced proportionally to the other two components reduction (v_{xv} in Fig. 3.21-c), the minimum phase error SVM voltage vector is obtained.

3.7.4 MMC Operation Under Voltage Constraints

MMCs are designed to operate in the linear region. However, under exceptional circumstances, they can be forced to operate with voltage restrictions, i.e. without enough voltage in the DC link to provide the desired AC voltage. Three types of events that result in values of a voltage margin $R_{thi} > 100$ have been considered:

- Decrease of the MMC DC voltage and/or increase of the MMC AC voltage (e.g. due to an increase of the grid voltage in grid connected MMCs) with respect to their rated values. Since the duration of such anomalies in the DC and/or AC voltages is in principle undefined, the MMC might need to withstand these operating conditions during relatively large periods of time.

- Sudden changes in the AC power, either due to changes in the power commands, or to disturbances in the AC side of the MMC. If this occurs, transients in the MMC voltage commands can produce a temporary lack of voltage. This situation should fade away after a relatively short time, but still will produce a transient disturbance in the operation of the MMC.

- Cell failure. One of the appealing properties of the MMC is its fault-tolerance capability. This can be achieved using redundant cells. If a cell fails in one arm, the remaining cells should be able to produce the commanded AC and DC port voltages and maintain the normal operation of the MMC. Ideally, the damaged cell would be replaced immediately and without discontinuing the operation. However, this might not be always the case in real practice. Failure of a cell in an MMC without spare cells, can force the MMC to operate with voltage constraints, or otherwise to stop its operation. In this case, the duration of the anomalies is in principle undefined, meaning that the MMC might need to withstand this operating conditions during a relatively large period of time.

The response of the MMC to these events will depend on the overmodulation strategy being used, as well as on the capability of the control loops to operate under voltage restrictions.

As described above, a particular case in MMCs occurs when a cell failure forces the converter to operate in overmodulation. As an example, when a cell in one arm fails and needs to be short-circuited. If there are not spare cells, this might force the MMC to operate into overmodulation.

The maximum AC port voltage that the MMC can supply as a function of the number of cells per arm N_{MMC} and the number of faulty cells M_f is given by (3.21), the voltage decrease in the AC port with respect to the case of no faulty cells being (3.22).

$$v_{ac} = \left(\frac{1}{2} - \frac{M_f}{N_{MMC}}\right) v_{dc} \frac{2}{\sqrt{3}} \tag{3.21}$$

$$\frac{v_{ac}}{v_{ac\,rated}} = \left(1 - \frac{2M_f}{N_{MMC}}\right) \tag{3.22}$$

Fig. 3.22 shows the variation of the AC port voltage limit as a function of the number of cells per arm for $M_f = 1$ (one faulty cell). The AC port voltage will reduce proportionally to the number of faulty cells. It should be also remarked that when half of the cells in one arm fail (i.e $M_f = N_{MMC}/2$), there is no capability to produce AC voltage, since all the voltage must be utilized to compensate the DC port voltage v_{dc}. It is noted that if there are no faulty cells, the available voltage is limited to the linear operation with zero sequence voltage injection ($v_{dc}/\sqrt{3}$). As the number of cells increases, the effect of a faulty cell is therefore decreased. Hence, the operation of the converter under overmodulation conditions is less likely to happen.

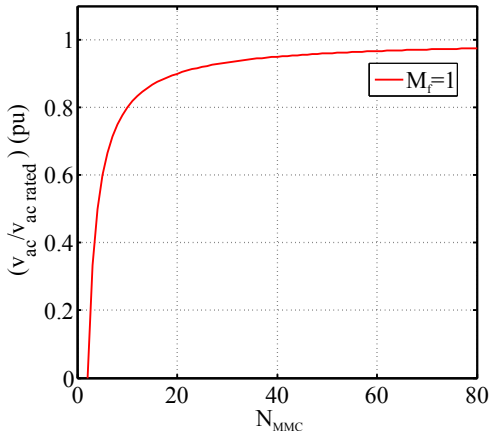

Figure 3.22: Reduction of the AC port voltage limit vs. number of cells per arm (N_{MMC}) in the event of one ($M_f = 1$) faulty cell.

Two different strategies can be used when damaged cells limit the voltage capability of one phase:

- Operate the MMC asymmetrically, i.e. with different number of cells in the arms/legs.

- Keep the symmetry among arms and legs by disabling M_f cells in the other two phases. This will limit however the maximum fundamental AC voltage.

The resulting voltage limits are shown in Fig. 3.23. Fig. 3.23-left, shows the case when the MMC is operated with a different number of cells in each leg. The voltage limits for each phase are now different, which results in an asymmetric hexagon. It is observed in this case that although the MMC is not able to supply an AC voltage command of $v_{dc}/\sqrt{3}$ (circle in red) operating in its linear region, it is possible to achieve the desired fundamental voltage if it operates in overmodulation. It is noted also that the limit to enter into the overmodulation region is now asymmetric. Fig. 3.23-right shows the case when the number of cells in the healthy phases is limited to be equal to the number of available cells in the faulty phase.

It is seen from the figure that the MMC cannot physically supply now the commanded voltage, not being able therefore to supply the required power. As a consequence, the MMC must be disconnected.

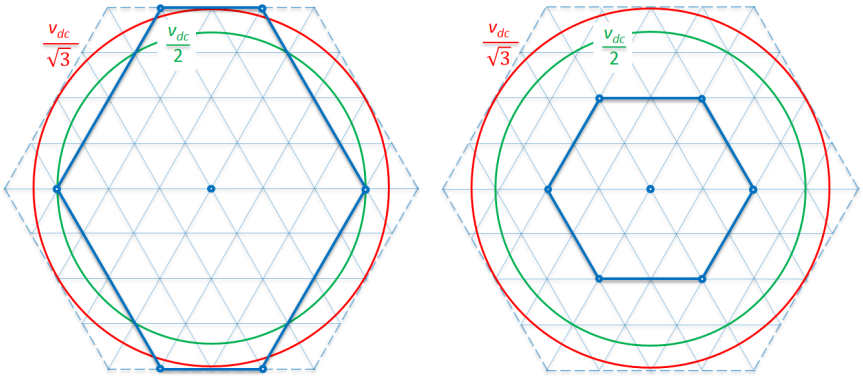

Figure 3.23: Overmodulation limits in the case of a faulty cell. Left- Asymmetric legs: $N_u = 3$, $N_v = N_w = 4$ in the top and bottom arms of one leg respectively. Right- Symmetric arms and legs: $N_u = N_v = N_w = 3$.

Comparing Fig. 3.23-left and Fig. 3.23-right, it is clear that the MMC can provide a significantly larger AC voltage in the first case, compared to the second case. However, this will produce an asymmetric behavior of the MMC, the harmonic content of the three phase voltages being therefore different.

3.7.5 Simulation Results

Simulation is used in this section to show the performance of the overmodulation strategies presented in Section 3.7.3, as well as the effects of a cell failure on the operation of the MMC under both asymmetric and symmetric operation (see Section 3.7.4).

The simulation model consists of a grid connected MMC with four cells per arm ($N_{MMC} = 4$). Homopolar voltage injection is used. Active and reactive powers for the AC side are commanded to the control. The same power profile will be used for all the simulations. Active power command increases linearly from 0 to $200kW$ between $t = 0$ and $t = 1.1s$.

Fig. 3.24 shows the AC active power, the fundamental component of AC voltage and the THD of the AC voltage vector, with the converter operating in normal conditions.

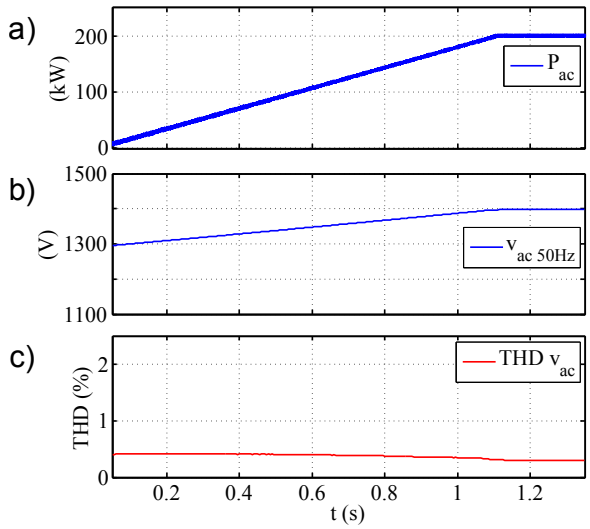

Figure 3.24: MMC in normal operation, i.e. without going into overmodulation. From top to bottom: a) AC active power, b) fundamental component of AC voltage; c) THD of AC voltage.

Fig. 3.25 and Fig. 3.26 show the MMC response when it is forced to operate into overmodulation, using *Minimum error* and *Minimum phase error* methods respectively. Current regulators used to control the injected AC power implement a *realizable references* strategy to operate under voltage constraints [93]. This avoids windup of the current regulator integrator, and provides a smooth transition between linear and saturated operation. It is noted from the figure that the lack of voltage reduces the power transfer capability (P_{ac} is slightly smaller than 200 kW in steady state). However, operation of the MMC is perfectly stable. It is interesting to note that *Min-*

imum error method (Fig. 3.25) produces a lower distortion (smaller THD) compared to *Minimum phase error* (Fig. 3.26). It is also observed from the figures that the oscillation of the capacitor voltages slightly increases, but remains under control. The most relevant harmonic components of the AC voltage vector occur at $-250Hz$ and $350Hz$, they are also shown in the figure.

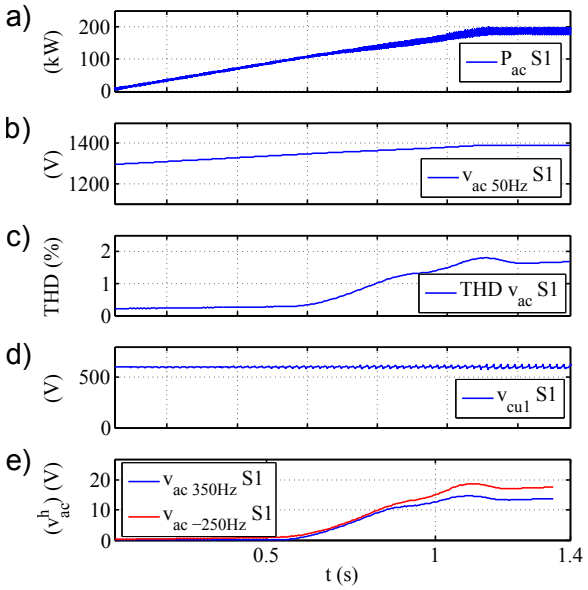

Figure 3.25: Simulation results. *Minimum error* ($S1$) overmodulation method. From top to bottom: a) AC active power, b) fundamental component of AC voltage, c) THD of AC voltage, d) voltage of one cell capacitor, e) 350Hz and -250Hz components of AC voltage vector.

It can be concluded that both *Minimum error* both *Minimum phase error* saturation methods can provide stable operation under voltage constraints. The oscillation of the cells capacitors voltage is maintained within reasonable limits, and without compromising the stability of the MMC.

Fig. 3.27 and Fig. 3.28 show the results when one cell in one arm fails. This forces the MMC to operate into overmodulation. For the *asymmetric* case, the other two phases are not modified. This corresponds to the case shown in Fig. 3.23-left. For the *symmetric* case, one cell is removed from every arm. This corresponds to the case shown in Fig. 3.23-right. It is observed that asymmetric operation (Fig. 3.27) provides a larger output voltage (and consequently allows an increased power transfer), while it does not imply a significant increase in the harmonic content in the output voltage. It is concluded that *asymmetric* configuration would be preferred over *symmetric* configuration. It is also observed that cells capacitors voltage oscillations increase but within reasonable limits and without compromising

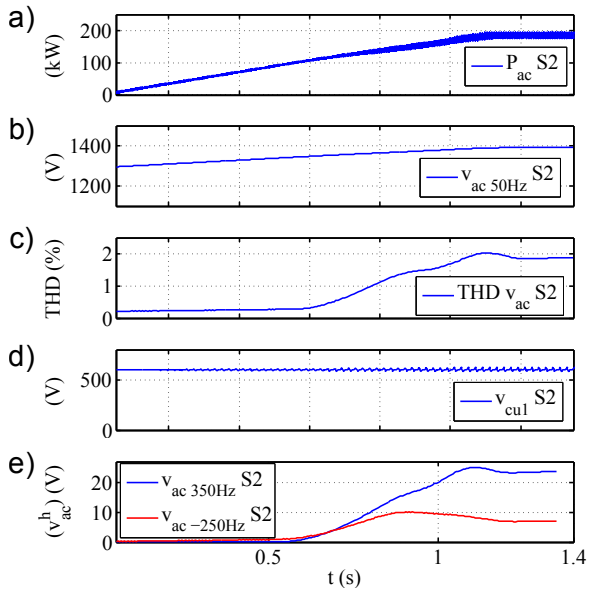

Figure 3.26: Simulation results. *Minimum phase error* ($S2$) overmodulation method. From top to bottom: a) AC active power, b) fundamental component of AC voltage, c) THD of AC voltage, d) voltage of one cell capacitor, e) 350Hz and -250Hz components of AC voltage vector.

the stability of the MMC.

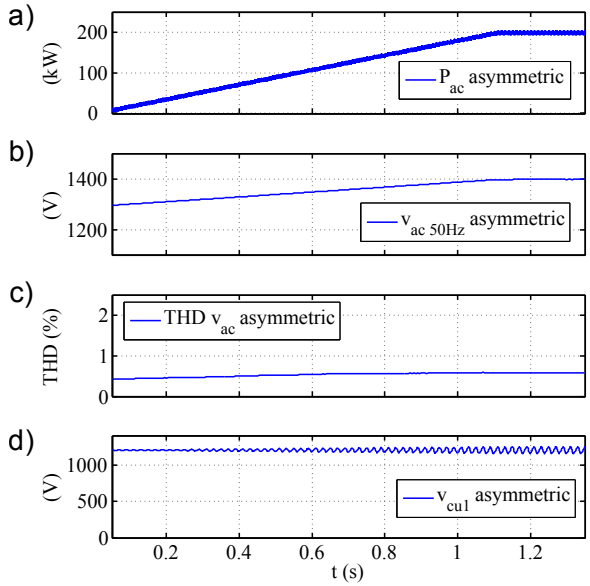

Figure 3.27: Simulation results showing the effects of a faulty cell using *Minimum error* overmodulation, for the case of *asymmetric* operation of the MMC.

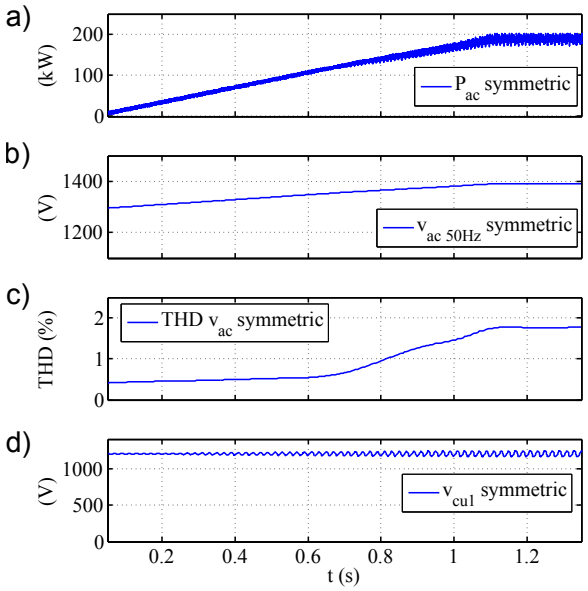

Figure 3.28: Simulation results showing the effects of a faulty cell using *Minimum error* overmodulation, for the case of *symmetric* operation of the MMC.

3.8 MMCs for Variable-Speed Drive Applications

The use of medium voltage adjustable-speed drives to replace constant speed machines, has gained significant acceptance over the last years as a viable option to improve the efficiency and performances in many applications as fans, blowers, compressors and pumps [8]. The use of multilevel converters topologies in motor drives, compared to the standard configuration with two levels, has several benefits. First of all, it allows to achieve large output voltages using devices of relatively reduced blocking capability. In addition, the wave shape of the output voltage waveform is significantly improved, reducing the current ripple and the resulting motor torque ripple, also mitigating other undesirable effects like common-mode voltage on ground leakage current and/or bearing current [56].

The use of MMC topology in motor drives has been a subject of intense research over the last years. While it provides all the aforementioned benefits, there are some concerns which are intrinsic to the MMC operation and which must be considered. It has been shown in the preceding sections that the submodule capacitor voltages experiment oscillations, the component at twice the output fundamental frequency being the most relevant. Voltage fluctuations can be modeled as (3.23) [56], where I is the motor RMS current, f is the fundamental frequency f, C_{cell} is the cell capacitance and $g(t)$ (3.24) *shapes* the voltage oscillations as a function of the modulation index

m_i and the motor power factor ϕ.

$$\tilde{v}_{cell} = \frac{\sqrt{2}I}{8\pi f C_{cell}} g(t) \tag{3.23}$$

$$g(t) = \frac{m_i^2 cos\phi}{2} \cdot cos\omega t - cos(\omega t - \phi) + \frac{m_i}{4} \cdot sin(2\omega t - \phi) \tag{3.24}$$

Line connected power converters operate with constant, relatively large fundamental frequency (typically 50 or $60Hz$, meaning that the oscillations are predictable and relatively small. On the contrary, variable speed AC drives operate with a variable frequency, including zero. This means that, independent of the capacitor size and the control strategy, there will be always a lower limit for the frequency at which the MMC can operate [56].

It is possible however to reduce the capacitor voltage oscillation by eliminating low frequency components in the arm/cell powers (see (3.10)(3.11)). This is done by shifting power oscillations to higher frequencies, reducing therefore the amplitude of the submodule capacitor voltage oscillations. Two different strategies can be used for this purpose [84]:

- Use of a high frequency common-mode phase voltage
- Shaping of circulating current by adding both low and high frequency components

With an adequate choice of the circulating current, low frequency terms of power fluctuations can be compensated such that the remaining terms occur at frequencies near the injected common-mode voltage frequency, which is chosen to be sufficiently high [84]. Eventually this allows stable operation of the converter at lower fundamental frequencies. Common-mode voltage wave-shapes proposed in the literature include among others, square-waves and sinusoidal-waves [57][59][84].

3.9 Summary

Modular Multilevel Converter (MMC) has been introduced in this chapter. MMC topology can be derived form the parallel connection of two CHBs, providing a high voltage DC link. In the end, the MMC mainly appears to answer the need of an AC-DC bidirectional multilevel converter

with a fully modular arrangement. Principles of operation, modeling and power balance equations have been analyzed in detail. Special attention has been paid to its distinguishing feature: the circulating current. Passive elements sizing, such as arm inductors and cell capacitors, have been also discussed.

Modulation strategies and capacitor voltage balancing methods have been studied. The choice of a certain balancing method may pose restrictions on the modulation strategy that can be applied, e.g. individual capacitor voltage balancing cannot be used with level-shifted modulation approaches. After that, control of the MMC has been presented, starting from the general control objectives and finally focusing on the different approaches for circulating current control. Most relevant control schemes have been also discussed, including the connection with capacitor voltage balancing methods.

Operation under voltage constraints has also been studied. It is possible to increase the AC fundamental component of the voltage beyond this limit by using overmodulation strategies. Operation of the MMC under voltage constraints have been analyzed, including operation in case of a faulty cell. Finally, the use of the MMC for variable-speed drive applications where the fundamental frequency varies, has been briefly discussed.

Chapter 4

MMC-based Multiport Power Converter and Solid State Transformers

This chapter firstly addresses the modification of conventional cells in the Modular Multilevel Converter to provide power transfer capability and thus, the transformation of this converter into the so-called MMC-based multiport power converters. Such multiport power converters can be asymmetric and symmetric, depending on the number and location of cells transferring power.

Different asymmetric topologies are analyzed, their feasibility based on power balance constraints being discussed. Limits of operation of cells with power transfer capability are studied in detail, including mathematical analysis and development of specific control strategies. The proposed methods are confirmed by means of simulation.

Symmetric approaches are then addressed as they are the basis for MMC-based solid state transformers. Similarly to the assymetric case, different configurations are analyzed, followed by a discussion of control strategies targeted for multiport power converters. Simulation results are then presented. Implementation of the control system for an MMC-based multiport power converter is also discussed. Finally, a comparative analysis between CHB and MMC-based multiport power electronic transformers is presented.

4.1 MMC Using Cells with Power Transfer Capability

Conventional MMCs use cells consisting of a half-bridge and a capacitor. Control and modulation strategies developed for MMCs are aimed to balance the power between the AC and DC ports, which is needed to maintain the average voltage of the cell capacitors at its target value. This is done by controlling the circulating current either explicitly or indirectly (i.e direct modulation, see Section 3.6). Balancing of the cell capacitors voltages is also required. Due to the fact that the cells have a limited energy storage capability, the net power balance for each cell is zero (neglecting losses), AC and DC powers being therefore equal to each other.

It is possible however to modify the cells design to provide power transfer (absorb or deliver) capability. This would enable the MMC with new potential features, including distributed energy storage [97]; integration of distributed energy resources (DER) at the cell level; multiport multilevel power converters combining the medium/high voltage DC and AC ports of the MMC with low voltage DC and AC ports. The resulting topology can also be seen as a SST [98]-[100] connecting a LVAC port and a HVAC port, but also providing a HVDC port. Such modification involves changes both in the cell design as well as in the control strategies. For the cell design, an electronic power converter will be needed in a general case to connect the power source transferring power to the cell (injecting or draining) with the cell capacitor. Depending on the characteristics of this power source (energy storage device, renewable energy sources, ...), unidirectional or bidirectional power flow capability can be needed. On the other hand, regarding the control strategies, the existing methods assume that all the cells in the MMC have similar design and operate identically. However, this is not true anymore if cells with the capability to transfer power are included, as it will be covered in following sections.

4.1.1 Modeling and Power Balance

Section 3.3 included modeling of the converter using complex vector notation. The same notation will be maintained in this chapter. In the current section, it is useful for analysis purposes to separate the MMC into its DC and AC subcircuits, as shown in Fig. 4.1. The discussion following assumes two cells per arm (N_{MMC}=2), without loss of generality. Also the voltage drop in the arm inductors is neglected for simplicity.

For the DC subcircuit (Fig. 4.1-left), all the cells are series connected, the

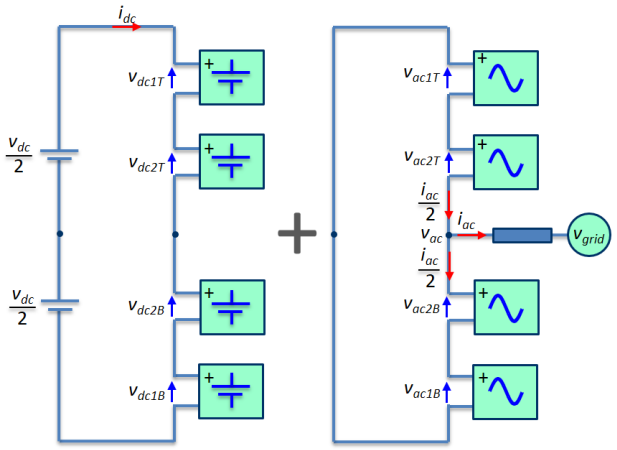

Figure 4.1: DC (left) nad AC (right) subcircuits of the MMC.

resulting voltage being equal to the DC-port voltage of the MMC (4.1). On the contrary, for the AC voltage subcircuit (Fig. 4.1-right), top and bottom arms are parallel connected, the corresponding AC cell voltages being (4.2) and (4.3) respectively. Consequently, AC current equally splits between the two arms as previously explained (3.3)(3.4).

$$v_{dcjT} = v_{dcjB} = \frac{v_{dc}}{2N_{MMC}}; \quad j = 1, 2 \tag{4.1}$$

$$v_{acjT} = \frac{v_{acT}}{N_{MMC}} = \frac{-v_{ac}}{N_{MMC}}; \quad j = 1, 2 \tag{4.2}$$

$$v_{acjB} = \frac{v_{acB}}{N_{MMC}} = \frac{v_{ac}}{N_{MMC}}; \quad j = 1, 2 \tag{4.3}$$

Since it has been assumed that the MMC is perfectly balanced (identical cells, identical operating points), the overall cell voltage is therefore (4.4)(4.5).

$$v_{jT} = v_{dcjT} + v_{acjT}; \quad j = 1, 2 \tag{4.4}$$

$$v_{jB} = v_{dcjB} + v_{acjB}; \quad j = 1, 2 \tag{4.5}$$

Fig. 4.2 graphically shows the DC and AC voltages for the MMC in Fig. 3.8 and 4.1 when operating with perfectly balanced cells. The AC voltages

and currents are represented by complex vectors. The real axis is selected to be aligned with the AC current vector, φ being the angle between the AC current and voltage vectors. Due to the limited energy storage capability of conventional cells, the power in the DC port has to be equal to the active power in the AC port (4.6), * standing for the complex conjugate. Assumed that the voltage in the DC side v_{dc} is constant, the MMC control has then to adjust the DC current to match the DC and AC powers (4.7)-(4.8). In addition, all cell capacitors voltages must be kept at their target values, e.g. using sorting algorithms or individual balancing (see Fig. 3.15).

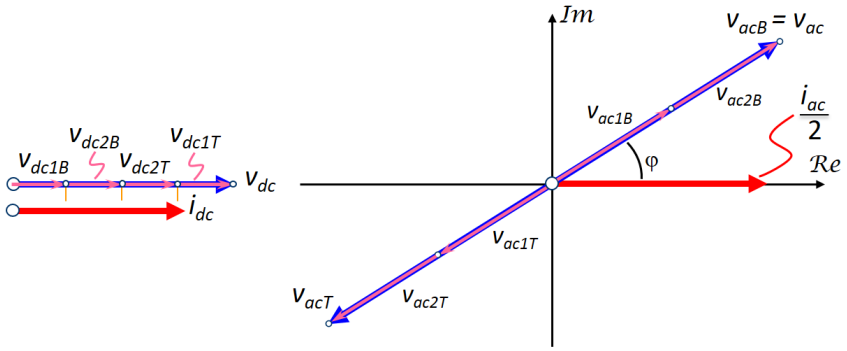

Figure 4.2: DC (left) and AC (right) voltages and currents.

$$P_{dc} = v_{dc} \cdot i_{dc} = P_{ac} = Re\left(v_{ac} \cdot {i_{ac}}^*\right) \tag{4.6}$$

$$P_{djT} = P_{djB} = \frac{v_{dc}}{2N_{MMC}} i_{dc} = \frac{v_{dc}}{4} i_{dc}; \quad j = 1, 2 \tag{4.7}$$

$$P_{ajT} = P_{ajB} = Re\left(\frac{v_{acT}}{N_{MMC}} \frac{{i_{ac}}^*}{2}\right) = Re\left(\frac{v_{acB}}{N_{MMC}} \frac{-{i_{ac}}^*}{2}\right) \tag{4.8}$$

As already mentioned, it is possible for the MMC to transfer power at the cell level. Assuming that cells are adequately controlled to maintain the capacitor voltage v_{cell} constant, transferring power to the standard cell design in Fig. 4.3-a) can be modeled as a current source connected to the cell capacitor, as shown in Fig. 4.3-b) [98]. It must be noted however that in a practical implementation, galvanic isolation between the cell capacitor and the power source will be normally needed. A current controlled dual active bridge (DAB) could be used for this purpose (Fig. 4.3-c) [97]-[100].

Since not all the cells in the MMC might necessarily have capability to transfer power, in the discussion following it is assumed without loss of

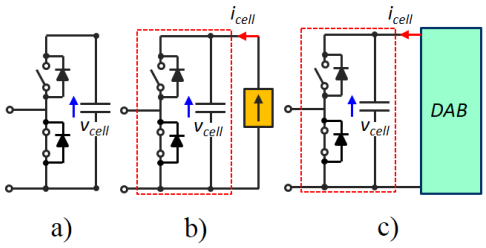

Figure 4.3: a) Conventional half-bridge cell with a capacitor in the DC link; b) cell including a current source; c) cell using a DAB.

generality that cells $1T$ and $1B$ account for all the cells that transfer power in the three phases, as shown in Fig. 4.4, while cells $2T$ and $2B$ account for conventional submodules.

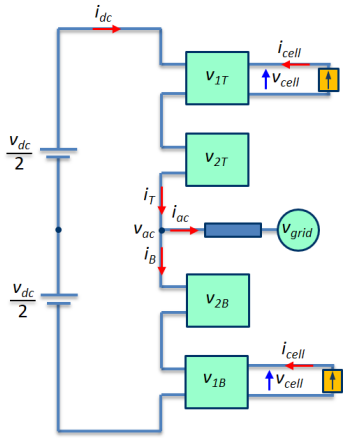

Figure 4.4: MMC including cells with power transfer capability in all the three phases. Same number of cells in top and bottom arms transfer power.

Use of cells with power transfer capability will affect to the power balance. The new power balance equation of the MMC including cells with power transfer capability is given by (4.9), where M_t stands for the number of cells transferring power per arm and P_{cell} corresponds to the power transferred by a complex vector cell (i.e. accounting for the three phases) both for top and bottom arms. The power balance equations for the individual cells are (4.10)-(4.13). It is noted that the power transferred by cells $2T$ and $2B$ is zero.

$$P_{dc} + P_{ac} + M_t \cdot P_{cell} = 0 \tag{4.9}$$

$$P_{cell1T} = P_{dc1T} + P_{ac1T} = v_{dc1T} \cdot i_{dc} + Re\left(v_{ac1T}\frac{{i_{ac}}^*}{2}\right) = v_{cell} \cdot i_{cell} \quad (4.10)$$

$$P_{cell2T} = P_{dc2T} + P_{ac2T} = v_{dc2T} \cdot i_{dc} + Re\left(v_{ac2T}\frac{{i_{ac}}^*}{2}\right) = 0 \quad (4.11)$$

$$P_{cell1B} = P_{dc1B} + P_{ac1B} = v_{dc1B} \cdot i_{dc} + Re\left(v_{ac1B}\frac{-{i_{ac}}^*}{2}\right) = v_{cell} \cdot i_{cell} \quad (4.12)$$

$$P_{cell2B} = P_{dc2B} + P_{ac2B} = v_{dc2B} \cdot i_{dc} + Re\left(v_{ac2B}\frac{-{i_{ac}}^*}{2}\right) = 0 \quad (4.13)$$

It is clear that differences in the power balance equation of the cells will imply asymmetries in their terminal voltages and/or currents. Since the DC current is common to all the cells, the asymmetries need to occur in the cell DC voltages v_{dcjT}, v_{dcjB}, AC voltages v_{acjT}, v_{acjB}, or in the AC component of the arm currents i_T and i_B.

In the discussion along this document, it is assumed that the asymmetries occur in the cell voltages (i.e. DC and AC voltages), modifying the AC component of the arm currents not being considered therefore. From this assumption, the DC and AC voltages equations can be rewritten as (4.14)-(4.15) and (4.16)-(4.17) respectively, Δv_{dc} and Δv_{ac} accounting for the DC and AC voltage imbalance among the cells in each arm. Fig. 4.5 shows both DC and AC voltage imbalances for the sake of clarity.

$$v_{dc1T} = \frac{v_{dc}}{4} + \Delta v_{dc} = v_{dc1B} \quad (4.14)$$

$$v_{dc2T} = \frac{v_{dc}}{4} - \Delta v_{dc} = v_{dc2B} \quad (4.15)$$

$$v_{ac1T} = \frac{v_{acT}}{2} + \Delta v_{ac} = v_{ac1B} \quad (4.16)$$

$$v_{ac2T} = \frac{v_{acT}}{2} - \Delta v_{ac} = v_{ac2B} \quad (4.17)$$

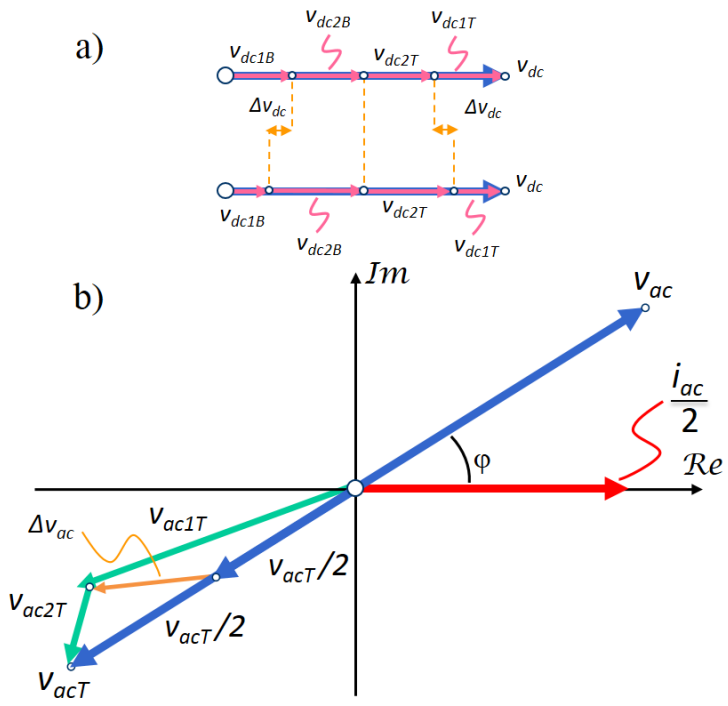

Figure 4.5: Voltage imbalance for $P_{ac} > 0$. a- DC cell voltage imbalance. b- AC cell voltage imbalance.

Since the AC voltage v_{ac} is a complex vector, Δv_{ac} will be a complex vector too. The real axis is selected to be aligned with the AC current vector (see Fig. 4.5 and Fig. 4.6). By doing this, the real part of the AC voltage imbalance vector $\Delta Re(v_{ac})$ only affects to the active power transferred by the cells. Different alternatives can be chosen when selecting the AC voltage imbalance [98]:

- Cells $1T$ and $1B$ keep the same voltage magnitude. However, its angle with respect to the AC current is different (Fig. 4.6-a).
- Cells $1T$ and $1B$ have different voltage magnitude, but its angle with respect to the AC current remains the same (Fig. 4.6-b).
- Real components of the voltage vector $\Delta Re(v_{ac1T})$ and $\Delta Re(v_{ac2T})$ are different, while imaginary components $\Delta Im(v_{ac1T})$ and $\Delta Im(v_{ac2T})$ are equal (Fig. 4.6-c).

While cases a) and b) imply modification of both real and imaginary part of the AC voltage vector, case c) is directly based on modifying the

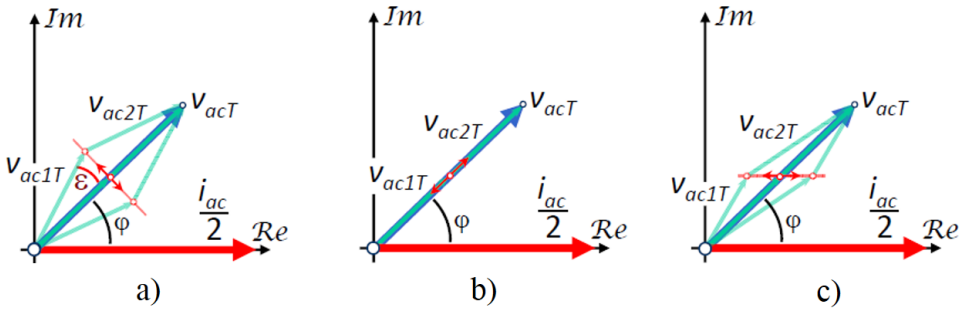

Figure 4.6: Strategies for the selection of the cell AC voltage imbalance. a- Same AC voltage magnitude b- Same angle with respect to the AC current c- Same imaginary component(Im(v_{ac1T})=Im(v_{ac2T})). In all the three cases the real component of AC voltage is changed.

real component and thus, affecting directly to the active power transferred by the cell $\Delta v_{ac} = \Delta Re(v_{ac})$. Consequently, case c) will be studied in more detail. It is finally noted that irrespective of the imbalances among cells being used, the overall DC and AC voltages of the MMC (4.18) and (4.19) must remain unchanged.

$$v_{dc1T} + v_{dc2T} + v_{dc1B} + v_{dc2B} = v_{dc} \tag{4.18}$$

$$v_{ac1T} + v_{ac2T} = v_{ac1B} + v_{ac2B} = v_{ac} \tag{4.19}$$

Using (4.10)-(4.17), it is possible to analyze the effects of Δv_{dc} and $\Delta Re(v_{ac})$ on the power transferred by the cells (4.10)-(4.13) and on the MMC power balance (4.9). Fig. 4.7-a shows the power transferred by cells $1T$ and $1B$ vs. Δv_{dc} and $\Delta Re(v_{ac})$, for constant AC power P_{ac} (Fig. 4.7-c). The power transferred by the cells is seen to affect to the power at the DC port of the MMC, (Fig. 4.7-b), (4.9) holding in all the cases. Power transferred by cells $2T$ and $2B$ is always zero. It can be concluded that the modification of the cell voltage (DC and/or AC voltage) affect to the cell power balance and consequently can be used to control cell power transfer. Detailed analysis of the effects of these voltage imbalances as well as limits of operation and physical constraints is performed following.

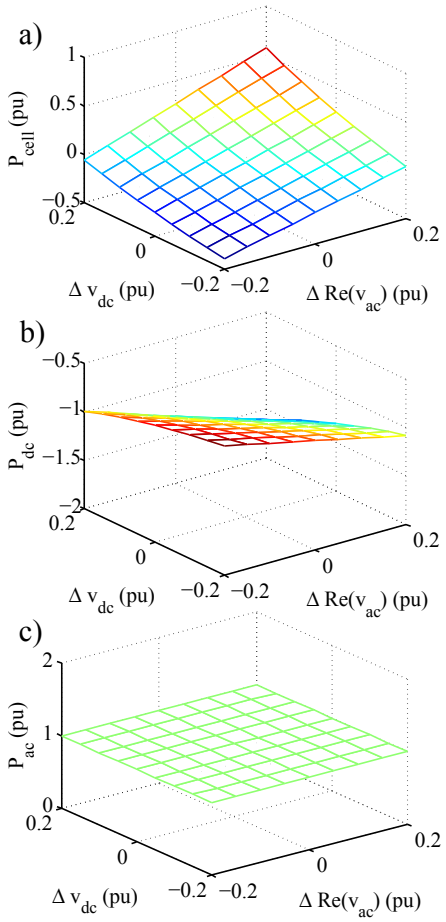

Figure 4.7: a) Cell power P_{cell}; b) DC port power P_{dc}; c) AC port power P_{ac}; as a function of Δv_{dc} and $\Delta Re(v_{ac})$, for constant AC power

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4.2 Asymmetric MMC-based Multiport Power Converter Topologies

The use of cells with power transfer capability opens new functionalities and uses for the MMC, including integration at the cell level of distributed energy storage, low-voltage/low-power sources/loads, and its operation as a multiport power converter, combining high and low voltage AC and DC ports. The adjective *asymmetric* has been used in order to describe MMC-based multiport topologies where not all the cells transfer power. Depending on the location (top/bottom arms and phases)(see 4.2.1) of the cells transferring power, as well as on the power being transferred by the MMC AC/DC ports (see 4.2.2), some constraints in the operation will appear. These asymmetries will lead to important consequences and constraints are discussed

following.

4.2.1 Types of asymmetries

Depending on the number and location of the cells transferring power (see Fig. 4.8), different types of asymmetries (imbalances) among cells, and consequently among arms or legs, can occur. In all the cases, all the cells in each leg of the MMC must have the same DC current.

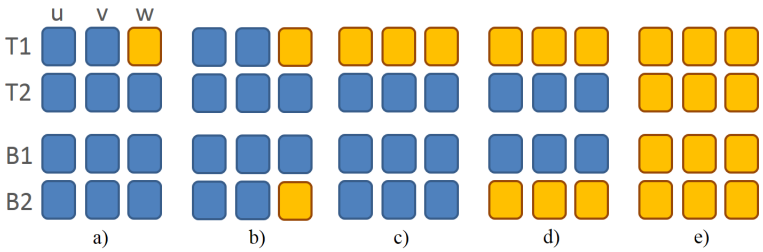

Figure 4.8: MMC configurations including cells with power transfer capability. Cells in light color transfer power, cells in dark color do not. a) asymmetric phases and arms; b) symmetric arms, asymmetric phases; c) asymmetric top and bottom arms; d) symmetric top and bottom arms, asymmetric cells; e) fully symmetric

In the discussion following, it is assumed that the AC current equally splits among the top and bottom arms of each leg. Accordingly, all the cells in each arm must have the same DC and AC currents. Consequently, producing asymmetries in the power transferred by the cells will necessarily imply asymmetries in their DC and/or AC voltages (4.14)-(4.17).

Table 4.1: Types of asymmetry and effects on the AC port depending on the applied cell voltage imbalance

Type of asymmetry	*Voltage imbalance*	*Effect on MMC operation*
Fig. 4.8-a)	Δv_{dc}	DC zero sequence in the AC port voltage
	$\Delta Re(v_{ac})$	Unfeasible
Fig. 4.8-b)	Δv_{dc}	DC zero sequence in the AC port voltage
	$\Delta Re(v_{ac})$	Different i_{cx} within phases
Fig. 4.8-c)	Δv_{dc}	DC zero sequence in the AC port voltage
	$\Delta Re(v_{ac})$	Unfeasible
Fig. 4.8-d)	Δv_{dc}	No effect
	$\Delta Re(v_{ac})$	No effect
Fig. 4.8-e)	$\Delta v_{dc} = 0$	No effect
	$\Delta Re(v_{ac}) = 0$	No effect

The different types of asymmetries are summarized in Table 4.1, the effects on the MMC/cells behavior is discussed following.

- Imbalances among phases and arms (Fig. 4.8-a) will result in different DC voltages for the cells in phase w, eventually resulting in a DC zero sequence voltage in the AC voltage vector v_{ac}. Unbalancing the cell AC voltages is not possible, since both top and bottom must generate the same AC voltage v_{ac} and the currents are the same.

- The case shown in Fig. 4.8-b, produces DC zero sequence voltage in the AC port when unbalancing the DC cell voltages. Unbalancing the AC cell voltages is also feasible, but will result in unbalances among phases in the circulating currents i_{ck}.

- Fig. 4.8-c produces imbalances between the DC voltage for the top and bottom arms of all the three phases, and consequently a DC zero sequence component in the AC voltage v_{ac}. Unbalancing the cell AC voltages is not possible due to the same reasons as case-a.

- In the case shown in Fig. 4.8-d, top and bottom arms are symmetric, but there are imbalances among the cells in each arm. Cell DC and/or AC voltages can be unbalanced in this case, but with no impact on the AC voltage of the MMC v_{ac}.

- Fig. 4.8-e does not produce any type of imbalance either in the MMC voltages or in the arm voltages.

4.2.2 Power Balance Constraints

MMCs including cells with power transfer capability must satisfy the power balance equation (4.9). However, there are constraints regarding the way in which the AC, DC and cell powers can be combined in (4.9) which need to be considered. Table 4.2 summarizes the different modes of operation and their feasibility for the particular case shown in Fig. 4.4 and Fig. 4.8-d.

Table 4.2: Power Transfer Modes (Topology in Fig. 4.8-d)

$Mode$	P_{cell}	P_{dc}	P_{ac}	Q_{ac}	$Feasible$
1	0	$\neq 0$	$\neq 0$	–	Yes ($P_{dc} + P_{ac}$=0)
2	$\neq 0$	0	$\neq 0$	–	Yes ($M_t P_{cell} + P_{ac}$=0)
3	$\neq 0$	$\neq 0$	0	0	Not feasible
4	$\neq 0$	$\neq 0$	0	$\neq 0$	Yes ($M_t P_{cell} + P_{dc} = 0$)
5	$\neq 0$	$\neq 0$	$\neq 0$	–	Yes ($P_{dc} + P_{ac} + M_t \cdot P_{cell}$=0)

- *Mode* 1.- Corresponds to the traditional operation of the MMC using cells with no power transfer capability. Power flows between DC and AC ports. It is noted that the dash in Table 4.2 indicates that reactive power has no effect.

- *Mode* 2.- In this mode all the cell power P_{cell} is transferred to the AC port. Cells that transfer power must modify their real part of AC voltage in order to achieve the adequate power imbalance, while cells that do not transfer power will handle reactive power, i.e. their AC cell voltage will be 90 degrees phase shifted with respect to the AC current.

- *Mode* 3.- Transferring the power from the cells to the DC port is not possible if there is no reactive power in the AC port. Since not all the cells transfer power (Fig. 4.8-d), is not possible to realized the required power balance for each cell, as the circulating current is common to all the cells. On the other hand, it must be remarked that this mode of operation becomes feasible for the fully symmetric topology in Fig. 4.8-e. In this case, the circulating current will balance the power in all cells.

- *Mode* 4.- Transferring the power from the cells to the DC port is only possible if there is reactive power in the AC port. A certain reactive current must exist in order to achieve the adequate power balance within each cell. Given a certain power transferred by the cells and a certain reactive current, cells will modify the real part of their AC voltage in order to achieve proper power balance, as shown in Fig. 4.9.

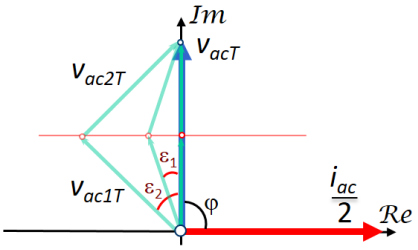

Figure 4.9: *Mode* 4: AC cell voltage imbalance.

As the reactive current increases, smaller imbalances in the AC voltage are needed (ε_1 vs ε_2). It must be noted that cells have limited voltage capabilities (v_{cell}), which are defined by means of the ratio (R) between the DC port and AC port voltages (see (3.17)(3.18)). It is noted that for the analysis developed along this section, (R) refers equally to both cases: with or without triplen harmonic injection. Considering the mentioned constraint, it is possible to define a minimum reactive

current that allows to create the necessary power imbalance in the cells. Fig. 4.10 shows the minimum reactive current (in pu) that is necessary to create a certain power imbalance in the cells, taking into account the voltage limitation in the cells. Different values have been included considering different voltage margins (R).

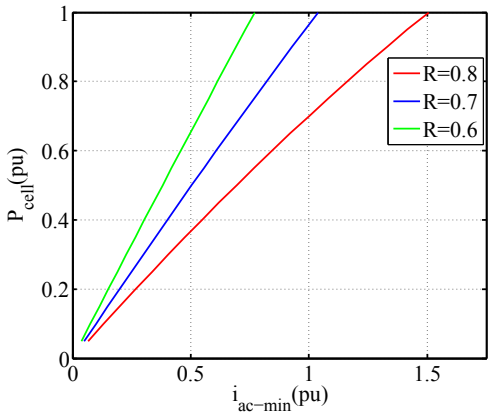

Figure 4.10: *Mode* 4: Minimum reactive current (in pu) to allow a certain power transferred by the cells (P_{cell}) as a function of three different ratios (R) between DC and AC port voltages.

As the ratio between the AC and DC-port voltages is smaller, the cells will be oversized and more voltage margin is available. As a consequence, smaller values of reactive current will be needed to achieve the same power imbalance, and eventually, the same power transferred by the cells.

- *Mode* 5.- Power flows among all ports of the MMC, which is perfectly possible by means of adequate selection of the voltage imbalance at each cell.

4.2.3 Limits of Operation of Cells with Power Transfer Capability

As explained in previous sections, it is possible to create certain power imbalances that are able to provide the cells power transfer capability. However, these imbalances are limited by certain constraints that must be eventually considered.

4.2.3.1 Submodules and MMC Voltage Limits

It has been shown in Section 4.1.1 that power transferred by cells is controlled by adequate selection of the voltage imbalance, the amount of power being transferred being proportional to $|\Delta v_{dc}|$ and $|\Delta Re(v_{ac})|$. The maximum power that can be transferred will depend therefore on the maximum voltage imbalance that can be produced. Consequently, cells and MMC voltage restrictions need to be considered.

Cells lower and upper voltage limits for half bridge cells are 0 and $v_{cell} = v_{dc}/N_{MMC}$ respectively. As for the MMC, the peak value of the AC voltage v_{ac} is limited to $-v_{dc}/2$ and $v_{dc}/2$. The ratio between the MMC AC and DC port voltages (3.18) will be therefore a key figure. It is noted that the line impedance voltage drop was neglected in this equation for simplicity. Triplen harmonic injection is also considered.

R indicates the voltage margin which is available to produce voltage imbalances among cells. For $R = 1$, all the cells operate at their voltage limit, no voltage imbalance being therefore possible. Values of $R < 1$ mean that a voltage margin exists to introduce imbalances among cells voltages.

The maximum power that cells can transfer will depend on:

- The voltage margin R
- The AC port power (active and reactive)
- The number of cells transferring power M_t

Fig. 4.11-a) and Fig. 4.11-b) schematically show the resulting DC and AC cell voltages, considering the imbalance limits $\Delta v_{dc\,max}$ and $\Delta Re(v_{ac\,max})$, which are function of the voltage margin R_{thi}. Subindex $1T$ and $1B$ account for all the cells in the top and bottom arms transferring power, and $2T$ and $2B$ for cells which do not transfer power. This representation is also valid for any particular case of voltage imbalance under positive active power without loss of generality.

Δv_{dc} and $\Delta Re(v_{ac})$ are selected according to the sign of the power being transferred by the cell (injected or drawn) and the sign of the AC power, as indicated in Fig. 4.12. Positive slope indicates that an increase of ΔP_{cell} implies an increase of $\Delta Re(v_{ac1T})$ or Δv_{dc1T}, opposite behavior occurring for the negative slope case.

Considering (4.10) and (4.20), for $P_{ac} > 0$, increasing the power injected by the cell (i.e. more negative cell power, according to the criteria defined by

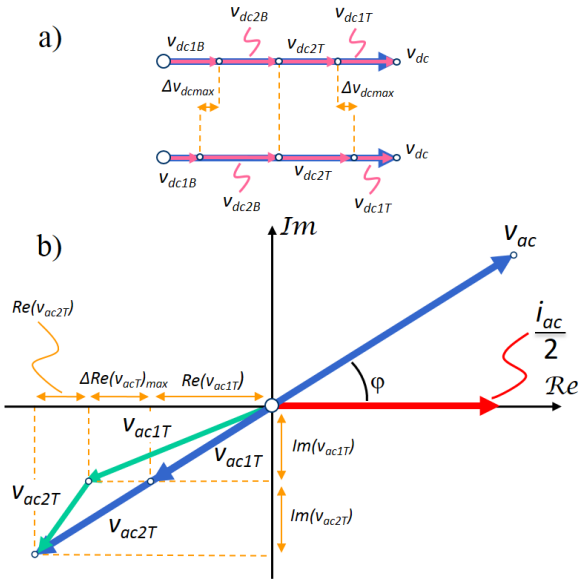

Figure 4.11: Voltage imbalance limits for $P_{ac} > 0$. a- DC cell voltage imbalance. b- AC cell voltage imbalance (real axis aligned with the AC current vector).

(4.9)) can be achieved either decreasing v_{dc1T} (less positive) and/or decreasing $Re(v_{ac1T})$ (more negative). Fig. 4.11 shows this particular case. On the contrary, if $P_{ac} < 0$, increasing the power injected by the cell can be done either increasing v_{dc1T} (P_{dc1T} becomes more negative) and/or decreasing $Re(v_{ac1T})$ (less positive). Fig. 4.12 illustrates all the cases.

$$P_{cell1T} = P_{dc1T} + P_{ac1T} \tag{4.20}$$

4.2.3.2 Maximum Power Transfer Using AC Voltage Imbalance

This subsection discusses the maximum power that can be transferred by the cells when the voltage margin R is used exclusively to produce an AC voltage imbalance. Since the d-axis is defined to be aligned with the AC current vector (see Fig. 4.11), the d-axis component of the voltage vector will be responsible of the AC active power and the q-axis voltage of the AC reactive power. The discussion following is particularized for the top arm voltages, identical conclusions are reached for the bottom arm voltages.

The maximum d-axis voltage that any cell can produce is given by (4.21), v_{acTq} being the q-axis voltage needed to supply the requested AC reactive

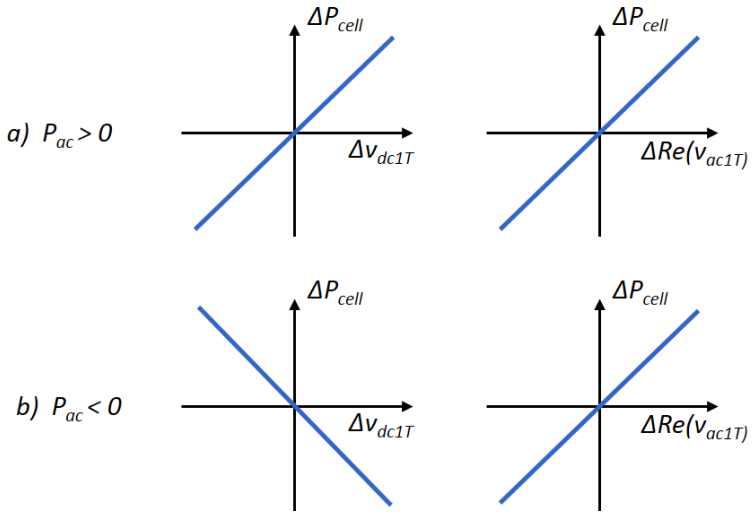

Figure 4.12: Variation in the power transferred by cells (ΔP_{cell}) as a function of variations in DC voltage imbalance (Δv_{dc1T}) and real part of AC voltage imbalance ($\Delta Re(v_{ac1T})$), for two cases: a) Positive AC-port active power $P_{ac} > 0$ and b) Negative AC-port active power $P_{ac} < 0$.

power.

$$v_{acTd\,max} = \sqrt{\left(\frac{v_{dc}}{2N_{MMC}}\right)^2 - \left(\frac{v_{acTq}}{N_{MMC}}\right)^2} \tag{4.21}$$

The actual AC voltage for each individual cell will depend on the sign of P_{ac}. For $P_{ac} > 0$, the maximum AC voltage of the cells injecting power is (4.21). The M_t cells injecting power account for a total voltage v_{ac1Td} (4.22). The $N_{MMC} - M_t$ cells which do not inject power account therefore for a total voltage of v_{ac2Td} (4.23). The overall AC voltage vector of the M_t cells injecting power and the $N_{MMC} - M_t$ cells which do not inject is given by (4.24) and (4.25) respectively.

$$v_{ac1Td} = M_t \cdot v_{acTd\,max} \tag{4.22}$$

$$v_{ac2Td} = v_{acTd} - v_{ac1Td} \tag{4.23}$$

$$v_{ac1T} = v_{ac1Td} + j\frac{v_{acTq}}{N_{MMC}} \tag{4.24}$$

$$v_{ac2T} = v_{ac2Td} + j\frac{v_{acTq}}{N_{MMC}} \tag{4.25}$$

Analogously, (4.26)-(4.29) hold for the case of $P_{ac} < 0$.

$$v_{ac2Td} = (N_{MMC} - M_t) \cdot v_{acTd\,max} \tag{4.26}$$

$$v_{ac1Td} = v_{acTd} - v_{ac2Td} \tag{4.27}$$

$$v_{ac1T} = v_{ac1Td} + j\frac{v_{acTq}}{N_{MMC}} \tag{4.28}$$

$$v_{ac2T} = v_{ac2Td} + j\frac{v_{acTq}}{N_{MMC}} \tag{4.29}$$

In both cases, (4.30) and (4.31) hold.

$$v_{dc1T} = \frac{v_{dc}}{2N_{MMC}} \cdot M_t \tag{4.30}$$

$$v_{dc2T} = \frac{v_{dc}}{2N_{MMC}} \cdot (N_{MMC} - M_t) \tag{4.31}$$

Considering that the total power transferred by the cells is expressed by (4.32) and the DC current can extracted from the power balance equation in the cells that do not transfer power (4.11), maximum power transferred by the cells can be performed (4.33).

$$P_{cell-total} = 2 \cdot P_{cell1T} = 2 \cdot (P_{dc1T} + P_{ac1T}) = 2 \cdot (v_{dc1T} \cdot i_{dc} + Re\left(v_{ac1T}\frac{{i_{ac}}^*}{2}\right)) \tag{4.32}$$

$$P_{cell\,max} = 3\left(\frac{v_{dc1T}}{v_{dc2T}}\, v_{ac2Td}\, \frac{i_{ac}}{2} + v_{ac1Td}\, \frac{i_{ac}}{2}\right) \tag{4.33}$$

In the end, the maximum power that can be transferred by the cells increases with the AC port current (i_{ac}) (see eq. (4.33)) and with the voltage

margin between the DC and the AC port voltage (see eq. (3.18)) (i.e. it is reflected in $v_{acTdmax}$, as shown in (4.21)(4.22))).

Finally, for practical implementation purposes, it is interesting to express the d-axis component of the AC voltage for the non-injecting cells ($2T$) and the injecting cells ($1T$) as a function the DC current i_{dc}, AC voltage v_{ac} and AC current i_{ac} (4.34)-(4.35). Alternatively, v_{ac2Td} and v_{ac1Td} can also be written as a function of the apparent power, load angle and power injected (or drained) by the cells.

$$v_{ac2Td} = -\frac{2}{3N_{MMC}} \frac{v_{dc}(N_{MMC} - M_t)i_{dc}}{i_{ac}} \tag{4.34}$$

$$v_{ac1Td} = v_{acTd} - v_{ac2Td} \tag{4.35}$$

4.2.3.3 Maximum Power Transfer Using DC Voltage Imbalance

Analogously to the preceding discussion, this subsection analyzes the maximum power that can be transferred by the cells when all the available voltage margin R is used to produce a DC voltage imbalance.

The maximum DC voltage imbalance ($|\Delta v_{dc}|$) that a conventional half-bridge submodule can handle is constrained by the maximum and minimum cell DC voltage (4.36)-(4.37), which depends on the AC-port and DC port voltages.

$$v_{dcT\,max} = \frac{v_{dc}}{N_{MMC}} - \frac{|v_{acT}|}{N_{MMC}} \tag{4.36}$$

$$v_{dcT\,min} = \frac{|v_{acT}|}{N_{MMC}} \tag{4.37}$$

Table 4.3 shows the DC voltage for the injecting and non-injecting cells v_{dc1T} and v_{dc2T}, as a function of the AC power sign and of the number of cells injecting power.

If $M_t > N_{MMC}/2$, i.e. there are more injecting than non-injecting cells, non-injecting cells will reach their voltage limit first. On the contrary, if $M_t < N_{MMC}/2$, i.e. there are more non-injecting than injecting cells, injecting cells will reach their voltage limit first. As an example, when the active power is positive, power transfer is achieved by reducing v_{dc1T}, as shown in

Table 4.3: DC voltage imbalance

P_{ac}	M_t vs. N_{MMC}	v_{dc1T}	v_{dc2T}
> 0	$M_t > N_{MMC}/2$	$\frac{v_{dc}}{2} - v_{dc2T}$	$v_{dcTmax}(N_{MMC} - M_t)$
< 0	$M_t > N_{MMC}/2$	$\frac{v_{dc}}{2} - v_{dc2T}$	$v_{dcTmin}(N_{MMC} - M_t)$
> 0	$M_t < N_{MMC}/2$	$v_{dcTmin}M_t$	$\frac{v_{dc}}{2} - v_{dc1T}$
< 0	$M_t < N_{MMC}/2$	$v_{dcTmax}M_t$	$\frac{v_{dc}}{2} - v_{dc1T}$

Fig. 4.12. Consequently, v_{dc2T} must increase. If the number of injecting cells is larger than the count of non-injecting cells ($M_t > (N_{MMC} - M_t)$), their voltage cannot be increased up to their limit, otherwise the remaining cells will run out of voltage. On the contrary, non-injecting cells voltage will be set to the upper limit v_{dcTmax}. In case $M_t = N_{MMC}/2$, i.e. the number of injecting and non-injecting cells is the same, both types reach their voltage limit simultaneously.

AC voltage sharing between the injecting and non-injecting cells is given in all cases by (4.38) and (4.39).

$$v_{ac1T} = \frac{v_{acT}}{N_{MMC}} \cdot M_t \tag{4.38}$$

$$v_{ac2T} = \frac{v_{acT}}{N_{MMC}} \cdot (N_{MMC} - M_t) \tag{4.39}$$

Maximum power that can be transferred by the cells is obtained from (4.33). As for the AC voltage imbalance case, for practical implementation purposes, the DC voltage for non-injecting and injecting cells can be expressed as a function the DC current i_{dc}, AC voltage v_{ac} and AC current i_{ac}, (4.40), (4.41).

$$v_{dc2T} = -\frac{3}{4}\frac{v_{ac2Td} \cdot i_{ac}}{i_{dc}} \tag{4.40}$$

$$v_{dc1T} = -\frac{v_{dc}}{2} - v_{dc2T} \tag{4.41}$$

Fig. 4.13 shows the maximum power that can be transferred by the cells, $P_{cell\,max}$, as a function of the apparent power S_{ac} and the AC load angle for three values of M_t, for the case of DC and AC voltage imbalances. Voltage margin between DC and AC ports has been set to $R_{thi} = 0.8$.

Fig. 4.13-left shows the maximum power when only a DC cell voltage imbalance is used. Peak values occur for the case of pure active power (0 and 180 degrees) in the AC port. In these cases, the ratio i_{dc} vs. $|i_{ac}|$ is maximum, so is the power transfer resulting from imbalances in the cell DC voltage. The maximum power capability occurs for the case of pure, negative active power. In this case, the MMC AC voltage decreases, increasing the voltage margin. On the contrary, it is not possible to transfer power by the cells if AC port power is purely reactive (i.e. 90 and 270 degress). This was expected, as in these case $i_{dc} = 0$, therefore imbalances in the cell DC voltage will not result in any power transfer.

It is seen from Fig. 4.13-left-a) and b) that increasing the number of active cells M_t increases the power transferred. However, there is a limit for this, which occurs when the number of cells injecting equals the number of cells which do not inject (i.e. $M_t = N_{MMC}/2$). Increasing M_t beyond this limit does not increase the overall power transfer (see Fig. 4.13-left-b) and c)). This is due to the fact that the overall DC port voltage v_{dc} has to be shared by all the cells while the DC current remains the same.

Fig. 4.13-right column shows the power transferred by the cells when only an AC cell voltage imbalance is used. Unlike the previous case, maximums of the transferred power occur when the AC power is reactive (90 and 270 degrees). The reason is that the voltage margin needed to produce the voltage imbalance increases when there is no active power. It is noted that in this case, the power transferred increases with the number of cells transferring power M_t.

According to Fig. 4.12, for positive values of active power, real part of AC voltage must be decreased (i.e. more negative results in an increase of its absolute value). Power injection capability is enhanced when there are more injecting than non-injecting cells (see Fig. 4.13-right-c, for power angles between -90 and +90 deg). On the other hand, when active power is negative, real part of AC voltage must be decreased (i.e. less positive results in a decrease of its absolute value) so that the cell voltage limit is reached first by the cells that are not injecting. Power transfer capability is in this case is enhanced when there are more non-injecting than injecting cells (see Fig. 4.13-right-a, between 90-270 deg). This behavior has been confirmed by numerical analysis.

It is concluded from the previous discussion that for any value of the apparent power and load angle, use of AC voltage imbalances (Fig. 4.13-right) allow to transfer more power compared to the use of DC voltage imbalances (Fig. 4.13-left).

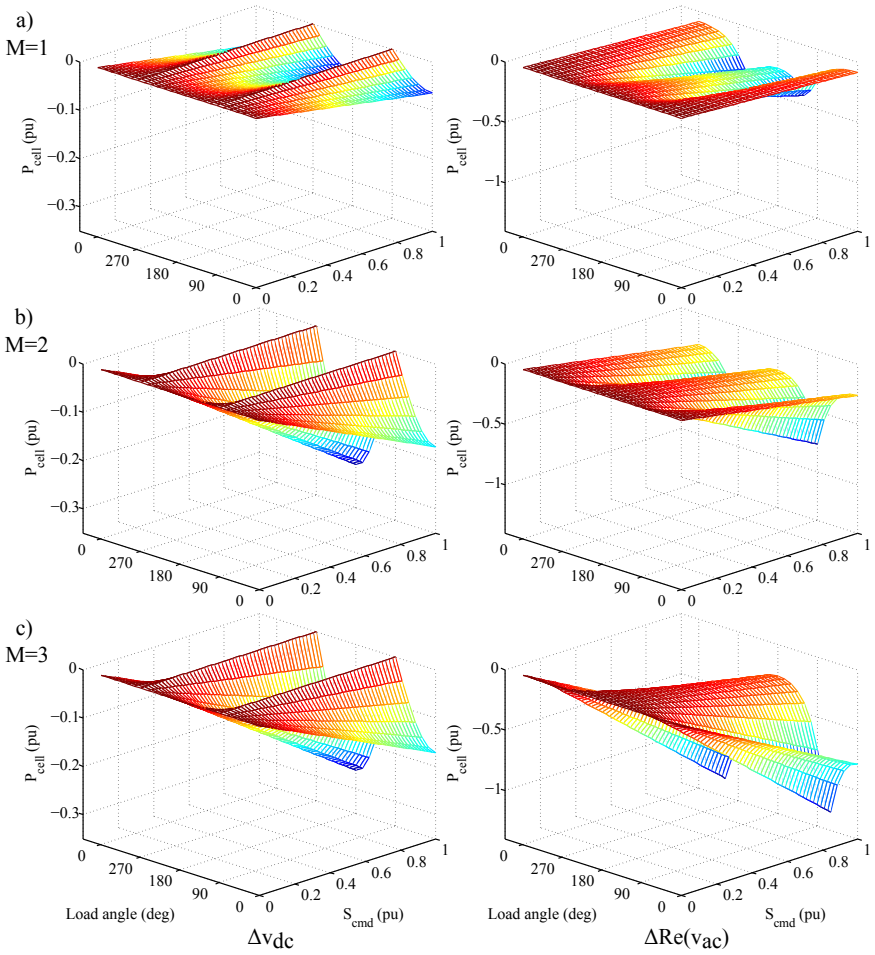

Figure 4.13: Maximum power transferred by the cells for a) $M_t = 1$, b) $M_t = 2$ and c) $M_t = 3$ ($N_{MMC} = 4$), as a function of the apparent power and load angle, for the case of DC (left) and AC (right) voltage imbalances. $R_{thi} = 0.8$ (fixed).

4.2.4 Modified Control Strategies Using Cells with Power Transfer Capability

The use of cells with power transfer capability poses new challenges regarding control and modulation strategies, as the existing methods are aimed to balance the operation of cells which have an identical design and operate identically [55][59][75][76][79][88][89]. It has been shown in the previous sections that the power transferred by the cells can be controlled by adequate selection of the voltage imbalances Δv_{dc} and $\Delta Re(v_{ac})$. Consequently, control strategies which provide individual voltage commands for each cell are convenient. A key feature of the potential methods will be therefore whether they use sorting algorithms or individual balancing (see

Fig. 3.15). Two different approaches are discussed following:

- Without explicit selection of Δv_{dc} and $\Delta Re(v_{ac})$
- With explicit selection of Δv_{dc} and $\Delta Re(v_{ac})$

4.2.4.1 No explicit selection of Δv_{dc} and $\Delta Re(v_{ac})$

Control strategies using sorting algorithms for balancing do not allow to generate individual voltage commands (see section 3.5). Still these strategies allow to control the power transferred by the cells thanks to the combined action of the circulating current control and the sorting algorithm. However, no explicit values for $\Delta v_{dc}$and $\Delta Re(v_{ac})$ are given. This means that for a given power in the AC side and a ratio R, it is not guaranteed that the cells will transfer the maximum possible power [98].

4.2.4.2 Explicit selection of Δv_{dc} and $\Delta Re(v_{ac})$

It is possible to control the power transferred by the cells by explicitly selecting Δv_{dc} and $\Delta Re(v_{ac})$. Fig. 4.14 shows the control strategy proposed in this work. Since individual voltage references are needed at the cell level, the control scheme is mainly based on individual capacitor voltage balancing and phase-shifted modulation, as already discussed in Section 3.6.2 and Fig. 3.18.

In Fig. 4.14 voltage commands ${v_d}^*$ and ${v_q}^*$ are referred to a reference frame in which d-axis is aligned with the grid voltage angle φ_{grid}. It is also assumed that the number of cells transferring power M_t is known in advance. *Voltage commands* block uses (4.34)-(4.35) to obtain the AC voltage imbalance required to transfer the cell power. This block operates in a reference frame aligned with the AC current (φ). The power transferred by the cells is intrinsically reflected in the DC current. Hence, the AC voltage for the cells that are injecting and non-injecting power can be easily obtained in real time using (4.34)-(4.35).

Similarly, (4.40)-(4.41) are used to obtain the DC cell voltage imbalance. It was already mentioned that AC voltage imbalances allow to transfer larger amounts of power compared to DC voltage imbalances. Therefore DC voltage imbalances can be disregarded, the DC port voltage being in this case evenly split among all the cells.

Once the required AC and DC cell voltages are set, (4.42)-(4.43) are used

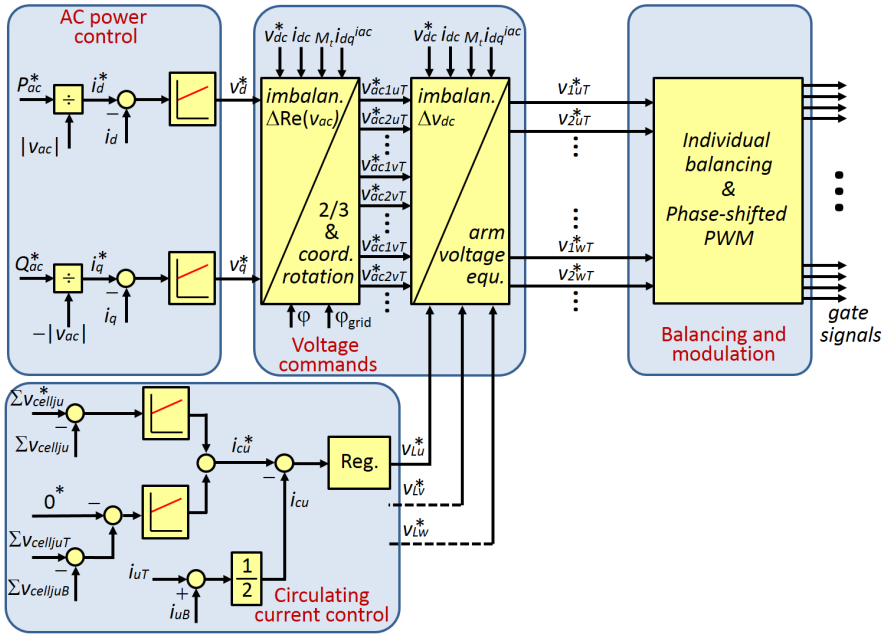

Figure 4.14: Explicit selection of AC and/or DC cell voltage imbalances. Proposed MMC control.

to obtain the overall cell voltages. Individual balancing and phase-shifted modulation are used further to obtain the necessary gate signals.

$$v^*_{jkT} = v_{dcjT} - v^*_{acjkT} - \frac{v^*_{Lk}}{2N_{MMC}} \quad j = 1 : N_{MMC}; \quad k = u, v, w \tag{4.42}$$

$$v^*_{jkB} = v_{dcjB} + v_{acjkB} - \frac{v^*_{Lk}}{2N_{MMC}} \quad j = 1 : N_{MMC}; \quad k = u, v, w \tag{4.43}$$

4.2.5 Control Strategies: Simulation Results

Simulation results are included in this section showing the performance and validity of the control strategy designed to operate with cells with power transfer capability.

The operation of an MMC with four cells per arm including cells with power transfer capability has been simulated using Matlab/Simulink. The control block diagram in Fig. 4.14 with AC voltage imbalance $\Delta Re(v_{ac})$

was used, as it allows to transfer more power compared to DC voltage imbalances.

Fig. 4.15 shows the control behavior in two different scenarios, with purely active and puerly reactive power in the AC port respectively. The AC power command follows a ramp until t=0.1sec. At t=0.3 sec, the cells with power transfer capability start injecting power according to a ramp too, reaching their rated power at t=0.4 sec. The AC port active and reactive powers remain unaffected, since they are controlled to be constant. Consequently, power injected by the cells affects to the DC power, which is controlled through the circulating current. Capacitor voltage for the two cells transferring power, $v_{cell1uT}$ and $v_{cell1uB}$, shows a small transient disturbance, which is readily controlled by the arm balancing control and the capacitor voltage balancing.

Table 4.4: Simulation results. AC voltage imbalance.

	v_{ac1Td}(V)		v_{ac1Tq}(V)		v_{ac4Td}(V)		v_{ac4Tq}(V)	
	before	after	before	after	before	after	before	after
$M_t = 3$ $\varphi = 0^o$	-341.1	-371.8	-21.75	-21.75	-341.1	-248.13	-21.75	-21.75
$M_t = 2$ $\varphi = 90^o$	-14.97	-116.54	-343.44	-343.44	-14.97	86.61	-343.44	-343.44

Table 4.4 shows the real and imaginary components of the cells AC voltage vectors for the two cases shown in Fig. 4.15, without and with cell power transfer. It is noted that real component of the voltage for cells transferring power v_{ac1Td} increases, while the imaginary component v_{ac1Tq} remains constant. Cells which do not inject power decrease the real component of their AC voltage v_{ac4Td}, which is required to maintain the power balance and to provide the required AC voltage (4.19).

4.3 Symmetric MMC-based Multiport Power Converter Topologies: MMC-based SST

This section describes MMC multiport topologies in which all the cells have power transfer capability, i.e. being therefore *symmetric*(see Fig. 4.8-e) [101][102]. It is assumed that a DAB is used to transfer power to the cells providing galvanic isolation, as shown in Fig. 4.3-c.

In this configuration, all the cells operate in the same working conditions, provided that they transfer a similar amount of power. Due to this, control of

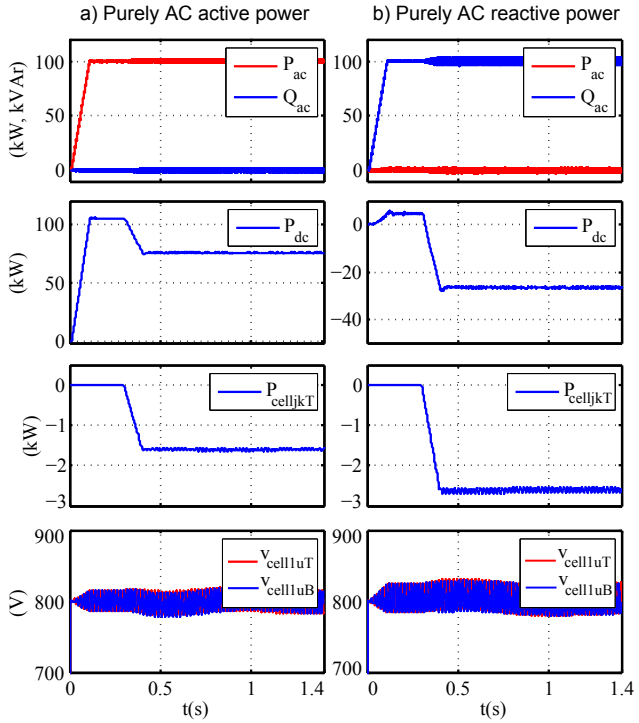

Figure 4.15: Simulation results. MMC with four cells per arm ($N_{MMC} = 4$). From top to bottom: AC active and reactive powers, DC port power, power injected by one cell, capacitor voltages for cells #1T and #1B of phase u. a) $P_{ac} = 100$ kW, $Q_{ac} = 0$ kVA, $M_t = 3$, $M_t \cdot P_{cell} = -28.8$ kW; b) $P_{ac} = 0$ kW, $Q_{ac} = 100$ kVAr, $M_t = 2$, $M_t \cdot P_{cell} = -31.2$ kW. (k=u,v,w)

the MMC is significantly simpler compared to the case described in Section 4.2. This arrangement is analyzed in detail as follows, as it will be the basis for the proposed multiport power converter topology.

4.3.1 MMC Based Multiport Power Converters

Providing the cells of the MMC the capability to transfer power opens several opportunities to realize multiport power converters. Examples of these are shown in Figs. 4.16-4.18. In all the configurations shown in these figures, the left-side of the power converter corresponds to MMC AC and DC ports, and will be considered as the high-voltage (HV) side. For simplicity, the MMCs in the figure use two cells per arm ($N_{MMC} = 2$). However, all the discussion following can be extended to any value of N_{MMC} without any loss of generality. In all the cases, the isolation between the high voltage (HV) and low voltage (LV) AC ports is provided by DABs. It is also observed that in all the implementations, each cell of the MMC is connected to a

DAB, meaning that the modularity of the MMC is extended to the isolation stage formed by the DABs. The right side of the power converter in Figs. 4.16-4.18 will be considered as the LV side. It is seen that the differences among the different topologies shown in Figs. 4.16-4.18 only affect to the LV side.

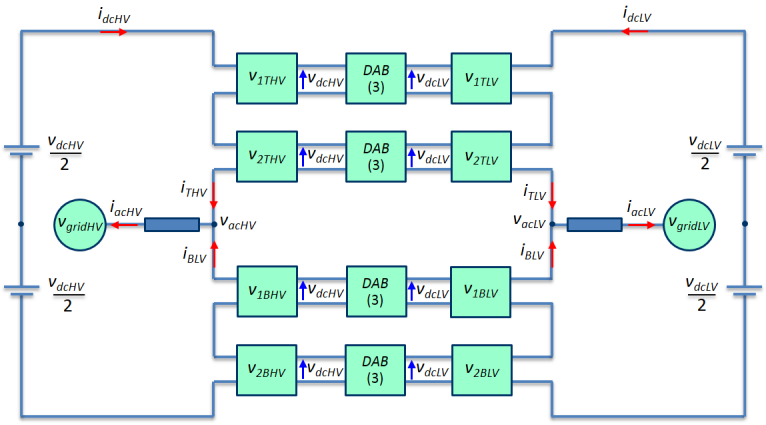

Figure 4.16: MMC-based multiport power converter. Cell-to-cell connected MMCs with symmetric primary and secondary (serialized input-serialized output).

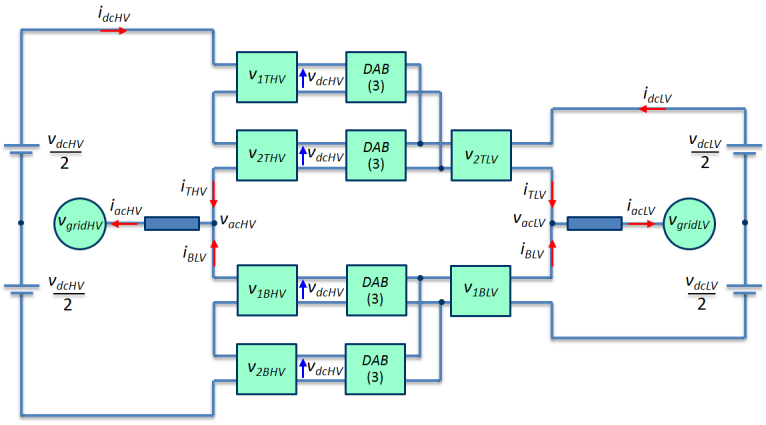

Figure 4.17: MMC-based multiport power converter. Cell-to-cell connected MMCs with serialized input-parallelized output.

- The configuration shown in Fig. 4.16 corresponds to two MMC connected through the cells capacitors and the DABs. It provides two AC ports and two DC ports (HV and LV), with the same number of voltage levels in both AC ports. Since the number of cells is the same in both sides, the transformation HV-to-LV between the primary and the secondary has to be realized by the DABs. Consequently, the DAB are not symmetrical. The left (HV) side of the power converter will

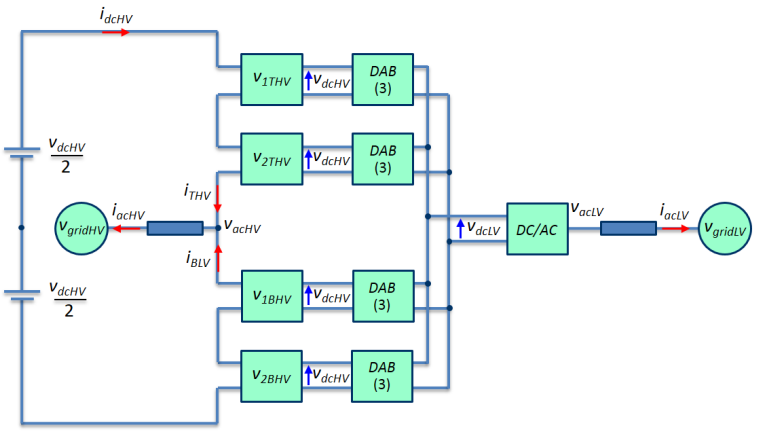

Figure 4.18: Multiport power converter with and MMC in the HV side and a conventional AC/DC power converter in the LV side.

require high voltage-low current power devices, while the cells in the right side (LV) would use low voltage-high current power devices.

- The configuration shown in Fig. 4.17 also corresponds to two MMC connected through the cell capacitors and the DABs. Therefore, it also provides two AC ports and two DC ports. However, in this case the DABs in each arm of the HV side are serialized, while there is some level of parallelization in the LV side. As a consequence, the number of cells (and thus the number of voltage levels) in the HV and LV sides are different. With this configuration, the transformation HV-to-LV between the primary and the secondary does not have to be realized only by the DABs, but can also be achieved by the effect of the serialization/ parallelization of the DBAs in the HV/LV sides respectively. This means that power devices with the closer voltage and current ratings can be used now for the HV and LV sides.

- Finally, in the configuration shown in Fig. 4.18, all the DABs in each leg are connected in parallel in the LV side. As a consequence, a conventional DC/AC power converter can be used now (e.g. two-level or multilevel NPC, FC, ...). In this configuration, the transformation HV-to-LV between the primary and the secondary can be entirely obtained by the effect of the serialization/parallelization of the DABs in the HV/LV sides. Thus, the DABs could now be symmetric, with a ratio 1:1 between the primary and the secondary. This would allow to use the same power devices in both sides, which is obviously advantageous. Due to practical feasibility, this will be the case considered through the following sections.

4.3.2 Control Strategies for the Multiport Power Converter

This section discusses potential control structures for the multiport power converter shown in Fig. 4.18. The converter provides three ports: HVDC, high voltage AC (HVAC) and low voltage AC (LVAC). The power balance equation can be expressed by (4.44). If losses are neglected, the power transferred by the DABs will be equal to the active power of the DC/AC power converter in the LV side (4.45).

$$P_{dcHV} = P_{acHV} + P_{acLV} \tag{4.44}$$

$$P_{DAB} = P_{acLV} \tag{4.45}$$

Two main control approaches can be considered for the control of the MMC-based multiport power converter. If voltage in the ports is established externally (i.e. by the grid), a *grid feeding* strategy can be used. The power transferred by the corresponding ports is therefore controlled in this case. On the other hand, if the voltage in a port must be established by the multiport converter, a *grid forming* strategy is needed. The target control in this case is to establish the desired voltage. As a consequence, the power transferred is not controlled. Still some type of inner current control loop is required to guarantee that the power limits of the converter are not exceeded. It is not possible therefore to operate all the ports in the *grid forming* mode, since the power balance cannot be guaranteed in this case. Consequently at least one port must be configured as *grid feeding*. Independently of the strategy being implemented, the control must always maintain the internal capacitor voltages at their target value.

4.3.2.1 *Grid feeding* configuration

A potential configuration could be based on the interconnection of two existing AC grids, i.e. HVAC and LVAC, and a HVDC link. The AC and DC voltages are therefore already present, the multiport power converter working as an ideal current source, transferring power among ports. Fig. 4.19 shows a potential implementation of the control. All the three ports (v_{acLV}, v_{acHV} and v_{dcHV}) are configured in the *grid feeding* mode. The LVAC (P^*_{DAB}=P^*_{acLV}) and HVAC (P^*_{acHV}) powers are assumed to be the references in this case, the central control regulating P_{dcHV} to match the power balance. The control is seen to consist of three major blocks:

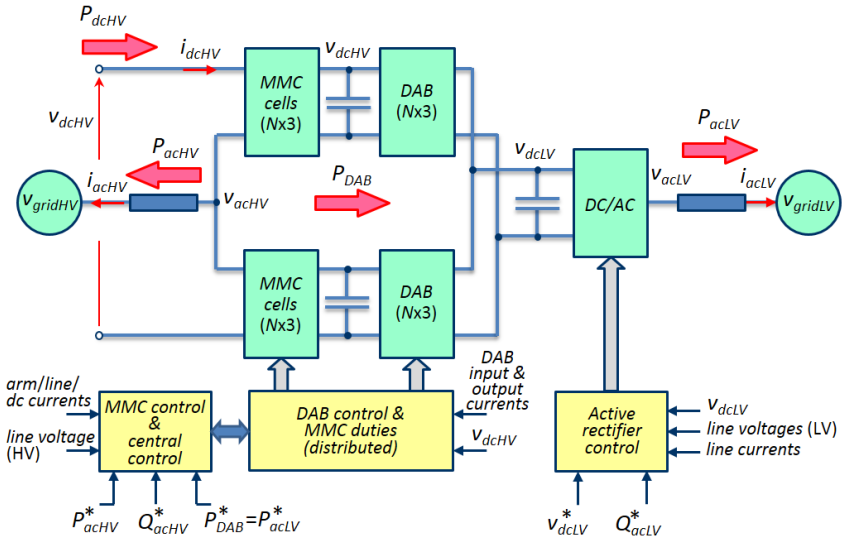

Figure 4.19: Schematic representation of *grid feeding* control structure of a MMC-based multiport power converter. Variables with superscript " * " indicate commanded values.

- *MMC control*: The MMC control implements the normal functionalities, i.e. control of the HVAC and HVDC ports, as well as of the cell capacitor voltages (v_{dcHV}), as discussed in Section 3.6.2 and Fig. 3.17.

- *DABs control*: It is advantageous to distribute the DAB control in each cell, as the DABs operate independently (even if they all receive the same power command) and at much higher switching rates compared to the MMC cells [99]. The DABs connect two ports of constant (controlled) voltages, v_{dcHV} and v_{dcLV}, operating therefore as a current source. Provided that the input and output voltages of the DABs are maintained at their target values, the power command for the DABs, P^*_{DAB}, directly translates into a current command.

- *Active rectifier (DC/AC converter in the LV side) control*: It operates as a conventional controlled rectifier, whose control is shown in Fig. 4.20. Commanded values for the active rectifier are the DC link voltage v^*_{dcLV} and the reactive power Q^*_{acLV}. The control will match P_{acLV} with P_{DAB} through the d-axis component of i_{acLV}, which is the required condition to maintain the DC link voltage v_{dcLV} at its target value.

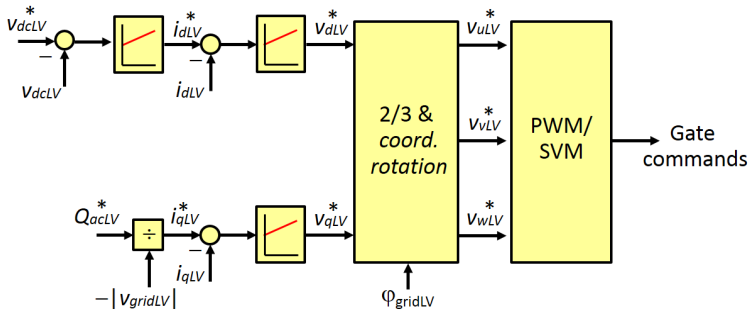

Figure 4.20: Control scheme of the active rectifier for the case of a *grid feeding* configuration of the MMC-based multiport power converter.

4.3.2.2 *Grid forming* configuration

In this possible configuration, the LVAC grid is not provided but must be formed by the multiport power converter, which works in this case as an ideal AC voltage source. Fig. 4.21 shows a potential implementation of the control structure.

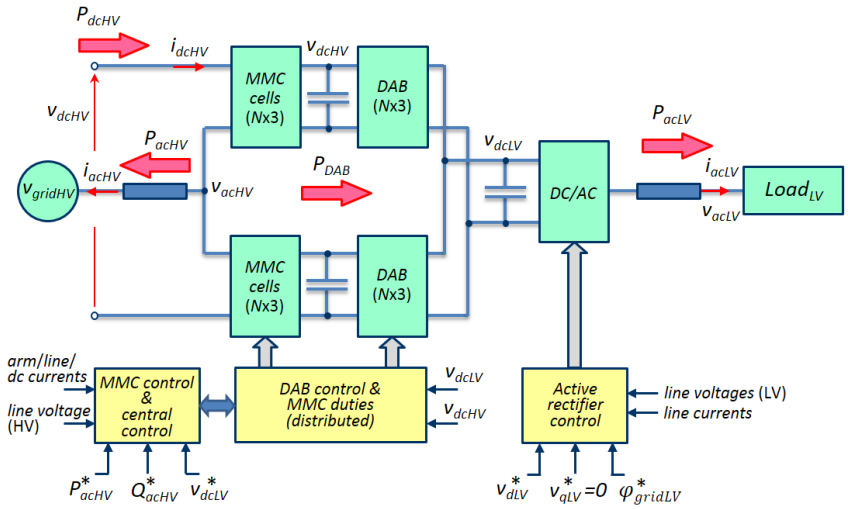

Figure 4.21: Schematic representation of *grid forming* control structure of a MMC-based multiport power converter. Variables with superscript " * " indicate commanded values.

While major control blocks as the same as in the case of the *grid feeding* configuration shown in Fig. 4.19, some relevant differences are observed.

- *MMC control*: The MMC is operated identically to the previous case,

controlling the HVAC and HVDC ports, as well as the cell capacitor voltages (v_{dcHV}).

- *DABs control*: It now regulates the LVDC bus (v^*_{dcLV}). The corresponding command is received from the central control unit.

- *DC/AC converter in the LV side*: It is now controlled to create the LVAC grid, the corresponding commands being the magnitude (v^*_{dLV}) and frequency/angle ($\varphi_{gridLV}{}^*$), which are received from the central control. Main control blocks for the active rectifier control are shown in Fig. 4.22. The control operates in a reference frame synchronous with the commanded grid voltage, the d-axis voltage (v_{dLV}) being equal to the magnitude of the grid voltage, the q-axis voltage (v_{qLV}) being zero.

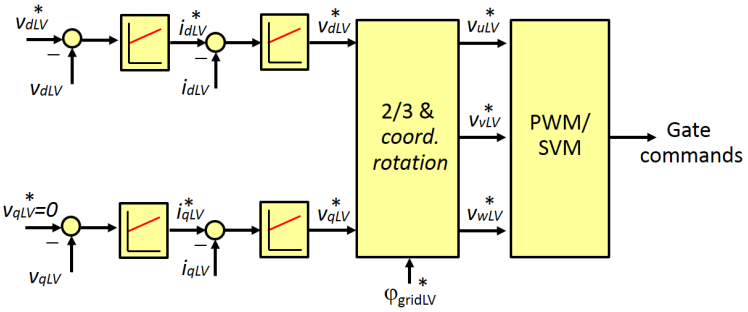

Figure 4.22: Control scheme of the active rectifier for the *grid forming* control structure of a MMC-based multiport power converter.

It is noted that other *grid forming* configurations can be implemented, e.g. grid forming in the HVAC port and grid feeding in both LVAC and HVDC ports.

4.3.3 Simulation Results

Fig. 4.23 shows simulation results obtained using Matlab/Simulink for the multiport power converter with *grid feeding* control structure. The MMC is enabled at t=10 ms, the active power command being set to 100 kW (Fig. 4.23-a). Initially the DABs are not transferring power. Therefore, the power in the HVDC port of the MMC (Fig. 4.23-b) matches the AC power plus the converter losses. At t=70 ms the active rectifier in the LV side is enabled. However, initially it will not transfer active power, since the DABs are not transferring power either (see Fig. 4.23-c-d). At t=0.3 s, the DABs are commanded to transfer 40 kW in total. This power is supplied by the

controlled rectifier in the LV side (Fig. 4.23-d). It is also observed from Fig. 4.23-b that the power supplied by the HVDC port of the MMC is decreased by the same amount, which is required to maintain the power balance. As discussed in section 4.3.2.1, only the AC active power in the HV side of the MMC and the power transferred by the DABs are commanded. The active power for the controlled rectifier and the power in the DC link of the MMC are adapted by the corresponding controls (Fig. 4.19) to maintain the power balance.

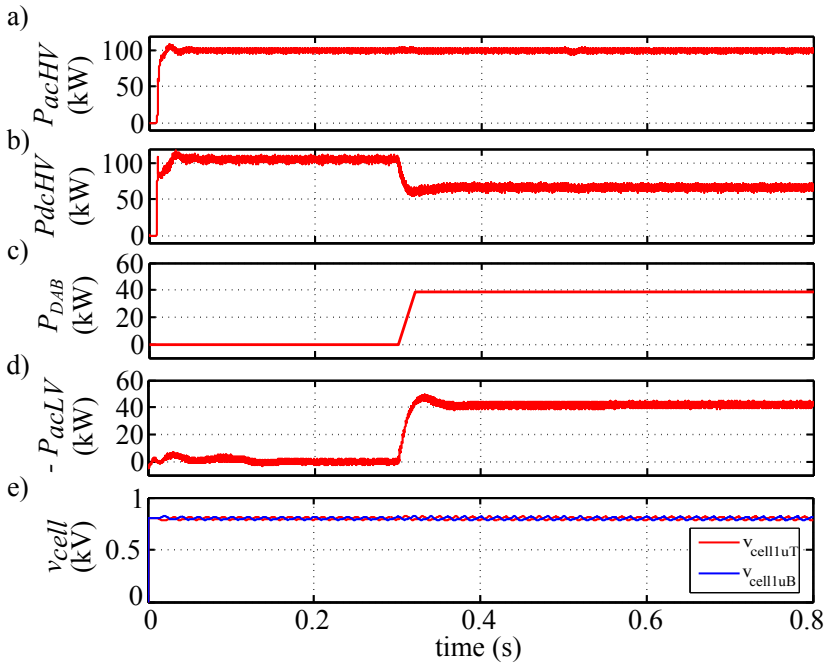

Figure 4.23: Simulation results. *Grid feeding* control structure in MMC-based multiport power converter. a) Active power in the HVAC port. b) Power in the DC port. c) Total power injected by the DABs. d) Active power in the LVAC port. e) Capacitor voltage of a cell in the top and bottom arms.

4.3.4 Control System Implementation

Potential implementations of the control of the MMC-based multiport power converter are discussed in this section. Two cases are considered:

- *Centralized control*, in which a central controller measures all the variables and controls all the power switches of the MMC and DABs.

- *Distributed control*, in which a central controller measures some variables and executes the main converter control algorithms, but each MMC cell/DAB has a dedicated local control. Both cases are discussed following.

4.3.4.1 Centralized Control

In a centralized control topology, one single processing unit is responsible for the control of both the MMC cells and the DABs. This is schematically shown in Fig. 4.24. In this configuration, the aforementioned processing unit will have to manage the acquisition of every voltage and current sensor signal by means of a high enough number of AD converters and generate the corresponding gate signals to be sent to the drivers. Therefore, this topology requires a very large number of input/output ports. Most of them will be connected via optical fiber transmitters and receivers, since it is necessary to maintain electrical isolation.

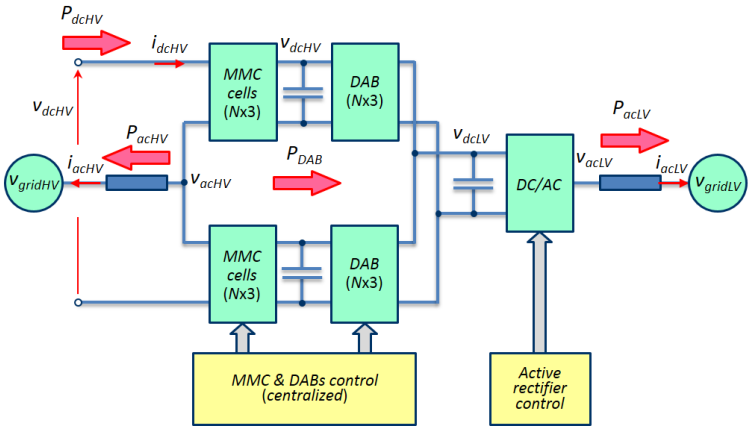

Figure 4.24: Implementation of the *centralized control*.

In addition to the hardware requirements, the computational requirements for the control unit are extremely high, as it has to implement both the control algorithms of the MMC and of all the DABs. It is also noted that these control algorithms operate with rather different sampling periods, which can be a few kHz for the MMC and in the range of several tens of kHz for the DABs typically, what adds further challenges to their implementation in a single digital device.

4.3.4.2 Distributed Control

In a distributed solution, control is split between a master (central) unit responsible of overall MMC control and several slave units, each in charge of one DAB and its corresponding MMC cell. This is schematically shown in Fig. 4.25. This arrangement allows a reduction of the number of input/output ports, also the computational burden of the central processing unit is significantly reduced. Moreover, since the slave devices are integrated in the DABs, the electrical isolation requirements for the sensors and drivers are lessened, reducing the count of optical fibers and shortening the length of those which are still necessary.

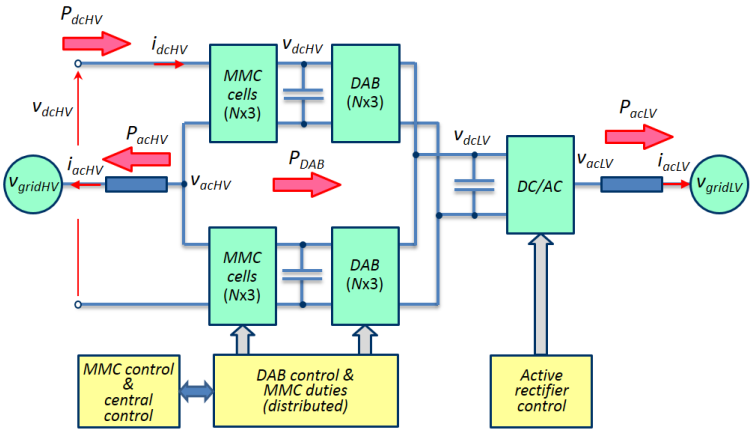

Figure 4.25: Implementation of the *distributed control*.

For the distributed control, it will be necessary to define a bidirectional communication between the central and slave devices. The central unit will send to the slave devices the commands for the DABs, as well as the corresponding duties for the MMC cells. The bandwidth for this communication is modest, as it does not need to transmit gate signals requiring precise timing. On the other hand, the slave units will send to the central unit through this link the measured cell capacitor voltages. These are needed by the central unit to implement the balancing algorithms.

Table 4.5 summarizes the input/output requirements for the central control unit in the case of a centralized and a distributed control for the particular case of an MMC with $N_{MMC} = 4$. It is noted that though these figures correspond to a particular implementation, i.e. with specific AD converters, drivers, ..., still some valuable conclusions can be reached. "OF" stands for optical fiber, while (*) stands for a functionality that will be implemented in the distributed control system. The table includes the number of A/D channels which are needed to measure currents and voltages at different

stages of the converter; number of lines for communications; number of lines to communicate with the drivers which control the power transistors. It is observed that for the case of an MMC with $N_{MMC} = 4$, i.e. four cells per arm in the MMC (which is a modest amount), a total number of 384 optical fiber connections are needed, in addition to 20 cable connections (i.e. which do not require isolation). It must be remarked in this regard that all the gate signals for both the DABs and the MMC cells come from the central control unit. On the other hand, the number of optical fiber connections is reduced to 6 for the case of the distributed control, where gate signals for each DAB and MMC cells are locally generated by the slave units.

Table 4.5: Centralized vs. Distributed Control: Input-Output requirements of the central control. *Grid feeding* strategy.

		Centralized Control	*Distributed Control*
Number of ADC channels	MMC variables	12	12
	DAB variables	3x3x2N_{MMC} = 18N_{MMC} (72 with $N_{MMC} = 4$)	- (*)
Number of signals for communications	To/from MMC ADCs (No OF needed)	20	20
	To/from DAB ADCs (OF)	(4+3)x3x2N_{MMC} = 42N_{MMC} (168 with N_{MMC}=4)	- (*)
	To/from slave FPGAs (OF)	-	3x2=6 (comm. OF rings)
Number of signals for the drivers	To/from MMC (OF)	3x3x2N_{MMC} = 18N_{MMC} (72 with N_{MMC}=4)	- (*)
	To/from DAB (OF)	6x3x2N_{MMC} = 36N_{MMC} (144 with N_{MMC}=4)	- (*)
I/O ports	Without OF	20	20
	With OF	(42+18+36) N_{MMC} = 96N_{MMC} (384 with N_{MMC}=4)	6
	Total	20+96N_{MMC} (404 with N_{MMC}=4)	20+6

4.3.4.3 Selection of Control Hardware and Communications

Based on the analysis carried out in the previous sections, a distributed control has been selected as the most suitable option. Fig. 4.26 shows the block diagram of the partially distributed control, particularized for the *grid feeding* strategy. The central control has medium processing requirements, the number of input/output signals being modest. These computational requirements could be met by a high performance DSP. For the implementation shown in Fig. 4.26, a Xilinx's Zynq-7000 SoC has been used. It com-

prises a dual core ARM processing system highly integrated with a FPGA. A Z-7020 device in a 200 I/O FPGA pins package has been chosen. It is noted that the I/O resources of the Zynq-7000 are significant higher than the actual needs for the implementation shown in Fig. 4.26.

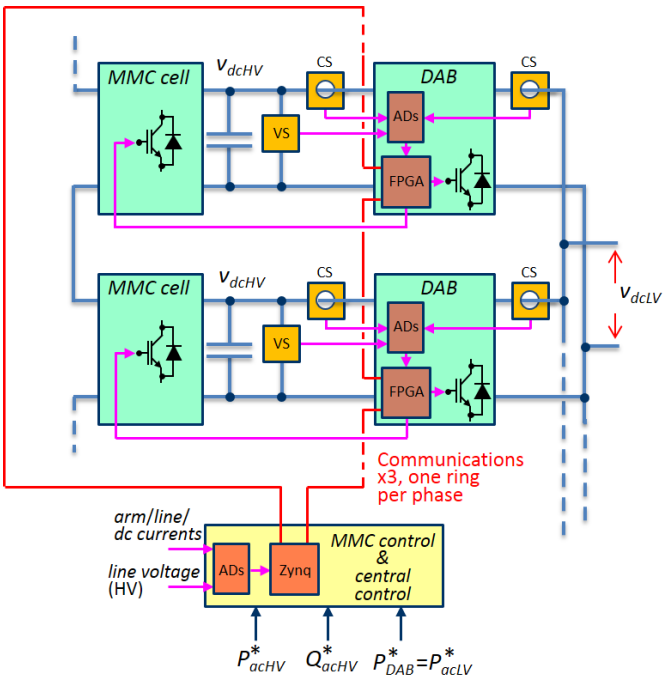

Figure 4.26: Detailed overview of the distributed control under *Grid feeding* strategy. VS and CS stand for voltage sensor and current sensor respectively.

A low cost FPGA Spartan 3E 250K by Xilinx has been selected for the control of the DABs and generation of MMC cell gate signals. The terminal current and voltages (i.e 12 signals in total) needed by the external control loops of the MMC are measured by two eight channel parallel bus 12 bit AD converters (MAX1308) managed by the Zynq-7000. This requires a total of 20 non-optical fiber lines between the converters and the central control, 12 of them being the data bus and the remaining 8 being control signals, with the electrical isolation being provided by the sensors themselves (see Table 4.5). Signals needed by the DAB control (i.e 3 signals per cell) are acquired by two ADCs in the HV side and one ADC in the LV side. The selected ADC is AD7476A from Analog Device. It uses 3 lines (data,chip select and clock). The two ADCs in the HV side shares clock and chip select (i.e 4 lines), resulting in a total of (4+3) signals coming from/to the ADCs in each DAB cell (see Table 4.5). MMC driver circuitry needs three signals (gate,fault and enable) per cell, while the DAB driver circuitry needs 6 signals per cell (i.e two gate signals and fault for each full bridge of the DAB converter)(see Table 4.5). Finally, the resulting amount of inputs/outputs

with and without optical fiber are included in the last row of Table 4.5.

The use of a *distributed control* system requires a communication network able to provide the bandwidth demanded by the control. As discussed in previous sections, communication between the central control unit and the slave FPGAs will be bidirectional: the central control unit will transmit duty cycle values to the distributed control units, while the distributed control units will communicate the measured cell capacitor voltages to the central control unit, which are needed for the control of the MMC. Regarding more specific data, the switching frequency of the MMC has been established in 5 kHz. Consequently, the information acquired by all the slave control units has to be transmitted in less than $200\mu s$.

The use of optical fiber is mandatory due to isolation requirements. Point-to-point communication is disregarded, due to the complexity and cost of the hardware. A ring configurations is therefore targeted. Each node in the ring will include one low-cost emitter and one receiver (see Fig. 4.26). The length of the optical fiber is also reduced, as the distance among DABs is significantly smaller than the distance between the DABs and the central control unit.

From the previous considerations, a serial communication protocol using optical fiber based on a modified version of TosNet protocol [103] was selected, as it can be fully implemented in the FPGAs with no need of additional hardware. In addition, TosNet is a master-slave sochronous protocol, which allows to coordinate the operation of all of the nodes by means of an internal deterministic synchronization signal (synchronization signal in Fig. 4.27).

The implemented protocol supports up to sixteen nodes. Therefore, three separate optical fiber rings will be used, one for each phase (see Fig. 4.26). Each ring consists of eight slave nodes, which correspond to the FPGAs in each DAB (four cells per arm, i.e eight cells per leg) and one master node, which is implemented in the central control unit. The central control unit is responsible of generating the synchronization signal, and consequently of the synchronization of the overall control.

TosNet makes use of a shared memory block, which is transmitted to all of the nodes in the ring in every network cycle. In the proposed configuration, each of the slave nodes has been assigned two sixteen-bit register of the memory block. The first register contains the MMC cell duty cycle; it is written by the central control and read by the slave FPGA. The second register contains the MMC cell capacitor voltage; it is written by the slave FPGA and read by the central control.

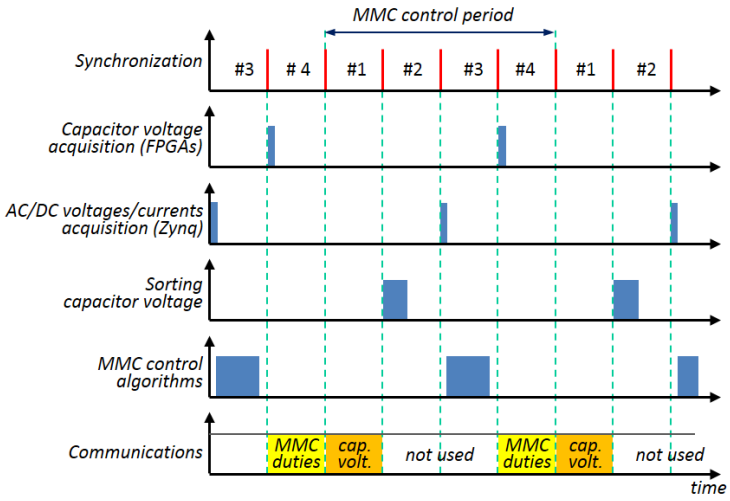

Figure 4.27: Timing diagram showing the different tasks needed for the MMC-based multiport converter *distributed control* system, including communications.

Fig. 4.27 shows the timing diagram, including the different tasks implemented by the multiport converter distributed control. The sampling period of the MMC is synchronized with the communication period, each MMC sampling period consisting of four communications periods (#1 to #4 in Fig. 4.27). In each communication period, the memory block containing the MMC cells duties and the cell capacitor voltages is transferred to all the elements in the ring (central control and slave FPGAs). However, the content of the memory block is only updated/read at well defined instants of time of the control process. The overall process works as follows:

- Communication period #4 (see Fig. 4.27): Cell capacitor voltages are acquired by the slave FPGAs. MMC duties to be applied to each MMC cell for the next control period are received by the slave FPGAs through the communications ring. Cell capacitor voltages transferred through the communications ring are not used.
- Communication period #1: Cell capacitors voltages are transferred by the slave FPGAs to the central control through the communications ring. Duties transferred through the communications ring in this period are not used.
- Communication period #2: Capacitor voltages are sorted by the MMC central control. Information transmitted through the communications ring is not used.
- Communication period #3: MMC AC and DC terminal voltages and currents are acquired. This occurs at the center of the MMC control

period, therefore reducing the switching harmonics in the sampled AC currents. After this, the central control executes the control algorithms of the MMC. As a result, the duties for the MMC are available to be transferred during the next communication period (#4). Information transmitted through the communications ring is not used.

4.4 CHB vs. MMC-based Multiport Power Electronic Transformer

Solid State Transformer (SST) (also called Power Electronic Transformer, PET) most representative topologies have been discussed in Section 2.3.1. It has been shown that a common criteria for their classification is the number of conversion stages. According to this criteria, the three-stage configuration appears to be the most popular choice (see Section 2.3.1.1). This arrangement is schematically shown in Fig. 4.28. It realizes a double DC/AC transformation in the HV side and in the LV side respectively. Isolation between the LV and HV sides is provided by a DC/DC stage using a HF transformer.

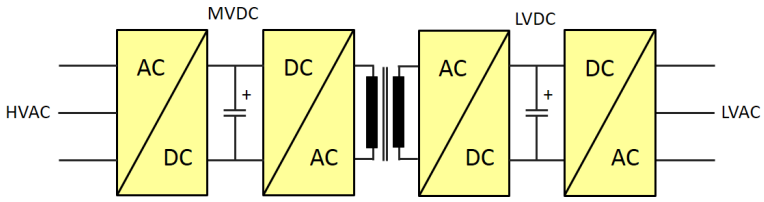

Figure 4.28: Three-stage SST/PET topology.

Practically all PET topologies provide at least a high-voltage AC (HV-AC) and a low-voltage AC (LV-AC) port, therefore connecting two AC systems. However, inclusion of additional ports, e.g. low-voltage and/or high-voltage DC (LV-DC/HV-DC) is often possible. The resulting multiport topologies enable additional functionalities in addition to the HV-AC to LV-AC transformation, e.g. interconnection to HVDC or the integration of energy storage devices or distributed energy resources (DER). However, this enhancement can imply an increase of the power converter complexity and cost, which needs to be considered.

Cascade H-Bridge (CHB) converter (see Section 2.2.2.3) can likely be considered as the most popular topology for the HV DC/AC stage of PETs (stage at the left side in Fig. 4.28) and will be used as a benchmark. The CHB-based PET is shown in Fig. 4.29-a. The topology discussed in this work in Section 4.3.1 based on a MMC topology, share several similarities

with the CHB-based topology, but also there are remarkable differences. This section addresses the comparative analysis of CHB and MMC based PETs [100],[102], according to the following criteria:

- Number and type of the ports provided by the PET
- Number and type of cells
- Number and rating of the power devices
- High frequency transformers count and requirements

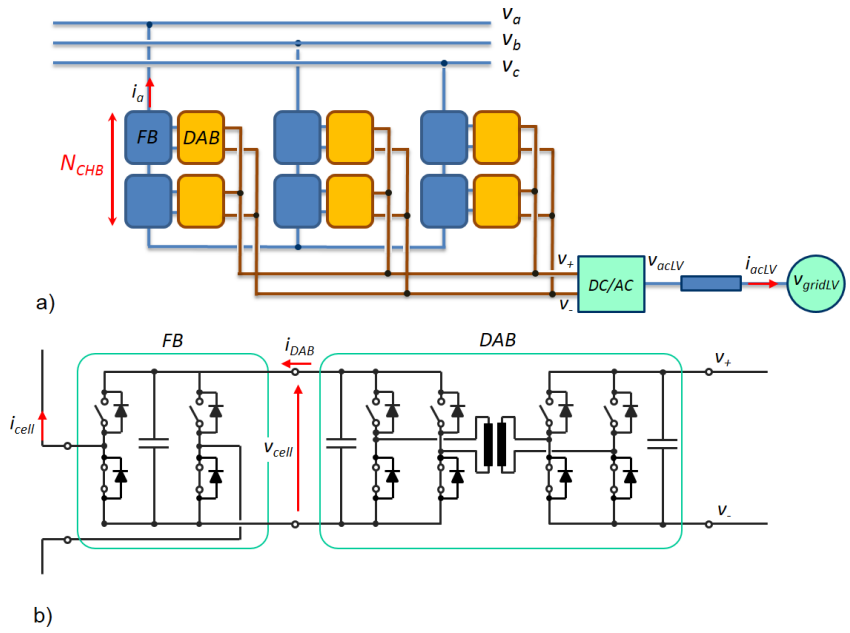

Figure 4.29: a) 3-phase CHB-based PET. b) Submodule including the full-bridge (FB) and the Dual Active Bridge (DAB) converter.

4.4.1 CHB-based Power Electronic Transformer

It consists of a series connection of a certain number of full-bridge submodules with a capacitor. Serialization of cells allow to withstand high voltages using relatively low voltage devices. While the CHB cells alone are not able to handle active power (see Section 2.2.2.3), this feature is achieved by providing the submodules the capability to transfer (absorb/deliver) power. Dual Active Bridges (DAB, Fig. 4.29-b) converters can be used for this purpose. This corresponds to the intermediate stage in Fig. 4.28. DABs outputs

are parallelized to obtain a low voltage-high current DC link, from which the LV-AC port is obtained using a DC-AC converter [32],[102]. Practical implementation of this concept can be found in [32],[33],[104].

The CHB-based PET in Fig. 4.29 connects an HV-AC port and a LV-AC port. It is also observed from this figure that it can offer a LV-DC port. However this topology does not provide a HV-DC port.

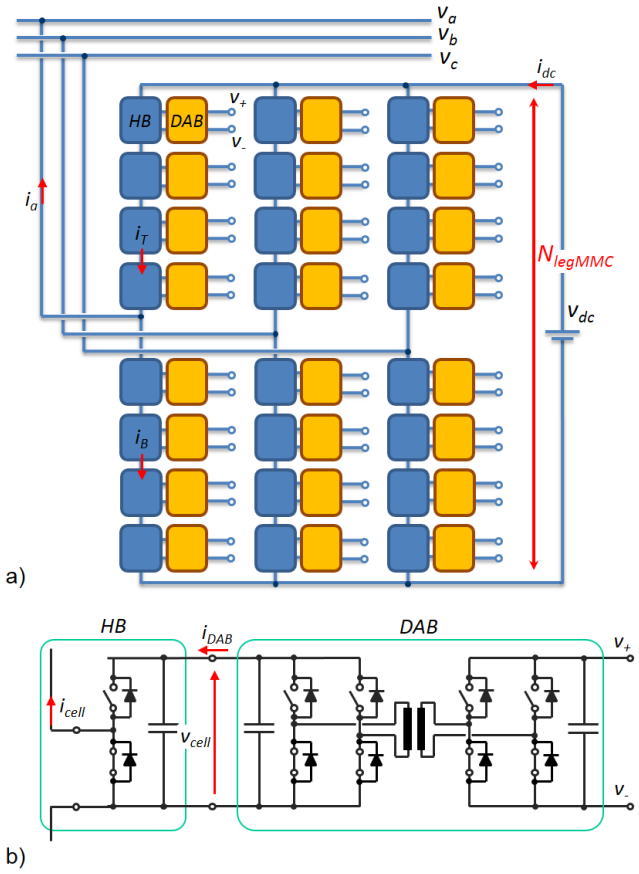

Figure 4.30: a) 3-phase MMC-based PET. LV-side outputs of the DAB (V_+, V_-) are connected as in Fig. 4.29 (not shown for the shake of clarity). b) Submodule including the half-bridge (HB) and the DAB converter.

4.4.2 MMC-based Power Electronic Transformer

To overcome the lack of a HVDC of the CHB-based PET, Modular Multilevel Converter (MMC) based PET can be used. This design uses a MMC in the HV side, which intrinsically provides an HV-DC and a HV-AC port (see Section 3.2.1). Figs.4.8-e and 4.18 show an arrangement of a MMC-based

multiport PET. Complex notation is used to model the LV-AC side. Fig. 4.30 shows in more detail the configuration of the power converter. Similarly to the CHB case, DABs are used to perform the intermediate stage in Fig. 4.28. DAB outputs in the LV side are parallelized to provide a LV-DC, high current port. MMC cells use the a half-bridge (HB) topology, as they do not need to invert the voltage.

Alternatively to the topology shown in Fig. 4.30, it is possible to connect the DABs directly to the HVDC port, as shown in Fig. 4.31 [105]. The design in Fig. 4.31 allows to have a different number of DAB and MMC cells. A potential advantage of this option is a reduction in the number of DABs and consequently of HF transformers. However, this is at the price of an increase of the DAB power devices ratings (voltage and current), also affecting to the design of the HF transformer. The limit case would eventually consist of a single DAB. Examples of MMC-based PET using a single HF transformer can be found in [106],[107].

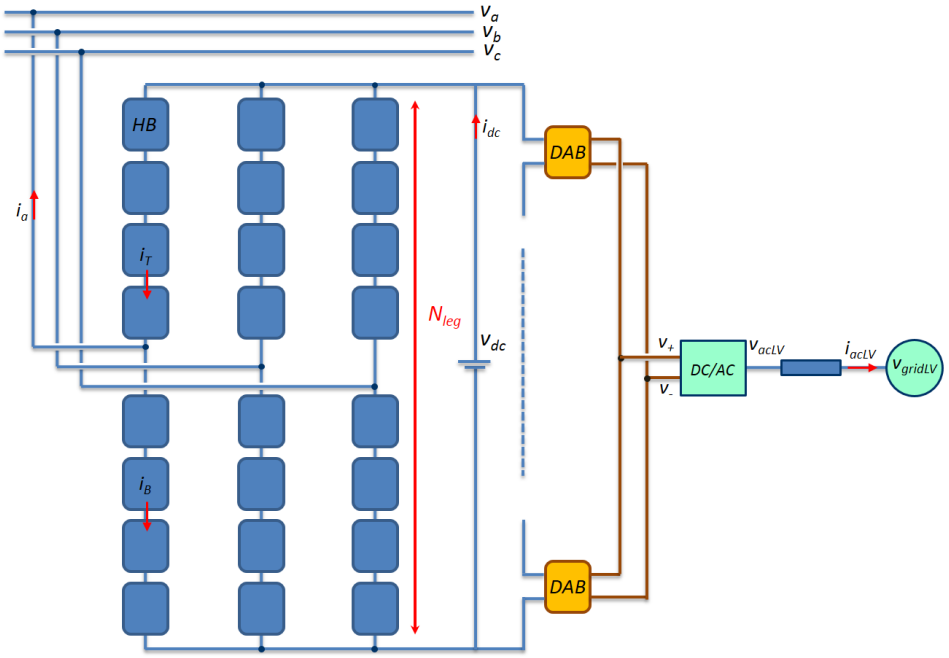

Figure 4.31: 3-phase MMC-based PET with the DABs connected to the HV-DC link.

4.4.3 Cell & Devices Count and Ratings

As already mentioned, the biggest difference between CHB and MMC-based PET topologies is the presence of an HV-DC port in the second. While

such port can be advantageous or even compulsory in certain applications, it has a significant impact in the PET design, which needs to be considered.

For the comparative analysis between CHB and MMC-based PET topologies following, it will be assumed that the voltage in the HV-AC and LV-AC ports is the same in all the cases. Numerical values are provided for the sake of clarity. The PET will connect two AC grids of $24kV$ and $400V$ respectively. The LV-DC is set to $1kV$. The HV-DC for the MMC-based PET topologies needs to be larger than the peak-to-peak phase value of the HV-AC, which is $39.2kV$. A HV-DC of $40kV$ was selected, the HV-AC to HV-DC ratio being $R_{no\,thi} = 0.98$ (3.18). While this ratio might be very tight in a practical implementation, the discussion following is valid for smaller values of R without any loss of generality. The voltage ratings are summarized in Table 4.6.

Table 4.6: AC and DC ports voltage

HV–AC	24 kV ($line$, rms)
LV–AC	400 V ($line$, rms)
HV–DC	40kV
LVDC	1kV

DC voltage for the HV side of the DAB was set to $2kV$ (i.e. $v_{cell} = 2kV$), the average current being $5A$. Consequently, each DAB will be able to transfer $10kW$. It is noted that the DAB design is identical for the topologies shown in Fig. 4.29a and Fig. 4.30a. On the contrary, the topology in Fig. 4.31 can require changes in the DAB ratings.

Regarding the number of devices required for the topologies under discussion, CHB cells use a full-bridge (FB) arrangement, each cell providing a voltage of $\pm v_{cell}$, with $v_{cell} = 2kV$. The number of cells required to produce the peak-to-peak phase HV-AC value is given by (4.46).

$$N_{CHB} = \frac{v_{ph-peak}}{v_{cell}} \tag{4.46}$$

For the required HV-AC voltage in Table 4.6, the number of FB cells per leg is 10, i.e. 30 in total, which is equal to the number of DABs. The total power that can be transferred between HV-AC and LV-DC ports is $P_{CHB-total} = P_{DAB-total} = 300kW$. The number of devices (transistors and diodes) for the CHB converter is 120.

For the MMC-based PET, the cells must be able to produce both the HV-DC and HV-AC voltages. Cells in this case are half-bridge (HB). The

number of cells per leg is given by (4.47) (see Fig. 4.30).

$$N_{legMMC} = \frac{v_{dc}}{v_{cell}} \cdot 2 \tag{4.47}$$

To achieve the HV-DC voltage in Table 4.6, the number of cells per leg is 40, i.e. 120 in total, which is equal to the number of DABs. The total power that can be transferred between the HV-AC and LV-DC ports is $P_{MMC-total} = P_{DAB-total} = 1200kW$. The number of devices (transistors and diodes) for the MMC converter is 240. It is noted that during this analysis, the DAB submodule remains unchanged.

It is interesting to note that to achieve the same HV-AC voltage, the MMC-based PET requires four times the number of cells of the CHB-based PET. This is the reason why the power of MMC-based design is four times the power of the CHB-based design, since each cell of the MMC-based design has an associated DAB, whose power remains invariant.

On the other hand, for the MMC-based PET implementation shown in Fig. 4.31, the MMC cell requirements are identical to the previous case. However, assumed that the DABs DC voltage remains constant, the number of DABs is reduced by 6 (i.e. $N_{DABs} = 40kV/2kV = 20$), but each DAB driving now six times the current (i.e. $P_{DABj} = 60kW$). The total power that can be transferred remains constant, i.e. $P_{DAB-total} = 1200kW$. Equalization of the DAB input voltage may be required in this case.

Table 4.7 summarizes the results of the previous discussion. It is noted that the number of devices $N_{devices}$ account for the devices (transistors & diodes) in the CHB and MMC cells, not including therefore power devices in the DABs.

Table 4.7: Sizing analysis for three different PET topologies

	CHB-based PET (Fig. 4.29)	MMC-based PET (Fig. 4.30)	MMC-based PET (Fig. 4.31)
v_{cell}	2kV	2kV	2kV
N_{leg}	10	40	40
N_{DABs}	30	120	20
P_{DABj}	10kW	10kW	60kW
P_{total}	300kW	1200kW	1200kW
$N_{devices}$	120	240	240
$I_{cell-peak}/I_{DAB}$	$\sqrt{3}$	$2/\sqrt{3} + 4\sqrt{3}$	$2/\sqrt{3} + 4\sqrt{3}$

Another important feature in the comparison regards the current rating of the devices. One major difference of MMC-based PETs compared to

CHB-based solution is their multiport feature. Such multiport feature modifies the power balance equation of the MMC-base PETs, and consequently the current that power devices must carry, which needs to be considered both for the cell design and for the control strategies of the converter.

In the CHB-based PET, all the power transferred by each DAB must be transferred by the corresponding CHB cell, the relationship between the DAB mean current and the CHB cell peak current being (4.48).

$$\frac{I_{cell-peak}}{I_{DAB}} = \sqrt{3} \tag{4.48}$$

On the other hand, the MMC-based PET offer different power flow routes, depending how the power transferred by the DABs ($P_{DAB-total}$) is split between the HV-DC port (P_{dcHV}) and HV-AC port (P_{acHV}) (4.49).

$$P_{dcHV} + P_{DAB-total} = P_{acHV} \tag{4.49}$$

The current that must circulate through the MMC cells power devices will depend on how the three terms in (4.49) are combined. For the discussion following, it is assumed without lost of generality that the DABs are transferring their rated power from the LV to the HV side. Three different cases can be considered:

- $P_{dcHV}/P_{DAB-total} > 0$: The HVDC port also injects a positive power P_{dcHV}. The HVAC-port must evacuate in this case the power coming both from the HV-DC port and from the DABs
- $-1 < P_{dcHV}/P_{DAB-total} < 0$: Only the DABs inject power, both HV-AC and HV-DC ports evacuate the power injected by the DABs
- $P_{dcHV}/P_{DAB-total} < -1$: The AC port injects power, the HV-DC port must evacuate the power coming both from the HV-AC port and the DABs

Fig. 4.32 shows the relationship between the MMC DC current i_{dc}, AC peak current i_a, and arm peak currents $i_{cell-peak(MMC)}$, for the three operating regions. The peak current for CHB-based PET cells $i_{cell-peak(CHB)}$ is also shown for reference. It is noted that, depending on how the power of the three ports are combined, the MMC cells devices must be designed to conduct currents which can be significantly larger than for the CHB case. Last line in Table 4.7 summarizes the results.

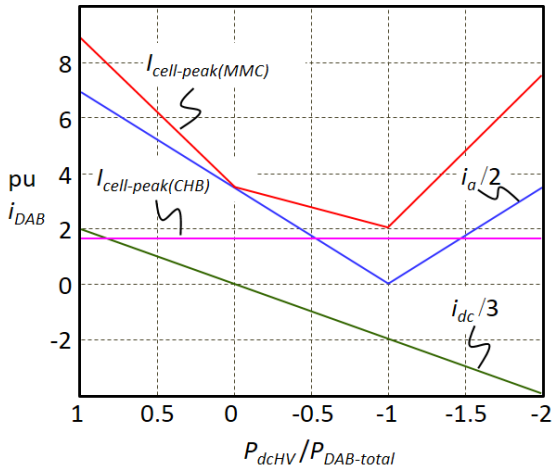

Figure 4.32: MMC-based and CHB-based PETs devices peak current as a function of $P_{dcHV}/P_{DAB-total}$, with $P_{DAB-total}$ equal to its rated value. Currents are shown in pu of the DAB average current.

4.4.4 High Frequency Transformer Design

High Frequency Transformer Design discussed in this section is mainly extracted from [108] and is included for the shake of completeness of this document. It is noted however that it is not an original contribution of this thesis.

The DAB HF transformer is key element of the PET, as it must be able to transfer the required power between the HV and LV sides with the highest possible efficiency, while providing galvanic isolation between the HV and LV ports. Key parameters for the transformer design are its power, input and and output voltages, switching frequency and the required isolation. Most of these parameters are directly linked to the characteristics of the switching devices.

For the PET design being considered, required isolation between HV and LV sides is $24kV$ (see Table 4.6). The base power will be $10kW$, which corresponds to the CHB and MMC-based PETS in the first two columns in Table 4.7. The design is optimized to minimize the overall losses and core size, while keeping the temperature below $60°C$. Mathcad and Matlab were used for the numerical analysis, Pmag and Maxwell being used for Finite Element Analysis.

For the HF transformer design, different core materials and coils arrangements were considered. Coil arrangements studied include concentric windings and two types of separate windings configurations. Concentric wind-

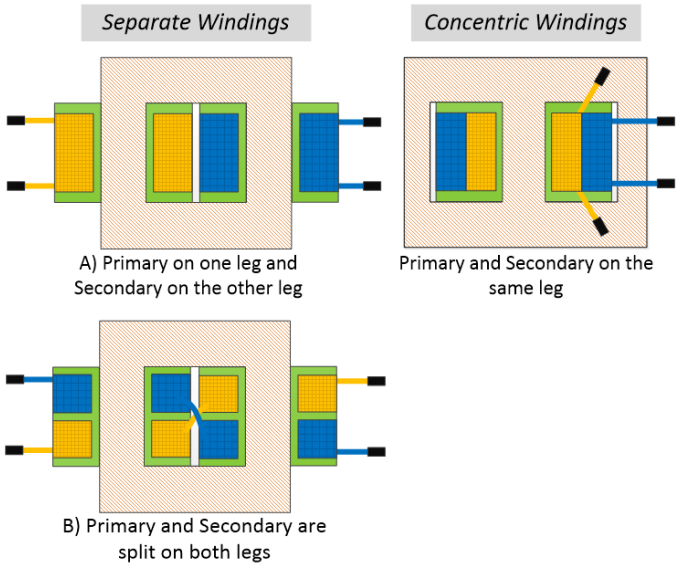

Figure 4.33: HF transformer coil arrangements. Left- Separate windings, Right- Concentric windings

ings achieve the lowest leakage inductance but high isolation levels might not be reached due to the fact that a certain isolation distance must be kept between the windings (see Fig. 4.33-left-a). On the contrary, the use of separate windings (see Fig. 4.33-right) provides a much easier way o achieving the required isolation, but at the price of a significant increase in the leakage inductance. An intermediate option is to use separate windings but split between both legs (see Fig. 4.33-left-b). This arrangement may result in an important decrease of the of the leakage inductance compared to the conventional separate windings option. However, achieving high isolation levels is highly penalized. As a consequence, separate windings configuration have been finally selected since it provides the best trade-off between isolation and leakage inductance requirements. An schematic representation of the HF transformer designed for the base case is shown in Fig. 4.34, *Case 2* in Table 4.8 showing its main characteristics.

Depending on the characteristics of the power devices, three design parameters must be considered for the design of the HF transformer:

- Rated power
- Input voltage (i.e. cell voltage)
- Switching frequency

Table 4.8 shows alternative transformer designs for different values of

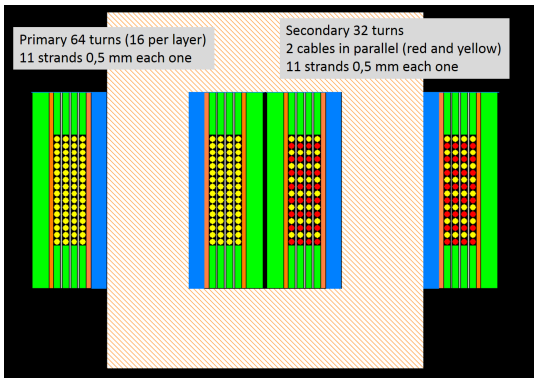

Figure 4.34: Schematic representation of HF transformer for the base case [108].

the input voltage and rated power of the MMC-based PETs, while keeping the same isolation requirements.

It is seen that increasing the power for the same input voltage and isolation, slightly increases the efficiency, the power density being increased significantly. However, this penalizes temperature. Comparison between cases 2 and 4 has been actually performed between one $60kW$ (see Fig. 4.31) transformer and six units of $10kW$ transformers. The important improvement in power density is mainly due to the fact that the required isolation imposes a certain distance between windings that must be maintained. Consequently, use of winding area and magnetic core improves as power increases.

Cases 1 and 3 in Table 4.8 show the effects of increasing the cell voltage to 1 kV and 4 kV. A cell voltage of 1 kV could be a achieved using available 1.7 kV SiC MOSFET. On the other hand, a cell voltage of 4 kV could be achieved using new 6.5 kV SiC power devices. It is observed that increasing the cell voltage is advantageous in terms of HF transformer efficiency and power density. However, temperature is slightly penalized. It is noted that, given specific isolation requirements and a rated power that fixes a particular magnetic core, it is advantageous to increase the input voltage (i.e. cell voltage). This will imply a smaller input current and thus, the required leakage inductance increases. In order to comply with those requirements, an increase in the number of turns is needed, which imply a decrease in the core losses (i.e. higher efficiency). It is noted that rated power of the designs has been adapted to keep the total power constant (e.g. if input voltage is reduced by half, double number of cells will be required and thus, each cell must transfer half the power to keep the same total power transfer).

Regarding the switching frequency of the power devices being used in the DAB, an increase leads to lower leakage inductance requirements. Hence,

Table 4.8: High-frequency transformer theoretical design parameters [108]

	Case 1	**Case 2**	**Case 3**	**Case 4**
Power	$5kW$	$10kW$	$20kW$	$60kW$
Input voltage	$1kV$	$2kV$	$4kV$	$2kV$
Efficiency	99.74%	99.83%	99.88%	99.92%
Temperature rise	$60°C$	$61°C$	$68.4°C$	$73°C$
Leakage inductance	$455\mu H$	$910\mu H$	$1800\mu H$	$152\mu H$
Power density	$49.8W/cm^3$	$60W/cm^3$	$79W/cm^3$	$176W/cm^3$

number of turns will need to be reduced and core losses will be increased. However, increasing the switching frequency is not always advantageous, since core losses will increase too, eventually reducing the efficiency. A trade-off between switching frequency, rated power (which is directly related to required leakage inductance) and core losses is then required.

4.5 Summary

This chapter has addressed the use of the Modular Multilevel Converter as the basis of a multiport power converter topology. Modification of the conventional MMC cells in order to provide power transfer capability and enable multiport capabilities has been discussed in detail first. Based on these modification, two main cases have been analyzed: Asymmetric and symmetric MMC-based multiport power converters.

Asymmetric arrangements have been deeply studied, starting from the different possible configurations that include cells with power transfer capability. After that, power balance constraints, limits of operation and voltage limits have been analyzed. Limits for power transfer capabilities based on the required voltage imbalances have been analyzed. Finally, control strategies able to cope with this asymmetric arrangements have been discussed. Numerical and simulation results have been include to validate the proposed concepts.

Symmetric configurations have been analyzed. These arrangements are the basis for the multiport topologies based on the MMC (i.e. Solid State Transformers). Modes of operation and control strategies have been studied, including simulation results. Practical implementation of the control using centralized and distributed strategies has been also included.

To conclude, CHB and MMC-based multiport power electronic transformers have been compared, starting from an individual analysis of both

approaches and ending with a comparison in terms of capabilities, device count and ratings. Finally, requirements and design of the high frequency transformer connecting HV and LV ports has been discussed.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

This thesis has developed a deep state-of-the-art analysis concerning multilevel converters. A new energy network scenario has been firstly described to remark the importance of electronic power converters and in particular, multilevel power converters. Both well established and more recent topologies have been discussed, ending with the introduction of the Solid State Transformer concept. Solid State Transformer's background has also been covered, including a proposal for their classification.

Modular Multilevel Converter has been analyzed in detail following. This kind of converter can be seen as the response to the need of an AC-DC bidirectional multilevel converter with a fully modular arrangement. Principles of operation, modeling and power balance equations have been analyzed in detail. Special attention has been paid to its most distinguishing feature: the circulating current. Passive elements sizing, such as arm inductors and cell capacitors, have been also discussed.

Operational aspects have been also covered, including modulation strategies, capacitor voltage balancing methods and control of the MMC. These three features are not fully independent but the choice of a certain balancing method may pose restrictions on the modulation strategy that can be applied. A thorough analysis has been included in this regard. In addition, control of the MMC has been presented, starting from the general control objectives and finally focusing on the different approaches for circulating current control. Most relevant control schemes have been also discussed,

including the connection with capacitor voltage balancing methods. Operation of the Modular Multilevel Converter under voltage constraints has also been analyzed, including not only the use of overmodulation strategies to increase the AC fundamental component of the voltage, but the operation in case of faulty cells.

Modular Multilevel Converter has been the basis of a multiport power converter topology. Modification of the conventional MMC cells in order to provide power transfer capability and enable multiport capabilities has been discussed in detail. The resulting multiport power converters have been classified attending to the number and location of cells transferring power into asymmetric and symmetric topologies.

Asymmetric arrangements have been studied in detail, starting from the different possible configurations that include cells with power transfer capability. After that, power balance constraints, limits of operation and voltage limits have been analyzed. Limits for power transfer capabilities based on the required voltage imbalances have been analyzed, providing a mathematical analysis. Finally, control strategies able to cope with this asymmetric arrangements have been discussed.

Symmetric configurations have been also analyzed. These arrangements constitute the basis for the multiport topologies based on the MMC (i.e. Solid State Transformer). Modes of operation and conventional control strategies focused on multiport power converters have been deeply covered. Additionally, a practical implementation of the control system for an MMC-based multiport power converter has been also discussed. To complete the whole study, CHB and MMC-based multiport power electronic transformers have been compared, starting from an individual analysis of both approaches and ending with a comparison in terms of capabilities, device count and ratings.

5.2 Contributions

Main contributions of this work are listed below:

- By the time this thesis was being developed, information about Modular Multilevel Converters along the literature has been found to be very unclear, dispersed and sometimes even chaotic. One of the main contributions of this work has been focused on gathering all the available information and obtaining a clear background and overview about Modular Multilevel Converters. Classification and analysis of modu-

lation strategies, capacitor voltage balancing methods, passives (i.e. arm inductance and cell capacitor values), control strategies and the influence and connection among all of them has been an important milestone of this work. In addition, a classification of the control methods based on the circulating current control strategies has been proposed.

- Operation of Modular Multilevel Converters under voltage constraints has been studied, including not only the use of overmodulation strategies to increase the AC fundamental component of the voltage, but the operation in case of a faulty cell.

- Novel topologies have been derived from the MMC by modification of conventional half-bridge cells to provide power transfer capability.

- MMC topology has been adapted into a multiport structure. MMC-based multiport power converters have been classified attending to the number and location of cells transferring power into asymmetric and symmetric topologies.

- In case of asymmetric MMC-based multiport power converter topologies, different configurations have been analyzed and its viability has been widely discussed considering power balance constraints. Limits of operation of cells with power transfer capability have been deeply studied providing a mathematical analysis.

- Specific control strategies for asymmetric MMC-based multiport power converter topologies have been proposed and analyzed.

- MMC-based Solid State Transformer has been pointed as a particular case of symmetric topology. Conventional control strategies have been adapted to cope with these arrangements.

- Practical implementation of the control system for an MMC-based multiport power converter has been discussed.

- A comparative analysis between CHB and MMC-based multiport power electronic transformers has been carried out, including functionalities as well as cells and devices requirements and ratings.

- Construction of experimental prototypes to validate the concepts developed along this work

5.3 Future Work

Based on the work developed along this thesis, there are several topics which are considered highly relevant and worth to be further explored:

- Optimization of SST performance. SSTs are significantly more complex and expensive than conventional transformers. In addition, it is arguable that they are more efficient (can be truth for low load levels, but not for high load or full load operation) or smaller (higher power density), as the reduction in volume and weight thanks to the use of HF transformers is compensated by the need of electronic power devices, passives, auxiliary elements and so on. The one aspect in which SSTs are undoubtedly superior to conventional transformers is controllability. SSTs can implement sophisticated algorithms to satisfy multiple control targets, including grid forming with precise voltage control, power flow control, harmonic and imbalance compensation, ride through and so on. Control methods reported so far can be considered as rather benign to the SST, i.e. are aimed to guarantee SST safety rather than to exploit all its potential. Development of control methods able to fully exploit SST power devices and passives (e.g. cells capacitors) would be critical to make the technology more appealing.

- New configurations in the MMC-based multiport power converter including integration of energy storage at cell level and integration of low voltage sources and/or loads. This will also imply a redesign of control strategies. This issue has been partially addressed in this thesis, but further analysis would be needed.

- Fault tolerance. This is a critical issue for modular converters, including SSTs. Modularity opens the opportunity for redundancy, which is of enormous importance for fault tolerance. However, structures based on MMC architectures using half-bridges are enormously sensitive to short circuits in the HVDC port. Potential solutions to this problem include the use of mechanical breakers, replacement of half-bridge cells by full-bridge cells, or the development of alternative cells topologies. All the previous solutions have drawbacks either in terms of cost, losses, or recovery time after the fault. Although the analysis of this issue was beyond the scope of this thesis, development of efficient and reliable fault tolerant methods will be of a paramount importance to make SSTs a competitive solution.

- Review of standards and regulations applicable to SSTs and proposal of new standards. As already discussed, SSTs present substantial differences with respect to conventional transformers. Consequently, reg-

ulations developed for conventional transformers cannot be by any mean extended to SST. On the other hand, a precise definition of SST requirements will be critical for their development and widespread use in the electrical system. Revision of existing standards and regulations which might be applicable to SSTs, and proposal of new standards will be undoubtedly a topic of the maximum relevance, especially from an industry perspective.

- Finally, construction of a fully operational MMC-based SST suitable for the experimental verification and validation of all the concepts discussed in this thesis would be needed.

Chapter 6

Conclusiones y Trabajo Futuro

6.1 Conclusiones

Esta tesis ha llevado a cabo un profundo análisis del estado del arte de los convertidores multinivel. Primeramente se describe el nuevo escenario energético para resaltar la importancia de los convertidores electrónicos de potencia y en particular, de los convertidores multinivel. Se han analizado tanto las topologías más asentadas como las más recientes, finalizando con una introducción al concepto de Transformador de Estado Sólido. Los antecedentes de los Transformadores de Estado Sólido también han sido abordados, proponiendo además una clasificación de los mismos.

A continuación, el Convertidor Modular Multinivel (MMC) ha sido analizado en detalle. Este convertidor puede ser visto como la respuesta a la necesidad de tener un convertidor AC-DC bidireccional con una estructura completamente modular. Sus principios de operación, modelado y ecuaciones de balance de potencias han sido estudiados en detalle. Se ha prestado una especial atención a su característica más distintiva: la corriente circulante. Además, se ha estudiado el dimensionamiento de elementos pasivos, tales como las bobinas de las ramas y los condensadores de celda.

Este trabajo también ha considerado aspectos operacionales, como estrategias de modulación, métodos de equilibrado de tensión de los condensadores de celda y control del MMC. Estas tres características no son totalmente independientes puesto que la elección de un cierto método de equilibrado de tensiones puede que imponga restricciones en la estrategia de modulación que se puede aplicar. Se ha realizado un análisis exhaustivo

en este aspecto. Adicionalmente, se ha presentado el control del MMC, empezando por los principales objetivos de control para finalmente centrarse en las diferentes opciones para el control de la corriente circulante. Además, se han estudiado los esquemas de control más relevantes incluyendo su relación con los métodos de equilibrado de tensión de los condensadores. La operación del MMC ante restricciones en la tensión también ha sido analizada, incluyendo no sólamente el uso de estrategias de sobremodulación para incrementar la componente fundamental de la tensión AC sino también la operación en caso de que existan celdas defectuosas.

El Convertidor Modular Multinivel ha sido la base para una topología de convertidor multipuerto. En este aspecto, se ha estudiado en detalle la modificación de las celdas convencionales del MMC para tener capacidad de transferir potencia y habilitar las capacidades multipuerto. Los convertidores multipuerto resultantes se han clasificado en topologías simétricas y asimétricas, en función del número y posición de las celdas que transfieren potencia.

Las configuraciones asimétricas han sido estudiadas en detalle, comenzando por las distintas topologías posibles que incluyen celdas con capacidad de transferir potencia. A continuación, se han analizado las limitaciones en el equilibrio de potencias, los límites de operación y los límites de tensión. Se ha elaborado un análisis matemático para analizar los límites en la capacidad para transferir potencia a partir de los posibles desequilibrios de tensión. Finalmente, se han presentado y estudiado estrategias de control capaces de funcionar con las citadas configuraciones asimétricas.

Las configuraciones simétricas también han sido abordadas. Estas configuraciones constituyen la base para las topologías multipuerto basadas en el MMC (i.e. Transformador de Estado Sólido). Los modos de operación así como las estrategias de control convencionales aplicadas a los convertidores multipuerto han sido estudiadas en profundidad. Se ha incluido además una implementación práctica del sistema de control para un convertidor de potencia multipuerto basado en MMC. Para completar el estudio global, se han comparado transformadores de estado sólido multipuerto basados en CHB y MMC, comenzando por un análisis individual de ambas configuraciones y finalizando con una comparativa en función de sus capacidades y número y características de sus dispositivos.

6.2 Aportaciones

Las principales aportaciones de este trabajo se enumeran a continuación:

- En el momento en que este trabajo estaba elaborándose, la información disponible en la literatura acerca de los convertidores multinivel modulares era muy confusa, dispersa y alguna veces incluso caótica. Una de las principales aportaciones de esta tesis se ha centrado en recopilar toda la información disponible y elaborar unos claros antecedentes y una correcta visión global de los convertidores modulares multinivel. Una meta importante de este trabajo se ha centrado en la clasificación y análisis de las estrategias de modulación, métodos de equilibrado de tensiones de los condensadores de celda, elementos pasivos (i.e. bobinas en las ramas y condensadores de celda), estrategias de control y la influencia y relación entre todos ellos. Adicionalmente, se ha propuesto una clasificación de las estrategias de control basada en el control de la corriente circulante.

- Se ha estudiado la operación de los convertidores modulares multinivel ante restricciones de tensión, incluyendo no sólamente el uso de estrategias de sobremodulación para incrementar la componente fundamental de la tensión AC sino también la operación en caso de una celda defectuosa.

- Se han obtenido topologías innovadoras derivadas del MMC a partir de modificar las celdas convencionales basadas en medios puentes, para obtener capacidad de transferir potencia.

- Se ha adaptado la topología MMC a una configuración multipuerto. Los convertidores multipuerto basados en MMC se han clasificado en topologías asimétricas y simétricas en función del número y posición de las celdas que transfieren potencia.

- En el caso de las topologías asimétricas de convertidores multipuerto basados en MMC, se han analizado diferentes configuraciones y se ha estudiado su viabilidad considerando las restricciones derivadas del equilibrio de potencias. Se han analizado además los límites de operación de las celdas con capacidad para transferir potencia a partir de un análisis matemático.

- Se han propuesto y analizado estrategias de control específicas para topologías asimétricas de convertidores multipuerto basados en MMC.

- Se ha establecido el transformador de estado sólido basado en MMC como una caso particular de la topología simétrica. Se han adaptado las estrategias de control convencionales para ser operativas en estas configuraciones.

- Se ha estudiado la implementación práctica del sistema de control para un convertidor multipuerto basado en MMC.

- Se ha desarrollado un análisis comparativo entre transformadores electrónicos de potencia multuipuerto basados en CHB y MMC, incluyendo funcionalidades así como los requisitos y potencia de los dispositivos.
- Se han construido prototipos experimentales para validar los conceptos desarrollados a lo largo de este trabajo.

6.3 Trabajo Futuro

A partir del trabajo desarrollado a lo largo de esta tesis, se han encontrado una serie de temáticas que pueden considerarse altamente relevantes y que merecen ser exploradas más adelante:

- Optimización del rendimiento del SST. Los SST son significativamente más complejos y caros que los transformadores convencionales. Además, es discutible que sean más eficientes (esto puede ser verdad para bajos niveles de carga pero no para altas cargas o a operación a plena carga) o mś pequeños (densidad de potencia más alta), puesto que la reducción en peso y volumen gracias al empleo de transformadores de alta frecuencia se ve compensado por la necesidad dispositivos electrónicos de potencia, pasivos, elementos auxiliares, etc. El aspecto en el que los SST son sin duda superiores a los transformadores convencionales es su controlabilidad. Los SST pueden implementar algoritmos complejos para satisfacer múltiples objetivos de control, como crear una red con un control preciso de la tensión generada, control de los flujos de potencia, compensación de armónicos y desequilibrios, capacidad de ride through, etc. Los métodos de control publicados hasta ahora se pueden considerar como bastantes benignos para el SST, i.e. su objetivo es garantizar la seguridad del SST más que explotar todo su potencial. El desarrollo de estrategias de control capaces de explotar en su totalidad los dispositivos de potencia y pasivos del SST (e.g. los condensadores de celda) seria crítico para hacer esta tecnología más atractiva.
- Nuevas configuraciones de convertidores multipuerto basados en MMC que incluyan integración de almacenamiento de energía a nivel de celda e integración de fuentes y/o cargas de baja tensión. Esto también implicará un rediseño de las estrategias de control. Esta temática ha sido parcialmente desarrollada en esta tesis pero un análisis más exhaustivo sería necesario.
- Tolerancia a fallos. Se trata de un asunto crítico para los convertidores modulares, incluyendo los SST. La modularidad abre la oportunidad

para la redundancia, lo cual es de importancia capital para la tolerancia a fallos. Sin embargo, las estructuras basadas en topologías MMC con medios puentes son muy sensibles a cortocircuitos en el puerto HVDC. El uso de interruptores mecánicos, la sustitución de los medios puentes por puentes completos, o el desarrollo de topologías de celda alternativas, se tratan de potenciales soluciones a este problema. Todas estas alternativas presentan inconvenientes en términos de coste, pérdidas o en tiempo de recuperación tras el fallo. Aunque el análisis de esta temática se encontraba más allá del objetivo de esta tesis, el desarrollo de métodos eficientes y fiables de tolerancia a fallos, será de suma importancia para hacer de los SST una solución competitiva.

- Revisión de los estándares y regulaciones aplicadas a los SST y propuesta de nuevos estándares. Como se comentó con anterioridad, los SST presentan una diferencia sustancial con los transformadores convencionales. Como consecuencia, las regulaciones desarrolladas para los transformadores convencionales no pueden bajo ningún concepto extenderse a los SST. Por otro lado, una definición precisa de los requisitos del SST será crítica para su desarrollo y uso generalizado en el sistema eléctrico. La revisión de los estándares y regulaciones existentes que puedan ser aplicables a los SST, así como la propuesta de nuevos estándares, se tratará indudablemente de un tema de máxima relevancia, especialmente desde el punto de vista de la industria.

- Para finalizar, la construcción de un SST basado en MMC completamente operativo sería necesaria para la verificación experimental y validación de todos los conceptos abordados a lo largo de esta tesis.

Appendix A

Experimental Setups & Results

A.1 Introduction

Research carried out during this thesis mainly dealt with the control of an MMC-based SST. Construction of a fully operational power converter of this kind is a extremely difficult task as in addition to the control, it involves the development of sophisticated power electronics and communications. This task was therefore beyond the scope of this thesis. Even if a full SST has not been built, many of the concepts proposed in this thesis have been verified in dedicated test benches. This section describes the experimental prototypes constructed along this thesis and discusses the experimental results.

Prototypes developed along this work, their current state of development and the experimental tests carried out are summarized in Table A.1

Table A.1: Experimental setups summary

Converter topology	Current State	Tests
Down scaled Single-phase MMC	Fully Operative	Circulating current control
Down scaled Three-phase MMC	Under Construction	None
Down scaled Single-phase MMC-based SST	Fully Operative	Asymmetric operation
Down scaled Three-phase MMC-based SST	Under Construction	None
Full-size CHB-based SST cell	Fully Operative	Individual cell commissioning

A.2 Down scaled Single-phase MMC

An eight cell, single-phase MMC has been designed and built in order to verify the different control methods discussed in Section 3.6.1. The details of the prototype are shown in Table A.2. Individual submodules have been developed as conventional MMC cells based on a half bridge structure and a DC link capacitor. Fig. A.1 shows the MMC submodule used for this prototype, while Fig. A.2 offers a view of the single-phase MMC prototype.

Table A.2: MMC experimental setup

Power switches	600V/23A
Cell capacitor/Arm inductance	2000uF/1mH
Cell voltage/DC bus voltage	100V/400V
Switching frequency	5Khz

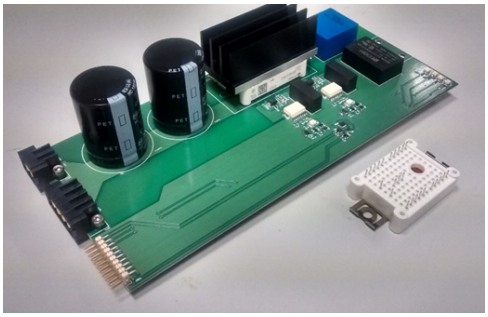

Figure A.1: MMC half bridge cell.

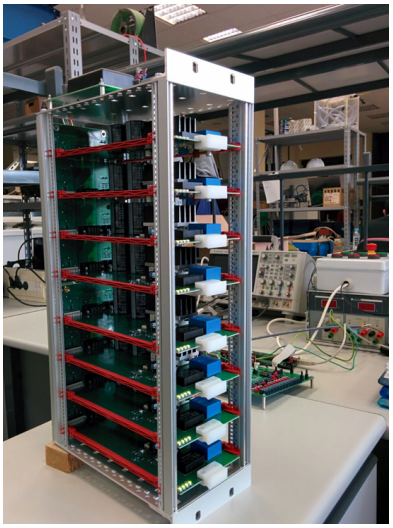

Figure A.2: Eight cells, single-phase MMC prototype.

A.2.1 Circulating current control tests

Four circulating current control strategies of those discussed in Section 3.6.1 were selected for their experimental verification using this prototype, namely: Direct modulation, control of the DC component, control of the DC and $2\omega_e$ components and control of the DC component and suppression of the $2\omega_e$ component.

Single phase power will unavoidably lead to oscillations at twice the fundamental frequency (i.e. $2\omega_e$) either in the circulating current, in the capacitor voltages, or both. Hence, the magnitude of the $2\omega_e$ component of the circulating current and capacitor voltages have been chosen as a representative metric to verify the performance of the control strategies being tested. Fig. A.3 shows the magnitude of the $2\omega_e$ component of the circulating current (i_c) and a capacitor voltage (v_{cap1}) for the control strategies listed above. The magnitudes are in % of the worst case (direct modulation).

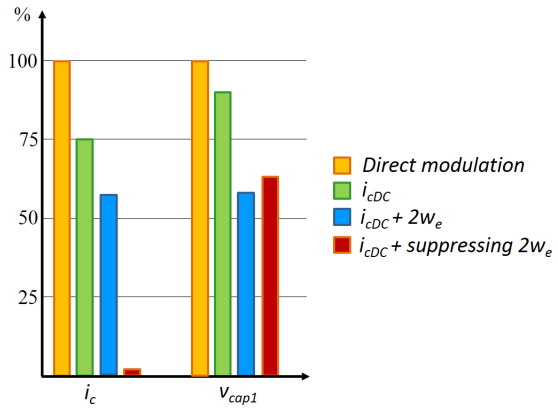

Figure A.3: Magnitude of the $2\omega_e$ component of circulating current i_c and a capacitor voltage v_{cap1}, for four different control strategies. The magnitudes are in % of the worst case (direct modulation).

It is readily observed the large magnitude of the harmonic at twice the fundamental frequency ($2\omega_e$) for the Direct Modulation strategy. By controlling the $2\omega_e$ component in the circulating current, this component as well as the oscillations of the capacitor voltage are significantly reduced. However, as expected, total suppression of the $2\omega_e$ component in the circulating current produces a slightly increase of the $2\omega_e$ component of the capacitor voltage.

Fig.A.4 shows experimental waveforms of top and bottom arm currents (i_T,i_B), and a capacitor voltage from top and bottom arms (v_{cap1}, v_{cap5}). Direct modulation was used for the results in Fig.A.4-a), the strategy $i_{cDC}+$

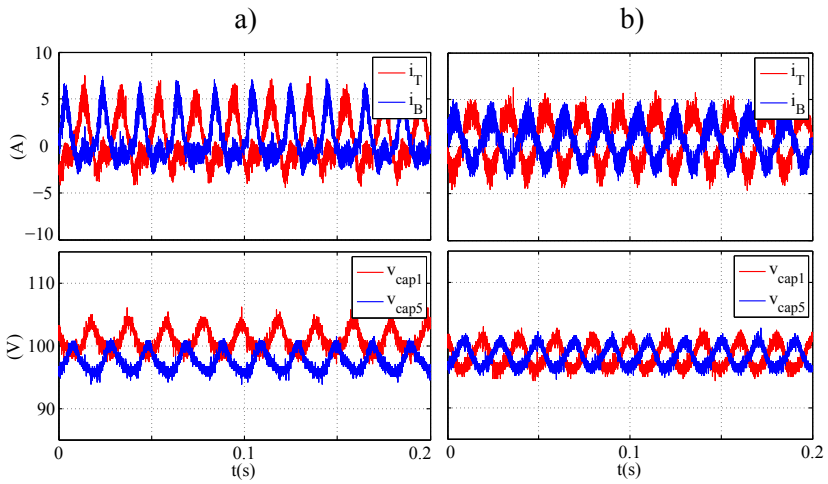

Figure A.4: Top, bottom arm currents i_T,i_B and capacitor voltages from top and bottom arms v_{cap1},v_{cap5} under two different control strategies. a) Direct modulation. b) $i_{cDC} + 2\omega_e$.

$2\omega_e$ being used for the results shown in Fig.A.4-b). It is readily observed that the oscillations of both currents and voltages are significantly reduced by controlling the circulating current.

A.3 Down scaled Three-phase MMC

From the experience acquired with the prototype shown in the preceding section, a second generation, three-phase MMC converter has been designed and built. The prototype is shown in Fig. A.5, it is not fully operational.

Due to the increased hardware requirements for the three-phase converter, experimental verification was limited to the single-phase case. Results are similar to those shown in Section A.2.1, they are not shown for the shake of brevity.

A.4 Down scaled Single-phase MMC-based SST

Derived from the design shown in section A.2, a single-phase MMC-based multiport power converter has also been designed and built. This experimental setup consists of two main parts:

- Single-phase MMC prototype as shown in Fig. A.2

Figure A.5: Eight cells, three-phase MMC prototype. Cells (left) and backplane (right)

- 8 Dual Active Bridge (DAB) converters (see Fig. A.6), whose main features are summarized in Table A.3

Table A.3: DAB experimental setup

Input voltage (LVDC)/Output voltage (v_{cell})	12V/80V
Switching frequency	100 KHz
Transformer leakage inductance	$5\mu H$

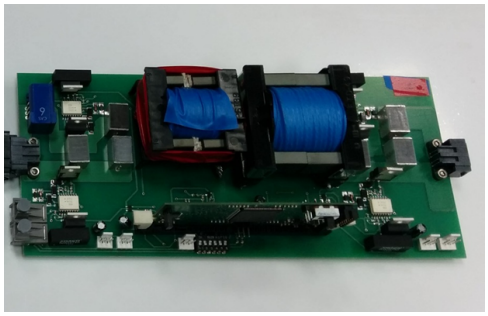

Figure A.6: Dual Active Bridge (DAB) converter.

A.4.1 Asymmetric Operation

In the experiments carried out on the single-phase MMC-based multiport power, both HVDC and LVDC ports were supplied externally, while an inductive load was connected in the HVAC port. Response of the control when asymmetric cell power is injected was verified by commanding only two DABs (i.e. 1 and 8) to inject power from the LVDC port to the HV side.

Fig. A.7 illustrates the multiport power converter setup for this experiment. Power flows from the LVDC and HVDC ports to the load placed in the HVAC port. No explicit selection of voltage imbalance commands has been carried out (see Section 4.2.4.1).

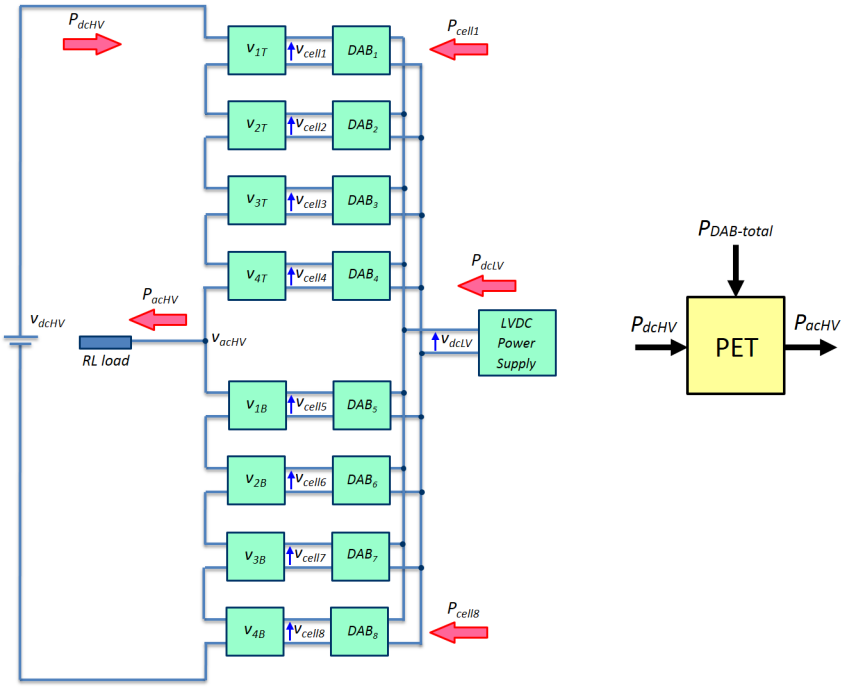

Figure A.7: Left- Schematic representation of one phase of the MMC-based multiport power converter developed as experimental setup. Right- Power flow directions in the converter.

Fig. A.8 shows the DC component as well as the magnitude and phase of the AC component (i.e. component at the fundamental frequency) of the cell voltages for the top arm, both for the case when the cells do not transfer power (conventional MMC) and when one cell per arm transfers power. Power transferred by the cells is 20% of the power delivered to the HVAC load. It is noted that bottom arm behaves similarly.

It is observed from this figure that the sorting algorithm naturally responds to power injection by cells by varying the magnitude and angle of the cell AC voltages, the DC voltage being barely affected. It is also noted that larger changes are observed in the angle of cell #4. This experimental verification has been used as the starting point to develop an optimized method to control the voltage imbalances, as shown in Section 4.2.4.2.

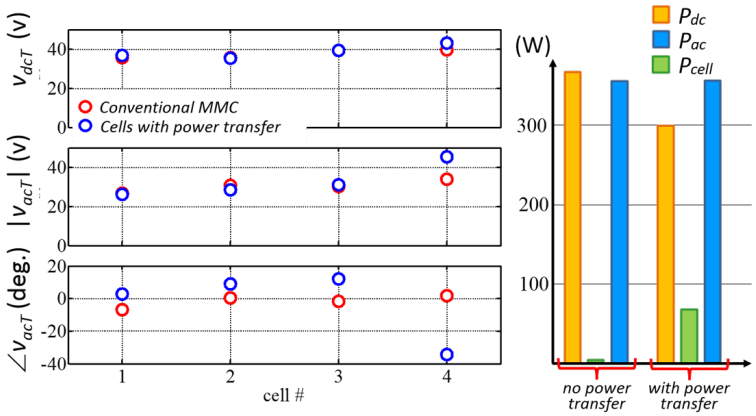

Figure A.8: Left- DC and AC component of cell voltages for cells #1 to #4 when $P_{DAB-total} = 0$ and $P_{cell1} + P_{cell8} = P_{DAB-total} = 0.2P_{acHV}$. Right- DC, AC and cell powers without/with cell power transfer.

A.5 Down scaled Three-phase MMC-based SST

A three-phase MMC-based multiport power converter has also been designed and built, although it is not fully operative. This experimental setup consists of two main parts:

- Three-phase MMC prototype as shown in Fig. A.5
- 24 Dual Active Bridge (DAB) converters (see Fig. A.6)

Fig. A.9-top shows the overall three-phase converter, including MMC and DABs, while Fig. A.9-bottom shows an individual cell, including the MMC half bridge and the DAB.

A.5.1 Asymmetric Operation

Experimental results have been obtained for single-phase operation, they are similar to those shown in Section A.4.1 and have not been included in this section. Commissioning of the three-phase converter has not been completed yet.

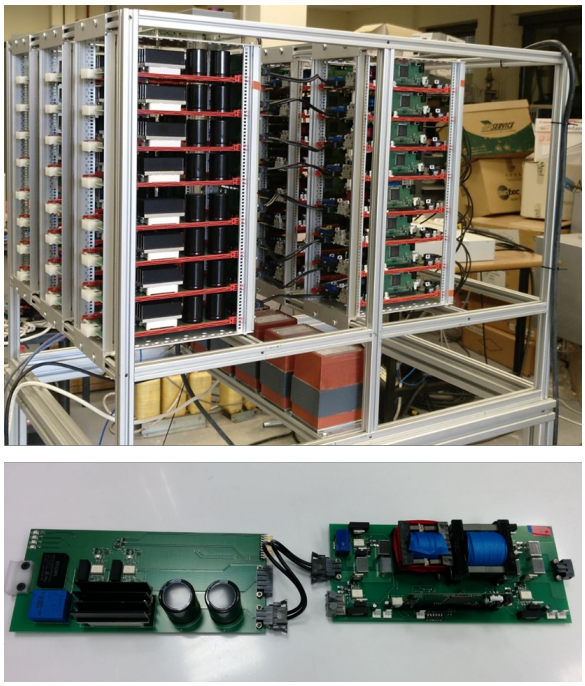

Figure A.9: Top- MMC-based Multiport Power Converter experimental prototype. Bottom- Individual cell: MMC half bridge + DAB.

A.6 Full-size CHB-based SST cell

In the framework of FP7-SPEED project, a CHB-based Power Electronic Transformer has been developed (see Section 4.4.1). This converter is intended to connect a 6kV AC grid with a conventional 400V AC grid. To achieve this, cell voltage has been set to 800V and thus, 7 cells per phase (21 cells in the whole tree phase arrangement) are required. With the mentioned cell voltage, 1.2kV Silicon Carbide CREE power MOSFETS are used in the DAB while 1.7kV INFINEON IGBT power modules are used in the full-bridge related to the CHB. LVDC sides of the DABs are parallelized (as shown in Fig.4.29) and a conventional DC/AC converter is used to connect with the LVAC grid. Control of the converter is based on a *distributed control* solution as those explained in Section 4.3.4.2. Parameters of the experimental setup are summarized in Table A.4. It is finally noted that though the target AC voltage in the HV side is 6 kV, the system should be scalable up to 24 kV. This would be achieved by simply piling up more cells. However, this must be considered for the cell design, as the high frequency transformer must be designed to provide this isolation.

Fig.A.10-left shows an individual cell consisting of a the full-bridge for the CHB side, the cell capacitor and the DAB connecting high-voltage and

Table A.4: CHB-based PET experimental setup

HVAC side	6kV (3ph-rms)
LVAC side	400V (3ph-rms)
Rated power	105kW
CHB power switches	1.7kV/30A
DAB power switches	1.2kV/28A
Cell capacitor	600uF
Cell voltage	800V
DAB input/output voltage	800V/800V
CHB switching frequency	4.8Khz
DAB switching frequency	30Khz

low-voltage sides. It is noted the high frequency transformer has a remarkable size due to the required isolation of 24kV. Fig.A.10-right shows the cabinet containing the whole converter consisting of 21 cells (7 per phase). Cell design is complete, some experimental results being shown in the next subsection. Construction of the whole power converter is still ongoing.

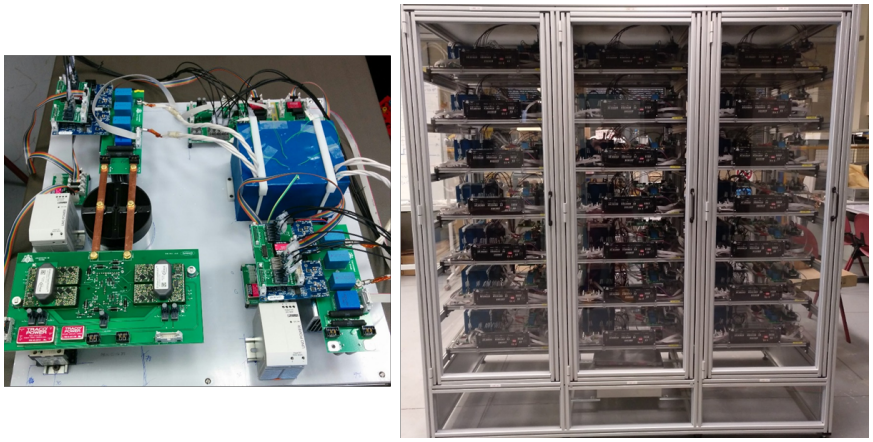

Figure A.10: Left- CHB-based PET cell consisting of Full-bridge + DAB. Right- CHB-based PET experimental setup.

A.6.1 Cell commissioning

Cells have been fully tested for different modes of operation at their rated conditions. An example of configuration for the experimental set up is schematically shown in Fig.A.11. LVDC side is supplied from a DC power supply. DAB is commanded to transfer 4kW from the LVDC side to the CHB side. This is performed by controlling the DAB output current (i_{DAB}) through the phase-shift between the two full-bridges. DAB operates therefore in a current regulated mode. Finally, the CHB full-bridge controls the cell voltage (v_{cell}) to maintain it at its target value. The power injected by

the DAB is evacuated to an RL load. This form of operation of the cell would correspond to a configuration of the SST in which the LVAC port is connected to an existing grid while the power converter creates the HVAC grid (i.e. grid-feeding in the LV side and grid-forming in the HV side).

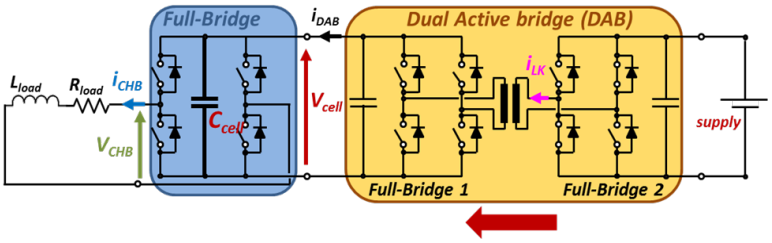

Figure A.11: Cell connections for the experimental verification. Power is transferred from the DAB to the CHB cell (i.e. from LV to HV port). An RL load is connected to the output of the CHB full bridge to dissipate the power.

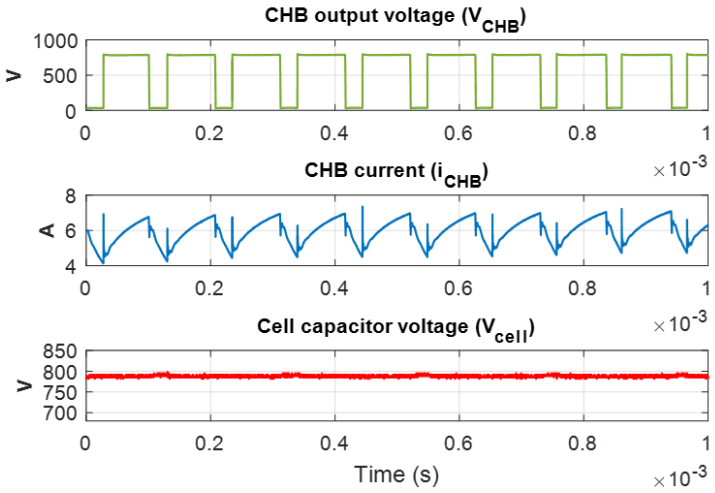

Figure A.12: CHB full-bridge current and voltage waveform. The DAB controls iDAB to a target valued received from the central control. CHB full-bridge controls V_{cell} to its target value of 800 V

Fig. A.12 shows the CHB voltage (i.e. the voltage applied to the RL load (V_{CHB}), the corresponding load current (i_{CHB}) and the voltage at the cell capacitor (V_{cell}). Capacitor voltage is seen to be precisely controlled at its target value of 800V. As for the DAB converter, Fig. A.13 shows gate signals for both the primary and secondary bridges. The phase shift among signals is controlled to transfer the required current. Fig. A.13 also shows the current through the leakage inductance (i_{Lk}), waveform evidencing ZVS condition.

As previously explained, this experiment has been carried out at rated

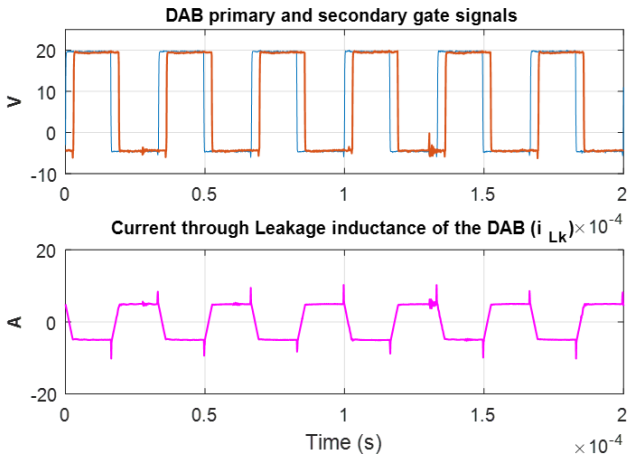

Figure A.13: DAB waveforms during experimental test.

conditions of 4kW and 800V. Thermal stress on the HF transformer has also been studied. Temperature at the surface has been measured using a thermal camera, obtaining around $40°C$ at the surface hottest point of the encapsulation, after three hours of operation at rated power and fan-cooled.

Appendix B

Related publications

B.1 Summary of Publications

1. Title: Operation and Control of MMCs Using Cells with Power Transfer Capability

    - Authors: Fernando Briz, Mario Lopez, Alberto Zapico, Alberto Rodriguez, David Diaz-Reigosa
    - Conference: 30th Annual IEEE Applied Power Electronics Conference & Exposition (APEC), 15-19 March 2015, Charlotte, NC, USA

2. Title: Comparative Analysis of Control and Modulation Strategies for Modular Multilevel Converters * [1]

    - Authors: Mario Lopez, Fernando Briz, Alberto Zapico, David Diaz-Reigosa
    - Conference: 22th Seminario Anual de Automatica, Electronica Industrial e Instrumentacion (SAAEI), 8-10 July 2015, Zaragoza, Spain

3. Title: Retos Tecnológicos en el Desarrollo de un Transformador de Estado Sólido Basado en un MMC con Inyección de Potencia a Nivel de Celda

    - Authors: Alberto Rodriguez, Manuel Arias, Javier Sebastian, Mario Lopez, Alberto Zapico, Fernando Briz

[1] * is used to indicate papers presented at the conference by the candidate

- Conference: 22th Seminario Anual de Automatica, Electronica Industrial e Instrumentacion (SAAEI), 8-10 July 2015, Zaragoza, Spain

4. Title: MMC Based SST

   - Authors: Fernando Briz, Mario Lopez, Alberto Rodriguez, Alberto Zapico, Manuel Arias, David Diaz-Reigosa
   - Conference: IEEE 13th International Conference on Industrial Informatics (INDIN), 22-24 July 2015, Cambridge, UK

5. Title: Design and Implementation of the Control of a MMC-Based Solid State Transformer

   - Authors: Mario Lopez, Alberto Rodriguez, Enrique Blanco, Mariam Saeed, Angel Martinez, Fernando Briz
   - Conference: IEEE 13th International Conference on Industrial Informatics (INDIN), 22-24 July 2015, Cambridge, UK

6. Title: Control Strategies for MMC Using Cells with Power Transfer Capability *

   - Authors: Mario Lopez, Fernando Briz, Alberto Zapico, Alberto Rodriguez, David Diaz-Reigosa
   - Conference: 7th Energy Conversion Congress and Exposition (ECCE), 20-24 Sept. 2015, Montreal, Canada

7. Title: Operation of Modular Multilevel Converters Under Voltage Constraints *

   - Authors: Mario Lopez, Fernando Briz, Alberto Zapico, David Diaz-Reigosa, Juan Manuel Guerrero
   - Conference: 7th Energy Conversion Congress and Exposition (ECCE), 20-24 Sept. 2015, Montreal, Canada

8. Title: Auxiliary Power Supply Based On A Modular Isop Flyback Configuration With Very High Input Voltage

   - Authors: Alberto Rodriguez, Maria R. Rogina, Mariam Saeed, Diego G. Lamar, Manuel Arias, Mario Lopez, Fernando Briz
   - Conference: 8th Energy Conversion Congress and Exposition (ECCE), 18-22 Sept. 2016, Milwaukee, WI, USA

9. Title: Fault Tolerant Cell Design for MMC-based Multiport Power Converters *

- Authors: Alberto Zapico, Mario Lopez, Alberto Rodriguez, Fernando Briz
- Conference: 8th Energy Conversion Congress and Exposition (ECCE), 18-22 Sept. 2016, Milwaukee, WI, USA

10. Title: Comparative Analysis of Modular Multiport Power Electronic Transformer Topologies *

    - Authors: Mario Lopez, Fernando Briz, Mariam Saeed, Manuel Arias, Alberto Rodriguez
    - Conference: 8th Energy Conversion Congress and Exposition (ECCE), 18-22 Sept. 2016, Milwaukee, WI, USA

11. Title: Modular Power Electronic Transformers: Modular Multilevel Converter Versus Cascaded H-Bridge Solutions

    - Authors: Fernando Briz, Mario Lopez, Alberto Rodriguez, Manuel Arias
    - Magazine: IEEE Industrial Electronics Magazine, vol. 10, no. 4, pp. 6-19, Dec. 2016

12. Title: Start-up, functionalities and protection issues for CHB-based Solid State Transformers

    - Authors: Jose Maria Cuartas, Antonio De La Cruz, Fernando Briz, Mario Lopez
    - Conference: 17th International Conference on Environment and Electrical Engineering (EEEIC), 6-9 June 2017, Milan, Italy

13. Title: Design and construction of a DAB using SiC MOSFETs with an isolation of 24 kV for PET applications

    - Authors: Mariam Saeed, Maria R. Rogina, Mario Lopez, Alberto Rodriguez, Manuel Arias, Fernando Briz
    - Conference: 19th European Conference on Power Electronics and Applications (EPE 17 ECCE Europe), 11-14 Sept. 2017, Warsow, Poland

Operation and control of MMCs using cells with power transfer capability

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***Abstract*— Cells in conventional Modular Multilevel Converters (MMC) designs use a capacitor for energy storage. This means that the net power balance for each cell (neglecting losses) needs to be equal to zero, the MCC realizing therefore a power transfer between its DC and AC sides. This paper analyzes the design, operation and control of MMCs in which the cells have the capability to transfer (inject or drain) power. The use of such cells opens several new functionalities and uses for the MMC. On one hand, it would allow integrating elements like distributed energy storage (e.g. batteries), low-voltage/low power sources (e.g. PV) and loads at the cell level. Cells with power transfer capability can also be used connect the medium/high voltage DC and AC ports intrinsic to the MMC, with low voltage DC/AC ports at the cell level. This would result in multiport power converters, potential applications of this topology including solid state transformers (SST).[1]**

Keywords—Modular Multilevel Converter, MMC, Energy Storage Integration, DER Integration, Solid State Transformer

I. Introduction

The increasing penetration of renewable energies as well as the demanding requirements in terms of efficiency and reliability for their integration in the power transmission system poses a big challenge, which is expected to increase in the near future, as a significant part of the installed capacity will be connected to the distribution levels [1]. Power electronics-based technologies, like HVDC and FACTS, able to provide functionalities to the power operator such as power flow control, reduction of transmission losses and power quality improvement, will be key for this purpose [2].

The MMC was proposed one decade ago [3]-[5]. It shares several advantageous characteristics of other modular multilevel topologies, like reduced losses due to low switching frequencies and good output voltage wave shape, which leads to smaller filters and reduced voltage stress in the power devices [3]-[5]. Also, its structure based on simple cells provides scalability, which is key to achieve high voltage levels using relatively low voltage power devices. A distinguishing characteristic of the MMC is that while it provides a high voltage DC link, the distributed energy storage at the cells capacitors eliminates the need of a bulk DC capacitor, which is advantageous for safety and reliability reasons [8].

Conventional MMC designs realize a bidirectional DC-AC power conversion (see Fig. 1). The block diagram in Fig. 1-left is valid to represent either a single phase or a three-phase MMC.

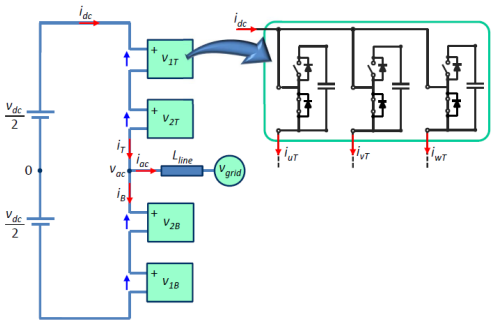


Fig. 1.- Left - Schematic representation of a conventional MMC, with the cells consisting of a half bridge For the sake of clarity, the arm inductances are not shown. Right – Corresponding cell circuit for the case of a three-phase MMC.

The physical cells forming each arm of the power converter typically consist of a half bridge and a capacitor. For the three-phase case, each cell in Fig. 1-left physically corresponds to three individual cells (Fig. 1-right). All the analysis and discussion following assumes a three-phase AC system. However, the concepts discussed are also valid for the single-phase case. For analysis purposes, it is also assumed that the AC port of the MMC is connected to a stiff grid through a purely inductive line. Active and reactive power in the AC port are therefore controlled through the AC voltage v_{ac}. Control and modulation strategies developed for MMC are aimed to balance the power transfer between the AC and DC ports, which is done controlling the circulating current [9]-[14], as well as to balance the cell capacitor voltages [3]-[16]. Because the cells of the MMC have a limited energy storage capability, the net power balance for each cell is zero (neglecting losses), the power at the AC and DC sides of the MMC being therefore equal to each other.

It is possible to modify the MMC to transfer power at the cell level. This would provide the MMC new potential capabilities, including distributed storage [19]; integration of distributed energy resources (DER) at the cell level; multiport power converters combining the medium/high voltage DC and AC ports of the MMC with low voltage DC and AC ports; and solid state transformers. Such modification involves changes both in the cells design as well as in the control strategy. For the cells design, an electronic power converter will be needed in a general case to connect the power source transferring power

[1] This work was supported in part by the Research, Technological Development and Innovation Programs of the Spanish Ministries of Science and Innovation and of Economy and Competitiveness, under grants MICINN-10-CSD2009-00046 and MINECO-13-ENE2013-48727-C2-1-R, and by the European Commission FP7 Large Project NMP3-LA-2013-604057, under grant UE-14-SPEED-604057.

to the cell (either injecting or draining) with the cell capacitor. Depending on the characteristics of this power source (energy storage device, renewable energy sources, …), unidirectional or bidirectional power flow capability can be needed. Regarding the control strategies, the existing methods assume that all the cells in the MMC have identical design and operate identically. However, this is not true anymore if cells with the capability to transfer power exist.

This paper analyzes the design, operation and control of MMCs in which one or more cells have the capability to transfer (inject or drain) power. As for the conventional MMC, the control has to balance the power and provide the required AC and DC voltages at the MMC terminals. However, and contrary to the conventional MMC, the power transferred by the cells will affect to the power balance, resulting in unbalances in the cells operating point. The paper is organized as follows. The model of the conventional MMC, i.e. without power transfer at the cell level, is presented in Section II. Design and operation of cells with power transfer capability are discussed in Sections III and IV. Control strategies are discussed in Section V. Experimental results using a single phase MMC are shown in Section VI, the conclusions being presented in Section VII.

II Model and Operation of MMC with Balanced Cells

The MMC realizes a bidirectional DC-AC power conversion (see Fig. 1). For the analysis presented in this paper, a three-phase MMC is assumed. Complex vector notation will be used to represent the AC variables. The voltage and current vectors in the AC port of the MMC are defined by (1) and (2). The resulting top and bottom arm currents are shown in (3), the circulating current i_c being (4), whose DC component is equal to the DC current. Harmonics of the circulating current used e.g. to reduce the oscillations of the cell capacitor voltage [14,18], are not considered in the analysis following.

$$i_{ac} = \frac{2}{3}\left(i_u + i_v\, e^{j2\pi/3} + i_w\, e^{j4\pi/3}\right) \quad (1)$$

$$v_{ac} = \frac{2}{3}\left(v_u + v_v\, e^{j2\pi/3} + v_w\, e^{j4\pi/3}\right) \quad (2)$$

$$i_T = i_{dc} + \frac{i_{ac}}{2}\ ;\ i_B = i_{dc} - \frac{i_{ac}}{2} \quad (3)$$

$$i_c = \frac{i_T + i_B}{2} = i_{dc} \quad (4)$$

Due to the limited energy storage capability of the cells, the power in the DC port of the MMC has to be equal to the active power in the AC port (5), * standing for complex conjugate.

$$P_{dc} = v_{dc}\, i_{dc} = P_{ac} = Re\,(v_{ac}\, i_{ac}^*) \quad (5)$$

It is useful to separate the MMC in Fig. 1 into its DC and AC sub-circuits, as shown in Fig. 2. For the sake of simplicity, the voltage drop in the arm inductor will be neglected. A MMC with two cells per arm (N=2), i.e. four cells per phase, will be considered. However, the conclusions are valid for MMCs with a different number of cells per arm (N). Assuming that the MMC is perfectly balanced (identical cells, identical operating point), the DC and AC voltages for each cell are given by (6)

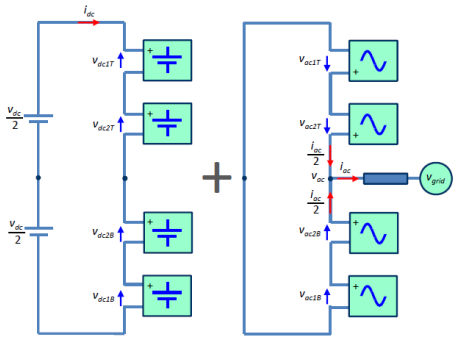


Fig. 2.- DC (left) and AC (right) sub-circuits of the MMC

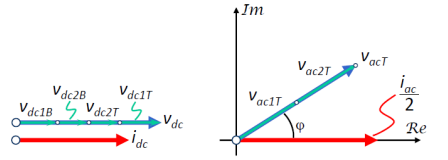


Fig. 3.- DC (left) and AC (right) voltages and currents. Only AC variables for the top arm are shown, they are the same for the bottom arm (see Fig. 2).

and (7) respectively. The overall cell voltage is therefore (8). Due to the arm inductors being neglected, the overall AC voltage for the upper and lower arms needs to be equal to v_{ac}, as they are connected in parallel (see Fig. 2-right). Consequently, the AC current splits equally between the upper and lower arms. All the cells have therefore the same DC and AC powers (9) and (10).

$$v_{dc1T} = v_{dc2T} = v_{dc1B} = v_{dc2B} = \frac{v_{dc}}{2N} = \frac{v_{dc}}{4} \quad (6)$$

$$v_{ac1T} = v_{ac2T} = v_{ac1B} = v_{ac2B} = \frac{v_{ac}}{N} = \frac{v_{ac}}{2} \quad (7)$$

$$v_{nX} = v_{acnX} + v_{dcnX} \quad \text{with } n = 1, 2 \text{ and } X = T, B \quad (8)$$

$$P_{dcnT} = P_{dcnB} = \frac{v_{dc}}{2N}\, i_{dc} = \frac{v_{dc}}{4}\, i_{dc} \quad ;\ n = 1, 2 \quad (9)$$

$$P_{acnT} = P_{acnB} = Re\left(\frac{v_{acT}}{N}\,\frac{i_{ac}^*}{2}\right) = Re\left(\frac{v_{acT}}{2}\,\frac{i_{ac}^*}{2}\right);\ n = 1, 2 \quad (10)$$

Fig. 3 graphically shows the DC and AC voltages for the MMC in Fig. 1 and 2. The AC voltages and currents are represented by complex vectors, the real axis being aligned with the AC current, where φ is the angle between the AC current and voltage vectors. Assumed that the voltage at the DC side of the MMC v_{dc} is constant, the MMC control has then to adjust the DC current i_{dc} to balance the power between the DC and AC ports (5). In addition, the cell capacitor voltages have to be kept at the target value. This is done by the balancing algorithms [3,4,9,12].

III. Cells with Power Transfer Capability

As already mentioned, it is possible to provide the MMCs the capability to transfer power at the cell level. Inserting cells with power transfer capability will produce, in general, unbalances in

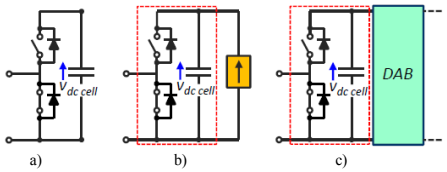


Fig. 4. a) Conventional cell with a capacitor in the DC link; b) cell with power transfer capability using a current source; c) cell using a DAB.

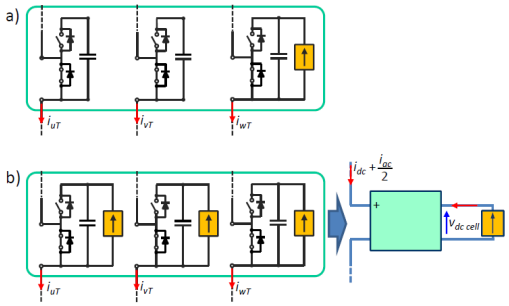


Fig. 5. a) MMC in which only one cell in one phase transfers power; b) MMC in which cells in all the three phases transfer the same (or similar) amount of power. An equivalent complex-vector cell (bottom-right) can be used in this case.

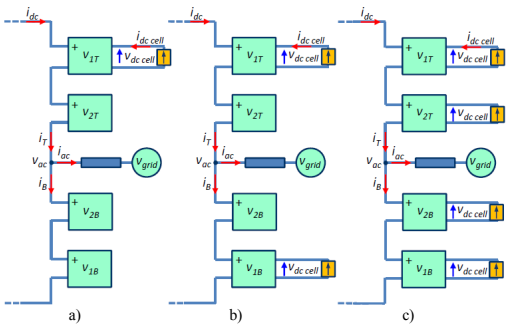


Fig. 6.- MMC including cells with power transfer capability in all the three phases. a) MMC in which only cells in the top arm transfer power; b) MMC in which the same number of cells in the top and bottom arms transfer power; c) MMC in which all the cells transfer power.

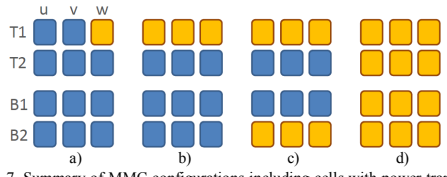


Fig. 7. Summary of MMC configurations including cells with power transfer capability. Cells in light color transfer power, cells in dark color do not (standard cells). a) Asymmetric phases (Fig. 5a); b) asymmetric top and bottom arms (Fig. 6a); c) symmetric top and bottom arms (Fig. 6b); d) fully symmetric (Fig. 6c).

the cells operation. Discussion on the design of the cells for this case, as well as the impact on the operation of the MMC, are presented in this section.

a) Cell design and power balance

When cells with power transfer capability are used, it is desirable that all the cells of the MMC have similar DC voltage $v_{dc\ cell}$, independently on whether they transfer power or not. This allows using power devices and capacitors with the same voltage ratings for all the cells. Assumed that the cells are controlled to have a capacitor voltage of $v_{dc\ cell}$, transferring power to the standard cell design in Fig. 4a can be modeled as a current source connected in parallel to the cell capacitor, as shown in Fig. 4b. It is noted however that in a practical implementation, voltage isolation between the cell capacitor and the power source will likely be needed. A current controlled dual active bridge (DAB) can be used for this purpose (Fig. 4c) [17]. This is described in section VI.

Standard MMCs require a perfect balance between the DC and AC powers (5), assumed that the losses can be neglected. Since all the cells have the same DC and AC currents, the cells are controlled to have (ideally) the same DC and AC voltages, (6) and (7). If one or more cells transfer power, the resulting MMC power balance equation is (11), where P_{cell} is the power transferred by each cell and M is the number of cells transferring power. It is assumed that all the cells transfer a similar amount of power. This restriction is discussed latter.

$$P_{dc} + MP_{cell} = P_{ac} \tag{11}$$

b) MMC topologies using cells with power transfer capability

Examples of MMC topologies using cells with power transfer capability are shown in Fig. 5 and 6. In the example shown in Fig. 5a, only one cell in phase *w* transfers power, while the cells at equivalent locations in phases *u* and *v* do not. In the case shown in Fig. 5b, all the three phases include cells with power transfer capability. This results in symmetric phases, whose AC sub-circuit can be modeled as an equivalent complex vector cell (Fig. 5b-right). This is equivalent to the complex vector cells shown in Fig. 1, but now including the current source connected to the cell capacitor. Fig. 6shows different configurations of the MMC using the complex vector cell in Fig. 5b. In the configuration shown in Fig. 6a, only cells in the upper arm transfer power. In the case shown in Fig. 6b, the same number of cells in the upper and lower arms transfer power, while in the case shown in Fig. 6c, all the cells transfer power. Fig. 7 summarizes all the cases.

Depending on the number and location of the cells transferring power (see Fig. 5 to Fig. 7), different types of asymmetries (unbalances) can occur among cells, and consequently among arms or legs of the MMC. Asymmetries cannot exist in the cells current. All the cells for each leg of the MMC have the same DC current. It is also assumed that the AC current equally splits among the top and bottom arms of each leg. In consequence, all the cells have the same DC and AC currents. Therefore, producing asymmetries in the operation of the cells will require varying their DC and/or AC voltages.

Unbalances among phases (Fig. 7a) will result in different DC voltages for the cells in phase *w*, eventually resulting in a DC zero sequence voltage in the AC voltage v_{ac}. The case shown in Fig 7b produces unbalances between the DC voltage for the top and bottom arms of all the three phases, eventually resulting in a DC

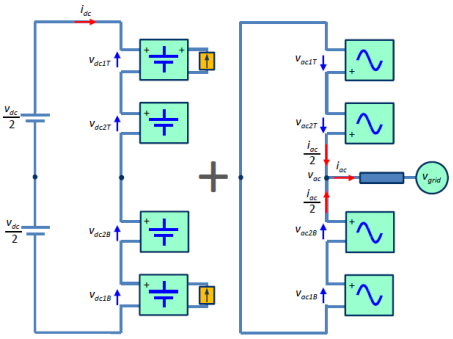


Fig. 8.- DC+cell (left) and AC (right) subcircuits of the MMC including cells with power transfer capability.

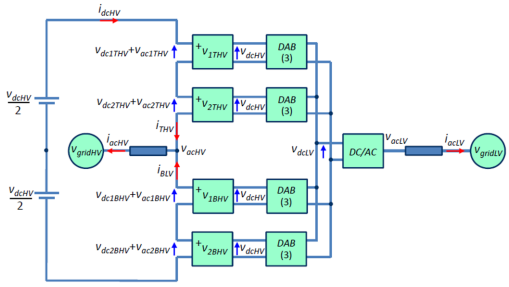


Fig. 9.- Multiport power converter using a MMC in the high voltage side and a conventional DC /AC power converter in the low voltage side.

TABLE I: TYPES OF ASYMMETRY AND EFFECTS OF CELLS WITH POWER TRANSFER:CAPABILITY

Type of asymmetry	***Effect on the AC port***	***Effect on the cells***
a) Asymmetric phases (Fig. 7a)	DC zero sequence voltage	Asymmetries in the cell DC voltages
b) Symmetric phases, asymmetric arms (Fig. 7b)		
c) Symmetric arms, asymmetric cells (Fig. 7c)s	No effect	Asymmetries in the cells DC/AC voltages
d) Fully symmetric (Fig. 7d)		No effect

zero sequence component in the AC voltage v_{ac} too. In the case in Fig. 7c, top and bottom arms are symmetric, but there are unbalances among the cells in the top arm, the same occurs for the cells in the bottom arm. These unbalances can affect to the cell DC voltage, AC voltage, or both. However, as the effect is the same in the top and bottom arms, it will not have any impact on the AC voltage of the MMC v_{ac}. Finally, the case shown in Fig. 7d does not produce any type of asymmetry or effect either in the terminal voltages, arms or cells of the MMC.

Table I summarizes the different types of asymmetries produced by cells transferring power, and the impact that these can have on the MMC behavior. Cases a) and b) produce a zero sequence voltage component in the AC voltage. Whether this is tolerable or not might depend on the application. Cases c) and d) do not have any adverse effect on the terminal properties of the MMC. However, in case c) there are differences in the operating conditions of the cells, which need to be considered for their control. This case is analyzed in more detail in the next section. Cases a), b) and d) are particular cases of c). In cases a) and b) only the cells DC voltage is varied, while case d) is an extension of case c) to all the cells.

c) MMC based multiport power converters

The use of cells with power transfer capability could potentially provide the MMC multiport capabilities. An example of this is shown in Fig. 9. It corresponds to the case shown in Fig. 7d in which all the cells transfer power. The AC and DC medium voltage ports of the MMC are connected through the cells and DABs to low voltage DC and AC ports in the right side of the figure. Other configurations are also possible, their design and analysis being the focus of ongoing research. Detailed discussion of this issue is beyond the scope of this paper.

IV. MODELING AND OPERATION OF MMC USING CELLS WITH POWER TRANSFER CAPABILITY

The use of cells with power transfer capability poses new challenges regarding the control and modulation strategies, as the methods that have been proposed are aimed to balance the operation of cells which have an identical design [3-16]. The configuration shown in Fig. 7c, (Fig. 6b) will be used for the analysis presented in this section. It has two cells per arm; cells *1T* and *1B* transfer power, while cells *2T* and *2B* do not.

a) Power balance

As already discussed in Section II, it is useful to separate the MMC in Fig. 6b into the DC and AC sub-circuits, as shown in Fig. 8. These are equivalent to the DC and AC sub-circuits shown in Fig. 2 for the conventional MMC. The power balance equation for the four cells in Fig. 8 are (12)-(15).

$$P_{dc1T} + P_{cell1T} = P_{ac1T} \tag{12}$$

$$P_{dc2T} = P_{ac2T} \tag{13}$$

$$P_{dc1B} + P_{cell1B} = P_{ac1B} \tag{14}$$

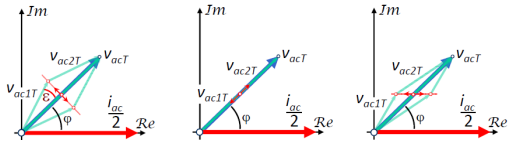
$$P_{dc2B} = P_{ac2B} \tag{15}$$

If the cells in the top and bottom arm transfer the same (or close) amount of power, then the same DC and AC voltages will exist in both arms (16). Thus, no zero sequence voltage component exists in the AC voltage of the MMC, v_{ac}. Since the AC current i_{ac} splits equally between the top and bottom arms, the power balance equation for the top arm is (17). The contribution of cells *1T* and *2T* are (18) and (19) respectively. Identical equations apply for the bottom arm.

In the preceding discussion, it has been assumed that all the cells transfer a similar amount of power P_{cell} (11). Significant unbalances among the power transferred by each individual cell in the cases shown in Fig. 7b-d, will result in asymmetric phases, being equivalent to Fig. 7a. The concerns previously discussed for this case would therefore apply.

$$v_{acT} = v_{acB} \; ; \; v_{dcT} = v_{dcB} \tag{16}$$

$$v_{dcT} i_{dc} + v_{dc\,cell} i_{dc\,cell} = Re\left(v_{acT} \frac{i_{ac}^*}{2}\right) \tag{17}$$



a) $|v_{ac1T}| = |v_{ac2T}|$ b) $\angle v_{ac1T} = \angle v_{ac2T}$ c) $Im(v_{ac1T})=Im(v_{ac2T})$

Fig. 10.- Strategies for the selection of the cell AC voltage unbalance

$$v_{dc1T} i_{dc} + v_{dc\,cell} i_{dc\,cell} = Re\left(v_{ac1T} \frac{i_{ac}^*}{2}\right) \quad (18)$$

$$v_{dc2T} i_{dc} = Re\left(v_{ac2T} \frac{i_{ac}^*}{2}\right) \quad (19)$$

b) Selection of cell voltage unbalance

The fact that cells *1T* and *1B* can transfer power while *2T* and *2B* cannot, will necessarily produce an unbalance in their operation. Since the DC and AC currents, i_{dc} and $i_{ac}/2$, are common to all the cells in the arm, the unbalance has to occur in the cell voltages v_{1T}, v_{1B}, v_{2T}, v_{2B}. This can be done unbalancing the cell DC voltage by an amount of Δv_{dc} (20)-(21), the AC voltage by an amount of Δv_{ac} (22)-(23), or both. It is noted that in all the cases (24) and (25) hold.

$$v_{dc1T} = \frac{v_{dc}}{4} + \Delta v_{dc} \quad ; \quad v_{dc1B} = v_{dc1T} \quad (20)$$

$$v_{dc2T} = \frac{v_{dc}}{4} - \Delta v_{dc} \quad ; \quad v_{dc2B} = v_{dc2T} \quad (21)$$

$$v_{ac1T} = \frac{v_{ac}}{2} + \Delta v_{ac} \quad ; \quad v_{ac1B} = v_{ac1T} \quad (22)$$

$$v_{ac2T} = \frac{v_{ac}}{2} - \Delta v_{ac} \quad ; \quad v_{ac2B} = v_{ac2T} \quad (23)$$

$$v_{dc1T} + v_{dc2T} = v_{dc1B} + v_{dc2B} = \frac{v_{dc}}{2} \quad (24)$$

$$v_{ac1T} + v_{ac2T} = v_{ac1B} + v_{ac2B} = v_{ac} \quad (25)$$

Using (12)-(25), it is possible to obtain the relationship between Δv_{dc} and Δv_{ac} and the power handled by the cells (12)-(15) and the MMC (11). For this process, it is assumed that the DC side voltage of the MMC v_{dc} and the grid voltage v_{grid} are constant (see Fig. 8), and that the active and reactive power demands from the AC port of the MMC, P_{ac} and Q_{ac}, are given. Therefore, the AC current i_{ac} and consequently the AC voltage v_{ac}, are imposed by the AC port power needs. It is also assumed that the current injected by the current source connected to the cells *1T* and *1B* in Fig. 8 ($i_{dc\,cell}$ in Fig. 6b) is determined by the power source connected to the cell capacitor, being therefore an independent variable. The DC current of the MMC i_{dc} needs then to be controlled to satisfy the overall power balance equation (11), similarly to the conventional MMC. In addition, Δv_{dc} and Δv_{ac} need to be selected to satisfy the balance equation of each cell.

The effect of Δv_{dc} on the power transferred by the cells can be readily calculated using (18)-(21). On the other hand, an extra degree of freedom exists for the selection of Δv_{ac}, since the AC voltage v_{ac} is a complex vector. Three different strategies for the selection of Δv_{ac} are shown in Fig. 10, which are defined by (26), (27) and (28) respectively. It is noted that in all the cases (25) holds.

$$|v_{ac1T}| = |v_{ac2T}| \quad ; \quad \angle v_{ac1T} \neq \angle v_{ac2T} \quad (26)$$

$$\angle v_{ac1T} = \angle v_{ac2T} \quad ; \quad |v_{ac1T}| \neq |v_{ac2T}| \quad (27)$$

$$Im(v_{ac1T}) = Im(v_{ac2T}) = Im(v_{acT})/2 \quad ;$$

$$Re(v_{ac1T}) \neq Re(v_{ac2T}) \; ; \; \angle v_{ac1T} \neq \angle v_{ac2T} \; ; \; |v_{ac1T}| \neq |v_{ac2T}| \quad (28)$$

In the strategy defined by (26) (Fig. 10a), cells *1T* and *2T* have the same AC voltage magnitude. However, the phase angle of v_{ac1T} and v_{ac2T} with respect to the AC current is different. In the strategy defined by (27) (Fig. 10b), cells *1T* and *2T* have different AC voltage magnitude, but the same phase angle with respect to the AC current. In the strategy defined by (28) (Fig. 10c), the imaginary part of the cells *1T* and *2T* AC voltage is the same, but the real components $Re(v_{ac1T})$ and $Re(v_{ac2T})$ are different.

c) Discussion on the selection of Δv_{dc} and Δv_{ac} and limits of operation

The following considerations can be made regarding the selection of the voltage unbalances Δv_{dc} and Δv_{ac} to realize the power balance of the cells (11):

- Transferring power between the cells and the DC port (29) is only possible if reactive power (reactive current) circulates through the AC port of the MMC, i.e. $Q_{ac} \neq 0$.

  $$P_{dc} = -P_{cell} \quad ; \quad P_{ac} = 0 \quad (29)$$

  This is due to the fact that the DC current i_{dc} is common to all the cells. An unbalance of Δv_{dc} in one cell would require an unbalance of $-\Delta v_{dc}$ in another cell to maintain the DC bus voltage constant (24). As a consequence, the power injected (or drained) by the first cell would be drained (or injected) by the second cell. This power would be therefore recirculated between these two cells, with no power transfer to the DC port. Consequently, AC current (either active or reactive) is required to transfer power between the cells and the MMC.
- It is possible to transfer power between the cells and the AC port of the MMC when the DC current i_{dc} is zero, i.e.

  $$P_{cell} = P_{ac} \quad ; \quad P_{dc} = 0 \quad (30)$$

  The amount of power that can be transferred by the cells, P_{cell}, increases with the AC current magnitude and with the power factor (cos(φ)) in the AC side.
- For an angle φ=90º (only reactive power is transferred through the AC port), the strategies to produce the AC voltage unbalance Δv_{ac} shown in Fig. 10a and Fig. 10c are equivalent. For φ=0º (only active power is transferred through the AC port), the strategies shown in Fig. 10b and Fig. 10c are equivalent too.
- Unbalancing the magnitude of the AC voltage (27) (Fig. 10b) does not allow to transfer power from the cells when φ=90º. Unbalancing the real component of the AC voltage (28) (Fig. 10c) has the advantage of a nearly linear relationship between the level of unbalance and the power transferred by the cell.

Fig. 11 shows the power transferred by cells *1T* (same for *1B*), and the power at the DC and AC ports of the MMC, as a function of Δv_{dc} and Δv_{ac}, for constant apparent power S_{ac} (constant $|i_{ac}|$)

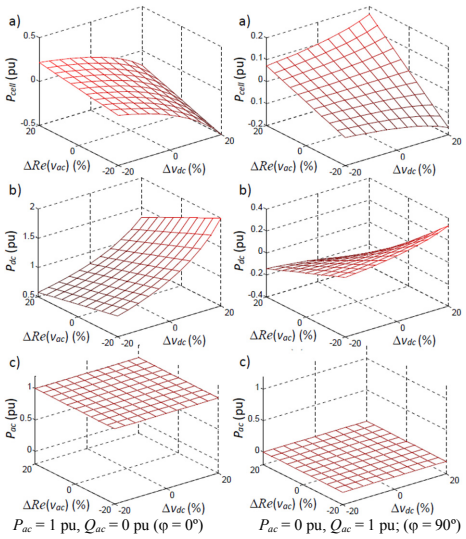


Fig. 11.- a) Cell power P_{cell}, b) DC port power P_{dc} and c) AC port power P_{ac}, as a function of $\Delta Re(v_{ac})$ and Δv_{dc}, for constant AC power S_{ac}. Left: Purely active power (φ = 0°); Right: Purely reactive power (φ = 90°) in the AC port. Powers are in pu of $|S_{ac}|$.

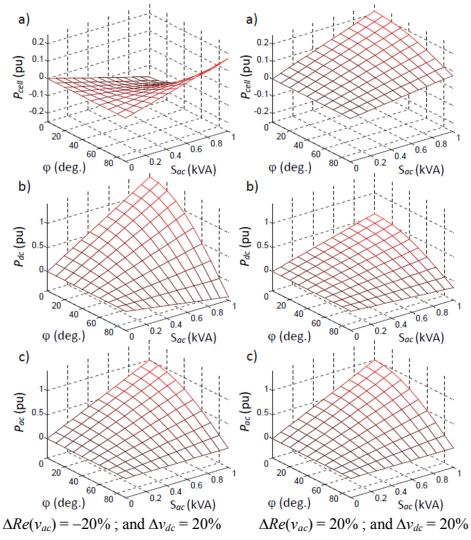


Fig. 12.- a) Cell power, b) MMC DC side power and c) MMC AC side power, as a function of apparent power S_{ac} and angle φ in the AC side, for two different unbalances $\Delta Re(v_{ac})$ and Δv_{dc}. Powers are in pu of $|S_{ac}|$.

and two different values of the angle φ. The strategy defined by (28) (Fig. 10c) was used, in which the real component of the cells AC voltage is varied, i.e. Δv_{ac}=$\Delta Re(v_{ac})$. Cells *2T* and *2B* do not transfer power (19). It is observed that for Δv_{dc} = $\Delta Re(v_{ac})$ = 0, P_{cell} = 0 and P_{dc} = P_{ac}, which corresponds to the normal operation of the MMCs. By controlling Δv_{dc} and Δv_{ac}, it is possible to change the amount of power transferred (injected or drained) by cells *1T* and *1B*. It is observed in Fig. 11-right that since P_{ac} = 0 (φ= 90°), all the power transferred by the cells goes to the DC port. In the case shown in Fig. 11-left, the power in the DC port adds to the power transferred by the cell to provide a constant power in the AC port. It is noted that in both cases, for constant Δv_{dc}, increasing $\Delta Re(v_{ac})$ increases the amount of power transferred by the cells. However, the effect of Δv_{dc} on the power transferred by the cells with constant $\Delta Re(v_{ac})$ varies with angle φ. This needs to be considered in the algorithms used to select Δv_{dc} and $\Delta Re(v_{ac})$.

Fig. 12 shows the power transferred by cell *1T* (same for *1B*), and the power at the DC and AC sides of the MMC, as a function of the apparent AC power (which is proportional to i_{ac}) and the angle φ in the AC side, for two different values of Δv_{dc} and Δv_{ac}. It is seen in Fig. 12b that independent of the voltage unbalance, no power is transferred by the cells when the apparent AC power is zero, i.e. $|i_{ac}|$ =0. For a given angle φ, the power transferred by cells *1T* and *1B* varies proportionally to S_{ac} (and therefore to $|i_{ac}|$). The variation of the power transferred by the cells with φ for constant S_{ac} is seen to change both with Δv_{dc} and Δv_{ac}.

It is concluded from the analysis presented in this subsection that the amount of power transferred (absorbed or delivered) by the cells which have power transfer capability, can be controlled by adequate selection of Δv_{dc} and Δv_{ac}. This is done without affecting to the power balance of cells which do not transfer power. This will require however the development of suitable control and modulation strategies. This is discussed in section V.

It is finally noted that in the preceding discussion the voltage drop in the arm inductors was not considered. As a result, the AC current i_{ac} equally splits between top and bottom arms. If the arm inductors are considered, then (25) does not necessary hold, i.e:

$$v_{ac1T} + v_{ac2T} \neq v_{ac1B} + v_{ac2B} \neq v_{ac} \qquad (31)$$

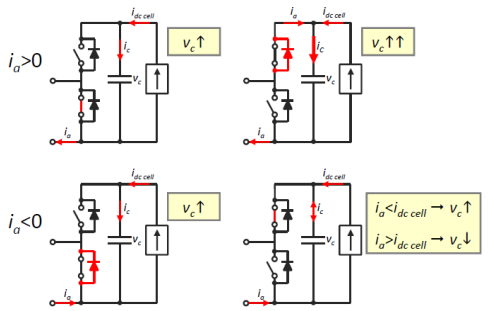
It is possible then to change how the current i_{ac} splits between the top and bottom arms. This would open new possibilities to produce asymmetries among the cells. Due to room limits, this case is not analyzed in this paper.

V. Modulation and Control Strategies

It has been shown that control of the power transferred by the cells is by achieved adequate selection of Δv_{dc} and Δv_{ac}. Two different methods to achieve this goal are discussed following. The first one uses a conventional control. In this case, the values for Δv_{dc} and Δv_{ac} to realize the power balance are the response of the balancing algorithms to the unbalance produced by the cells transferring power. No explicit commands for Δv_{dc} and Δv_{ac} are given. In the second method, explicit commands for Δv_{dc} and Δv_{ac} are given.

a) No explicit selection of Δv_{dc} *and* Δv_{ac}

Control of the MMC with cells transferring power can be realized combining the circulating current control with a sorting algorithm [14]. Power transferred by the cells naturally results



a) Bottom switch closed b) Top switch closed

Fig. 13.- Variation of the cell capacitor voltage v_c as a function of the switches state, arm current and cell current.

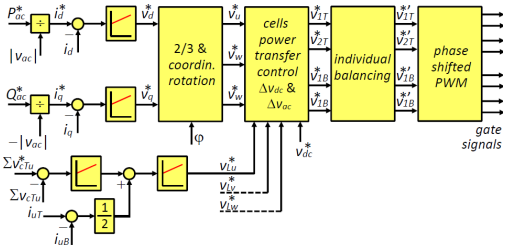


Fig. 14.- Implemented control. * stands for commanded values.

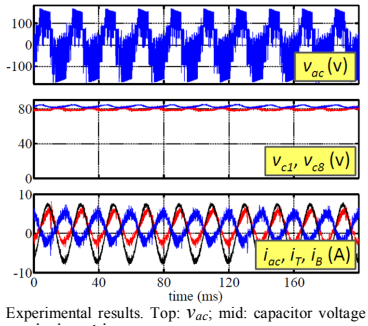


Fig. 15.- Experimental results. Top: v_{ac}; mid: capacitor voltage for cells 1&8, bottom: i_P, i_N and i_{ac} currents.

TABLE II: EXPERIMENTAL SETUP

MMC	Power switches	600V/23A
	Cell capacitor / Arm inductance	2000uF / 1mH
	Cell voltage / DC bus voltage	80 V / 320 V
	Sampling frequency	5 kHz
DAB	Input / output voltage	12 V / 50 V
	Switching frequency	100 kHz
	Turn ratio / Leakage inductance of the transformer	N=4 / L_k=5uH

in a decrease of the circulating current (i.e. i_{dc}) and consequently of the power being transferred from the DC port.

Regarding the cell capacitor voltage balancing, sorting algorithms will naturally select the cells transferring power if needed. Fig. 13 schematically shows the variation of the cell capacitor voltage v_c as a function of the switches state and of sign and magnitude of the arm current when a cell is transferring power. Assumed that the current source is injecting power (i.e. $i_{dc\ cell}$ >0), the cell capacitor voltage will decrease (v_c↓) only when the top switch is closed and $i_a > i_{dc\ cell}$. In all the other cases the capacitor voltage increases (v_c↑). The sorting algorithms will select the cells transferring accordingly. It is noted that in this case, no explicit values for Δv_{dc} and Δv_{ac} are given.

b) Explicit selection of of Δv_{dc} and Δv_{ac} commands

It is possible to control the amount of power injected by the cells with power transfer capability by explicitly selecting Δv_{dc} and Δv_{ac} (see Fig. 11 and Fig. 12). In this case, control of each individual cell voltage is needed. It is noted that conventional balancing algorithms based on sorting the capacitor voltages does not have this capability [3,4,12].

Fig. 14 shows a potential implementation. The desired active and reactive power in the AC side are the inputs to the control. The "*cells power transfer control*" block selects the voltage unbalance Δv_{dc} and Δv_{ac} needed to realize the power transfer. With this control strategy, the power in the AC side of the MMC is maintained constant, the power transferred by the cells therefore modifying the power in the DC side. The circulating current is controlled to balance the DC power, based on the total voltage in each arm. The individual voltage reference for each cell, which includes the desired unbalance, is then obtained. Individual capacitor voltage balancing is required, a phase-shifted carrier modulation strategy is needed for this purpose [9].

VI. EXPERIMENTAL RESULTS

Preliminary experimental verification of the proposed method has been realized on an eight cell single-phase MMC. Two cells, one in the top arm and one in the bottom arm, have DAB [20,21] connected to their capacitor, therefore having the capability of transferring power (Fig. 4c). The details for the MMC and the DAB can be found in Table II. The DAB realizes a bidirectional DC/DC conversion. It uses two active full bridges interfaced through a high-frequency transformer, which provides galvanic isolation. Soft-switching operation of all the devices at nominal conditions is possible. Two complementary signals with a 50% duty cycle were used to control each full bridge. The power flow is controlled by varying the phase-shift between these signals. Feedback control with a PI regulator was used to control the current injected to the cell by the DAB.

The control strategy described in Section V-a was used to control the MMC. Therefore, no explicit commands for Δv_{dc} and Δv_{ac} are given, instead they result from the reaction of the control and sorting algorithms to the power transferred by the cells. Fig. 15 shows various wave shapes during the normal operation of the MMC. Fig. 16 shows the DC component as well as the magnitude and phase of the AC (50 Hz) component of the cells voltage for the top arm, both for the case when the cells do not transfer power (conventional MMC) and when one cell per arm transfers power. Bottom arm behaves similarly. Two different cases of power transferred by the cells P_{cell} of 10% and 20% of the AC power P_{ac} are shown in Fig. 16a and Fig. 16b respectively. Fig. 16-right shows the power in the DC

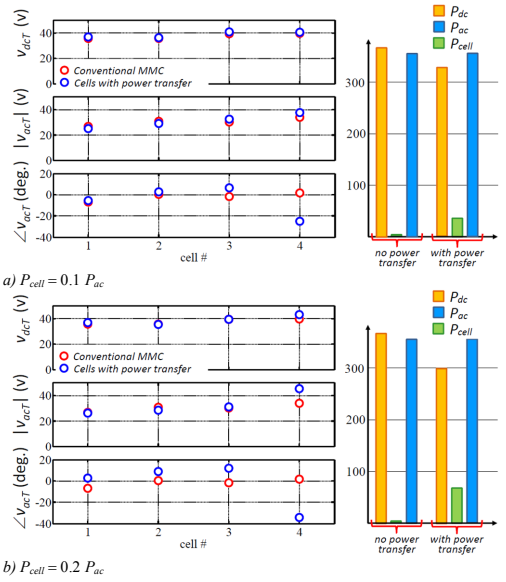


Fig. 16.- Experimental results. Left: DC and AC component of the cell voltage (only results for cells #1 to #4 shown); right: DC, AC and cells power without/with cell power transfer, for two different values of the power transferred by the cells. P_{ac} remains constant when the cells transfer power.

and AC sides of the MMC, as well as the power transferred by the cells. As already mentioned, the MMC is controlled to maintain constant the power in the AC side, meaning that power transferred by the cells affect to the DC side of the converter.

It is observed from Fig. 16a and 16b that the DC component of the cells voltage barely changes. Larger changes are observed in the magnitude of the AC voltage of cell #4 v_{ac4T}. However, the most noticeable changes in the cell voltage occur in the angle $\angle v_{ac4T}$. This would correspond to the case shown in Fig. 10a. It is noted that Δv_{dc} and Δv_{ac} are not explicitly given, the use of the strategy shown in Fig. 14 would allow to optimize their use. Implementation of this strategy is in progress.

VII. Conclusions

This paper analyzes the design and control of MMCs in which the cells have the capability to transfer (inject of absorb) power. The use of such cells provides to the MMC new functionalities, like distributed energy storage and connection of low-voltage/low power sources and loads at the cell level. The concept can also be used to realize different types of multiport power converters, including SSTs. Cell design, operational limits and control strategies have been presented and discussed. In the proposed cell design, a DAB has been used to transfer power providing galvanic isolation. It has been shown it is possible to control the amount of power injected by the cells by adequate selection of the cell DC and AC voltages. This can be realized using conventional control algorithms for the MMC. However, design of control algorithms to optimize the selection of Δv_{dc} and Δv_{ac} is desirable and is the focus of ongoing research. The proposed concepts have been confirmed experimentally.

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Comparative Analysis of Control and Modulation Strategies for Modular Multilevel Converters

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***Abstract*—Control of Modular Multilevel Converters (MMCs) is a challenging problem as multiple control objectives need to be satisfied simultaneously, including the generation of the desired output voltage, the control of the circulating current and the balancing of the cell capacitors. Though a number of control strategies have been proposed, an intuitive approach is often used for the design of the control structure. Furthermore, the performance of a specific control configuration can be significantly affected by issues like the modulation strategy, the modes of operation of the MMC and the sizing of the passive components. This paper presents a methodology for the analysis of the control and modulation strategies for MMCs, including the classification and assessment of the methods that have been reported in the literature.**

***Index Terms*—Modular Multilevel Converter, MMC, circulating current control, modulation strategies.**

I. INTRODUCTION

The increasing penetration of renewable energies as well as the demanding requirements in terms of efficiency and reliability for their integration in the power transmission system poses a big challenge, which is expected to increase in the near future, as a significant part of the installed capacity will be connected to the distribution levels [1]. Power electronics-based technologies, like HVDC (High Voltage Direct Current) and FACTS (Flexible AC Transmission System), able to provide functionalities to the power operator such as power flow control, reduction of transmission losses and power quality improvement, will be key for this purpose [2].

The MMC was proposed one decade ago [3]-[6]. It shares some appealing properties of other modular multilevel topologies, like reduced losses due to low switching frequencies and better output voltage wave shape, which leads to smaller filters and reduced voltage stress in the power devices. In addition, the MMC structure based on simple cells provides scalability to increase the voltage levels. Furthermore, while it provides a high voltage DC link, the distributed energy storage at the cells capacitors eliminates the need of a bulk DC capacitor, which is advantageous for safety and reliability reasons [7].

Despite of its advantages, control of MMC is a challenging task as multiple control objectives need to be satisfied simultaneously, including generation of the desired output voltage, control of the circulating current and balancing of the cell capacitors. Though a number of control strategies have been proposed, an intuitive approach is often used for the design and analysis of the control structure. Furthermore, the performance of a specific control configuration can be significantly affected by issues like the modulation strategy, the modes of operation of the MMC (e.g. constant AC voltage and frequency for the case of grid-connected MMC vs. variable voltage and frequency for the case of MMCs used in electric drives) and the sizing of the passive components (arm inductances and cell capacitors). It is interesting to note in this regard the large dispersion observed in the sizing of the passive elements for the experimental prototypes reported in the literature, making difficult to realize a fair comparison and assessment.

The primary goal of this paper is to propose a methodology for the analysis of MMC control strategies. Control and implementation issues to be considered are established first. Then, the methods that have been reported are systematically classified and analyzed. The same platform will be used for the assessment through simulation and experimental verification of the different methods. A fair comparative analysis is therefore possible.

The paper is organized as follows. A brief analysis of the MMC basic concepts, modeling and power balance is presented first. Discussion and classification of the circulating current control methods is addressed in Section III. Modulation strategies and capacitor voltage balancing methods are covered in Section IV. Section V addresses passive elements sizing. Simulation and experimental results are shown in Section VI, conclusions being presented in Section VII.

II. MMC MODEL AND POWER BALANCE

MMCs realize a bidirectional DC-AC power conversion. The AC side can be either single phase or three-phase (see Fig. 1). The physical cells forming each arm of the converter typically consist of a half bridge and a capacitor. For the three-phase case, each cell in Fig. 1-left physically corresponds to three individual cells. For the three-phase case, complex vector notation can be used to represent the AC variables, such as voltage (1) and current vectors (2).

$$v_{ac} = \frac{2}{3}(v_u + v_v e^{j2\pi/3} + v_w e^{j4\pi/3}) \tag{1}$$

$$i_{ac} = \frac{2}{3}(i_u + i_v e^{j2\pi/3} + i_w e^{j4\pi/3}) \tag{2}$$

The voltages inserted by the upper and lower cells are given by (3) and (4). The AC output voltage can be expressed as

This work was supported in part by the Research, Technological Development and Innovation Programs of the Spanish Ministries of Science and Innovation and of Economy and Competitiveness, under grants MICINN-10-CSD2009-00046 and MINECO-13-ENE2013-48727-C2-1-R, and by the European Commission FP7 Large Project NMP3-LA-2013-604057, under grant UE-14-SPEED-604057

(5), the voltage drop along the arm inductors being (6), with i_c standing for the circulating current. It is seen from (5) and (6) that v_L can be used to control the circulating current i_c without affecting to the output voltage v_{ac}. The powers for the upper and lower arms are given by (7) and (8), the combined and differential powers being (9) and (10) respectively.

$$v_T = \sum_{j=1}^{N} v_{nT} = \frac{v_{dc}}{2} - v_{ac} - \frac{v_L}{2} \tag{3}$$

$$v_B = \sum_{j=1}^{N} v_{nB} = \frac{v_{dc}}{2} + v_{ac} - \frac{v_L}{2} \tag{4}$$

$$v_{ac} = \frac{1}{2}(v_B - v_T) - \frac{L_{arm}}{2}\frac{di_{ac}}{dt} - \frac{R_{arm}}{2} i_{ac} \tag{5}$$

$$v_L = 2(L_{arm}\frac{di_c}{dt} + R_{arm} i_c) = v_{dc} - (v_B + v_T) \tag{6}$$

$$P_T = v_T \cdot i_T = \left(\frac{v_{dc}}{2} - v_{ac} - \frac{v_L}{2}\right) \cdot \left(i_c + \frac{i_{ac}}{2}\right) \tag{7}$$

$$P_B = v_B \cdot i_B = \left(\frac{v_{dc}}{2} + v_{ac} - \frac{v_L}{2}\right) \cdot \left(i_c - \frac{i_{ac}}{2}\right) \tag{8}$$

$$P_T + P_B = v_{dc} \cdot i_c - v_{ac} \cdot i_{ac} - v_L \cdot i_c \tag{9}$$

$$P_T - P_B = v_{dc} \cdot \frac{i_{ac}}{2} - 2 \cdot v_{ac} \cdot i_c - v_L \cdot \frac{i_{ac}}{2} \tag{10}$$

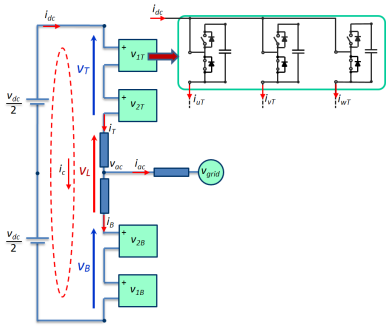

Fig. 1. Left - Schematic representation of a conventional MMC, with the cells consisting of a half bridge. Right - Corresponding cell circuit for the case of a three-phase MMC.

III. CIRCULATING CURRENT CONTROL STRATEGIES

The circulating current is one of the distinguishing features of the MMC. A number of strategies have been proposed for its control. Analysis and classification of the proposed methods is not trivial, as often the control of the circulating current is combined with the balancing and modulation strategies.

Fig. 2 shows a generic block diagram for the circulating current control loop (per phase) and the different mechanisms that can be used to obtain the reference value. Different control actions can be combined to obtain the final arm voltage. Switches S1 to S3 are used to indicate the actions that are selected, i.e. the control being used. The different strategies are discussed following, the brackets indicate the switches which are open (S=0) or closed (S=1).

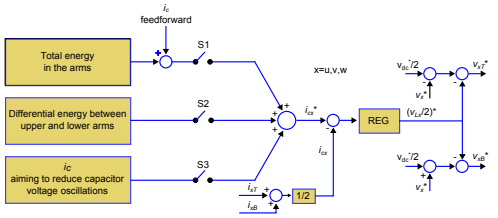

Fig. 2. Circulating current control loop (per phase), x stands for u,v or w .

A. No Circulating Current Control: Direct Modulation (S1=S2=S3=0)

In this strategy there is no explicit control of the circulating current. The converter produces the commanded output voltage, which may come from an outer current or power loop. A capacitor voltage balancing method is of course needed. Though simple, this method has remarkable drawbacks. The circulating current contains a large component at $2\omega_e$, increasing the losses in the arm inductances and power devices, also leading to large oscillations in the capacitor voltages. Moreover, the choice of the arm inductors and the cell capacitors can be critical due to potential resonance phenomena [8].

B. Suppression of the $2\omega_e$ Component of the Circulating Current (S1=S2=S3=0)

As for the direct modulation, the DC component of the circulating current is not explicitly controlled. However, a controller for the suppression of the $2\omega_e$ is included, thus eliminating the major drawback of the direct modulation.

C. Control of the DC Component of the Circulating Current: i_{cDC} (S1=1, S2=S3=0)

The combined arm power (9) reflects a power mismatch between the DC and AC sides. The last term in the right side of (9) can be neglected due to the small value of v_L. It is readily seen that the term $v_{ac} \cdot i_{ac}$ will produce two components in the arm power at DC and $2\omega_e$ respectively. The component at $2\omega_e$ will produce oscillations in the capacitor voltages, which can be acceptable. On the contrary, the DC component will produce an continuous increase/decrease of the capacitor voltage, which is obviously unacceptable. A DC circulating current i_c is then calculated and injected to make $v_{dc} \cdot i_c$ equal to the DC component of $v_{ac} \cdot i_{ac}$.

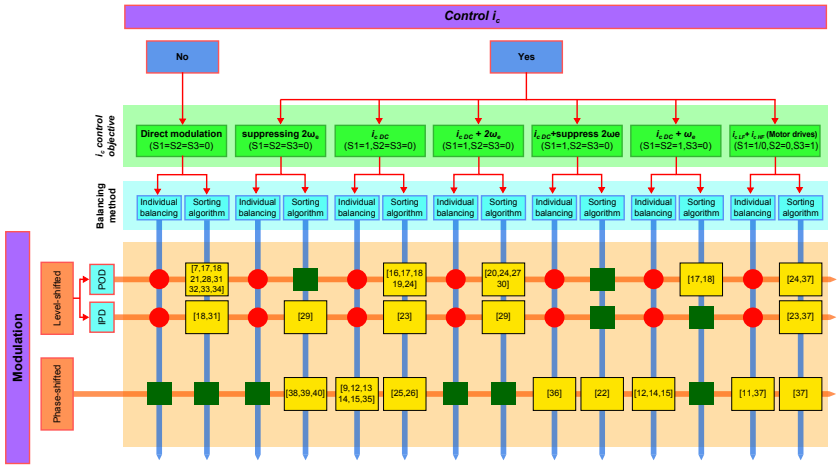

Fig. 3. Classification of the control and modulation methods for MMCs. References using *Phase shifted* modulation in this figure implement *Interleaved carriers* (see Table I)

D. Control of the DC and $2w_e$ Components of the Circulating Current: $i_{cDC} + 2\omega_e$ (S1=1, S2=S3=0)

Also derived from (9), the circulating current can be used not only to balance the average power but also to reduce the $2\omega_e$ components of the capacitor voltage. This is done by injecting a circulating current of the form given by (11).

$$i_c = \frac{v_{ac} \cdot i_{ac}}{v_{dc}} \tag{11}$$

E. Control of the DC Component and Suppression of the $2\omega_e$ Components of the Circulating Current (S1=1, S2=S3=0)

In this strategy, in addition to the control of the DC component of the circulating current, some type of current regulation strategy is implemented to cancel the $2w_e$ component of the circulating current. The goal of this strategy is to reduce the RMS value of the arm current, and therefore the losses in the arm inductors. However, this produces an increase of the $2\omega_e$ component of the capacitor voltage.

F. Control of the DC and w_e Components of the Circulating Current: $i_{cDC} + \omega_e$ (S1=S2=1, S3=0)

Small power imbalances (10) can occur during the normal operation of the power converter between the upper and lower cells. As such imbalance cannot be compensated either by the DC or the $2w_e$ components of the circulating current, a component at w_e in phase with the output voltage can be used for this purpose.

G. Circulating Current Control with High Frequency Circulating Current Injection (Motor Drives) (S1=1/0, S2=0, S3=1)

A relatively new field of research is the use of the MMCs for medium voltage electric drives. The operation of the motor at low speed worsen the oscillations of the capacitors voltages. Strategies that have been proposed to solve this problem include control of the low frequency components and the modulation at high frequency of the circulating current. By doing this, the power oscillations in the cells are shifted to a higher frequency, significantly reducing the impact on the cells capacitor voltage. The desired circulating current reference includes both low and high frequency components (S3 in Fig. 2), different options have been proposed to obtain this current reference (see references in Fig. 3).

Fig.3 shows a classification of the methods that have been described. Balancing and modulation strategies are also considered in Fig.3, being discussed in Section IV. Cells in green indicate configurations which are feasible but which to our best knowledge have not been reported in the literature. Cells in red indicate configurations which are unfeasible.

As a conclusion from the previous discussion, the direct modulation approach, though simple, leads to large $2\omega_e$ component of both circulating current (what implies increased losses in the arm inductances and power devices) and capacitor voltage (what can affect to the capacitors lifetime). Adding some type of circulating current control (especially the DC and $2\omega_e$ components) produces remarkable improvements, this

option being normally preferred.

IV. MODULATION STRATEGIES AND CAPACITOR VOLTAGE BALANCING METHODS

The primary goal of the modulation is to calculate the cells gate signals to obtain the desired output voltages. Table I summarizes the existing modulation strategies, N standing for the number of submodules per arm. The number of inserted cells determines the number of voltage levels applied to the arm inductors. In general, a reduced number of voltage levels leads to a decrease in the circulating current switching ripple. However, the number of levels in the output voltage is also reduced, therefore increasing its harmonic distortion.

The choice of a certain modulation strategy determines the capacitor voltage balancing method that can be implemented. Level-shifted strategies use carriers covering the whole voltage range and cannot therefore be applied with individual voltage balancing methods (based on individual cell control). On the contrary, phase-shifted strategies can be used with individual cell references, allowing the use of both balancing methods described below.

While the modulation strategy defines the number of submodules that must be inserted at any time, the voltage balancing method selects the specific cells that must be inserted/removed based on the capacitor voltages and the sign of the arm current. Two different methods have been proposed, they are discussed following. It is noted that the selection of the balancing strategy is conditioned in some cases by the modulation method (see Fig. 3).

A. Individual Capacitor Voltage Balancing at Each Cell

This approach was first proposed in [9], it uses an independent controller for each capacitor. Its implementation poses restrictions on the modulation method (see Fig. 3), as it cannot be used with level-shifted modulation methods.

B. Sorting Algorithm

The number of cells to be inserted in the upper and lower arms to obtain the desired output voltage are set by the modulation strategy. The fact that not all the cells need to be inserted normally leaves some freedom to select the cells to be included and therefore to balance the capacitor voltages. These algorithms sort the capacitor voltages and select the cells to be inserted based on the capacitor voltage needs and the direction of the arm currents. Sorting algorithms can be used in principle with any modulation strategy (see Fig. 3).

V. PASSIVE ELEMENTS SIZING

Selection of the cell capacitor and arm inductor has been seen to have a significant impact on the performance provided by different control methods, and should be considered in order to realize a fair comparison. Table II summarizes the values used in several experimental setups reported in the literature. A large dispersion in the sizing is observed.

Selection of the the arm inductors faces several goals: They are necessary to handle the voltage difference between the top and bottom side of the converter, and also help to limit the current in case of a DC-side short circuit. Also they can filter high-frequency harmonics in the circulating current. In the end, sizing of the arm inductors will be a trade-off between the filtering requirements (or circulating current control needs) and the short-circuit current limit [10].

TABLE II
ARM INDUCTANCES AND CELL CAPACITANCES REPORTED IN THE LITERATURE.

Arm inductance (H)	Cell Capacitance (mF)	Reference
$1e^{-3}$ (3.20%)	3	[9]
$1e^{-3}$ (4%)	3.3	[11]
$0.25e^{-3}$ (1.31%)	3.3	[12]
$0.75e^{-3}$ (4%)	6.6	[14][15]
$2e^{-3}$ (18.6%)	4.4	[23]
$3.1e^{-3}$ (10.4%)	3.3	[19][18]
$3.3e^{-3}$ (3.3%)	3.3	[16]
$4.74e^{-3}$ (7.4%)	5.6	[36]
$2e^{-3}$ (17.4%)	4.4	[24]
$3.6e^{-3}$ (22.6%)	3.6	[28]

Selection of the cell capacitors involves a trade-off between their size, cost and the voltage ripple [10]. For a given permissible peak-to-peak cell capacitor voltage ripple $\delta v_{cap,pp}$, Lesnicar and Marquardt have proposed (12) to determine the required capacitance C_{cell}, where P is the real power transferred, v_{cap} is the nominal capacitor voltage, m is the modulation index, and $cos\phi$ is the power factor [5].

$$C_{cell} = \frac{P}{3Nmv_{cap}\delta v_{cap,pp}\omega cos\phi}\left(1-(\frac{mcos\phi}{2})^2\right)^{\frac{3}{2}} \quad (12)$$

VI. SIMULATION AND EXPERIMENTAL RESULTS

Simulations as well as experimental verifications have been used to validate the analysis presented in the previous sections. Matlab/Simulink was used for simulation. Fig. 4 shows the magnitude of the $2\omega_e$ component of both the circulating current and a capacitor voltage for four different control strategies. It is readily observed the large magnitude of this harmonic for the Direct Modulation control strategy. By controlling the $2\omega_e$ component in the circulating current, this component as well as the oscillations of the capacitor voltage are significantly reduced. However, as expected, total suppression of the $2\omega_e$ component in the circulating current produces a slightly increase of the $2\omega_e$ component of the capacitor voltage.

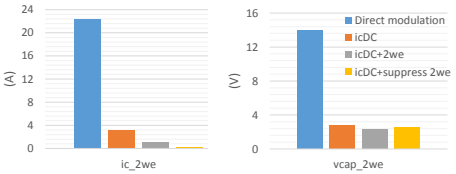

Fig. 4. Simulation results. $2\omega_e$ component of the circulating current (left) and capacitor voltage (right) for different control strategies.

Experimental verification of the different control methods has been realized on an eight cell, single-phase MMC (see Fig. 5). The details of the prototype are shown in Table III.

TABLE I
MODULATION STRATEGIES AND CARRIERS DISPOSITION.

Carriers Disposition	Output voltage levels	Inserted cells
Phase-shifted		
Evenly spaced carriers	N+1	N ($v_L = 0$) [N+1,N,N-1] ($v_L \neq 0$)
Interleaved carriers	2N+1	[N+1,N,N-1]($v_L = 0$) [N+2,N+1,N,N-1,N-2] ($v_L \neq 0$)
Level-shifted		
In-Phase-Disposition (IPD)	2N+1	[N+1,N,N-1] ($v_L = 0$) [N+2,N+1,N,N-1,N-2] ($v_L \neq 0$)
Phase-Opposite-Disposition (POD)	N+1	N ($v_L = 0$) [N+1,N,N-1] ($v_L \neq 0$)

TABLE III
EXPERIMENTAL SETUP

Power switches	600V/23A
Cell capacitor/Arm inductance	2000uF/1mH
Cell voltage/DC bus voltage	100V/400V
Switching frequency	5Khz

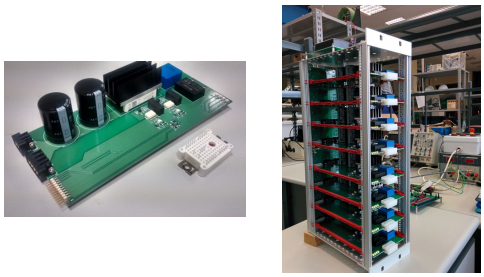

Fig. 5. Left: half bridge cell. Right: eight cells, single-phase, experimental MMC prototype.

Fig.6 shows experimental waveforms of top and bottom arm currents (i_T,i_B), and a capacitor voltage from top and bottom arms (v_{cap1}, v_{cap5}). Direct modulation was used for the results in Fig.6-a), the strategy $i_{cDC} + 2\omega_e$ (see Section III) being used for the results in Fig.6-b). It is readily observed the oscillations of both currents and voltages are significantly reduced by controlling the circulating current.

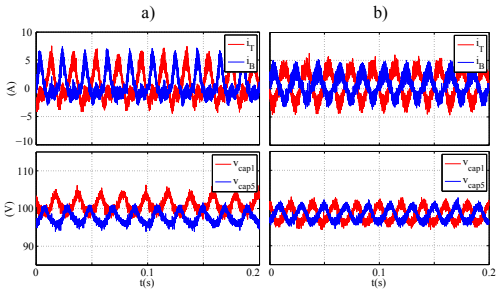

Fig. 6. Experimental results. Top, bottom arm currents i_T,i_B and capacitor voltages from top and bottom arms v_{cap1},v_{cap5} under two different control strategies. a) Direct modulation. b) $i_{cDC} + 2\omega_e$ (see Section III)

Fig. 7 shows the magnitude of the $2\omega_e$ component of the circulating current (i_c) and a capacitor voltage (v_{cap1}), for the same control strategies considered in Fig. 4. The magnitudes are shown in % of the worst case (i.e. direct modulation). Experimental verification confirms simulation results.

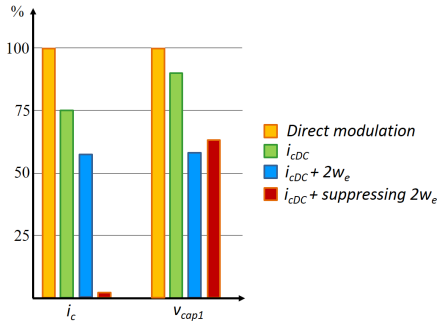

Fig. 7. Experimental results. Magnitude of the $2\omega_e$ component of circulating current i_c and a capacitor voltage v_{cap1}, for four different control strategies. Level-shifted POD modulation was used. The magnitudes are in % of the worst case (direct modulation)

VII. CONCLUSIONS

This paper addresses the classification and assessment of modulation and control strategies for MMCs. Classification of the existing methods is based on the circulating current control, modulation and capacitors voltage balancing strategies. The pros and cons for each method have been discussed. Criteria for the selection of the arm inductances and cell capacitance, as well as the impact on the performance of the MMC have also been addressed. Simulation and experimental results have been provided to support the analysis.

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Retos tecnológicos en el desarrollo de un transformador de estado sólido basado en un convertidor modular multinivel con inyección de potencia a nivel de celda

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***Abstract*— Uno de los pilares de las redes eléctricas inteligentes son los transformadores de estado sólido (SST, de sus siglas en ingles). La sustitución de transformadores clásicos por SSTs dota a la red de un gran número de funcionalidades adicionales. En este artículo se propone una posible topología para la implementación de un SST basado en un convertidor modular multicelda con inyección de potencia a nivel de celda. Se presentan los retos tecnológicos que supone el manejo de dispositivos semiconductores de potencia a elevadas tensiones y las necesidades de elevados aislamientos galvánicos.**

***Index Terms*—Transformador de Estado Solido (SST), Convertidor Modular Multicelda (MMC), Convertidor en Doble Puente Activo (DAB), alto aislamiento galvánico.**

I. INTRODUCCIÓN

ESTE artículo detalla los retos tecnológicos encontrados en el desarrollo de una nueva topología de transformador de estado sólido (SST, de sus siglas en ingles). Los transformadores electrónicos de potencia son elementos fundamentales en los sistemas de distribución de energía eléctrica. Los transformadores masivamente utilizados en la actualidad son componentes relativamente baratos y sobre todo fiables y basados en una tecnología sobradamente conocida. Sin embargo, tienen ciertas limitaciones como pueden ser su baja densidad de potencia (teniendo un elevado tamaño, peso y volumen para una potencia determinada), elevadas pérdidas a baja carga y la no existencia de una capacidad efectiva de reacción ante sobrecargas.

El uso de un SST es una novedosa alternativa al uso de transformadores clásicos (Fig. 1). En este caso, el uso de dispositivos electrónicos de potencia conmutando a una frecuencia más elevada permite una reducción del peso y del volumen gracias a la reducción del tamaño del núcleo magnético. Además, un SST puede implementar otras funcionalidades como pueden ser la capacidad de almacenamiento de energía, permitiendo compensar desbalances de potencia.

Resulta descabellado realizar una comparativa únicamente en términos de coste, rendimiento o robustez entre un SST y un transformador clásico, debido a que las posibilidades adicionales que el uso de un SST incorpora deberían ser tenidas en cuenta. El coste extra que supone el uso de un SST puede ser recompensado en determinadas aplicaciones en las que sus funcionalidades extra supongan un importante valor añadido.

De manera muy resumida, un SST está compuesto por un convertidor CA/CC, un convertidor CC/CC con aislamiento galvánico de alta frecuencia, un convertidor CC/CA (Fig. 1(b)) y una plataforma de control y comunicaciones. En general todos los convertidores deben permitir una transferencia bidireccional de la energía.

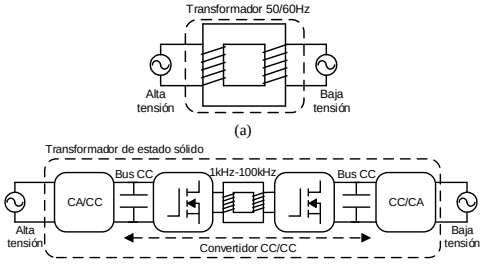

Fig. 1. (a) Esquema de un transformador clásico. (b) Esquema de un transformador de estado sólido (SST).

Existen diferentes topologías de convertidores de potencia propuestas para el desarrollo de SSTs [1]-[4]. En este artículo se propone el uso de un convertidor modular multinivel (MMC, de sus siglas en inglés) para realizar la conversión bidireccional de potencia desde la red de alterna de alta tensión a un bus de continua. Para la conversión CC/CC se propone el uso de un convertidor en doble puente activo (DAB, de sus siglas en inglés) [5]. Por último, para la conversión del bus de continua de baja tensión a una tensión de alterna, aunque se podría utilizar otro MMC, se propone el uso de un inversor (por sencillez, aprovechando la reducida tensión).

La gran ventaja del uso de un MMC, es la obtención de un bus de continua de alta tensión a través de buses distribuidos de menor tensión de continua. En el caso del convertidor CC/CC se propone la utilización de dispositivos de carburo de silicio (SiC) con el fin de reducir el tamaño (incrementando su frecuencia de conmutación) o las pérdidas del mismo [6]-[10].

II. Desarrollo de un SST utilizando una topología MMC

Al igual que otros convertidores modulares, el MMC permite reducir las pérdidas, gracias al uso de bajas frecuencias de conmutación, además de reducir los esfuerzos de tensión que deben soportar los semiconductores [10]-[13]. Además, su estructura basada en sencillas celdas posibilita una escalabilidad clave para permitir operar a elevadas tensiones utilizando dispositivos de potencia que deban soportar relativamente bajas tensiones. Una característica fundamental del MMC es el almacenamiento de la energía en cada celda de una manera distribuida, proporcionando un enlace de alta tensión de continua sin la necesidad de un voluminoso condensador conectado a este enlace, lo cual es una importante ventaja en términos de seguridad y fiabilidad del sistema [14].

El diseño convencional de un MMC realiza una conversión bidireccional de potencia entre corriente alterna y continua. En la Fig. 2 se presenta el esquema monofásico, aunque sería válido para un MMC trifásico. Cada una de las celdas de un MMC estará compuesta por un medio puente o un puente completo y un condensador. Por simplicidad nos centraremos en el caso monofásico y con únicamente dos celdas por brazo (cuatro celdas por fase), aunque todos los conceptos serían trasladables a un mayor número de celdas (el número depende de la tensión del bus de continua y la tensión de cada celda) y al caso trifásico (en el caso trifásico, habría tres fases conectadas al bus de continua).

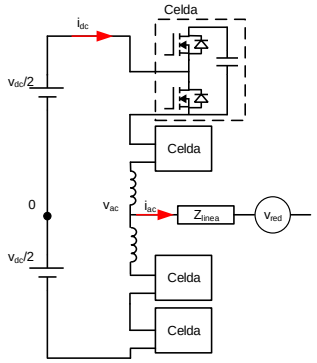

Fig. 2. Esquema de un MMC. Representación de una celda.

El objetivo principal de las estrategias de control y modulación de un MMC es doble. Por un lado balancear la transferencia de potencia entre los puertos de alterna y continua y por otro lado regular la tensión de cada uno de los condensadores de las celdas [15]-[20]. Debido a que el almacenamiento energético de los condensadores de cada celda es reducido, el balance de la potencia de cada celda es cero (despreciando las pérdidas) y por lo tanto la potencia en los puertos de alterna y continua debe ser igual.

La transferencia de potencia a nivel de celda del MMC proporciona nuevas capacidades, como puede ser el almacenamiento o la generación distribuida de energía. Obviamente, la inyección de potencia a nivel de celda implica cambios en el diseño de las celdas y en la estrategia de control del MMC. En el caso del diseño de las celdas, en función de las características de la fuente de energía será necesario la incorporación de un convertidor de potencia que podrá ser unidireccional o bidireccional. Con respecto al control, previamente se ha considerado que en un MMC el balance energético neto en una celda es cero. Sin embargo, este supuesto es falso en el caso de inyección de energía a nivel de celda [21].

La funcionalidad de inyección o absorción de energía a nivel de celda es la clave fundamental para el uso de un MMC en el desarrollo propuesto de un SST. Dos redes de distribución de corriente alterna de alta tensión podrían ser interconectadas usando dos MMCs interconectados a nivel de celda por un convertidor CC/CC bidireccional (Fig. 3).

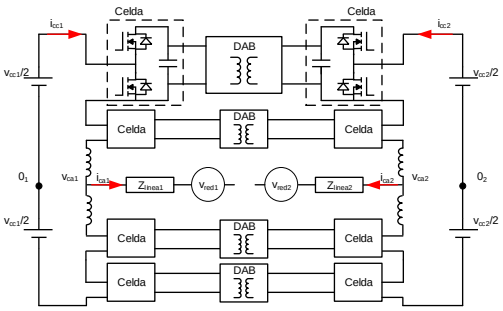

Fig. 3. Esquema de un SST compuesto por dos MMC interconectados a nivel de celda por DABs.

En la aplicación concreta que se analiza en este artículo, una de las redes trifásicas de alterna es de alta tensión (13,8kV/60Hz) mientras que la red a la que se debe interconectar es de baja tensión (480V/60Hz). Para implementar la conversión CC/CA en esta red de baja tensión el uso de un MMC no se considera necesario, por lo que se propone la conexión en paralelo de los buses distribuidos de continua y la conversión a alterna a través de un sencillo inversor, como se muestra esquemáticamente en la Fig. 4. Como se observa en la Fig. 4, considerando un flujo de potencia dirigido desde la red de alta tensión a la de baja, la tensión de salida del convertidor CC/CC queda directamente determinada por la tensión de la red de alterna de baja tensión, sin embargo la tensión de entrada del mismo, quedará determinada por la tensión de la celda del MMC, que a su vez queda determinada por el número de celdas del mismo.

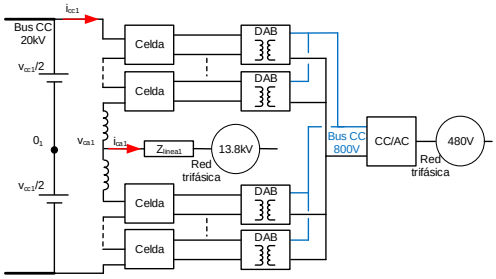

Fig. 4. Esquema de un SST compuesto por un MMC para la red de distribución de alta tensión, DABs a nivel de celda proporcionando el aislamiento y un inversor para la red de baja tensión.

III. Dificultades ligadas al mantenimiento de aislamiento en un convertidor modular

La operación de convertidores operando a elevadas tensiones supone importantes dificultades. Gracias al funcionamiento del MMC, los semiconductores de potencia tanto de cada celda del mismo como del convertidor CC/CC no deben soportar toda la tensión del bus de continua. No obstante, existe una dificultad añadida inherente al funcionamiento a alta tensión que es mantener el necesario aislamiento, tanto entre las celdas del MMC de distintos niveles, como entre el primario y el secundario del convertidor DAB. Este aislamiento deberá soportar toda la tensión del bus.

A. *Tensiones de alimentación auxiliares aisladas*

Cada una de las celdas que componen el MMC será controlada a través de una unidad de control central. Las señales de control serán transferidas a cada celda a través de fibra óptica para mantener el aislamiento. Además cada celda necesita al menos una tensión auxiliar, para alimentar sistemas de control, como sensores y drivers. Por supuesto, esta tensión auxiliar deberá estar aislada entre las distintas celdas. Además, aunque la tensión de cada celda no es demasiado elevada, ya que la tensión del bus se divide entre el número de celdas, si la tensión auxiliar de cada celda se obtiene de una misma fuente de tensión externa centralizada, cada una de estas tensiones deberá mantener un aislamiento de, al menos la tensión de bus (20kV). Lamentablemente, no es común encontrar convertidores para fuentes auxiliares (de baja tensión y baja potencia) comerciales con aislamientos mayores de 10kV. Por lo tanto, la posibilidad de usar una fuente de tensión centralizada a partir de la cual se obtengan las tensiones auxiliares aisladas para cada celda se desvanece por la dificultad de encontrar convertidores comerciales con aislamientos superiores a los 10kV. Habitualmente, los convertidores con aislamiento reforzado cumplen la tercera edición del estándar IEC/EN 60601-1, que exige un aislamiento de al menos 4kV [22], [23].

Una alternativa para la obtención de tensiones auxiliares para cada celda sin necesidad de un aislamiento tan elevado, es el aprovechamiento de la energía de la propia celda (Fig. 5). Como se ha comentado previamente uno de los objetivos del convertidor MMC es regular la tensión del condensador de cada celda. Por lo tanto, la energía almacenada en este condensador se puede utilizar para obtener una tensión auxiliar que alimente a los sistemas de control de la propia celda. En este caso, el convertidor a utilizar para obtener una tensión auxiliar desde la tensión del condensador de la celda no necesita aislamiento. Sin embargo, necesita realizar una elevada reducción de tensión desde la tensión de la celda (alrededor de 1000V) hasta la tensión auxiliar, que debe ser segura (en torno a los 24V). Una dificultad añadida es que la tensión del condensador no será absolutamente constante. Por un lado, tendrá un pequeño rizado, que no tiene demasiada influencia, pero por otro lado, cuando en el arranque la celda no esté controlada, la tensión del condensador puede ser la mitad de la tensión regulada de la celda (cuando el MMC esté controlado), por lo que el rango de tensión de entrada del convertidor debe ser muy amplio (para el caso de una celda de 1000V, su rango de tensión de entrada debe ser, al menos, desde 500V a 1000V). Aunque el convertidor auxiliar necesario tiene unas especificaciones complejas, su adquisición comercial es más sencilla y económica, al menos para una tensión de celda de alrededor de 1000V.

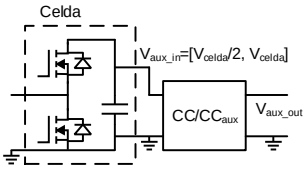

Fig. 5. Esquema de obtención de la tensión auxiliar a través de la energía del condensador de cada celda.

Las tensiones auxiliares obtenidas a partir del condensador de cada celda serán utilizadas también para alimentar los circuitos de control del convertidor CC/CC bidireccional que interconecta las dos redes de distribución.

B. *Aislamiento del transformador del DAB*

Una de las mayores dificultades en el desarrollo del SST, será el diseño del transformador que aporte aislamiento galvánico de al menos 24kV$_{cc}$. Para ello se ha optado por una configuración de devanados separados en un núcleo en UU. El devanado primario se arrolla en uno de los brazos del núcleo magnético y el devanado secundario en otro. Otras configuraciones implican mayor complejidad constructiva y en muchos casos refrigeración forzada con agua [24], [25]. El principal problema de separar los devanados es el incremento de la inductancia de dispersión, lo que en el DAB puede llegar a implicar un límite en la potencia a transferir.

Para estimar la inductancia de dispersión de distintos diseños se han utilizado dos diferentes métodos: usando cálculo por elementos finitos (más preciso, aunque más lento) o mediante las ecuaciones que definen dicha inductancia (menos preciso, pero más rápido y aporta una valoración del peso de distintos parámetros de diseño en el valor de la dispersión).

Se ha desarrollado el modelo matemático que predice la inductancia de dispersión para distintos diseños, siguiendo [26] y [27]. Una vez verificado que el diseño cumple con los

valores deseados de inductancia de dispersión, se procede a su verificación a través del cálculo por elementos finitos. A continuación, se muestran algunas de las ecuaciones obtenidas que se consideran de mayor relevancia:

$$L_{CU\_1} = 2\pi\mu_o h \int_{r_{cu1}}^{r_{cu1}+l_{cu1}} \rho \cdot \left[\frac{N_1 \cdot (\rho - r_{cu1})}{l_{cu1} \cdot (h + 2 \cdot \rho)}\right]^2 \cdot d\rho \quad (1)$$

$$L_a = \mu_o h \int_0^{2\pi} \int_{r_{cu1}+l_{cu1}}^{5 \cdot lm} \rho \cdot \left[\frac{N_1 \cdot (1 - k_{cu\_2}(\rho,\theta))}{(h + 2 \cdot \rho)}\right]^2 \cdot d\rho \cdot d\theta \quad (2)$$

donde L_{cu_1} y L_a son las inductancias ligadas a los flujos dispersos a través del devanado primario y a través de la zona más allá de este devanado (con las que se puede estimar la inductancia de dispersión). Para este último espacio se debe tener en cuenta que existen zonas afectadas por el segundo devanado y zonas donde este devanado no está presente y, por tanto, no afecta. Esto se ha tenido en cuenta mediante el factor corrector $k_{cu\_2}(\rho, \theta)$. Asimismo, h es la altura de los devanados, r_{cu_1} el radio interior del devanado primario, l_{cu_1} el ancho de dicho devanado, N_1 es el número de vueltas del devanado primario, l_m es la longitud entre ambos brazos magnéticos y $k_{cu\_2}(\rho, \theta)$ es:

$$k_{cu_2}(\rho,\theta) = \frac{r_{cu2} + l_{cu2} - \left|\sqrt{l_m^2 + \rho^2 - 2 \cdot \rho \cdot l_m \cdot \cos(\theta)}\right|}{l_{cu2}} \quad (3)$$

donde r_{cu2} es el radio interior del devanado secundario y l_{cu2} es su grosor.

La Tabla I muestra varios posibles diseños de transformador. En color verde se indican aquellas configuraciones que tienen una inductancia de dispersión lo suficientemente baja como poder transferir la potencia deseada y en color rojo aquellas en las que la inductancia de dispersión es demasiado elevada. Como se puede apreciar, el grado de acercamiento entre los resultados obtenidos mediante la simulación 2D obtenida usando PEmag (del programa PExprt de Ansys) es bastante aproximada a los resultados obtenidos con las ecuaciones matemáticas del modelo.

Siguiendo el proceso de diseño previamente comentado, se ha construido un transformador en un núcleo UU93 con material N87 cumpliendo las siguientes especificaciones: tensión de entrada de 1000V, relación de transformación 1, potencia máxima de 10kW y una frecuencia de conmutación de 50kHz (primera fila de la Tabla I). En la Fig. 6 se muestran los valores medidos de inductancia de dispersión (L_k=260uH) y magnetizante (L_{mag}=3600uH), mientras que en la Fig. 7 se muestra una foto, donde se puede observar que se ha utilizado como material de aislamiento el aire y kapton, y los resultados del ensayo de aislamiento (hasta 30kV).

Actualmente se está analizando una configuración de devanados partidos donde la mitad del primario y la mitad del secundario se devanan alrededor de un brazo magnético (cada uno en su propio carrete para asegurar el aislamiento galvánico) y la otra mitad de primario y secundario se devanan en el otro brazo magnético según la misma condición. De esta forma, la inductancia de dispersión puede reducirse ostensiblemente a cambio de perder muy poco porcentaje del área de ventana y sin incrementar la complejidad constructiva del transformador.

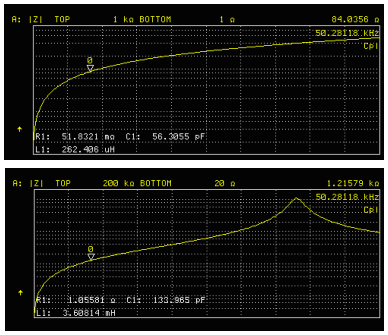

Fig. 6. Medida experimental de la inductancia de dispersión y magnetizante del transformador construido.

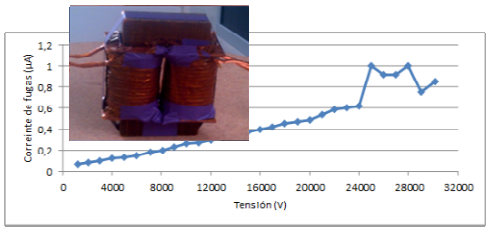

Fig. 7. Fotografía y resultado del ensayo de aislamiento del transformador.

C. Uso de dispositivos de elevado ancho de banda prohibida de alta tensión

La frecuencia de conmutación de las celdas del MMC no determinará de manera clave el tamaño de la misma, por lo que ésta puede ser suficientemente baja como para que el uso de IGBTs no suponga un gran porcentaje de pérdidas. Sin embargo, el tamaño del convertidor CC/CC bidireccional, en concreto un DAB, vendrá fuertemente determinado por la frecuencia de conmutación, por lo que su incremento provocará una deseable reducción, sobre todo, en el tamaño de los magnéticos.

Para permitir un incremento de la frecuencia de

TABLA I
PRINCIPALES CARACTERÍSTICAS DE ALGUNOS DISEÑOS POSIBLES PARA EL TRANSFORMADOR MAGNÉTICO.

Potencia (kW)	V_{dev} (V)	Frecuencia (kHz)	Núcleo	Material	Aislamiento	N	Llk (uH) Estimada	Lmag (uH) Estimada	Llk (uH) Estimada Pmag	Lmag (uH) Estimada Pmag	Llk (uH) Necesaria
10	1000	50	U93	N87	Aire+Kapton	30	159,2	5322	139	7321	230
5	1000	50	U93	N87	Aire+Kapton	60	636,0	21290	500	25741	455
5	1000	50	U93	N87	Aire+Kapton	50	442,0	14780	341	17875	455
10	1000	25	U93	N87	Resina (ER2183)	71	885,0	30700	799	35125	455
10	1000	25	U93	N87	Resina (ER2183)	50	439,0	14780	425	17928	455

conmutación sin penalizar en exceso el incremento de las pérdidas de los semiconductores se propone la implementación del DAB utilizando dispositivos de SiC.

Los nuevos dispositivos electrónicos de potencia basados en semiconductores de banda prohibida ancha tienen unas características excepcionales para convertirse en el centro de atención de la electrónica de potencia de los próximos años [6]-[8]. Las características más relevantes del SiC son su elevado campo de ruptura, ocho veces mayor que en el Silicio (Si) y su conductividad térmica, tres veces mayor. Estas características proveen a los dispositivos de potencia basados en SiC alta capacidad de bloqueo de la tensión, baja caída de tensión en estado de conducción, alta velocidad de conmutación y baja resistencia térmica. Todas estas propiedades permitirán diseñar convertidores conmutados de alta potencia, alta tensión y alta frecuencia.

Actualmente, es posible la obtención comercial de MOSFETs de SiC de Rohm (Japón) y Cree (EEUU). Otros fabricantes pueden suministrar muestras, pero no de manera comercial abierta. Ambos fabricantes no recomiendan considerar los MOSFETS de SiC como un recambio directo de MOSFETs de alta tensión de silicio. Se recomienda, por tanto, el uso de drivers particulares para cada dispositivo y diversos autores han presentado distintas soluciones [28]-[34]. Siguiendo las recomendaciones del fabricante, se diseña y construye un *driver* específico para estos MOSFETs de SiC. Este *driver* aplica una tensión V_{GS}=20V en el encendido para compensar la modesta transconductancia de estos dispositivos mientras que en el apagado V_{GS}=-5V para evitar encender el dispositivo de manera indeseada o realizar apagados parciales. En la Fig. 8 se muestra el diagrama del driver.

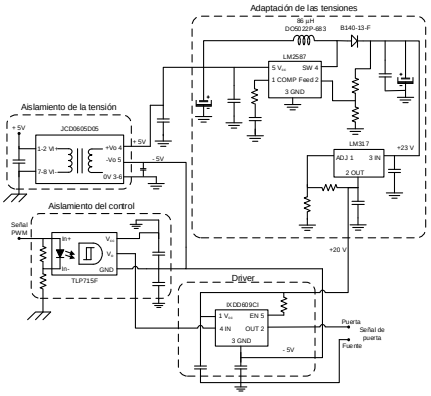

Fig. 8. Esquema del driver desarrollado para el control del MOSFETs de SiC.

Las máximas tensiones de ruptura que pueden soportar los actuales MOSFETs comerciales de SiC son 1200V y 1700V. Esta limitación de la tensión de ruptura máxima determina el máximo de la tensión de la celda del MMC, que será la tensión que deban soportar los semiconductores del DAB (y del MMC). La potencia máxima a manejar por el DAB se fija en 10kW por limitaciones en el tamaño de los componentes magnéticos. Considerando estas premisas se presentan las especificaciones del DAB en la Tabla II. Teniendo en cuenta el elevado aislamiento que debe proporcionar el transformador y su consecuente configuración, es importante determinar el valor de inductancia de dispersión que se necesita para transferir la potencia máxima, que viene determinada por:

$$P = \frac{(1-d)dTv_i v_o}{nL_k} \rightarrow L_k = \frac{(1-d_{max})d_{max}Tv_i v_o}{nP_{max}} \quad (4)$$

siendo d_{max} el desfase máximo, T el semiperiodo de conmutación, v_i la tensión de entrada, v_o la de salida, n la relación de transformación del transformador y P_{max} la potencia máxima [35].

Si el transformador tuviera una inductancia de dispersión mayor que la obtenida con (4) y determinada en la Tabla II, el DAB no podría transferir la potencia máxima deseada.

TABLA II
PRINCIPALES ESPECIFICACIONES DEL DAB

Tensión de entrada / salida:	1000V / 1000V
Potencia máxima:	10kW
Frecuencia de conmutación:	50kHz
Relación de transformación del trafo:	1:1
Aislamiento:	24kV
Inductancia de dispersión:	L_k = 230µH
Corriente máxima por los MOSFETs:	15.4A

En la Tabla III se presentan las características principales de dos alternativas de MOSFETs de SiC que compondrán el DAB. Se ha descartado el uso de semiconductores que soporten 1700V por su no idoneidad a nivel de corrientes máximas. Como se puede observar las capacidades parásitas de los MOSFETs de SiC son relativamente bajas para dispositivos de alta tensión. Estos MOSFETs de SiC también serán los semiconductores de las celdas del MMC, aunque en este caso se mantendrá una baja frecuencia de conmutación, reduciendo las pérdidas de conmutación.

TABLA III
PRINCIPALES CARACTERÍSTICAS DE LOS MOSFETS DE SIC BAJO ANÁLISIS

	SiC MOSFET (C2M0080120D)		SiC MOSFET (C2M0040120D)	
Fabricante	Cree		Cree	
V_{DS_max} (V)	1200		1200	
I_{D_max} (A)	36		60	
R_{DSon_max} (mΩ)	80		40	
V_{GS_op}/V_{GS_th} (V)	+20, -5 / 3		+20, -5 / 2.8	
Ciss (pF)	950	@	1893	@
Coss (pF)	80	V_{DS}=1000V	150	V_{DS}=1000V
Crss (pF)	7.6	f=1MHz	10	f=1MHz

IV. CONCLUSIONES

El desarrollo de un SST basado en el uso de una topología MMC con inyección de energía a nivel de celda mediante el uso de DABs supone un importante reto, tanto desde el punto de vista topológico y de control, como desde el punto de vista constructivo, donde existen importantes limitaciones en los dispositivos comerciales utilizados comúnmente.

Para realizar la interconexión de dos redes de alta tensión es importante mantener un elevado grado aislamiento entre las mismas, lo que dificulta el diseño y construcción de un transformador de alta frecuencia que proporcione el deseado aislamiento galvánico. Se han propuesto distintos diseños,

obteniendo resultados analíticos cercanos a la realidad, lo que permite estimar la idoneidad de los diseños para unas especificaciones concretas.

El uso de dispositivos de SiC, cada vez más extendido en los sistemas de alimentación, permite una reducción de las pérdidas y del tamaño de los convertidores. No obstante, su incorporación exige diseñar circuitería de control adecuada.

En este artículo se mencionan los retos tecnológicos detectados en la fase inicial de un proyecto de construcción de un SST. Se proponen las soluciones que se han adoptado y los resultados que se han obtenido por el momento.

AGRADECIMIENTOS

Este trabajo ha sido financiado en parte por la Unión Europea en el contexto de "Large Scale Integrating Collaborative Research Project" del 7º Programa Marco a través del proyecto SPEED FP7-NMP3-LA-2013-604057, por el Ministerio de Economía a través de proyecto Consolider RUE CSD2009-00046, el proyecto MINECO-13-ENE2013-48727-C2-1-R y el proyecto DPI2013-47176-C2-2-R y por el Gobierno del Principado de Asturias a través del proyecto FC-15-GRUPIN14-143 y los fondos FEDER.

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MMC based SST

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***Abstract* — The Modular Multilevel Converter (MMC) is a type of DC-AC electronic power converter suitable for HVDC applications, thanks to its modularity and to the symmetrical design of the cells. Cells in conventional MMCs use a capacitor in the DC link, meaning that the net power balance of the cell needs to be equal to zero. It is possible however to modify the cells of the MMC to provide the capability to transfer (inject or drain) power. The use of such cells opens several new functionalities and uses for the MMC. Cells with power transfer capability can be used to connect the medium/high voltage DC and AC ports intrinsic to the MMC, with low voltage DC/AC ports, the power transfer among ports being realized at the cell level. This results in multiport power converters, potential applications including solid state transformers (SST). This paper analyzes the design and control of multiport power converters based on MMC topologies, including their use as a SST. Topologies, control strategies and implementation issues will be covered.**

Keywords— Modular Multilevel Converter, MMC, Multiport Power Converters, Medium Frequency Transformer, Solid State Transformer, SST

I. Introduction

Transformers are key elements in power distribution systems. Classical transformers are a relatively cheap, reliable and well established technology. However, they suffer from several limitations, including low power density (large weight /volume for a certain power) and increased losses at light load. Also, they have an increased sensitivity to harmonics and imbalances.

Solid state transformers (SSTs), also called smart transformers, are an alternative to classical transformers. SSTs use fast-switching power devices to reduce significantly the volume/weight need for the core material. Moreover, SSTs can provide additional functionalities like harmonics, reactive power and imbalances compensation. Consequently, comparison of classical transformer and SST solutions cannot be performed only in terms of price and robustness, additional functionalities provided by SST also need to be considered.

Several topologies have been proposed for the practical realization of the SST [1]-[3]. Criteria for the classification of the existing solutions can include the number of stages (transformations of the electric power format), or whether the power flow can be unidirectional or bidirectional. In all the cases, the SST should connect two AC (normally three-phase) systems and provide galvanic isolation.

This work was supported in part by the Research, Technological Development and Innovation Programs of the Spanish Ministries of Science and Innovation and of Economy and Competitiveness, under grants MICINN- 10-CSD2009-00046 and ENE2013-48727-C2-1-R, and by the European Commission FP7 Large Project NMP3-LA-2013-604057, under grant UE-14-SPEED-604057

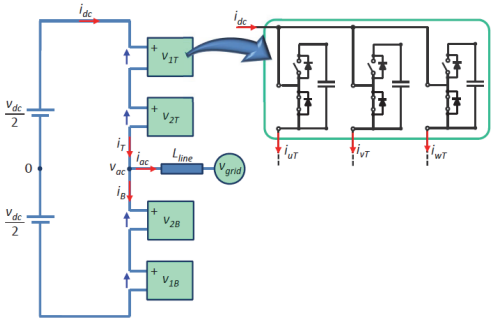


Fig. 1.- Left - Schematic representation of a conventional MMC, with the cells consisting of a half bridge For the sake of clarity, the arm inductances are not shown. Right – Cells using half-bridges for the case of a three-phase MMC.

The Modular Multilevel Converter is a DC/AC electronic power converter that was proposed one decade ago [4]-[6]. The AC port of the MMC can be single-phase or three-phase. All the analysis and discussion in this paper assumes a three-phase AC system. The MMC owns several appealing properties of other modular topologies. Its structure based on simple cells provides scalability, which is key to achieve high voltage levels using relatively low voltage power devices. Losses are significantly reduced due to the low switching frequencies of the individual cells. Also, its modularity results in good output voltage wave shapes, enabling the reduction of the filters as well as of the voltage stress in the power devices [4]-[6]. A distinguishing characteristic of the MMC is that while it provides a high voltage DC link, no bulk DC capacitor is needed. The energy storage is distributed at the cells capacitors. This is advantageous for safety and reliability reasons [7].

Fig. 1 shows the schematic representation of a three-phase MMC. The physical cells forming each arm of the power converter typically consist of a half bridge and a capacitor. Therefore, each cell in Fig. 1-left physically corresponds to three individual cells (Fig. 1-right). Control and modulation strategies developed for MMC are aimed to balance the power transfer between the AC and DC ports, which is done controlling the circulating current [8]-[10], as well as to balance the cell capacitor voltages [10]-[12].

Because the cells of the MMC have a limited energy storage capability, the net power balance for each cell is zero (neglecting losses), the power at the AC and DC sides of the MMC being therefore equal to each other. It is possible to modify the MMC to transfer power at the cell level. This would provide the MMC new potential capabilities, including distributed storage [13]-[15]; integration of distributed energy

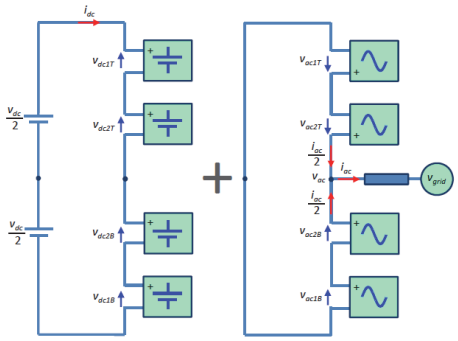


Fig. 2.- DC (left) and AC (right) sub-circuits of the MMC

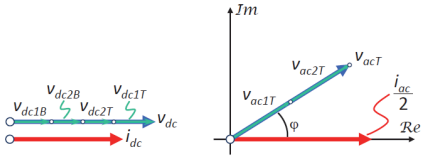


Fig. 3.- DC (left) and AC (right) voltages and currents. Only AC variables for the top arm are shown, they are the same for the bottom arm (see Fig. 2).

resources (DER) at the cell level [16]-[18]; multiport power converters [19]. It is also possible to combine the medium/high voltage DC and AC ports of the MMC with low voltage DC and AC ports. Furthermore, multiport power converters based on the MMC topologies could provide the desired functionalities of the SST, i.e. connection of two AC systems providing galvanic isolation and full control of the power flow, but enhanced with the availability of a high voltage DC link, which is intrinsic to the MMC. However, such modification involves changes both in the cells design as well as in the control strategy [19].

This paper analyzes the design, operation and control of MMCs modified to operate as multiport power converters, including SST. The paper is organized as follows. The model of the conventional MMC is presented in Section II. Design and operation of cells with power transfer capability is discussed in Section III. Multiport power converters based on the MMC, including SSTs, are discussed in Section IV. Control strategies are discussed in Section V. Simulation and experimental results are presented in section VI and VII respectively. Section VIII summarizes the conclusions.

II. Model and Operation of the MMC

The MMC realizes a bidirectional DC-AC power conversion (see Fig. 1). For the discussion following, complex vector notation will be used to represent the AC variables. The voltage and current vectors in the AC port of the MMC are defined by (1) and (2). The resulting top and bottom arm currents are shown in (3), the circulating current i_c being (4), whose DC component is equal to the DC current. Harmonics of the circulating current used e.g. to reduce the oscillations of the cell capacitor voltage [11],[10],[20], are not considered in the analysis following.

$$i_{ac} = \frac{2}{3}\left(i_u + i_v\, e^{j2\pi/3} + i_w\, e^{j4\pi/3}\right) \quad (1)$$

$$v_{ac} = \frac{2}{3}\left(v_u + v_v\, e^{j2\pi/3} + v_w\, e^{j4\pi/3}\right) \quad (2)$$

$$i_T = i_{dc} + \frac{i_{ac}}{2}\ ;\ i_B = i_{dc} - \frac{i_{ac}}{2} \quad (3)$$

$$i_c = \frac{i_T + i_B}{2} = i_{dc} \quad (4)$$

Due to the limited energy storage capability of the cells, the power in the DC port of the MMC has to be equal to the active power in the AC port (5), with * standing for complex conjugate.

$$P_{dc} = v_{dc}\, i_{dc} = P_{ac} = Re\,(v_{ac}\, i_{ac}^*) \quad (5)$$

It is useful to separate the MMC in Fig. 1 into its DC and AC sub-circuits, as shown in Fig. 2. A MMC with two cells per arm (N=2), i.e. Four cells per phase, will be considered as an example for the discussion following. If the MMC is perfectly balanced (identical cells, identical operating point), the cell DC and AC voltages are (6) and (7) respectively, the overall cell voltage being (8). Since the upper and lower arms are connected in parallel, the overall AC voltage needs to be equal to v_{ac}, (see Fig. 2-right). Consequently, the AC current splits equally between the upper and lower arms, all the cells having the same DC and AC powers (9) and (10). It is noted that for the sake of simplicity, the voltage drop in the arm inductor has been neglected in the preceding discussion.

$$v_{dc1T} = v_{dc2T} = v_{dc1B} = v_{dc2B} = \frac{v_{dc}}{2N} = \frac{v_{dc}}{4} \quad (6)$$

$$v_{ac1T} = v_{ac2T} = v_{ac1B} = v_{ac2B} = \frac{v_{ac}}{N} = \frac{v_{ac}}{2} \quad (7)$$

$$v_{nX} = v_{acnX} + v_{dcnX} \quad \text{with } n = 1, 2 \text{ and } X = T, B \quad (8)$$

$$P_{dcnT} = P_{dcnB} = \frac{v_{dc}}{2N}\, i_{dc} = \frac{v_{dc}}{4}\, i_{dc} \quad ; n = 1, 2 \quad (9)$$

$$P_{acnT} = P_{acnB} = Re\left(\frac{v_{acT}}{N}\ \frac{i_{ac}^*}{2}\right) = Re\left(\frac{v_{acT}}{2}\ \frac{i_{ac}^*}{2}\right) ; n = 1, 2 \quad (10)$$

Fig. 3 graphically shows the DC and AC voltages for the MMC in Fig. 1 and 2. For the AC complex vectors, the real axis real is defined to be aligned with the AC current, φ being the angle between the AC current and voltage vectors. If the voltage at the DC side of the MMC v_{dc} is maintained constant, the MMC control will adjust the DC current i_{dc} to balance the power between the DC and AC ports (5). In addition, the cell capacitor voltages must be kept at their target value. This is done by the balancing algorithms [8],[10],[11].

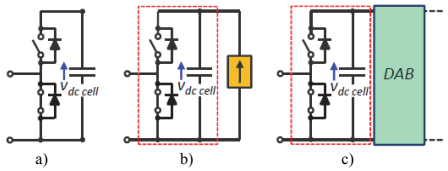


Fig. 4. a) Conventional cell with a capacitor in the DC link; b) cell with power transfer capability using a current source; c) cell using a DAB.

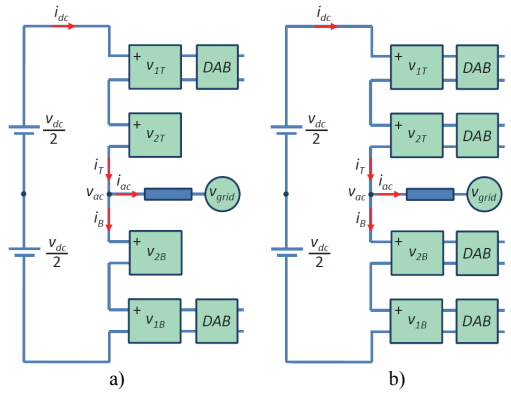


Fig.5.- MMC including cells with power transfer capability. a) MMC in which the same number of cells in the top and bottom arms transfer power; b) MMC in which all the cells transfer power.

III. Cells with Power Transfer Capability

Standard MMC cells have a capacitor in their DC link (see Fig. 1 and Fig. 4a), meaning that the net power balance has to be equal to zero. However, it is possible to provide the MMCs the capability to transfer power at the cell level [19]. Assumed that the cells are controlled to have a constant capacitor voltage of $v_{dc\ cell}$, transferring power to the standard cell design in Fig. 4a can be modeled as a current source connected in parallel to the cell capacitor, as shown in Fig. 4b. In a practical implementation, voltage isolation between the cell capacitor and the power source might be needed, a current controlled dual active bridge (DAB) can be used for this purpose (Fig. 4c) [2],[19],[21],[22].

If one or more cells transfer power, the resulting MMC power balance equation is (11), where P_{cell} is the power transferred by each cell and M is the number of cells transferring power. It is assumed that all the cells transfer a similar amount of power.

$$P_{dc} + MP_{cell} = P_{ac} \tag{11}$$

Two major cases can be considered for the case in which there are cells with the capability to transfer power: 1) only some cells of the MMC have that capability, and 2) all the cells of the MMC have this capability. These two cases are schematically represented in Fig. 5a and Fig. 5b respectively.

The case shown in Fig. 5a in which only some cells transfer power, will result in asymmetries in the mode of operation of the cells. Consequently, cells in the same arm will have different AC and/or DC voltages, depending on whether they transfer power or not. This produces significant differences with respect to the normal operation of the MMC, where all the cells have (ideally) the same DC and AC voltages (switching harmonics neglected). Modification of the control strategy can be required in this case, as conventional control strategies assume that all the cells operate identically. Furthermore, the fact that not all the cells inject power, will place limitations on how the power injected by the cells can be split between the AC and DC ports of the MMC. Detailed discussion of this can be found in [19].

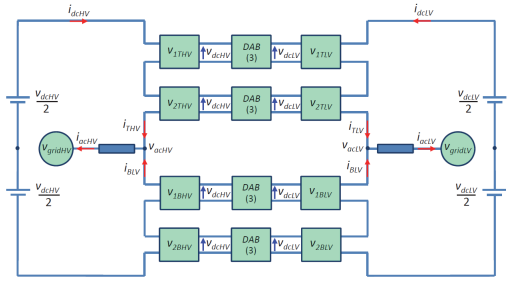
In the case shown in Fig. 5b, all the cells operate in the same working conditions, provided that they transfer a similar amount of power. Due to this, control of the MMC is significantly simpler compared to the case in Fig. 5a. This case is analyzed in detail in the next sections, as will be the base of the proposed multiport power converter topology.

IV. Multiport Topologies Based on the MMC

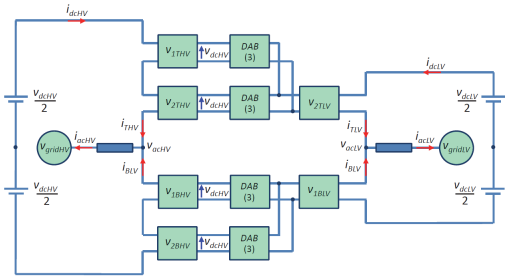
Providing the cells of the MMC the capability to transfer power opens several opportunities to realize multiport power converters. Examples of these are shown in Fig. 6a-c. In all the configurations shown in this figure, the left-side of the power converter corresponds to an MMC AC and DC ports, and will be considered as the high-voltage (HV) side. For simplicity, the MMCs in the figure use two cells per arm (N=2). However, all the discussion following can be extended to any value of N without any loss of generality. In all the cases, the isolation between the high voltage (HV) and low voltage (LV) AC ports is realized by DABs. It is also observed that in all the implementations, each cell of the MMC is connected to a DAB, meaning that the modularity of the MMC is extended to the isolation stage formed by the DABs. The right side of the power converter in Fig. 6a-c will be considered as the LV side. It is seen that the differences among the topologies shown in Fig. 6 only affect to the LV side.

The configuration shown in Fig. 6a corresponds to two MMC connected through the cells capacitors and the DABs. It provides two AC ports and two DC ports (HV and LV), with the same number of voltage levels in both AC ports. Since the number of cells is the same in both sides, the transformation HV-to-LV between the primary and the secondary has to be realized by the DABs. Consequently, the DAB are not symmetrical. The left (HV) side of the power converter will require high voltage-low current power devices, while the cells in the right (LV) side would use low voltage-high current power devices.

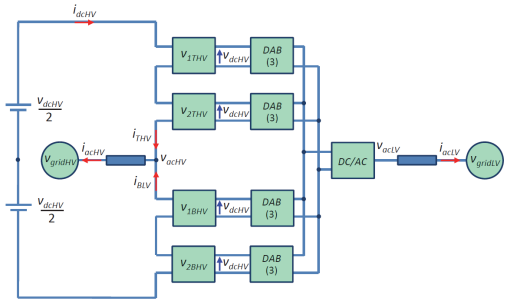
The configuration shown in Fig. 6b also corresponds to two MMC connected through the cells capacitors and the DABs. Therefore, it also provides two AC ports and two DC ports. However, in this case the DABs in each arm of the HV side are serialized, while there is some level of parallelization in the LV side. As a consequence, the number of cells (and thus the number of voltage levels) in the HV and LV sides are different. With this configuration, the transformation HV-to-LV



a) Cell-to-cell connected MMCs with symmetric primary and secondary (serialized input-serialized output)



b) Cell-to-cell connected MMCs with serialized input-parallelized output



c) Multiport power converter with and MMC in the HV side and a conventional AC/DC power converter in the LV side

Fig. 6. Different configurations of MMC based multiport power converters

between the primary and the secondary does not have to be realized only by the DABs, but can also be achieved by the effect of the serialization/ parallelization of the DBAs in the HV/LV sides respectively. This means that power devices with the same or close voltage ratings can be used now for the HV and LV sides.

Finally, in the configuration shown in Fig. 6c, all the DABs in each leg are connected in parallel in the LV side. As a consequence, a conventional DC/AC power converter can be used now (e.g. Two level or multilevel NPC, FC, …). In this configuration, the transformation HV-to-LV between the primary and the secondary can be entirely obtained by the effect of the serialization/parallelization of the DBAs in the

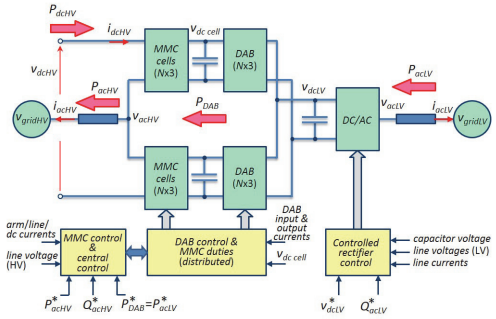


Fig. 7. Schematic representation of the control of the multiport power converter. Variables with "*" indicate commanded values. Variables without "*" indicate measured signals needed used by the control.

HV/LV sides. Thus, the DABs could now be symmetric, with a ratio 1:1 between the primary and the secondary. This would allow to use the same power devices in both sides.

It is important to note that Fig. 6c shows explicitly three ports: HV-DC, HV-AC, and LV-AC. Though a LV-DC port also exists, it is not shown in the figure, as it will not be considered in the discussion following. This means that the power transferred by the DABs needs to be equal to the active power of the AC port in the LV side (losses neglected). Control and behavior of the topology shown in Fig. 6c is discussed in the following sections.

V. Control Strategies

This section addresses the control for the multiport power converter shown in Fig. 6c. The power balance equation is given by (12). If losses are neglected, the power transferred by the DAB will be equal to the active power of the DC/AC power converter in the LV side (13).

$$P_{acLV} + P_{dc} = P_{acHV} \tag{12}$$

$$P_{DAB} = P_{acLV} \tag{13}$$

In the discussion following, it is assumed that the power transferred by the DAB (and consequently P_{acLV}) and the active power in the HV AC port P_{acHV} are the commanded values. Consequently, the power in the DC port of the MMC P_{dc} needs to be adapted by the MMC control to realize the power balance. This is done by controlling the circulating current.

Fig. 7 shows a potential implementation of the control. It is seen to consist of three major blocks:

- MMC control
- DAB control
- Controlled rectifier (DC/AC converter in the LV side) control

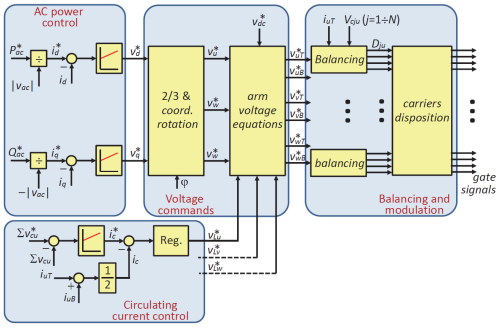


Fig. 8. Control of the MMC.

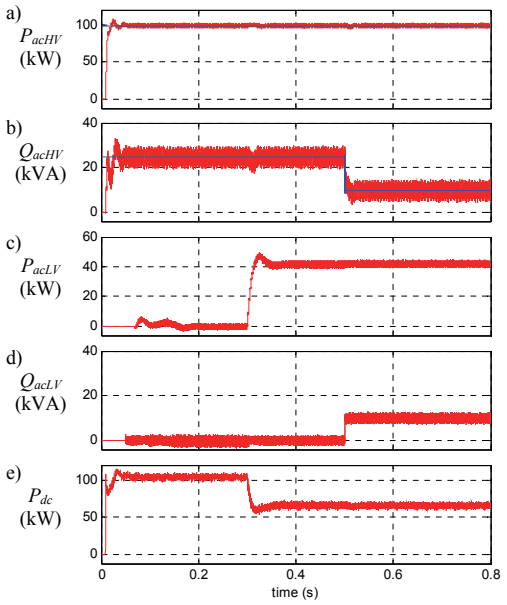


Fig. 9. Simulation results. Active and reactive power at the different stages of the power coverter. a) active power in the HV AC side, b) reactive power in the HV AC side, c) actrive power in the LV AC side, d) reactive power in the LV AC side, e) power in the DC link of the MMC

MMC control: The MMC control implements the normal functionalities for this type of power converter [10]. Multiple control objectives need to be satisfied simultaneously, a potential control strategy being shown in Fig. 8:

- d and q-axis current references for the HV AC side are obtained from the active and reactive power commands. Synchronous PI current regulators are used to obtain the required d and q-axis voltage commands.
- In order to guarantee the power balance between the DC and AC ports, the energy stored in the arm capacitors –and therefore the capacitors voltage– must remain constant. The circulating current command is obtained from the errors in the overall cell capacitors voltage, a PI controller being used for this purpose. The voltage applied to the arm inductors is used to control the circulating current.
- Once the voltage commands for the upper and lower arms are obtained, balancing of the cell capacitors voltages is required. A sorting algorithm is implemented in Fig. 8 [4]-[6]. In this strategy, the cells to be inserted are selected based on the capacitors voltage needs and the direction of the arm currents.
- Finally, gate signals are obtained by means of a level-shifted PWM modulation.

In the prototype under construction, the control of the MMC is distributed between a master control unit based on a Zynq SoC (System on a chip) by Xilinx, and several slave control units based on FPGAs. Details on the implementation of the control can be found in [23].

DAB control: The DABs operate as current sources. Each DAB includes a low cost FPGA, their control being therefore distributed. It is noted that the DABs do not control their input and output voltages. This is done by the MMC through the control of the cell capacitors $v_{dc\ cell}$, and by the controlled rectifier, which controls the capacitor voltage in the low voltage DC link $v_{dc\ LV}$. It is also noted that though the DABs receive a current command, this directly corresponds to a power command, provided that the input and output voltages are maintained at their target values. The current commands are the same for all the DABs, they are sent by the central control via optic fiber.

AC/DC converter control: The AC/DC power converter in the low voltage side is controlled as a conventional controlled rectifier. The commanded values are the DC link voltage and the reactive power. The active power is internally controlled to maintain the DC link capacitor $v_{dc\ LV}$ at its target value. The control is implemented on a DSP. The reactive power command is received from the central control.

The signals that need to be measured by each control block are also shown in Fig. 7. It is noted that for the MMC control, the DC current, AC currents and arm currents can be needed for different control purposes. Since these currents are not independent variables, there are different options for the placement of the current sensors. Measuring the top and bottom arm currents is sufficient in principle to estimate the other currents. However, redundant sensors are often used to improve the accuracy and reliability.

VI. Simulation Results

The operation of power converter topology shown in Fig 7 has been simulated using Matlab/Simulink. Fig. 9 shows the behavior of the system in different modes of operation. The MMC is enabled at t=10 ms, with, the active and reactive power commands being 100 kW (Fig. 9a) and 25 kVAr (Fig. 9b) respectively. Initially the DABs are not transferring power. Therefore, the power in the DC link of the MMC (Fig. 9e) matches the AC power plus the converter losses. At t=70 ms

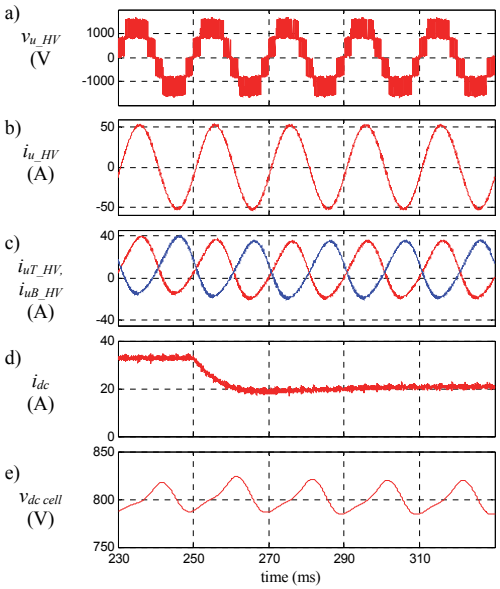


Fig. 10. Simulation results. Voltages and curresnts at different stages of the MMC. a) phase *u* voltage, b) phase *u* currant, c) currents in the top and bottom arms of phase *u*, d) dc current, e) capacitor voltage in one cell of the MMC.

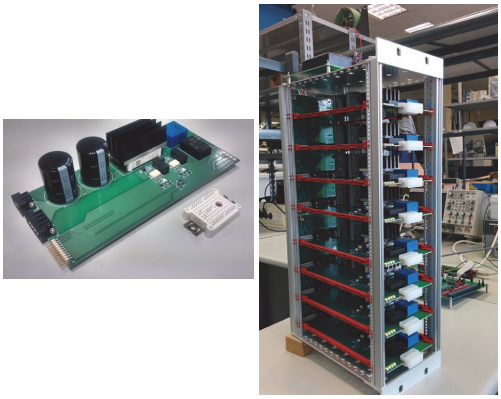


Fig. 11. Experimental prototype. Left – MMC cell.; right – MMC leg consisting of eight cells, inserted in the rack.

the controlled rectifier in the LV side of Fig. 7 is enabled (Fig. 9c). However, initially it will not transfer active power, since the DABs are not transferring power either. The reactive power command for the controlled rectifier in the LV side is also set initially to zero (Fig. 9d). In *t*=0.3 s, the DABs are commanded to transfer a total amount of 40 kW. This power is supplied by the controlled rectifier in the LV side (Fig. 9d).

TABLE I: EXPERIMENTAL SETUP

MMC	Power switches	600V/23A
	Cell capacitor / Arm inductance	2000uF / 1mH
	Cell voltage / DC bus voltage	80 V / 320 V
	Sampling frequency	5 kHz
DAB	Input / output voltage	12 V / 50 V
	Switching frequency	100 kHz
	Turn ratio / Leakage inductance of the transformer	N=4 / L_k=5uH

It is also observed from Fig. 9e that the power supplied by the DC bus of the MMC is decreased in the same amount, as needed to maintain the power balance. As discussed in the preceding section, only the AC active power in the HV side of the MMC and the power transferred by the DABs are commanded. The active power for the controlled rectifier and the power in the DC link of the MMC are adapted by the corresponding controls (see Fig. 7) to maintain the power balance. As already mentioned, the reactive power in the HV side (Fig. 9b) and LV side (Fig. 9d) are controlled independently, the only restriction coming from the current ratings of the power devices and passive elements of each power converter.

Fig. 10 shows a closer view of the voltages and currents at different stages of the MMC during the transient in Fig. 9 occurring at t=0.3 s. It is observed that the phase voltages and currents in the AC port of the MMC do not change, as the AC power in the HV side remains constant during the transient. Injection of power from the LV side through the controller rectifier and the DABs results in a decrease of the DC current of the MMC (Fig. 10d), and consequently of the DC component of the top and bottom arm currents of the MMC (Fig. 10c). Finally, Fig. 10e shows the capacitor voltage of one cell of the MMC. The ripple due to the oscillations of the phase power of the MMC are readily visible. The balancing algorithm implemented in the MMC control maintains these oscillations within admissible limits, not having any adverse effect on the MMC response.

VII. EXPERIMENTAL RESULTS

The experimental setup needed for the implementation of the proposed concepts is under construction. Preliminary results are shown in this section.

The MMC prototype consists of eight cells (N=4). Fig. 11-left shows one cell of the MMC. Fig. 11-right shows one leg of the MMC. The cells are seen to be inserted in a rack, the connectors both for the control signals as well for the power (cell DC link) being located in a back-plane.

Currently, one leg of the MMC and two DAB have been built and are operative. This means that a topology of the type shown in Fig. 5a, but for the case of single phase MMC, can be experimentally tested. The other two legs of the MMC have also been built. However, development and construction of the final version of the DABs is not complete yet. They are expected to be operative in a few months. The implementation of the control is as described in Section V.

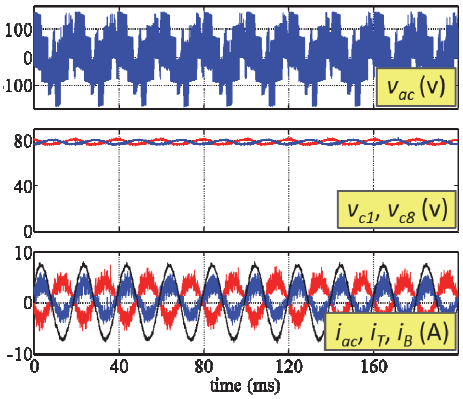


Fig. 12.- Experimental results. Top: v_{ac}; mid: capacitor voltage for cells 1&8, bottom: i_P, i_N and i_{ac} currents.

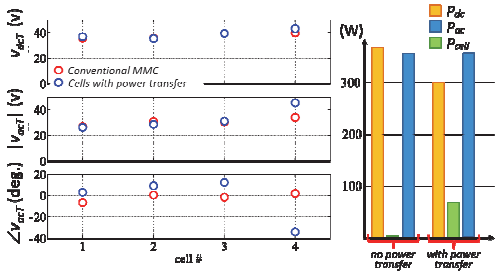
The details of the MMC and the DABs can be found in Table II. The DABs realize a bidirectional DC/DC conversion. It uses two active full bridges interfaced through a high-frequency transformer, which provides galvanic isolation. Soft-switching operation of all the devices at nominal conditions is possible. Two complementary signals with a 50% duty cycle were used to control each full bridge. The power flow is controlled by varying the phase-shift between these signals. Feedback control with a PI regulator was used to control the current injected to the cell by the DABs [21],[22].

Fig. 12 shows an example of the normal operation of the MMC, i.e. without power transfer.

Fig. 13-left shows the DC component as well as the magnitude and phase of the AC (50 Hz) component of the cells voltage for the top arm, both for the case when the cells do not transfer power (conventional MMC) and when one cell per arm transfers power. Bottom arm behaves similarly, and is not shown. The power transferred by the cells P_{cell} is 20% of the AC power P_{ac}. Fig. 13-right shows the power in the DC and AC sides of the MMC, as well as the power transferred by the cells. The MMC is controlled to maintain constant the power in the AC side, meaning that power transferred by the cells is reflected in the power in the DC side of the converter.

VIII. Conclusions

Multiport power converters based on MMC topologies have been proposed and analyzed in this paper. The proposed concept can connect high voltage and low voltage DC ports and AC ports, providing therefore the functionalities of a solid state transformer. Isolation is provided by DABs through a modular structure. Control strategies have also been discussed. Simulation results as well as preliminary experimental results confirming the viability of the proposed concepts have been provided.



b) $P_{cell} = 0.2\ P_{ac}$

Fig. 13.- Experimental results. Left: DC and AC component of the cell voltage (only results for cells #1 to #4 shown); right: DC, AC and cells power without/with cell power transfer, for two different values of the power transferred by the cells. P_{ac} remains constant when the cells transfer power.

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Design and Implementation of the Control of an MMC-Based Solid State Transformer

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***Abstract*— Implementation of the control of a Solid State Transformer (SST) is described in this paper. The SST topology considered is derived from a Modular Multilevel Converter (MMC), in which the cells have the capability to transfer (inject or drain) power. The MMC is combined with an isolation stage formed by Dual Active Bridges (DABs) and a DC/AC power converter. The resulting modular multiport power converter can connect both high voltage and low voltage AC and DC ports, providing isolation between the high voltage and the low voltage terminals, and with full control of the power flow. Implementation of the control of this power converter is not trivial, due to the large amount of power devices and sensors involved, and to the complexity of the control algorithms. Furthermore, the need to provide isolation among the different stages adds further concerns mainly related with cost. This paper discusses the configuration, selection of the required hardware, as well as implementation aspects for the control of the proposed SST topology.**

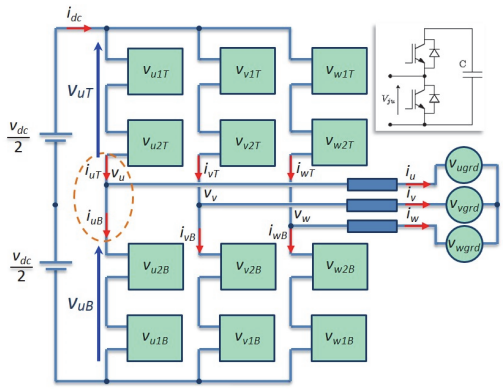
Keywords—Solid State Transformer (SST), Modular Multilevel Converter (MMC), centralized control, distributed control, FPGA

I. INTRODUCTION

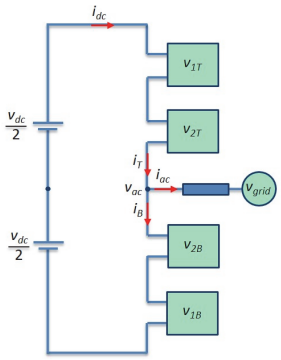
Industrialized countries have turned their energy policies towards a reduction of the dependence on fossil resources due to environmental concerns, limited resources and the uncertain and progressive increase of their cost. Massive integration of renewable as well as maximum efficiency have become a priority. This scenario has pushed the development of innovative solutions based on high-power, high-voltage electronics power converters, like HVDC (High Voltage Direct Current), FACTS (Flexible AC Transmission Systems) and SST (Solid State Transformer), able to cope with these challenges [1].

Conventional transformers represent a key element in the power transmission system. Although it is a relatively cheap and well stablished technology, power system operation is demanding innovative and challenging new requirements, such as power quality improvements (i.e harmonics, reactive power and imbalances compensation), power flow control and a reduction of transmission losses, among others. Solid State Transformers based on power electronics devices, have the potential to manage these new functionalities, while fulfilling its main objective: connecting two AC systems providing galvanic isolation [2].

This work was supported in part by the Research, Technological Development and Innovation Programs of the Spanish Ministries of Science and Innovation and of Economy and Competitiveness, under grants MICINN- 10-CSD2009-00046, ENE2013-48727-C2-1-R, DPI2013-47176-C2-2-R and by the European Commission FP7 Large Project NMP3-LA-2013-604057, under grant UE-14-SPEED-604057



a) Three-phase MMC



b) Complex vector equivalent circuit

Fig. 1. a) Three-phase MMC, with the cells consisting of a half bridge. b) Complex vector equivalent cirtuit. For the sake of clarity, the arm inductances are not shown.

The Modular Multilevel Converter (MMC) is a promising DC/AC multilevel power converter topology subject of extensive research nowadays. It was first introduced one decade ago [3],[4]. Fig. 1a shows the schematic representation of a three-phase MMC. The physical cells forming each arm of the power converter typically consist of a half bridge and a capacitor. While it shares the advantages of conventional multilevel topologies (i.e. reduced size of filters, lower switching

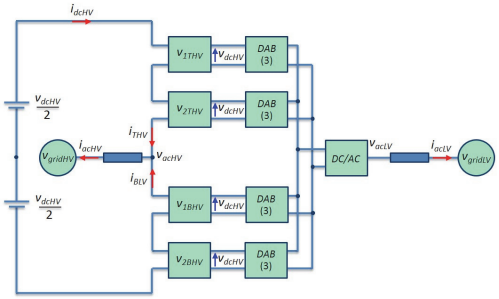


Fig. 2. MMC based multiport power converter MMC with serialized input-parallelized output.

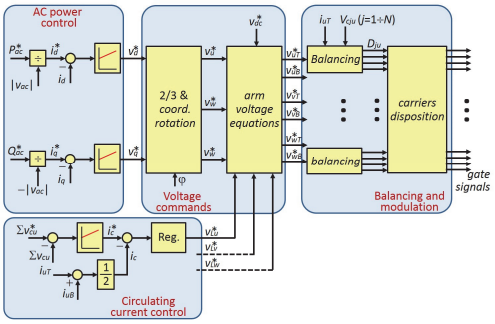


Fig. 3. Control of the MMC.

losses, capability of withstanding large terminal voltages using relatively lower voltage power devices), it also provides some attractive features such as modularity, easy scalability and distributed energy storage, therefore eliminating the need of a bulk DC capacitor [3],[4].

The MMC in Fig. 1a explicitly shows the three phases. It is possible to use a complex vector notation to represent the AC quantities (voltages and currents) of the MMC. The equivalent MMC with complex vector cells is shown in Fig. 1b [11].

It is possible to modify the MMC to transfer power at the cell level, providing new potential features such as distributed energy storage [5],[6],[7], integration of distributed energy resources at the cell level [8],[9],[10] and multiport power converters combining the high/low voltage AC/DC ports. Furthermore, multiport power converters based on the MMC topologies could provide the desired functionalities of the SST, i.e. connection of two AC systems, including galvanic isolation and full control of the power flow [11],[12] (see Fig.2). However, construction and control of the MMC based SST places significant challenges, due to the large number of power devices and sensors involved [22]. Either centralized or distributed control strategies can be used, each having advantages and disadvantages. Selection of a suitable implementation requires a thorough evaluation of the computational requirements and hardware requirements (number of input/outputs, optical fiber requirements for isolation, analog to digital channels, communications, …), as well as the existing digital control devices that can be used to realize the control.

This paper addresses the selection and implementation of the digital control of a MMC based SST, which is characterized by a large number of power devices and sensors, and large computational requirements due to the complexity of the control algorithms. Section II briefly describes the power converter topology. Section III addresses the requirements for the control of the two main stages: MMC and isolation stage using Dual Active Bridges (DABs). Alternatives for the implementation of the control are discussed in Section IV. Selection of the control hardware, implementation of the control and communications are presented in section V, VI and VII respectively. Experimental results are provide in Section VIII, Section IX summarizes the conclusions.

II. Proposed SST Topology

Fig. 2 shows the configuration of MMC based SST. For simplicity, the MMCs in the figure uses only two cells per arm (N=2). However, all the discussion following can be extended to any value of N without loss of generality. The topology of Fig. 2 is seen to combine a MMC (left side) with an isolation stage using DABs. In this figure, the left-side of the power converter will be considered as the high-voltage (HV) side. The right side of all the DABs in each leg (low voltage side), are connected in parallel. A conventional DC/AC power converter (e.g. two level or multilevel NPC, FC, …) can be used to connect with the LV AC grid.

It is noted that the power converter in Fig. 2 explicitly shows three ports: high voltage DC, high voltage AC and low voltage AC. A low voltage DC port also exists, but will not be used. This means that the power transferred by the DABs needs to be equal to the active power of the AC port in the low voltage side (losses neglected). This needs to be considered by the control algorithms.

III. Control Requirements

This section describes the control requirements for the different stages of the SST. This will be used later to assess the existing alternatives of its implementation.

a) Control of the MMC

Control of the MMC is challenging, as multiple control objectives need to be satisfied simultaneously. These include generation of the output AC voltage, control of the circulating current and balancing of the cells capacitors. Control and modulation strategies developed for MMC are basically aimed to balance the power between the AC and DC ports, which is performed by controlling the circulating current and by the balancing of the cell capacitor voltages [13].

Fig.3 shows a conventional control strategy. Active and reactive power commands are set in the high voltage AC side (see Fig.2 and Fig.3 “AC power control” block). By regulating the total capacitors voltage, the circulating current (i.e the DC current, neglecting harmonics) is trimmed to match the power between the DC and AC ports (Fig.3 – “Circulating current

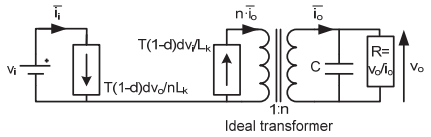


Fig. 4. Simple averaged model of the DAB.

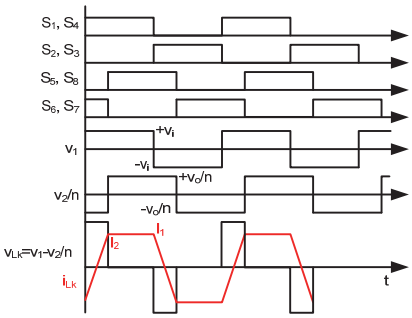


Fig. 5. Main operation waveforms of the phase-shift control method.

control" block). Simultaneously, the sorting algorithm selects the adequate cells that must be inserted/removed according to the individual cell capacitor voltages and the direction of the arm currents. Finally, a level shifted modulation strategy is responsible for generating the gate signals (Fig.3 – "Balancing and modulation" block).

As it can be noticed, control of the MMC implies a large amount of measurements and control signals. These include:

- Cell capacitor voltages (*N* x 3 x 2)
- DC current (1)
- Arm currents (6)
- AC currents (3)
- AC voltages (3)

It is noted that both the DC current of the MMC and the AC currents can be obtained from the measured arm currents. However, redundant current sensors are often used to enhance the accuracy and reliability. Typical sampling frequencies can be in the order of a few kHz.

b) Control of the DAB

The DAB converter was originally proposed in [3] and [15], and analyzed in more detail in [16],[17]. It is a bidirectional DC/DC converter with galvanic isolation based on two active bridges interfaced through a high-frequency transformer.

In the MMC-based SST shown in Fig.2, all the DABs are commanded to transfer the same amount of power at each MMC cell. The easiest way to control the DAB is by switching each full bridge (FB) using complementary constant pulse-width modulated signals with a 50% duty cycle, as shown in Fig.4. Using this modulation, a high-frequency square-wave voltage signal is generated at the transformer terminals ($\pm v_i$, $\pm v_o$). Considering the presence of the known leakage inductance of the transformer and controlling the transistors of both full bridges, the two square waves can be properly phase-shifted to regulate the power flow. These two phase-shifted signals (v_1 and v_2) generate a voltage (v_{Lk}) in the leakage inductance (L_k) of the transformer and a certain current (i_{Lk}) flows through it. This current is controlled by the phase shift between the primary and secondary voltages of the transformer (v_1 and v_2) [16],[17].

An averaged equivalent circuit of the DAB can be easily obtained [18], the input and output average current being (1) and (2), where d is the phase-shift, T is the semiperiod, and n the transformer ratio. Fig. 5 shows a simplified average model of the DAB.

$$\overline{i_i} = \frac{(1-d)dTv_o}{nL_k} \tag{1}$$

$$\overline{i_o} = \frac{(1-d)dTv_i}{nL_k}. \tag{2}$$

To design a feedback loop that ensures stable operation of the DAB, the small-signal dynamic model of the DAB must be considered. A simplified small-signal model of the DAB is proposed in [18] using the well-known averaged techniques presented in [19] and [20]. In this model, the output voltage variations due to variations in both the phase shift and the input voltage have the same characteristics as a first-order system response (the dynamic response of the converter is mainly determined by the value of the output capacitor and the load).

c) Control of the active rectifier on the LV side

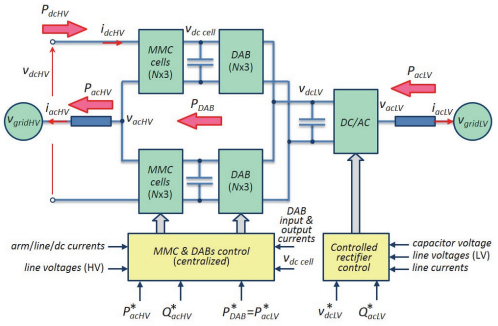
The LV DC/AC converter is controlled as a conventional active rectifier, where the commands are the DC link voltage and the reactive power at the LV AC side. The active power is therefore controlled to maintain the DC link capacitor voltage at its commanded value [23]. Control requirements for the low voltage DC/AC power converter are almost negligible compared to the requirements for the control of the MMC and DABs stages, and will not be further discussed in this paper.

IV. Control Structures: Centralized vs. Distributed Control

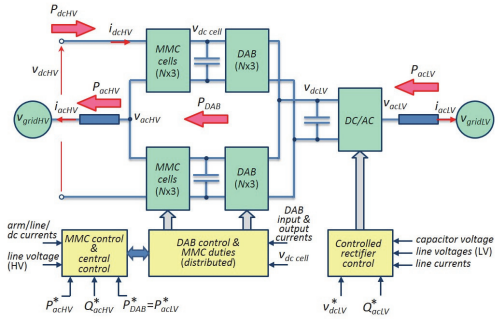
This section discusses potential implementations for the control of the SST. The two cases considered are a fully centralized control –in which a central controller measures all the variables and controls all the power switches of the MMC and DABs–, and a distributed control –in which a central controller measures some variables and executes the main converter control algorithms, but each MMC cell/DAB has a dedicated local control. Both cases are discussed following.

a) Centralized control

In a centralized control topology, one single processing unit is responsible of the control of both the MMC cells and the DABs. This is schematically shown in Fig. 6a. In this configuration, the aforementioned processing unit will have to manage the acquisition of every voltage and current sensor signal by means of a high enough number of AD converters and generate the corresponding gate signals sent to the drivers. Therefore, this topology requires a very large number of



a) Centralized control



b) Distributed control

Fig. 6.- Implementation using a) a centralized control and b) a distributed control

TABLE I. CENTRALIZED VS. DISTRIBUTED CONTROL: INPUT-OUTPUT REQUIREMENTS OF THE CENTRAL CONTROL

		Centralized control	Distributed control
Number of ADC channels	MMC variables	12	12
	DAB variables	3×3×2N = 18N (72 with N=4)	– (*)
Number of signals for communications	To/from MMC ADCs (No OF needed)	20	20
	To/from DAB ADCs (OF)	(4+3)×3×2N = 42N (168 with N=4)	– (*)
	To/from slave FPGAs (OF)	–	3×2=6 (communications optical fiber rings)
Number of signals for the drivers	To/from MMC (OF)	3×3×2N = 18N (72 with N=4)	– (*)
	To/from DAB (OF)	6×3×2N = 36N (144 with N=4)	– (*)
I/O ports	Without OF	20	20
	With OF	(42+18+36) N = 96N (384 with N=4)	6
	Total	20+96N (404 with N=4)	20+6

Notes: (*)This functionalities will be implemented in the distributed control
OF stands for Optical fiber

input/output ports. Most of them will be connected via optical fiber transmitters and receivers, since it is necessary to maintain electrical isolation. Table I summarizes the hardware requirements, they are assessed later in this section.

In addition to the hardware requirements, the computational requirements for the control unit are extremely high, as it has to implement both the control algorithms of the MMC and of all the DABs described in sections III-a and III-b respectively. It is also noted that these control algorithms operate with rather different sampling periods, a few kHz for the MMC and in the range of several tens of kHz for the DABs typically, what adds further challenges to their implementation in a single digital device.

b) Distributed control

In a distributed solution, control is split between a master/central control unit in charge of the MMC control algorithms and several slave processing units, each in charge of one DAB and its corresponding MMC cell. This is schematically shown in Fig. 6b. This topology allows a reduction of the number of input/output ports, also the computational burden of the central processing unit is significantly reduced. Moreover, since the slave devices are integrated in the DABs, the electrical isolation requirements for the sensors and drivers are lessened, reducing the count of optical fibers and shortening the length of those which are still necessary.

For the distributed control, it will be necessary to define a bidirectional communication between the central and slave devices. The central unit will send to the slave devices the commands for the power that each DABs has to transfer, as well as the corresponding duties for the MMC cells. The bandwidth for this communication is modest, as it does not need to transmit gate signals with precise timing. On the other hand, the slave units will send to the central unit through this link the measured cell capacitor voltages. These are needed by the central unit to realize the balancing of the MMC cell capacitors.

Table I summarizes the input/output requirements for the central control unit for the case of a centralized and a distributed control. The table includes the number of A/D channels which are needed to measure currents and voltages at different stages of the converter; number of lines for communications; number of lines to communicate with the drivers which control the power transistors. It is observed from this figure that, for the case of a SST with N=4, i.e. four cells per arm in the MMC (which is a modest amount), a total number of 384 optical fiber connections are needed, in addition to 20 cable connections (do not need isolation). It must be remarked in this regard that all the gate signals for both the DABs and the MMC cells come from the central control unit. On the other hand, the number of optical fiber connections is reduced to 6 for the case of the distributed control, where gate signals for each DAB and MMC cell are locally generated by the slave units.

Based on the preceding analysis, a distributed control has been selected. For the central control unit, a high performance System on Chip (SoC) will be used. For the slave units, low cost FPGAs are used. Discussion on the selection of the central control unit and slave units is presented in the next section.

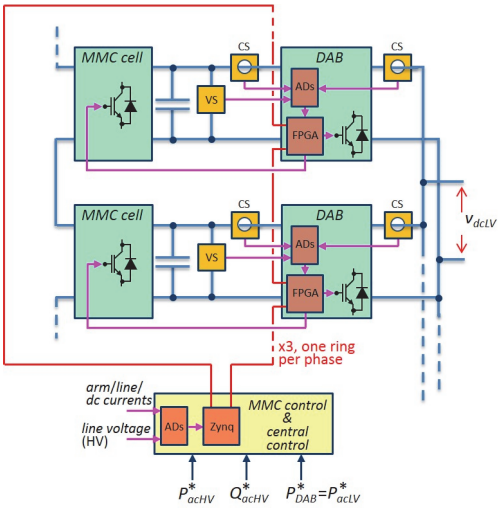


Fig. 7.- Overview of the distributed control. VS and CS stand for voltage sensor and current sensor respectively.

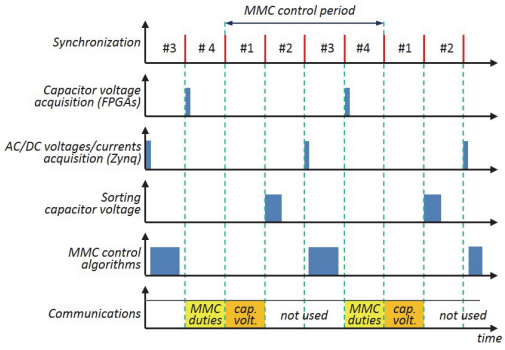


Fig. 8.- Timing diagram showing the different tasks needed for the SST distributed control, including communications

V. Selection of the Control Hardware

Fig. 7 shows the block diagram of the partially distributed control. The central control has medium processing requirements, the number of input/output signals being modest. These computational requirements could be met by high performance DSP type digital signal processors. For the implementation shown in Fig. 7, a Xilinx's Zynq-7000 SoC has been used. It comprises a dual core ARM processing system highly integrated with a FPGA. A Z-7020 device in a 200 I/O FPGA pins package has been chosen. It is noted that the I/O resources of the Zynq-7000 are significant higher than the actual needs for the implementation shown in Fig. 7. The reason for this selection is that the Zynq-7000 is currently being used to implement the control of conventional MMCs.

A low cost FPGA Spartan 3E 250K by Xilinx has been selected for the control of the DABs and generation of MMC cells gate signals. The current and voltages needed by the external control loops of the MMC are measured by two eight channel parallel bus 12 bit AD converters managed by the Zynq-7000. This requires a total of 20 non-optical fiber lines between the converters and the central control, 12 of them being the data bus and the remaining 8 being control signals, with the electrical isolation being provided by the sensors themselves (see Table I).

VI. Communications

The use of a distributed control system requires a communication network able to provide the bandwidth demanded by the control. As already mentioned, communication between the central control unit and the slave FPGAs will be bidirectional: the central control unit will transmit duty cycle values to the distributed control units, while the distributed control units will transmit the measured cell capacitor voltages to the central control unit, which are needed for balancing of the MMC cell capacitor voltages. The switching frequency of the MMC has been established in 5 kHz. Consequently, the information acquired by all the slave control units has to be transmitted in less than 200 µs.

The use of optical fiber is mandatory due to isolation requirements. Point-to-point communication is disregarded, due to the complexity and cost of the hardware. Ring configurations are therefore targeted. Each node in the ring will include one low-cost emitter and one receiver. The length of the optical fiber is also reduced, as the distance among DABs is significantly smaller than the distance between the DABs and the central control unit.

Considering the described scenario, a serial communication protocol using an optical fiber ring was considered advantageous. A modified version of TosNet protocol [21] was selected, as it can be fully implemented in the FPGAs with no need of additional hardware. In addition, TosNet is a master-slave isochronous protocol, which allows to coordinate the operation of all of the nodes by means of an internal deterministic synchronization signal (synchronization signal in Fig. 8).

The implemented protocol supports up to sixteen nodes. Three separate optical fiber rings will be used, one for each phase (see Fig. 7). Each ring consists of eight slave nodes, which correspond to the FPGAs in each DAB (four cells per arm, i.e eight cells per leg), and one master node, which is implemented in the central control unit. The central control unit is responsible for generating the synchronization signal, and consequently for the synchronization of the overall control process.

TosNet makes use of a shared memory block, which is transmitted to all of the nodes in the ring in every network cycle. In the proposed configuration, each of the slave nodes has assigned two sixteen-bit register of the memory block. The first register contains the MMC cell duty cycle; it is written by the central control and read by the slave FPGA. The second register contains the MMC cell capacitor voltage; it is written by the slave FPGA and read by the central control.

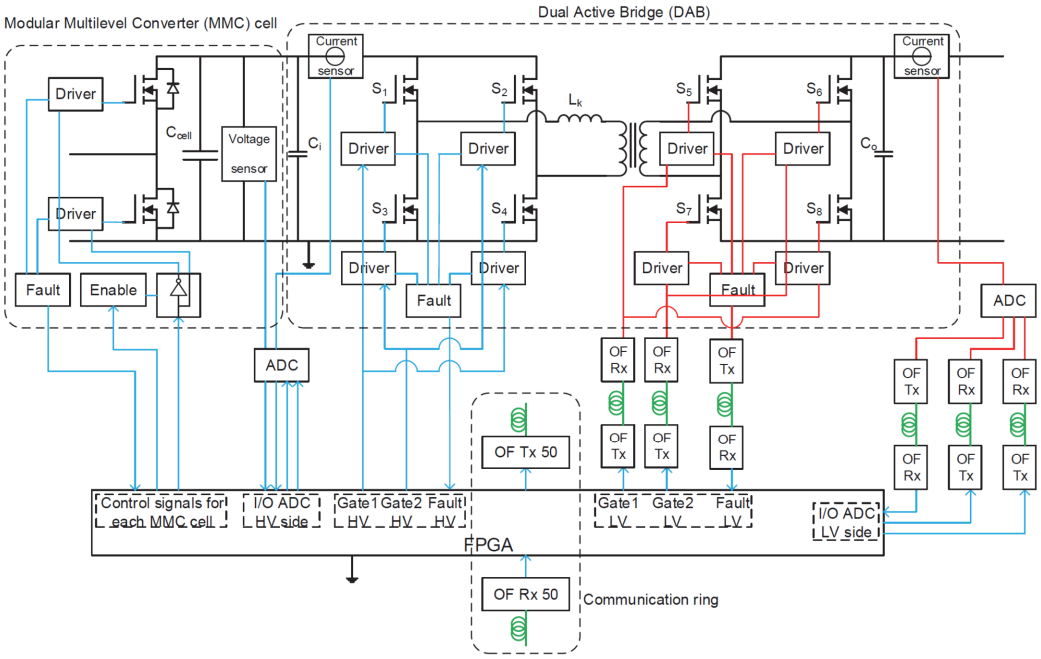


Fig. 9.- Detailed MMC cell and DAB, including sensors and control signals to/from drivers. "Of" stands for optical fiber.

Fig. 8 shows the timing diagram with the different tasks needed for the SST distributed control. The sampling period of the MMC is synchronized with the communications period, each MMC sampling period consisting of four communications periods (#1 to #4 in Fig. 8). In each communication period, the memory block containing the MMC cells duties and the cells capacitors voltage is transferred to all the elements in the ring (central control and slave FPGAs). However, the content of the memory block is only updated/read at well defined instants of time of the control process. The overall process works as follows:

- Communication period #4 (see Fig. 8): Cell capacitor voltages are acquired by the slave FPGAs. MMC duties to be applied to each MMC cell for the next control period are received by the slave FPGAs through the communications ring. Cell capacitor voltages transferred through the communications ring are not used.
- Communication period #1: Cell capacitors voltages are transferred by the slave FPGAs to the central control through the communications ring. Duties transferred through the communications ring in this period are not used.
- Communication period #2: Capacitor voltages are sorted by the MMC central control. Information transmitted through the communications ring is not used.
- Communication period #3: MMC AC and DC terminal voltages and currents are acquired. This occurs at the center of the MMC control period, therefore reducing the switching harmonics in the sampled AC currents. After this, the central control executes the control algorithms of the MMC. As a result, the duties for the MMC are available to be transferred during the next communication period (#4). Information transmitted through the communications ring is not used.

VII. Implementation of the Distributed Control

Fig. 9 shows a detailed block diagram of a generic MMC-based SST cell, including MMC cell and DAB. The central control unit (SoC) is responsible for the acquisition of the MMC terminal current/voltage measurements (DC and AC ports), implementation of the outer level control loops, and synchronization of the communications ring.

The slave FPGAs mounted in each DAB control the gate signals for both the DAB and MMC cell power switches, and measure the current and voltage signals needed for the control of the DAB current and MMC cell DC voltage. It is observed from Fig. 9 that the FPGA is located in the high voltage side of the DAB. The voltage sensor of each cell and the current sensor in the high voltage side of the DAB are connected to the corresponding ADC, which is directly connected to the FPGA (no isolation is needed). On the contrary, the current sensor in the low voltage side of the DAB requires an isolated ADC. Three optical fibers are needed for the communication between the FPGA and the low voltage side ADC.

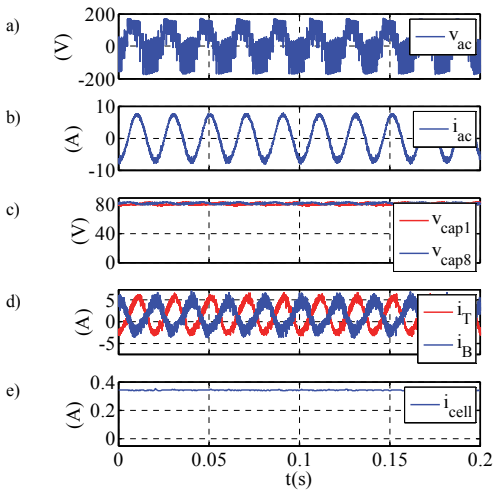


Fig.10.- Experimental results. a) AC voltage, b) AC current, c) capacitor voltage of two cells, d) top and bottom arm currents, and e) current transferred by the DAB

The driver signals for the power switches in the primary of the DAB are directly connected to the FPGA. Optical fiber is used to provide the required isolation between the FPGA and the secondary of the DAB. Two gate signals are required to control the four power switches used by each full bridge of the DAB.

The gate signals for the MMC cell half-bridge are calculated by the FPGA from the duty commands received from the MMC central control through the communications ring. Three signals are used to connect the FPGA with the MMC cell:

- Gate signal. Using this gate signal and analog circuitry, two complementary PWM signals are generated to control the two power devices of the cell.
- Enable signal. Open all the switches of the MMC in case of failure, or previously to the DAB turn off.
- Fault signal. Is sent by the drivers to the central control whenever an anomalous condition is detected.

Finally, only two fiber optic lines are required for the communication ring connecting the central control and the slave FPGAs. To fulfill bandwidth of the communication protocol, the selected optical fiber can operate up to 50MBd. However, the rest of signals transmitted using optics fiber (gate signals, fault signals and ADC signals) can use a reduced bandwidth (up to 1MBd), thus enabling a cheaper optical fiber.

VIII. Experimental Results

Fig. 10 shows the experimental results obtained with a scaled prototype using the proposed SST concept and decentralized control strategy. The experiments were realized using a single phase MMC. Fig. 10a and 10b show the phase currents and voltages of the AC side of the MMC. Fig. 10c and 10d show two MMC capacitors voltages, and the top and bottom arm currents. Finally, Fig. 10e shows the current transferred by the DAB. As described in the preceding sections, the central control unit implements the control loops of the MMC shown in Fig. 3, while the DAB low cost FPGA shown in Fig. 9 controls the DAB current.

IX. Conclusions

This paper has described the implementation of the control of a modular solid state transformer. Configuration of the control, selection of the control hardware, and communications requirements have been addressed. A distributed control, with the central control using a high performance Zynq device and the local controls using a low cost Spartan FPGA, combined with a TosNet protocol for the communication, has been shown to be a viable solution, meeting the control requirements at a reasonable cost.

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Control Strategies for MMC Using Cells with Power Transfer Capability

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***Abstract*—Conventional MMCs use cells which typically consist of a half-bridge and a capacitor. Due to their limited energy storage capability, the net power balance of the cells is zero (neglecting losses), the MMC therefore realizing a bidirectional power transfer between its DC and AC ports. It is possible however to provide the MMC with the capability to transfer power at the cell level. The use of such cells opens new functionalities and uses for the MMC, including integration at the cell level of distributed energy storage (e.g. batteries), low-voltage/low power sources/loads, and its operation as a multiport power converter, combining high and low voltage AC and DC ports. Existing control strategies for MMCs assume that all the cells have an identical design and operate identically. However, use of cells with power transfer capability can result in imbalances in their operation, provided that not all the cells transfer power, or that they do not transfer the same amount of power.**

This paper addresses the design and control of MMCs using cells with power transfer capability, with special focus on the design of suitable control strategies and on the definition of their limits of operation.

***Index Terms*—Modular Multilevel Converter, MMC, Multiport Power Converters, Solid State Transformer**

I. Introduction

Reducing the dependence on conventional fossil fuels has become a priority for industrialized countries due to environmental concerns, limited resources and the progressive increase of their cost. This scenario has pushed the penetration of renewable energies in the existing transmission system. However, massive integration of renewable energy into the existing and future grids poses major challenges, as a significant part of the installed capacity will be connected to the distribution levels [1]. Innovative solutions based on high-power, high-voltage electronic power converters, like High Voltage Direct Current (HVDC) and Flexible AC Transmission Systems (FACTS) have the potential to cope with these challenges, also providing to the power system operator functionalities such as power flow control, power quality improvement and reduction of transmission losses among others [2].

Multilevel converters are well suited for medium-high voltage/power ranges which are required for electronic power converters connected to medium voltage electrical grids [3]. Among these, the Modular Multilevel Converters (MMCs) appear as a promising topology for applications requiring a high voltage DC port (e.g. HVDC), being a hot research topic nowadays. MMC was first introduced one decade ago [4]-[6]. It realizes a bidirectional DC/AC power conversion, sharing the advantages of other multilevel converters: reduced size of filters due to better output voltage wave shape; lower switching losses due to the reduced switching frequency; capability of withstanding large terminal voltages using relatively low voltage power devices. Additionally, it provides attractive features compared to other multilevel topologies, such as modularity (identical cells are piled-up to increase the voltage) and consequently easy scalability, and distributed energy storage, therefore eliminating the need of a bulk DC capacitor [4]-[7].

Conventional MMC use cells consisting of a half-bridge and a capacitor. Control and modulation strategies developed for MMCs are aimed to balance the power between the AC and DC ports, which is needed to maintain the average voltage of the cells capacitors at its target value. This is done by controlling the circulating current either explicitly [8]-[13] or indirectly (i.e direct modulation) [14]-[16]. Balancing of the cell capacitor voltages is also required [4]-[16]. Due to the fact that the cells have a limited energy storage capability, the net power balance for each cell is zero (neglecting losses), AC and DC powers being therefore equal to each other. It is possible however to transfer (absorb or deliver) power through the MMC cells. This would provide the MMC with new potential features, including distributed energy storage [17]; integration of distributed energy resources (DER) at the cell level; multiport multilevel power converters combining the medium/high voltage DC and AC ports of the MMC with low voltage DC and AC ports. Another potential application being Solid State Transformers (SST) [19]-[21].

This paper addresses the design and control of MMCs using cells with power transfer capability. The paper is organized as follows. Basic concepts and power balance requirements of conventional MMCs are presented in Section II. Section III extends the analysis to the case of MMCs using cells with power transfer capability. Section IV presents MMC configurations using cells with power transfer capability. Limits of operation and control strategies are presented in Sections V and VI respectively, simulation and experimental results being presented in Sections VII and VIII. Finally, conclusions are presented in Section IX.

This work was supported in part by the Research, Technological Development and Innovation Programs of the Spanish Ministries of Science and Innovation and of Economy and Competitiveness, under grants MICINN-10-CSD2009-00046 and MINECO-13-ENE2013-48727-C2-1-R, and by the European Commission FP7 Large Project NMP3-LA-2013-604057, under grant UE-14-SPEED-604057.

978-1-4673-7151-3/15/$31.00

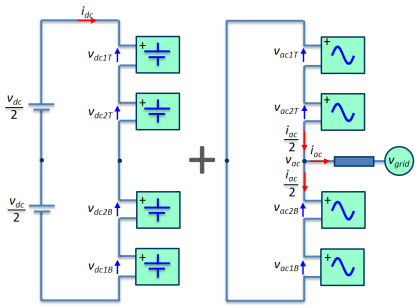

Fig. 1. DC (left) and AC (right) subcircuits of the MMC.

II. MMC Model and Power Balance

MMCs realize a power transfer between an AC and a DC port. It is useful for analysis purposes to separate the MMC into its DC and AC subcircuits, as shown in Fig. 1. The discussion following assumes two cells per arm (N=2), without loss of generality. Also the voltage drop in the arm inductors is neglected for simplicity. For the case of a three-phase MMC, complex vector notation can be used to represent the AC variables, such as voltage (1) and current vectors (2). For the DC subcircuit (Fig. 1-left), the cells are series connected, the resulting voltage being equal to the DC voltage of the MMC (3). On the contrary, for the AC voltage subcircuit (Fig. 1-right), top and bottom arms are parallel connected, the corresponding AC cell voltages being (4) and (5) respectively. Consequently, AC current equally splits between the two arms. The resulting top and bottom arm currents are (6) and (7), the circulating current being (8). For the sake of simplicity, it is assumed that the circulating current does not contain harmonics [13][18], being therefore equal to the DC current.

$$v_{ac} = \frac{2}{3}\left(v_u + v_v e^{j2\pi/3} + v_w e^{j4\pi/3}\right) \tag{1}$$

$$i_{ac} = \frac{2}{3}\left(i_u + i_v e^{j2\pi/3} + i_w e^{j4\pi/3}\right) \tag{2}$$

$$v_{dcnT} = v_{dcnB} = \frac{v_{dc}}{2N} \tag{3}$$

$$v_{acnT} = \frac{v_{acT}}{N} = \frac{-v_{ac}}{N};\ \ n = 1,2 \tag{4}$$

$$v_{acnB} = \frac{v_{acB}}{N} = \frac{v_{ac}}{N};\ \ n = 1,2 \tag{5}$$

$$i_T = i_{dc} + \frac{i_{ac}}{2} \tag{6}$$

$$i_B = i_{dc} - \frac{i_{ac}}{2} \tag{7}$$

$$i_c = \frac{i_T + i_B}{2} = i_{dc} \tag{8}$$

Since conventional cells have limited energy storage capability, the power in the DC port has to be equal to the active power in the AC port (9). The DC current is controlled to match the DC and AC powers (10)-(11). In addition, cell capacitor voltages must be kept at their target value, e.g. using sorting algorithms [12]-[16] or individual balancing [8]-[10].

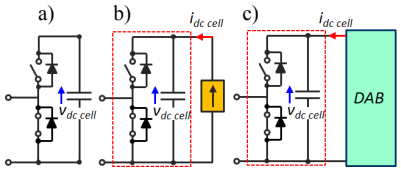

Fig. 2. a) Conventional half-bridge cell with a capacitor in the DC link; b) cell including a current source; c) cell using a DAB.

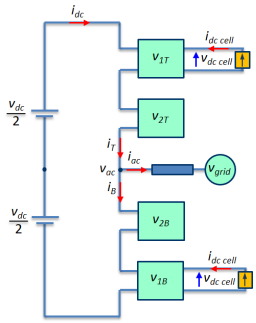

Fig. 3. MMC including cells with power transfer capability in all the three phases. Same number of cells in top and bottom arms transfer power.

$$P_{dc} = v_{dc} \cdot i_{dc} = P_{ac} = Re\left(v_{ac} \cdot {i_{ac}}^*\right) \tag{9}$$

$$P_{dcnT} = P_{dcnB} = \frac{v_{dc}}{2N} i_{dc} = \frac{v_{dc}}{4} i_{dc};\ \ n = 1,2 \tag{10}$$

$$P_{acnT} = P_{acnB} = Re\left(\frac{v_{acT}}{N}\frac{{i_{ac}}^*}{2}\right) = Re\left(\frac{v_{acB}}{N}\frac{-{i_{ac}}^*}{2}\right) \tag{11}$$

III. Power Balance in MMCs Using Cells with Power Transfer Capability

As already mentioned, it is possible for the MMC to transfer power at the cell level. Assumed that the cells are adequately controlled to maintain the capacitor voltage v_{dccell} constant, connection of a power source to the cell can be modeled as a current source connected to the cell capacitor (Fig. 2 b)[19]. In a practical implementation, galvanic isolation between the cell capacitor and the power source will be normally needed. A current controlled dual active bridge (DAB) could be used for this purpose (Fig. 2-c) [17], [19]-[21]. In the discussion following, it is assumed that cells $1T$ and $1B$ in all the three-phases transfer power (see Fig.3). Due to the symmetry among phases and between the top and bottom arms, injection of power at the cell level will not produce any type of harmonics or imbalances in the DC and AC voltages of the MMC.[19].

The power balance equation of the MMC including cells with power transfer capability is given by (12), where M stands for the number of cells transferring power. The power balance equations for the individual cells are (13)-(16). It is noted that the power transferred by cells $2T$ and $2B$ is zero.

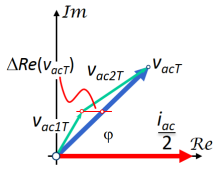

Fig. 4. AC voltage unbalance varying only the real component of the cell voltages (Im(v_{ac1T})=Im(v_{ac2T})).

$$P_{dc} + P_{ac} + M \cdot P_{cell} = 0 \tag{12}$$

$$P_{cell1T} = v_{dc1T} \cdot i_{dc} + Re\left(v_{ac1T} \frac{{i_{ac}}^*}{2}\right) = v_{dccell} \cdot i_{dccell} \tag{13}$$

$$P_{cell2T} = v_{dc2T} \cdot i_{dc} + Re\left(v_{ac2T} \frac{{i_{ac}}^*}{2}\right) = 0 \tag{14}$$

$$P_{cell1B} = v_{dc1B} \cdot i_{dc} + Re\left(v_{ac1B} \frac{-{i_{ac}}^*}{2}\right) = v_{dccell} \cdot i_{dccell} \tag{15}$$

$$P_{cell2B} = v_{dc2B} \cdot i_{dc} + Re\left(v_{ac2B} \frac{-{i_{ac}}^*}{2}\right) = 0 \tag{16}$$

Differences in the power balance equation of the cells will imply asymmetries in their terminal voltages and/or currents. Since the DC current is common to all the cells, the asymmetries need to occur in the cell DC voltages v_{dcnT}, v_{dcnB}, AC voltages v_{acnT}, v_{acnB}, or in the AC component of the arm currents i_T and i_B. In the discussion following, it is assumed that the asymmetries occur in the cell voltages. The DC and AC voltages equations can be rewritten as (17)-(18) and (19)-(20) respectively, Δv_{dc} and $\Delta Re(v_{ac})$ accounting for the DC and AC voltage imbalance among the cells in each arm.

$$v_{dc1T} = \frac{v_{dc}}{4} + \Delta v_{dc} = v_{dc1B} \tag{17}$$

$$v_{dc2T} = \frac{v_{dc}}{4} - \Delta v_{dc} = v_{dc2B} \tag{18}$$

$$v_{ac1T} = \frac{v_{acT}}{2} + \Delta Re\left(v_{ac}\right) = v_{ac1B} \tag{19}$$

$$v_{ac2T} = \frac{v_{acT}}{2} - \Delta Re\left(v_{ac}\right) = v_{ac2B} \tag{20}$$

It is noted that since the AC voltage v_{ac} is a complex vector, $\Delta Re(v_{ac})$ is a complex vector too. In the discussion following, the real axis is defined to be aligned with the AC current vector (see Fig. 4). By doing this, $\Delta Re(v_{ac})$ only affects to the active power transferred by the cells [19]. It is finally noted that irrespective of the imbalances among cells, the overall DC and AC voltages of the MMC (21) and (22) remain unchanged.

$$v_{dc1T} + v_{dc2T} + v_{dc1B} + v_{dc2B} = v_{dc} \tag{21}$$

$$v_{ac1T} + v_{ac2T} = v_{ac1B} + v_{ac2B} = v_{ac} \tag{22}$$

Using (13)-(20), it is possible to analyze the effects of Δv_{dc} and $\Delta Re(v_{ac})$ on the power transferred by the cells (13)-(16) and on the MMC power balance (12). Fig. 5-a shows the power

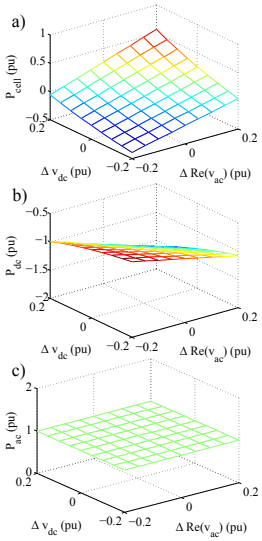

Fig. 5. a) Cell power P_{cell}; b) DC port power P_{dc}; c) AC port power P_{ac}; as a function of Δv_{dc} and $\Delta Re(v_{ac})$, for constant AC power

transferred by cells $1T$ and $1B$ vs. Δv_{dc} and $\Delta Re(v_{ac})$, for constant AC power P_{ac} (Fig. 5-c). The power transferred by the cells is seen to affect to the power at the DC port of the MMC, (Fig. 5-b), (12) holding in all the cases. Power transferred by cells $2T$ and $2B$ is always zero.

A. MMC Power Balance Constraints

MMCs including cells with power transfer capability must satisfy the power balance equation (12). However, there are constraints regarding the way in which the AC, DC and cell powers can be combined in (12) which need to be considered. Table I summarizes the different modes of operation and their feasibility for the particular case shown in Fig. 3 and Fig.6-d. It is possible to transfer all the cell power P_{cell} to the AC port ($Mode$ 2). On the contrary, transferring the power from the cells to the DC port is only possible if there is reactive power in the AC port ($Mode$ 4). It must be remarked that $Mode$ 3 is not possible for the topology in Fig.6-d, but becomes feasible for the fully symmetric topology in Fig.6-e.

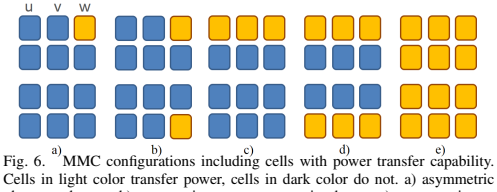

Fig. 6. MMC configurations including cells with power transfer capability. Cells in light color transfer power, cells in dark color do not. a) asymmetric phases and arms; b) symmetric arms, asymmetric phases; c) asymmetric top and bottom arms; d) symmetric top and bottom arms, asymmetric cells; e) fully symmetric

TABLE I
POWER TRANSFER MODES (TOPOLOGY IN FIG.6-D)

$Mode$	P_{cell}	P_{dc}	P_{ac}	Q_{ac}	$Feasible$
1	0	$\neq 0$	$\neq 0$	–	Yes ($P_{dc}+P_{ac}$=0)
2	$\neq 0$	0	$\neq 0$	–	Yes ($MP_{cell}+P_{ac}$=0)
3	$\neq 0$	$\neq 0$	0	0	Not feasible
4	$\neq 0$	$\neq 0$	0	$\neq 0$	Yes ($MP_{cell}+P_{dc}=0$)
5	$\neq 0$	$\neq 0$	$\neq 0$	–	Yes ($P_{dc}+P_{ac}+M\cdot P_{cell}$=0)

TABLE II
TYPES OF ASYMMETRY AND EFFECTS ON THE AC PORT DEPENDING ON THE APPLIED CELL VOLTAGE IMBALANCE

Type of asymmetry	*Voltage imbalance*	*Effect on MMC operation*
Fig.6-a)	Δv_{dc}	DC zero sequence in the AC port voltage
	$\Delta Re(v_{ac})$	Unfeasible
Fig.6-b)	Δv_{dc}	DC zero sequence in the AC port voltage
	$\Delta Re(v_{ac})$	Different i_{cx} within phases
Fig.6-c)	Δv_{dc}	DC zero sequence in the AC port voltage
	$\Delta Re(v_{ac})$	Unfeasible
Fig.6-d)	Δv_{dc}	No effect
	$\Delta Re(v_{ac})$	No effect
Fig.6-e)	$\Delta v_{dc}=0$	No effect
	$\Delta Re(v_{ac})=0$	No effect

IV. MMC CONFIGURATIONS USING CELLS WITH POWER TRANSFER CAPABILITY

In the MMC shown in Fig. 3, the same number of cells in the top and bottom arms and in all the three phases transfer power, i.e. phases and arms are symmetric. While this is the case analyzed in detail in this paper, other options exist, they are discussed briefly in this section. Depending on the number and location of the cells transferring power (see Fig.6), different types of asymmetries (imbalances) among cells, and consequently among arms or legs, can occur. In all the cases, all the cells in each leg of the MMC must have the same DC current. It is also assumed that the AC current equally splits among the top and bottom arms of each leg. Accordingly, all the cells must have the same DC and AC currents. Consequently, producing asymmetries in the power transferred by the cells will produce asymmetries in their DC and/or AC voltages (17)-(20).

Imbalances among phases and arms (Fig.6-a) will result in different DC voltages for the cells in phase w, eventually resulting in a DC zero sequence voltage in the AC voltage vector v_{ac}. Unbalancing the cells AC voltages is not possible, since both top and bottom must generate the same AC voltage v_{ac} and the currents are the same. The case shown in Fig.6-b, produces DC zero sequence voltage in the AC port. Unbalancing the AC cell voltages is also feasible, but will result in unbalances among phases in the circulating currents i_{cx}. Fig.6-c produces imbalances between the DC voltage for the top and bottom arms of all the three phases, and consequently a DC zero sequence component in the AC voltage v_{ac}. Unbalancing the cell AC voltages is not possible. In the case shown in Fig.6-d, top and bottom arms are symmetric, but there are imbalances among the cells in each arm. Cells DC and/or AC voltages can be unbalanced in this case, but with no impact on the AC voltage of the MMC v_{ac}. Finally, Fig.6-e does not produce any type of unbalance either in the MMC voltages or in the arm voltages. Table II summarizes the different types of asymmetries and the effects on the MMC/cells behavior.

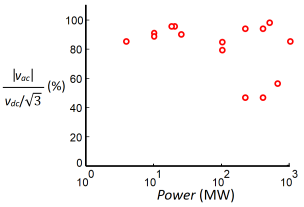

Fig. 7. AC/DC voltage ratio R vs. power in existing (or in progess) MMC.

V. LIMITS OF OPERATION OF CELLS WITH POWER TRANSFER CAPABILITY

A. Cells and MMC voltage limits & cell power transfer limits

It has been shown in Section III that power transferred by cells is controlled by adequate selection of the voltage imbalance, the amount of power being transferred being proportional to $|\Delta v_{dc}|$ and $|\Delta Re(v_{ac})|$. The maximum power that can be transferred will depend therefore on the maximum voltage imbalance that can be produced. Consequently, cells and MMC voltage restrictions need to be considered.

Cells lower and upper voltage limits for half bridge cells are 0 and $v_{dc\,cell}=v_{dc}/N$ respectively. As for the MMC, the peak value of the AC voltage v_{ac} is limited to $-v_{dc}/2$ and $v_{dc}/2$. The ratio between the MMC AC and DC port voltages (23) will be therefore a key figure. It is noted that the line impedance voltage drop was neglected in this equation for simplicity. Triplen harmonic injection is also considered.

$$R=\frac{\sqrt{3}\cdot|v_{ac}|}{v_{dc}} \tag{23}$$

R indicates the voltage margin which is available to produce voltage imbalances among cells. For $R=1$, all the cells operate at their voltage limit, no voltage imbalance being therefore possible. Values of $R<1$ mean that a voltage margin exists to introduce imbalances among cells voltages. For reference, Fig. 7 shows examples of the R ratio reported for already installed (or under development) MMC.

The maximum power that cells can transfer will depend on:

- The voltage margin R
- The AC port power (active and reactive)
- The number of cells transferring power M

Fig. 8-a) and Fig. 8-b) schematically show the resulting DC and AC cell voltages, considering the imbalance limits $\Delta v_{dc\,max}$ and $\Delta Re(v_{ac\,max})$, which are function of the voltage margin R. Subindex $1T$ and $1B$ account for all the cells in the top and bottom arms transferring power, and $2T$ and $2B$ for cells which do not transfer power.

It is finally noted that the sign of Δv_{dc} and $\Delta Re(v_{ac})$ need to be selected according to the sign of the cell power (injected or drawn) and the sign of the AC power, as shown in Table III. For $P_{ac}>0$, increasing the power transferred by the cell (i.e. more negative cell power, $\downarrow$) can be achieved either decreasing Δv_{dc} ($\downarrow$) or increasing $\Delta Re(v_{ac})$ ($\uparrow$). The opposite behavior occurs for $P_{ac}<0$. Sign $(+)$ in brackets stands for the same variation direction as P_{cell}, the opposite represented by $(-)$.

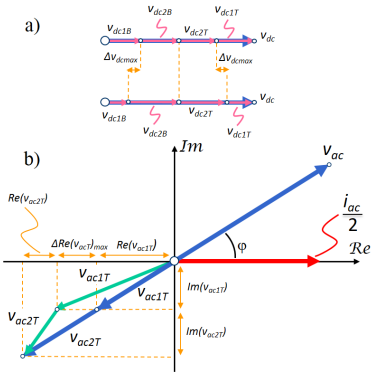

Fig. 8. Voltage imbalance limits for $P_{ac} > 0$. a- DC cell voltage imbalance. b- AC cell voltage imbalance (real axis aligned with the AC current vector)

TABLE III
CELL POWER VS. VOLTAGE IMBALANCE

AC Power	*Voltage imbalance*	
P_{ac}	$\frac{\Delta P_{cell}}{\Delta v_{dc}}$	$\frac{\Delta P_{cell}}{\Delta Re(v_{ac})}$
> 0	$(+)$	$(-)$
< 0	$(-)$	$(+)$

B. Maximum power transfer using AC voltage imbalance

This subsection discusses the maximum power can be transferred by the cells when the voltage margin R is used exclusively to produce an AC voltage imbalance. Since the d-axis is defined to be aligned with the AC current (see Fig. 8), the d-axis component of the voltage vector will be responsible of the active power and the q-axis voltage of the reactive power. The discussion following is particularized for the top arm voltages, identical conclusions are reached for the bottom arm voltages. The maximum d-axis voltage that any cell can produce is given by (24), v_{acTq} being the q-axis voltage needed to supply the requested AC reactive power.

$$v_{acTd\,max} = \sqrt{\left(\frac{v_{dc}}{2N}\right)^2 - \left(\frac{v_{acTq}}{N}\right)^2} \tag{24}$$

The actual AC voltage for each particular cell will depend on the sign of P_{ac}. For $P_{ac} > 0$, the maximum AC voltage of the cells injecting power is (24). The M cells injecting power account for a total voltage v_{ac1Td} (25). The $N - M$ cells which do not inject power account therefore for a total voltage of v_{ac2Td} (26). The overall AC voltage vector of the M cells injecting and the $N - M$ cells which do not inject is given (27) and (28) respectively.

$$v_{ac1Td} = M \cdot v_{acTd\,max} \tag{25}$$

$$v_{ac2Td} = v_{acTd} - v_{ac1Td} \tag{26}$$

$$v_{ac1T} = v_{ac1Td} + j\frac{v_{acTq}}{N} \tag{27}$$

$$v_{ac2T} = v_{ac2Td} + j\frac{v_{acTq}}{N} \tag{28}$$

Analogously, (29)-(32) hold for the case of $P_{ac} < 0$.

$$v_{ac2Td} = (N - M) \cdot v_{acTd\,max} \tag{29}$$

$$v_{ac1Td} = v_{acTd} - v_{ac2Td} \tag{30}$$

$$v_{ac1T} = v_{ac1Td} + j\frac{v_{acTq}}{N} \tag{31}$$

$$v_{ac2T} = v_{ac2Td} + j\frac{v_{acTq}}{N} \tag{32}$$

In both cases, (33) and (34) hold.

$$v_{dc1T} = \frac{v_{dc}}{2N} \cdot M \tag{33}$$

$$v_{dc2T} = \frac{v_{dc}}{2N} \cdot (N - M) \tag{34}$$

The maximum power that the cells can transfer is (35).

$$P_{cell\,max} = 3\left(\frac{v_{dc1T}}{v_{dc2T}}\, v_{ac2Td}\, \frac{i_{ac}}{2} + v_{ac1Td}\, \frac{i_{ac}}{2}\right) \tag{35}$$

Finally, it is possible to express the d-axis component of the AC voltage for non-injecting ($2T$) and injecting ($1T$) cells as a function the DC current i_{dc}, AC voltage v_{ac} and AC current i_{ac} (36)-(37). Alternatively, v_{ac2Td} and v_{ac1Td} can also be written as a function of the apparent power, load angle and power injected (or drained) by the cells.

$$v_{ac2Td} = -\frac{2}{3N}\frac{v_{dc}(N - M)i_{dc}}{i_{ac}} \tag{36}$$

$$v_{ac1Td} = v_{acTd} - v_{ac2Td} \tag{37}$$

C. Maximum power transfer using DC voltage imbalance

This subsection discusses the maximum power that can be transferred by the cells when all the available voltage margin R is used to produce a DC voltage imbalance. The maximum and minimum DC voltage that a conventional half-bridge cell can withstand are (38)-(39).

$$v_{dcT\,max} = \frac{v_{dc}}{N} - \frac{|v_{acT}|}{N} \tag{38}$$

$$v_{dcT\,min} = \frac{|v_{acT}|}{N} \tag{39}$$

Table IV shows the voltage for the injecting and non-injecting cells v_{dc1T} and v_{dc2T}, as a function of the AC power sign and of the number of cells injecting.

TABLE IV
DC VOLTAGE IMBALANCE

P_{ac}	M vs. N	v_{dc1T}	v_{dc2T}
> 0	$M > (N - M)$	$\frac{v_{dc}}{2} - v_{dc2T}$	$v_{dcT\,max}(N - M)$
< 0	$M > (N - M)$	$\frac{v_{dc}}{2} - v_{dc2T}$	$v_{dcT\,min}(N - M)$
> 0	$M < (N - M)$	$v_{dcT\,min}M$	$\frac{v_{dc}}{2} - v_{dc1T}$
< 0	$M < (N - M)$	$v_{dcT\,max}M$	$\frac{v_{dc}}{2} - v_{dc1T}$

AC voltage sharing between the injecting and non-injecting cells in all the cases is given by (40) and (41).

$$v_{ac1T} = \frac{v_{acT}}{N} \cdot M \tag{40}$$

$$v_{ac2T} = \frac{v_{acT}}{N} \cdot (N - M) \tag{41}$$

Maximum power that can be transferred by the cells is obtained from (35). As for the AC voltage imbalance case, the DC voltage for non-injecting and injecting cells can be expressed as a function the DC current i_{dc}, AC voltage v_{ac} and AC current i_{ac}, (42), (43).

$$v_{dc2T} = -\frac{3}{4}\frac{v_{ac2Td} \cdot i_{ac}}{i_{dc}} \tag{42}$$

$$v_{dc1T} = -\frac{v_{dc}}{2} - v_{dc2T} \tag{43}$$

D. Numerical analysis

Fig. 9 shows the maximum power that can be transferred by the cells, $P_{cell\ max}$, as a function of the apparent power S_{ac} and the AC load angle for three values of M, for the case of DC and AC voltage unbalances.

Fig. 9-left shows maximum power when only a DC cell voltage imbalance is used. Peaks occur for the case of pure active power (0 and 180 degrees) in the AC port. In these cases, the ratio i_{dc} vs. $|i_{ac}|$ is maximum, so is the power transfer resulting from imbalances in the cell DC voltage. The maximum power capability occurs for a purely negative active power. In this case, the MMC AC voltage decreases, increasing the voltage margin. On the contrary, it is not possible to transfer cell power if purely reactive power exists in the AC port (90 and 270 degress). In these cases $i_{dc} = 0$, imbalances in the cell DC voltage not producing a power transfer.

It is seen from Fig. 9-left-a) and b) that increasing the number of active cells M increases the power transferred. However, there is a limit for this, which occurs when the number of cells injecting equals the number of cells which do not inject (i.e. $M = N/2$). Increasing M beyond this limit does not increase the overall power transfer (see Fig. 9-left-b) and c)). This is due to the fact that the overall DC port voltage v_{dc} has to be shared by the cells injecting power.

Fig. 9-right shows the power transferred by the cells when only a AC cell voltage imbalance is used. Unlike the previous case, peaks of the power transfer occur for purely AC reactive power (90 and 270 degrees). The reason is that the voltage margin needed to produce the voltage unbalance increases when there is no active power. It is noted that in this case, the power transferred increases proportionally to the number of cells transferring power M.

It is finally noted that for any value of the apparent power and load angle, AC voltage imbalances (Fig. 9-right) allow to transfer more power than DC voltage imbalances (Fig. 9-left).

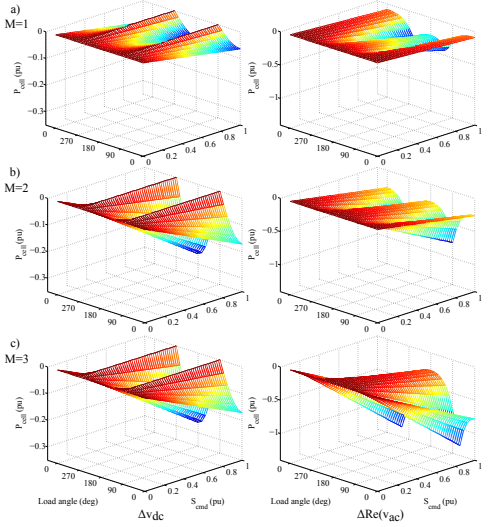

Fig. 9. Maximum power transferred by the cells for a) $M = 1$, b) $M = 2$ and c) $M = 3$ ($N = 4$), as a function of the apparent power and load angle, for the case of DC (left) and AC (right) voltage imbalances.

VI. Control Strategies for MMCs Using Cells with Power Transfer Capability

The use of cells with power transfer capability poses new challenges regarding control and modulation strategies, as the existing methods are aimed to balance the operation of cells which have an identical design and operate identically [7]-[16]. It has been shown in the previous sections that the power transferred by the cells can be controlled by adequate selection of the voltage imbalances Δv_{dc} and $\Delta Re(v_{ac})$. Consequently, control strategies which provide individual voltage commands for each cell are convenient. A key feature of the potential methods will be therefore whether they use sorting algorithms [12]-[16] or individual balancing [8]-[10]. Two different control strategies are discussed following: A) without explicit selection of Δv_{dc} and $\Delta Re(v_{ac})$ and B) with explicit selection of Δv_{dc} and $\Delta Re(v_{ac})$. In the discussion following, MMC with symmetric top and bottom arms (Fig.6-d)-e)) is assumed.

A. No explicit selection of Δv_{dc} and $\Delta Re(v_{ac})$

Control strategies using sorting algorithms for balancing do not allow to generate individual voltage commands. These strategies still allow to control the power transferred by the cells thanks to the combined action of the circulating current control and sorting algorithm [13]. However, no explicit values for Δv_{dc} and $\Delta Re(v_{ac})$ are given. This means that for a given power in the AC side and a ratio R, it is not guaranteed that the cells will transfer the maximum possible power [19].

B. Explicit selection of Δv_{dc} and $\Delta Re(v_{ac})$ commands

It is possible to control the power transferred by the cells by explicitly selecting Δv_{dc} and $\Delta Re(v_{ac})$. Fig. 10 shows the control strategy proposed in this paper. Its main blocks are discussed following.

The desired active and reactive powers in the AC side are the inputs to the *AC power control* block. The resulting voltage commands $v_d{}^*$ and $v_q{}^*$ are referred to a reference frame aligned with the grid voltage angle φ_{grid}. The number of cells transferring power M must be known in advance. *Voltage commands* block uses (36)-(37) to obtain the AC voltage imbalance required to transfer the cell power. This block operates in a reference fame aligned with the AC current. Similarly, (42)-(43) are used to obtain the DC cell voltage imbalance. It was already mentioned that AC voltage imbalances allow to transfer larger amounts of power compared to DC voltage imbalance.

If wished, DC voltage unbalance can be disabled, the DC port voltage being in this case evenly split among all the cells. Once the required AC and DC cell voltages are set, (44)-(45) are used to obtain the overall cell voltages [9].

$$v^*_{jxT} = v_{dcjT} - v^*_{acjxT} - \frac{v^*_{Lx}}{2N} \quad j = 1:N; x = u, v, w \quad (44)$$

$$v^*_{jxB} = v_{dcjB} + v_{acjxB} - \frac{v^*_{Lx}}{2N} \quad j = 1:N; x = u, v, w \quad (45)$$

Circulating current control block controls the circulating current to balance the DC power. An arm balancing control strategy is used to balance the voltage between the upper and lower cell capacitors [13],[15]. Once the references for all the cells are obtained, individual balancing and phase shifted modulation are used to obtain the switches gate signals [9].

TABLE V
SIMULATION RESULTS. AC VOLTAGE IMBALANCE.

	v_{ac1Td}(V)		v_{ac1Tq}(V)		v_{ac4Td}(V)		v_{ac4Tq}(V)	
	before	after	before	after	before	after	before	after
M=3 $\varphi = 0^o$	-341.1	-371.8	-21.75	-21.75	-341.1	-248.13	-21.75	-21.75
M=2 $\varphi = 90^o$	-14.97	-116.54	-343.44	-343.44	-14.97	86.61	-343.44	-343.44

VII. Simulation Results

The operation of a MMC with four cells per arm including cells with power transfer capability has been simulated using Matlab/Simulink. The control block diagram in Fig.10 was used. Only AC voltage imbalance $\Delta Re(v_{ac})$ was used, as it allows to transfer more power than DC voltage imbalance.

Fig. 11 shows the response in two different scenarios, with purely active and reactive power in the AC port respectively. The AC power command follows a ramp until t=0.1sec. At t=0.3 sec, the cells with power transfer capability start injecting power according to a ramp too, reaching their rated power at t=0.4 sec. The AC port active and reactive powers are not affected, since they are controlled to be constant. Consequently, power injected by the cells affects to the DC power, which is controlled through the circulating current. Capacitor voltage for the two cells transferring power, v_{cu1} and v_{cu5}, shows a small transient disturbance, which is readily controlled by the arm balancing control and the capacitor voltage balancing.

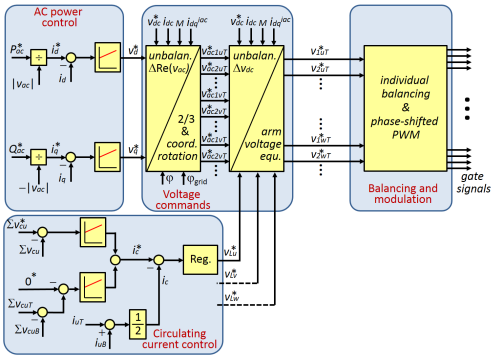

Fig. 10. Proposed MMC control.

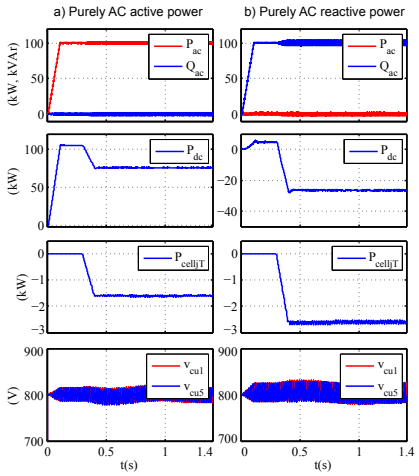

Fig. 11. Simulation results. MMC with four cells per arm (N=4). From top to bottom: AC active and reactive powers, DC port power, power injected by one cell, capacitor voltages for cells #1 and #5 of phase u. a) $P_{ac} = 100$ kW, $Q_{ac} = 0$ kVA, $M = 3$, $M \cdot P_{cell} = -28.8$ kW; b) $P_{ac} = 0$ kW, $Q_{ac} = 100$ kVAr, $M = 2$, $M \cdot P_{cell} = -31.2$ kW.

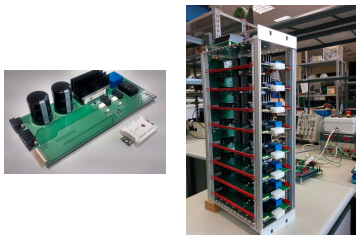

Fig. 12. Eight cell, single-phase, experimental MMC prototype.

Table V shows the real and imaginary component of the cells AC voltage vectors for the two cases shown in Fig. 11, without and with cell power transfer. It is noted that real component of the voltage for cells transferring power v_{ac1Td}, increases , the imaginary component v_{ac1Tq} remaining constant. Cells which do not inject decrease the real component of their AC voltage v_{ac4Td}, which is required to maintain the power balance and to provide the required AC voltage (22).

VIII. Experimental Results

Preliminary experimental verification of the proposed control methods for MMCs using cells with power transfer capability have been realized using an eight cell, single-phase MMC (see Fig.12). The details of the prototype are shown in Table VI. Two cells, one in the top arm and one in the bottom arm, have power transfer capability. DABs are used to transfer power to the cells [22]-[23] (see Fig. 2 c).

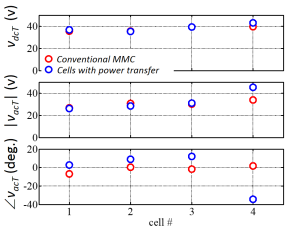

Fig. 13. Experimental results. DC and AC cell voltages for cells #1 to #4 when $P_{cell} = 0.2P_{ac}$, without explicit selection of Δv_{dc} and $\Delta Re(v_{ac})$.

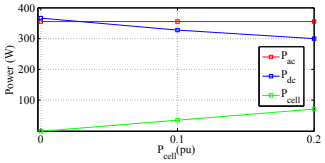

Fig. 14. Experimental results. AC, DC and cell powers for three different cases of P_{cell}. No explicit selection of Δv_{dc} and $\Delta Re(v_{ac})$ is implemented.

A control strategy based on a conventional sorting algorithm has been used (see Section VI-A). Fig. 13 shows AC and DC cell voltages when the power transferred by the cells is $P_{cell} = 0.2pu$. It is observed from this figure that the sorting algorithm responds varying the magnitude and angle of cell AC voltage, the DC voltage being barely affected. Fig. 14 shows DC, AC and cell powers for three different values of P_{cell}. Since the AC power is controlled to be constant, the power transferred by the cells result in a decrease of the power absorbed from the DC port of the MMC.

TABLE VI
EXPERIMENTAL SETUP

Power switches	600V/23A
Cell capacitor/Arm inductance	2000uF/1mH
Cell voltage/DC bus voltage	80V/320V
Switching frequency	5Khz

IX. CONCLUSIONS

This paper analyzes the design and control of MMC including cells with power transfer capability. The use of such cells can enhance the functionalities of the MMC, including energy storage integration, connection of low power/low voltage sources/loads, and multiport power converters. However, this requires the development of adequate control strategies, able to cope with the unbalanced operation of the MMC cells.

Mechanisms to control the voltage imbalance needed to transfer power from the cells have been analyzed, as well as the limits of operation, i.e. the maximum power that can be transferred by the cells. A key figure in this regard is the voltage margin between the DC and AC ports of the MMC. A control strategy capable of precisely controlling the power transferred by the cells has been proposed. Simulation and preliminary experimental results have been provided.

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Operation of Modular Multilevel Converters Under Voltage Constraints

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***Abstract*—MMCs are normally designed to operate in the linear region of the PWM. This limits the peak-to-peak phase voltage in the AC port to be lower than the DC port voltage. It is possible to increase the AC voltage beyond this limit by the use of overmodulation strategies. However, this is at the price of an increase in the harmonic content (THD) of the voltages and currents, and consequently, of a decrease of the power quality. While this type of operation is not desired in normal conditions, there are exceptional circumstances in which the MMC could be forced to operate in this mode. These would include transient anomalies, e.g. a temporary decrease of the DC port voltage or a temporary increase of the AC port voltage, or quasi-permanent conditions, e.g. the failure (and subsequent disconnection) of one or more cells in one or more arms of the MMC. Under this circumstances, the voltage margin between the DC and the AC port voltages required for the normal operation of the MMC might be lost. Consequently, the MMC should operate in the overmodulation region, or turned-off otherwise.**

This paper addresses the use of overmodulation techniques in MMC under voltage constraints. Under these circumstances, the MMC control should guarantee stable operation, (i.e. a controlled power transfer between the DC and AC ports with the cell voltages maintained at their target values) and minimize the distortion of the currents, and consequently the adverse effect on the power quality.

***Index Terms*—Modular Multilevel Converter, MMC, overmodulation, power quality, zero sequence voltage**

I. Introduction

Multilevel converters are a suitable option to cope with the new functionalities imposed by the power system operator, like power flow control, high power quality and reduction of transmission losses [1]. Among these, Modular Multilevel Converter (MMC) appears as a promising topology and it is a hot research topic nowadays.

MMC was first introduced one decade ago [2]-[4]. It realizes a bidirectional DC/AC power conversion, sharing the advantages of other multilevel converters: reduced size of filters due to better output voltage wave shape; lower switching losses due to the reduced switching frequency; capability of withstanding large terminal voltages using relatively low voltage power devices. Additionally, it provides attractive features compared to other multilevel topologies, such as modularity (identical cells are piled-up to increase the voltage), and consequently easy scalability; distributed energy storage, therefore eliminating the need of a bulk DC capacitor [2]-[5].

MMCs are normally designed to operate in their AC side in the linear region of the PWM. This limits the peak-to-peak voltage in the AC port to be lower than the DC port voltage. It is possible to increase the AC fundamental component of the voltage beyond this limit by using overmodulation strategies. However, this is at the price of an increase in the harmonic content (THD) of the voltages, and consequently in the currents and power. While this type of operation is not desired in normal operation, there are exceptional cases in which the MMC could be forced to operate in this mode. These would include transient conditions, e.g. temporary decrease of the DC port voltage below its rated value and temporary increase of the AC port voltage above its rated value, or quasi-permanent conditions, e.g. failure (and subsequent disconnection) of one or more cells in one or more arms of the MMC. Under these circumstances, the voltage margin between the DC and the AC port voltages required for the normal operation of the MMC might be lost. Consequently, the MMC will be forced to operate in the overmodulation region to maintain its power transfer capability, or be turned-off otherwise.

This paper addresses the use of zero sequence voltage components and overmodulation techniques in MMCs in the event of a mismatch between the DC and AC ports voltages, with the purpose of guaranteeing stable operation of the power converter, maintaining the power transfer capability between the DC and AC ports and minimizing the distortion of the currents and powers.

This paper is organized as follows. Basic concepts and power balance of the MMC are presented in Section II. Section III analyzes the voltage limits and overmodulation strategies for MMCs. Section IV discuss MMC operation under voltage constraints, while simulation results are presented in Section V. Finally, the conclusions are given in Section VI.

II. MMC Model and Power Balance

The analysis and methods proposed in this paper are specially well suited for three-phase MMCs (see Fig. 1). Furthermore, some of the overmodulation strategies that will be discussed are an extension of already existing methods for other types of three-phase power converters. It is useful therefore to use complex vector cells to represent the AC

This work was supported in part by the Research, Technological Development and Innovation Programs of the Spanish Ministries of Science and Innovation and of Economy and Competitiveness, under grants MICINN-10-CSD2009-00046 and MINECO-13-ENE2013-48727-C2-1-R, and by the European Commission FP7 Large Project NMP3-LA-2013-604057, under grant UE-14-SPEED-604057.

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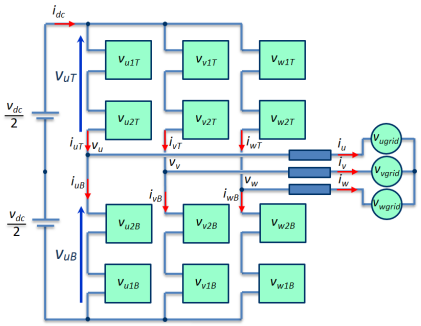

Fig. 1. Schematic representation of 3-phase grid connected MMC.

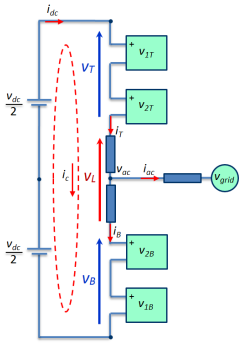

Fig. 2. Schematic representation of the MMC using complex vector notation.

variables of the MMC. These include AC port voltages and currents, as well as the AC component of the top and bottom arms voltages and currents.

The AC voltage and current vectors of the MMC are defined by (1) and (2) respectively, the same transformation can be applied to the AC component of the arms currents and voltages (3)-(6). By doing this, the three-phase MMC in Fig. 1 results in the equivalent MMC using complex-vector cells in Fig. 2.

$$v_{ac} = \frac{2}{3}\left(v_u + v_v e^{j2\pi/3} + v_w e^{j4\pi/3}\right) \tag{1}$$

$$i_{ac} = \frac{2}{3}\left(i_u + i_v e^{j2\pi/3} + i_w e^{j4\pi/3}\right) \tag{2}$$

$$v_T = \frac{v_{dc}}{2} - v_{ac} - \frac{v_L}{2} \tag{3}$$

$$v_B = \frac{v_{dc}}{2} + v_{ac} - \frac{v_L}{2} \tag{4}$$

$$i_T = i_{dc} + \frac{i_{ac}}{2} \tag{5}$$

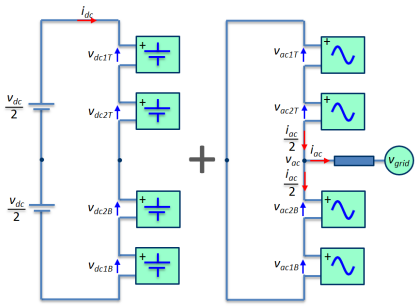

Fig. 3. DC (left) and AC (right) subcircuits of the MMC.

$$i_B = i_{dc} - \frac{i_{ac}}{2} \tag{6}$$

It is useful for analysis purposes to separate the MMC in Fig. 2 into its DC and AC subcircuits, as shown in Fig. 3. The voltage drop in the arm inductors has been neglected for simplicity. It is observed that the cells are series connected in the DC subcircuit (Fig. 3-left), the overall DC voltage of the cells corresponding to the DC voltage of the MMC (7).

$$v_{dcnT} = v_{dcnB} = \frac{v_{dc}}{2N};\ \ n = 1:N \tag{7}$$

On the contrary, for the AC voltage subcircuit (Fig. 3-right), top and bottom arms are connected in parallel, the corresponding AC cell voltages being (8) and (9) respectively.

$$v_{acnT} = \frac{-v_{ac}}{N} \tag{8}$$

$$v_{acnB} = \frac{v_{ac}}{N} \tag{9}$$

The AC current equally splits between the two arms. The resulting top and bottom arm currents are (5) and (6), while the circulating current is defined as (10). For the sake of simplicity, it is assumed that the circulating current does not contain harmonics [8][10], being therefore equal to the DC current.

$$i_c = \frac{i_T + i_B}{2} = i_{dc} \tag{10}$$

The limited energy storage capability of the MMC imposes that the power in the DC port has to be equal to the active power in the AC port (11) (losses neglected), with "*" standing for the complex conjugate. To achieve this, the DC current is controlled to adjust the power between DC and AC ports. The DC power in the cells (12) has to be therefore equal to the AC power (13) on average.

$$P_{dc} = v_{dc} \cdot i_{dc} = P_{ac} = Re\left(v_{ac} \cdot {i_{ac}}^*\right) \tag{11}$$

$$P_{dcnT} = P_{dcnB} = \frac{v_{dc}}{2N} i_{dc} \tag{12}$$

$$P_{acnT} = P_{acnB} = Re\left(\frac{v_{acT}}{N}\frac{{i_{ac}}^*}{2}\right) = Re\left(\frac{v_{acB}}{N}\frac{-{i_{ac}}^*}{2}\right) \quad (13)$$

In addition, cell capacitor voltages must be kept at their target value. This is done by balancing methods, e.g. sorting algorithms [8][9] or individual balancing [7].

III. Voltage Limits and Overmodulation Strategies for MMCs

A. MMC Voltage limits

A key figure in the design and operation of MMCs is the relationship between the DC and the AC voltages. Fig. 4 shows the MMC AC side voltage limits using complex vector notation in the $d-q$ plane.

A MMC with four cells per arm ($N = 4$) is considered. It is noted that this does not imply any lost of generality. Vertexes correspond to the voltage vectors that can be physically produced by the MMC, outer hexagon corresponding to the maximum voltage. As for other types of three-phase power converters, the maximum AC voltage that can be achieved will depend on whether zero sequence voltage components are used or not. The outer circle represents the voltage limit when a zero sequence voltage (triplen harmonics) [6] is added to the phase voltages. This corresponds to the physical voltage limit of the MMC in linear operation. The inner circle represents the voltage limit when triplen harmonics are not used. The use of triplen harmonics is seen to increase the voltage limit by an amount of $\approx 15\%$. However, this is at the price of injecting a zero sequence voltage between the DC port and the neutral voltage of the AC port. The peak value of the phase voltage in the AC side of the MMC is equal to the magnitude of the AC voltage complex vector (1), being limited to $v_{dc}/\sqrt{3}$ when triplen harmonics are added.

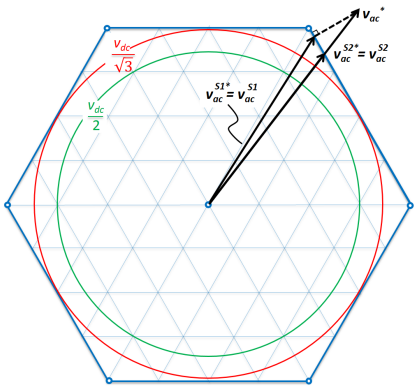

Fig. 4. Voltage limits and overmodulation strategies for a grid-connected MMC with 4 cells per arm. Outer circle: voltage limit in linear operation (requires the injection of zero sequence components to the individual phase voltage commands). Inner circle: voltage limit in linear operation without zero sequence voltage injection.

One difference between conventional three-phase converters and the MMC regarding the use of zero sequence voltage components, is that while in the first case the zero sequence voltage is obtained from a set of three phase voltages [6], for the MMC case six voltage references exist, i.e. top and bottom voltages (14)-(15) for phases u, v and w.

$$v_{xT}^* = v_{dcT} - v_{acxT}^* - \frac{v_{Lx}^*}{2} \quad x = u, v, w \quad (14)$$

$$v_{xB}^* = v_{dcB} + v_{acxB}^* - \frac{v_{Lx}^*}{2} \quad x = u, v, w \quad (15)$$

DC port voltage vs. AC port voltage is a key design aspect of the MMC. It is therefore useful for analysis and comparison purposes to define the ratio between the AC and DC voltages. This ratio indicates *how much* of the available DC bus voltage is actually used to produce the AC voltage. For a given v_{dc} and v_{ac}, this ratio is (16) if triplen harmonics are added to the phase voltages, and increases to (17) (i.e. less margin between v_{dc} and v_{ac}) if triplen harmonics are not used.

$$R_{thi(pu)} = \frac{\sqrt{3}\cdot|v_{ac}|}{v_{dc}} \quad (16)$$

$$R_{no\ thi(pu)} = \frac{2\cdot|v_{ac}|}{v_{dc}} \quad (17)$$

Fig. 5 shows the reported ratio R_{thi} (in %) vs. MMC power for already installed MMCs (or under development). It is interesting to note the dispersion of the data shown in this figure. Values of R_{thi} significantly lower than 100% means that the MMC has a large safety margin between its DC and AC ports voltages, and that therefore can likely operate within its voltage limits even in the event of anomalies, e.g. DC voltage lower than expected, or AC voltages larger than expected. Also this opens the opportunity to implement redundancy-based fault tolerant designs. I.e. it is possible to disconnect or by-pass faulty cells, without compromising the operation of the MMC. However, small values of R also implies a misuse of the power devices, and of the cells in general. On the contrary, for values of R closer to 100, a better use of the cells and power devices is made, but at the price of an increased risk of forcing the MMC to operate without the required safety voltage margin. Finally, values of $R > 100$ will

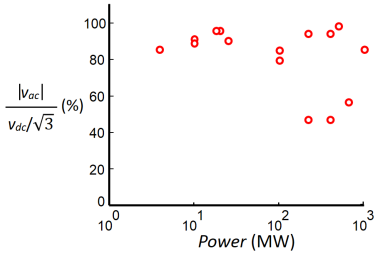

Fig. 5. AC-to-DC voltage ratio R vs. power of already installed (or under development) MMC.

impede the normal operation of the MMC. Depending on the severity of this anomaly and its duration, these effects can be manageable by the MMC control algorithms, or can produce an inadmissible degradation of the voltages (and currents) or even unstable operation, and consequently the disconnection of the MMC.

B. Overmodulation strategies

It is possible to increase the fundamental AC voltage supplied by the MMC with respect to the voltage limit in linear operation (outer circle in Fig. 4) by operating the MMC in the overmodulation region. This occurs whenever the commanded voltage vector is beyond the limit of $v_{dc}/\sqrt{3}$. Two different cases can be distinguished:

- If the AC voltage command $v_{ac}^{\star}$ is outside the circle limit but within the hexagon limits, then the voltage command (on average) can be feasible.
- If the AC voltage command is outside the hexagon, then then the voltage command is not feasible.

An example of the second case is the voltage command v_{ac}^{*} in Fig.4. Since this voltage command is permanently beyond the limits of the hexagon, it cannot be physically produced by the MMC. When this occurs, different strategies can be used to obtain a feasible voltage vector [6]:

- *Minimum phase error*: With this strategy, the magnitude is reduced to match the hexagon limits, the phase angle of the resulting voltage vector remaining unchanged. This corresponds to v_{ac}^{S2} in Fig. 4.
- *Minimum error*: The vector command is projected on the hexagon, the resulting feasible voltage vector being v_{ac}^{S1}. It is noted that both magnitude and phase of the resulting voltage vector are modified with respect to the voltage vector command. This corresponds to v_{ac}^{S1} in Fig. 4.

Minimum phase error and *Minimum error* strategies allow to increase the fundamental component of the AC voltage compared to linear operation. However, this is at the price on an increase in the harmonic content of the AC voltage, and consequently of the currents and power. The physical limit for the fundamental component of the AC voltage would occur when the MMC operates in a six-step. The ratio R_{thi} can be increased with respect to the case of linear operation by an amount of $\approx 10\%$ in this case. It is noted however that the six-step limit is unlikely to be used in practice, due both to power quality degradation as well as to MMC controllability issues.

C. Overmodulation methods with sine-triangle modulators

Space vector modulation representation has been used in the preceding discussion on overmodulation methods. However, sinte-triangle modulators are often used in MMCs. The dc-bus utilization by sine-triangle modulators can be increased to that of SVM through the use of zero sequence voltage components [6]. Centering the phase voltages with respect to the triangular carrier limits extends the maximum voltage in linear operation by $\approx 15\%$. After injecting the homopolar component, the modulator will come into overmodulation when two phase

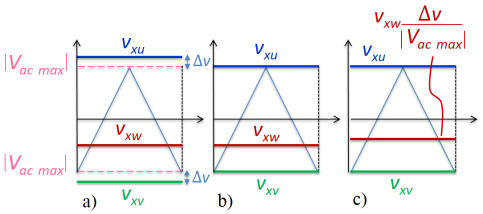

Fig. 6. a) zero sequence voltage injection. Unlimited voltage vector; b) *Minimum error* (v_{ac}^{S1} in Fig. 4); c) *Minimum phase error* (v_{ac}^{S2} in Fig. 4).

voltages touch the triangular carrier limits. This corresponds to touching the hexagon limit in Fig. 4, it is schematically shown in Fig.6. If after injecting the homopolar component two phase voltages go outside the triangular carrier bounds (v_{xu} and v_{xv} in Fig. 6-a), they will be physically limited (v_{xu} and v_{xv} in Fig. 6-b and Fig. 6-c). If the third phase voltage remains unchanged (v_{xw} in Fig. 6-b), the resultant voltage vector will correspond to the minimum error SVM voltage vector. If it is reduced proportionally to the other two components reduction (v_{xv} in Fig.6-c), the minimum phase error SVM voltage vector is obtained.

IV. Operation of MMC Under Voltage Constraints

MMCs are designed to operate in the linear region. However, under exceptional circumstances, they can be forced to operate with voltage restrictions, i.e. without enough voltage in the DC link to provide the desired AC voltage. Three types of events that result in values of a voltage margin $R_{thi} > 1$ are considered:

- Decrease of the MMC DC voltage and/or increase of the MMC AC voltage (e.g. due to an increase of the grid voltage in grid connected MMCs) with respect to their rated values. Since the duration of such anomalies in the DC and/or AC voltages is in principle undefined, the MMC might need to withstand these operating conditions during relatively large periods of time.
- Sudden changes in the AC power, either due to changes in the power commands, or to disturbances in the AC side of the MMC. If this occurs, transients in the MMC voltage commands can produce a temporary lack of voltage. This situation should fade away after a relatively short time, but still will produce a transient disturbance in the operation of the MMC.
- Cell failure. One of the appealing properties of the MMC is its fault-tolerance capability. This can be achieved using redundant cells. If a cell fails in one arm, the remaining cells should be able to produce the commanded AC and DC port voltages and maintain the normal operation of the MMC. Ideally, the damaged cell would be replaced immediately and without discontinuing the operation. However, this might not be always the case in real practice. Failure of a cell in an MMC without spare cells, can force the MMC to operate with voltage

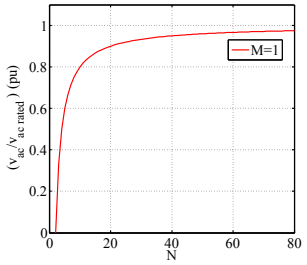

Fig. 7. Reduction of the AC port voltage limit vs. number of cells per arm (N) in the event of one ($M = 1$) faulty cell.

constraints, or otherwise to discontinue its operation. In this case, the duration of the anomalies is in principle undefined, meaning that the MMC might need to withstand this operating conditions during a relatively large period of time.

The response of the MMC to these events will depend on the overmodulation strategy being used, as well as on the capability of the control loops to operate under voltage restrictions. Further discussion on this can be found in the next section.

An special case occurs when a cell failure forces the MMC to operate in overmodulation. The maximum AC port voltage that the MMC can supply as a function of the number of cells per arm N and the number of faulty cells M is given by (18), the voltage decrease in the AC port with respect to the case of no faulty cells being (19).

$$v_{ac} = \left(\frac{1}{2} - \frac{M}{N}\right) v_{dc} \frac{2}{\sqrt{3}} \tag{18}$$

$$\frac{v_{ac}}{v_{ac\ rated}} = \left(1 - \frac{2M}{N}\right) \tag{19}$$

Fig.7 shows the variation of the AC port voltage limit as a function of the number of cells per arm for $M = 1$ (one faulty cell). AC port voltage will reduce proportionally to the number of faulty cells. It should be also remarked that when half the cells in one arm fail (i.e M=N/2), there is no capability to produce AC voltage, since all the voltage is utilized in compensating the DC port voltage v_{dc}.

Two different strategies can be used when damaged cells limit the voltage capability of one phase:

- Operate the MMC asymmetrically, i.e. with different number of cells in the arms/legs.
- Maintain the symmetry among arms and legs, i.e. limit the AC voltage in the other two phases by disabling M cells.

The resulting voltage limits are shown in Fig. 8. Fig. 8-left, shows the case when the MMC is operated with a different number of cells in each leg. Fig. 8-right shows the case when the same number of cells is disabled in all the phases. Comparing Fig. 8-left and Fig. 8-right, it is clear that the MMC can provide a significantly larger AC voltage in the first case,

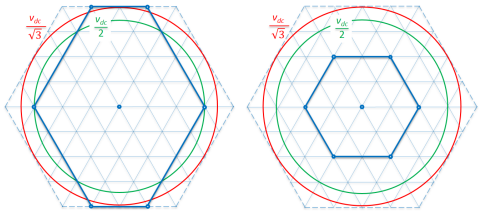

Fig. 8. Overmodulation limits in the case of a faulty cell. Left- Asymmetric legs: $N_u = 3$, $N_v = N_w = 4$ in the top and bottom arms of one leg respectively. Right- Symmetric arms and legs: $N_u = N_v = N_w = 3$.

compared to the second case. However, this will produce an asymmetric behavior of the MMC, the harmonic content of the three phases being different. Simulation results showing this behavior are presented in the next section.

V. Simulation Results

Simulation results using the proposed concepts are presented in this section. The simulation setup consists of a grid connected MMC with four cells per arm ($N = 4$). Active and reactive powers for the AC side are commanded to the control. The same power profile will be used for all the simulations. Active power command increases linearly from 0 to $200kW$ between $t = 0$ and $t = 1.1s$. Homopolar harmonic injection is used.

Fig. 9 shows the AC active power, the fundamental component of AC voltage and the THD of the AC voltage vector, with the converter operating in normal conditions.

Fig. 10 and Fig. 11 show the MMC response when it is forced to operate into overmodulation, using *Minimum error* and *Minimum phase error* methods respectively. It is noted from the figure that the lack of voltage reduces the power transfer capability (P_{ac} is slightly smaller than 200 kW in steady state). However, operation of the MMC is perfectly

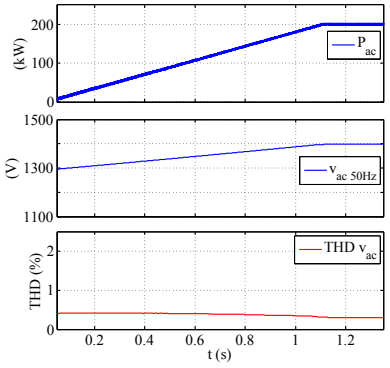

Fig. 9. MMC in normal operation, i.e. without going into overmodulation. From top to bottom: AC active power, fundamental component of AC voltage; THD of AC voltage.

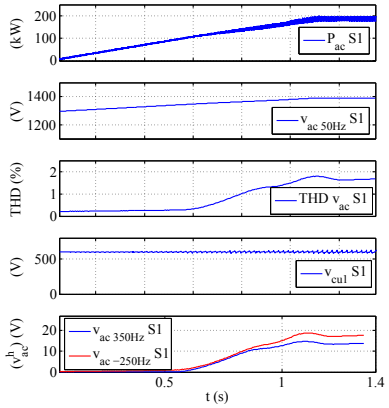

Fig. 10. Simulation results. *Minimum error* ($S1$) overmodulation method. From top to bottom: AC active power, fundamental component of AC voltage, THD of AC voltage, voltage of one cell capacitor, 350Hz and -250Hz components of AC voltage.

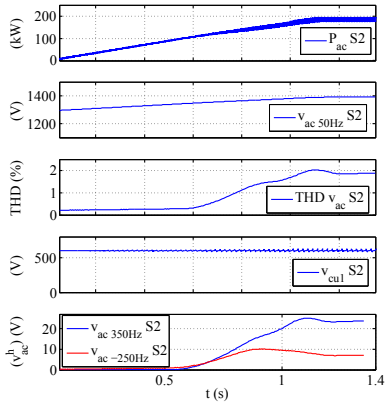

Fig. 11. Simulation results. *Minimum phase error* ($S2$) overmodulation method. From top to bottom: AC active power, fundamental component of AC voltage, THD of AC voltage, voltage of one cell capacitor, 350Hz and -250Hz components of AC voltage.

stable. It is interesting to note that *Minimum error* method (Fig. 10) produces a lower distortion (smaller THD) and can transfer more power, compared to *Minimum phase error* (Fig. 11). It is also observed from the figures that the oscillation of the capacitor voltages slightly increases, but remains under control. The most relevant harmonic components of the AC voltage are at -250Hz and 350Hz, they are also shown in the figure.

It is concluded that both *Minimum error* both *Minimum phase error* saturation methods provide stable operation under voltage constraints. The oscillation of the cells capacitors voltage is maintained within reasonable limits, and without compromising the stability of the MMC.

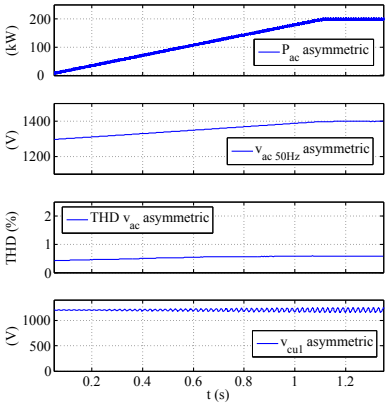

Fig. 12. Simulation results showing the effects of a faulty cell using *Minimum error* overmodulation, for the case of *asymmetric* operation of the MMC.

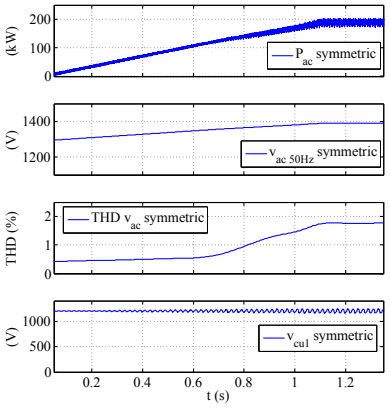

Fig. 13. Simulation results showing the effects of a faulty cell using *Minimum error* overmodulation, for the case of *symmetric* operation of the MMC.

Fig. 12 and Fig. 13 show the results when one cell in one arm fails. This forces the MMC to go into overmodulation. For the *asymmetric* case, the other two phases are not modified. This corresponds to the case shown in Fig. 8-left. For the *symmetric* case, one cell is removed from all the arms. This corresponds to the case shown in Fig. 8-right. As already mentioned, the asymmetric operation allows to obtain a higher output voltage (and consequently to transfer more power), and does not mean larger harmonics in the output voltage, since there is lack of voltage just in some sectors of the hexagon. It is important to note that by using the *asymmetric* case option, more power can be transferred and lower distortion is produced, compared to the *symmetric* case. Consequently, it is proved to be the best option. Similarly to the previous case, the oscillation of the cells capacitors voltage increase but within reasonable limits, and without compromising the

stability of the MMC.

VI. Conclusions

This paper analyzes the operation of the MMC under voltage constraints. This mode of operation can occur due to different reasons, including a decreased DC port voltage, an increased AC port voltage, or the failure of cells in one or more arms. To overcome this situation, it is possible to implement overmodulation techniques. By doing this, the MMC will be able to remain operative, but at the price of a decrease in the power quality.

Simulation results evaluating different overmodulation methods as well as strategies when failure of one cell occurs, have been provided. The combined use of *Minimum error* overmodulation with a *realizable references* strategy in the AC current regulator have been shown to guaranteeing stable operation of the MMC, providing good results.

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Auxiliary Power Supply Based On A Modular Isop Flyback Configuration With Very High Input Voltage

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***Abstract*— This paper proposes a Flyback-based Input-Series Output-Parallel (ISOP) Auxiliary Power Supply (APS), intended to feed the control system of the cells of a Solid-State Transformer (SST). The SST topology is based on a modular Multiport Multilevel Converter (MMC). Energization of the cells auxiliary circuitry is not trivial due to the high voltages involved (tens of kV for the electric power distribution system), most of the commercially available control and driving circuitry not being usable due to the isolation requirements. It is possible to energize the control circuitry from an APS, connected to the cell capacitor voltage. However, in the SST under consideration, cells target DC voltage is in the range of 1.5kV to 2.5kV. Design of an APS capable of feeding the auxiliary circuitry from such high voltage and the required isolation is not trivial. A modular APS using autonomous Flyback converters in Continuous Conduction Mode (CCM) and based on commercial AC adapters is proposed in this paper. The solution is scalable and therefore applicable to cells with larger DC voltages.**

***Keywords*— ISOP, High voltage, APS, DC/DC converter.**

I. INTRODUCTION

Distributed generation has become a necessity due to many economic, environmental and technical reasons. With the increasing energy demand worldwide, energy efficiency has become a crucial consideration, the term "Microgrid" has become very common and the increasing energy demand is intended to be fed by distributed energy resources such as wind and solar installations [1]. The need for bidirectional as well as high-voltage and high-power conversion applications are growing fast to interconnect these new grids with the main grid and increase their reliability leading to the emergence of Flexible AC Transmission Systems (FACTS), High-Voltage DC (HVDC) and Solid-State Transformer (SST).

Conventional Line-Frequency Transformers (LFT) are a key element in the transmission system. While they are cheap and a reliable and a well-established technology, they have limitations regarding functionalities demanded by the power system operator, such as harmonics, reactive power and imbalances compensation, and power flow control. Also, their efficiency can be compromised when operating with low load levels. Solid State Transformers (SSTs) are envisioned as semiconductor based alternative to LFT. SSTs use power converters with fast switching devices, enabling a significant reduction of the volume and weight of the core material. Additionally, they are able to provide advanced functionalities such as power flow control, as well as reactive power, harmonics and imbalances compensation [2]-[5]. Generally speaking, the SST is expected to beat the LFT in terms of power density and much superior functionalities, but it would be inferior in terms of cost, efficiency (full load) and reliability.

The concept of SST has been discussed since 1970 [6]. The SST topology derived from a Multiport Multilevel Converter (MMC) has drawn great attention in the SST research field [7]. The connection of a Dual Active Bridge (DAB) [8]-[11] to each cell capacitor of the MMC provides the capability to transfer power between the primary and the secondary with galvanic isolation [12], [13]. A simplified diagram of the MMC based SST topology is shown in Fig. 1.

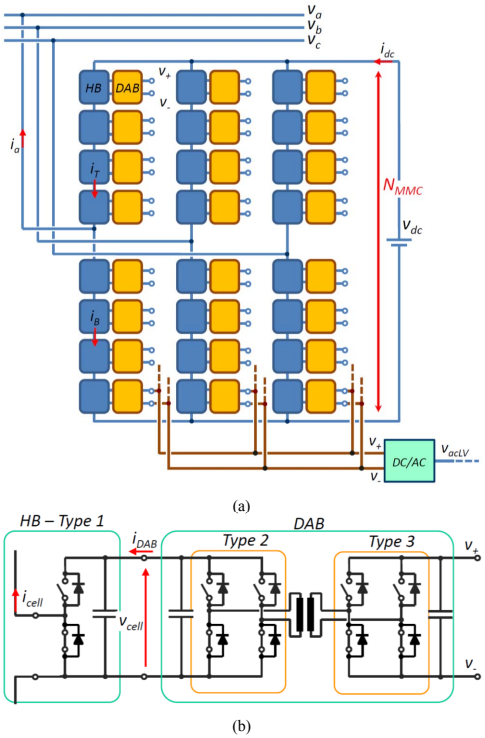
An Auxiliary Power Supply (APS) providing a low-voltage (i.e. 24/15/12V) and low power (in the range of 30-50W) is necessary to feed the control circuitry of each cell (including DAB and MMC cells). Although the proposed APS is intended to feed the control circuitry of a SST, it could be also applied in different modular multilevel topologies.

Actual DC bus voltage of multilevel converters is in the range of 800V-1.5kV, mainly due to the maximum voltage withstood by the switches available in the market (Silicon IGBTs or even SiC MOSFETs). However, recent developments of 10-15kV SiC MOSFETs and IGBTs have enhanced the scope of dc bus voltages of 7kV and above [14]. In order to address the increase of the voltage in DC links, a modular APS is proposed in this paper. Thanks to the modularity, the APS can be used in cells with high voltage DC links by increasing the number of modules.

The main requirements of the APS for the modular multilevel topologies can be summarized in two:

- On one hand, isolation between primary and secondary of the APS is needed. Moreover, the input of the APS is the DC bus voltage of the cell, usually over 1kV and probably higher in the future. Due to the high input voltage of the DC bus, in addition to the high isolation required, the conversion ratio of the APS is also very high, usually higher than 100.

- On the other hand, the DC bus voltage of each cell is not referred to ground. The DC link of several cells can be dozens of kV over the global reference. Consequently, the control circuitry of all the stacked MMC-DAB cells cannot be connected to the same DC voltage supply, due to very high isolation requirements, as a relatively large number of cells need to be piled-up to provide the required HV AC side voltage.



(a)

(b)

Fig. 1. (a) Representation of the proposed SST topology. (b) MMC cell and DAB for each cell of the MMC-based SST. Cell capacitor voltage (v_{cell}) is used to feed the proposed APS.

As an example, the particular application of a SST connecting two AC grids of 24kV and 400V respectively is analyzed in this paper (one of the configurations being considered within the SPEED project [15]). A cell voltage v_{cell} = 1.4kV was selected, which is equal to the DAB voltage in the HV side and the input voltage of the APS proposed in this paper. The DC link voltage in the LV side is 750V. The DABs are designed for rated power of 10kW. Commercially available APSs do not provide the required isolation for this kind of application. The solution proposed in this paper integrates a modular APS in each MMC-DAB cell. A modular Input-Series Output-Parallel (ISOP) structure based on a Flyback topology was chosen to accomplish with the HV at its input and low output power requirements [16].

This paper is organized as follows. In Section I, the main application and requirements of the APS under development has been mentioned. In Section II, the analytical equations of the proposed Flyback-Based Modular ISOP converter are stated and simulation results are presented. In Section III, experimental results using two different prototypes are shown. Finally, conclusions are drawn in Section IV.

II. Analysis Of The Flyback-Based Modular ISOP Converter

To feed the control circuitry of each cell (including DAB and MMC cells) of a SST topology fulfilling the previously detailed isolation requirements, an APS providing a low voltage and low output power from the cell capacitor voltage (v_{cell}) is proposed.

Different solutions are proposed in the literature. For example, two quite expensive and complex methods are provided for auxiliary power supply for SST in [17]. Also, resonant topologies, as series half bridge structure, and three-level structure are analyzed in [18] and [19], but they are limited when the DC bus voltage and consequently their input voltage is increased. To get over the actual increase in the DC bus voltage level, ISOP structures are evaluated in [20], which can be used for very high voltage thanks to the possibility of increasing the number of modules connected in series in the input.

In this paper, an autonomous, simple and cheap Flyback-based ISOP converter is proposed and analyzed. The maximum input voltage of the converter can be easily increased, using Flyback converters, thanks to their autonomy. In Section III two different prototypes are proposed to validate the modular concept. Four Flybacks converters connecting their inputs in series and their outputs in parallel (ISOP configuration) compose the definitive APS prototype intended to feed the control circuitry of the SST. This configuration is used as an example to validate the proper operation of the proposed structure with an input voltage of 1400V (the voltage at the MMC cell, v_{cell}) and an output voltage of 15V. It is important to say that each Flyback operates in open loop configuration. All the simulation and analytical results presented in this section have been obtained using the configuration and specifications previously mentioned.

The main challenge faced by the ISOP configuration is to achieve a balanced Input Voltage Sharing (IVS) and Output Current Sharing (OCS). Flyback converters are proposed for each module because they are cheap, reliable, use a simple topology, provide galvanic isolation and have a high conversion ratio. In fact, low power commercial AC/DC adapters available on large scale can be adjusted to meet the requirements. To avoid additional control circuitry (mainly the feedback loop) and to obtain a load-independent output voltage, open loop and CCM operation are selected. The unregulated output voltage will be determined by a fixed duty cycle, the turn ratio of the transformer and the input voltage.

Analytical study of the converter topology to proof the IVS and OCS concept will be performed. Simulations of the switching and averaged model (Fig. 2) also will be performed to confirm the correctness of the model.

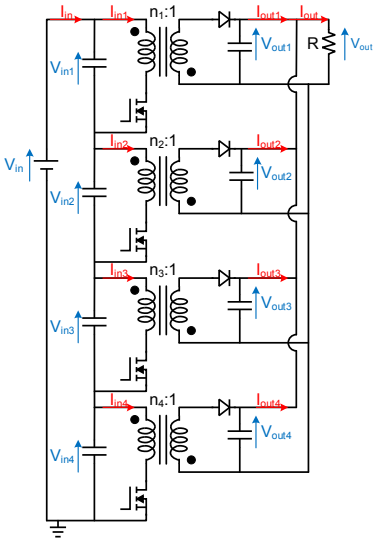
A. *Analytical expressions of the Flyback-based ISOP converter*

Traditionally, in an ISOP configuration with paralleled outputs, Discontinuous Conduction Mode (DCM) operation is preferred, as in this mode of operation the converter works as a current source and it is easy to parallelize their outputs [21], [22]. The main disadvantage of the DCM is that the ratio between input and output voltage depends on the load. In addition, rms currents and conduction losses are higher. On the other hand,

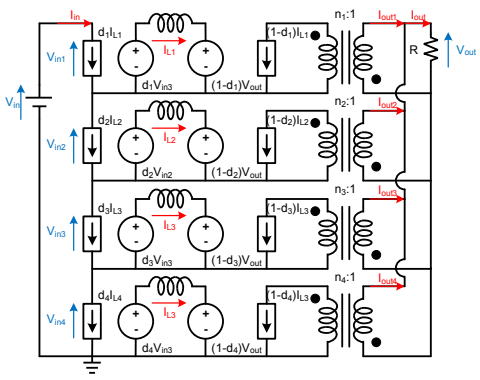
with CCM, the output voltage of a Flyback is constant for a given input voltage and a duty cycle, allowing open loop operation if the input voltage is controlled (as a theoretical DC transformer, i.e. a DCX).

To validate the operation of Flyback modules in CCM in an ISOP configuration and an acceptable IVS and OCS, the input voltage and output current equations are analyzed. Since the average inductor voltage over one switching cycle should be zero [23], the input voltage is given by:

$$V_{in} = \frac{V_{out} \cdot n \cdot (1-d)}{d}, \quad (1)$$



(a)



(b)

Fig. 2. Simulation models: (a) switching and (b) averaged.

being n the transformer turns ratio, V_{in} the input voltage, V_{out} the output voltage and d the duty cycle. Generalizing the equation for the ISOP topology, where the output voltage is the same in all converters, and using i as the number of the module, the input voltage of each module is given by:

$$V_{in_i} = \frac{V_{out} \cdot n_i \cdot (1-d_i)}{d_i}. \quad (2)$$

To estimate the input voltage of each converter in an ISOP configuration it is useful to define the parameter N_i (used as a figure of merit to validate IVS and OCS), given by:

$$N_i = \frac{d_i}{n_i \cdot (1-d_i)}. \quad (3)$$

Using (3) in (2), the input voltage can be calculated by:

$$V_{in_i} = \frac{V_{out}}{N_i}. \quad (4)$$

The output current of each Flyback converter is given by:

$$I_{out_i} = (1-d_i) I_{L_i} n_i, \quad (5)$$

being I_{Li} the average current through the Flyback's magnetizing inductance. Due to the ISOP configuration, and considering zero the average current through each input capacitor over one switching cycle, the input current of the ISOP converter is the input current of each Flyback converter, $I_{in} = I_{in_i}$. The average current through each magnetizing inductance can be obtained by:

$$I_{L_i} = \frac{I_{in}}{d_i}. \quad (6)$$

Assuming there are no converter losses $P_{in} = P_{out}$, the input current can be written as:

$$I_{in} = \frac{{V_{out}}^2/R}{V_{in}}, \quad (7)$$

where R is the value of the load.

Finally, the output current of each module can be defined by:

$$I_{out_i} = \frac{{V_{out}}^2 \cdot n_i \cdot (1-d_i)}{R \cdot V_{in} \cdot d_i}. \quad (8)$$

It is important to say that commercial transformers can guarantee similar turn ratio (n) in all the Flyback converters with an acceptable tolerance (±10% for resistance and inductance values and ±1-2% for turn ratio [24]). Consequently, taking into account (2) and (8) both depending on d_i and n_i, IVS and OCS can be easily achieved by only controlling d_i.

B. Simulation results (switching and averaged model)

Switching and averaged models of the Flyback-based ISOP configuration converter have been simulated using LTSpice (Fig. 2). TABLE I shows the main specifications of the Flyback converters that composes the ISOP converter used for the simulations. These specifications match with the scenario previously mentioned (i.e. SPEED project). It is seen that some dispersion among converters (based on the differences observed in the developed prototypes that will be described in Section III.A) has been included. The value of the parameter N (determine by d and n) is also included. The similarity of N_i in all the Flyback converters determines the proper IVS and OCS.

TABLE II shows the results obtained using the switching and averaged simulation (Fig. 3) and the analytical model. Good agreement between simulation and analytical results and good

OCS and IVS exist. Some differences arise between simulations and results because model of components closer to real behavior have been used in the switching simulation, while in the average simulation all the components are ideal. As can be seen the input voltage in Flyback 3 is considerably lower, mainly due to its higher value of *N*. In Section III, TABLE IV shows that Flyback 3 also gives the highest experimental output voltage (as can be predicted using (4)).

TABLE I. SPECIFICATIONS OF THE CUSTOMIZED FLYBACK CONVERTERS THAT COMPOSE THE ISOP CONFIGURATION

Flyback	**1**	**2**	**3**	**4**
L (mH)	20.838	20.28	25.503	21.195
d	0.295	0.296	0.312	0.297
n	9.89	9.88	10.31	9.84
N	0.0423	0.0425	0.044	0.0429
f_{sw} (kHz)	100	100	100	100

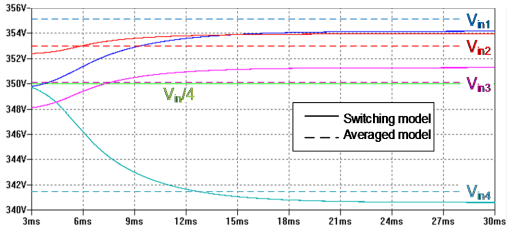


Fig. 3. Switching and averaged simulation models results.

TABLE II. SIMULATION AND ANALITICAL MODELS RESULTS

Common specifications				
V_{in} (V)	1400		**R (Ω)**	6
Switching model results				
I_{in} (mA)	30.5		**P_{in}(W)**	42.7
V_{out} (V)	15.04		**P_{out}(W)**	37.69
Flyback	**1**	**2**	**3**	**4**
V_{in} (V)	354.17	353.96	340.59	351.28
I_{out} (A)	0.635	0.634	0.607	0.630
Averaged model results				
I_{in} (mA)	26.9		**P_{in}(W)**	37.66
V_{out} (V)	15.03		**P_{out}(W)**	37.64
Flyback	**1**	**2**	**3**	**4**
V_{in} (V)	355.19	353.13	341.66	350.02
I_{out} (A)	0.635	0.632	0.611	0.626
Analytical model results				
V_{in} (V)	355.38	353.34	341.57	350.24
I_{out} (A)	0.636	0.632	0.611	0.627

III. EXPERIMENTAL PROTYPES AND EXPERIMENTAL RESULTS

To develop the Flyback-based ISOP configuration converter two different approach have been developed in order to demonstrate that this idea is easily implemented on commercially available structures that can be modified without difficulty as they are well known.

On one hand, a commercial AC adapter is used to obtain individual Flyback converters. These AC adapters usually include Flyback converters working in DCM and closed loop, and consequently some modifications have been introduced to achieve the open loop operation mode in CCM. As an example, three of these converters are used to obtain a Flyback-based ISOP converter with an input voltage (V_{in}) of 600V. This value was selected because each of the three converters were modified to work in open loop in CCM with an input voltage of 200V each.

On the other hand, customized Flyback converters have been developed, mainly to increase the input voltage of each individual Flyback (V_{ini}) and their range of operation in CCM. With four of these customized converters, a 1500V input voltage Flyback-based ISOP converter is developed and tested.

Obviously, in both cases, thanks to the autonomy of each Flyback converter, V_{in} can be easily increased by connecting more Flyback converters.

A. Using a modified commercial AC adapter

1) Individual Flyback converter

Initially, individual Flyback converters were obtained by introducing some modifications to a commercial AC adapter with an integrated current mode PWM control IC (OB2236). The input rectifier was removed, being the DC input voltage directly applied to the input capacitor. The OB2236 IC is self-powered from its input voltage (V_{ini}). The closed loop circuitry used to regulate the output voltage of the AC adapter is removed and the converter is controlled in open loop applying a constant voltage to the feedback input pin of the IC. The operation in CCM is obtained by increasing the switching frequency.

The specified commercial AC adapter (Fig. 4) is selected to guarantee similar performance among them, however some differences exists due to the tolerances in the manufacturing process. The input voltage of each Flyback was limited to 200V because the converter is not optimized for the selected switching frequency and the aim is not entering in DCM.

2) Flyback-based ISOP converter

A 50W prototype has been built using three Flyback converters. As has been previously mentioned, the total input voltage is 600V. Fig. 5 shows the experimental waveforms of the total input voltage (V_{in}) and the input voltage distribution in each Flyback converter (V_{ini}). TABLE III shows the input voltage and output current distribution. It is seen that the input voltage and the output current of Flyback 1 are considerably lower due to its lower turn ratio, which implies a higher value of N_i. The experimental results are in good agreement with the analytical and simulation results. The small differences are mainly due to the low efficiency (<75%) of each Flyback converter.

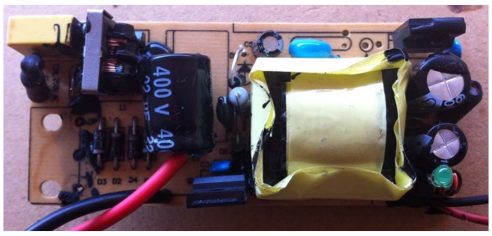


Fig. 4. Commercial Flyback adapted for the ISOP modular converter.

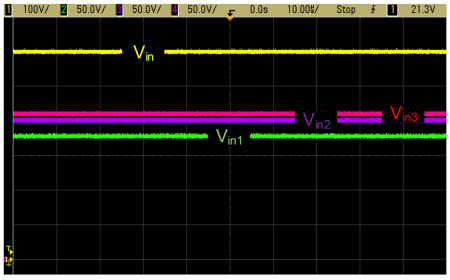


Fig. 5. Experimental waveforms of the input voltage distribution.

TABLE III. IVS AND OCS EXPERIMENTAL AND ANALYTICAL RESULTS WITH THREE OF THE MODIFIED AC ADAPTERS

Iin (A)	0.127	**Pin(W)**	76.2
Vout (V)	12.8	**Pout(W)**	49.65
Flyback	**1**	**2**	**3**
Vin (V)	181	208	211
Iout (A)	1.14	1.34	1.4
Analytical model results			
Vin (V)	190.87	203.19	206.06
Iout (A)	1.40	1.49	1.51

B. Using customized Flyback converters

1) Individual Flyback converter

As mentioned before, in order to increase the input voltage of each individual Flyback and to increase the range of operation in CCM, also four customized Flyback converters have been developed (Fig. 6 shows one of the four customized Flyback).

One of the key points taken into account during the design was achieving a low cost manufacturing prototype, since this is the goal of any commercial APS. In fact, the estimated price of each of the proposed prototypes (considering materials and PCB) is below $5.

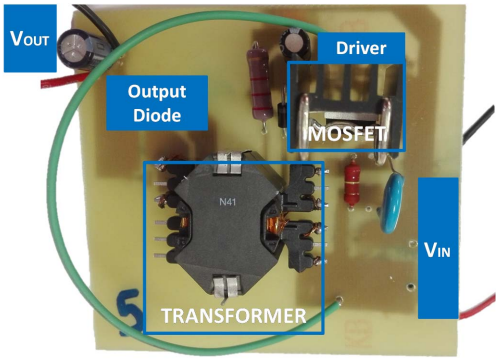


Fig. 6. Customized Flyback prototype developed for higher input voltage

In this case, the current mode standby PWM control IC NCP1271 has been used [25]. This controller allows a fixed-frequency operation of 100 kHz (with some jittering for EMI purposes), as well as, overload, overvoltage, and over-temperature detection, and high voltage start-up. With this controller, a fixed duty cycle (d) can be set, only varying due to the tolerances of the components of the device, itself.

The autonomy of the Flyback converter is mainly provided by the in chip startup circuit implemented in the selected IC. During startup, the supply voltage is provided by the HV pin. This pin is capable of supporting up to 500V, so it can be connected directly to the input voltage of each cell of the ISOP structure (V_{inj}). This pin connects to a current source that charges the decoupling capacitor to its threshold. Once the controller turns on, the transformer auxiliary winding delivers the required charge to the decoupling capacitor and the startup system is turned off.

In the typical application circuit of the IC NCP1271, the duty cycle is usually controlled in closed loop using an optocoupler connected to the FB pin. In the proposed prototype, a feedback loop is not used. The open loop operation is easily implemented connecting a resistor between the FB pin and ground. The value of this resistor will directly determine the fixed duty cycle (d). However, it is also necessary to remove the sense resistor in order to cancel DCM.

Regarding the switch, a 900V / 4A MOSFET has been selected (FQP4N90C of Fairchild [26]). The semiconductor is over-dimensioned in order to withstand possible overdumping when applying input voltages from up to 450V together with duty cycles close to 30%. In commercial AC adapters, also similar MOSFETs are used, because no significant differences in cost exist compared with lower voltage semiconductors.

Concerning the transformer, a thorough 3-winding design has been put into practice. For a nominal input voltage of 350V, output voltage of 15V, a frequency of 100kHz and a duty cycle of 30%, the transformer turns ratio must be around 9.9, and the magnetizing inductance needed must be bigger than 18mH in order to guarantee CCM operation.

The main effort in the design of the transformer is put in increasing the range of CCM operation of the Flyback converter. As has been previously mentioned, the CCM operation has to be maintained to keep the output voltage constant for a given input voltage and a given duty cycle. The transformer has been designed to keep the CCM operation for loads as low as 3W. If it is needed to guarantee the CCM operation for lower loads, even for open circuit operation, a minimum load that ensures a consumption of 3W should be used.

A RM10 and N41 core material were selected, together with a six-layer interleaved configuration among windings, to achieve a good relation among leakage and magnetizing inductances, as well as, low resistance and mutual capacitance values, without increasing the size of the component.

Once each Flyback is developed, they are fully tested to validate their proper operation. All the Flyback converters have been developed as similar as possible, but due to tolerances in the components, especially the IC, some differences in the output voltages given by each Flyback is measured. The proper IVS and OCS will be mainly determined by the differences in the parameter N_i and consequently in the output voltage of each Flyback when the same input voltage and output power is applied. TABLE IV shows the main parameters of each Flyback converter in a given operation point.

Efficiency is not a key point during the design of the transformer or the selection of components of this converter, since power losses are trifling compared to the power managed in these kind of applications.

TABLE IV. EXPERIMENTAL RESULTS OF EACH CUSTOMIZED FLYBACK WORKING INDEPENDENTLY

Common operation point				
V_{in} (V)	350		**R (Ω)**	30
Particular measurements				
Flyback	**1**	**2**	**3**	**4**
I_{in} (mA)	31	30	33	31
V_{out} (V)	15.27	15.17	15.63	15.22
I_{out} (A)	0.518	0.515	0.531	0.517

TABLE V. IVS AND OCS EXPERIMENTAL RESULTS WITH FOUR OF THE CUSTOMIZED CONVERTERS

I_{in} (mA)	36		**P_{in}(W)**	50.39
V_{out} (V)	14.99		**P_{out}(W)**	37.96
Flyback	**1**	**2**	**3**	**4**
V_{in} (V)	352.2	356.1	338	353.4
I_{out} (A)	0.642	0.651	0.6	0.639

1) Flyback-based ISOP converter

Using four customized Flyback converters a 1500V input voltage Flyback-based ISOP converter is developed and tested in different operation points (input voltages from 1200V to 1500V and output power from 35W to 55W). As an example, TABLE V shows the input voltage and output current distribution operating with an input voltage of 1400V and an output power of 38W (these specifications are also used to obtain the simulation results show in TABLE II)In Fig. 7 three different characteristics of the Flyback-based ISOP converter are shown. The startup is captured to verify that there is not important overvoltage at the input of each Flyback converter and the input current is shared, even when each converter starts up and begins to transfer power. In addition, the voltages at the input of three of the four Flyback converters, all of them referred to the same ground, are shown to check a good IVS. Finally, the output voltage is included to validate that it is proportional to the input voltage.

Finally, Fig. 8 shows the voltages at the input of the four Flyback converters, all of them referred to the same ground.

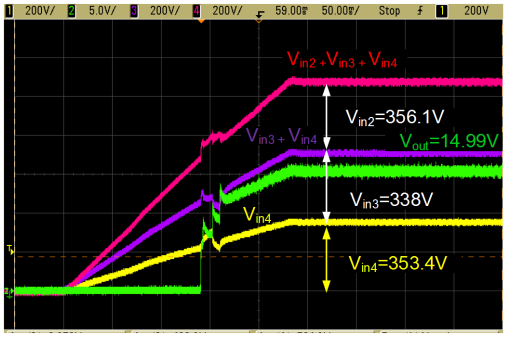


Fig. 7. Experimental waveforms during startup: input voltage distribution and output voltage.

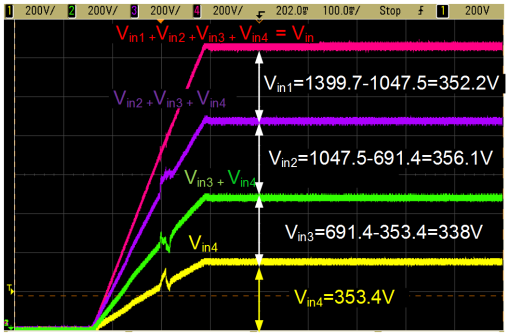


Fig. 8. Experimental waveforms of the input voltage distribution of the four Flyback converters.

IV. Conclusions

An APS intended to feed the cells of a modular SST is presented in this paper. The proposed solution uses a modular ISOP connection of autonomous Flyback converters operating in CCM and in open loop. A modular solution allows the use of the APS in cells with high voltage DC links by increasing the number of Flyback converters.

The validation of the proposed topology and control strategy has been confirmed by simulation and experimental results. The experimental results have been obtained using two different approach. On one hand, a modified commercial AC adapter has been used to develop the Flyback-based ISOP converter to show the flexibility of the topology. On the other hand, a customized Flyback converter was designed to perform the final prototype of a Flyback-based ISOP converter with an input voltage of 1400V. It was tested to evaluate the IVS and OCS at high voltage.

It has been shown that, assuming a good similarity between all the Flyback converters (mainly in the value of *N*) that compose the ISOP configuration, a proper IVS and OCS can be obtained.

Acknowledgment

This work was carried out by funding from the Government of Spain through projects DPI2013-47176-C2-2-R, MINECO-15-DPI2014-56358-JIN and the grant FPI BES-2014-070785, through funding from the Government of Asturias through the project FC-15-GRUPIN14-143 and FEDER funds, and thanks to the project of the European Commission “Silicon Carbide Power Electronics Technology for Energy Efficient Devices”, SPEED, FP7 Large Project (NMP3-LA-2013-604057).

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Fault Tolerant Cell Design for MMC-based Multiport Power Converters

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***Abstract*—The Modular Multilevel Converter (MMC) is a promising technology for medium-high voltage DC/AC converters, being adequate for HVDC transmission systems. Among the appealing characteristics of the MMC are their modularity, and consequently their scalability, as well as the fact that there is no bulk storage element. One key aspect for the operation of the MMC is the response in the event of a short circuit in the DC link. Conventional MMC cells consist of a half-bridge and a capacitor, and have no capability to block the short circuit in the DC side, meaning that expensive and bulky circuit breakers might be needed in this case. Several fault tolerant cell designs have been proposed. However, these desings always bring an increase in the number of power devices and losses.**

Conventional MMC design can be enhanced to provide added functionalities, e.g. multiport power converters and solid state transformers (SST). A mean to achieve this is by providing the cells the capability to transfer power. This enhancements will imply an increase in the number of power devices and passives, as well as further complexity of the control. However, the resulting cells structures can offer new opportunities regarding fault tolerance.

This paper revises the fault tolerance capability of MMCs, and analyzes the behavior of MMC-based multiport power converters in the event of faults. A new cell structure will be proposed capable of blocking the DC short circuit current, therefore protecting the power converter with reduced extra elements. [1]

***Index Terms*—MMC converters, HVDC transmission, fault tolerance, fault current, short-circuit, ride-through capability.**

I. Introduction

The Modular Multilevel Converter (MMC) (see Fig. 1) was first introduced by Lesnicar and Marquardt [1], [2], [3], [4], being considered one of the most attractive options for medium/high voltage DC/AC electronic power converters [5], especially for High Voltage Direct Current (HVDC) transmission systems [6], [7]. It its more common implementation, MMC cells consist of a half-bridge and a capacitor (see Fig. 2(a)).

Compared to other multilevel converter topologies, the main features of the MMC are:

- Modularity and scalability, which enables construction of high voltage converters using cells of with relatively low voltage.
- High efficiency due to their multilevel design. This allows the use of low switching frequencies and therefore reduced switching losses [5],[8].
- Reduced harmonic content, which is intrinsic to the better wave shapes produced by multilevel designs [5], [6], [8], [9].
- Since the devices don't have to switch at the same time, their stress is reduced [5].
- No need of a bulk energy storage system (capacitor), as the energy storage is distributed through the cells.

Despite of its appealing properties, lack of DC short circuit current blocking and ride through capabilities are important drawbacks that must be considered for their use e.g. in HVDC transmission systems [10]. Cells in conventional MMCs have a half-bridge structure (Fig. 2(a)). In the event of a short circuit in the DC side, the cell diodes will conduct, feeding the short circuit. An external switch, i.e. DC breaker can be used to cutoff the fault current. However, such breakers are expensive and there are concerns regarding their effectiveness in terms of response time and fault recovery [11]. Alternatively, silicon-based solutions can be used to improve the fault tolerance capability of the MMC. Several modified cell topologies have been proposed for this purpose. However, these modifications are always at the price of an increase in the number of power devices and losses [1], [6], [9]-[12].

Conventional MMC provides an AC and a DC port. Several MMC-based multiport power converter topologies have been proposed [9], [13]-[14]. These topologies use modified cell designs to enhance the functionalities of the MMC. A popular arrangement for such enhanced cells use a Dual Active Bridge (DAB) to transfer power to the MMC cell capacitor. The resulting cell requires a larger number of power devices compared to the conventional cell. However, this extra devices offer the possibility to implement fault tolerance methods with relatively minor modifications.

This paper proposes a fault tolerant cell design for MMC-based multiport power converters. The digest is organized as follows. The conventional MMC and the MMC-based multiport power converter are presented in Section II. Analysis of both topologies in the event of a short circuit in the DC link are presented in Sections III and IV respectively. The proposed cell design is presented in Section V. Preliminary experimental results are provided in Section VI, the conclusions being presented in Section VII.

II. MMC-Based Multiport Power Converters

Conventional MMCs realize a bidirectional DC/AC transformation. Since the cells of the MMC have a limited storage

[1]This work was supported in part by the Research, Technological Development and Innovation Programs of the Spanish Ministry of Economy and Competitiveness MINECO-13-ENE2013-48727-C2-1-R and by the European Commission FP7 Large Project NMP3-LA-2013-604057, under grant UE-14-SPEED-604057

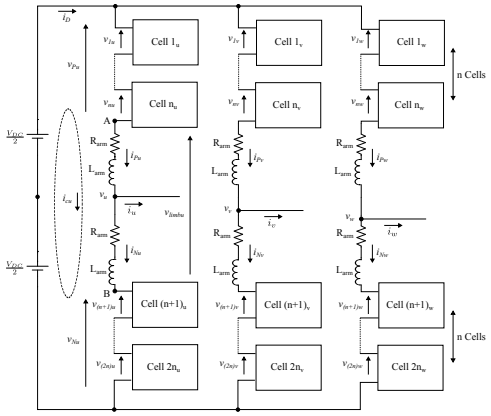


Fig. 1: Modular Multilevel Converter

capability, the net balance of AC and DC powers for each cell must be zero (neglecting losses). Its possible to provide the MMC cells the capability to transfer power at the cell level [9], [13]-[14]. This is done by connecting an electronic power converter to the cell capacitor. Topologies with galvanic isolation are preferred, an example of such cell arrangement using a Dual Active Bridge (DAB) is shown in Fig. 3(a), the details of the cell are shown in Fig. 3(b). Parallelization of the LV side of the DABs provides a LVDC port. This port can be either used directly or transformed into an LVAC port by means of a DC/AC power converter stage, as shown in Fig. 3(a). The use of such cell arrangement therefore results in modular multiport converter combining the HVDC/HVAC ports intrinsic to the MMC cells, LVDC/LVAC ports being obtained by adequate parallelization of the secondary of the DABs [9], [13], [14], [15].

III. Limitation and Control of the DC Short Circuit Current in MMCs

Conventional MMC designs using half-bridge cells are able to block the AC short circuit current. However, as already mentioned, it lacks a mechanism to block the DC short circuit current. This can be deduced from Fig. 1, where each cell has a half bridge topology (see Fig. 2(a)). If the short circuit occurs in the AC side, and the modulation is disabled once the fault is detected, the current will flow through freewheeling diode D_1 (Fig. 2(a)), entering the capacitor through the positive terminal. Since in normal operation the sum of the capacitor voltages is higher than the DC voltage, when the path inductance is discharged, freewheeling diodes are reverse biased and the current is naturally blocked. On the contrary, if the short circuit occurs in the DC link, the current in this case will flow through the freewheeling diode D_2 (Fig. 2(a)) of each cell directly to the DC link, bypassing the cell capacitor and feeding the short circuit [4], [11], [16], [17]. This will occur even if the modulation is disabled.

A. Modified Cell Structures

To overcome the DC short circuit current problem, several modified cell topologies have been proposed in the literature.

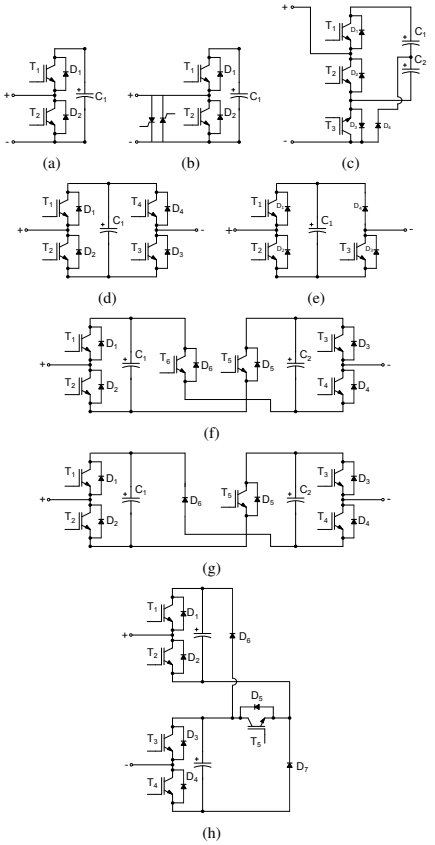


Fig. 2: MMC cell designs aimed to improve the fault tolerance capability. (a) Half Bridge cell (HB). (b) Cell with thyristor. (c) Diode Clamp cell. (d) Full Bridge cell (FB). (e) Unipolar Full Bridge cell (UFB). (f) Five-Level Cross Connected cell (5LCC). (g) Three-Level Cross Connected cell (3LCC). (h) Dual clamped cell (DC)

Two different cases can be distinguished for the analysis of these cell topologies: cells with blocking capability and cells with ride-through capability [10]. In the first case, when the fault is detected, the modulation is disabled. The operation of the cell is determined in this case by the diodes, the cells being designed to naturally block the fault current. Cells with ride-through capability have the ability to reverse the cell voltage without disabling the modulation. This allows to control to zero the voltage in the DC side of the MMC, therefore blocking the fault current, while maintaining control over the AC side voltage.

The principles, advantages and drawbacks of the proposed solutions are briefly discussed following:

- *Cell with thyristor* (Fig. 2(b)), [9]. One simple option for non-permanent faults is to add one or two thyristors per cell to bypass it. When a DC fault is detected, all IGBTs

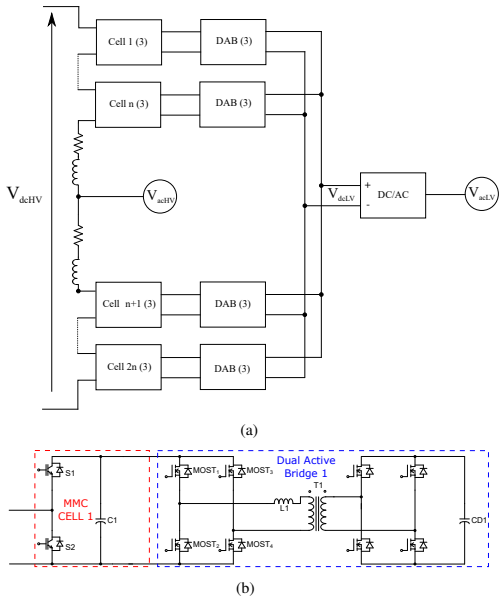


Fig. 3: MMC based Multiport Power Converter. (a) MMC-based multiport power converter. (b) MMC cell connected to a DAB. For the sake of simplicity the cells and DABs of all the three phases are grouped in a single block

are blocked and thyristors enabled, bypassing the cells and eliminating the rectifier formed by the freewheeling diodes. This allows to transform the DC short-circuit into an AC short-circuit which can be extinguished naturally. Since the fault is non-permanent, when DC current decays to zero, the DC arc fades away naturally. This structure is cost-effective and does not add extra losses in normal operation. However, it has several drawbacks, such as the need of snubber circuits and the relatively long times which are needed to block the fault (about 80-100ms), [9].

- *Diode Clamp topology* (Fig. 2(c)), [18]. In normal operation, transistor S_3 is in ON state, D_4 OFF and the cell is working as a half bridge having only the possibility to supply positive or zero voltage. When a fault occurs, all IGBTs are opened and current is forced to pass through diode D_4, capacitor C_2 going against the short circuit current through diode D_2. This structure has the capability to block the short circuit current, and the extra devices must withstand only half the DC cell bus voltage. However, it adds one IGBT and two diodes per cell, also it implies to split the cell DC capacitor in two.
- *Full-Bridge cell (FB)* (Fig. 2(d)), [11], [19]-[20]. This cell design provides DC short circuit fault ride through capability, as it allow to invert the voltage between the cell terminals. Also, the short circuit current can be naturally blocked by disabling the gate signals (blocking capability). However, the full-bridge cell topology uses twice the number of devices compared to the half-bridge cell, the conduction losses being twice too [10], [17].
- *Unipolar Full-Bridge (UFB)* (Fig. 2(e)), [21]. This is a simplified version of a half-bridge but without transistor T_4. In normal operation, T_3 is ON and D_4 is reverse biased, resulting in a half-bridge circuit. When a fault is detected, all IGBTs are disabled and it operates in the same way as a full-bridge structure blocking the short-circuit current. Compared to the full-bridge option, the amount of extra devices is reduced. However, it cannot put negative voltage at the cell output.
- *Five-level Cross Connected topology (5LCC)* (Fig. 2(f)), [6], [21], [22]. This structure has two half bridges connected back-to-back in a cross disposition. It adds four extra devices per cell (two IGBTs and two diodes). It can generate 5 symmetrical output levels, both positive and negative, providing therefore fault ride-through capability. If all switching devices are disabled, both capacitors are connected in series, blocking the current. In this topology, extra devices must switch even in normal operation, both switching losses and conduction losses being therefore increased.
- *Three-level Cross Connected structure (3LCC)* (Fig. 2(g)), [21]. This topology is derived from the Double clamp and Five-level Cross Connected. Operation of this topology during normal operation is similar to Double Clamp topology, but the Three level Cross Connected structure can generate three levels, i.e. 0, v_c and $2 \cdot v_c$, where v_c is the cell capacitor voltage. The Three Level structure can generate a reverse voltage of V_{dc} per cell, while Double Clamp topology generates V_{dc} for each two cells.
- *Double Clamp Cell (DCC)* (Fig. 2(h)), [1], [12]. In this solution, the extra devices needed to withstand the short-circuit are shared by two adjacent cells. This reduces the number of extra devices, and consequently the cost and the losses. In normal operation, T_5 is closed. When a DC short circuit is detected, T_5 is opened, the short circuit current sharing equally between the two capacitors and diodes D_6 and D_7. This topology can provide short circuit blocking capability, while ride through is not possible.

Table I summarizes the main characteristics for each of the designs discussed above, regarding extra devices, blocking voltage generated per MMC cell and fault handling capability (short circuit current blocking capability, ride through capability or both). It is noted that in some fault tolerant topologies the extra devices are shared by more than one MMC cell.

TABLE I: Fault tolerant MMC cell topologies comparison

	HB	Diode C.	FB	UFB	5LCC	3LCC	DCC
Extra dev/cell	0	3	4	3	2	1.5	2
Blocking Voltage	0	$V_{cap}/2$	V_{cap}	V_{cap}	V_{cap}	V_{cap}	$V_{cap}/2$
Blocking Capability	NO	YES	YES	YES	YES	YES	YES
Ride Through Capability	NO	NO	YES	NO	YES	NO	NO

B. Fault Tolerant Hybrid MMC Structures

In the preceding discussion it is assumed that all the cells of the MMC are identical. In MMC-based HVDC systems, the use of half-bridge cells is conventionally suitable

for underground or sub-sea cables, while full-bridge cells and double clamp structures have been shown to be more adequate in overhead lines [21]. The half-bridge structure presents the lowest cost and the highest efficiency, however it does not provide fault tolerant (either blocking or ride-through) capabilities. On the other hand, all fault tolerant structures providing short circuit current blocking or ride-through capability sacrifice efficiency and cost, as they require extra devices [21].

The compromise between cost, efficiency and fault tolerance can be varied by using hybrid structures merging different types of cells [21], [23]. Half-bridge and full-bridge submodules can be combined for this purpose. It is needed to determine in this case the number of cells of each type, and how they are arranged. Assumed that once the short circuit is detected all IGBTs are turned off, the condition to block the fault current is that the sum of the capacitor voltages connected in series must be equal or higher than the AC peak voltage. Therefore, the following relationship must hold [21], where $V_{cap_{fault}}$ is the steady state submodule capacitor voltage after short circuit is blocked, N_f is the number of capacitors per arm that are connected in series to produce the voltage opposing to the short circuit current during the blocking period and $V_{peak_{LL}}$ the line-to-line AC peak voltage.

$$2 \cdot N_f \cdot V_{cap_{fault}} \geq V_{peak_{LL}} \tag{1}$$

Equation (1) establishes that, to clear the fault, N_f series connected capacitors per arm charged at a voltage $V_{cap_{fault}}$ must match the AC side voltage. During normal operation, assumed $2 \cdot N_f \cdot v_c < V_{peak_{LL}}$, the capacitors belonging to cells with DC fault handling capability will be charged to $V_{cap} = V_{peak_{LL}}/2N_f$ in order to comply with (1) and block the short circuit current after being charged. Based on this concept, to ensure that the capacitor voltages are maintained at their nominal values $V_{cap_{ref}}$ during a fault, the minimum number of capacitors connected in series N_f is given by (2).

$$N_f \geq \frac{V_{peak_{LL}}}{2\, V_{cap_{ref}}} \tag{2}$$

Once N_f is obtained, the number of MMC cells with fault handling capability can be determined. It is noted however that N_f is not necessarily equal to the number of required submodules with fault handling capability. As an example, full bridge submodules (see Fig. 2(d)) provide one capacitor in series in the event of fault, the number of cells with fault handling capability being therefore N_f. On the contrary, in the double clamp arrangement (see Fig. 2(h)), two capacitors are connected in parallel, the resulting blocking voltage being $V_{cap}/2$ (see Table I). As a consequence, the required number of double-clamp submodules would be $2N_f$. The number of series connected capacitors provided by the cells with fault handling capability will also determine the fault blocking time. The higher this number is, the higher reverse voltage is produced, the fault current being blocked faster. This is at the price of higher losses and cost.

Table II shows a comparative analysis of the number of required fault tolerant (FT) cells for different hybrid MMC structures based on HB cells and other modified submodules (see Fig.2). The MMC-based multiport converter based on the Double Clamp concept (MP HB+DDC) shown in the table is discussed in Section IV.

TABLE II: Hybrid converters comparison

	HB+FB	HB+UFB	HB + 5LCC	HB + 3LCC	HB+DCC	MP HB+DDC
N° HB SMs	$N - N_f$				$N - 2 \cdot N_f$	
N° FT SMs	N_f				$2 \cdot N_f$	

C. Hybrid MMC Structures: Symmetric and Asymmetric Mixed Cell Arrangements

The number of required fault handling submodules is not the only concern when designing hybrid MMC structures, also how the conventional and fault tolerant cells are arranged must be considered, two different options can be analized [23]: the so called symmetric (Fig. 4) and asymmetric (Fig. 5) mixed cell topologies. Both arrangements combine the same amount of Half Bridge (HB) and Full Bridge (FB) submodules. In the symmetric structure, equal number of HB and FB submodules are alternately placed along each arm of the MMC, while the asymmetric structure consists of fully HB submodules in one arm and fully FB submodules in the other arm.

During normal operation, the symmetric mixed converter works as a conventional MMC, regardless of the FB cells. However, in the event of a DC short circuit, the half bridge cells are bypassed and the converter works as a full bridge based MMC to provide ride through capability. For the case of the asymmetric topology, the upper arm consisting of HB submodules will work as a conventional HB-based MMC both during normal and short circuit operation. The lower arm will operate as HB-based MMC in normal operation and as FB-based MMC in fault mode and low power transmission mode (i.e. DC bus voltage is lower than the rated DC bus voltage).

Arm voltages in MMCs are typically assumed to be always positive. However, it is possible for the arm voltages to be negative, this can occur due to different reasons, e.g.

- A DC bus voltage lower than the rated DC bus voltage (e.g. a MMC is commanded to produce DC bus voltage lower than its rated value [23])
- In the event of a fault (ride through operation)

Under these circumstances, there are significant differences between symmetric and asymmetric mixed converters regarding the submodules capacitor voltage balancing.

For the symmetric mixed converter, when the arm voltage is negative, HB cells are bypassed and FB cells must work in a bipolar mode. In this scenario, capacitor voltages of FB cells can change while capacitor voltages of HB cells remain constant. As the negative arm voltage and the current get larger, the imbalances among arms for the symmetric mixed MMC increase, eventually resulting in a disconnection of the converter. On the contrary, positive arm voltages will not affect the normal operation of the submodule capacitor voltage balancing algorithm.

On the other hand, for the asymmetric mixed converters, the DC component of the upper arm voltage is fixed as a half of the rated DC bus voltage, while the DC component of the lower arm voltage determines the DC bus voltage ($V_{dc}{}^{*} - V_{dcrated}/2$). Due to this, negative voltage only appears in the bottom arm, the voltage balancing algorithm being

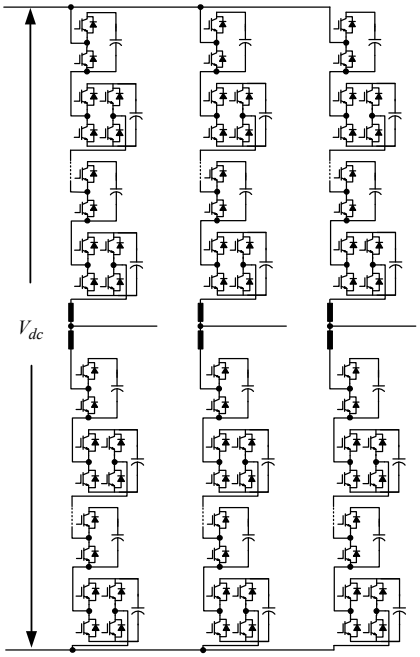


Fig. 4: MMC symmetric hybrid converter structure

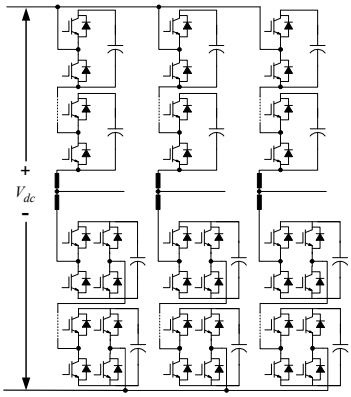


Fig. 5: MMC asymmetric hybrid converter structure

able to operate correctly. Hence, voltage imbalances between submodules do not occur.

IV. DC Short Circuit Current Blocking in MMC-based Multiport Power Converters

Similarly to the conventional MMC, MMC-based multiport topologies do not have an intrinsic mechanism to handle the DC link short circuit. When a DC short circuit occurs, cells cannot generate a negative output voltage to drive the short circuit current to zero. Consequently, fault handling (i.e.short

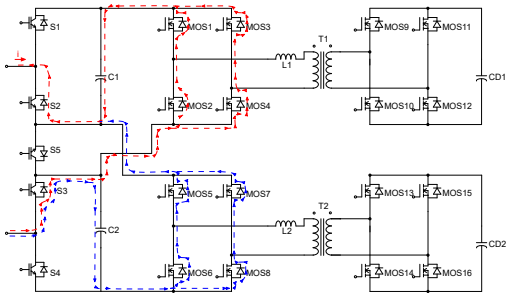


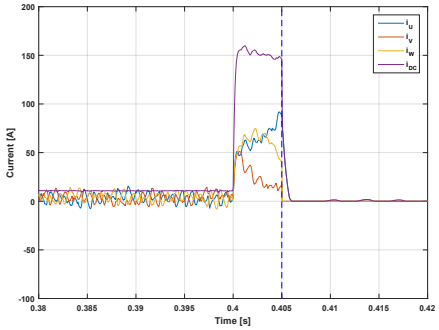
Fig. 6: Double Clamp based fault tolerant cell topology for multiport converter showing the currents in the event of a DC short circuit in the blocking period

circuit current blocking and ride through) is not possible in this topology.

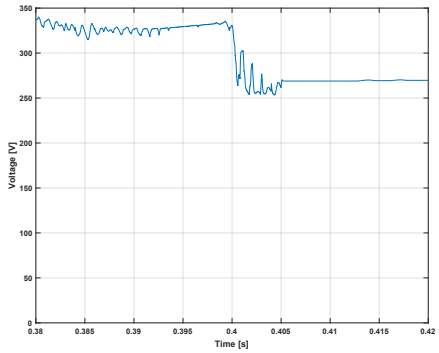
If the gate signals are disabled in the event of a DC short-circuit fault, the resulting topology is obtained from Fig. 3(a) by eliminating the transistors and leaving only the freewheeling diodes. Since the converter is not modulating, the high frequency transformer of the DAB will not transfer power. The DABs can be omitted in this case, the cell behaving as in the conventional MMC with half bridge submodules. The discussion in Section III applies therefore in this case too. Consequently, the modified fault tolerant MMC cell topologies discussed in the previous section can be used in the multiport MMC-based power converter.

Thanks to the presence of the DABs in the modified cell, is it possible to take advantage of the DAB devices to modify the MMC cells with a reduced penalty in terms of cost (extra devices) and losses. Especially suitable is the *double-clamp* concept shown in Fig. 2(h). This topology was shown to be advantageous due to the reduced count of extra devices and reduced losses compared to other fault tolerant cells. For the case of the MMC-based multiport converter using the cell shown in Fig. 3(b), the freewheeling diodes of the DAB can replace in this case the clamping diodes.

As for the conventional MMC, the double clamp concept adds an IGBT and a diode in antiparallel connecting two cells (S5). In normal operation, S5 is closed and the two cells operate as two conventional MMC based Multiport converter cells (See Figure 3), with the difference that in the lower HB the output voltage is taken between $S3$ terminals (see Figure 6). During blocking period, S5 is opened, blocking the voltage of the two cell capacitors connected in parallel. Therefore the voltage rating of $S5$ is the same than the rest of IGBTs. When a DC short circuit is detected, DABs' diodes operate similar to the clamping diodes of the Double Clamp structure [12], creating two identical paths that force the fault current to flow across the capacitors, charging them and eventually blocking the short circuit current. Fig. 6 shows the paths of the DC short circuit current when a DC fault occurs. For the sake of simplicity capacitors $C1s$ and $C2s$ in Fig. 8(a) are not shown in Fig. 6, as they are much smaller than the cell capacitors and are needed only for the DABs output current control, having a negligible impact in the process of blocking the short-circuit



(a)



(b)

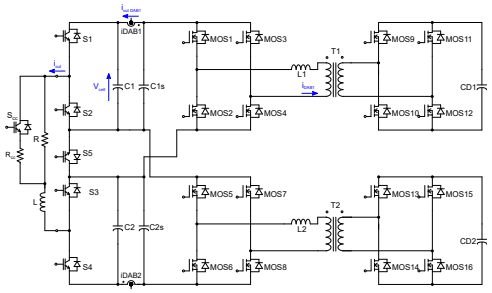
Fig. 7: Simulation results. (a) DC and phase currents. (b) Cell capacitor voltage

current.

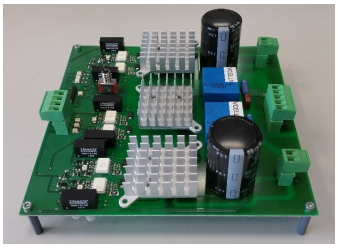
A. Simulation Results

Fig. 7 shows the behavior of the MMC-based multiport power converter in the event of a short circuit in the DC side. At $t = 0.4s$ the short circuit occurs. At $t = 0.405s$, short circuit is detected and the modulation is disabled, starting the blocking period. Fault current has now to flow through the freewheeling diodes of the DAB switches, to the positive terminal of the cell capacitor, blocking the fault current. While the sum of cell capacitor voltages is higher than the rectified value of the AC voltage, the fault remains blocked. Since in normal operation the capacitors are charged until the sum of their voltage reaches twice the value of the rectified AC voltage, the fault is blocked very quickly (less than $1ms$ in the Figure 7).

Fig. 7(a) shows the DC and phase leg currents, which are seen to reach inadmissible values during the short circuit, and rapidly blocked once the fault is detected. Fig. 7(b) shows the evolution of the capacitor voltage during the process. While the converter is supplying the short circuit current, the capacitors discharge, charging slightly during the blocking period.



(a)



(b)

Fig. 8: Experimental setup. (a) Cell block diagram. (b) Experimental setup

Although the losses have not been quantified, the converter has extra losses compared with the multiport using half bridge MMC cells. However, losses are lower compared with the case when fault tolerant cells are used, since there is a reduction in the number of extra devices, and S_5 must not conduct the converter current all the time.

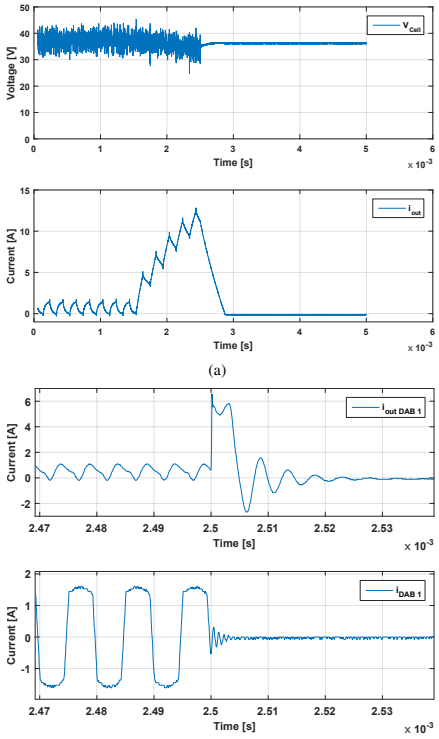
V. Experimental Results

Preliminary verification of the proposed methods was realized using the configuration shown in Fig. 8(a), the experimental setup being shown in Fig. 8(b). Fig. 8(b) implement the MMC cells shown in the schematic in Fig. 8(a).

Figure 9 shows the capacitor voltage of one MMC cell (top) and the output current going from the converter to the load (bottom). At $t = 1.5e^{-3}s$ the short circuit occurs (S_{cc} ON), the output current quickly increasing. During this period, the capacitor voltages slightly decrease.

At $t = 2.5e^{-3}$, the fault is detected and the modulation is disabled. The current starts flowing through the capacitors, quickly decreasing. At $t = 0.374ms$, the current is fully blocked, the converter can restart once the fault is cleared.

Fig. 9(b) shows the current through the DAB. The top graph shows the current flowing from the DAB to the MMC cell, the bottom graph shows the current through the DAB transformer. It is noted that the overcurrent occurs at the DAB output current but not in the high frequency transformer. This is because the DAB is not actually supplying current, the overcurrent circulating across the blocking path.



(a)

(b)

Fig. 9: Experimental results. a) Cell capacitor voltage and output current. b) DAB currents

VI. Conclusions

Fault tolerance is a key requirement for MMC power converters, especially in HVDC applications. Conventional MMC design does not have the capability to withstand DC short circuits. For this reason, modified cell topologies have been proposed capable to block the short circuit current. However, this is always at the price of increased number of power devices and losses. The adaptation of the double clamp cell concept to MMC-based multiport power converters has been proposed in this paper. The presence of DABs used to transfer power to the cells in this type of power converters, allows a reduction in the number of extra power devices needed, and consequently in the cost. Simulation results of a three-phase MMC-based multiport power converter with dual double clamp topology cells as well as experimental results have been provided to demonstrate the feasibility of the proposed concepts.

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Comparative Analysis of Modular Multiport Power Electronic Transformer Topologies

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***Abstract*—Conventional line-frequency transformers are a key element in the current power transmission system. Although they are a relatively cheap and well established technology, they are not able to provide new functionalities demanded by the power system operator. Solid State Transformers (SSTs), also called Power Electronic Transformers (PETs) are power electronics-based arrangements able to provide, in addition to the basic functions of a conventional transformer, new functionalities like harmonics, reactive power and imbalance compensation, and power flow control.**

This paper addresses a comparative analysis of modular PET topologies, including the popular CHB-based approach and MMC-based topologies. Criteria for the evaluation will include aspects like the number of cells required, ratings of the power devices, number and type of the PET ports and design requirements for passive elements.

***Index Terms*—Modular Multilevel Converter, MMC, Multiport Power Converters, Solid State Transformer, Power Electronic Transformer**

I. Introduction

The need to reduce the dependence on fossil fuels due to the progressive increase of their cost, limited resources and the environmental concerns, has resulted in a sustained increase in the share of renewable energies in the gross final energy consumption. However, massive integration of renewable energy into the existing and future grids poses significant challenges to fulfill reliability and efficiency requirements. Innovative solutions based on high-power, high-voltage electronic power converters, like HVDC (High Voltage Direct Current), FACTS (Flexible AC Transmission Systems) and SSTs have the potential to cope with these new challenges [1],[2].

Conventional Line-Frequency Transformers (LFT) are a key element in the current power transmission system. Although they are a relatively cheap, reliable and well established technology, they cannot provide new functionalities demanded by the power system operator, such as power quality improvements (i.e harmonics, reactive power and imbalances compensation), power flow control and reduction of transmission losses.

SSTs are based on power converters with fast-switching devices, which enable the use of high frequency (HF) transformers. This potentially enables a significant reduction of the volume and weight of the core material. Additionally, they are able to provide advanced functionalities such as reactive power, harmonics and imbalances compensation, and power flow control.

This work was supported in part by the Research, Technological Development and Innovation Programs of the Spanish Ministry of Economy and Competitiveness MINECO-13-ENE2013-48727-C2-1-R and by the European Commission FP7 Large Project under grant UE-14-SPEED-604057

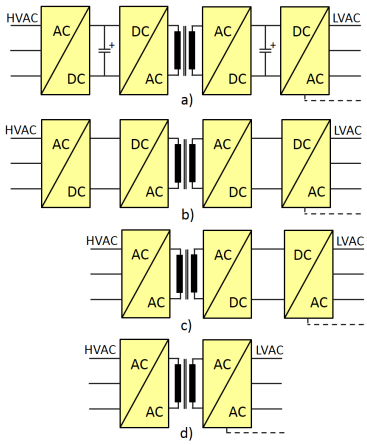

Fig. 1. 3-phase PET arrangements. a- Fully modular three-stage PET including DC link back-to-back converters in both HV and LV sides. b- Three-stage PET consisting of indirect matrix converters in both HV and LV sides. c-Two-stage PET based on direct matrix converter in the HV side and indirect matrix converter in the LV side. d- One-stage PET based on direct matrix converter. Note: LVAC port can be either 3 wire or 4 wire.

A common criteria for the classification of SST is the number of energy conversion stages. According to this criteria, a number of PET topologies comprising one, two or three energy conversion stages have been proposed [3]-[11]. The fully modular three-stage configuration (see Fig.1-a) appears to be the most popular choice [6], examples of this can be found in Europe in FP6 project UNIFLEX [10] and in US in NSF project FREEDM [5],[11]. This topology realizes a double DC/AC transformation in the HV side and in the LV side respectively. Isolation between the LV and HV sides is provided by a DC/DC stage using a HF transformer. The presence of DC links offers remarkable advantages in terms of optimization in each conversion stage. Elimination of DC link capacitors is possible, bur requires the use of indirect matrix converter topologies (see Fig. 1-b). The reduction of the number of stages to two or one will require the use of direct matrix converters (see Fig. 1-c-d). It is noted that

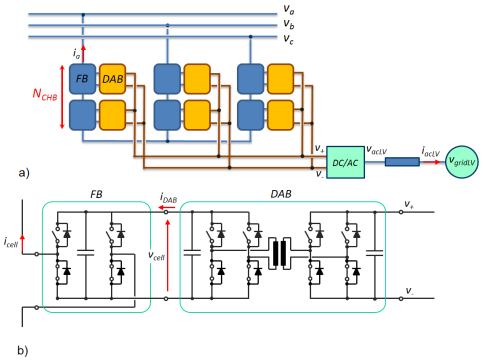

Fig. 2. a) 3-phase CHB-based PET. b) Submodule including the full-bridge (FB) and the Dual Active Bridge (DAB) converter.

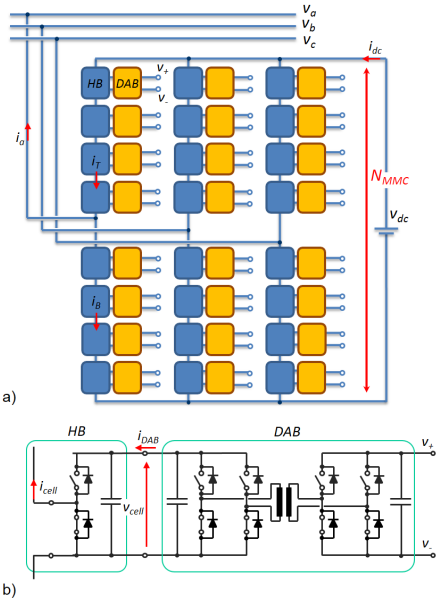

Fig. 3. a) 3-phase MMC-based PET. LV-side outputs of the DAB (V_+, V_-) are connected as in Fig. 2 (not shown for the sake of clarity). b) Submodule including the half-bridge (HB) and the DAB converter.

implementations requiring the use of matrix topologies will imply in general an increase in cost and complexity [6].

Practically all PET topologies provide at least a high-voltage AC (HV–AC) and a low-voltage AC (LV–AC) port, therefore connecting two AC systems. However, inclusion of additional ports, e.g. low-voltage and/or high-voltage DC (LV–DC/HV–DC) is often possible. The resulting multiport topologies enable additional functionalities, e.g. interconnection to HVDC [12]-[14] or the integration of energy storage devices or distributed energy resources (DER) [15]. However, this enhancement can imply an increase of the PET complexity and cost, which needs to be considered.

This paper realizes a comparative analysis of modular PET topologies. Designs being considered include the CHB-based PET [11], as well as various MMC-based topologies [9],[14]. Criteria for the evaluation will include:

- Number and type of the ports provided by the PET
- Number and rating of the power devices
- High frequency transformers count and requirements

The paper is organized as follows. The CHB topology is discussed in Section II, and it will be used as the reference case. MMC-based topologies being considered are presented in Section III. Comparative analysis is presented in Section IV. Discussion of the DAB and the HF transformer design are addressed in Sections V and VI, respectively. Experimental results are provided in Section VII, conclusions being presented in Section VIII.

II. CHB-Based Power Electronic Transformer

Cascade H-Bridge (CHB) converter can likely be considered as the most popular topology for the HV DC/AC stage of PETs (stage in the left side of Fig. 1-a) and will be used as a benchmark. The CHB-based PET is shown in Fig. 2-a. It consists of a series connection of a certain number cells, each consisting of a full-bridge submodule and a capacitor. Serialization of cells allows to withstand high voltages using relatively low voltage devices. It is noted that the CHB cells alone are not able to handle active power, this feature is achieved by providing the submodules the capability to transfer (absorb/deliver) power. Dual Active Bridge (DAB, Fig. 2b) converters can be used for this purpose. This corresponds to the intermediate stage in Fig. 1-a. The output of the DABs is parallelized to obtain a low voltage-high current DC link, from which the LV–AC port is obtained using a DC-AC converter [9], [11]. Practical implementation of this concept can be found in [5], [10], [11].

III. MMC-Based Multiport Power Electronic Transformer

The CHB-based PET in Fig.2 connects a HV–AC port and a LV–AC port. It is also observed from this figure that it can offer a LV–DC port. However, this topology does not provide a HV–DC port. To overcome this limitation, Modular Multilevel Converter (MMC) based PET can be used, which intrinsically provides a HV–DC and a HV–AC port [16]-[18].

Fig. 3 shows an MMC-based multiport PET [9],[14]. Similarly to the CHB case, DABs are used to perform the intermediate stage in Fig.1-a. DAB outputs in the LV side are parallelized to provide a LV–DC, high current port.

Simulation results showing the operation of the MMC-based multiport PET are shown in Fig. 4. The MMC is enabled at t=10 ms, with the active power command being $100kW$ (Fig. 4-a). Initially the DABs are not transferring power, the power in the DC link of the MMC (Fig. 4-b) matching therefore the AC power plus the converter losses. At t=70 ms the controlled

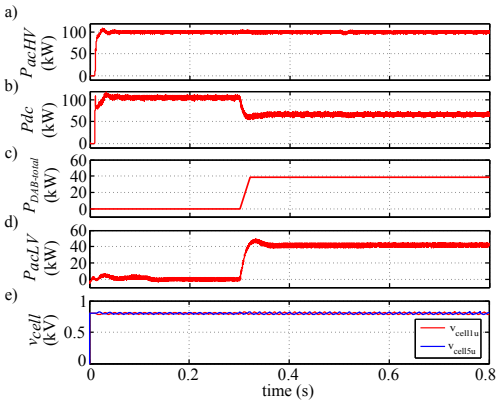

Fig. 4. Simulation results. MMC-based multiport PET. a) Active power in the HVAC port. b) Power in the DC port. c) Total power injected by the DABs. d) Active power in the LVAC port. e) Capacitor voltage of a cell in the top and bottom arms.

rectifier in the LV side of Fig. 3 is enabled, though there is no power transfer. At t=0.3 s, the DABs are commanded to transfer a total amount of $40kW$, which is supplied by the controlled rectifier in the LV side (Fig. 4-d). In order to keep the power balance, power supplied by the DC bus of the MMC is decreased in the same amount (see eq. (4)). The commanded values are the AC active power in the HV side of the MMC and the power transferred by the DABs. The active power for the controlled rectifier and the power in the DC link of the MMC are internally controlled to maintain the power balance. The capacitor voltage of two cells are shown in Fig. 4-e, they are seen to remain perfectly stable.

Alternatively to the topology shown in Fig. 3, it is possible to connect the DABs directly to the HVDC port [4] (Fig.5). MMC cells in this case use the conventional half-bridge (HB) topology. The design in Fig. 5 allows a different number of DAB and MMC cells. A potential advantage of this option is a reduction in the number of DABs and consequently of HF transformers. However, this is at the price of an increase of the DAB power devices ratings (voltage and current), also affecting to the design of the HF transformer. This is discussed in Sections IV and V. Finally, examples of MMC-based PET using a single HF transformer can be found in [7], [19].

IV. Comparative Analysis of Modular PET

Comparative analysis of the modular PET topologies is presented in this section. As already discussed, the biggest difference between CHB and MMC based PET topologies is the presence of a HV-DC port in the latter, which is added to the existing high-voltage AC (HVAC) and low-voltage AC (LVAC) ports. This topology performs therefore a multiport power conversion. While such port provides new functionalities compared to the power converter in Fig. 2, and can be compulsory in certain applications, this is at the price of an increase in the number of required cells, and as a consequence, of power devices, passive elements and auxiliary circuitry.

TABLE I
AC and DC ports voltage

HV–AC	24 kV $(line, rms)$
LV–AC	400 V $(line, rms)$
HV–DC	40kV
LVDC	800 V

In order to illustrate the differences between the CHB and MMC-based arrangements, the particular case of a PET connecting two AC grids of $24kV$ and $400V$ is discussed. The LV-DC is set to $800V$. The HV-DC for the MMC-based PET topologies needs to be larger than the peak-to-peak phase value of the HV-AC, which is $39.2kV$. A HV-DC of $40kV$ was selected, the HV-AC to HV-DC ratio being $R_{nothi} = 0.98$ without triplen harmonic injection, [13]. It would reduce to $R_{thi} = 0.85$ using triplen harmonic injection. While this ratio might be very tight in a practical implementation, the discussion following is valid for smaller values of R_{nothi} without loss of generality. Rated power for the DABs is $P_{DAB} = 5kW$. Voltage ratings are summarized in Table I.

A. CHB-based PET

CHB cells use a full-bridge (FB) topology. Each cell can provide a voltage equal $\pm v_{cell}$, with $v_{cell} = 800V$. The number of cells required to produce the peak-to-peak phase HV-AC value is given by (1).

$$N_{CHB} = \frac{v_{ph-peak}}{v_{cell}} \tag{1}$$

For the required HV–AC voltage in Table I, the number of FB cells per leg is 25, i.e. 75 in total, which is equal to the number of DABs. The total power that can be transferred between the HV-AC and LV-DC ports is $P_{CHB-total} = P_{DAB-total} = 375kW$. The number of devices (transistors and diodes) for the CHB converter is 300.

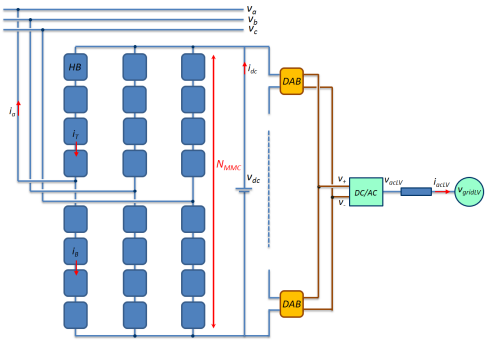

Fig. 5. 3-phase MMC-based PET with the DABs connected to the HV–DC link.

B. MMC-based PET

For the MMC-based PET, the cells must be able to produce both the HV–DC and HV–AC voltages. Cells in this case are half-bridge (HB). The number of cells per leg is given by (2) (see Fig. 3).

$$N_{MMC} = \frac{V_{dc}}{v_{cell}} \cdot 2 \tag{2}$$

To achieve the HV–DC voltage in Table I, the number of cells per leg is 100, i.e. 300 in total, which is equal to the number of DABs. The total power that can be transferred between the HV-AC and LV-DC ports is $P_{MMC-total} = P_{DAB-total} = 1500kW$. The number of devices (transistors and diodes) for the MMC converter is 600.

It is interesting to note that to achieve the same HV-AC voltage, the MMC-based PET requires four times the number of cells of the CHB-based PET. This is the reason why the power of MMC-based design is four times the power of the CHB-based design, since each cell of the MMC-based design has an associated DAB.

For the MMC-based PET implementation shown in Fig. 5, the MMC cells requirements are identical to the previous case. However, assumed that the DABs DC voltage remains constant, the number of DABs is reduced by 6 (i.e. $N_{DABs} = 40kV/800V = 50$), but each DAB driving now six times the current (i.e. $P_{DAB} = 30kW$). The total power that can be transferred remains constant, i.e. $P_{DAB-total} = 1500kW$.

Table II summarizes the results of the previous discussion. It is noted that the number of devices $N_{devices}$ account for the devices (transistors & diodes) in the CHB and MMC cells, not including therefore power devices in the DABs.

TABLE II
SIZING ANALYSIS FOR THREE DIFFERENT PET TOPOLOGIES

	CHB-based PET (Fig. 2)	MMC-based PET (Fig. 3)	MMC-based PET (Fig. 5)
v_{cell}	800 V	800 V	800 V
N_{leg}	25	100	100
N_{DABs}	75	300	50
P_{DAB}	5kW	5kW	30kW
P_{total}	375kW	1500kW	1500kW
$N_{devices}$	300	600	600

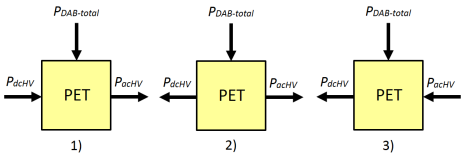

Fig. 6. MMC-based PET possible power flow routes. Case 1- HVAC port must evacuate power coming from both the HVDC port and DABs. Case 2- Both HVAC and HVDC ports evacuate the power injected by the DABs. Case 3- HVDC port must evacuate power coming from both the HVAC port and DABs.

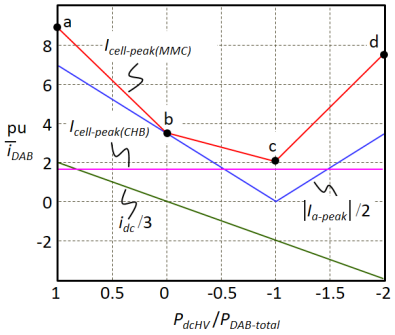

Fig. 7. MMC-based and CHB-based PETs devices peak current as a function of $P_{dcHV}/P_{DAB-total}$, with $P_{DAB-total}$ equal to its rated value. Currents are shown in pu of the DAB average current.

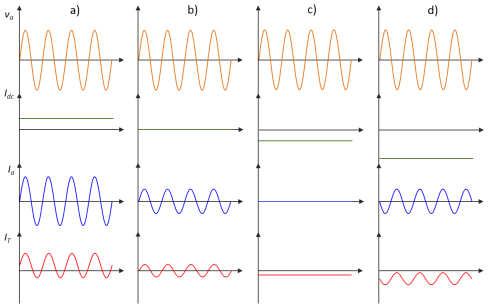

Fig. 8. MMC-based PET representative waveforms: AC voltage v_a, DC current i_{dc}, AC current i_a and top arm current i_T. Four different cases specified as (a-b-c-d) in Fig. 7 are included.

C. CHB vs. MMC cell power devices requirements

The requirements for the power devices in the circuits shown in Fig. 2-b and Fig. 3-b present important differences. The power devices in the FB and HB connecting the DABs with the high-voltage ports of the PETs, must withstand the same voltage. Consequently, they should have similar voltage rating. However, there are significant differences in the required current ratings and switching characteristics. Commutation requirements for the devices in CHB and MMC cells are low, due to the multilevel nature of both power converter topologies [21]. In addition, diodes in CHB and MMC cells must conduct for relatively long periods of time, high quality free-wheeling diodes are therefore required. From the previous discussion, $1.7kV$ Silicon IGBTs, using either Si or SiC free-wheeling diodes are an adequate solution for the CHB and MMC cels.

One major difference of MMC-based PETs compared to CHB-based solution is their multiport feature. Such multiport feature modifies the power balance equation of the MMC-based PETs, and consequently the current that the power devices must carry. This needs to be considered both for the cell design and for the control strategies of the converter.

In the CHB-based PET, all the power transferred by each DAB must be transferred by the corresponding CHB cell, the relationship between the DAB mean current and the CHB cell peak current being (3).

$$\frac{i_{cell-peak}}{\bar{i}_{DAB}} = \sqrt{3} \tag{3}$$

It is noted that i_{cell} is an AC current at the grid frequency (50 or $60Hz$ typically). On the contrary, i_{DAB} is a high frequency pulsated current, $\bar{i}_{DAB}$ being its average (DC) value. The relationship between the DAB average and peak current can be roughly approached by $i_{DABpeak} \approx 1.3\ \bar{i}_{DAB}$.

Selection of the current rating for the power devices in MMC-based PETs is not so straightforward. The MMC-based PET offers different routes for the power flow, depending how the power transferred by the DABs ($P_{DAB-total}$) is split between the HV-DC port (P_{dcHV}) and HV-AC port (P_{acHV}) (4). This will affect to current requirements of the power devices.

$$P_{dcHV} + P_{DAB-total} = P_{acHV} \tag{4}$$

The current that must be carried out by the MMC cells power devices will depend on how the three terms in (4) are combined. For the discussion following, it is assumed without loss of generality that the DABs are injecting their rated power from their LV to the HV sides.

Three cases can be considered:

1) $P_{dcHV}/P_{DAB-total} > 0$: In this case $|P_{dcHV}| > |P_{DAB-total}|$. Consequently, the HV–DC port also injects a positive power P_{dcHV}. The HV–AC-port must evacuate the power coming both from the HV–DC port and from the DABs in this case (see Fig. 6-1)
2) $-1 < P_{dcHV}/P_{DAB-total} < 0$: It occurs when $|P_{dcHV}| < |P_{DAB-total}|$, and both powers have opposite signs. Only the DABs inject power in this case, both HV–AC and HV–DC ports evacuate the power injected by the DABs (see Fig. 6-2)
3) $P_{dcHV}/P_{DAB-total} < -1$: It occurs when $|P_{dcHV}| > |P_{DAB-total}|$, and both powers have opposite signs. AC port inject power in this case, the HV–DC port must evacuate the power coming both from the HV–AC port and the DABs. (see Fig. 6-3)

Fig. 7 shows the relationship between the MMC DC current i_{dc}, AC peak current i_a, and arm peak currents $i_{cell-peak(MMC)}$, for the three operating regions. The peak current for CHB-based PET cells $i_{cell-peak(CHB)}$ is also shown for reference. It is noted that, depending on how the power of the three ports are combined, the MMC cells devices must be designed to conduct currents which can be significantly larger than for the CHB case. Fig. 8 shows representative waveforms for the four different operating conditions indicated in Fig. 7 as a) -b) -c) and -d). It should be remarked how the DC power is negative in cases c) and d), while AC power is negative only in case d).

V. Isolation Stage: DAB Power Devices

High switching frequencies are desired for the DABs, as this allows to reduce size of the HF transformer. For the HV side of the DABs, $1.2kV$ SiC MOSFET will be used. Two options have been considered: SiC MOSFET Power module Cree CCS050M12CM2, with rated voltage and current values of $1.2kV$ and $59A$ respectively, and discrete SiC MOSFET Rohm SCT2080KE, with rated values $1.2kV$ and $28A$. The latter was eventually chosen as it fits better with the power requirements. The DC voltage for the HV side of the DAB was set to $800V$, the average current being $6.25A$, each DAB transferring the required $5kW$. It is noted that the DAB design is the same for the topologies shown in Fig. 2a and Fig. 3a, while the topology in Fig. 5 can require changes in the DAB ratings.

Identical switching frequencies are required for both HV and LV sides of the DAB. Since the voltage in the LVDC link is similar to the voltage in the HV side, same devices can be directly used. Synchronous rectification can be used for the control of the DAB, meaning that the requirements for the diodes are weak. The MOSFET body diode could be enough in this case.

VI. Isolation Stage: DAB High-Frequency Transformer Design

The DAB HF transformer is a key element for PETs, as it must be able to transfer power between the HV and LV sides with the highest possible efficiency, while providing galvanic isolation between the HV and LV ports. Key parameters for the transformer design are its power, input and and output voltages, switching frequency, leakage inductance and the required isolation. Transformer power, input and output voltages as well as switching frequency are directly linked to the characteristics of the power devices being used. The base case design, as well as alternative designs depending on the devices available are discussed following.

A. Base Case Design

For the PET design considered in this paper, the isolation between the HV and LV sides that must be provided by the HF transformer is $24kV$ (see Table I). The target switching

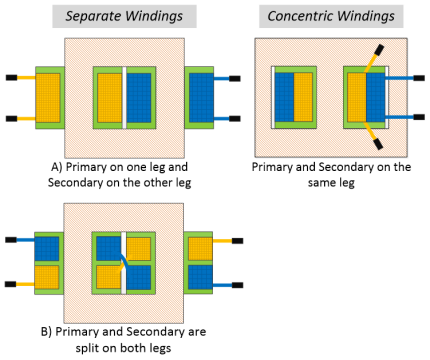

Fig. 9. HF transformer coil arrangements. Left- Separate windings, Right- Concentric windings

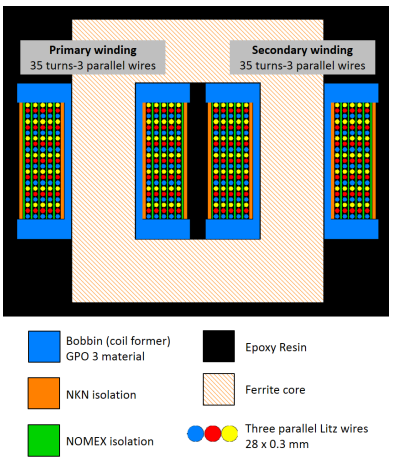

Fig. 10. Schematic representation of HF transformer for the base case.

frequency is $30kHz$, which is adequate for the SiC MOSFET being used. The target base power is $5kW$, which corresponds to the CHB and MMC-based PETS in the two columns on the left of Table II. The design objective is to minimize the overall losses and core size, keeping the temperature rise around $60°C$.

Different core materials and coil arrangements were considered. Concentric windings configuration achieves the lowest leakage inductance. However, high isolation levels (i.e. $24kV$) might not be possible to achieve due to the fact that a certain isolation distance must be kept between the windings. A schematic representation of this arrangement can be seen in Fig. 9-left-a). On the contrary, the use of separate windings (see Fig. 9-right) provides a much easier way of achieving the required isolation, but at the price of a significant increase in the leakage inductance. An intermediate option is to use separate windings but split between both legs (see Fig. 9-left-b). This arrangement may result in a four times decrease of the lekage inductance compared to the conventional separate windings option. However, achieving high isolation levels is highly penalized as the required distances between windings and terminals become hard to obtain. As a consequence, the HF transformer design developed along this paper will be based on a separate windings configuration, since it provides the best trade-off between isolation and leakage inductance requirements. A schematic representation of the base HF transformer design is shown in Fig. 10, including the different materials being used.

Experimental HF transformer prototypes have been designed based on 1.2 kV SiC MOSFET, as specified in Section V.

Table III shows experimentally measured parameters for three HF transformer designs. It is noted that figures with * refer to values that have not been obtained experimentally. First column includes experimentally obtained parameters for the *base case* transformer (see Fig. 11-Bottom). It is noticed that with the magnetic core material being used, the

TABLE III
HIGH-FREQUENCY TRANSFORMER EXPERIMENTAL DESIGN PARAMETERS

	Base case	**v2.0**	**v3.0**
Power	$5kW$	$5kW$	$10kW$
Input voltage	$800V$	$800V$	$800V$
Efficiency	$99.70\%^*$	$99.76\%^*$	$99.46\%^*$
Temperature rise	$62°C$	$28°C$	$> 100°C$
Leakage inductance	$485\mu H$	$485\mu H$	$235\mu H$
Mag. inductance	$11mH$	$11mH$	$2.5mH$
Power density	$10.45W/cm^3$	$10.45W/cm^3$	$36.25W/cm^3$
Number of turns	35	35	28
Turns ratio	1 : 1	1 : 1	1 : 1
Core material	$CF138$	$3C94$	$3C94$

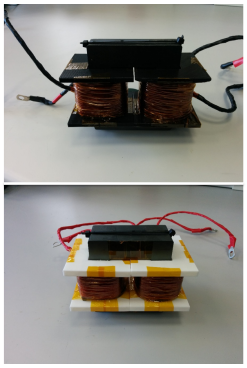

Fig. 11. Experimental HF transformer designs. Top- $v3.0$ in Table III; Bottom- Base case in Table III

temperature increased up to $62°C$, exceeding the permissible values, especially taking into account that these designs do not include resin cover, which would penalize heat evacuation. To overcome this problem, a different magnetic material has been used, $3C94$, which resulted in a significant reduction of the temperature rise ($28°C$). This leads to the design denoted as $v2.0$ in Table III (See Section VII).

To explore the possibility of transferring more power, another design has been studied ($v3.0$ in Table III)(see Fig. 11-Top). With the magnetic core available and the design constraints of rated power, isolation and input/output voltage, the required leakage inductance is significantly low. In this regard, a low number of turns is needed leading therefore to important core losses that drastically increases the temperature up to unacceptable values. Further experimental results can be found in Section VII.

It must be remarked that the transformers shown in Fig. 11 do not include the resin cover that would actually provide higher isolation features (see Section VII).

B. Alternative HF Transformer Designs

The HF transformer design described in the previous subsection used $1.2kV$ SiC power devices. However, it would be inadequate if larger voltage power devices were used. Depending on the characteristics of the power devices, three

design parameters must be considered for the design of the HF transformer:

- Rated power
- Input voltage (i.e. cell voltage)
- Switching frequency

Table IV shows alternative transformer designs for different values of the input voltage and rated power of the MMC-based PETs, while keeping the same isolation requirements. Mathcad and Matlab were used for the mathematical analysis, Pmag and Maxwell being used for FEA.

It is seen that increasing the power for the same input voltage and isolation, slightly increases the efficiency, the power density being increased significantly. However, this penalizes the temperature. The mentioned comparison between *Case 2* and *Case 4* has been actually performed between one $60kW$ transformer and six units of $10kW$ transformers. The important improvement in power density is mainly due to the fact that the required isolation imposes a certain distance between windings that must be maintained. Consequently, the better use of the winding area and magnetic core improves when the transferred power increases.

On the other hand, cases 1 and 3 in Table IV show the effects of increasing the cell voltage to 1 kV and 4 kV. A cell voltage of 1 kV could be a achieved using available 1.7 kV SiC MOSFET. On the other hand, a cell voltage of 4 kV could be achieved using new 6.5 kV SiC power devices. It is observed that increasing the cell voltage is advantageous in terms of HF transformer efficiency and power density. However, the temperature is slightly penalized. It is noted that, given specific isolation requirements and a rated power that fixes a particular magnetic core, it is advantageous to increase the input voltage (i.e. cell voltage). This will imply a smaller input current and thus, the required leakage inductance increases. In order to comply with those features, an increase in the number of turns is needed, meaning a decrease in the core losses (i.e. higher efficiency). It is noted that rated power of the designs has been adapted to keep the total power constant (e.g. if input voltage is reduced by half, double number of cells will be required and thus, each cell must transfer half the power to keep the same total power transfer).

Regarding the switching frequency of the power devices being used in the DAB, an increase in that variable leads to a lower required leakage inductance. Hence, number of turns will need to be reduced and core losses will be increased. However, increasing the switching frequency is not always advantageous, since core losses will be in principle simultaneously increased, eventually reducing the efficiency. A trade-off between switching frequency, rated power (which is directly related to required leakage inductance) and core losses is then required, this issue being the subject of ongoing research.

VII. Experimental Results

Fig. 12 shows the DAB prototype used for the experiments.

Some preliminary experimental tests have been performed using the HF transformer named as *Base Case* in Section VI-A.

Fig. 13 shows a three-hour temperature test with the HF transformer transferring its rated power of $5kW$. The test has been performed for two different magnetic core materials, CF138 and 3C94, as previously specified in Table III as *Base case* and *v2.0*, respectively, the improvement obtained with the second material being evident.

TABLE IV
High-frequency transformer theoretical design parameters

	Case 1	**Case 2**	**Case 3**	**Case 4**
Power	$5kW$	$10kW$	$20kW$	$60kW$
Input voltage	$1kV$	$2kV$	$4kV$	$2kV$
Efficiency	99.74%	99.83%	99.88%	99.92%
Temperature rise	$60°C$	$61°C$	$68.4°C$	$73°C$
Leakage inductance	$455\mu H$	$910\mu H$	$1800\mu H$	$152\mu H$
Power density	$49.8W/cm^3$	$60W/cm^3$	$79W/cm^3$	$176W/cm^3$

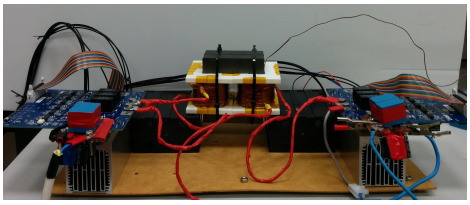

Fig. 12. Experimental 800V/5kW DAB prototype.

Fig. 14 shows the results for an isolation test (up to 24 kV) applied to the *Base case* HF transformer. The test was performed using a static tester. A DC voltage is applied to one winding while the other is grounded, obtaining an indication of the leakage current flowing through the insulation. This type of measurement provides a preliminary idea of a possible partial discharge or insulation failure. Fig. 14 also includes results for the HF transformer with a resin encapsulation. It is clear that encapsulation in some kind of insulating material provides better results since resin significantly increases the voltage surge at which isolation would be compromised. Both designs therefore comply with the 24 kV isolation requirement.

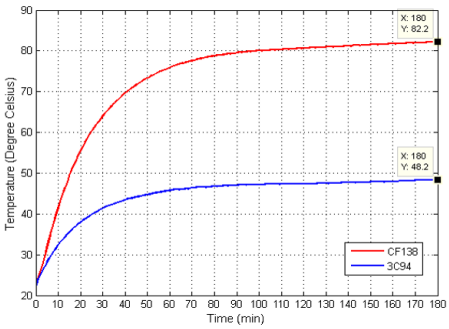

Fig. 13. Three hour temperature test for the base case HF transformer ($5kW$) with two different magnetic core materials. Red- CF138, Blue-3C94.

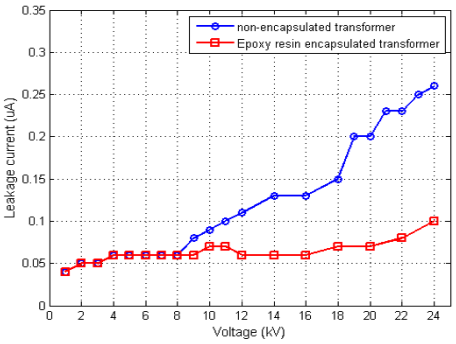

Fig. 14. Isolation test for the base case HF transformer. Blue- Non encapsulated, Red- Epoxy resin encapsulation

VIII. Conclusions

This paper analyzes modular PET designs based on CHB and MMC topologies. MMC-based topologies feature multi-port capabilities, intrinsically providing an HV–DC port, which can be key advantage compared to CHB-based solutions for certain applications. However, to withstand the same voltage in the HV ports, they require four times the number of cells and double number of devices compared to their CHB counterparts. The flexibility of MMC-based PETs to combine the power of their three ports also needs to be considered for its design and control, as it affects to the current ratings of the power devices.

Regarding the HF transformer, different core materials and coil arrangements have been studied. The availability of higher voltage switching devices (i.e. higher cell voltage) would be in principle advantageous, as it results in reduced core losses for a given isolation requirement. As a consequence, less number of submodules with higher voltage would be desirable. Similarly, for the same cell voltage and the required isolation, an increase in the rated power result in a better use of the magnetic core, achieving therefore a better performance. The availability of fast switching devices would lead in principle to higher switching frequencies, but this is not always desirable, as the core losses may significantly increase. A trade-off between switching frequency, transferred power and losses must be found.

Finally, experimental results have been provided showing the validity of the HF transformer design methodology.

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Modular Power Electronic Transformers

Modular Multilevel Converter Versus Cascaded H-Bridge Solutions

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Digital Object Identifier 10.1109/MIE.2016.2611648
Date of publication: 21 December 2016

This article analyzes two modular power converter concepts, cascaded H-bridges (CHB) and modular multilevel converter (MMC) topologies, with special attention to the latter design. Both concepts have some characteristics in common and can provide the required functionalities for power electronic transformers (PETs). This analysis will cover aspects like the number of required cells, characteristics of the power devices, functionalities, and potential uses.

Conventional line-frequency transformers (LFTs) are key elements in transmission and distribution systems to interface the different voltage levels in the grid. LFTs are a well-established technology, and they are relatively cheap, efficient, and reliable. They have several limitations, however, including voltage drop under load; sensitivity to harmonics, load imbalances, and dc offsets; no

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overload protection; and low efficiency when operated with low load levels or no load [1].

PETs, also called solid-state transformers, are envisioned as a semiconductor-based alternative to LFTs. PETs are able to provide advanced functionalities such as power flow control, reactive power, harmonics and imbalances compensation, availability of low-voltage dc (LVdc) link, and smart protection. High switching frequencies of the semiconductors also enable a significant reduction of the volume and weight of the core material [1]–[4].

Generally speaking, PETs beat LFTs in terms of power density and much superior functionalities, but PETs are inferior in terms of cost, efficiency (full load), and reliability. For this reason, there are some applications in which the use of PETs can be advantageous compared to standard LFTs. Smart-grid applications require an efficient integration of distributed generation and storage resources, flexible routing mechanisms, active filtering, and protection mechanisms. While power density might not be a key aspect for onshore applications, it can be of paramount importance for offshore applications [5]. Traction and subsea systems are also examples of space-critical applications in which the improved performance and power density of PETs compared to LFTs can be determinant [6], [7].

Practically all PET topologies provide at least a high-voltage ac (HVac) and an LVac port, therefore connecting two ac systems (see Figure 1). It is noted that the terms *HVac* and *LVac*, as well as *medium-voltage ac* (*MVac*), are generic and do not necessarily correspond to voltage ranges defined in standards. The general scheme shown in Figure 1 can be used to realize either an HVac/MVac, an MVac/LVac, or an HVac/LVac transformation according to defined voltage levels (e.g., in standard IEC 60038).

PET topologies in Figure 1 are seen to consist of three major blocks:

- one (or more) power-converter blocks to transform the grid frequency (low-frequency) ac voltage into a high-frequency (HF) ac voltage
- a central isolation block using an HF transformer
- one (or more) power-converter block to transform the HF ac voltage into a low-frequency ac voltage.

A common criterion for the classification of PET topologies is the number of energy conversion stages. While PET designs using one, two, or three stages have been proposed [5], [8], a fully modular three-stage approach [Figure 1(a)] appears to be the most popular choice [2], [9]–[11]. This configuration implies the use of capacitors in the dc links, but this enables a separate design and optimization of each converter stage. Elimination of the dc link capacitors is possible but requires the use of indirect matrix converter topologies [(Figure 1(b)]. It is also possible to reduce the number of stages to two [(Figure 1(c)] or one [(Figure 1(d)], with the use of direct matrix converter topologies being required in this case. Matrix-based approaches avoid bulky and lifetime-limited energy-storing capacitors, therefore improving power density and reliability. They do, however, require the use of a larger number of power devices, introduce constraints in their optimization, and complicate the control and protection mechanisms [5], what

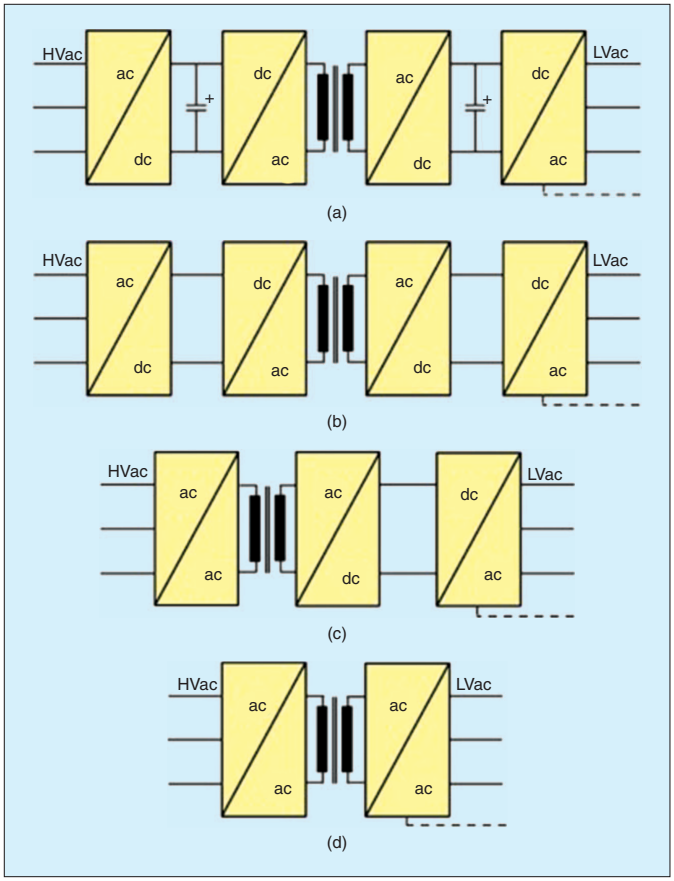

FIGURE 1 – Three-phase PET arrangements: (a) a fully modular three-stage PET including a dc link and back-to-back converters in both HV and LV sides, (b) a three-stage PET using indirect matrix converters in both HV and LV sides, (c) a two-stage PET using a direct matrix converter in the HV side and indirect matrix converter in the LV side, and (d) a one-stage PET based on using direct matrix converter. Note: LVac ports can be either three-wire or four-wire.

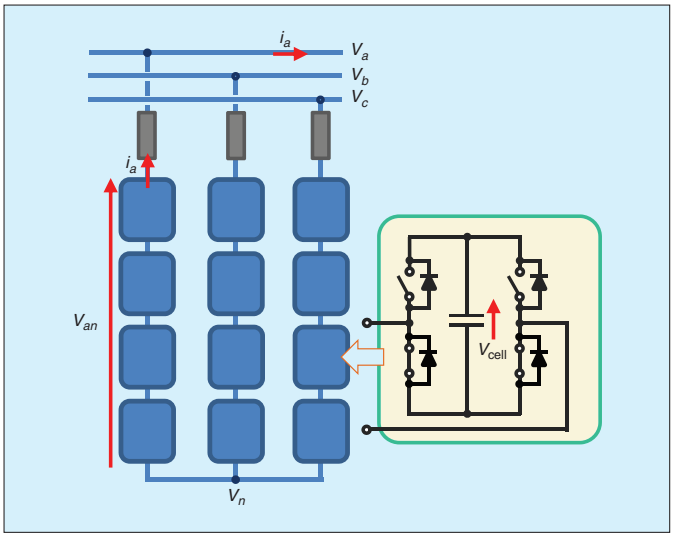

FIGURE 2 – A schematic representation of a CHB multilevel converter.

has prevented widespread industrial application [12].

One further advantage of the three-stage design shown in Figure 1 is the presence of dc links both in the HV and LV sides, enabling the inclusion of LVdc and/or HVdc ports in the PET. The resulting multiport topologies can provide additional functionalities, e.g., connection to HVdc transmission systems or the integration of energy storage devices or distributed energy resources (DER) [13], [14]. These enhancements, however, can imply an increase of the PET complexity and cost, which needs to be considered.

We have analyzed two modular PET topologies, namely CHB-based PET [11] and MMC-based PET [15], [16]. Criteria for the evaluation include number and type of the ports provided by the PET, number of cells, and number and rating of power devices. CHB and MMC topologies are introduced first. The resulting PET structures using both concepts are later analyzed. Finally, two application examples of MMC-based multiport converters are discussed: smart grids and vessels.

CHB and MMC Topologies

The CHB converter is a particular type of cascaded converter, based on the series connection of H-bridge cells. A three-phase CHB is shown in Figure 2. The cells can produce three voltage levels: v_{cell}, 0, and $-v_{cell}$ (negative v_{cell}). By series connection of the N cells in each phase, $2N + 1$ levels for the phase voltages and $4N + 1$ levels for the phase-to-phase voltages can be obtained. The implementation shown in Figure 2 does not include a dc voltage source to supply the cell voltage. As a result, its use is limited to applications that do not involve active power handling, such as reactive power and harmonic compensation. The cells' capacitors are maintained at a constant target voltage (average) by the control in this case [17], [18]. Inverter operation (i.e., power conversion between dc and ac ports) of the CHB multilevel converter is possible by feeding each cell from an isolated dc supply, which is normally obtained from multipulse diode rectifiers [19].

The most relevant properties of the CHB topology are as follows.

- High terminal voltages are achieved by just serializing identical cells.
- Voltage sharing among devices is intrinsic to the design, because the voltage blocked by each device is limited to v_{cell}.
- The design allows redundancy by simply including spare cells in the legs.
- It shares advantageous features of other multilevel topologies that are derived from the improved output voltage wave shape, e.g., reduced size of ac filters, electromagnetic interference reduction and lower switching losses thanks to the reduced switching frequency.

One distinguishing characteristic of the CHB topology shown in Figure 2, compared to other multilevel topologies like the neutral point clamped or flying capacitor, is that it does not provide an HVdc port.

The MMC can be seen as an evolution of the CHB to provide a dc port [20], [23]–[25]. The dc voltage (v_{dc}) is obtained between the neutral point of two CHBs connected in parallel, as shown in Figure 3. The desired dc voltage (1) is produced by adding homopolar voltage components v_{n1} and v_{n2} to the voltage commands of both CHBs (2), (3). This is shown graphically in Figure 4:

$$v^*_{dc} = v^*_{n1} - v^*_{n2}, \quad (1)$$

$$v^{*'}_{x1} = v^*_{x1} + v^*_{n1} \text{ with } x = a, b, c, \quad (2)$$

$$v^{*'}_{x2} = v^*_{x2} + v^*_{n2}. \quad (3)$$

If a load is now connected between both neutrals, a dc current (i_{dc}) will flow (the switch is closed at $t = t_3$ in Figure 4). Such dc current will add up to the ac currents (i_{a1}; i_{a2}) but will circulate within the converter legs, i.e., it will not show up in the grid current i_a, which remains purely ac. The grid current i_a is evenly split (ideally) between the two CHBs. The dc current i_{dc} is the so-called circulating current and is evenly split (ideally) among all three phases.

While in the scheme shown in Figure 3, the dc port is a passive load and therefore can only consume power, the power flow in the dc link can be bidirectional. The power balance equation of the MMC, neglecting losses and assuming that the cell capacitor voltages remain constant, is given by (4) and (5):

$$P_{ac} = v_a i_a + v_b i_b + v_c i_c, \quad (4)$$

$$P_{ac} = P_{dc} = v_{dc} i_{dc}. \quad (5)$$

Rearranging the two CHBs in Figure 3, the conventional representation of the MMC is obtained (Figure 5). The basic equations describing the electric behavior of the MMC (6)–(8) are readily deduced from Figure 5, where subindexes T and B stand for the top and bottom arms of the MMC, respectively [26]–[34]. The voltage drop in the arm inductors has been ignored for the sake of simplicity. It is seen from Figure 4, (7), and (8) that both arm (and, therefore, cell) voltages and currents include dc and ac components [26], [27]:

$$v_{xT} + v_{xB} = v_{\mathrm{dc}} \quad \text{with } x = a, b, c, \tag{6}$$

$$v_{xT} = \frac{v_{\mathrm{dc}}}{2} - v_x; \quad v_{xB} = \frac{v_{\mathrm{dc}}}{2} + v_x, \tag{7}$$

$$i_{xT} = \frac{i_{\mathrm{dc}}}{3} + \frac{i_x}{2}; \quad i_{xB} = \frac{i_{\mathrm{dc}}}{3} - \frac{i_x}{2}. \tag{8}$$

A key aspect in the design of the MMC is the ratio between the dc and ac port voltages, which indicates how much of the available dc bus voltage is actually used to produce the ac voltage. This ratio is given by (9) adding triplen harmonics to the phase voltages and increases to (10) (i.e., less margin between v_{dc} and v_{a}) if triplen harmonics are not used:

$$R_{\mathrm{thi}\,(pu)} = \frac{\sqrt{3}\,|v_{a\,(\mathrm{peak})}|}{v_{\mathrm{dc}}}, \tag{9}$$

$$R_{\mathrm{no\,thi}\,(pu)} = \frac{2\,|v_{a\,(\mathrm{peak})}|}{v_{\mathrm{dc}}}. \tag{10}$$

Values of R significantly lower than one indicate that the MMC has a large voltage margin between its dc and ac port voltages; therefore, it can operate without violating its voltage limits even in the event of anomalies, e.g., dc voltage lower than expected or ac voltage larger than expected. This also provides the opportunity to implement redundancy-based fault-tolerant designs [35], [36]. However, small values of R also imply a misuse of the cells. On the contrary, values of R closer to one imply a better use of the cells and power devices but at the price of an increased risk of forcing the MMC to operate without the required voltage safety margin.

Several conclusions can be reached comparing the topologies in Figures 2 and 5:

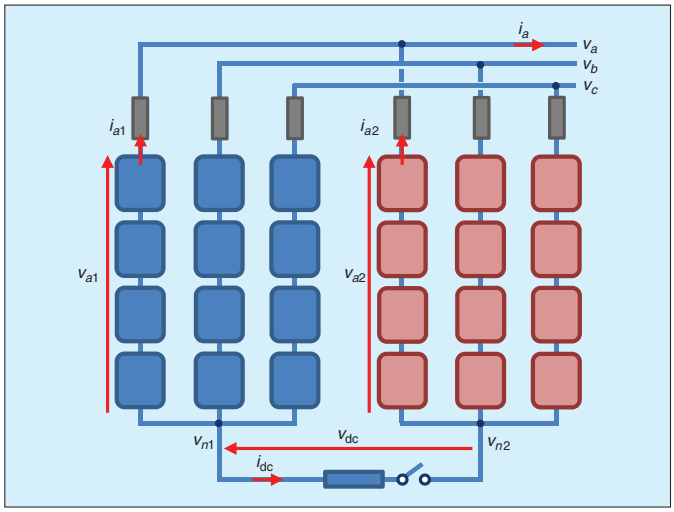

FIGURE 3 – The parallel connection of two CHB MMCs.

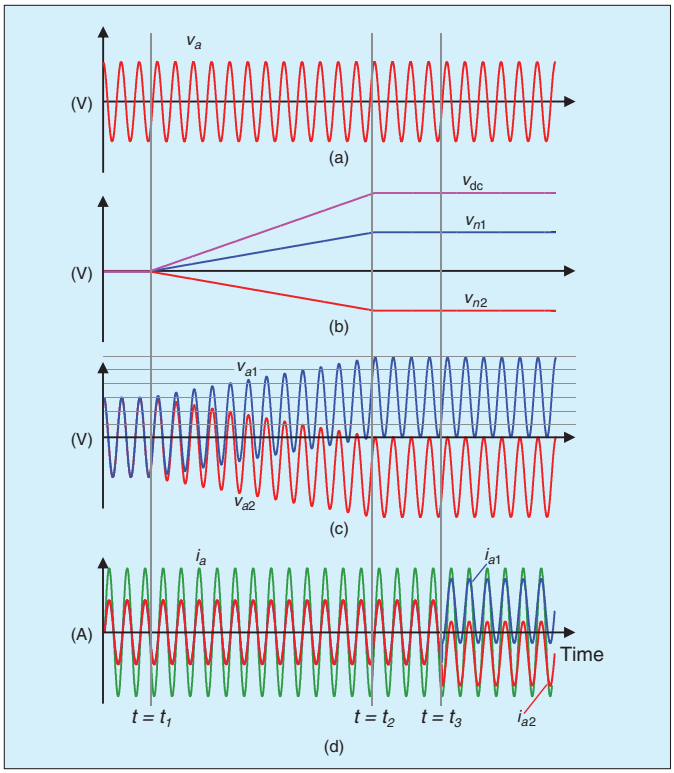

FIGURE 4 – Wave shapes for the power converter in Figure 3: (a) the grid voltage, (b) the homopolar voltage for the two CHBs and the neutral-to-neutral voltage, (c) the phase-to-neutral voltage for the two CHBs, and (d) the phase current for the two CHBs and the grid current. Only the variables for phase (a) are shown. Homopolar voltage injection starts at $t = t_1$ and reaches its steady state value at $t = t_2$. The switch connecting the two neutrals is closed at $t = t_3$.

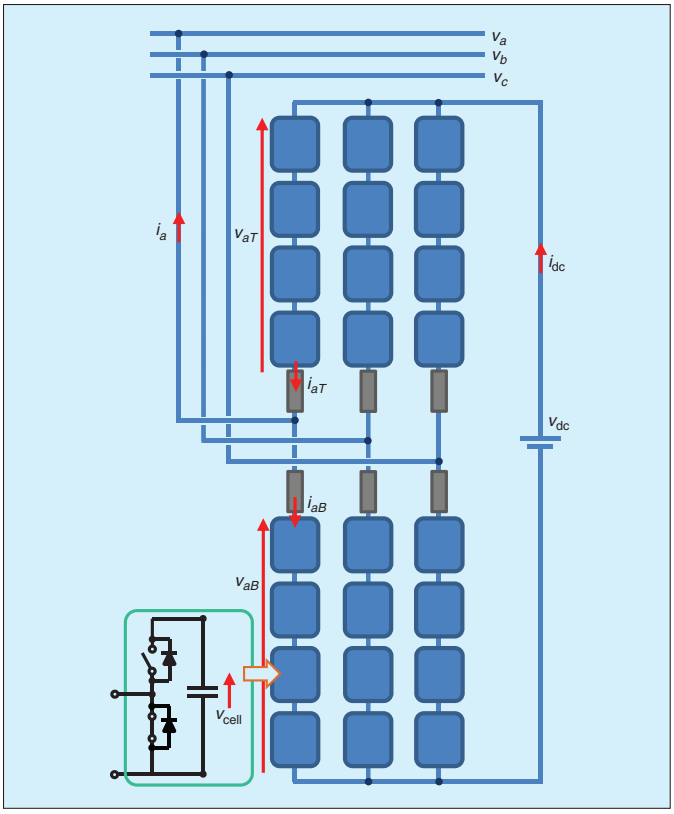

FIGURE 5 – An MMC.

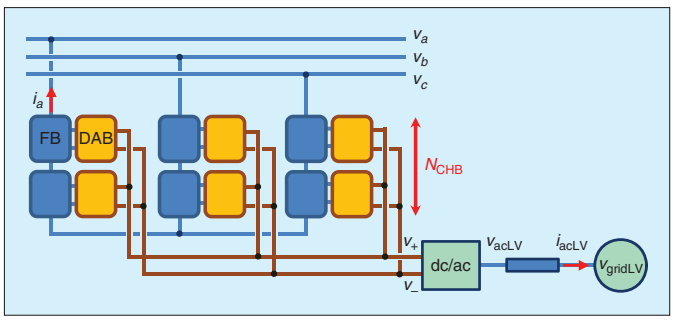

FIGURE 6 – A CHB-based PET. For the sake of simplicity, inductors connecting the CHB to the grid are not shown.

- Because of the injection of homopolar voltages v_{n1} and v_{n2}, phase-to-neutral voltages in the MMC are unipolar but of larger peak value compared to the case without injecting homopolar voltages [Figure 4(c)]. As a result, for a given ac voltage (v_a; v_b; v_c) and cell voltage (v_{cell}), the MMC requires twice the number of cells per arm, thus, four times the number of cells compared to the CHB. This can be seen as the price to pay to obtain the dc link.
- The voltage produced by the CHB cells must be bipolar, which means that full bridges are required (Figure 2). On the contrary, the voltage produced by the MMC cells is unipolar, so half bridges can be used (Figure 5).
- The use of full-bridge cells in the CHB design can result in a higher current capability, as two states are now available to bypass the cell (cell voltage equal to zero), enabling a better distribution of the losses.

A comparative analysis between the MMC and CHB topologies in terms of semiconductor requirements, efficiency, cell capacitor sizing, etc., can be found in [37]–[38].

CHB- and MMC-Based PETs

One of the most widely studied configurations for the three-stage PET in Figure 1 is derived from the CHB topology (Figure 6) [9]–[11], [15]. A dual active bridge (DAB) dc/dc converter is used to inject/drag power from the CHB cells. Figure 7 shows a detailed representation of the CHB cell and DAB. The LV side of the DAB is parallelized to form an LV, high-current dc link. A conventional dc/ac three-phase power converter (controlled rectifier) is then used to provide the LVac port. The CHB-based PET in Figure 6 performs an ac/ac power conversion with galvanic isolation, similar to the LFT, but can also implement all the functionalities that are intrinsic to the CHB (reactive power and harmonic compensation, etc.), as well as control the power flow and avoid the propagation of disturbances between the HV and LV sides.

It is possible to extend the concept used in Figure 6 to the case of the MMC, with the resulting structure shown in Figure 8, [15], and [16]. As in the CHB case, DABs are used to realize a bidirectional power transfer between the MMC cells and the LV side on the converter. Figure 9 shows the MMC cell and DAB in detail. Other MMC-based configurations can be found in [21] and [22].

The topology in Figure 6 has two ports, which perform an ac/ac transformation. On the other hand, the power converter in Figure 8 has three ports: HVdc, HVac, and LVac. The HVdc link in the MMC-based implementation in Figure 8 enables new functionalities compared to the power converter in Figure 6, but this is at the price of a significant increase in the number of cells, and consequently of power devices, passives, and auxiliary circuitry.

To illustrate the differences between the CHB- and MMC-based topologies, the particular case of a PET connecting two ac grids of 24 kV and 400 V, respectively, is discussed. This is one of the configurations being considered within the Silicon Carbide Power Technology for Energy Efficient Devices (SPEED) project [39]. A cell voltage $v_{\text{cell}} = 2\,\text{kV}$ was selected, which is equal to the DAB voltage in the HV side. The dc link voltage in the LV side is 1 kV. The DABs are designed for rated power of 10 kW.

Number of Cells

The peak-to-peak phase voltage of the HVac is 39.2 kV. The number of cells required for the CHB implementation is given by (11), where *ceil* stands for the next larger integer:

$$N_{\text{CHB}} = ceil\left(\frac{v_{\text{phase peak}}}{v_{\text{cell}}}\right). \qquad (11)$$

The HVdc voltage for the MMC-based PET topology must be larger than this value, so an HVdc of 40 kV was selected. The HVac-to-HVdc ratio without triplen harmonic injection in the ac voltage is $R_{\text{no thi}} = 0.98$. The minimum number of cells required for the MMC-based implementation is given by (12), assuming that triplen harmonic injection is not used. The minimum number of cells if triplen harmonic injection is used is obtained replacing $\sqrt{3}$ with 2 in the right side of (12). A discussion of the effects of triplen harmonic injection in the ac voltages of the MMC is found in [40]:

$$N_{\text{MMC}} = ceil\left(\frac{2 \cdot v_{\text{dc}}}{v_{\text{cell}}}\right). \qquad (12)$$

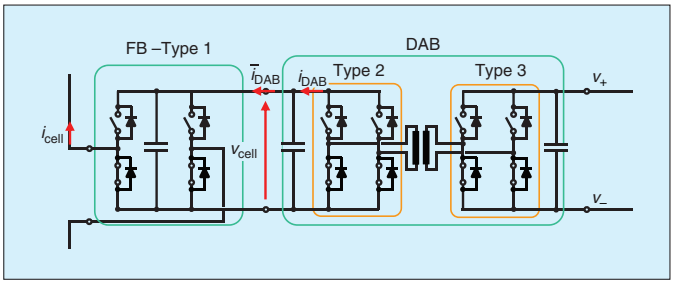

FIGURE 7 – A CHB cell and DAB for the CHB-based PET.

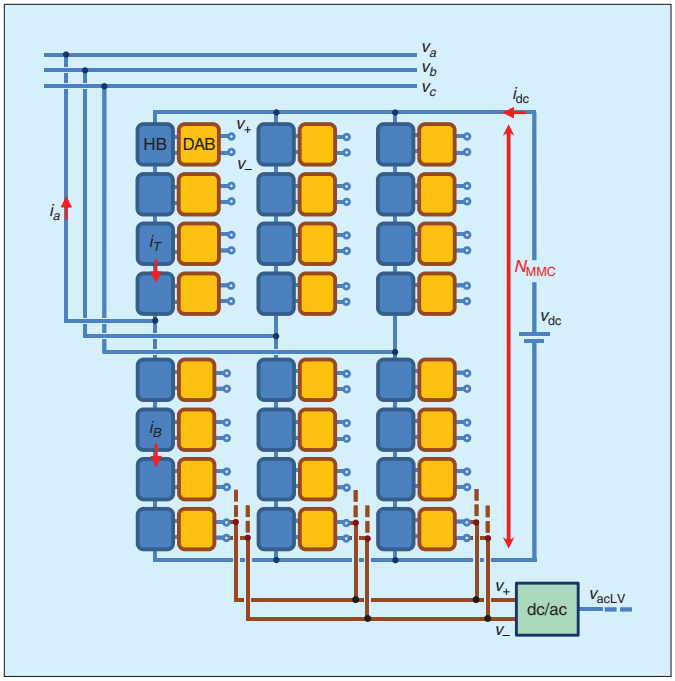

FIGURE 8 – An MMC-based PET.

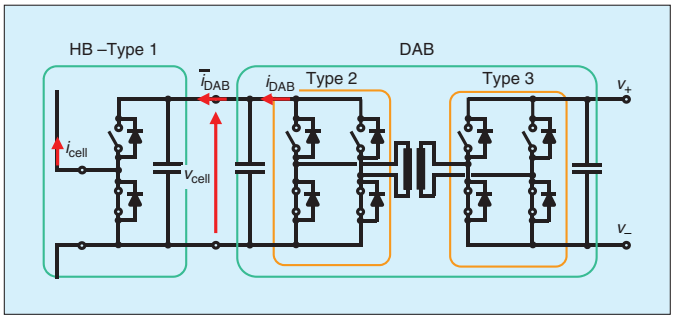

FIGURE 9 – An MMC cell and DAB for the MMC-based PET.

TABLE 1 – COMPARATIVE ANALYSIS OF CHB AND MMC TOPOLOGIES.

	CHB-BASED PET	MMC-BASED PET
v_{acHV}/v_{acHV}	24 kV/400 V (phase-phase, root mean square)	
v_{cell}	2 kV	
N_{leg}	10	40
N_{DAB}	30	120
P_{DAB}	10 kW	
P_{total}	300 kW	1,200 kW
# devices*	120	240
$i_{cell\text{-}peak}/IDAB$	$\sqrt{3}$	$2+4\sqrt{3}$

*Only CHB and MMC cells are considered. DAB power devices are not included.

TABLE 2 – HF TRANSFORMER PARAMETERS.

Rated power	10 kW
Switching frequency	50 kHz
Leakage inductance	950 μH
dc link voltage on HV side	2 kV
Turns ratio	2:1
Primary-to-secondary isolation	24 kV
Core material	CF138

Table 1 shows the main constructive characteristics for both implementations. It is observed that for the same HV side voltage, the MMC-based design requires four times the number of cells of the CHB-based design. However, the number of devices for the MMC case is only double than for the CHB case, as the second uses full bridges while the first requires half bridges. It is also worthwhile to note that the power transferred between the HV and LV sides for the MMC-based implementation is four times the power of the CHB implementation. This is due to the fact that the DABs in both configurations have the same ratings, but the MMC-based PET uses four times the number of cells of the CHB case.

Power Device Requirements and HF Transformer

There are significant differences in the requirements for the power devices in the circuits shown in Figures 7 and 9. In the following discussion, type 1 devices are the power devices in the full bridge (FB) and half bridge (HB) connecting the DABs with the high-voltage ports of the PETs. Type 2 and type 3 devices refer to the devices in the HV and LV sides of the DAB, respectively.

All the devices in the HV side withstand the same dc link voltage. Consequently, they should have the same (or similar) voltage rating, albeit with different commutation requirements and current ratings. Commutation requirements for type 1 devices in CHB and MMC cells are low due to their multilevel nature [18], [41]. In the limit, a switching frequency as low as the fundamental frequency can be achieved using staircase modulation, provided that the number of levels is large enough [42], [43]. Diodes in CHB and MMC cells must conduct for relatively long periods of time, so free-wheeling diodes with low conduction losses are therefore preferred. Considering the dc link voltage of 2 kV and the commutation requirements, a 3.3-kV silicon (Si) insulated-gate bipolar transistor, using either Si or Si carbide (SiC) free-wheeling diodes, are an adequate solution.

To reduce the size and weight of the HF transformer, a high switching frequency (in the range of several tens kHz) is desired in the DAB. For the required dc link voltage and switching frequency, a modern 3.3-kV SiC metal—oxide—semiconductor field-effect transistor (MOSFET), with a peak current of 15 A, is a good candidate for the type 2 device.

The operation of the DAB in nominal conditions provides zero voltage switching, which is needed to achieve high efficiency with high switching frequencies. A straightforward control method for the DAB is the phase-shift modulation. This requires a careful selection of the leakage inductance of the HF transformer. Values that are too low imply nonzero voltage switching under low loads, whereas values that are too large can limit the maximum power [44]. This second case is more likely to occur due the isolation required between the primary and secondary sides of the HF transformer to guarantee galvanic isolation between the HV and LV sides of the PET. It is finally noted that the zero voltage switching range is ideally not limited for the case of an input/output voltage ratio equal to one (both referred to the same side of the transformer). This is not necessarily true in practice, however, due to the parasitic capacitances of the switches. The main parameters of the HF transformer are given in Table 2, its design and construction being a challenging task [45].

As phase-shift modulation is used to control the power transfer between the HV and LV sides of the DABs, identical switching characteristics are desired for type 2 and type 3 power devices. Since the voltage in the LVdc link is half of the voltage in the HV side, type 3 devices should be rated for approximately half the voltage and twice the current of type 2 devices (a 1.7-kV SiC MOSFET is considered adequate). Synchronous rectification can be used, meaning that the requirements for the diodes are low, so the MOSFET body diode can be enough.

All the power transferred by the DAB must be delivered by the FB (13) (losses neglected). The relationship between the peak current for type 1 (FB) and type 2 (DAB) devices for the CHB case is then given by (14):

$$P_{acLV} = P_{DAB\text{-}total} = -P_{acHV}, \quad (13)$$

$$\frac{i_{cell\,peak}}{\overline{i}_{DAB}} = \sqrt{3}. \quad (14)$$

It is noted that i_{cell} is an ac current at the grid frequency (50 or 60 Hz typically). On the contrary, i_{DAB} is an HF pulsated current, $\overline{i}_{DAB}$ being its average (dc) value, so the DAB peak current can be roughly approached by $i_{DAB\,peak} \approx 1.3\ \overline{i}_{DAB}$.

Selection of the current ratings for the MMC-based PETs is not so straightforward. The multiport nature of this design opens new possibilities to split the power among the three ports, which affects to the current ratings of the power devices. Neglecting losses, the power balance in this case is given by (15) and (16):

$$P_{dcHV} + P_{acHV} + P_{DAB\text{-}total} = 0, \quad (15)$$

$$P_{\text{DAB-total}} = P_{\text{acLV}}. \quad (16)$$

Figure 10 shows the relationship between the MMC dc current i_{dc}, ac peak current i_{a} peak, and arm peak currents i_{cell} peak (MMC) when the DAB is transferring its rated current, i.e., PDAB-total is at its rated value. The peak current for CHB-based PET cells i_{cell} peak (CHB) is shown for reference. Minimum current in the type 1 devices is obtained for $P_{\text{dcHV}}/P_{\text{DAB-total}} = -1$, i.e., the power injected by the DAB being entirely delivered to the dc port of the MMC. For $P_{\text{dcHV}}/P_{\text{DAB-total}} = 0$, all the power injected by the DABs is delivered to the ac port. In all the other cases, the power injected by the cells is split between the ac and dc ports of the MMC. Control strategies to achieve this are discussed in the section "MMC-Based PET Control." Table 3 summarizes the requirements for the power devices in the MMC design.

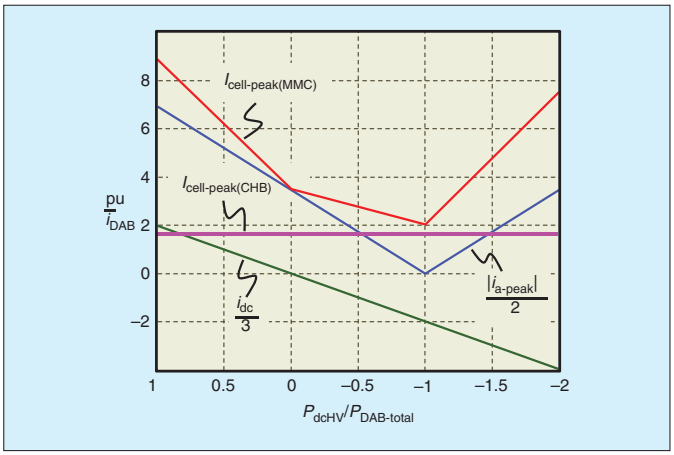

FIGURE 10 – The peak current of the MMC- and CHB-based PETs as a function of $P_{\text{dcHV}}/P_{\text{DAB-total}}$. $P_{\text{DAB-total}}$ is constant and equal to its rated value. Currents are shown in per unit (pu) of the DAB average current.

MMC Control

Control of the MMC involves multiple objectives, which must be satisfied simultaneously. The control must maintain all the cell capacitors at their target voltage. This implies matching the power of the MMC ac and dc ports. Additional control targets can include minimization of the switching losses, minimization of the cell capacitor voltage ripple or minimization of the harmonic content of the circulating current [33], [46], [47]. Some of these targets conflict, however, and trade-off between targets must be part of the control strategy. There is a wide literature on MMC control strategies [23], [26], [27], [31]–[34], and detailed discussion of this topic is beyond the scope of this article. To illustrate the difficulty of the control, a potential implementation is shown in Figure 11. The ac power references are transformed into *d*- and *q*-axis current references, with synchronous proportional-integral current regulators being used to obtain the required ac voltages (ac power control block). The circulating current control block matches the power of the dc and ac ports by controlling the circulating current through the top and bottom arm voltages. Arm voltages are then transformed into cell voltages. Modulation of the commanded cell voltages must be combined with a sorting algorithm to avoid imbalances among the capacitor voltages [23], [24], [34]. This is done by the balancing and modulation block in Figure 11.

TABLE 3 – REQUIREMENTS FOR THE POWER SWITCHES.

	TYPE 1	TYPE 2
Switching frequency	×100 Hz	×10 kHz
Transistor current	×10	×1
Diode current	Large	Small (dead-time)

MMC-Based PET Control

Different approaches can be considered for the control of the CHB-based and MMC-based PETs in Figures 6 and 8. If the voltage in the ports is established externally (i.e., by the grid), then a grid-feeding strategy can be used. The power transferred by the port is controlled in this case. On the contrary, if the voltage in a port must be established by the PET, a grid-forming strategy is needed. The target of the control in this case is to maintain the desired voltage. Since the power transferred is not controlled, some inner control loop is needed to guarantee that the current limits of the converter are not surpassed. It is not possible to configure all the ports in the grid-forming mode, as the power balance cannot be guaranteed in this case. Consequently, at least one port must be configured in the grid-feeding mode. Regardless of the strategy being implemented, the control must always maintain the internal capacitor voltages at their target value.

As an example, two different control strategies for the MMC-based PET are briefly described here. In the first case (Figure 12), all three ports are configured in the grid-feeding mode. This means that there is full control on the power transfer among ports. In the second case (Figure 13), the LVac port is configured in the grid-forming mode.

MMC-Based PET with a Grid-Feeding Configuration

This configuration is shown in Figure 12. All the PET terminal voltages (v_{acHV}, v_{dcHV} and v_{acLV}) are already present. The LVac ($P^*_{\text{DAB}} = P^*_{\text{acLV}}$) and HVac ($P^*_{\text{acHV}}$) powers are commanded values, the central control regulating P_{dcHV} to match the power equation. The control consists of three major blocks.

- MMC is a centralized control [48] that implements the normal functionalities, i.e., control of the HVac

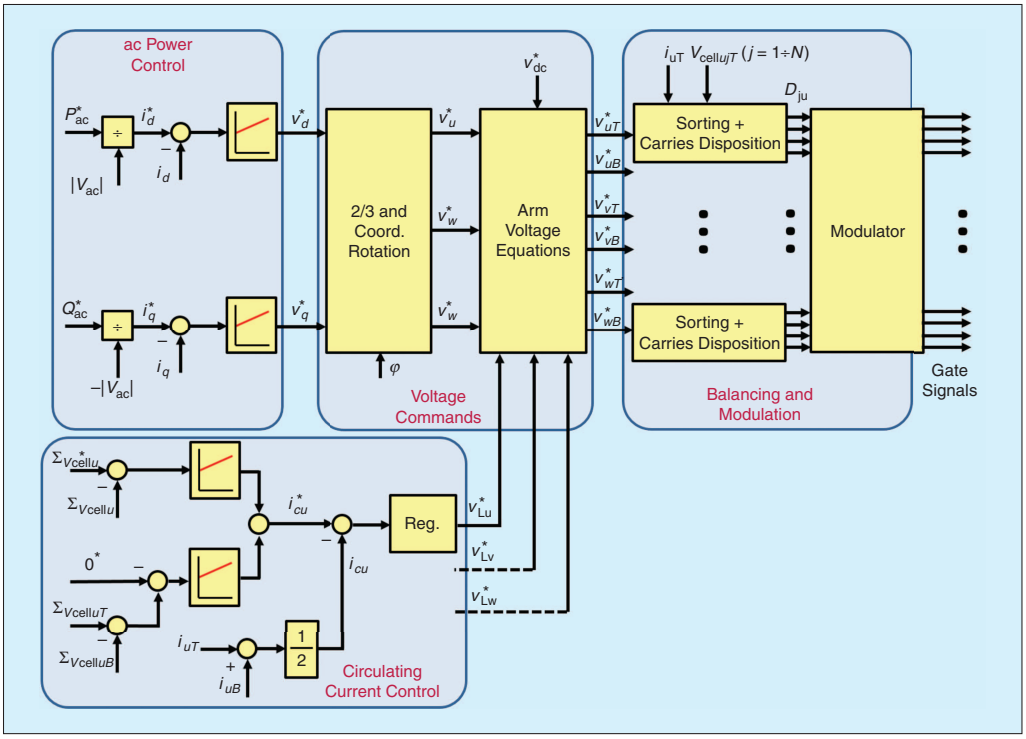

FIGURE 11 – A schematic representation of the MMC control.

and HVdc port currents as well as the current of the cell capacitor voltages v_{cell} [26], [27], [35]–[41].

- It is advantageous to distribute the DAB control in each cell, as the DABs operate independently (even if they all receive the same power command) and at much higher switching rates than the MMC cells [48]. The DABs connect two ports of constant (controlled) voltages, v_{cell} and v_{dcLV}, operating therefore as a current source.
- Having a dc/ac converter in the LV side allows the converter to operate as a conventional controlled rectifier [49]. Commanded values for the active rectifier are the dc link voltage v^*_{dcLV} and the reactive power Q^*_{acLV}. The control will match P_{acLV} with $P_{DAB\text{-}total}$ through the d-axis component of i_{acLV}, which is required to maintain the dc link voltage v_{dcLV} at its target value.

Figure 14 shows the response of the control strategy shown in Figure 12. Commanded values are P_{acHV} and P_{DAB}. The MMC is enabled at $t = 10$ ms, and the active power command is 100 kW [Figure 14(a)]. Initially the DABs do not transfer power, so the power in the dc link of the MMC [Figure 14(b)] matches the ac power plus the converter losses. At $t = 0.3$ s, the DABs are commanded to transfer a total of 40 kW, which is supplied by the controlled rectifier in the LV side [Figure 14(d)]. To keep the power balance, the power supplied by the dc bus of the MMC is decreased by the same amount. The active power in the controlled rectifier and the power in the dc link of the MMC are internally controlled to balance the power.

MMC-Based PET with a Grid-Forming Configuration

This configuration is shown in Figure 13. The MMC-based PET must provide in this case a voltage reference in the LVac side, v_{acLV}. Major control blocks are the same as in the case of the grid-feeding configuration in Figure 12, with some relevant differences.

- DABs now regulate the LVdc bus, v_{dcLV}. The corresponding command is received from the central control unit.
- With the dc/ac converter in the LV side, the converter is now controlled to create the LVac grid. The corresponding commands for the magnitude $|v^*_{acLV}|$ and frequency f^*_e of the LV grid are received from the central control.

Uses of the MMC-Based Multiport Power Converter

Potential applications of the MMC-based topologies include those requiring a multiport power conversion with MVdc/HVdc and MVac/HVac ports. The configuration shown in Figure 8 provides three ports: HVdc, HVac, and LVac. With relatively minor modifications, however, other configurations

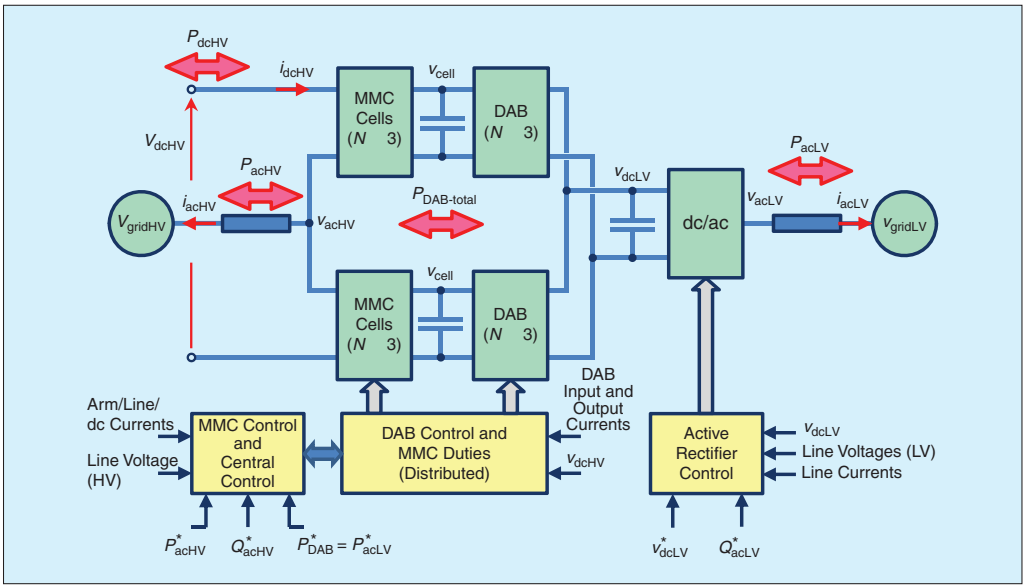

FIGURE 12 – A schematic representation of a grid-feeding control structure of an MMC-based multiport power converter. Variables with * indicate commanded values.

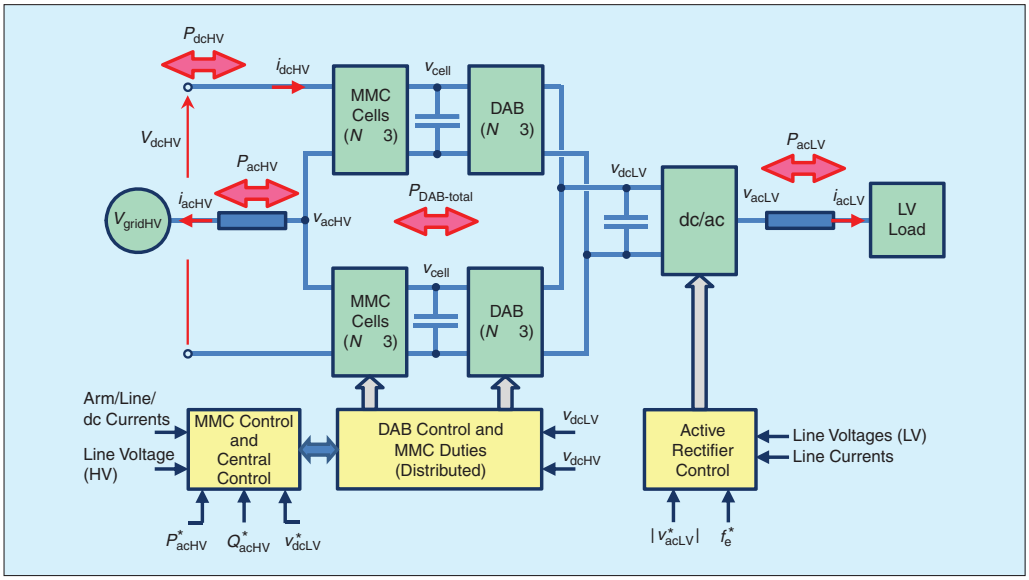

FIGURE 13 – A schematic representation of an LV side grid-forming control structure of an MMC-based multiport power converter. Variables with * indicate commanded values.

can be obtained in the LV side. Two uses of the MMC-based implementation are 1) integration of DER and/or energy storage at the cell level and 2) its use in vessels.

DER and Storage Integration

In the configuration shown in Figure 8, all the MMC cells are parallelized via DABs to form a full-power/LVdc bus. It is possible, however, to connect elements to the dc link of the cells, e.g., energy storage [13] or DER [14], as shown in Figure 15. The converter connecting the DER/energy storage to the MMC cell does not necessarily

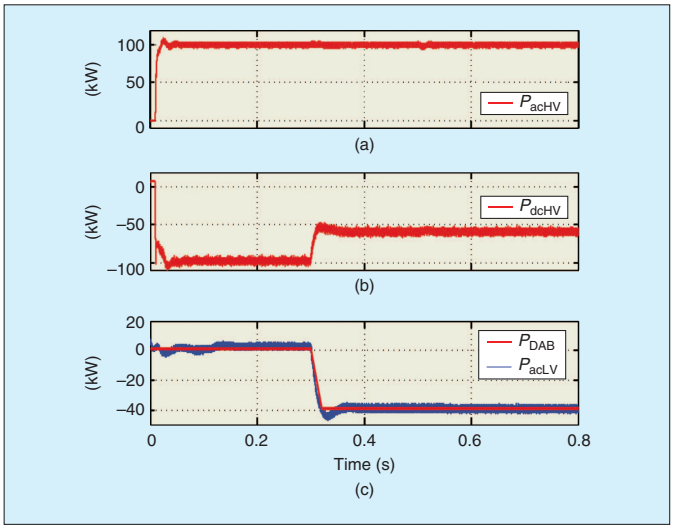

FIGURE 14 – Simulation results for an MMC-based multiport power converter with grid-feeding control. If the power has positive values, it flows from the PET port to the grid; if the power has negative values, it flows from the grid to the PET port. (a) Active power in the HVac port. (b) Power in the HVDC port. (c) Total power injected by the DABs and active power in the LVac port.

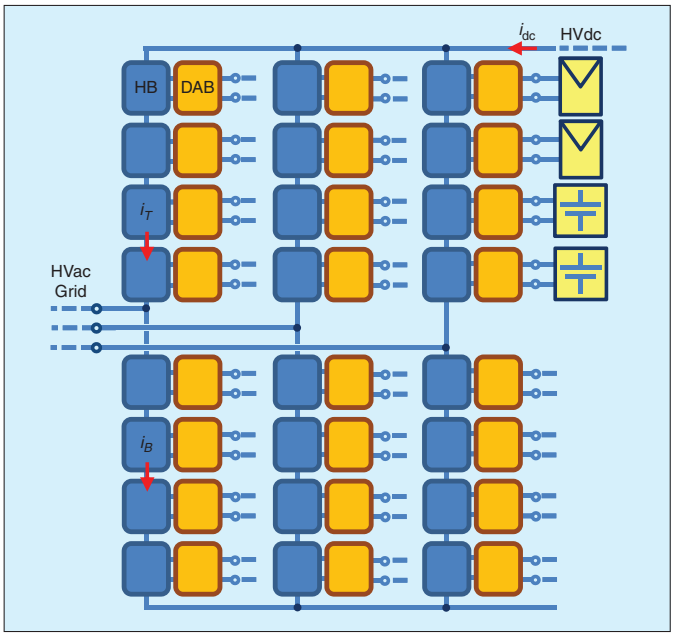

FIGURE 15 – The DER and/or energy storage integration in an MMC.

have to be a DAB, but can be optimized instead for specific needs (galvanic isolation, bidirectional power flow, etc.).

One concern for the configuration shown in Figure 15 is an imbalance in the power being transferred by each cell of the MMC. Existing control

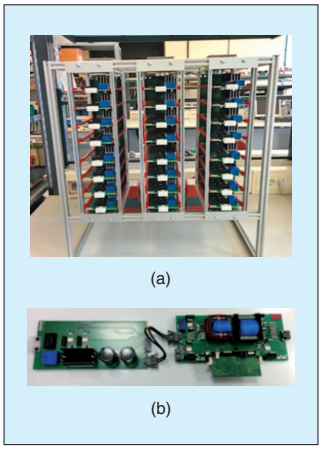

FIGURE 16 – An MMC-based PET prototype: (a) front view and (b) an MMC cell (HB, left) and DAB (right), including the HF transformer.

methods for MMCs assume that all the cells have identical design and operate identically, meaning that both dc and ac components of the overall voltages in (7) are evenly split among cells. Imbalances in the power transferred by the cells (e.g., due to panels receiving different solar radiation, or batteries operating with different states of charge) will necessarily result in imbalances among the cell voltages, as the current is common to all the cells in each arm. This is illustrated using the MMC-based PET prototype shown in Figure 16. Figure 17 shows the wave shapes for the MMC ac port and the dc link voltage of two cells during normal (balanced) operation. Figure 18(a) shows the dc component and the magnitude and phase of the ac (50 Hz) component of the cells voltage for the top arm, both for the case when the cells do not transfer power (conventional MMC) and when one cell per arm transfers power. The bottom arm behaves similarly and is not shown. The power transferred by the cells P_{cell} is 20% of the ac power P_{ac}. The imbalance in the power transferred by the MMC cells is seen to produce an imbalance in the cells voltages. Figure 18(b) shows the power in the dc and ac sides of the MMC, as well as the power transferred by the cells. The MMC is controlled to maintain constant power in the ac side,

meaning that power transferred by the cells is reflected in the power in the dc side of the converter.

Depending on the type asymmetry in the power (i.e., asymmetric among phases, arms, or cells), different types of imbalances can occur in the cell voltages and in the HVac port voltage [50], [51]. Figure 18 shows a stable system, but power imbalances can force certain cells to reach their voltage limits. This will occur when the commanded voltage for a cell is less than 0 or greater than v_{cell}). If this occurs, the ability to control will be lost. Control strategies to cope with this situation should therefore be implemented if this condition is foreseen [51].

Use of the MMC-Based Multiport Topology in Vessels

Large vessels require complex electrical power systems, which must combine a large variety of main and auxiliary generation units, loads, and storage systems, with powers that can go up to several tens megawatts. The Green Port concept, which aims to reduce pollution when the vessel is at port, implies the integration of storage systems (e.g., batteries or flywheels) with their corresponding power converters. Onshore power supply can be either LV (400–700 V) or MV (6–11 kV).

Traditional power systems for large commercial vessels are characterized by an MVac distribution, which is supplied by diesel generator sets. MVdc is considered a promising technology to improve power system performance [52], [53]. The IEEE Standard 1709 establishes 6, 12, 18, 24, and 30 kV as the preferred MVdc levels for future vessel designs [54]. Compared to MVac distribution, MVdc has several well-known advantages:

- no need for phase angle synchronization of sources, thus simplifying connection and disconnection of different devices
- reduction of the size and ratings of switchgear and cables and elimination of bulky low-frequency transformers
- improved fault management and system reconfiguration
- elimination of reactive current
- removal of frequency constraints from the design and operation of generator sets.

The ac distribution systems still have two major advantages over the dc option:

- the requirement to supply ac voltages to conventional transformers
- the significantly lower cost for circuit breakers for ac than for dc.

Connection of such a variety of sources and loads in a flexible, controllable, and reliable manner requires the intensive use of electronic power converters. Figure 19 shows a schematic representation of the future onboard grid based on MVdc [53], in which large generators (powered by diesel engines or gas turbines) and propulsion motors coexist with a variety of distributed resources. The need for an MVdc link makes the MMC-based multilevel power converter a candidate able to cope with such requirements.

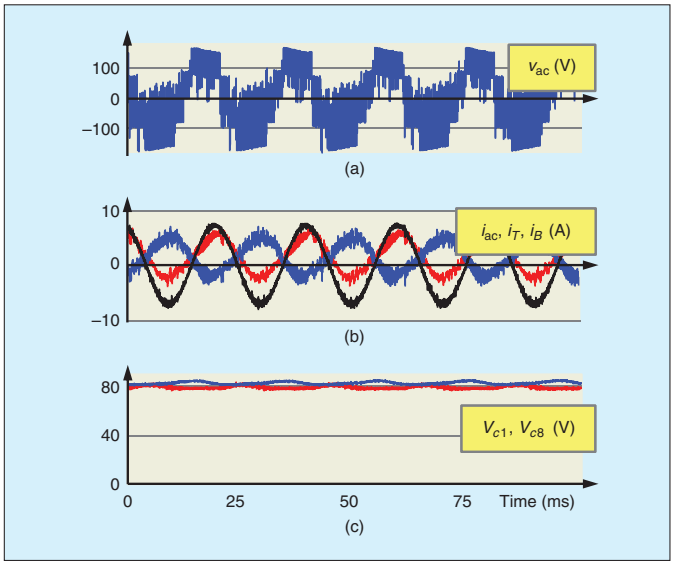

FIGURE 17 – Experimental results: (a) the ac output voltage of the MMC; (b) the top-arm, bottom-arm, and ac-output current of the MMC; and (c) the dc link voltage for cells 1 and 8.

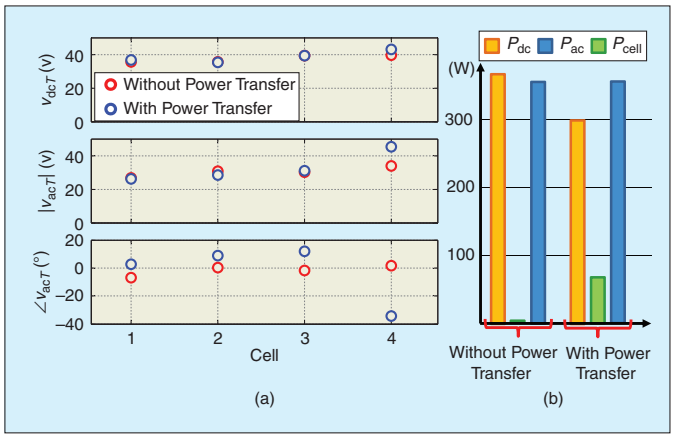

FIGURE 18 – Experimental results: (a) the dc and ac component of the cell voltage (results only for cells 1–4 shown) and (b) the dc, ac, and cell power without/with cell power transfer. P_{ac} remains constant when the cells transfer power.

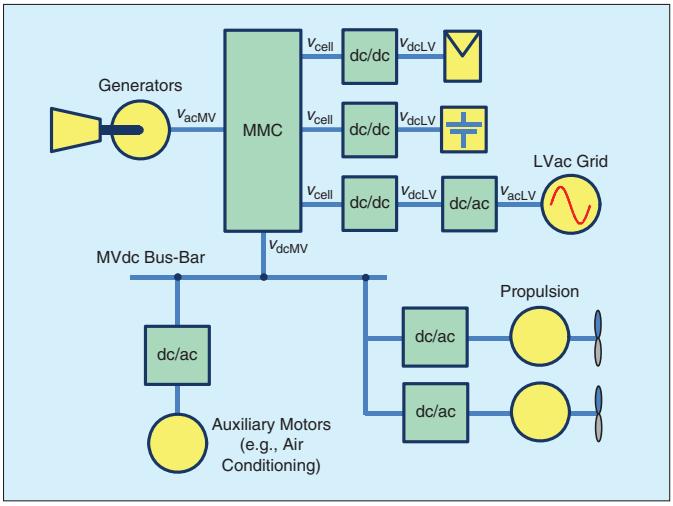

FIGURE 19 – A schematic representation of an onboard architecture in vessels using an MMC-based multiport power converter with an MVdc link.

Conclusions

CHBs are one of the most widely studied configurations for the three-stage PET. It is possible to extend the concept to MMC topology. The resulting MMC-based topology features multiport capabilities, intrinsically providing an HVdc port. To withstand the same voltage in the HV ports, MMC-based implementation requires four times the number of cells and twice the number of power devices compared to their CHB counterparts. Examples of applications in which MMC-based multiport topologies can be advantageous include integration of LV DER and/or energy storage in HVdc systems, and power systems in vessels.

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Start-up, functionalities and protection issues for CHB-based Solid State Transformers

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***Abstract*—Solid State Transformers (SSTs) are envisioned as an alternative to conventional Line Frequency Transformers (LFT) able to meed with the requirements of future power systems. Intensive studies covering SSTs' applications, topologies, functionalities and the performance are in progress. Other relevant aspects to consider are the startup (energization) of the transformer as well as its behavior and potential control strategies in the event of anomalies, e.g. imbalances in the load or even short-circuits. This papers addresses all these issues for CHB-based SSTs.**

I. Introduction

Nowadays Solid State Transformers (SST) are an under way technology which copes with the current requirements in power systems in terms of power quality and funcionalities..Their denomination as transformers can lead to a comparison with the conventional LFT. However their features are quite different.

LFTs are reliable, efficient at rated load and relatively cheap. However, they are not controllable. On the contrary, SSTs are able to provide advanced functionalities such as power control, harmonics and voltage imbalance compensation. However, SSTs are significantly more expensive, their construction and operation placing multiple challenges. Potential applications may be focused on renewable energy and smart grids [1] [2].

A remarkable feature of SSTs concerns the capability of handling voltage imbalances in the grid. Such imbalances could be handled in the more convenient way for the grid through the control of the SST.

On the other hand, SSTs do not present the robustness of LFTs, hence, reliability and operativity must be ensured. In this aspect, overcurrent and overvoltage protections must be considered. Overvoltages can be handled by means of protection devices installed in the SST ports. However, overcurrents can be managed via the control and the presence of filters.

Complexity of the SSTs also adds new aspects that must be considered, such as start-up and circuitry power supply. The start-up or energization procedure implies the design of a charging circuit which prevents the SST from peaks currents during the capacitor pre-charging stage. On the other hand, the supply for the auxiliary circuitry is not an easy task considering low number of cells and high voltage power devices.

This work was supported by the European Commission FP7 Large Project NMP3-LA-2013-604057, under grant UE-14-SPEED-604057

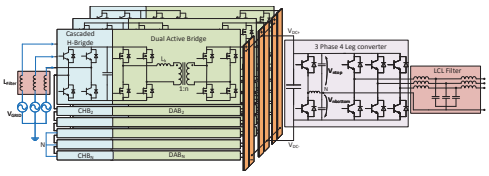

Fig. 1. SST based on CHB

The SST behavior under imbalances, harmonics compensation and reactive power control are studied in this paper. Moreover, auxiliary power supplies, start-up circuit,overvoltage and overcurrent protections are also assessed.

II. CHB-based SST

The SST studied in this paper (Fig 1) is based on a Cascaded-H Bridge (CHB) topology [1]. Conventional CHBs use capacitors as the only storage element in the cells and cannot therefore transfer power. Power transfer capability can be achieved by adding DC/DC converters with galvanic isolation at the cell level, the Dual Active Bridge (DAB) being the preferred topology. DABs can then be parallelized in the low-voltage side to obtain a low-voltage DC bus. The subsequent DC/AC converter in the low voltage side can be either 3-phase 3-wires, or 3-phase 4-wires if a neutral voltage is required. This second case is shown in (Fig 1).

III. SST Control and Functionalities

The SST described in the previous section is able to control the power flow as well as to realize reactive power control, harmonic and imbalance compensation. General principles of control as well as discussion of SST functionalities are addressed in this section.

There are two major control strategies for both sides of the converter, namely grid feeding and grid forming (Fig 2). Grid feeding mode assumes that the grid voltages already exist, the SST operating as a current (or power) source. In the grid forming mode, the SST is fed from one port (e.g. HVAC port), behaving as an ideal voltage source in the other port

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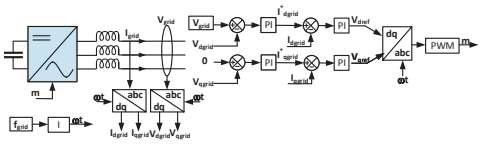
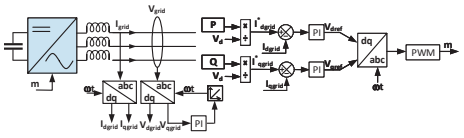


(a) Grid forming



(b) Grid feeding

Fig. 2. Control structures

(e.g. LVAC port), setting the voltage (magnitude,frequency and phase angle) demanded by a central controller. In both cases, power in the HV and LV sides must be balanced.

A. Imbalance compensation

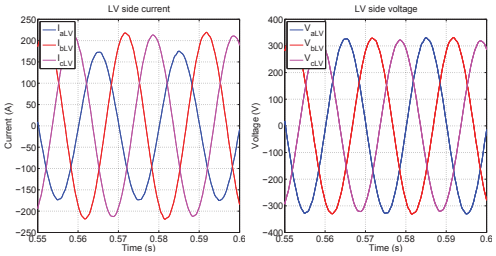
Imbalances in three phase systems are caused by different power demand in the phases [3]. This leads to current imbalances (Fig 3), eventually producing a pulsating power (Fig 3). LFTs will transfer the imbalances from the secondary to the primary, as they have no voltage regulation capability. On the contrary, SSTs have the capability to compensate imbalances by using positive, negative and zero sequence control loops (Fig 4) [4], keeping the positive sequence at the target value.

In addition the effect of the imbalance in the HV side is quite important since it can distort the HV grid. In principal its transference to the HV side can be decided by the control of the SST. For example, it can be transferred as a negative sequence in the HV side keeping a balanced three-phase system, or on the contrary, it can be directly transferred to the HV side as an umbalanced three-phase system. However the DC bus capacitors in each stage will play a important role. High capacitance capacitors can adsorb the imbalance but they are bulky. Therefore there is a trade-off between power quality, prize and size.

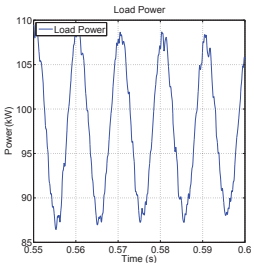
In this paper, the control structure (Fig 4) has been implemented in LV side with a 3-phase four leg inverter, with the fourth leg decoupled from the three-phase inverter. This simplifies the control since the neutral branch is controlled independently from the others. Therefore the SST with a 3P4L inverter in the LV side can handle individual single phase loads keeping the voltage within its nominal value according to the control capability [3]. In addition DC bus capacitor values are taken into account for different results.

B. Harmonics compensation

Harmonics are mainly produced by nonlinear and time varying loads. They produce a distorted current waveform that



(a) LV current (b) LV voltage



(c) LV total power

Fig. 3. Power imbalance in the LV side

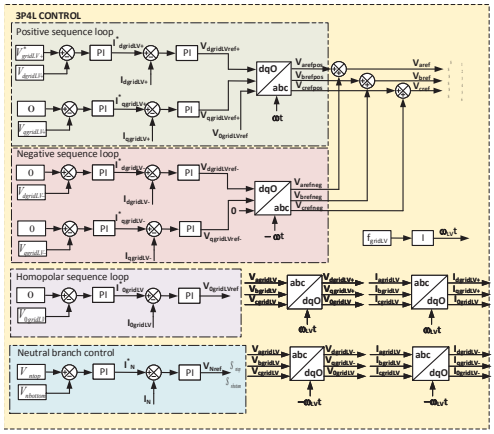
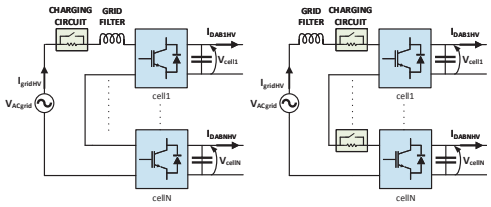


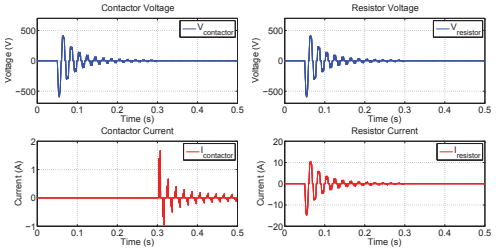
Fig. 4. 3P4L control structure

can be decomposed in the a fundamental component at the grid frequency plus a series of components at integer multiples of the supply frequency. The control applied for the SST is based on synchronous reference frame, so the voltage and currents at the fundamental frequency becomes constant magnitudes (DC value), which are easily compensated by synchronous frame PI regulators. Harmonics cancellation requires of harmonic



(a) Single charging resistor (b) Charging resistors distributed in the AC side of the cells

Fig. 5. Charging resistors disposition



(a) Magnitudes in the contactor (b) Magnitudes in the resistor

Fig. 6. Voltage and current in (a) contactor and (b) resistor

current regulators which consist of PI regulators connected in parallel. Each regulator is tuned for cancel a frequency component [5].

C. Reactive power control

SST is able to compensate reactive power in the node where it is connected. This feature cannot be accomplished with LF transformers because disturbances are reflected between their windings. In the SST, the reactive power is controlled through the q axis current (Fig 2). However this control is not assessed in this paper.

IV. Start-up

Start-up of the SST is not trivial. First, the cell capacitors must be charged. This must be done without jeopardizing internal elements of the SST or tripping protections e.g. due to excessive currents. Assumed that there is no extra circuitry for the initial charge of the capacitors, the charging process will occur through the free wheeling diodes, which will operate as a uncontrolled rectifier. Charging resistors are needed for this purpose. A contactor is connected in parallel with the resistor to by pass it once the charging process is complete. As the SST is a bidirectional converter, charging of the cell capacitors can be realized either from the low voltage side or from the high voltage sides,both cases are discussed following.

A. Start-up from the HV side

Starting the SST from the HV side is in general challenging, as the auxiliary circuitry must withstand large voltages. Two options have been considered: a) single charging resistor (Fig 5-a); b) distributed charging resistors, with the resistors placed in the AC side of the cells (Fig 5-b).

1) Charging resistors in the cell AC side: Distributing the charging circuit in each cell (Fig 5-b) ,reduces the voltage requirements for the contactor and the resistor. This allows to split the high voltage among cells, LV contactors and resistor can therefore be used in this case.

Fig 6 shows a simulation of the charging process using a resistor of 40Ω for the case of a 6kV grid voltage and a SST with 7 cells per phase.

B. Start-up from the LV side

Start-up the SST from the LV voltage side has to consider the particularities of the LV inverter. The 3 phase 4 wire applied on the SST has the DC bus is split in two DC buses (Fig 7) which are interconnected in the Neutral point. Therefore, each bus is charged to the peak phase voltage (Fig 8-c), so the overall value is twice the mentioned magnitude.

In the SST introduced in this paper, the low voltage grid is $400V$ 50Hz which means a DC bus of $650V$ (Fig 8-d).

Regarding the charging circuit is based on the previous section arrangement.This means a resistor which is bypassed once the steady state value is reached in the DC bus (Fig 8-d).The most suitable location of this circuit is at the LV port (Fig 7) between the filter and the LV terminals, because it limits the inrush current in the inverter and in the LCL filter. Other set-ups have been studied, such as a charging circuit in the DC lines between both converters, but this implies problems with the current path during the start-up, which lead to an equally charge of the DC ideal capacitors.

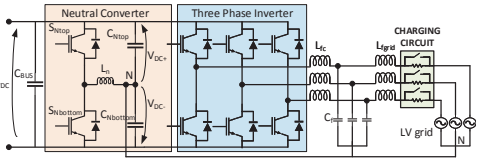


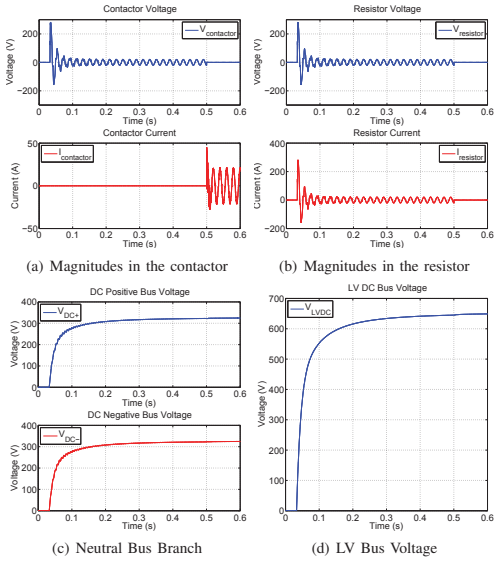
Fig. 7. Charging circuit in the Low Voltage Inverter

V. Overcurrent and overvoltage protection

SSTs intended to be installed in power systems should provide increased reliability and robustness against anomalies occurring in the grid [6]. These anomalies can be in general of two types: a) overcurrents, normally due to short-circuits, and b) overvoltages. Their effects on the SST as well as remedial actions are discussed following.

A. Overcurrents

Overcurrents will occur whenever the equivalent impedance at the terminals of the SST becomes excessively low or even



(a) Magnitudes in the contactor (b) Magnitudes in the resistor

(c) Neutral Bus Branch (d) LV Bus Voltage

Fig. 8. Magnitudes during the LV start-up

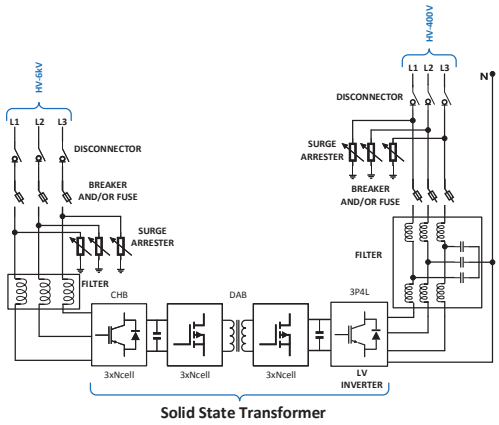


Fig. 9. SST protection system approach

zero in the case of a pure short-circuit. Protections against overcurrents can be implemented at different levels.

At the hardware level the drivers can protect the SST from overcurrents. At the software level, the control can handle these anomalies. In addition the inductance in the HV and LV side play a key role since they define the maximum value of the short-circuit current. The overcurrent handle by the control will be assessed in future work.

B. Overvoltages

Overvoltages that could damage the power devices or other elements of the SST can be produced either internally by the commutations of the power devices due to parasitic elements, or externally due e.g. to lighting. Typically the power devices are overrated by a factor of 100% with respect to their nominal operating voltage in the converter to protect against overvoltages due to commutation. While this increases to a certain level robustness against external overvoltages, this is not enough to protect the power devices and other elements against lighting. Additional protection using e.g surge arresters (Fig 9) is therefore compulsory. The effectiveness of the arresters will lead to a good study of the permanent and temporary voltages [7] in the grid, the neutral earthing system and the location of the arresters [8].

VI. Auxiliary Power Supply

Voltage supply for the auxiliary circuits of the SST, e.g. including drivers, sensors optical fiber fiber optics is a complex task.First of all the galvanic isolation between the HV and LV side has to be considered. Another issue is the high voltage conversion grade from tens of kV to $48V$ or $24V$

Auxiliary circuits can be fed from the DC cells by means of a DC/DC converters. This is relatively simple when the cell voltage is below $1000V$ since there are many commercial voltage sources in that range. On the other hand, low-power voltage sources with an input voltage $> 1000V$ are difficult to find, ad-hoc designs can be needed.In that case Input Series Output Parallel (ISOP) Flybacks [9] would be a good option.

VII. Conclusion

SST provides significantly improved functionalities compared to the LFT. Nevertheless, start-up, protections and control of imbalances require a careful study. The start-up procedure in the HV and the LV side has been covered in this paper. The passive elements energization requires an extra circuit which limits the peak current during the start-up. In the case of low current and high voltage is not trivial to find adequate components for an unique 3 phase charging circuit so individual distributed charging circuit per cell is the most suitable solution. On the other hand, in the LV side a 3 phase charging circuit in the SST port is easy to implemented due to availability of components in a wide range of currents.

Regarding protections, the SST is able to handle overcurrents by hardware (drivers and filter) and by software (control strategies). Although SST power devices are voltage overrated, this is not enough to withstand overvoltage phenomena such as lighting. Hence external protection devices are needed e.g surge arresters.

The SST presented in this paper is able to handle imbalances in the LV port. The control applied ensures a LV side supply with constant voltage and frequency, being the current unbalanced.The effect of imbalances in the HV side depends on the control and the passive components size.

The fourth wire increases the potential application of the SST because it allows single phase systems connection to its LV port.

Future works will be focused on a more detailed of imbalance handle study as well as the control overcurrents capabilities of the SST.

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Design and construction of a DAB using SiC MOSFETs with an isolation of 24 kV for PET applications

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Acknowledgements

This work was supported by the European Commission FP7 Large Project under grant UE-14-SPEED-604057 and by the Spanish Government under projects DPI2014-56358-JIN and the grant FPI BES-2014-070785.

Keywords

«Silicon Carbide (SiC)», «ZVS converters», «High Frequency Transformer (HFT)», « High voltage power converters», «Power electronic transformer (PET)», «Multilevel converters», «Dual Active Bridge».

Abstract

This paper analyzes the design and construction of a SiC-based Dual Active Bridge (DAB) converter for its use in a three-stage Power Electronic Transformer (PET) based on a Modular Multilevel Converter (MMC). The galvanic isolation between primary and secondary of the PET provided by the DAB High Frequency Transformer (HFT) is 24 kV. Challenges for the HFT design are discussed. A 5 kW DAB prototype using commercial 1.2–kV SiC MOSFETs is built to confirm the correctness of the design process. Parallelization of the DAB HFT to increase the power being transferred is also discussed.

Introduction

Line-Frequency Transformers (LFTs) are a mature technology. They are relatively cheap and robust, but fail to cope up with the modern grid demands. Solid State Transformers (SST), also called Power Electronic Transformers (PETs), were introduced in 1970 [1], and are considered an alternative to LFT to interface different voltage levels in the grid [2]. PET is an energy conversion system based on controllable fast-switching semiconductor devices which enables a significant reduction in volume and weight as well as fulfilling the controllability and power quality needs of emerging distributed generation grids [2], [3].

PET can be classified according to the number of stages, designs of one, two, or three stages have been proposed [4]–[7], the three-stage approach (AC/DC, DC/DC and DC/AC) appears to be the most popular choice [2], [8]–[10]. The use of Modular Multilevel Converters (MMC) at the front end (i.e. first stage AC/DC converter) is possible in this approach providing multiport capability [10]–[13].

In many applications, PET can require high isolation between its primary and secondary sides. This isolation is provided by the intermediate DC/DC stage. A Dual Active Bridge (DAB) DC/DC converter is commonly used for this role as proposed by many recent works [14]–[16]. However, in most of the works, the required isolation is not a major issue in the design mainly due to the application of interest. In this work, the selected PET topology is a modular three-stage topology based on an MMC. The HV-AC grid has a phase-to-phase voltage of 24 kV, which is the isolation required for the HFT.

A DAB converter designed to act as the intermediate DC/DC stage of a PET, and providing 24 kV of isolation through its High frequency transformer (HFT), is presented in this paper. The input and output voltages of the DAB are 800 V. SiC MOSFETs are used to comply with the high voltage and high switching frequency requirements.

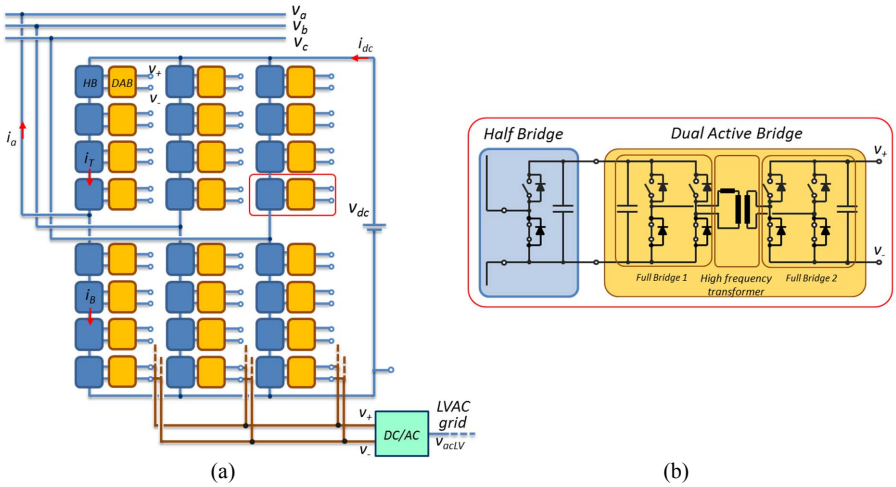
The paper is organized as follows. Section II describes the selected PET topology. The SiC-based DAB converter for PET is discussed in Section III. The HFT design is presented in Section IV. Section V discuss the selection of the 1.2 kV SiC power devices. Experimental results are provided in Section VI.

PET topology description

The selected PET topology is a three-stage multiport configuration based on an MMC [12], [13], [17]–[19]. Fig. *1*-a shows a schematic of the PET topology. The MMC acts as the front end AC/DC converter providing a high-voltage AC (HVAC) and a high-voltage DC (HV-DC) links. Each MMC cell (blue) integrates a bidirectional DAB DC/DC converter (orange) to inject or drag power from the MMC cell and to provide the isolation between the primary and the secondary (see Fig. *1*-b). The outputs of all DABs are connected in parallel to provide a low-voltage (LV), high-current DC link, which is connected to the controlled rectifier (green) providing the LV-AC link.

Consequently, the considered MMC-based PET configuration provides three ports: LV-AC, HV-AC and HV-DC. The additional HV-DC port introduced by the MMC-based topology enables new functionalities compared to topologies providing only LV-AC and HV-AC ports [13].

It should be noted that the required galvanic isolation between both AC grids is provided by each DAB transformer and is not alleviated by modular design, i.e. each transformer must withstand the total peak voltage between primary and secondary. Therefore, in this specific PET topology, modularity is not an advantage from the point of view of the HFT isolation requirements as discussed previously in [18].



(a) (b)

Fig. 1: (a) Three-stage MMC-based PET topology. (b) Structure of one cell composed of the MMC half bridge (blue) and the DAB (orange).

Dual Active Bridge (DAB)

The DAB (see Fig. 2) is a symmetric, bidirectional DC/DC converter based on two active full bridges interfaced through an HFT. This makes it a suitable candidate for the intermediate stage of the PET, as it provides galvanic isolation through its HFT as well as realizing a bidirectional power transmission between the MMC cells and the LV side of the PET [13], [20], [21].

Both bridges are controlled with a constant duty cycle to produce a high frequency square-wave voltage at the HFT terminals. By controlling the phase shift between these square-wave voltages, a voltage difference is applied on the HFT series leakage inductance, and power is transferred from the leading bridge to the lagging one [22].

The output power delivered by the DAB P_O can be expressed by (1), where T is half of the switching period, d is the phase shift as a ratio of half a period, L_{lk} is the leakage inductance, v_O is the output voltage, v_i is the input voltage, i_O is the output current and n is the HFT turns ratio.

$$P_O = i_O \cdot v_O = \frac{(1-d)\cdot d \cdot T \cdot v_O \cdot v_i}{n \cdot L_{lk}} \quad (1)$$

This converter can have a relatively high efficiency as zero-voltage switching (ZVS) of all the devices at nominal conditions can be achieved [23].

The specifications for the DAB converter are shown in Table I. A switching frequency of 30 kHz is selected based on the tradeoff between leakage inductance value and power transfer (see (1)).

Table I: Specifications for the DAB

Parameter	Value
Rated power	5 kW
Isolation	24 kV
Switching frequency	30 kHz
RMS current	8.4 A
Input voltage	800 V
Transformer turns ratio	1 : 1
Series leakage inductance	485 uH
Transformer maximum temperature rise	60 ºC

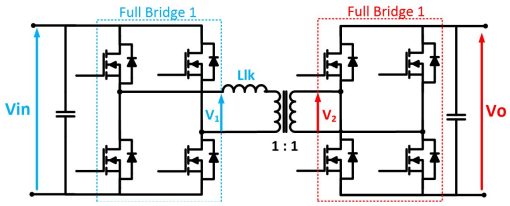


Fig. 2: Dual-Active-Bridge (DAB) converter.

High Frequency Transformer (HFT)

Targets and constraints

The HFT is one of the key components in a PET. First, it enables scaling the MMC cells voltages and the DC/AC power converter in the LV side of the PET by adequate selection of its turns ratio. It also provides galvanic isolation between the HV and LV ports of the PET, in this case 24 kV, which is considered the main challenge of this HFT design [24], [25] compared to other designs considered in the literature [26]–[28]. This high isolation implicates fixing certain design parameters related with the geometry of the transformer and consequently constraining the value of the leakage inductance as well as the temperature rise as explained in the next section.

The targets of the HFT design are shown in Table I. From (1) and the specifications shown in Table I, the required value of leakage inductance is 485 µH.

In a DAB, the leakage inductance determines the power transfer for a given switching frequency and phase shift (see (1)). Therefore, it is important to achieve an accurate value for the leakage inductance to enable working at nominal power with the nominal phase shift, thus ensuring ZVS [21]–[23]. In order to increase the power density and to reduce cost, it is advisable to magnetically integrate this series inductance as the leakage inductance of the HFT. Making use of the HFT leakage flux also makes the DAB series inductance value independent of the core and therefore independent of the core temperature

variation. However, this imposes a constraint on the design as the value of the DAB inductance will be completely dependent on the other design parameters [25].

A tradeoff must be therefore achieved between the optimization of size and losses (i.e. temperature rise) while achieving the required leakage inductance and isolation.

Design and construction

The whole HFT design is an iterative process in which isolation, temperature rise and leakage inductance requirements have to be simultaneously achieved. The process combines the use of analytical models intended to evaluate losses with Finite Element Analysis (FEA), which are used to estimate the resulting leakage inductance, temperature rise and the required isolation distances in a single magnetic component.

1. *Geometry comparative analysis:*

Three different winding structures for the HFT have been analyzed (Fig. 3): concentric, split and separate winding.

Concentric winding (see (a) in Fig. 3) can provide very low leakage inductances [26], but it is not always advantageous in a DAB application where the leakage value must be accurately selected for a certain operating point. An excessively low leakage inductance might require the use of an external inductor whose size may be comparable to the HFT, with the subsequent increase in the cost, weight and volume of the system [26]–[29]. Moreover, concentric windings configuration may compromise the maximum achievable galvanic isolation, due to the proximity of both windings. Although the required isolation may be reached, the resulting transformer design is difficult to build and not desirable therefore for industrial applications [29]. Due to this, concentric windings are disregarded.

Split windings (see (b) in Fig. 3) can achieve the required value of the leakage inductance. However, similar to the concentric design, this winding configuration compromises the maximum isolation.

Separate windings provide the required isolation but its main problem is the minimum achievable leakage inductance, as the leakage flux increases with the increase of the volume between windings. However, in this particular case, separate winding allows to integrate the required series inductance into the HFT [29]. Due to this, a configuration with separate windings was chosen finally.

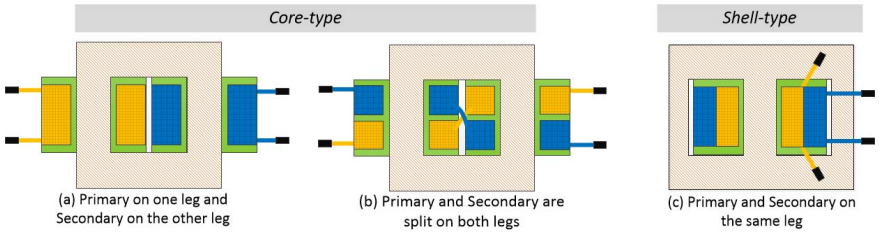


Fig. 3: The studied HFT winding structures.

2. *Core structure:*

A frequently used structure in literature is the UU core [25], [30]. The HFT is developed using two stacked UU-cores (UU100/57/25). The primary and the secondary windings are placed on separate legs of the UU-core. Ferrite material is used for the core based on the selected switching frequency (30 kHz) [26].

Both isolation between windings and between core and windings is considered. A minimum clearance distance is required between primary and secondary windings as well as between each winding and the core. These distances can be significantly decreased by encapsulating the HFT using a resin material of high dielectric strength. They are calculated based on the dielectric properties (kV/mm) of the bobbins

material (GPO3) and the encapsulation material with a safety factor of 70%. Although encapsulation is advantageous to decrease the HFT size while complying with the required isolation, it compromises the HFT core and copper temperature rise. ROYAPOX 912 THC/2 epoxy resin material was selected as it provides sufficient isolation (15 kV/mm) and good thermal conductivity (3 W/mK).

Fig. 4 shows a schematic representation of the HFT design from ANSYS PEmag®. Fig. 5-a shows the non-encapsulated laboratory developed HFT for test purposes. Fig. 5-b shows the final encapsulated HFT prototype. Isolation tests are performed using a 30 kV high potential (hipot) tester between both windings. Fig. 6 shows the experimentally measured leakage current flowing between primary and secondary windings through the air/resin versus the voltage difference between them during the isolation test for encapsulated and non-encapsulated transformers (see Fig. 5-(a) and (b)). Obviously, the encapsulated prototype shows lower leakage current between both windings, which is advantageous for high *dv/dt* to avoid very large instantaneous leakage currents leading to partial discharge and eventual isolation breakdown.

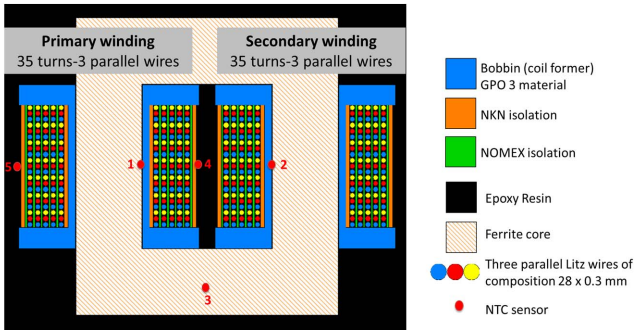
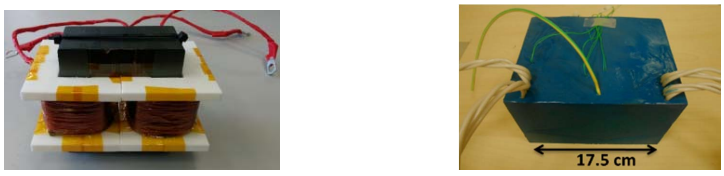


Fig. 4: HFT structure taken from ANSYS PEmag®.



(a) (b)

Fig. 5: (a) Non-encapsulated HFT laboratory prototype using two 3-D printed bobbins with 35 turns on each (b) Factory encapsulated HFT. Both designed for a rated power of 5 kW @ 30 kHz with separate windings.

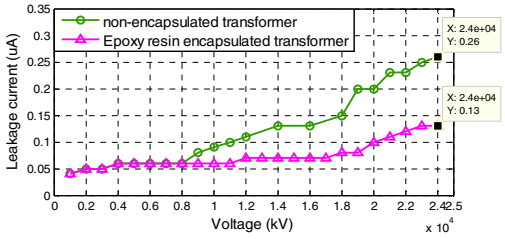


Fig. 6: Experimental results. Isolation test showing lower leakage current for the encapsulated HFT.

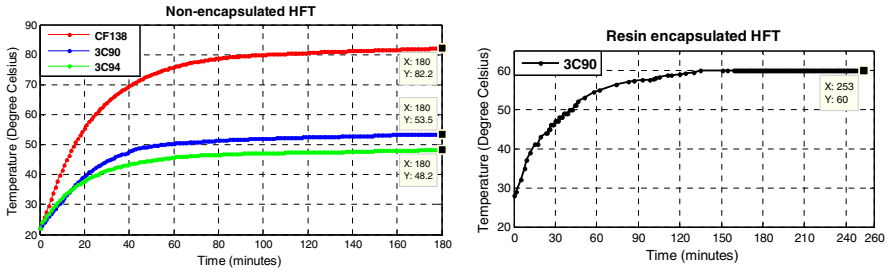
3. Temperature rise

Losses in core and copper are translated into heat, raising the temperature of the transformer, and therefore it is important to maintain this rise within acceptable limits.

Temperature rise is roughly estimated using (2) [31], where P is the sum of the winding losses and the core losses, h is the coefficient of heat transfer, A_t is the surface area and ΔT is the temperature rise. The estimated temperature rise is 40 ºC.

$$P = hA_t\Delta T \quad (2)$$

Core losses and consequently the core temperature rise strongly depends on the core material used. Three ferrite materials were tested, CF138, 3C94 and 3C90. Lab prototype is shown in Fig. 5-a. Forced air cooling is used and the temperature is measured using an NTC attached to the bare core at the hottest point, being previously identified (NTC (1) in Fig. 4). Fig. 7-a shows the temperature rise for the three materials during 3 hours of the converter operation at rated power (5 kW), 3C94 material providing the best results due to its lowest specific power loss (kW/m^3).



(a) (b)

Fig. 7: Experimental results. Hottest point temperature rise vs. time for (a) non-encapsulated HFT using three different ferrite materials and (b) encapsulated HFT using 3C90, both transferring 5 kW.

3C90 ferrite from Ferroxcube® was used to produce an encapsulated prototype. To confirm the correctness of the design, five NTC sensors are placed at different locations of the encapsulated HFT prototype to monitor its temperature (see Fig. 4). Fig. 7-b shows the temperature rise vs. time of the HFT hottest point during 4 hours of continuous operation of the DAB at 5 kW. The temperature rise is approximately 40 ºC with an ambient temperature of 20 ºC. This meets the target temperature (see Table II). This gives a margin of approximately 20 ºC to allow for additional temperature rise due to the closed cabinet structure.

In order to maintain the copper temperature rise within reasonable limits, the windings cable diameter and composition were calculated based on copper losses, skin effect and available window area [25]. The windings are build using three parallel litz wire of composition (28/0.5 mm) as illustrated in Fig. 4.

4. Leakage inductance

The leakage flux is mainly governed by two parameters: the volume between the windings and the number of turns. Both, higher volume and higher number of turns lead to larger leakage flux.

On one hand, the volume between both windings is constrained by the minimum isolation distances. In a separate winding transformer, this volume is difficult to calculate as it is not confined to the window volume like in the case of concentric windings and therefore it is difficult to analytically obtain a precise value for the leakage inductance.

On the other hand, the number of turns is fixed by the core and copper losses. For a fixed core structure, a theoretical optimum number of turns can be obtained which results in a minimum core and copper losses and therefore a minimum temperature rise [32].

Therefore, in this HFT design, a tradeoff is achieved between the number of turns (i.e. losses) and the value of the leakage inductance while fixing the isolation distances to the minimum required value. It is obtained using ANSYS PEmag® FEA simulations then validated by experimental measurements. The

required value of leakage inductance of 485 µH is achieved using 35 turns. The measured value from the final prototype is 435 µH.

SiC devices for the DAB

Effect of using SiC devices on the DAB

To comply with the target voltage and switching frequency (i.e. 800 V and 30 kHz), SiC MOSFETs are selected [33], [34]. Use of larger cell voltages is advantageous for the HFT design. Increasing the cell voltage for a given rated power, the required leakage inductance increases (see (1)), alleviating the problems due to long isolation distances and separate windings. It must be noted however that larger cell voltage might imply practical problems on the Auxiliary Power Supply (APS) providing the low-voltage (i.e. 24/15/12V) needed to feed the control circuitry of each cell [35].

Selection of SiC MOSFETs

Based on the DC-link voltage value (see Table I) and switching frequency, 1.2 kV SiC MOSFETs are selected. Several commercially available MOSFETs were tested in a 2-kW 400-800 V boost converter, for switching frequencies of 30, 50 and 100 kHz. The efficiency of the whole boost converter (consisting of two SiC MOSFETs) using these devices is compared.

Table II shows the results for five different options; one SiC power module as well as four different discrete N-channel SiC power MOSFET devices. It is observed from Table II that all the devices show a high efficiency. The largest dispersion occurs at 50 kHz, but is as small as 0.6 %.

Table II: SiC MOSFET Comparative Analysis

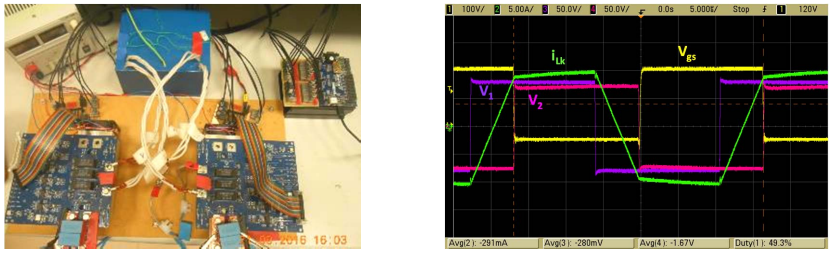
Device	Rated current (A) @100 ˚C	Rds (mΩ) @100ºC	Cout (pF)	Measured efficiency (%)		
				30 kHz	50 kHz	100 kHz
ST (SCT30N120)	34	80	130	97.77	98.16	97.81
ROHM (SCH2080KE + SBD)	28	80	175	97.71	98.02	97.69
ROHM (SCT2080KE)	28	80	77	97.82	98.17	97.93
CREE (C2M0040120D)	40	40	150	97.76	98.10	97.84
CREE module (CCS050M12CM2+ SBD)	59	25	400	97.49	97.54	97.50

Experimental results

Two devices were selected for the construction of the DAB: CREE (CCS050M12CM2) power module and ROHM (SCH2080KE) discrete power MOSFET. Two 5 kW DAB prototypes were constructed using these devices (Fig. 8-a) and efficiency is compared at rated power of the converter (i.e. 5 kW).

Commercial CREE drivers (CGD15FB45P1) were used with CREE modules CCS050M12CM2. The control signals are generated using a FPGA. Due to the high isolation requirements, the control board is divided into two sections with enough clearance to provide the 24 kV isolation. Fig. 8-b shows the measured waveforms when the DAB transfers 5 kW (see Fig. 2). The calculated efficiency of the converter from the input and output average voltages and currents is 98.5 %.

A second prototype was developed using the ROHM (SCH2080KE) discrete power MOSFET. In this case, CREE 2-channel drivers (CGD15HB62P1) are used. The efficiency of the converter is 98.1 %. The slight decrease in efficiency is attributed to the higher on-resistance of the ROHM discrete device as its rated current is relatively lower compared to the CREE module (see Table II).



(a) (b)

Fig. 8: (a) 5 kW DAB prototype using CCS050M12CM2 modules. (b) Experimental results. 5 kW DAB prototype waveforms. Voltage on both sides of the HFT (V_1 and V_2) and leakage inductance current (i_{LK}).

A mean to increase the power transfer while maintaining the isolation is parallelization of HFTs. To analyze this issue a DAB prototype was built with two identical HFTs connected in parallel. CREE modules CCS050M12CM2 were used. The resulting leakage inductance is 221 µH, the maximum power transferred being doubled. Fig. 9 shows the measured efficiencies for both cases: a DAB using a single HFT with a maximum power 5.7 kW and a DAB using two parallel HFTs with a maximum power of 11 kW. For both cases, the switching frequency is kept constant (30 kHz). The minimum power is limited by the DAB ZVS range while the maximum power is limited by the leakage inductance of the HFT [23]. It is observed, from Fig. 9 that increasing the power has a modest effect on the converter efficiency.

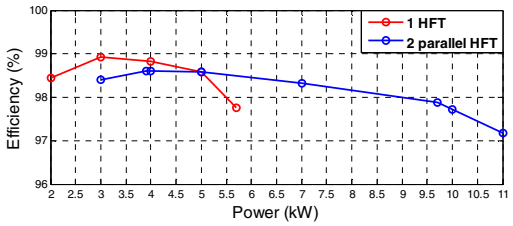


Fig. 9: Experimental results. Efficiency of the SiC DAB converter vs. transferred power at 30 kHz for two cases; (a) one HFT per DAB and (b) two HFTs in parallel per DAB.

Efficiency versus switching frequency

DAB efficiency vs. switching frequency was analyzed both analytically and experimentally. Two cases are considered: a DAB with a single HFT and with two parallel HFTs, however results are shown only for the case of two HFTs because conclusions were the same in both cases. In the case of two parallel HFTs the maximum transferable power at 80 kHz is 4 kW. It is observed from Table III that the efficiency decrease is < 0.5 % when the switching frequency increases by a factor of approximately 2.6.

Table III: SiC-based DAB converter efficiency with different switching frequencies

Switching frequency	DAB efficiency (two HFT transferring 4 kW) (%)	
	Analytical	Experimental
30 kHz	99.00	98.60
50 kHz	98.82	98.62
70 kHz	98.64	98.41
80 kHz	98.54	98.19

An estimation of the losses breakdown in the DAB between conduction, switching and HFT losses estimated analytically is shown in Fig. 10. From Table III and Fig. 10, it is observed that increasing the switching frequency by a factor of approximately 2.6 produces an increase of the switching losses of less than 15 W for a rated power of 4 kW (< 0.5%).

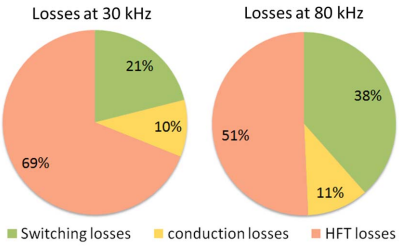


Fig. 10: Analytically estimated switching, conduction and HFT losses in the DAB at 30 and 80 kHz.

Conclusion

Design of a SiC-based DAB for a PET application has been addressed in this work. The required isolation is 24 kV which is provided by the HFT. Challenges imposed by the application on the HFT design have been discussed. These concern mainly leakage inductance, temperature rise and isolation. A 5 kW HFT, intended for a switching frequency of 30 kHz, has been built. Experimental results are shown for a DAB prototype using two different 1.2 kV SiC power devices, efficiencies as high as 98% are achieved. The measured temperature rise at the hottest point of the HFT is 40 ˚C.

Parallelization of HFTs has been proposed as a mean to increase the cell power transfer capability while complying with the high isolation requirements. This case has also been confirmed experimentally with a flat converter efficiency curve showing a slight decrease of less than 1 %. The effect of varying the switching frequency on the efficiency of the converter is analyzed. Both analytical and experimental results show a reduction of less than 0.5 % when almost tripling the switching frequency.

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