Novel Selection Criteria of Primary Side Transistors for LLC Resonant Converters

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***Abstract*— An insightful evaluation of commercial high-voltage power MOSFETs for soft-switching converters is reported in this paper with special emphasis on elucidating power loss contributions and electrical parameter requirements. Experimental tests have been carried out to evaluate different Silicon Super-Junction technologies used in the primary side of a 600 W half-bridge LLC resonant converter operating in inductive mode. Unexpectedly, none of the existing figures of merit, inferred from datasheets, can predict the performance ranking due to the additional soft-switching losses (E_{SW_SOFT}). Subsequently, a new characterization test based on a pulsed I-V system is suggested and proved to quantify E_{SW_SOFT}.**

Keywords*— *LLC, figure of merit, soft-switching, super-junction MOSFET

I. INTRODUCTION

Resonant circuits have a long history in power conversion [1]. However, it was not until last decade that the market adoption of LLC converters (Figure 1) was massive in the segments of adapters, flat panel TV, datacenters, Electric and Hybrid Vehicle (EV/HEV) and Photovoltaic (PV) inverters among others [2], [3]. Many of these applications must meet the highest efficiency standard, such as, 80PLUS® Titanium [4]. Consequently, the efficiency of the selected converter topology must be very high and the selection of a resonant topology achieving Zero Voltage Switching (ZVS) can provide a reduction of losses and volume. Nowadays, the proper selection of high-voltage (~600 V) Super Junction MOSFETs (SJ-MOSFETs) used in the LLC primary side is crucial to obtain an optimum system design with a small footprint, low cost and high efficiency [5].

This work aims to review the methodology followed to select SJ-MOSFETs by deeply investigating their different power losses contributions. This means interpreting all the power loss contributions and which are the electrical parameters that have direct impact in them. Besides, new characterization techniques and Figures of Merit (FoMs), that will help the designer during the selection of the devices for the application, are proposed.

This paper is organized as follows. Section II explains the criterion to select the SJ-MOSFETs under comparison. Moreover, a detailed insight on the power losses contributions of the SJ-MOSFETs is carried out (losses models are developed) in order to compare them with the obtained experimental results. In Section III a new electrical characterization is proposed and a new FoM which takes into account soft-switching losses is proposed. Finally, conclusions are drawn in Section IV.

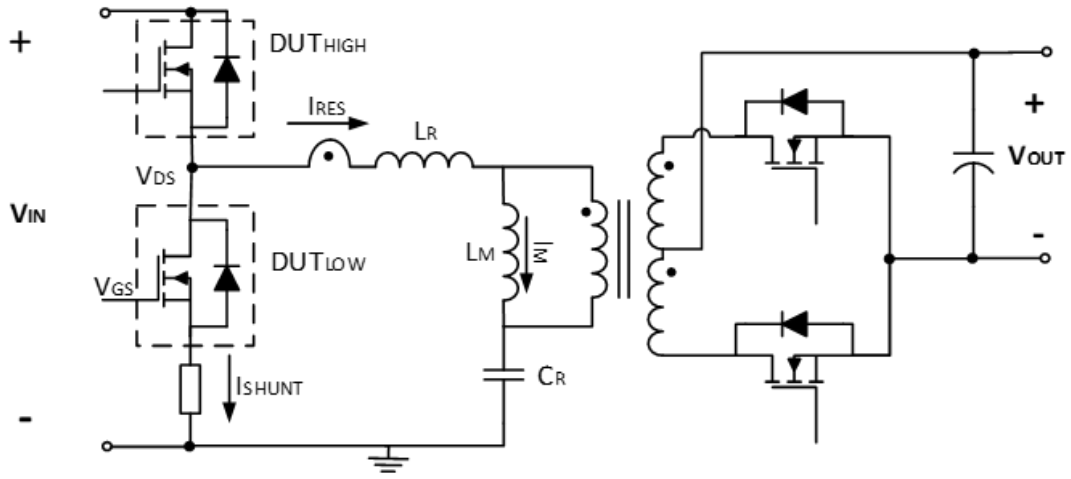


Figure 1 Simplified circuit scheme for LLC resonant converter and sensing method

Table 1 List of SJ-MOSFETs explicitly for LLC primary side with main electrical characteristics and FoMs. All devices are packaged in TO-220 except DUT4 in TO-220FP

DUT (SJ_MOSFET)	R_{ON} (mΩ)	BV_{DSS} (V)	V_{TH} (V)	R_G (Ω)	Q_G (nC)	Q_{GD} (nC)	Q_{GS} (nC)	E_{OSS} (µJ)	Q_{OSS} (nC)	R_{ON}*Q_G (Ω*nC)	R_{ON}*Q_{GD} (Ω*nC)	R_{ON}*E_{OSS} (Ω*µJ)	R_{ON}*Q_{OSS} (Ω*nC)
1	155	600	3.5	0.9	24	8	5	2.7	140	3.7	1.2	0.4	21.7
2	168	650	4	0.6	60	25	12	6.4	121	10.1	4.2	1.1	20.3
3	171	600	4	3.4	37	13	11	4.9	106	6.3	2.2	0.8	18.1
4	160	650	3.5	6	31	10	12	3.6	124	5.0	1.6	0.6	19.8
5	168	600	3	7	29	12	6	4.1	123.8	4.9	2.0	0.7	20.8
6	175	600	3	7	29	12	6	4.6	122.4	5.1	2.1	0.8	21.4

II. APPLICATION MEASUREMENTS AND BENCHMARKING

A group of SJ-MOSFETs (with similar values of conduction resistance, R_{ON}, and output charge, Q_{OSS}) from different manufacturers (Table 1) was tested in a commercial evaluation board featuring a 600 W/ 200 kHz half-bridge LLC resonant converter with input voltages (V_{IN}) between 350-410 V_{DC} and a fixed output voltage (V_{OUT}) of 12 V_{DC}. [6]. All the SJ-MOSFETs under examination are recommended for LLC resonant converters by the major vendors. The basic requirements of the SJ-MOSFETs related to a fixed resonant tank (L_M, L_R, C_R) and deadtime (t_{dead}) are fulfilled by all transistors in order to ensure ZVS inductive mode test during the entire load range.

A minimum deadtime between the turn-off of one primary-side SJ-MOSFET and the turn-on of the other one must be assured to avoid short-circuits (time domain analysis (1), (2)).

$$t_{d,min} = \frac{t_{lin}}{2} + \frac{2 \cdot Q_{oss}}{I_{M\,pk}} \quad (1)$$

$$t_{lin} = f\left(R_G, V_{GS\,th}, \frac{C_{DS}}{C_{GD}}\right) \quad (2)$$

$t_{d,min}$ is the minimum deadtime needed, proportional to t_{lin} (the linear time of operation of the SJ-MOSFETs), Q_{OSS} (output charge of the SJ-MOSFETs) and I_{Mpk} (peak magnetizing current of the transformer). t_{lin} is function of R_G (gate resistance), V_{GSth} (gate threshold voltage), C_{DS} (drain-to-source capacitance) and C_{GD} (gate-to-drain capacitance).

Moreover, the energy in the resonant tank must be enough to discharge the output capacitance of the SJ-MOSFET (energy domain analysis (3)).

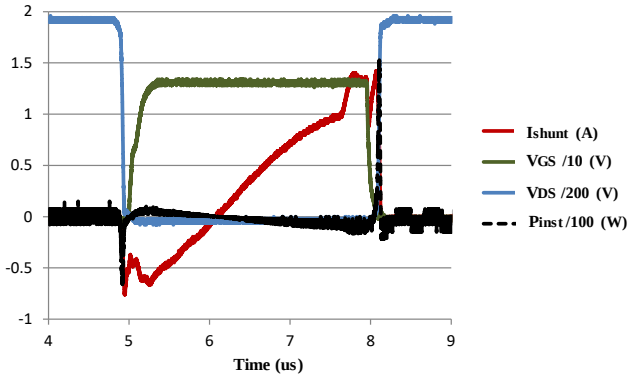
$$\left.\begin{aligned} E_{res,min} &= \frac{1}{2}(L_M + L_R) I_{M\,min}^2 \\ E_{cap,max} &= \frac{1}{2}(2C_{OSS}) V_{DS\,max}^2 \end{aligned}\right\} E_{res,min} > E_{cap,max} \quad (3)$$

$E_{res,min}$ is the minimum energy required in the resonant tank, which is proportional to L_M (magnetizing inductance of the transformer), L_R (leakage inductance of the transformer) and $I_{M\,min}$ (minimum magnetizing current of the transformer). The maximum energy that the SJ-MOSFET must store ($E_{cap,max}$) depends on C_{OSS} (its output capacitance) and $V_{DS\,max}$ (the maximum drain-to-source voltage in the switching node).

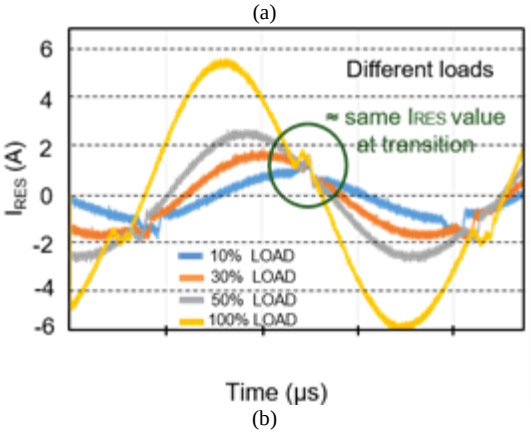
It is not necessary to design a different L_M for each SJ-MOSFET in order to optimize the performance since the devices that have been selected share the same R_{ON} and Q_{OSS} values, and ZVS is guaranteed for all the power range.

Examples of experimental waveforms measured in the converter are shown (I_{SHUNT}, V_{GS}, V_{DS} and estimated P_{ins} in Figure 2a and I_{RES} in Figure 2b) for different load levels. It is worth to remark that even if ZVS is achieved ($t_{d,min}$ is assured and there is no ringing in the measurements) some power losses appear during the switching (see P_{ins} in Figure 2a). Moreover, the I_{RES} value during the transition is nearly the same regardless of the load level, which will be helpful in order to estimate the switching losses.

An efficiency comparison is performed in the full load range with the same test protocol and operating conditions (V_{IN}=380V, V_{OUT}=12V). In Figure 3a, differential efficiencies for loads going from 20% to 100% of full load are presented). DUT1 is considered as the reference, since it shows the best performance in the whole range. The dispersion error is estimated considering the information given by the LLC evaluation board manufacturer and the lab equipment utilized.



(a)



(b)

Figure 2 (a) Measured waveforms: I_{SHUNT} (A) in red, $V_{GS}/10$ (V) in green, $V_{DS}/200$ (V) in blue and calculated $P_{inst}/100$ (W) in black. (b) Experimental I_{RES} measured at different loads.

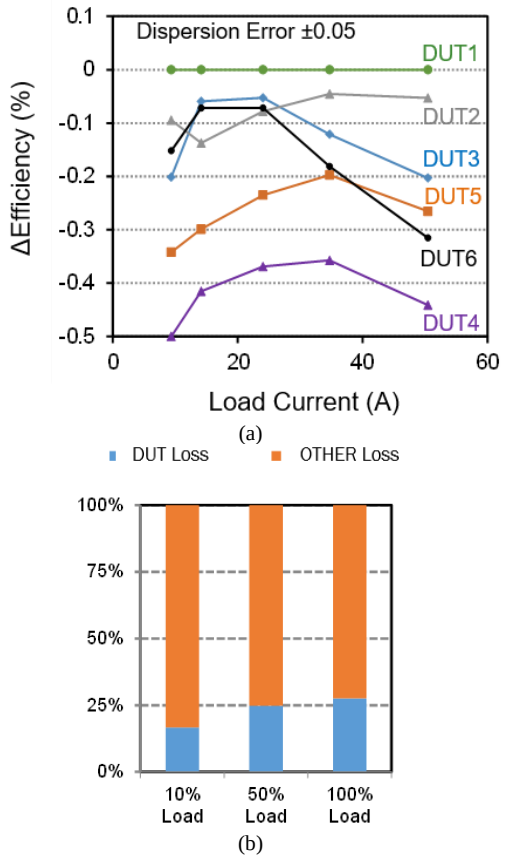


Figure 3 (a)Measured variation of efficiency with respect to the best SJ-MOSFET. (b) Measured system power loss contribution from the two primary-side transistors (DUT3)

Figure 3b shows that primary-side SJ-MOSFETs dissipate 20-30% of the system total loss based on the experimental measurements obtained, while the other 70-80% of the losses are spread out among the magnetics, layout, secondary-side devices, digital circuitry, etc. This makes imperative a proper selection of the primary-side devices.

The extraction of experimental I_{SHUNT}, V_{DS}, V_{GS} and I_G waveforms (Figure 1) allows to estimate contributions from switching (P_{SW}), driving (P_{DR}) and conduction (P_{ON}) power losses of those primary-side SJ-MOSFETs (Figure 4) under different power load requirements (60W, 300W and 600W Figure 4a,b,c, respectively).

Even performing ZVS, P_{SW} losses are relevant and differences in the power losses between transistors are due to P_{SW}+P_{DR} at light loads (Figure 4a) and to P_{SW}+P_{ON} at heavy loads (Figure 4c). Traditional selective procedures for power devices, based on only one FoM, for example, the conduction resistance (R_{ON}) are not sufficient since they cannot explain differences among efficiencies for low and medium loads (Figure 3a).

In Figure 4a, at low load, whereas low P_{ON} losses remain almost equal for all the DUTs, differences in P_{DR} losses have small impact and P_{SW} losses are dominant.

Besides, at medium load (Figure 4b), divergence in this parameter (P_{SW}) among devices make the difference (P_{ON} losses are the highest but fairly the same value, but differences at P_{SW} have a great impact in the losses contribution). However, it is known that P_{SW} does not depend only on one electrical parameter (E_{oss}, Q_{oss}, etc… in Table 1) and, therefore, new FoMs are mandatory in order to evaluate divergence of power losses.

For heavy loads (Figure 4c), P_{ON} is by far the main factor of losses in the SJ-MOSFETs, yet disparity among the P_{SW} losses are discernible.

Therefore, depending on the application and the range of power that will be demanded a suitable selection criterion based on more complex FoMs is needed.

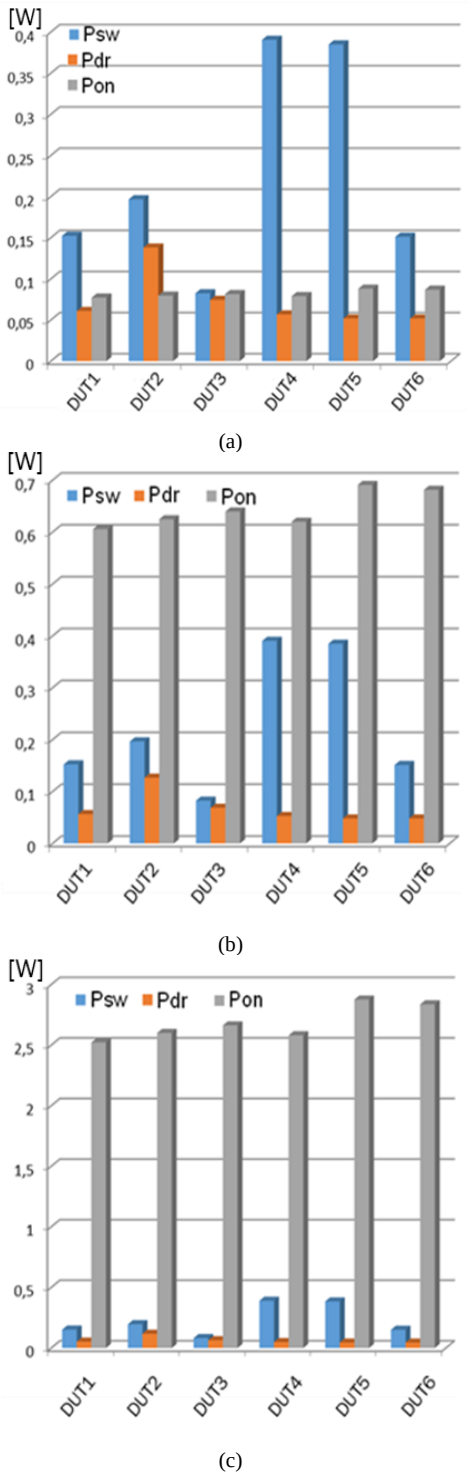


Figure 4 Measured power loss due to driving (P_{DR}), switching (P_{SW}) and conduction (P_{ON}) at (a) 10%, (b) 50% and (c) 100% load per primary-side SJ-MOSFET

All power losses contributions have been measured experimentally and some losses models have been developed. P_{SW} losses are calculated by means of the energy dissipated during turn-on and turn-off transitions (4). It is almost constant for different load levels, since there is little dispersion in I_{RES} (Figure 1) value during transitions (Figure 2b).

$$E_{SW} = E_{ON} + E_{OFF} = \int_{<turn\ on>} I_{SHUNT} \cdot V_{DS} \cdot dt + \int_{<turn\ off>} I_{SHUNT} \cdot V_{DS} \cdot dt \quad (4)$$

Little dispersion (< 5%) between P_{ON} experimental and theoretical values is achieved (Figure 5a), based on R_{ON} and I_{SHUNT} waveforms, guaranteeing a fitting model of losses.

However, there are many factors to consider when calculating P_{DR} (11) [7] (Figure 5b,c), such as: $P_{d1}(5), P_{d2}(6), P_{d3}(7), P_{d4}(8)$ (losses due to the commercial driver IC itself, commonly disregarded), driving-on (9) and driving-off losses (10).

The factors that contribute to the total driving power dissipation are:

- The quiescent current (high side and low side) of the IC.

$$P_{d1} = I_{DDmax} \cdot V_{DDmax} \quad (5)$$

$$P_{d2} = I_{QBS} \cdot V_{BSmax} \quad (6)$$

where I_{DDmax} is the operating current for the maximum switching frequency of the application, V_{DDmax} the maximum supply voltage of the driver, I_{QBS} the quiescent current of the high side section and V_{BSmax} the maximum voltage at the bootstrap capacitor.

- The input sections that generate losses by means of their input structures (pull-down resistors, $R_{pull\text{-}down}$).

$$P_{d3} = \frac{V_{INdriver}^2}{R_{pull-down}} \quad (7)$$

- The leakage losses between the control to any high side section.

$$P_{d4} = I_{LVS} \cdot V_{IN} \quad (8)$$

where I_{LVS} is the leakage current and V_{IN} is the high side DC voltage.

- The output sections, driving-on (P_{on}) and driving-off (P_{off}) losses:

$$P_{On} = Q_G \cdot V_{DD} \cdot f_s \cdot \frac{R_{Gon}}{R_{Gon} + R_G + R_{Gint}} \quad (9)$$

$$P_{Off} = Q_G \cdot V_{DD} \cdot f_s \cdot \frac{R_{Goff}}{R_{Goff} + R_G + R_{Gint}} \quad (10)$$

where Q_G is the total gate charge of the power transistor, f_s the switching frequency and R_{Gon}, R_G, R_{Gint} and R_{Goff} are the gate and MOSFET resistances detailed in Figure 6.

All contributions can be estimated as the sum of the above-mentioned factors. The final power dissipation is:

$$P_{DR} = P_{d1} + P_{d2} + P_{d3} + P_{d4} \quad (11)$$

As an example of this driving power losses model, a comparison between theoretical and experimental driving-on losses calculation is shown (Figure 5c).

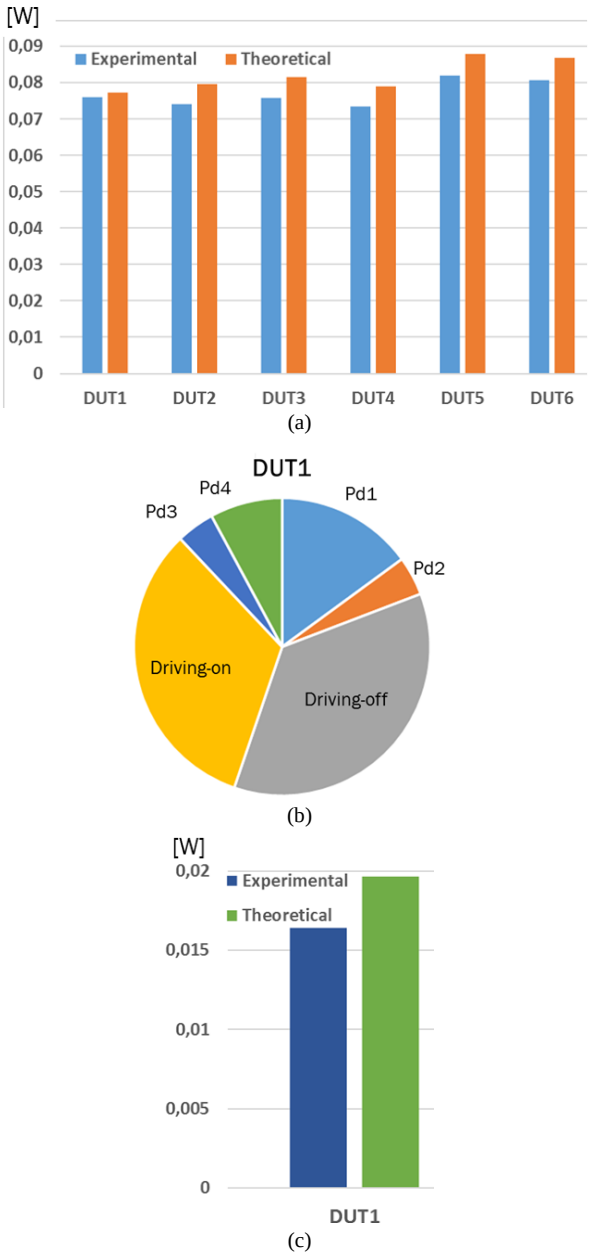


Figure 5 (a)Measured vs. Theoretical conduction losses (P_{ON}) at 10% load, (b) driving power losses (P_{DR}) breakdown for DUT1 at 10% load and (c) experimental vs. theoretical driving-on losses at 10% load

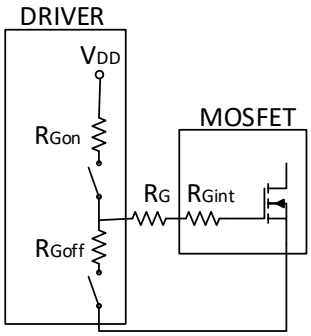


Figure 6 Driver and MOSFET gate resistors

III. NEW ELECTRICAL CHARACTERIZATION

As has been shown, P_{SW} losses are significant, especially at low and medium load, even if the converter is working with ZVS. It is important to predict and quantify those additional soft-switching losses, E_{SW_SOFT} [8].

The quantification of E_{SW_SOFT} for SJ-MOSFETs in LLC resonant converters has drastically changed during the last decade. Despite some initial works neglecting them [5], other investigations point out to an increasing E_{SW_SOFT} predominance in modern soft-switching converters [9]. Efforts have been done to include non-linear capacitance effects [10]-[11] and non-ZVS operation [12] in MOSFETs simulation models. However, the most recent discoveries in output capacitance (C_{OSS}) hysteresis for SJ-MOSFETs are not considered in those models [13]-[16].

A physical relationship between unexpected ZVS power loss and C_{OSS} hysteresis was introduced in [17] for SJ MOSFETs. The experimental observations published in [13] were qualitatively reproduced in [17], elucidating the existence of E_{SW_SOFT} during C_{OSS} charge and discharge.

The value of E_{SW_SOFT} varies from device to device in function of geometrical and technological features. Furthermore, no information on this effect is provided in datasheets, application notes or simulation models. In fact, C_{OSS} provided by device vendors is typically extracted by small-signal techniques when only large-signal analysis captures C_{OSS} hysteresis.

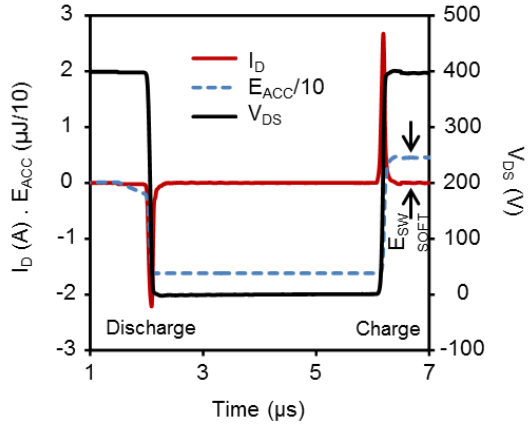
In order to obtain a new explicative FoM, an Auriga pulsed I-V system [18] is proposed for E_{SW_SOFT} characterization. Differently from other reported techniques [19]-[21], this is the first suggested commercial system. The characterization system that this hardware delivers is able to capture measurements with very high speed and resolution (up to 0.01% of max current), and it is temperature independent. Moreover, voltage/current measurements have emerged as the preferred method of getting different characteristics of active devices.

Figure 7a shows an example of some measurements done to extract E_{SW_SOFT} (by applying a 400 V pulse on the device with the period/frequency desired, and measuring I_D, V_{DS} and the cumulative energy -E_{ACC}- waveforms). Concretely, E_{SW_SOFT} is considered as the energy accumulated after applying a complete cycle of discharge-charge to the device.

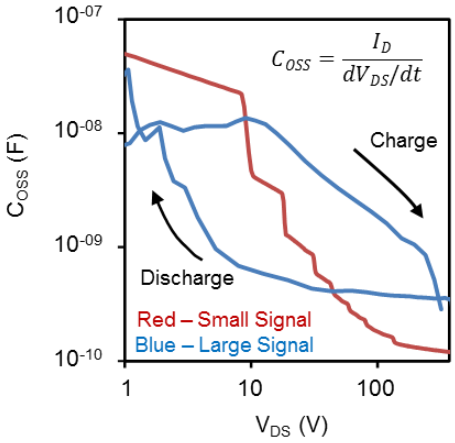
Based on the information extracted, the mechanism to detect C_{OSS}-hysteresis can be seen in Figure 7b (by dividing the current by the derivative of the voltage), noticeable and measurable during the charge and discharge of the SJ-MOSFETs. This effect is an inherent loss mechanism for SJ-MOSFETs due to their inner structure. Differently from the information usually provided by the manufacturer (Figure 7, small signal waveform, in red), this characterization shows dissimilarities between the charge and discharge of the devices (large signal, in blue) which states and validates an intrinsic energy loss.

By using this characterization method, Figure 7c compares the new FoM defined as R_{ON}*E_{SW_SOFT} for different technologies (GaN E-Mode devices, SiC MOSFETs and some of the DUTs characterized in this paper). This FoM which considers both R_{ON} (important for heavy loads) and E_{SW_SOFT} (crucial for low and medium loads) qualitatively matches with efficiencies (Figure 3a) and P_{SW} trends (Figure 4), since the experimental results show that DUT_1 presents better performance than DUT_5 or DUT_4, and it can be extended to the rest of devices under test.

It is worth to remark that other technologies (GaN, SiC) for the same range of voltage promise better performance according to the proposed FoM.



(a)



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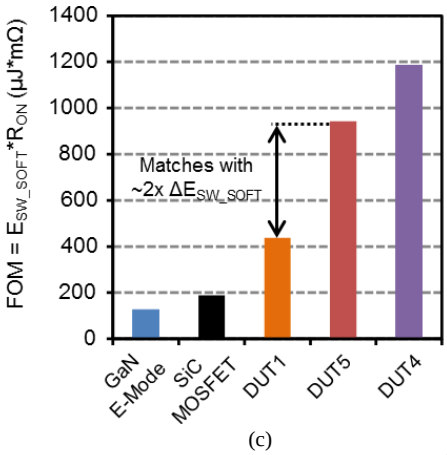

(c)

Figure 7 Auriga pulsed I-V tests: (a) I_D, V_{DS} and E_{ACC} waveforms, (b) C_{OSS} hysteresis, (c) R_{ON}*$E_{SW\text{-}SOFT}$ in SJ-MOSFETs, GaN E-Mode and SiC MOSFET

IV. Conclusions

This paper presents an original perspective of the requirements and trends in power transistors for LLC primary side converters by covering new insights in power loss analysis and application-oriented characterization techniques.

A deep power loss model, which takes into account PON, PDR and PSW contributions, is followed and compared with experimental results, showing a good match.

Up to now, existing FoMs are not enough to select the optimum power transistors for LLC primary side. New FoMs which consider P_{DR} and P_{SW}, especially relevant at low and medium loads, are needed. Eventually, a new I-V based E_{SW_SOFT} characterization method is proposed and explained and a new FoM based on this intrinsic energy is described.

Acknowledgment

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