Universidad de Oviedo
Universidá d'Uviéu
University of Oviedo

Electrical and Electronic, Computers and Systems Engineering Department

PhD Programme in Electrical and Electronic Engineering

HIGH PERFORMANCE ELECTRONIC SYSTEMS FOR HIGH BAY LIGHT EMITTING DIODES FED FROM ALTERNATING CURRENT POWER GRIDS

presented by

Ignacio Castro Álvarez

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A dissertation submitted to University of Oviedo for the degree of Doctor of Philosophy in Electrical Engineering

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Ignacio Castro Álvarez

JULY 2018

Universidad de Oviedo
Universidá d'Uviéu
University of Oviedo

Departamento de Ingeniería Eléctrica, Electrónica, de Computadores y Sistemas

Programa de doctorado en Ingeniería Eléctrica y Electrónica

SISTEMAS ELECTRÓNICOS DE ALTAS PRESTACIONES PARA DIODOS EMISORES DE LUZ DESDE REDES DE DISTRIBUCIÓN DE ENERGÍA ELÉCTRICA EN CORRIENTE ALTERNA

TESIS DOCTORAL

por

Ignacio Castro Álvarez

JULIO 2018

Universidad de Oviedo
Universidá d'Uviéu
University of Oviedo

PhD dissertation

HIGH PERFORMANCE ELECTRONIC SYSTEMS FOR HIGH BAY LIGHT EMITTING DIODES FED FROM ALTERNATING CURRENT POWER GRIDS

presented by

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JULY 2018

RESUMEN DEL CONTENIDO DE TESIS DOCTORAL

1.- Título de la Tesis	
Español/Otro Idioma: Sistemas Electrónicos de Altas Prestaciones para Diodos Emisores de Luz desde redes de distribución de energía eléctrica en corriente alterna.	Inglés: High Performance Electronic Systems for High Bay Light Emitting Diodes fed from alternating current power grids

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RESUMEN (en español)

Los diodos emisores de luz (*Light-Emitting Diodes*, LEDs) se están convirtiendo en la fuente de luz preferida en nuestras casas, oficinas o calles, debido a su fiabilidad, su larga vida útil, su alto rendimiento lumínico y su bajo coste de mantenimiento. Sin embargo, estos sigues siendo diodos, permitiendo que la corriente sólo circule en un único sentido. Lo cual es de suma importancia ya que existe una relación directa entre la luz emitida y la corriente que atraviesa al LED, haciendo que la conexión directa a una red de distrbución de corriente alterna no sea adecuada debido al fenómeno del parpadeo o *flicker* en la literatura anglosajona, que no sólo es molesto para los seres humanos, sino que a la larga puede causar perjuicios en su salud. Es por ello necesario el uso de una interfaz entre la red y los LEDs de manera que se controle que la corriente que circula a través de ellos sea constante, para así obtener una alta calidad lumínica. Este elemento o interfaz se conoce como controlador de LEDs o *driver* de LEDs en su terminología anglosajona.

Un *driver* de LEDs no deja de ser un convertidor de potencia que alimenta una carga singular y que además no es lineal, lo cual hace que tenga que cumplir una cierta normativa y satisfacer las necesidades de su carga. Por norma general, un equipo electrónico como es un *driver* de LEDs conectado a la red, necesita cumplir la normativa de inyección de harmónicos de baja frecuencia definida por el estándar IEC 61000-3-2, que establece unos límites extremadamente estrictos para todo equipo de iluminación de más de 25 W, no siendo así para aquellos de menor potencia. En este sentido, la normativa específica qué a efectos prácticos, la corriente que demande el *driver* ca-cc de LEDs sea sinusoidal y en fase con su tensión de entrada, lo cual se consigue de forma tradicional mediante el uso de convertidores que alcancen una corrección del factor de potencia (*Power Factor Correction*, PFC) activa, siendo capaces a su vez de propiciar un comportamiento de resistencia libre de pérdidas (*Loss Free Resistor*, LFR) a su entrada. Este comportamiento se consigue en un gran número de topologías mediante un control adecuado. De hecho, en el caso particular de los convertidores ca-cc monofásicos uno de los sistemas más utilizados tradicionalmente se basa en un convertidor elevador con PFC seguido de un convertidor cc-cc aislado galvánicamente, donde el primer convertidor se encarga de obtener el comportamiento

como LFR mientras que el segundo se encarga de controlar la corriente en los LEDs, mejorar el comportamiento dinámico frente a cambios que se produzcan en la carga y de eliminar el condensador electrolítico presente en los convertidores ca-cc para desacoplar la ca de la entrada de la cc a la salida, asegurando que se cumple la normativa de *flicker* definida en la práctica 1 del estándar del IEEE 1789-2015. Este estándar propuesto de forma reciente asegura que el controlador de LEDs garantice una buena calidad lumínica, mediante la limitación del contenido de baja frecuencia típico de las redes de ca en la luz emitida.

La eliminación del condensador electrolítico es de suma importancia, debido a que uno de los requisitos que un *driver* de LEDs debe cumplir es tener una vida útil comparable a la de los LEDs, siendo este elemento es el más limitante para conseguirlo. De hecho, el programa ENERGY STAR®, que define una serie de normas para el *driver* ca-cc de LED, considera que este debe tener un mínimo tiempo de vida útil para otorgarle su sello. Por lo tanto, es comprensible que durante los últimos años la literatura desarrollada alrededor de los *drivers* ca-cc de LED se centre en la eliminación de este elemento mediante el uso de topologías como las cuasi-únicas etapas. Aun así, esto no es siempre factible cuando el coste del *driver* ca-cc de LEDs, y no su fiabilidad, es la especificación de mayor importancia para su diseño, necesitando por tanto un driver ca-cc de LEDs simple y de una única etapa.

El objetivo de la presente tesis es la investigación de diferentes drivers ca-cc de LED para la alimentación de cargas LED (de más de 25 W), en instalaciones comerciales e industriales, para redes monofásicas y trifásicas de corriente alterna, en un rango de potencias que abarque desde las decenas de vatios a unos pocos kilovatios, garantizando también el cumplimiento de la normativa necesaria y con el objetivo de mejorar las soluciones propuestas con anterioridad en la literatura. Teniendo en cuenta que los LED están tendiendo a desplazar a los sistemas de iluminación tradicionales en todos los ámbitos, entonces también lo harán con los focos de alta potencia que necesitarán *drivers* ca-cc de la misma potencia. En ese sentido, y considerando que la mayor parte de instalaciones para las que se propone instalar este tipo de focos tienen disponible el conexionado a la red trifásica, se abre así la posibilidad de usar controladores LED trifásicos. Aquí es importante puntualizar, que el objetivo no es renovar la instalación eléctrica en el entorno doméstico sino utilizar la red trifásica allí donde sea posible.

El estudio realizado en la presente tesis se divide en cinco capítulos proponiendo soluciones de *drivers* ca-cc de LEDs en redes ca. Por ese motivo, y con el objetivo de sentar las bases para el resto de capítulos, el primero de ellos se encarga de resumir los conceptos más básicos en el ámbito del control de iluminación con LEDs, queriendo contestar dos cuestiones: 'por qué van a reemplazar a las luminarias tradicionales' y 'cómo se deben controlar'. Además, se ha realizado un estudio en profundidad que se encarga de especificar las normativas más importantes y de resumir el estado del arte de drivers ca-cc de LED en redes ca. Este último se encarga de clasificar los *drivers* ca-cc de LED en diferentes categorías en función del número de etapas y del tipo de red (ya sea monofásica o trifásica), analizando las ventajas y desventajas de aquellas topologías que se consideren más prometedoras.

RESUMEN (en Inglés)

Light-Emitting Diodes (LEDs) are increasingly becoming our main source of artificial light in our homes, offices or streets due to their reliability, long life, luminous efficacy and low maintenance requirements. However, LEDs are diodes, which means that the current is able to go through them in only one direction. This fact is of utter importance because of the direct relationship between the light outputted by the LED and the current across it, making an impossibility the direct connection to an ac power grid without incurring into the flicker phenomenon which is not only annoying but harmful for human beings. Thus, an interface is required between the ac power grid and the LEDs in order to drive the LEDs with a constant current that ensures a good quality light output. This interface is normally referred as ac-dc LED driver.

An ac-dc LED driver is but a power converter that feeds a very unique and non-linear load, and as such it needs to meet several requirements in accordance to the regulations and the needs of the LEDs. Then, as any equipment connected to the ac power grid it needs to comply with the harmonic injection regulation, IEC 61000-3-2, which in this particular case sets extremely strict limits for ac-dc LED drivers of more than 25 W, being much laxer for those of lower power. In that respect, the regulations demands for the input current of the ac-dc LED driver to be sinusoidal and in phase with the input voltage. This performance is traditionally achieved in Power Factor Correction (PFC) with active solutions whose behaviour at the input is equivalent to a resistance, normally referred as Loss Free Resistor (LFR). Achievement that is feasible by several topologies by means of operating them adequately with the proper control methodology. In fact, for single-phase ac-dc converters, this is conventionally achieved by means of a PFC boost converter, normally followed by a cascaded isolated dc-dc converter. The first converter achieves the desired LFR performance while the second controls the current through the LEDs, improves the dynamic response to load changes, could provide galvanic isolation and could remove the electrolytic capacitor while keeping a flicker free performance that should be ensured by meeting the requirements set by Practice 1 of the IEEE Std. 1789-2015. The newly proposed flicker standard ensures the achievement of good light quality, setting the rules for how much ripple is allowed in the output instantaneous luminance and thus for the current ripple across the LEDs.

The removal of the electrolytic capacitor is extremely important as one of the requirements for ac-dc LED drivers is having a lifetime comparable to that of the LEDs, being this element the most limiting one in order to achieve this feat. In fact, the ENERGY STAR® program, which is a renowned set of rules for ac-dc LED drivers, considers the minimum lifetime of the LED driver as one of the requisites to give its seal of approval. Therefore, it can be understood why the current literature has put so much effort on the study of electrolytic capacitor-less ac-dc LED drivers, which is normally achieved by means of ac-dc quasi-single-stages. Nonetheless, this is not always possible when the cost of the LED driver and not its reliability, is the most limiting factor to be considered in the design, hence requiring the use of a simpler single-stage ac-dc LED driver.

The present dissertation investigates different solutions to drive LED luminaires, which are LED loads of more than 25 W, in commercial and industrial installations for both single-phase and three-phase ac power grids in the range of decades of watts to a few kilowatts, while complying with all of the aforementioned regulations and with the aim of improving the performance of the current state-of-the-art solutions. As a matter of fact, LEDs are prone to take over traditional lighting technologies in every environment, thus replacing high power spotlights that would require high power ac-dc LED drivers.

In that respect, and considering that in most installations in which this high power spotlights are required the three-phase grid is also available, it opens the possibility of using specific three-phase ac-dc LED drivers. It should be noted, it is not the aim of this dissertation to rewire household environments with three-phase power grids, but to use those that are readily available.

The study carried out in this dissertation is organized into five different chapters discussing the driving of LEDs on ac power grids. For that matter, and in order to lay the foundations for the rest of the chapters, the first one summarizes the most basic concepts around LED driving aiming to answer two basic questions, which are: 'why are LEDs more prone to be used in spite of traditional lighting technologies' and 'how are LEDs supposed to be driven'. In addition a thorough analysis has been carried out regarding the different rules set by the regulations for ac-dc LED drivers and the state-of-the-art solutions to drive LED from ac power grids. The latter classifies the ac-dc LED drivers under several categories in accordance to the amount of power stages and the kind of power grid they are meant to be used on (i.e., single-phase or three-phase) while discussing at the same time the advantages and disadvantages of the most promising topologies.

Agradecimientos

Esta quizás sea una de las pocas partes escritas en castellano en este documento de Tesis, y pese a ello va a ser la más complicada de completar, así que intentaré ser breve y conciso. Si alguien considera que me he olvidado de él en esta sección, simplemente gracias y ruego me perdone.

Quisiera agradecer a mis directores de tesis, el Dr. Diego González Lamar y la Dra. Marta María Hernando Álvarez, por su tiempo, dedicación y contribuciones, tanto a la investigación desarrollada como a la realización del presente documento de Tesis. Sin sus ideas y propuestas, la calidad del trabajo se hubiera visto mermada. Me gustaría, además, agradecer encarecidamente al Dr. González Lamar, su paciencia, fe y apoyo, y es que si una cosa tengo clara es que, si no hubiera sido por él, ahora mismo no estaría presentando esta Tesis. Gracias Diego, contigo sí que empezó todo.

Siguiendo con mis directores de tesis, aunque oficialmente no lo sean, me gustaría agradecer al Dr. Francisco Javier Sebastián Zúñiga y al Dr. Manuel Arias Pérez de Azpeitia su tiempo, paciencia y dedicación. Al Dr. Sebastián porque de manera desinteresada ha sido capaz de inocularme una pequeña parte de todo lo que sabe. Y al Dr. Arias porque, aunque te diga a priori: "tú sabes mucho más que yo de este tema", siempre es capaz de aportarte buenas ideas. De verdad, gracias a los dos.

Durante estos cuatro años, he podido disfrutar de un fantástico ambiente de trabajo en el grupo de investigación de Sistemas Electrónicos de Alimentación y por ello me gustaría agradecer al resto de sus componentes: Dr. Alberto Rodríguez, Dr. Aitor Vázquez, Kevin, Juan, María y Dani. En particular, al Dr. Rodríguez y al Dr. Vázquez, por mantener su puerta siempre abierta, aunque fuera para hablar de gilipolleces o José Luises, y al último, además, por participar en la revisión de este documento. La última mención se la dedico a Dani por su ayuda con el proyecto de EFIBAT.

Llegados a este punto considero que Kevin se merece su propio párrafo, por muchos motivos, pero principalmente por la ayuda brindada, porque siempre ha sido capaz de sacarme una sonrisa incluso en los peores momentos y porque es la única persona que conozco a la cual las manzanas le dan angustia al estómago. Gracias, K.

A mis amigos, aunque nos veamos cada vez menos, siempre habéis estado ahí cuando más lo necesitaba. Gracias.

Finalmente, me gustaría agradecer a mis padres, Julios Luis y María Begoña, abuelos, Ignacio, Amelia, María Luisa y Gelinos, tíos, Pedro y Beatriz, primas, Aurora y Ana, y a los que no están, por vuestro apoyo, por vuestro tiempo, por estar ahí, porque nada de esto hubiera sido realmente posible sin vosotros.

It is a well-known established fact throughout the many-dimensional worlds of the multiverse that most really great discoveries are owed to one brief moment of inspiration. There's a lot of spadework first, of course, but what clinches the whole thing is the sight of, say, a falling apple or a boiling kettle or the water slipping over the edge of the bath. Something goes click inside the observer's head and then everything falls into place. The shape of DNA, it is popularly said, owes its discovery to the chance sight of a spiral staircase when the scientist's mind was just at the right receptive temperature. Had he used the elevator, the whole science of genetics might have been a good deal different.

This is thought of as somehow wonderful. It isn't. It is tragic. Little particles of inspiration sleet through the universe all the time traveling through the densest matter in the same way that a neutrino passes through a candyfloss haystack, and most of them miss. Even worse, most of the ones that hit the exact cerebral target, hit the wrong one.

For example, the weird dream about a lead doughnut on a mile-high gantry, which in the right mind would have been the catalyst for the invention of repressed-gravitational electricity generation (a cheap and inexhaustible and totally non-polluting form of power which the world in question had been seeking for centuries, and for the lack of which it was plunged into a terrible and pointless war) was in fact had by a small and bewildered duck.

By another stroke of bad luck, the sight of a herd of wild horses galloping through a field of wild hyacinths would have led a struggling composer to write the famous Flying God Suite, bringing succor and balm to the souls of millions, had he not been at home in bed with shingles. The inspiration thereby fell to a nearby frog, who was not in much of a position to make a startling contributing to the field of tone poetry.

Many civilizations have recognized this shocking waste and tried various methods to prevent it, most of them involving enjoyable but illegal attempts to tune the mind into the right wavelength by the use of exotic herbage or yeast products. It never works properly.

— Terry Pratchett, Sourcery

Resumen

Los diodos emisores de luz (*Light-Emitting Diodes*, LEDs) se están convirtiendo en la fuente de luz preferida en nuestras casas, oficinas o calles, debido a su fiabilidad, su larga vida útil, su alto rendimiento lumínico y su bajo coste de mantenimiento. Sin embargo, estos sigues siendo diodos, permitiendo que la corriente sólo circule en un único sentido. Lo cual es de suma importancia ya que existe una relación directa entre la luz emitida y la corriente que atraviesa al LED, haciendo que la conexión directa a una red de distrbución de corriente alterna no sea adecuada debido al fenómeno del parpadeo o *flicker* en la literatura anglosajona, que no sólo es molesto para los seres humanos, sino que a la larga puede causar perjuicios en su salud. Es por ello necesario el uso de una interfaz entre la red y los LEDs de manera que se controle que la corriente que circula a través de ellos sea constante, para así obtener una alta calidad lumínica. Este elemento o interfaz se conoce como controlador de LEDs o *driver* de LEDs en su terminología anglosajona.

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La eliminación del condensador electrolítico es de suma importancia, debido a que uno de los requisitos que un *driver* de LEDs debe cumplir es tener una vida útil comparable a la de los LEDs, siendo este elemento es el más limitante para conseguirlo. De hecho, el programa ENERGY STAR®, que define una serie de normas para el *driver* ca-cc de LED, considera que este debe tener un mínimo tiempo de vida útil para otorgarle

su sello. Por lo tanto, es comprensible que durante los últimos años la literatura desarrollada alrededor de los *drivers* ca-cc de LED se centre en la eliminación de este elemento mediante el uso de topologías como las cuasi-únicas etapas. Aun así, esto no es siempre factible cuando el coste del *driver* ca-cc de LEDs, y no su fiabilidad, es la especificación de mayor importancia para su diseño, necesitando por tanto un driver ca-cc de LEDs simple y de una única etapa.

El objetivo de la presente tesis es la investigación de diferentes drivers ca-cc de LED para la alimentación de cargas LED (de más de 25 W), en instalaciones comerciales e industriales, para redes monofásicas y trifásicas de corriente alterna, en un rango de potencias que abarque desde las decenas de vatios a unos pocos kilovatios, garantizando también el cumplimiento de la normativa necesaria y con el objetivo de mejorar las soluciones propuestas con anterioridad en la literatura. Teniendo en cuenta que los LED están tendiendo a desplazar a los sistemas de iluminación tradicionales en todos los ámbitos, entonces también lo harán con los focos de alta potencia que necesitarán *drivers* ca-cc de la misma potencia. En ese sentido, y considerando que la mayor parte de instalaciones para las que se propone instalar este tipo de focos tienen disponible el conexionado a la red trifásica, se abre así la posibilidad de usar controladores LED trifásicos. Aquí es importante puntualizar, que el objetivo no es renovar la instalación eléctrica en el entorno doméstico sino utilizar la red trifásica allí donde sea posible.

El estudio realizado en la presente tesis se divide en cinco capítulos proponiendo soluciones de *drivers* ca-cc de LEDs en redes ca. Por ese motivo, y con el objetivo de sentar las bases para el resto de capítulos, el primero de ellos se encarga de resumir los conceptos más básicos en el ámbito del control de iluminación con LEDs, queriendo contestar dos cuestiones: 'por qué van a reemplazar a las luminarias tradicionales' y 'cómo se deben controlar'. Además, se ha realizado un estudio en profundidad que se encarga de especificar las normativas más importantes y de resumir el estado del arte de drivers ca-cc de LED en redes ca. Este último se encarga de clasificar los *drivers* ca-cc de LED en diferentes categorías en función del número de etapas y del tipo de red (ya sea monofásica o trifásica), analizando las ventajas y desventajas de aquellas topologías que se consideren más prometedoras.

Después de haber estudiado y clasificado las soluciones presentes en la literatura, el resto de los capítulos proponen soluciones novedosas en esta temática:

- El **capítulo 2** propone el uso de topologías multi-celda para controlar luminarias LED en redes trifásicas de ca donde se alcanza la eliminación del condensador electrolítico debido a que la potencia no pulsa en una red trifásica balanceada. Por este motivo, se proponen dos *drivers* ca-cc de LEDs, uno con aislamiento galvánico basado en el rectificador trifásico de onda completa, y otra sin aislamiento que se basa en sumar la luz de cada una de las fases de la red para obtener una luz constante. Además, se rescata la topología clásica propuesta por Delco adaptándola para su uso como *driver* ca-cc de LEDs. Este capítulo se centra, sobre todo, en el análisis estático y dinámico que se realiza sobre los tres drivers anteriormente mencionados, poniendo especial énfasis en el comportamiento del *driver* ca-cc de LEDs como LFR trifásicos. De manera particular, para el caso del *driver* basado en la suma de luces es necesario revisar el estudio de los límites entre modo de conducción continuo y discontinuo debido al alto rizado de tensión y corriente permitido a la salida de cada una de

las celdas. Finalmente, el capítulo describe los resultados experimentales obtenidos para los tres *drivers* ca-cc de LED bajo estudio. Posteriormente, se comparan entre sí y con las soluciones presentes en el estado del arte para discernir de forma adecuada sus ventajas y desventajas, mientras se asegura el correcto cumplimiento de la normativa.

- El **capítulo 3** estudia el uso de las topologías alimentadas en corriente con aislamiento galvánico como convertidores ca-cc monofásicos y, por lo tanto, como *drivers* ca-cc de LED monofásicos. Estas topologías, pertenecientes a la familia del convertidor elevador son capaces de obtener un funcionamiento como LFR mediante un control adecuado. Sin embargo, presentan una serie de desventajas que evita que se usen de manera masiva en PFC. Por este motivo, se recupera el convertidor *push-pull* de doble inductancia alimentado en corriente, donde se usa tradicionalmente como convertidor cc-cc de alta ganancia, estudiando su operación como convertidor ca-cc y proponiendo a su vez una estrategia de control sencilla basada en una única medida aislada. Además, es capaz de conseguir un entrelazado (*interleaving*, en la literatura anglosajona) inherente a la topología entre sus dos bobinas reduciendo así el rizado de alta frecuencia en su corriente de entrada y presente en ambas bobinas debido a su operación en modo de conducción crítico, manteniendo un diseño simple de su transformador que es capaz de mejorar su rendimiento superando así muchas de las limitaciones presentes en las topologías alimentadas en corriente y consiguiendo compararse con soluciones presentes en el estado del arte de los *drivers* ca-cc LED monofásicos.

- **El capítulo 4** presenta una familia de convertidores simples para su conexión a redes de corriente continua, y que en la presente tesis tienen como objetivo ser usados como post-reguladores, siendo esta la última etapa de un *driver* ca-cc de LEDs multi-etapa. La idea se basa en reemplazar el diodo rectificador de los convertidores tradicionales cc-cc más básicos por LEDs. De esta manera, los LEDs trabajarán no sólo como carga sino también como diodo rectificador del convertidor, circulando a través de ellos corrientes de alta frecuencia cuya luz se aprecia como constante por del ojo humano. Este tipo de control se conoce en la literatura como control AC-LED. Desde el punto de vista de usar LEDs como rectificadores es necesario realizar un estudio sobre sus capacidades de conmutación, especialmente estudiando el fenómeno de la recuperación inversa. Este último se puede eliminar reemplazando el interruptor principal con un interruptor cuasi-resonante de onda completa. Con este cambio se concibe una nueva familia de convertidores que es analizada estáticamente y experimentalmente validada. Finalmente, el capítulo compara en términos de fiabilidad en un periodo de 700 h el uso de los convertidores AC-LED cuasi-resonantes con los que no lo son y con las topologías tradicionales, observando así el impacto del fenómeno de recuperación inversa en la vida útil de los LEDs.

- El **capítulo 5** concluye este trabajo debatiendo sobre las conclusiones más importantes que se han podido extraer de los desarrollos teóricos y los resultados experimentales. Finalmente, se proponen líneas de investigación futuras alrededor de la temáctica de esta tesis.

Abstract

Light-Emitting Diodes (LEDs) are increasingly becoming our main source of artificial light in our homes, offices or streets due to their reliability, long life, luminous efficacy and low maintenance requirements. However, LEDs are diodes, which means that the current is able to go through them in only one direction. This fact is of utter importance because of the direct relationship between the light outputted by the LED and the current across it, making an impossibility the direct connection to an ac power grid without incurring into the flicker phenomenon which is not only annoying but harmful for human beings. Thus, an interface is required between the ac power grid and the LEDs in order to drive the LEDs with a constant current that ensures a good quality light output. This interface is normally referred as ac-dc LED driver.

An ac-dc LED driver is but a power converter that feeds a very unique and non-linear load, and as such it needs to meet several requirements in accordance to the regulations and the needs of the LEDs. Then, as any equipment connected to the ac power grid it needs to comply with the harmonic injection regulation, IEC 61000-3-2, which in this particular case sets extremely strict limits for ac-dc LED drivers of more than 25 W, being much laxer for those of lower power. In that respect, the regulations demands for the input current of the ac-dc LED driver to be sinusoidal and in phase with the input voltage. This performance is traditionally achieved in Power Factor Correction (PFC) with active solutions whose behaviour at the input is equivalent to a resistance, normally referred as Loss Free Resistor (LFR). Achievement that is feasible by several topologies by means of operating them adequately with the proper control methodology. In fact, for single-phase ac-dc converters, this is conventionally achieved by means of a PFC boost converter, normally followed by a cascaded isolated dc-dc converter. The first converter achieves the desired LFR performance while the second controls the current through the LEDs, improves the dynamic response to load changes, could provide galvanic isolation and could remove the electrolytic capacitor while keeping a flicker free performance that should be ensured by meeting the requirements set by Practice 1 of the IEEE Std. 1789-2015. The newly proposed flicker standard ensures the achievement of good light quality, setting the rules for how much ripple is allowed in the output instantaneous luminance and thus for the current ripple across the LEDs.

The removal of the electrolytic capacitor is extremely important as one of the requirements for ac-dc LED drivers is having a lifetime comparable to that of the LEDs, being this element the most limiting one in order to achieve this feat. In fact, the ENERGY STAR® program, which is a renowned set of rules for ac-dc LED drivers, considers the minimum lifetime of the LED driver as one of the requisites to give its seal of approval. Therefore, it can be understood why the current literature has put so much effort on the study of electrolytic capacitor-less ac-dc LED drivers, which is normally achieved by means of ac-dc quasi-single-stages. Nonetheless, this is not always possible when the cost of the LED driver and not its reliability, is the most limiting factor to be considered in the design, hence requiring the use of a simpler single-stage ac-dc LED driver.

The present dissertation investigates different solutions to drive LED luminaires, which are LED loads of more than 25 W, in commercial and industrial installations for both single-phase and three-phase ac power grids in the range of decades of watts to a few kilowatts, while complying with all of the aforementioned regulations and with the aim of improving the performance of the current state-of-the-art solutions. As a matter of fact, LEDs are prone to take over traditional lighting technologies in every environment, thus replacing high power spotlights that would require high power ac-dc LED drivers. In that respect, and considering that in most installations in which this high power spotlights are required the three-phase grid is also available, it opens the possibility of using specific three-phase ac-dc LED drivers. It should be noted, it is not the aim of this dissertation to rewire household environments with three-phase power grids, but to use those that are readily available.

The study carried out in this dissertation is organized into five different chapters discussing the driving of LEDs on ac power grids. For that matter, and in order to lay the foundations for the rest of the chapters, the first one summarizes the most basic concepts around LED driving aiming to answer two basic questions, which are: 'why are LEDs more prone to be used in spite of traditional lighting technologies' and 'how are LEDs supposed to be driven'. In addition a thorough analysis has been carried out regarding the different rules set by the regulations for ac-dc LED drivers and the state-of-the-art solutions to drive LED from ac power grids. The latter classifies the ac-dc LED drivers under several categories in accordance to the amount of power stages and the kind of power grid they are meant to be used on (i.e., single-phase or three-phase) while discussing at the same time the advantages and disadvantages of the most promising topologies.

After having studied and classified the state-of-the-art solutions, the rest of the chapters discuss the proposals of this work in accordance to the aforementioned classification:

- **Chapter 2** proposes the use of multi-cell three-phase topologies to drive LED loads in three-phase ac power grids, taking advantage of the intrinsic removal of the electrolytic capacitor due to the non-pulsation of the power in balanced three-phase power grid. In that respect, it proposes two ac-dc LED drivers, one with galvanic isolation based on the three-phase full-wave rectifier, and another one without galvanic isolation based on summing the light output of each phase. In addition, the Delco topology is retrieved for this application and adjusted accordingly to operate as an ac-dc LED driver. More importantly, this chapter includes the static and dynamic analysis of all three ac-dc LED drivers with special focus on the desired LFR performance at the input of each phase. Particularly, the operation of cells in the multi-cell ac-dc LED driver based on summing the light output requires to revise the limits between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) due to the high voltage and current ripple allowed at the output of each cell. The last sections of these chapter are dedicated to the experimental results obtained for the three ac-dc LED drivers under study which are compared in between and with the state-of-the-art solutions carefully analyzing their advantages and disadvantages while ensuring compliance with the required regulations.

- **Chapter 3** discusses the use of isolated current-fed topologies as single-phase ac-dc converters, and thus as single-phase ac-dc LED drivers. These topologies from the boost family achieve a LFR performance by means of control. However, they present several drawbacks preventing them from achieving outstanding performances. For that matter, the Dual Inductor Current-fed Push-Pull (DICPP) is retrieved from literature, where it is used as a high step-up dc-dc converter, and studied to operate as an ac-dc converter, proposing a simple control based on one isolated measurement. In addition its intrinsic interleaving between both inductors is able to reduce the input current ripple that both inductors present due to their operation in Boundary Conduction Mode (BCM), while it simpler transformer design improves the efficiency overcoming most of the limitations present for single-phase current-fed topologies and achieving a performance comparable to state-of-the-art single-phase ac-dc LED drivers. At the cost of having a demagnetization circuit and requiring switches with breakdown voltages of 900/1200 V to correctly operate in universal voltage range.

- **Chapter 4** presents, unlike the previous chapters, a family of simple converters that are to be connected to a dc power grid, thus aimed to be used as the post-regulator stage of a multi-stage ac-dc LED driver. The idea behind this family of converters is based on replacing the rectifier diode of the conventional dc-dc converters with the LED load. Hence, the LED load will work both as the load and as the rectifier diode of the converter, being driven by a high frequency current whose output light human eyes render constant, and being referred in literature as AC-LED driving. In that respect, the switching performance of the LEDs needs to be studied with special focus put on the reverse recovery effect. The latter is avoided by replacing the main switch with a full-wave quasi-resonant switch rendering the actual family of converters, which is statically analyzed and experimentally validated. Finally, the chapter compares experimentally the reliability over a period of 700 hours for the conventional converter, the quasi-resonant AC-LED driver and the non-resonant version, focusing on observing the impact of the reverse recovery on the lifetime of the LEDs.

- **Chapter 5** concludes this work discussing the most important conclusions extracted from the theoretical and experimental analysis, that lead to the proposal of future research around the topic of this dissertation.

Contents

List of figures

List of tables

Nomenclature

Symbol	Definition
α	Constant that relates linearly the relationship between the low frequency modulation of the light and the current provided to the LEDs, for a certain LED under study.
α_n	Variable that defines the set of values that ensure ZCS operation in the DL//S AC-LED driver.
β_n	Variable that defines the set of values that ensure ZCS operation in the DL//L AC-LED driver.
$\Delta i_{\%}$	Percentage peak-to-peak current ripple of the current across the main inductance in a ZCS-QRC AC-LED driver.
Δi_{CN}	Peak-to-peak current ripple of the current across the LED load.
Δi_L	Current ripple of the current across the main inductance in a ZCS-QRC AC-LED driver.
ζ	Factor that scales the output current when measuring the experimental open loop gain in the ZCS-QRC AC-LED drivers.
κ	Factor that scales t_{on} to admissible values of the ADC.
μ	Control variable of the ZCS-QRC AC-LED drivers.
ξ	Damping of the resonant tank defined by L_r and C_r.
σ	Factor that scales the average output current in the DICPP ac-dc LED driver.
φ	Defines a phase shift between voltage and current. Typically refers to (2.42).
φ_{norm}	Normalized value of φ, when referred as (2.42).
$\phi(t)$	Instantaneous value of the perceived light by the human eye.
Φ_1	Constant perceived light by the human eye at half load.
Φ_2	Constant perceived light by the human eye at full load.
Φ_p	Peak of the emitted light with PWM dimming.
ω	Angular frequency of the mains.
ω_n	Angular frequency of the resonant tank in the ZCS-QRC AC-LED drivers.

$a(k)$	Coefficients of the Fourier series.
$a(t)$	Auxiliary waveform defined during the analysis carried out in Section 4.2.
a_1	Auxiliary parameter defined for the analysis carried out in Subsection 2.4.1.2.
a_2	Auxiliary parameter defined for the analysis carried out in Subsection 2.4.1.2.
A_3	Auxiliary parameter defined for the analysis carried out in Subsection 2.4.3.2.
A_4	Auxiliary parameter defined for the analysis carried out in Subsection 2.4.3.2.
$b(t)$	Auxiliary waveform defined during the analysis carried out in Section 4.2.
$c(t)$	Auxiliary waveform defined during the analysis carried out in Section 4.2.
$C(z)$	Discrete transfer function of the compensator designed in Appendix A.
C_{AF}	Active filter capacitance.
C_B	Bulk capacitor.
C_r	Resonant capacitor.
C_N	Intermediate bulk capacitor used in a two-stage cell connected to phase N, or output capacitor of phase N in a multi-cell LED driver based on summing the light output of each phase. Considering that N can take either the R, S or T value.
C_R	Intermediate bulk capacitor used in a two-stage cell connected to phase R, or output capacitor of phase R in a multi-cell LED driver based on summing the light output of each phase.
C_S	Intermediate bulk capacitor used in a two-stage cell connected to phase S, or output capacitor of phase S in a multi-cell LED driver based on summing the light output of each phase.
C_T	Intermediate bulk capacitor used in a two-stage cell connected to phase T, or output capacitor of phase T in a multi-cell LED driver based on summing the light output of each phase.
C_o	Output capacitance of an ac-dc LED driver, typically electrolytic-free.
C_{oss}	Output capacitance on a MOSFET.

CCT(t)	Correlated Color Temperature measured in Kelvin and considering its variation with time.
d	Duty cycle.
$\hat{d}$	Small-signal ac variations of the duty cycle.
D	Duty cycle particularized at a certain operating point.
D_1	Duty cycle at half load when applying PWM dimming.
D_2	Duty cycle at full load when applying PWM dimming.
f_0	Fundamental frequency of the luminance.
f_n	Frequency of the resonant tank in the ZCS-QRC AC-LED drivers.
f_s	Switching frequency.
$f_s(t)$	Instantaneous value of the switching frequency, when allowed to changed due to control criteria.
$f_{s,min}$	Minimum value of $f_s(t)$.
$f_{s,max}$	Maximum value of $f_s(t)$.
f_s	Normalized value of f_s.
$f_{s,norm}(t)$	Normalized value of $f_s(t)$.
g_{iggp}	Input current gain versus variations in the on time.
g_{iogp}	Output current gain versus variations in the peak input voltage.
g_{ioon}	Output current gain versus variations in the on time.
$G_{i_o d}(s)$	Transfer function that relates the small-signal ac variations of d to the small-signal ac variation of i_o.
$G_{i_o d}(z)$	Discrete transfer function that relates the small-signal ac variations of d to the small-signal ac variation of i_o.
$G_{i_o t_{on}}(s)$	Transfer function that relates the small-signal ac variations of t_{on} to the small-signal ac variation of i_o.
$G_{i_o v_c}(s)$	Transfer function that relates the small-signal ac variations of v_c to the small-signal ac variation of i_o.
$G_{i_o v_{gp}}(s)$	Transfer function that relates the small-signal ac variations of v_{gp} to the small-signal ac variation of i_o.
$G_{i_{oN} v_c}(s)$	Transfer function that relates the small-signal ac variations of v_c to the small-signal ac variation of i_{oN}.
$G_{l_o v_c}(s)$	Transfer function that relates the small-signal ac variations of v_c to the small-signal ac variation of l_o.

i_{ac}	Peak current value of the ac component that across the LED load in a multi-cell ac-dc LED driver based on summing the light output of each phase.
$i_{ac,norm}$	Normalized value of i_{ac}.
I_{base}	Parameter defined as the knee-voltage over the dynamic resistance of a certain LED.
$i_{Cellm}(t)$	Input current demanded by the m^{th} LFR cell in a multi-cell ac-dc LED driver, considering its variation with time.
i_{dc}	Dc current value of the current across the LED load in a multi-cell ac-dc LED driver based on summing the light output of each phase.
$i_D(t)$	Instantaneous value of the current across the high frequency diode bridge in the DICPP ac-dc LED driver.
$i_{D,avg}(t)$	Instantaneous value of the current across the high frequency diode bridge averaged at switching period in the DICPP ac-dc LED driver.
I_{Dmax}	Maximum current that needs to be withstood by each of the diodes that comprise the high frequency diode bridge in the DICPP ac-dc LED driver.
i_F	Average LED forward current.
$i_F(t)$	Instantaneous value of the LED forward current.
I_{F1}	Constant LED forward current at half load.
I_{F2}	Constant LED forward current at full load.
I_{Fp}	Peak forward current of an LED when applying PWM dimming.
$i_{in}(t)$	Instantaneous value of the input current of a single-phase ac-dc LED driver, considering its variation with time and typically averaged at switching frequency.
$i_{in,avg}(t)$	Instantaneous value of the input current averaged at switching period in the DICPP ac-dc LED driver.
$i_{Lin1}(t)$	Instantaneous value of the current across L_{in1} in the DICPP ac-dc LED driver.
$i_{Lin1,peak}(t)$	Instantaneous value of the peak current across L_{in1} in the DICPP ac-dc LED driver.
$i_{Lin1,avg}(t)$	Instantaneous value of the current across L_{in1} averaged at switching period in the DICPP.

$i_{Lin2}(t)$	Instantaneous value of the current across L_{in2} in the DICPP ac-dc LED driver.
$i_{Lin2,peak}(t)$	Instantaneous value of the peak current across L_{in2} in the DICPP ac-dc LED driver..
$i_{Lin2,avg}(t)$	Instantaneous value of the current across L_{in2} averaged at switching period in the DICPP ac-dc LED driver.
$i_{Lr}(t)$	Instantaneous value of the current across the resonant inductance in the ZCS-QRC AC-LED drivers.
i_n	Dimensionless parameter defined for the normalized analysis carried out in Subsection 2.4.1.2, and strongly related to the dc current across the LED load.
$i_N(t)$	Instantaneous value of the input current of phase N in a three-phase ac-dc LED driver. Typically averaged in terms of the switching frequency. Considering N takes the value of either R, S or T.
i_o	Output current of an LED driver, being also the current across the LED load.
$i_o(t)$	Instantaneous value of the output current of an LED driver, being also the instantaneous value of the current across the LED load.
$\hat{i}_o$	Small-signal ac variations of the output current of an LED driver.
I_o	Output current of an LED driver particularized at a certain operating point.
$i_{oCellm}(t)$	Instantaneous value of the output current of $Cell_m$.
i_{oN}	Average value of the output current across the LED load of phase N in the multi-cell ac-dc LED driver based on summing the light output of each phase. Considering N can take either the R, S or T value.
$\hat{i}_{oN}$	Small-signal ac variation of the output current across the LED load of phase N in the multi-cell ac-dc LED driver based on summing the light output of each phase. Considering N can take either the R, S or T value.
I_{oN}	Output current across the LED load of phase N particularized at a certain operating point, in the multi-cell ac-dc LED driver based on summing the light output of each phase. Considering N can take either the R, S or T value.
$i_{oN}(t)$	Instantaneous value of the output current across the LED load of phase N in the multi-cell ac-dc LED driver based on summing the

	light output of each phase. Considering N can take either the R, S or T value.
$i_{oN,norm}(t)$	Normalized expression of $i_{oN}(t)$.
$i_{oR}(t)$	Instantaneous value of the output current across the LED load of phase R in the multi-cell ac-dc LED driver based on summing the light output of each phase.
$i_{oS}(t)$	Instantaneous value of the output current across the LED load of phase S in the multi-cell ac-dc LED driver based on summing the light output of each phase.
$i_{oT}(t)$	Instantaneous value of the output current across the LED load of phase T in the multi-cell ac-dc LED driver based on summing the light output of each phase.
I_{Qmax}	Maximum current that needs to be withstood by the main switches in the DICPP ac-dc LED driver.
$i_R(t)$	Instantaneous value of the input current of phase R in a three-phase ac-dc LED driver. Typically averaged in terms of the switching frequency.
i_{ref}	Current reference for an output current feedback loop.
$i_S(t)$	Instantaneous value of the input current of phase S in a three-phase ac-dc LED driver. Typically averaged in terms of the switching frequency.
$i_T(t)$	Instantaneous value of the input current of phase T in a three-phase ac-dc LED driver. Typically averaged in terms of the switching frequency.
k	k^{th} harmonic of the Fourier series.
K	Number of the harmonic coincidental with the maximum frequency set by Practice 1 of the IEEE Std. 1789.
$k(\omega t)$	Dimensionless parameter traditionally defined for the study of the limits between CCM and DCM in a dc-dc converter.
K_1	Constant that helps defining the resistive value of an LFR, and that depends on the design parameters of the converter.
$k_2(\omega t)$	Auxiliary parameter that gives the condition that guarantee CCM or DCM operation on a dc-dc converter operating with high ripple current on its LED load.
$k_{2,norm}(\omega t)$	Normalized value of $k_2(\omega t)$.
$k_{2,norm,N}(\omega t)$	Generalization of $k_{2,norm}(\omega t)$ for any phase. Considering N takes the value of either R, S or T.

$k_{crit}(\omega t)$	Value of the dimensionless parameter, traditionally defined for the study of the limits between CCM and DCM in a dc-dc converter, in the boundary between CCM and DCM.
k_n	Dimensionless parameter defined for the normalized analysis carried out in Subsection 2.4.1.2 and strongly related to the value of C_N.
$l(t)$	Instantaneous value of the luminance.
L	Main inductance of a converter.
L_{70}	Defines the elapsed operating time over which the LED light source will maintain a 70% of its initial light output.
L_{dc}	Constant average luminance.
$l_H(t, k)$	Instantaneous value of the k^{th} harmonic of the luminance.
$L_{H,min}(k)$	Minimum luminance of the k^{th} harmonic.
$L_{H,max}(k)$	Maximum luminance of the k^{th} harmonic.
L_m	Magnetizing inductance of a transformer.
L_{min}	Minimum luminance of a luminance waveform.
L_{max}	Maximum luminance of a luminance waveform.
l_o	Average value of the output luminance of the multi-cell ac-dc LED driver based on summing the light output of each phase.
$\hat{l}_o$	Small-signal ac variation of the output luminance of the multi-cell ac-dc LED driver based on summing the light output of each phase.
$l_{o,norm}$	Normalized average value of the output luminance of the multi-cell ac-dc LED driver based on summing the light output of each phase.
$l_o(t)$	Instantaneous value of the output luminance of the multi-cell ac-dc LED driver based on summing the light output of each phase.
L_r	Resonant inductor.
m	Number of elements in a series. Typically used as the number of LED strings in parallel comprising an LED load.
M	Ratio between the voltage withstood by the LED load and the peak of the input voltage.
$m(\omega t)$	Dc voltage conversion ratio of an LFR.
Mod. (%)	Defines percent flicker, in accordance to (1.4).

n	Number of elements serialized in a matrix. Typically used as the number of LEDs in an LED string.
N	Represents the phase under study in a three-phase ac-dc LED driver, taking either the R, S or T value.
N_1	Number of turns on the primary side of a transformer.
N_2	Number of turns on the secondary side of a transformer.
$p(t)$	Pulsating power.
P_{base}	Parameter defined as I_{base} multiplied by the knee-voltage of the LED.
$p_{CAF}(t)$	Pulsating power at twice the mains frequency on the output capacitance of an active filter, C_{AF}.
p_{in}	Average input power of an LED driver.
$p_{in}(t)$	Pulsating input power of an ac-dc LED driver. Typically at twice the mains frequency.
$p_{indc}(t)$	Pulsating power at twice the mains frequency at the input of dc-dc converter used as a second stage. Typically referred to a single-phase multi-stage ac-dc LED driver.
p_{LED}	Power consumption of a single LED.
p_N	Average input power of phase N in a three-phase ac-dc LED driver. Considering N takes the value of either R, S or T.
$p_N(t)$	Pulsating input power of phase N in a three-phase ac-dc LED driver. Considering N takes the value of either R, S or T.
p_o	Average output power of an LED driver.
$p_{o,max}$	Maximum output power of an LED driver.
$p_o(t)$	Pulsating output power of an ac-dc LED driver at either twice or six times the mains frequency, depending if the ac-dc LED driver is connected to a single-phase or three-phase, respectively.
$p_R(t)$	Pulsating input power of phase R in a three-phase ac-dc LED driver.
$p_{R+}(t)$	Pulsating input power of phase R demanded by $Cell_1$ in a multi-cell ac-dc LED driver based on the thee-phase full-wave rectifier.
$p_{R-}(t)$	Pulsating input power of phase R demanded by $Cell_4$ in a multi-cell ac-dc LED driver based on the thee-phase full-wave rectifier.

$p_S(t)$	Pulsating input power of phase S in a three-phase ac-dc LED driver.
$p_{S+}(t)$	Pulsating input power of phase S demanded by $Cell_2$ in a multi-cell ac-dc LED driver based on the thee-phase full-wave rectifier.
$p_{S-}(t)$	Pulsating input power of phase S demanded by $Cell_5$ in a multi-cell ac-dc LED driver based on the thee-phase full-wave rectifier.
$p_T(t)$	Pulsating input power of phase T in a three-phase ac-dc LED driver.
$p_{T+}(t)$	Pulsating input power of phase T demanded by $Cell_3$ in a multi-cell ac-dc LED driver based on the thee-phase full-wave rectifier.
$p_{T-}(t)$	Pulsating input power of phase T demanded by $Cell_6$ in a multi-cell ac-dc LED driver based on the thee-phase full-wave rectifier.
Q	Designation used for the main switches of an LED driver.
$r(\omega t)$	Input resistance seen by an LFR.
R_B	Resistor responsible for limiting the maximum peak in passive ac-dc LED drivers.
R_{EXT}	External resistor added in series with an LED string to achieve resistive passive current sharing.
r_{eq}	Equivalent resistance of an LED load, defined by (2.6).
R_{eq}	Equivalent resistance of an LED load particularized at a certain operating point, and defined by (2.14).
r_i	Input current inverse gain versus variations in the peak input voltage.
r_{LED}	Dynamic resistance of an LED.
R_{LFR}	Resistive value of an LFR.
r_o	Output current inverse gain versus variations in the output voltage.
T_0	Fundamental period of the luminance.
T_{delay}	Amount of time that sets the adequate phase shift of the slave driving signal in a DICPP ac-dc LED driver.
t_{on}	On-time of the main switch. Typically referred to a constant on-time required for operation in BCM in a boost converter.

$\hat{t}_{on}$	Small-signal variations of the on-time of the main switch.
T_{on}	On-time of the main switch particularized at a certain operating point.
$t_{off}(t)$	Instantaneous value of the off-time on the main switch.
T_n	Resonant period of the resonant tank in the ZCS-QRC AC-LED drivers.
T_s	Switching period.
$T_s(t)$	Instantaneous value of the switching period, when allowed to changed due to control criteria.
V_{γ_LED}	Knee-voltage of an LED.
v_a	Control variable responsible for controlling the input power in a boost operating in CCM with MBC as an LFR.
$\hat{v}_a$	Small-signal ac variations of the control variable responsible for controlling the input power in a boost operating in CCM with MBC as an LFR.
V_a	Control variable responsible for controlling the input power in a boost operating in CCM with MBC as an LFR, particularized at a certain operating point.
$v_{CAF}(t)$	Pulsating voltage at twice the mains frequency on C_{AF}. Typically referred to the Multi-output voltage ripple cancellation method, see Fig. 1.18 (b).
$v_{CB}(t)$	Pulsating voltage at twice the mains frequency on C_B. Typically referred to the Multi-output voltage ripple cancellation method, see Fig. 1.18 (b).
v_c	Control variable responsible for controlling the input power in an LFR based dc-dc converter.
$\hat{v}_c$	Small-signal ac variation of the variable responsible for controlling the input power in an LFR based dc-dc converter.
V_c	Control variable responsible for controlling the input power in an LFR based dc-dc converter particularized at a certain operating point.
V_{cc}	Voltage set by an auxiliary power supply.
$v_{CN}(t)$	Instantaneous value of the voltage on capacitance C_N.
$v_{Cr}(t)$	Instantaneous value of the output voltage in the ZCS-QRC AC-LED drivers.

V_{Dmax}	Maximum voltage that needs to be withstood by each of the diodes that comprise the high frequency diode bridge in the DICPP ac-dc LED driver.
$v_{DS}(t)$	Voltage withstood by a MOSFET between drain and source.
v_{EN}	Signal that enables a certain PFC boost in a two-stage cell.
v_F	LED forward voltage.
V_{GG}	Maximum voltage of the driving signal (i.e., $v_{GS}(t)$).
v_{gn}	Dimensionless parameter defined for the normalized analysis carried out in Subsection 2.4.2.1, and strongly related to the v_{gp}.
v_{gp}	Peak of the input voltage in an ac power grid.
$\hat{v}_{gp}$	Small-signal ac variations of the peak of the input voltage in an ac power grid.
V_{gp}	Peak of the input voltage in an ac power grid particularized a certain operating point.
V_{gpmax}	Maximum peak of the input voltage in an ac power grid.
$v_{GS}(t)$	Voltage applied between gate and source on a MOSFET to drive it.
v_{in}	Average value of the input voltage.
$v_{in}(t)$	Instantaneous value of the input voltage of a single-phase ac-dc LED driver.
v_{IN}^{+}	Positive input port of an LFR cell.
v_{IN}^{-}	Negative input port of an LFR cell.
$v_L(t)$	Instantaneous value of the luminance measured by a transimpedance amplifier with low bandwidth.
$v_N(t)$	Input voltage of phase N in a three-phase ac-dc LED driver. Considering N can take either the R, S or T value.
v_o	Output voltage of an LED driver, being also the voltage withstood by the LED load.
$v_o(t)$	Instantaneous value of the output voltage of an LED driver, being also the current withstood by the LED load.
V_o	Output voltage of an LED driver particularized at a certain operating point.
v_o^{+}	Positive output port of an LFR cell.
v_o^{-}	Negative output port of an LFR cell.

v_{oN}	Average value of the output voltage withstood the LED load of phase N in the multi-cell ac-dc LED driver based on summing the light output of each phase. Considering N can take either the R, S or T value.
$v_{oN}(t)$	Instantaneous value of the output voltage withstood the LED load of phase N in the multi-cell ac-dc LED driver based on summing the light output of each phase. Considering N can take either the R, S or T value.
V_{Qmax}	Maximum voltage that needs to be withstood by the main switches in the DICPP ac-dc LED driver.
$v_R(t)$	Input voltage of phase R in a three-phase ac-dc LED driver.
v_s	Equivalent voltage source of an AICS.
$v_S(t)$	Input voltage of phase S in a three-phase ac-dc LED driver.
$v_T(t)$	Input voltage of phase T in a three-phase ac-dc LED driver.
Z_n	Characteristic impedance of the resonant tank in the ZCS-QRC AC-LED drivers.

Abbreviations

Symbol	Definition
ADC	Analog-Digital Converter.
ac-dc	Alternating current – direct current.
AC-LED driver	LED driver that uses a pulsating current to drive the LED load.
AICS	Active Input Current Shaper.
AHB	Asymmetrical Half Bridge.
ANSI	American National Standards Institute.
AWG	American Wire Gauge.
BCM	Boundary Conduction Mode.
CCM	Continuous Conduction Mode.
CCT	Correlated Color Temperature.
CENELEC	European committee for electrotechnical standardization.
CFL	Compact Fluorescent Lights.
CPP	Current-fed Push-Pull.
CR	Current Regulator.
CRI	Color Rendering Index.
dc-dc	Direct current-direct current.
DCM	Discontinuous Conduction Mode.
DICPP	Dual Inductor Current-fed Push-Pull.
DL//L	LED paralleled with the converters inductor.
DL//S	LED paralleled with switch.
EMI	Electromagnetic Interference.
FEA	Finite Element Analysis.
FPGA	Field-Programmable Gate Array.
HF	High Frequency.
HV	High Voltage.
IC	Integrated Circuit.

ICC	Input Current Controller.
IEC	International Electrotechnical Commision.
IEEE	Institute of Electrical and Electronics Engineers.
InGaN	Indium gallium nitride.
IPOP	Input Parallel Output Parallel.
IPOS	Input Parallel Output Series.
ISOP	Input Series Output Parallel.
ISOS	Input Series Output Series.
Lamp	Lighting load of less than 25 W.
LED	Light-Emitting Diode.
LF	Low Frequency.
LFR	Loss Free Resistor.
LR	Light Regulator.
Luminaire	Lighting load of more than 25 W.
MBC	Multiplier Based Control.
MKP	Metallized Polypropylene.
MKT	Metallized Polyester.
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor.
NLCC	Nonlinear-Carrier Control.
NOEL	No Observable Effect Level.
OCC	One-Cycle Control.
OECD	Organization for Economic Co-operation and Development.
PCB	Printed Circuit Board.
PF	Power Factor.
PFC	Power Factor Correction.
PLL	Phased Lock Loop.
PWM	Pulse Width Modulation.
QRC	Quasi-Resonant Converter.
Si	Silicon.
SiC	Silicon Carbide.

SMPS	Switching Mode Power Supply.
THD	Total Harmonic Distortion.
VCCRC	Voltage Controlled Compensation Ramp Control.
VFC	Voltage Follower Control.
VLC	Visible Light Communications.
ZAHB	Zeta Asymmetrical Half-Bridge.
ZCD	Zero Current Detector.
ZCL	Zero Current Level.
ZCS	Zero Current Switching.
ZCS-QRC	Zero Current Switching-Quasi Resonant Converter.
ZVS	Zero Voltage Switching.

1

Introduction

Electric power is modern society's cornerstone technology on which virtually all other infrastructures and services depend.

— National Research Council.

The present chapter serves as an introduction into the current state of the art strategies to drive light-emitting diodes from ac power grids, stating the scope and motivation for this dissertation. Moreover, the chapter focuses on analyzing the required regulations, challenges and applicability of LED drivers in both single-phase and three-phase ac power grids, after thoroughly analyzing the state-of-the-art. Finally, the contributions promoted in this dissertation will be presented in the last section of this chapter.

1.1 General trends in power electronics

Power electronics become a necessity and a possibility at the beginning of the 20th century and have continued to grow exponentially to our days. The reason behind this growth can be found all around us with the tremendous amount of electronic systems and devices that require electricity and a power conversion to adjust their voltage and current to their specific requirements. Hence, making power electronics one of the biggest markets in our modern society and a major research topic [1.1], [1.2].

From the beginning, research on the topic of power electronics, independently of the area, has been focused on achieving: higher efficiencies, higher power density, lower failure rate and lower costs. In fact, the exponential growth of electronic systems and devices, due to our newer demands, have made us the most electrically dependent society in human history [1.3]. These demands have increased electronic waste and electric consumption dramatically; in fact, the latter has multiplied by four worldwide from 1971 to 2015. However, in the last 10 years due to legislation, media awareness and research in power electronics, the electricity consumption has stabilized in countries belonging to the Organization for Economic Co-operation and Development (OECD) reducing also their dependency to fossil fuels [1.4], which has helped the rise of renewable energy sources. Hence, apart from achieving the aforementioned performance improvements, nowadays, power electronics also need to be sustainable for the environment. Accomplishing those performance improvements is not a simple task, as there are limited

degrees of freedom in the design of power electronic systems, such as, components, topologies, control, design procedure, standardization, manufacturing and application areas [1.5].

The ubiquity of power electronics in our daily life and in almost every commercial topic, from the automation to the telecommunication industry, is key to make the most of the limited electrical energy at our disposal. Similarly, the lighting industry is completely reliant on power electronics from the driver to the newer and most efficient lighting products, based on Light-Emitting Diodes (LEDs).

1.1.1 Lighting

Nowadays, life seems almost inconceivable without an electrical light source by our side. In fact, during 2016 the estimation of electric energy consumption by both the residential sector and the commercial sector in the US, as a matter of exemplifying the aforementioned fact, represented about 7% of the total US electricity consumption [1.6]. Not so long ago, in 2003 electrical light consumption was about 38% of the total electric energy consumption in the commercial sector, being by far the largest end use as a share of total electric energy consumption [1.6]. This number has lowered over the years thanks to the improvements made in lamp technology, which have replaced most of their inefficient and obsolete incandescent lamps with fluorescents lamps. Hence, looking for more efficient methods to light our homes, offices, streets and cars is key for a sustainable world. It should be noted that throughout this dissertation, the term lamp will be used to define those lighting products of less than 25 W.

The latest trends in lighting technology are summarized in Table 1.1, where it can be seen a comparison for different lightning technologies in terms of their luminous efficacy, lifetime and Color Rendering Index (CRI). The luminous efficacy gives an estimation of how efficient the lighting technology actually is, whereas the CRI indicates its ability to show natural colors the higher this index is. As a result of this comparison, it can be seen that white LEDs represent the lighting technology with the higher lifetime and luminous efficacy potential at the cost of having lower CRI. Nonetheless, the newest lamps from manufacturers, such as Cree or Lumiled, are able to achieve luminous efficacies up to 170 lm/W with a lifetime of 50,000 h and a CRI close to 90 [1.8].

1.2 Light-emitting diodes

LED technology has been a reality since the latest 1950s. However, the first visible LEDs were extremely inefficient [1.9]. It would not be until the 1990s, that Dr. Isamu Akasaki, Dr. Hiroshi Amano and Dr. Shuji Nakamura invented the first blue LED, making a possibility to achieve an efficient white LED. In fact, this breakthrough research earned them the Nobel Prize in Physics in 2014 [1.10]. Following this achievement, white LEDs started to look promising in early 2000s to replace inefficient light sources, but they were still too expensive. In that sense, Fig. 1.1 shows the expectations for the lighting market until 2022. As can be seen LEDs are supposed to replace incandescent light and even start to replace Compact Fluorescent Lights (CFL) by that date. The reasons for the LEDs coming strongly into the lighting market can be found in their advantages over conventional lighting solutions: energy efficient, controllable in both light and color, long lifetime, lack of a warm-up period and high power density [1.13]. Some of these advantages will make LED light sources to be more than just a lightbulb, being able to

transmit data [1.14], [1.15], control light color, hue and intensity or even detect people in indoor environments [1.16] [1.17]. Nevertheless, these advantages attributed to LED

Table 1.1. Typical efficacies, lifetimes and color quality of lamps [1.7].

	Efficacy [lm/W]	Lifetime[h]	CRI [%]
Maximum ratings for an ideal white light	250 - 350 [1.11]	∞	100
Incandescent	10 - 19	750 - 2500	97
Standard fluorescent			
Fluorescent – T5	25 - 55	6000 - 7500	52 - 75
Fluorescent – T8	35 - 87	7500 - 20000	52 - 90
Fluorescent – T12	35 - 92	7500 - 20000	50 - 92
Compact Fluorescent	40 - 70	10000	82
High-intensity discharge			
Mercury vapor	25 - 50	29000	15 – 50
Metal halide	50 -115	3000 - 20000	65 – 70
High-pressure sodium	50 - 124	29000	22
Halogen	14 - 20	2000 - 3500	99
LED	20 - 100↑	15000 - 50000	33 - 97

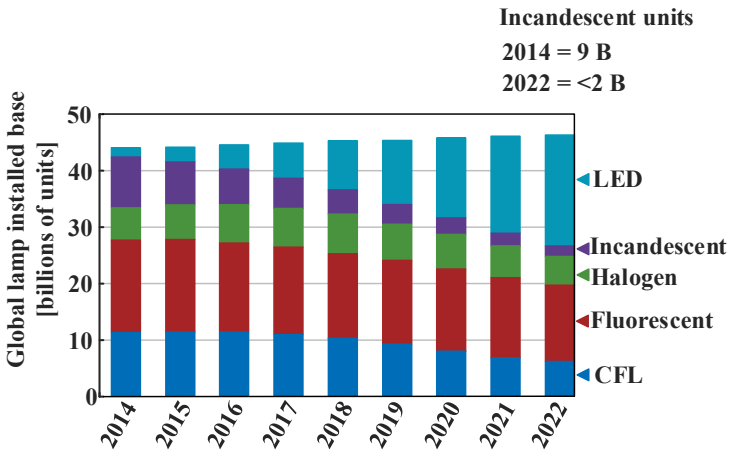


Fig. 1.1. Expectations of global installed base of lamps in terms of light-source technology [1.12].

capabilities are, in reality, achieved by the LED driver, which can be defined as the power supply that controls and ensures an adequate light output of the LEDs.

1.2.1 Working principle

LEDs generate light based on the electrolumiscence phenomenon that occurs when an electric field is applied to a direct semiconductor. Specifically, when the sufficient forward voltage is applied to the P-N junction that comprises the basic structure of an LED, the electrons start migrating from the N to the P region. Some of the free electrons (i.e., free carriers) will have enough energy to travel from the conduction band to the valence band, see Fig. 1.2. It is at this point, when an electron recombines with a hole dropping the excess of energy as it orbits into a lower energy state, that a photon is liberated in the process [1.18], [1.19]. However, this process does not have an ideal efficiency, and thus the rest of the energy is lost in terms of heat. This efficiency is measured in terms of the internal quantum efficiency, which can be defined as the ratio between the number of emitted photons and the number of free carriers passing through the junction [1.20]. In fact, this increase in heat in the P-N junction causes the luminous efficacy of the LED to lower, which implies that a correct thermal management is required [1.21].

From the PN structure, it can be concluded that the working principle of an LED is similar to a diode. However, Silicon (Si) diodes, being a direct semiconductor, do not emit visible light, because in the recombination process the momentum difference between electrons and holes generates phonons instead of photons. In the case of LEDs, indirect materials must be used, in which the momentum during the recombination between electrons and holes is the same, generating photons at a determined wavelength and frequency depending on the energy lost in the recombination [1.22]. Hence, in order

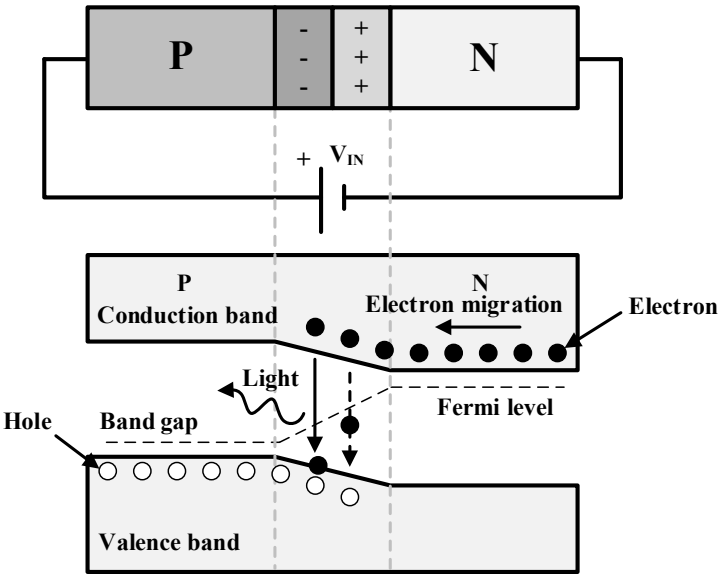


Fig. 1.2. Band diagram of an LED when applying a voltage to the P-N junction.

to generate the adequate wavelength, normally blue, to achieve a white LED, the knee-voltage is required to be much higher (i.e. 2 or 3V) than in a normal diode. The implementation of these LEDs is normally performed with an InGaN blue die coated with a mix of phosphors [1.23].

In summary, the main electrical particularity of an LED is that significant current is only able to go across it in one direction, as any other diode. Hence, the LED can be considered as a non-linear load that follows a V-I curve, as depicted in Fig. 1.3 for three different commercial LEDs. As can be seen, the curves are extremely similar to each other, and emphasis should be put at the higher knee-voltages (i.e., $V_{\gamma 1}$, $V_{\gamma 2}$ and $V_{\gamma 3}$) when compared with commonly used Schottky diodes [1.2]. After reaching this value, the current rapidly increases causing the luminous flux to fluctuate accordingly, following an almost linear relationship, as shown in Fig. 1.4 [1.24], [1.25]. The aforementioned reasons imply that an LED load should be controlled in terms of its forward current instead of its forward voltage. Therefore, the luminous intensity of the light can be controlled online to be adequate to the requirements of the user, the online variation of this parameter in terms of a reference is referred in literature as dimming [1.18].

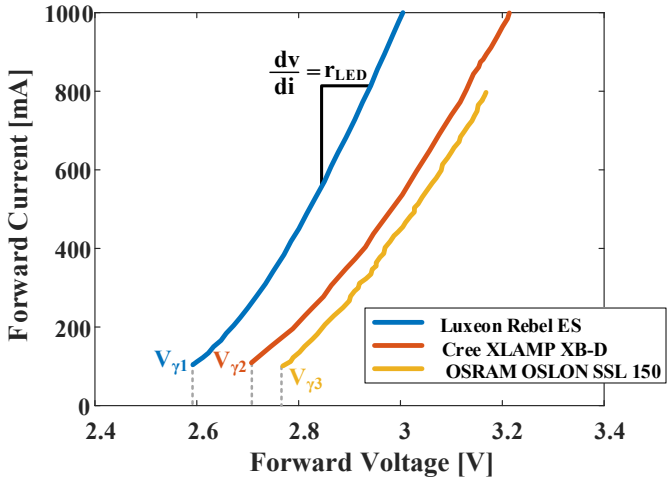


Fig. 1.3. V-I diagram for some commercial LED from the biggest manufacturers: Lumiled [1.26], Cree [1.27] and OSRAM [1.28].

1.2.2 The light-emitting diode as an electric load

The concept introduced in the previous paragraph helps to present the LED as an electric load, which can be defined as a connected group of LEDs either arranged in parallel, series or a combination of both, in order to achieve a determined output power or lumens required for the design. Hence, conforming an LED matrix, as the one depicted in Fig. 1.5. (a), where m LED strings comprised of n LEDs each are connected in parallel. In order to be able to simply analyze a complex matrix LED load, and following the behaviour introduced in Fig. 1.3, the LED load can be approximated by the circuit depicted in Fig. 1.5. (b), where r_{LED} represents the dynamic resistance of the LED, which is the slope of curve as stated in Fig. 1.3, and V_{γ_LED} represents the knee-voltage of the LED. The intrinsic constant voltage load behaviour of an LED is what makes it suitable to be driven by a current source, as its voltage will be closely fixed to nV_{γ_LED} [1.29].

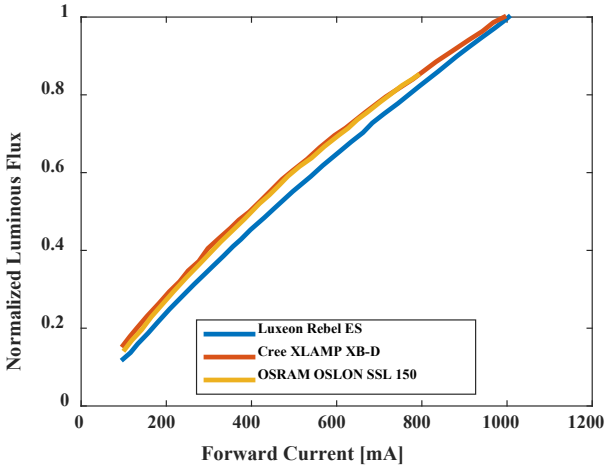


Fig. 1.4. Normalized luminous flux for some commercial LED from the biggest manufacturers: Lumiled [1.26], Cree [1.27] and OSRAM [1.28].

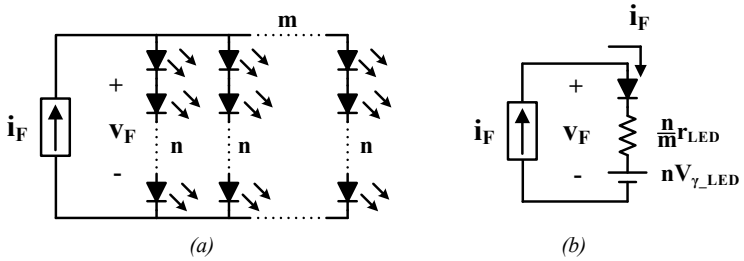


Fig. 1.5. (a) LED matrix comprised of m LED strings that are conformed of n LEDs each. (b) Equivalent circuit of the LED matrix.

As has been mentioned, an LED load can be formed into either a single-string or multi-string configuration. The case of a single-string is the easiest in terms of current balancing, but the problem with this configuration lies in case of failure of one or more LEDs in open circuit, which will render the whole LED load useless. Even though this problem is not present in the preferred multi-string configuration, from the tolerance variation of V_{γ_LED} and r_{LED} comes the inability to guarantee that each LED string shares the same current, which leads to undesired effects, such as, differences in their light output intensity or their temperature, thus causing difference in their lifetime [1.30], [1.31].

1.2.2.1 Current sharing

In order to solve the aforementioned issue, several current sharing methodologies can be found in literature, which can then be divided into two categories: passive and active. The passive methods are based on including passive components to the LED load, such as, capacitors, inductors and resistors [1.31]-[1.39]. In fact, the easiest way to ensure passive current sharing is based on adding a resistor in series with each string (R_{EXT}), as show in Fig. 1.6. (a). This method is simple and cheap, but it is inefficient as the voltage drop on R_{EXT} causes both power losses and the temperature to increase on the LEDs, which is undesired as the luminous efficacy of the LEDs decreases with temperature

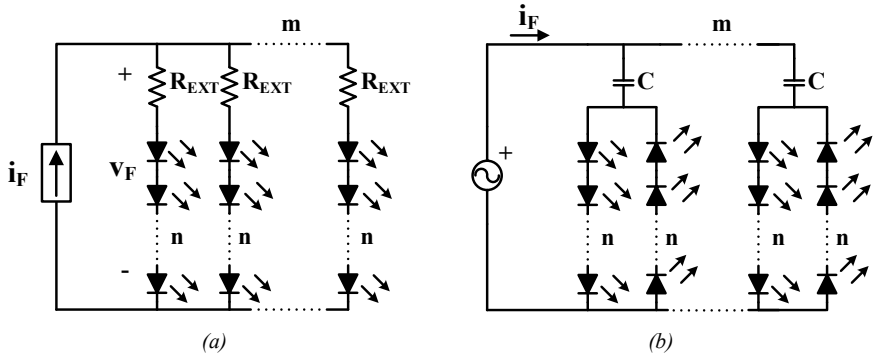


Fig. 1.6. (a) Passive current sharing from a dc source based on series resistors. (b) Passive current sharing from an ac source based on capacitors.

[1.29]. Another way to achieve passive current sharing is depicted for an ac source in Fig. 1.6. (b), which was a widely used method in cold cathode fluorescent lamps [1.32]. The idea is based on using the capacitor in series with each string to achieve similar impedance on each branch. Thus, accomplishing ideal current sharing even under different values of r_{LED} at the cost of increasing the amount of LEDs used.

Active current sharing methods are based in controlling the current through each LED string by means of a current regulator depending on the value of a current reference, i_{ref}, see Fig. 1.7. Particularly, depending on the implementation of the current regulator, two types of active current sharing methods can be differentiated: linear based and Switching Mode Power Supply (SMPS) based. On the one hand, the linear based solution can be illustrated by means of a transistor typically working as a current sink [1.40], [1.41], see Fig. 1.7. (a). This solution, preferred over the series resistors due to the control over the current, still suffers from poor efficiency due to the power losses on the transistor.

On the other hand, the SMPS based solution is normally implemented with a non-isolated dc-dc converter per string that controls the current level across the LED string [1.42]-[1.44], for example a buck converter with a current feedback loop as depicted in Fig. 1.7. (b). This solution is the most efficient, but at the same time is both the most expensive and complex. Therefore, its use is recommended for high-end applications.

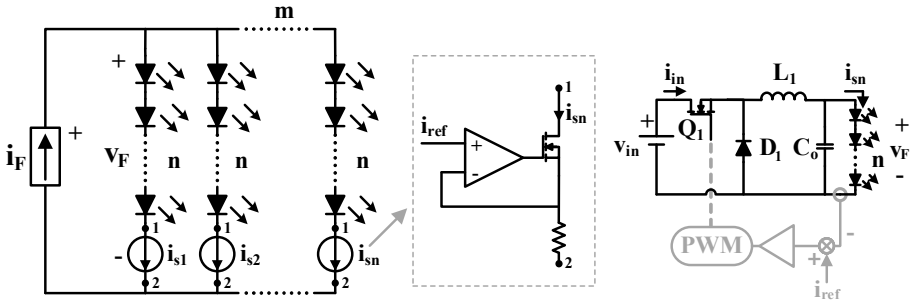


Fig. 1.7. Active current sharing. (a) Linear based current source. (b) Switching-mode power supply current source.

1.2.3 Dimming techniques

The light controllability of LEDs in terms of its forward current is an interesting characteristic that can be leveraged to adjust the luminous flux online in a certain environment, according to the user requirements. In the previous subsection, the concept of active current sharing has been introduced, in which, the current across an LED string is regulated in accordance to a determined current reference, i_{ref}. Therefore, the variation of this reference will cause the luminous flux to change accordingly.

The current literature records two different dimming techniques: analog and Pulse Width Modulation (PWM) dimming. The first is based on supplying the LEDs with a dc current that will determine their luminous flux [1.45]. This implies that the average current across the LEDs varies as the current across them increases or decreases. As a consequence, the Correlated Color Temperature (CCT), which is a measure of light color appearance, will show some degree of variation [1.46], being this its main drawback. To correctly exemplify the previous statements, Fig. 1.8. (a), shows the scheme that the analog dimming follows. As can be seen, the emitted visible light is equal to the perceived light, (i.e., $\phi(t)$) being both of them a function of the forward current present on the LEDs (i.e., $\phi(t)=f(i_F(t))$).

As regards the second dimming method, see Fig. 1.8 (b), the CCT variation is not an issue as the forward current during the operation of the LED is always at the same level, I_{Fp} [1.47]. In order to vary the luminous flux, the PWM current is used, increasing or decreasing its duty cycle [1.48]. This control is possible due to the LEDs fast dynamic response, so their light output will follow the same PWM modulation as the current across them. Nonetheless, the bandwidth of the LEDs should be considered before selecting the switching frequency of the signal. In addition, the frequency of the PWM signal has to be selected carefully as the human eye is extremely sensitive to low frequency signals which can potentially cause harmful effects [1.49]. In that sense, a frequency above 3 kHz is considered to be completely safe for humans, as the human eye is not able to perceive the higher frequency ac component. Therefore, the perceived light can be considered as a function of the average forward current (i.e., $\phi(t)=f(avg(i_F(t)))$ [1.30].

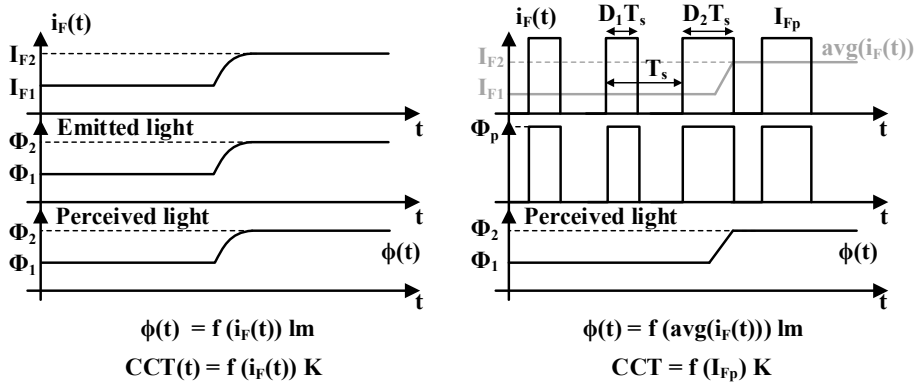


Fig. 1.8. (a) Analog dimming and (b) PWM dimming schemes for obtaining the same amount of perceived light.

1.3 LED drivers regulations

The main application for LEDs is to replace inefficient lighting technologies in residential and commercial environments, which normally have primary access to the ac power grid. Considering the inherent behaviour of the LED as a diode, only letting the current to go across it in one direction, it is necessary to use an ac-dc converter to ensure that the LEDs are driven with an adequate dc current. The reason behind requiring this power conversion comes from the fast current-light response from the LEDs, which could replicate the sinusoidal current from the grid at double the mains frequency causing an undesirable visible flicker to occur.

The regulations that an LED driver needs to comply with are to be understood before discussing which solutions are the most appropriate for each application. This section focuses on the specific regulations and recommendations for an LED driver, as are the ENERGY STAR® program requirements product specification for luminaries, harmonic standard (i.e. IEC 61000-3-2) and the flicker regulation (i.e. IEEE Std. 1789-2015).

1.3.1 Energy Star® Program Requirements Product Specification for Luminaires

The ENERGY STAR® is a US Environmental Protection Agency voluntary program that helps businesses and individuals save money and protect our climate through superior energy efficiency [1.51]. The international standard has been adopted in Australia, Canada, Japan, New Zealand, Taiwan and the European Union, setting specifications for a large list of consumer products. Within this list, the requirements for LED lighting products are enumerated, including the LED load and the ac-dc LED driver. However, the regulation differentiates between two kinds of LED load: LED lamps and LED lighting fixtures (i.e., LED luminaires), and excludes a series of products, such as, solid state retrofits, high bay fixtures, outdoor street and area lighting and party or entertainment lighting [1.52]. Nonetheless, it still covers a wide spectrum of LED lighting products both in residential and commercial environments.

Of the aforementioned requirements, the first one is directed to lamps intended to replace incandescent light bulbs [1.53], whereas the second is intended for most lighting products intended for direct connection to the power grid with an input power below 250 W [1.54]. Specifically, Table 1.2 lists the requirements that the ac-dc LED driver needs to meet in order to comply with ENERGY STAR®. From this list, it should be noted that the most restrictive constraints are the rated life and the Power Factor (PF). The first, because it requires the ac-dc LED driver to last longer than 10,000 h, which is the rated lifetime of the most restrictive component frequently used in low cost ac-dc LED drivers, the electrolytic capacitor [1.55]. The second, since its compliance drastically reduces the possible topologies that can be used for its design, as an almost sinusoidal current waveform in phase with the voltage needs to be guaranteed at the input of the LED driver.

1.3.1.1 Power Factor and Total Harmonic Distortion

In fact, PF defines the ratio of the total input power in watts to the total apparent power in volt-amperes on the ac side of the converter [1.56], and it can be considered as a measure of how well voltage and current are aligned in an ac system and of how efficiently is the power extracted from the ac power grid. Mathematically, it can be expressed as,

$$PF=\frac{\sum \text{Watts per Phase}}{\sum \text{RMS Volt-amperes}}=\frac{\text{Active Power}}{\text{Apparent Power}}. \quad (1.1)$$

Another useful concept that needs to be introduced to define the quality of a sinusoidal waveform input waveform, is the one of Total Harmonic Distortion (THD). THD is defined as the ratio, expressed as a percent, of the rms value of the ac signal after the fundamental component is removed and inter-harmonic components are ignored, to the rms value of the fundamental [1.56]. The formula defining THD is provided below,

Table 1.2. LED driver requirements, in accordance to ENERGY STAR® [1.54].

Rated Lifetime	The LED package(s) / LED module(s) / LED array(s), including those incorporated into LED light engines or retrofit kits, shall meet the following L_{70} lumen maintenance life values: • $L_{70} \geq 25{,}000$ hours for indoor. • $L_{70} \geq 35{,}000$ hours for outdoor. • $L_{70} \geq 50{,}000$ hours for inseparable luminaires. Note: L_{70} defines the elapsed operating time over which the LED light source will maintain a 70% of its initial light output.
Source Start Time	Light source shall remain continuously illuminated within 1 second of application of electrical power.
Power Factor	Total luminaire input power ≤ 5 watts: PF ≥ 0.5. Total luminaire input power > 5 watts: PF ≥ 0.7.
Standby Power Consumption	Luminaires shall not draw power in the off state.
Operating Frequency	Lamp light output shall have a frequency ≥ 120Hz.
Transient Protection	Ballast or driver shall comply with ANSI/IEEE C62.41.1-2002 and ANSI/IEEE C62.41.2-2002, Category A operation. The line transient shall consist of seven strikes of a 100 kHz ring wave, 2.5 kV level, for both common mode and differential mode.
Dimming Performance	The luminaire and its components shall provide continuous dimming from 100% to 20% of light output. Note: This only applies for certified dimmable luminaires.
Audible noise	Luminaire shall not emit noise above 24 dBA at 1 meter or less at the minimum output.

$$THD = \frac{\sqrt{\sum_{k=2}^{n} i_{rms,k}^2}}{i_{rms,1}} \cdot 100\%, \quad (1.2)$$

where $i_{rms,k}$ is the rms value of the k^{th} harmonic of the current and $i_{rms,1}$ is the rms value of the fundamental harmonic of the current.

1.3.2 Harmonic injection standard, IEC 61000-3-2

Over the last few decades, the rise of non-linear loads connected to the grid has caused the amount of low frequency harmonics to increase. This increase is principally caused by the usage of inadequate ac-dc converters that demand non sinusoidal currents with a poor PF. In fact, a diode bridge followed by an electrolytic capacitor is commonly used in low cost applications causing the current to be demanded as short duration current peaks. If this were the norm, it would cause the grid to suffer from different effects, such as, voltage drops, overheating of both, transformers and power generators, or oscillations in electrical machines diminishing their lifetime [1.57]. In order not to cause the quality of the grid to decrease, the International Electrotechnical Commision (IEC) released several regulations to limit the low frequency harmonic injection from electronic equipment to the grid. For the scope of this dissertation, the IEC 61000-3-2 regulation, which limits the harmonic injection in equipment that draws input currents of ≤ 16 A per phase, is going to be considered as an indispensable requirement in the design of ac-dc LED drivers.

The latest version of this regulation dates of November, 2014, and it is a European Union standard (i.e., EN 61000-3-2:2014), which was approved by the European

Table 1.3. Equipment classification, in accordance to IEC 61000-3-2 [1.58].

Class A	• Balanced three-phase equipment. • Household appliances, excluding equipment identified by Class D. • Tools excluding portable tools. • Dimmers for incandescent lamps. • Audio equipment. • Everything else that is not classified as B, C or D.
Class B	• Portable tools. • Arc welding equipment which is not professional equipment.
Class C	• Lighting equipment.
Class D	• Personal computers and personal computer monitors. • Television receivers. Note: Equipment must have power level 75W up to and not exceeding 600W.

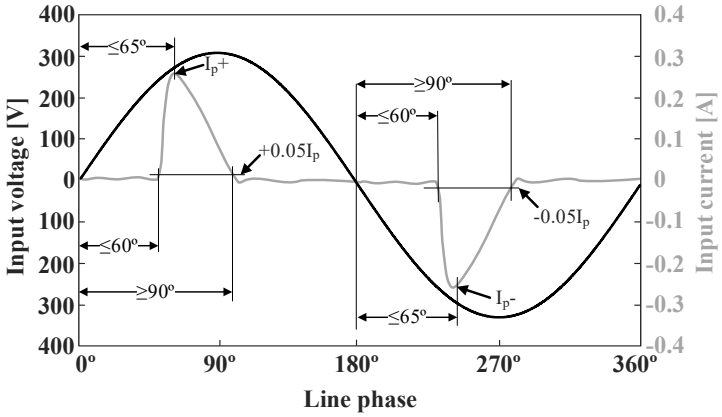
committee for electrotechnical standardization (CENELEC). The regulation details how the low frequency harmonics of the input current (i.e., the first 40 from the fundamental frequency) need to be limited and measured depending on the classification summarized in Table 1.3. According to this, lighting equipment falls under the Class C category for single phase ac power grids. However, the regulation is not clear at stating under which category falls a balanced three-phase equipment for lighting applications as it falls in both Class A and Class C. Consequently, this specific equipment will be considered as Class C due to its more restrictive nature over Class A.

Furthermore, Class C differentiates two scenarios depending on the active input power of the lighting equipment. If the power exceeds 25 W (i.e., luminaires), then the harmonic content of the input current needs to be limited to the values stated in column 4 of Table 1.4 (i.e., Class C limits). However, if that is not the case and the active input power is below or equal to 25 W (i.e., lamps), then the input current needs to either have its harmonic components limited by those of column 5 of Table 1.4. (i.e., Class D limits), or fulfil that the third and the fifth harmonic component of the current shall not exceed 86% and 61% of the fundamental current, respectively. In the latter, these conditions need to be achieved while fulfilling that the input current reaches 5% of its crest value at 60º or before, that its crest is reached at 65º or before, and that its value does not fall below 5% of its crest value before reaching 90º, referred to any zero cross of the input voltage, as can be seen in Fig. 1.9.

Taking into account the preceding requisites, it can be concluded that the regulation is laxer for lighting equipment below 25 W. In that sense, this broadens the study of

Table 1.4. Harmonic limit content, in accordance to IEC 61000-3-2 [1.58].

Harmonic [n]	Class A [A]	Class B [A]	Class C [% of fund.]	Class D [mA/W]
Odd harmonics				
3	2.30	3.45	$30F_p$	3.4
5	1.14	1.71	10	1.9
7	0.77	1.155	7	1.0
9	0.40	0.60	5	0.5
11	0.33	0.495	3	0.35
13	0.21	0.315	3	3.85/13
$15 \le n \le 39$	$0.15\frac{15}{n}$	$0.225\frac{15}{n}$	3	$\frac{3.85}{n}$
Even harmonics				
2	1.08	1.62	2	-
4	0.43	0.645	-	-
6	0.30	0.45	-	-
$8 \le n \le 40$	$0.23\frac{8}{n}$	$0.345\frac{8}{n}$	-	-



Note: I_p represents the higher value of I_p+ or I_p-.

Fig. 1.9. Illustration of the relative phase angle and current parameters [1.58].

topologies that can distort the input current to a certain extent while still achieving a low cost solution. However, this is not the case for equipment exceeding 25 W, as Class C limits are considered to be the most restrictive of the four. This implies that the current shape needs to be sinusoidal and aligned with that of the input voltage, which normally means achieving unity PF. This characteristic limits ac-dc LED drivers of more than 25 W to those topologies that can achieve Power Factor Correction (PFC), as will be seen in Section 1.4 of this chapter, and understanding PFC as the ability of demanding a sinusoidal current in phase with the input voltage, thus achieving unity PF.

1.3.3 Flicker regulation, IEEE Std. 1789-2015

The flicker phenomenon can be defined in terms of any lighting equipment as a rapid repetitive change in luminance [1.59]. Particularly, in the case of LEDs, it occurs due to the fast response to current variations. Precisely, the harmonic content of the current flowing across the LEDs translates into a light output modulated by those components. However, not all frequency components are equally harmful for humans, and only those below 3 kHz can be considered as such. In fact, whether the low frequency modulation is visible or invisible, it can trigger headaches, migraines, fatigue, epilepsy or any other neurological response [1.60].

Reducing flicker harmful effects has become increasingly important for ac-dc LED drivers, since conceptually double the mains frequency can easily appear at the current across the LEDs. For instance, without a proper regulation, the output capacitor of the ac-dc LED driver that decouples the ac component of the current across the LEDs and thus controls the admissible ripple of the current, can be overestimated causing the life expectancy of the ac-dc LED driver to decrease. In that sense, two parameters were defined in order to give a measure of flicker [1.60]:

- Flicker index [1.61] is defined as the area above the line of average luminance (i.e., L_{dc}) divided by the total area of the light output curve during a cycle, refer to Fig. 1.10,

$$\text{Flicker Index}=\frac{\text{Area}_1}{\text{Area}_1+\text{Area}_2}. \quad (1.3)$$

- Percent flicker [1.61], also known as Modulation (%), which is the preferred expression, can be defined as,

$$\text{Mod. (\%)}=\frac{L_{max}-L_{min}}{L_{max}+L_{min}}\cdot 100, \quad (1.4)$$

where L_{max} and L_{min} define the maximum and minimum luminance that the LEDs are producing, respectively.

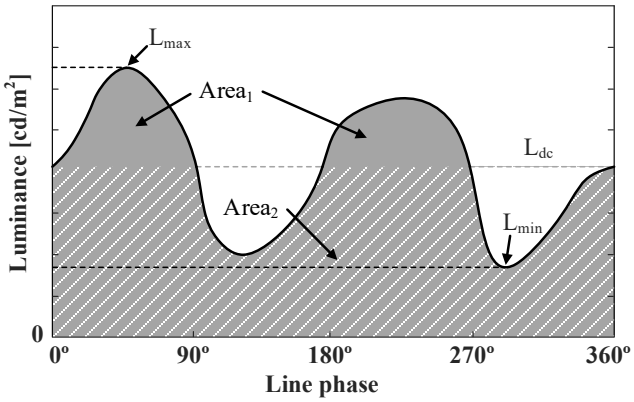


Fig. 1.10. Illustration of the luminance over the line phase to exemplify the estimation of flicker index and Mod. (%).

The issue with the aforementioned definitions is their independence from the frequency of the signal. In the last decade, efforts toward a set of recommendations have been made due to the lack of association between flicker and frequency in previous literature. As a matter of fact, the requirements in terms of flicker should not be the same for frequencies below 90 Hz than for those that are higher, since our eyes are more sensitive to those lower frequencies [1.49].

Nowadays, there is still no such thing as a flicker regulation, but a set of recommendation practices defined by the IEEE standard 1789-2015 in 2015 [1.62]. These practices are summarized in Table 1.5. Consequently, the aim of this dissertation is to follow particularly Practice 1 to design ac-dc LED drivers, which is restrictive enough to limit the adverse biological effects caused by flicker in detriment of the most restrictive, as is Practice 2, which guarantees No Observable Effect Level (NOEL). The recommendation of Practice 1 is depicted in Fig. 1.11, where the area below the curve is the recommended operating area where the Mod. (%) calculated from the measured luminance of the lighting equipment should be.

It should be noted that the light output of any lighting equipment connected to an ac power grid can contain several harmonics related to the fundamental frequency of the grid (i.e., 50 Hz for Europe and 60 Hz for the US), or even subharmonics below those frequencies due to failures either in the driver or the grid, which can be potentially hazardous. In those cases, the recommendation is clear, stating that all the harmonic components of the measured luminance over a line cycle should lie within the shaded area

Table 1.5. Recommended practices, in accordance to IEEE Std. 1789-2015 [1.62].

Practice 1	If it is desired to limit the possible adverse biological effects of flicker, then flicker Mod. (%) should satisfy the following goals: • Below 90 Hz, Mod. (%) is less than 0.025×frequency. • Between 90 Hz and 1250 Hz, Mod. (%) is below 0.08×frequency. • Above 1250 Hz, there is no restriction on Mod. (%).
Practice 2	If it is desired to operate within the recommended NOEL of flicker, then flicker Mod. (%) should be reduced by 2.5 times below the limited biological effect level given in Recommended Practice 1: • Below 90 Hz, Mod. (%) is less than 0.01×frequency. • Between 90 Hz and 3000 Hz, Mod. (%) is below 0.0333×frequency. • Above 3000 Hz, there is no restriction on Mod. (%).
Practice 3	For any lighting source, under all operating scenarios, flicker Mod. (%) shall satisfy the following goal: • Below 90 Hz, Mod. (%) is less than 5%.

of Fig. 1.11 [1.62]. In fact, considering the luminance is a periodic and real signal, it can be defined by a Fourier series truncated at the maximum frequency (i.e. 1250 Hz, as defined by Practice 1) [1.63], as follow,

$$l(t)=\frac{L_{dc}}{2}+\sum_{k=1}^{K}|a(k)|\sin\left(2\pi k f_0 t+\angle a(k)\right), \tag{1.5}$$

where f_0 defines the fundamental frequency of the luminance, K is an integer whose value is based on the maximum frequency defined by Practice 1 and a(k) are the coefficients of the Fourier series, which are defined by,

$$a(k)=\frac{1}{T_0}\int_0^{T_0} l(t)e^{-j2\pi k f_0 t}dt, \tag{1.6}$$

where T_0 is the fundamental period of the luminance.

After determining the Fourier series coefficients of the luminance, it becomes immediate to obtain each of the harmonics,

$$l_H(t,k)=|a(k)|\sin\left(2\pi k f_0 t+\angle a(k)\right). \tag{1.7}$$

Hence, being able to determine the Mod. (%) for each of the harmonics of the luminance as,

$$\text{Mod.}(\%)(k)=\frac{L_{H,max}(k)-L_{H,min}(k)}{L_{H,max}(k)+L_{H,min}(k)+L_{dc}}\cdot 100, \quad (1.8)$$

where $L_{H,max}(k)$ and $L_{H,min}(k)$ define the maximum and minimum value of harmonic k. Thus, all Mod. (%) components defined by (1.8) for all harmonics of the luminance should fall in the recommended area of Fig. 1.11.

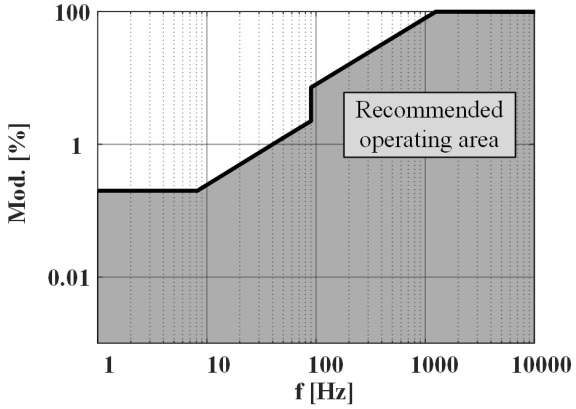


Fig. 1.11. Recommended Practice 1 operating area [1.62].

1.4 LED drivers, state of the art

As has been previously stated, LEDs are increasingly becoming our main source of artificial light in our homes, offices or streets due to their reliability, long life, luminous efficiency and low maintenance requirements. For that matter, it is crucial for the elements surrounding the LED load for its driving not to limit their benefits.

Their intrinsic diode behaviour bases their driving on controlling the dc forward current, as has been mentioned in Section 1.2. This requirement has made the driving of LEDs from the mains an important research topic in a wide range of power [1.30]. Therefore, according to previous literature, an ac-dc LED driver needs to be efficient, compact, operate in universal voltage range, comply with the regulations described in Section 1.3, dispose of the most limiting element in terms of the driver lifespan, which is the electrolytic capacitor, and control the current across the LED load in order to achieve dimming and an adequate light output. In that sense, Fig. 1.12 shows at a glance, a classification of ac-dc LED drivers for both single-phase and three-phase ac power grids in terms of the number of power conversion stages used. The different solutions will be further detailed along this section considering the latest trends with a special focus on the aforementioned requirements that an ac-dc LED driver should have.

1.4.1 Single-phase ac-dc LED drivers

In Section 1.1, it was emphasized the importance of replacing the old and inefficient light in homes, streets or offices for newer and better technologies as are LEDs. Considering that the primary access in homes, streets and offices is single-phase ac, it is required the use of an ac-dc converter in order to drive the LED load (i.e., ac-dc LED driver), to guarantee a flicker free performance. However, several distinctions can be

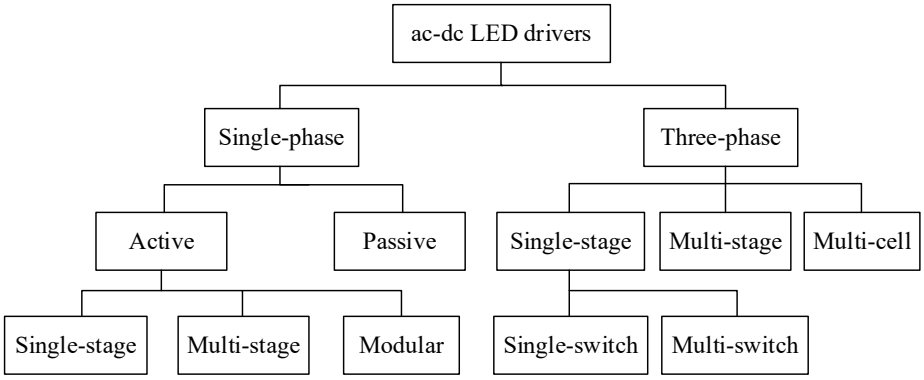


Fig. 1.12. Classification of ac-dc LED drivers for both single-phase and three-phase ac power grids.

made depending on the application. In fact, the regulations (i.e., ENERGY STAR® and IEC 61000-3-2) differentiate between two rules in function of the input power of the LED load. The laxer regulation set for lamps (i.e., < 25 W) makes possible the usage of simple, and inexpensive passive solutions, whereas luminaires (i.e., > 25 W) need to comply with the most restrictive set of rules, requiring the use of a PFC solution.

1.4.1.1 Passive

The passive solutions, normally applied to retrofit/replacement lamps of less than 25 W, require the least components of all the solutions that are going to be discussed along this section. In this case, the input current of the driver is not required to be sinusoidal in accordance to Class D regulation, allowing some degree of distortion to happen in the input current. In contrast, some benefits are traded-off:

- the ability to control the current, unless a trimmer that will further distort the current is used [1.64].
- the lower lifespan of the lamp, due to the inability to remove the electrolytic capacitor.
- the efficiency, due to the resistive elements introduced to limit the peak current.

The conventional passive solution, depicted in Fig. 1.13 (a) and (b), is based on using a capacitor-input filter to generate a dc voltage in order to feed the LED load at either high voltage [1.65] or low voltage [1.66]. The current across the LED load is not controllable and resistor R_B needs to be included to limit the peak current. The inclusion of this resistive element hinders the efficiency of the solution. Another possibility to passively drive LEDs is depicted in Fig. 1.13 (c); this solution is based on using the LED load to rectify the input voltage, thus using a string for the positive half line cycle and the other one for the negative half line cycle. This technique is referred in literature as Low Frequency (LF) AC-LED driving [1.67]-[1.72], and presents two important drawbacks: the first is the low frequency flicker due to the driving of the LEDs with a sinusoidal current, and the second is that the amount of LEDs used is duplicated when compared to the capacitor-input filter solution. In contrast, the lifetime of the driver is prolonged as the electrolytic capacitor is not required, and the ac driving does not have an impact on

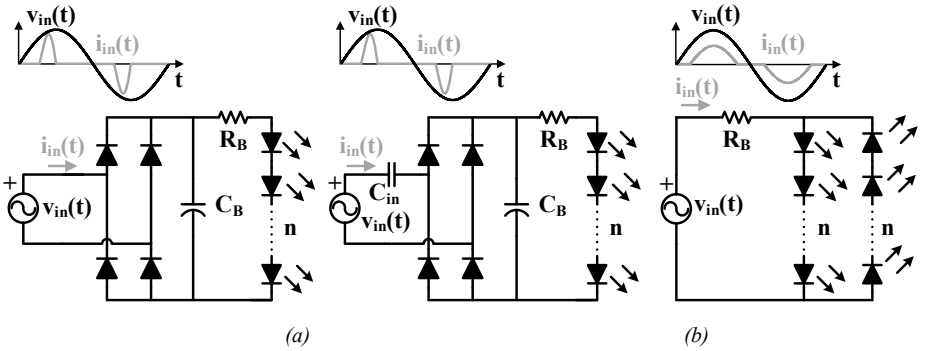


Fig. 1.14. Typical passive solutions to drive LEDs from ac single-phase power grids. (a) Capacitor-input filter. (b) Voltage step-down capacitor-input filter. (c) AC-LED driver.

the lifespan of the LEDs in accordance to [1.73]. It should be noted that there have been some proposals to reduce the amount of LEDs used in this solution, however the number is always greater than the conventional solution [1.70]. Furthermore, the limiting resistance is still required. However, it can be replaced by a capacitor to passively balance several LED strings, as it was previously introduced in Fig. 1.6 (b) solution, or even inductors in series with the string [1.33]. The latter, would increases the size of the ac-dc LED driver significantly due to the low frequency inductors required, and its use is mainly recommended for high frequency AC-LED driving.

In order to solve some of the aforementioned problems, some authors have proposed using a valley-fill circuit in conjunction with an output inductance [1.74]-[1.76]. This configuration reduces the harmonic content of the input current and eliminates the electrolytic capacitor, thus improving the lifespan of the ac-dc LED driver, see Fig. 1.14. (a). In contrast, other authors included complex input filters to improve the THD and PF improving the scope of the passive solutions to not only drive low power luminaires, but not eliminating the bulk capacitor, see Fig. 1.14. (b) [1.77]. However, the trade-off that comes with this kind of solutions is the increased cost due to the amount of components and the inclusion of low frequency bulky inductors that will increase the size and weight.

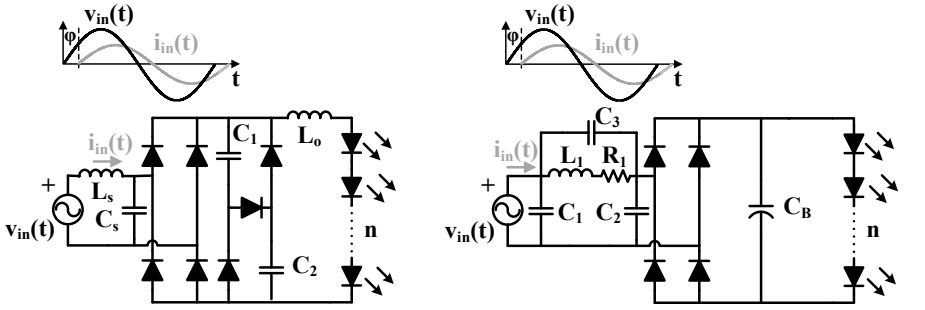


Fig. 1.13. State of the art passive solutions to drive LEDs from ac single-phase power grids. (a) Valley-fill circuit based [1.74]. (b) Filter based [1.76].

1.4.1.2 Active

Active single-phase ac-dc solutions are defined by one or various active components that are controlled in order to shape the input current while keeping a dc output voltage/current. The analysis carried out in this dissertation is centered on SMPS considering that linear regulators are extremely inefficient for this purpose.

One way to classify active ac-dc LED drivers, following Fig. 1.12, depends on the amount of power stages included in the ac-dc LED driver. In that sense, an ac-dc LED driver comprised by a single power stage, whereas a driver with two or more cascaded power stages will fall into the multi-stage category. Those ac-dc LED drivers that fall in between, based on the integration of two stages or in the addition of a power stage that does not process all the power, will be classified as single-stage, and normally referred as quasi-single-stages. In this classification an extra category is added in order to include those drivers comprised of more than one SMPS connected in either of the modular connection configurations: Input Series Output Parallel (ISOP), Input Parallel Output Series (IPOS), Input Series Output Series (ISOS) or Input Parallel Output Parallel (IPOP). Furthermore, within the three prior categories, there are some design conditions that should be distinguished: firstly, the inclusion of galvanic isolation or not, which is a recommended practice to isolate the normally safe voltages withstood by the LED load from the grid; secondly, the input power of the luminaire; and lastly, the removal of the electrolytic capacitor. Accordingly, different solutions can be rendered when conceiving these distinctions.

1.4.1.2.1 Loss Free Resistors basics

Before discussing the different topologies used in ac-dc LED drivers, it is important to define the concept of Loss Free Resistors (LFR). An LFR is a dc-dc converter behaving as a resistor at its input and as a power source at its output by means of control [1.78], [1.79], see Fig. 1.15. The resistive value of the LFR (i.e., R_{LFR}) depends on the control variable, v_c. This is a well-known concept in the ac-dc PFC field, where a sinusoidal current in phase with the input voltage of the converter is desired [1.80].

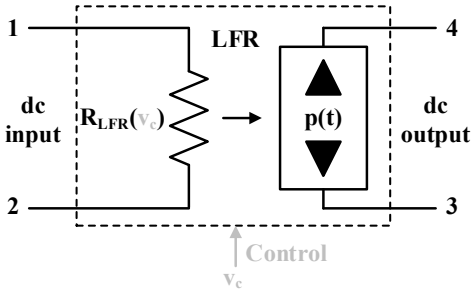


Fig. 1.15. Loss free resistor concept.

In order for a dc-dc converter to be able to operate as an LFR it needs to satisfy two conditions. The first condition is related to the resistance as seen by the LFR, which needs to be defined as,

$$r(\omega t)=\frac{r_{eq}}{2\sin^2(\omega t)}, \tag{1.9}$$

assuming perfect power transfer from input to output of the LFR, and where r_{eq} represents the equivalent resistance of the LED load.

The second condition is related to the dc voltage conversion ratio of the LFR, which is required to be,

$$m(\omega t)=\frac{M}{|\sin(\omega t)|}, \tag{1.10}$$

where M is defined as the ratio between the voltage withstood by the LED load and the peak of the input voltage.

There are several ways in which an LFR performance can be achieved. The most common one is depicted in Fig. 1.16. (a), where a current feedback loop is responsible for shaping the input current in accordance to the input voltage, usually referred as Multiplier Based Control (MBC). This technique is normally used with converters working in Continuous Conduction Mode (CCM) [1.81], [1.82]. Another massively used method for an LFR performance, shown in Fig. 1.16. (b), is achieved by some dc-dc converters that in certain operating conditions intrinsically perform as an LFR, referred as Voltage Follower Control (VFC) [1.83] [1.84]. Furthermore, an LFR performance can almost be achieved by means of a One-Cycle Control (OCC) [1.85], Voltage Controlled Compensation Ramp Control (VCCRC) [1.86] or Nonlinear-Carrier Control (NLCC) [1.87], as long as the current ripple on the main inductance can be considered negligible.

In particular, a boost converter, or any of the converters derived from this topology are able to perform as an ideal LFR in accordance to all three presented strategies. Thus, it is able to achieve it by working in CCM with a MBC, in VFC by operating the boost in Boundary Conduction Mode (BCM) and in OCC, VCCRC or NLCC. In a similar fashion, a buck-boost converter is able to achieve all presented strategies, but its control as a VFC is inherently obtained by operating in Discontinuous Conduction Mode (DCM).

In this section, out of the three conventional dc-dc converters (i.e. buck, boost and buck-boost) the buck was not discussed at all. The reason comes from the intrinsic behaviour of a buck converter which is only able to reduce its input voltage to a lower output voltage. This fact renders the converter unable to demand a sinusoidal current

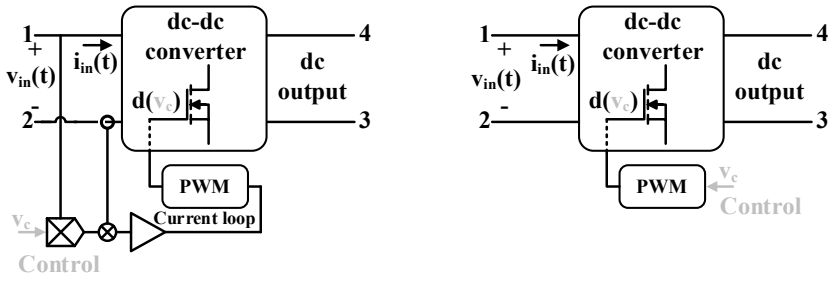


Fig. 1.16. Some LFR implementations. (a) Multiplier Based Control. (b) Voltage Follower Control.

because of the input voltage variation, as there are regions close to the zero crossing in which the buck converter is not able to conduct, thus making it unable to satisfy the condition set by (1.10). Hence, the buck family of converters is only able to demand a sinusoidal current during a certain conduction angle [1.88]. This behaviour hinders their performance as a PFC and is the main reason why they are traditionally neglected for ac-dc LED drivers with a p_{in} higher than 25 W, where unity PF is almost mandatory to comply with the harmonic injection regulation.

1.4.1.2.2 Single-stage solutions

Active single-stage ac-dc solutions are massively used in ac-dc LED drivers due to their low cost and simplicity over the conventional two stage solution. In contrast, some limitations appear on the requirements set at the start of this section: the electrolytic capacitor cannot always be removed, the efficiency tends to be low (i.e., < 90%) and the dc voltage conversion ratio needs to be high. The removal of the electrolytic capacitor is normally performed with a second stage that compensates the low frequency ripple on the output voltage. However, achieving this in a single-stage ac-dc converter is not an easy task and more components are required. In that sense, some authors propose the use of valley-fill circuits [1.89]-[1.91] similarly to what was shown in Fig. 1.14. (a). The proposal is able to remove the electrolytic capacitor at the cost of having an increased amount of passive components and a low efficiency.

Another alternative to remove the electrolytic capacitor, in single-stage ac-dc converters, is distorting the input current. Some authors have proposed the injection of the third, fifth or even seventh harmonics attempting to reduce the heavy pulsation of the input power if a pure sinusoidal current is demanded [1.92]-[1.95]. The analysis shows for ac-dc LED drivers that requirements with ENERGY STAR® can be met in terms of PF, however, ensuring compliance with Class C IEC 61000-3-2 still requires the use of an electrolytic capacitor. Hence, the distortion of the input current is particularly interesting for ac-dc LED drivers dedicated to retrofit LED lamps (i.e., p_{in} < 25 W). This opens a handful of simple active solutions, even if the electrolytic capacitor is not removed considering the cost is the main concern, as are: the use of Active Input Current Shapers (AICS), or buck converter and its multiple variants, normally neglected for PFC.

Several solutions for retrofit LED lamps have been proposed based on using non-isolated buck converters either as a single-stage or quasi-single-stage [1.96]-[1.101], [1.146], see Fig. 1.17. (a), isolated converters from the buck family [1.102], [1.147], using an LFR as the limiting resistor rendering an AICS [1.103], as depicted in Fig. 1.17. (b), or even a more traditional AICS approach based on a quasi-single-stage [1.104], [1.105], see its equivalent circuit in Fig. 1.17 (c). The converters from the buck family show better efficiencies than the ones from the buck-boost family, with the limitation of the conducting angle that is able to comply with the regulation set for LED lamps.

As regards the solution based on using an LFR to limit the current on the LEDs, it should be noted that it is able to achieve a high step-down ration between input and output voltage with a simple approach requiring an isolated converter working as an LFR. This solution slightly distorts the input current demanded rendering an AICS, whose main drawback is its inability to remove the electrolytic capacitor [1.103]. Continuing the analysis with the traditional AICS approach, its operation is based on integrating an AICS with a dc-dc converter. This solution is able to remove the electrolytic capacitor allowing

a certain ripple to appear on the intermediate bus capacitor (i.e., C_B), causing some distortion to appear on the input current. The main drawbacks of this solution are its low efficiency and its narrow input voltage range operation [1.104], [1.105].

That being said, the simplest and most massively used converter in single-stage ac-dc LED drivers for both power ranges, with its multiple variants, is the flyback converter [1.106]. A flyback converter, see Fig. 1.17. (d), is a converter from the buck-boost family

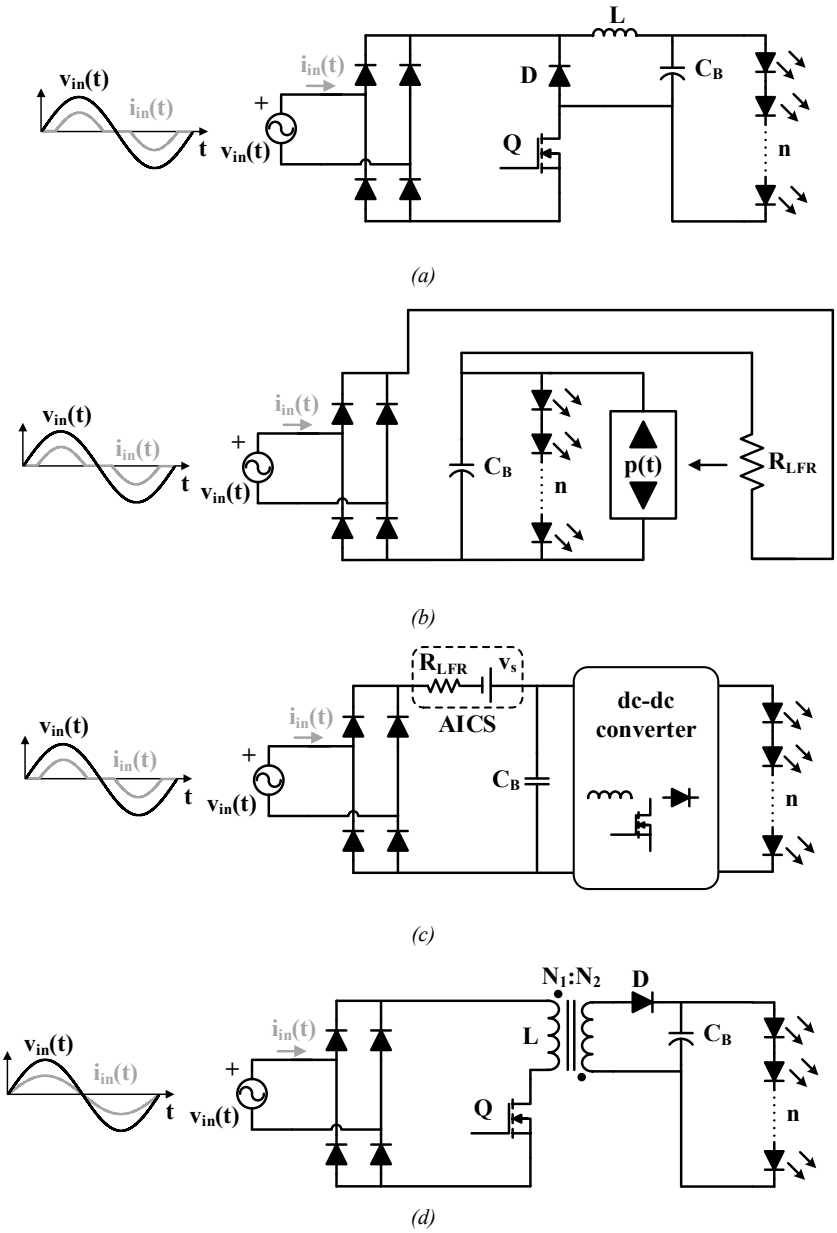


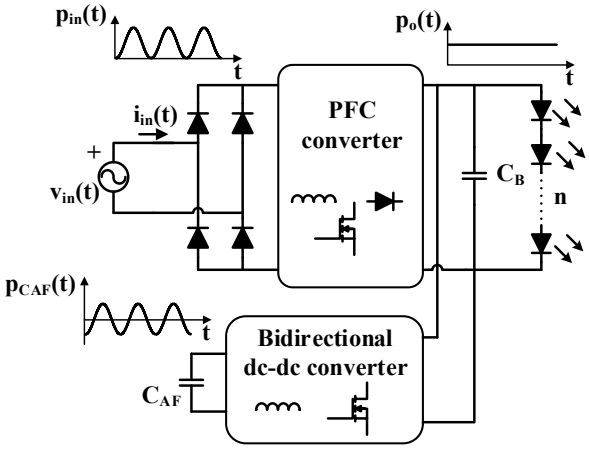
Fig. 1.17. Some examples of LED drivers for retrofit lamps. (a) Buck converter. (b) Equivalent circuit of the LFR based AICS. (c) Equivalent circuit of the traditional quasi-single-stage AICS. (d) Flyback converter.

that includes galvanic isolation thanks to its coupled inductor [1.83]. By being a member of the buck-boost family, it is able to achieve unity PF and PFC naturally by working in DCM, which simplifies its control. In contrast, the converter is unable to remove the electrolytic capacitor, unless any of the forthcoming methods depicted in Fig. 1.18 is used, and it suffers from low efficiencies due to the passive snubber used in low cost solutions to protect the main switch from voltage spikes caused by the leakage inductance of the couple inductor [1.107]-[1.120].

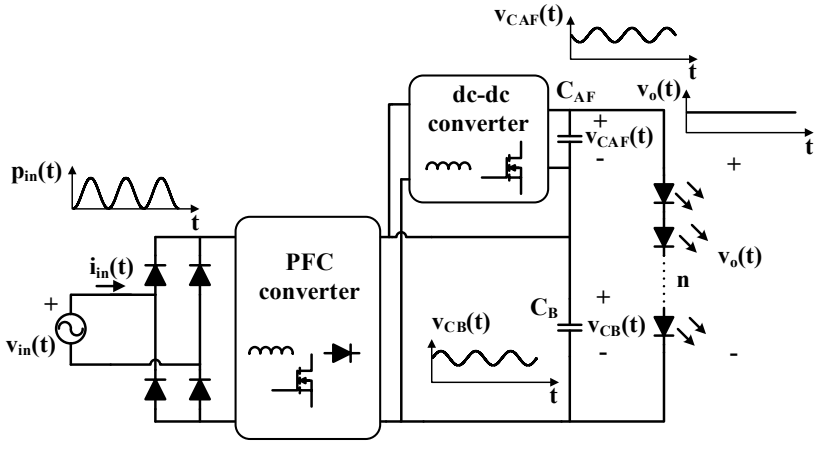
Continuing on the proposals to remove the electrolytic capacitor, the last ones are those that fall into what can be considered quasi-single-stage ac-dc converters. These converters do not fall strictly into the single-stage category but they cannot be considered as part of the multi-stage category either. Such are the ones that include a bidirectional dc-dc converter in parallel with the LEDs [1.121]-[1.127], the ones based on multi-output ripple cancellation [1.128]-[1.135] or the ones that combine the first and the second stage under shared switches [1.136]-[1.167] based on the concept proposed in [1.168]. In the first scenario, see Fig. 1.18. (a), the bidirectional converter handles the pulsating power (i.e., $p_{CAF}(t)$) of C_B consequently diminishing its size. In addition, C_{AF} can have a reduced capacitance as its charge and discharge is done more efficiently in comparison to the grid pulsating power, and unlike the two stage solution, the bidirectional converter does not process all the power. It should be noted that this solution based on a capacitor can have its equivalent inductance based on a series converter; however, the required inductance is much bulkier, thus it is avoided for ac-dc LED driver. A similar principle is applied in the multi-output voltage ripple cancellation solution, see Fig. 1.18. (b), in which a certain voltage ripple is allowed on C_B due to its size reduction which is compensated by the dc-dc converter responsible for cancelling it in order to drive the LED load with a dc current. For that reason, the output of the dc-dc converter will be a voltage waveform with its phase inverted from the output voltage of the PFC converter. The aforementioned quasi-single-stage solutions present high efficiencies at the cost of a complex control, higher cost and low bandwidth on the output current feedback loop. In fact, this complex control would in most cases require the use of digital control, which can also be seen as a drawback, as analog control is preferred for single-stage ac-dc LED drivers.

The last of the quasi-single-stage solutions discussed in this section, see Fig. 1.18. (c), bases its operation on allowing a certain ripple on C_B similarly to the ripple cancelling technique. However, this ripple is cancelled at the output of the converter with the help of a control loop included in the dc-dc converter stage that is able to correct the low frequency variations. In particular, this case follows the same principle used in two-stage solutions that will be discussed later on in Subsection 1.4.1.2.3. Then, it is not unexpected that the presented topologies are based on the most popular multi-stage solutions. However, the rendered topologies are not as efficient as the two-stage solutions that they come from, due to stress happening on the switches as a consequence of sharing operation for both stages, or the aforementioned quasi-single-stage, due to the double power conversion that occurs, which is the trade-off for a more cost effective solution with a higher power density.

Delving into single-stage ac-dc LED drivers for luminaires (i.e., $p_{in} > 25$ W), most of the topologies are shared topologies with the retrofit ones, as long as they demand a sinusoidal current [1.109]. In the case of luminaires, the preferred solutions are focused around the buck-boost and the boost converter family. The first is able to provide the LED with lower voltages while keeping a sinusoidal current. Among the non-isolated



(a)



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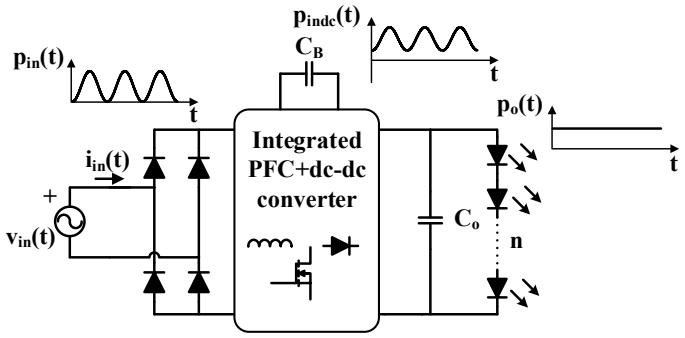


(c)

Fig. 1.18. Most common quasi-single-stage solutions to remove the electrolytic capacitor. (a) Bidirectional dc-dc converter. (b) Multi-output voltage ripple cancellation. (c) Integration of a two-stage into a single-stage with common active components.

buck-boost family solutions: the buck-boost [1.138]-[1.145], see Fig. 1.19. (a), the Ćuk [1.169]-[1.172], see Fig. 1.19. (b), the SEPIC [1.162]-[1.167], [1.173]-[1.175], see Fig. 1.19. (c) and the Zeta [1.176] converters can be found. The last three are normally avoided in low cost applications due to their increased number of components [1.177], [1.178]. In fact, their isolated variants are barely used in ac-dc LED drivers due to the versatility of the flyback converter and the fact that their integrated stages with an isolated or non-isolated dc-dc converter tend to be more efficient, able to remove the electrolytic capacitor and have a lower component count [1.106].

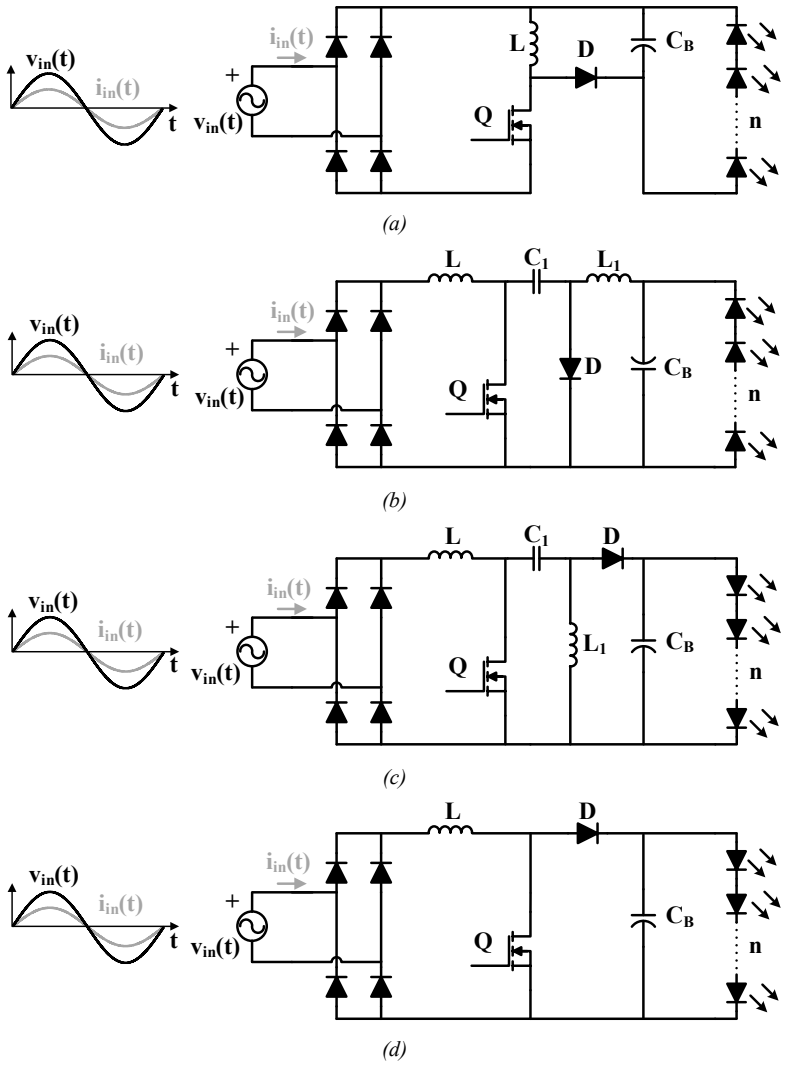
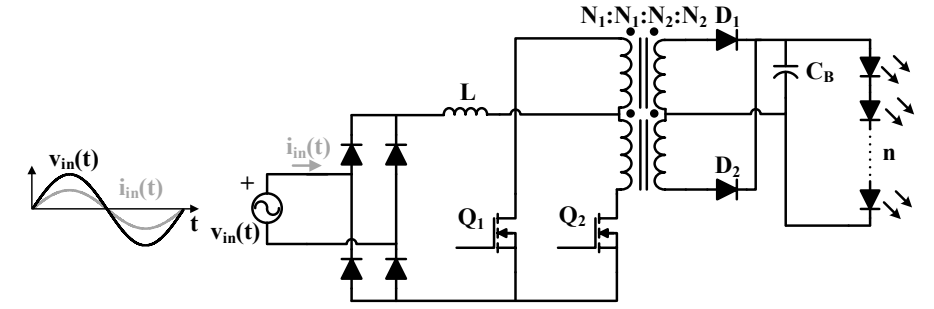


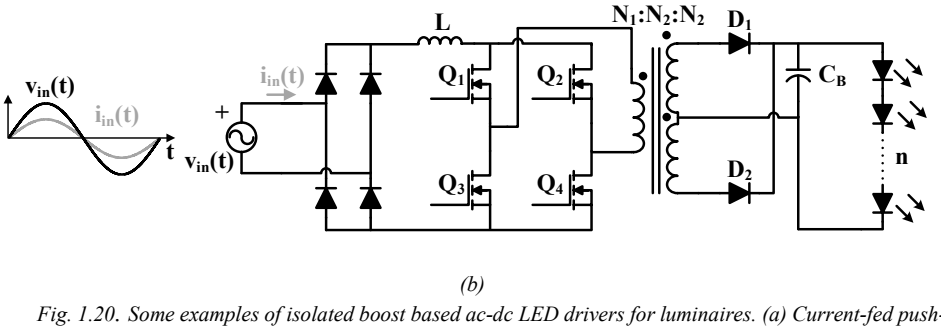
Fig. 1.19. Some examples of non-isolated ac-dc LED drivers for luminaires. (a) Buck-boost converter. (b) Ćuk converter. (c) SEPIC converter. (d) Boost converter.

The boost converter, see Fig. 1.19. (d), can also be used in single-stage ac-dc LED drivers for luminaires. However the necessity to work with higher voltages has made the use of this converter situational due to the amount of LEDs required in series for the LED load, which as have been seen in Section 1.2.2 is not a recommended practice. Nevertheless, the advances in LED technology have made possible the use of an ac-dc single-stage boost converter to drive high voltage LEDs [1.179], [1.180]. Otherwise, a boost integrated with a step-down dc-dc converter can be used to drive LEDs, being either a conventional [1.149]-[1.155] or a bridgeless PFC boost [1.156]-[1.159]. The latter, has the same operation as a conventional boost but the low frequency diode bridge is removed in order to achieve an improvement in its efficiency.

The isolated variations of the boost converter family, also referred as current-fed isolated converters, are rarely used in PFC due to the several issues they present, such as, complex transformer design, the need for demagnetization path for their main inductance or inductances, or complementary signals in comparison to the traditional controllers. It is because of these issues that their potentially higher efficiency is hindered achieving a similar level to that of the buck-boost family isolated converters [1.181]. Nonetheless, some works of single-stage ac-dc current-fed isolated converters have been proposed in literature, such as, a current-fed push-pull [1.182], see Fig. 1.20. (a) or a current-fed full-bridge [1.183], see Fig. 1.20. (b). In the previous literature, the use of these topologies to implement LED drivers can be found, particularly a push-pull converter is in [1.184]. The proposal does not address any of the aforementioned issues, achieving a very low efficiency while suffering at the same time from high voltage stress on the main switches. Furthermore, due to the lack of commercially available analog controllers for the driving



(a)



(b)

Fig. 1.20. Some examples of isolated boost based ac-dc LED drivers for luminaires. (a) Current-fed push-pull. (b) Current-fed full-bridge.

of current-fed topologies, the control is normally implemented digitally, which in this particular scenario can be considered a drawback as its cost and complexity increases.

As regards the dynamic response of single-stage ac-dc LED drivers, it is normally slow due to the low bandwidth output current loop required to filter the low frequency harmonics from the mains that appear on the output current. This is not the case for most solutions that integrate a two-stage ac-dc LED driver or in the upcoming multi-stage ac-dc LED drivers, as the second stage can provide a higher bandwidth. Nonetheless, the dynamic response is unimportant for LEDs as they are considered a slow load, as long as the low frequency output ripple is cancelled [1.18].

1.4.1.2.3 Multi-stage solutions

Conventionally, in PFC, two-stage solutions have been used to drive dc loads, see Fig. 1.21. (a) [1.80]. The first stage is dedicated exclusively to perform PFC by using topologies that could achieve unity PF and provide the second stage with an almost constant voltage. Consequently, the second stage is dedicated to ensure an adequate voltage or current level on the dc load and correct the low frequency ripple that appear on C_B due to its lower capacitive value to achieve the removal of the electrolytic capacitor. It should be noted that for the power range in which the multi-stage solution is used (i.e.,

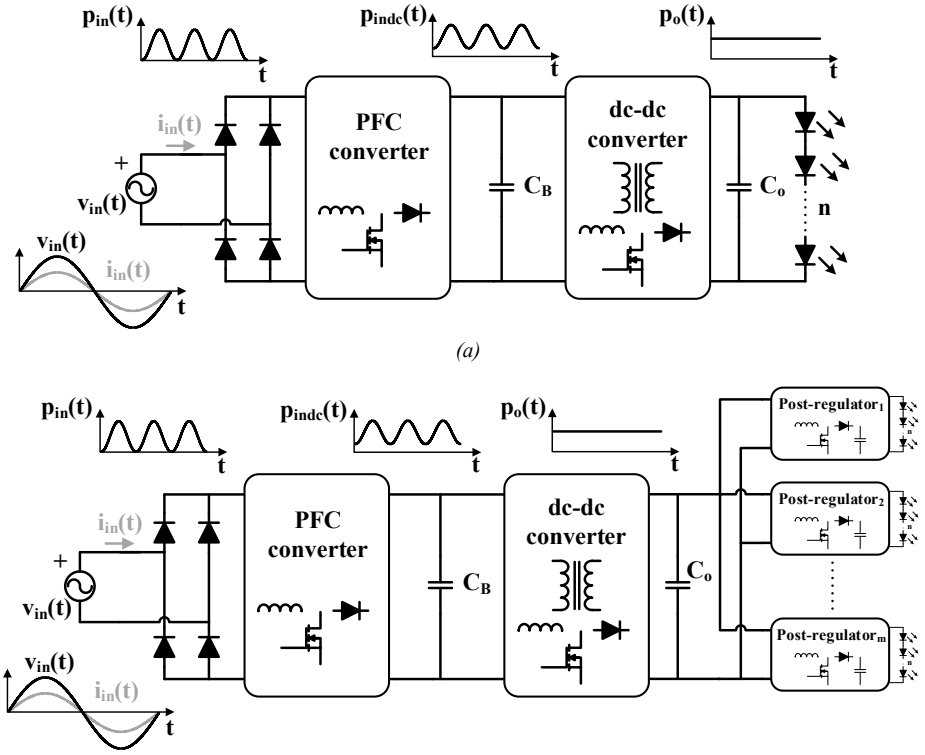


Fig. 1.21. Multi-stage solutions for LED drivers. (a) Two-stage solution. (b) Two-stage cascaded with a parallel input post-regulator configuration.

the driving of LED luminaries), the inclusion of galvanic isolation is recommended and tends to be mandatory. In fact, galvanic isolation can be included either in the first or the second stage. Although it can be done in the first stage by means of a flyback converter, this implementation suffers from low efficiencies and a bulkier capacitor due to the lower power density of low voltage capacitors in comparison to high voltage ones [1.55], [1.186]. Considering this fact, the inclusion of galvanic isolation is normally performed in the second stage.

It is commonplace to think that a two-stage solution would be less efficient than the previously presented single stage solutions. The reasons are the increased number of components and the double power conversion. Even so, the two-stage solution overall performance is better in terms of efficiency and reliability, due to the better optimization of its tasks in its two different stages and the removal of the electrolytic capacitor [1.185].

The aforementioned reasons make the use of two-stage solutions a reality for ac-dc LED drivers. However, as it has been mentioned before, the cost and complexity are the most limiting factors in most applications. Hence, these solutions are normally used for high performance luminaires (i.e., achieving full dimming and flicker free performances) in which reliability and efficiency are of utmost importance. In fact, ac-dc LED drivers occasionally add a cascaded extra stage, referred in previous literature as a post-regulator stage [1.44], see Fig. 1.21. (b). The post-regulator is connected directly to the LED string, requiring as many post-regulators as there are LED strings in the LED load, and is responsible for actively sharing the current between strings to ensure an adequate light output of the luminaire.

In the previous section different solutions to implement the PFC stage have been evaluated. Particularly for multi-stage LED drivers, the most common topology is the PFC boost converter working in either Continuous Conduction Mode (CCM) or Boundary Conduction Mode (BCM) to achieve unity PF. The latest trends are focused on using its bridgeless variants to achieve higher efficiencies by removing the input diode bridge rectifier [1.187], [1.188], making the use of digital control mandatory. Nonetheless, its cost and complexity is justified in multi-stage solutions considering their aim for higher reliability and performances, even though traditionally in PFC analog combo controllers have been used [1.189]. That being said, the focus of this section will be put on the other stages: the isolated dc-dc converter and the post-regulator.

Traditionally the second stage provides fast output voltage response and galvanic isolation. In the case of an LED load, the main characteristic that needs to be fulfilled is the cancelling of the low frequency ripple of the PFC converter while achieving a high efficiency. There is a limited spectrum of isolated solutions that can achieve this performance by means of a fast output feedback loop or a feed-forward input closed-loop, while guaranteeing a flicker free light output. In fact, there are two favored solutions over simpler ones, such as the flyback [1.190], for this particular application: the LLC resonant converter, that can be found either in its half-bridge, see Fig. 1.22. (a), or full-bridge configuration, or the Asymmetrical Half-Bridge (AHB), see Fig. 1.22. (b).

In the case of the AHB, this stage is able to provide high reliability and high efficiency by reaching Zero Voltage Switching (ZVS) in the primary switches [1.191]-[1.195]. In addition, the control scheme and the limited output voltage range required for the driving of LEDs allow a small design for its output filter. In fact, the low voltage range makes it

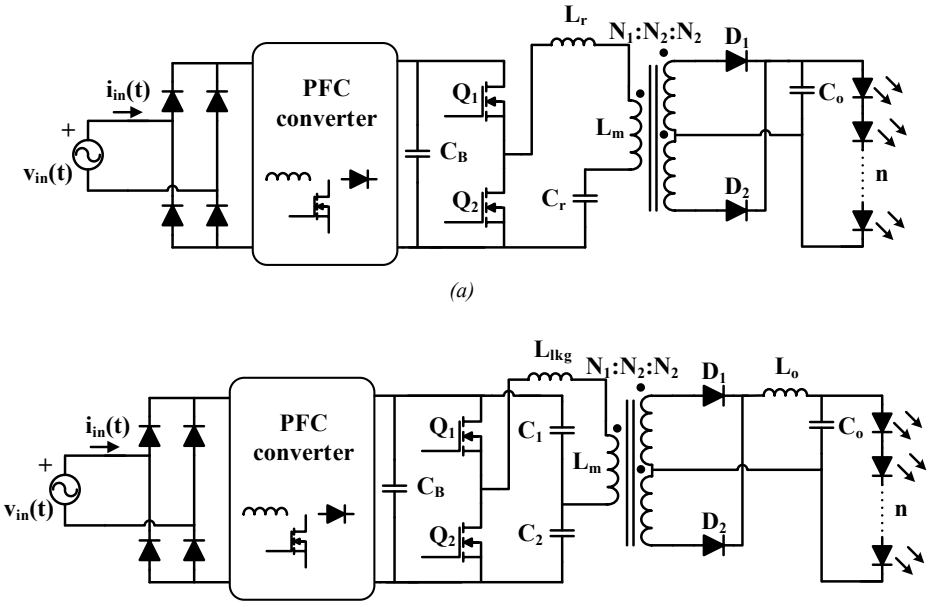


Fig. 1.22. Preferred solutions for the dc-dc isolated stage of a multi-stage ac-dc LED driver. (a) Half-bridge resonant LLC (b) Asymmetrical Half-Bridge (AHB).

possible to implement self-driving techniques when using synchronous rectification in the secondary side of the transformer [1.193]. On the contrary, the duty cycle range is limited to variations between 0 and 0.5, the potential bandwidth of its output feedback loop is limited due to the resonance that occurs between the input capacitors and the magnetizing inductance, and the dc gain is not linear. Some authors have proposed different techniques to overcome the bandwidth limitation to cancel the voltage ripple, such as the use of a feed-forward loop [1.193], [1.194]. Others have proposed the use of the Zeta AHB (ZAHB), which solves the two main disadvantages of the AHB, as are non-linear gain and the duty limitation [1.196].

The LLC resonant converter has been widely used for LED driving due to its high efficiency achieved by obtaining soft-switching in its main switches [1.197]-[1.205]. However, ZVS is achieved during the turn-on on the primary switches and Zero Current Switching (ZCS) is achieved on the diodes for singular conditions. These conditions limit the operating frequency to lower values than the resonant tank. Hence, when the load reduces the operating frequency will surpass that of the resonant tank, which means that the turn-off losses will increase. Some of the issues related to obtaining soft-switching conditions in in this topology are improved for wider power ranges with the help of other resonant tanks [1.206]-[1.208].

According to the previous literature, the introduced second stages are able to remove the electrolytic capacitor without incurring in flicker, achieve high efficiencies (i.e., > 97%) and perform total dimming. However, they are unable to ensure a correct light output in complex LED loads due to the lack of current control on each of the strings,

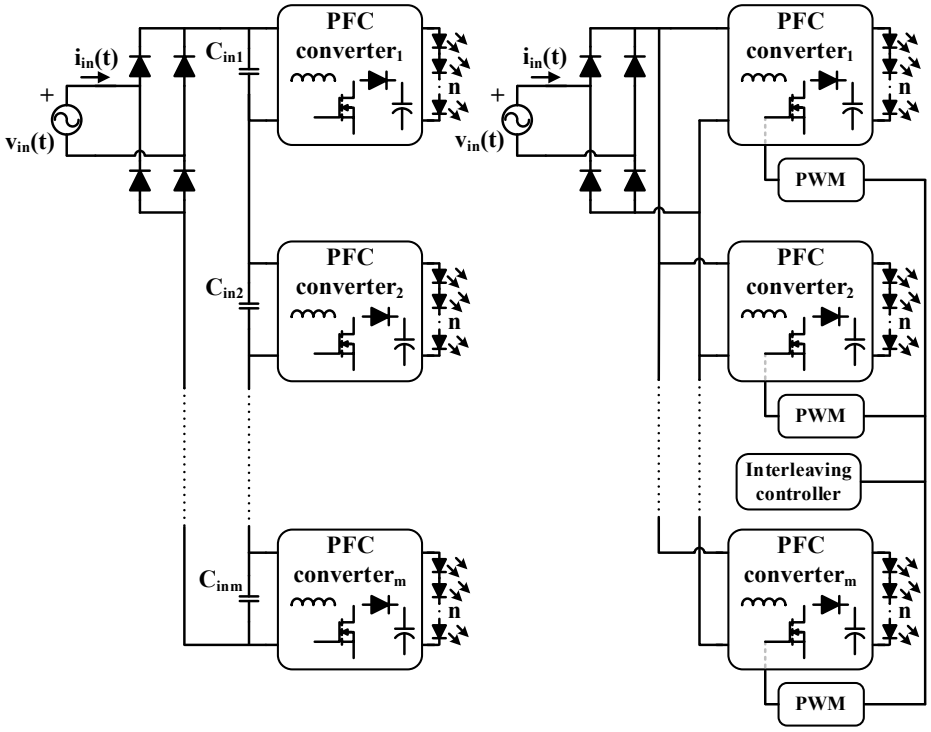
unless one of the current sharing techniques described in Section 1.2.2 is used. Consequently, for the scope of multi-stage solutions the implemented current sharing method needs to be extremely efficient. This statement discards the linear based regulator and the passive resistor current sharing techniques because of their low efficiencies, reducing the solutions to the use of a post-regulator per string [1.42]-[1.44], [1.210]-[1.213] or a PWM dimmer per string [1.214], [1.215]. Another possibility is the integration of the post-regulator with the isolated dc-dc converter to reduce the cost and achieve active current sharing by means of multi-output converters [1.206], [1.209]. The issues with the integration come from the requirement of several high frequency transformers, which would make the ac-dc LED driver bulkier, and require a complex control to ensure the active current sharing. For this particular application, the buck converter is the preferred solution.

Among the newer trends that could be found in literature to reduce the cost of the second stage or the post-regulator is the driving of LEDs with high frequency pulsed current, also referred in literature as High Frequency (HF) AC-LED. Unlike the LF AC-LED described in Subsection 1.4.1.1, the HF AC-LED does not incur in flicker due to the high frequency used. In fact, the difference with a PWM dimming pulsed current is using the switching frequency output current of a dc-dc converter by removing the output filter responsible for obtaining a dc current. This method has been applied to isolated dc-dc converters driving LEDs with a HF sinusoidal waveform [1.207], [1.216], [1.217], a flyback working in DCM pulsed current, therefore, the driving is performed with a triangular waveform [1.218], [1.219] and a self-oscillating driving the LEDs with a quasi-sinusoidal waveform [1.220]. None of the authors had empirically demonstrated the impact of pulsed current driving of LEDs on their lifetime, since they incur in some cases in extremely high current peaks to achieve an adequate dc current level. Moreover, some of them require the duplication of the LED strings [1.207], [1.216], [1.217] not justifying the cost reduction, as the switching output current of the isolated dc-dc converter is required to be rectified.

1.4.1.2.4 Modular solutions

Modular solutions are rarely used on ac-dc LED drivers due to the increased amount of components and complexity, potentially reducing the reliability of the driver. Nevertheless, some authors have studied solutions based on stacking several converters in series connected to the ac grid [1.121], see Fig. 1.23. (a). This technique allows the use of cheaper and more efficient semiconductors due to the reduction of voltage and current withstood by them, but the overall power density is reduced due to the size limitation of the control stage, requiring another feedback loop to control the power demanded by each module. Furthermore, it is able to reduce the size of the output capacitor by stacking several capacitors; however, the removal of the electrolytic capacitor is not achieved naturally.

The other solution, which is well-known in PFC, can be implemented with an input-parallel connection. The idea behind this one is connecting several PFC converters in parallel at its input and phase shifting their PWM in such a manner that the sum of the input currents reduces the ripple of the input current of the ac-dc LED driver [1.221]-[1.223], not requiring for the LED loads to be connected in between, see Fig. 1.23 (b). In fact, the more converters there are the lower the overall current ripple is. This method is referred in literature as interleaving and can be achieved both in open or closed loop with



(a) (b)

Fig. 1.23. Modular solutions for LED drivers. (a) Input-series. (b) Input-parallel with interleaving.

any ac-dc or dc-dc converter. Consequently, it is used with the ones that present significant input current ripples in order to reduce it, as those working in DCM or BCM [1.224], [1.225]. The main reason for using this technique is the reduction in size of the EMI filter, which grows larger with the input current ripple, affecting both the size and weight of the LED driver [1.226]. It should be noted that this technique does not impact the removal of the electrolytic capacitor and that the reduction of the EMI filter needs to consider the increased amount of components, as well as, the increase in size and control complexity of a modular solution.

1.4.2 Three-phase LED drivers

Along Section 1.4.1, it has been seen that the removal of the electrolytic capacitor is crucial to increase the lifetime of the ac-dc LED driver for it to be comparable to that of the LEDs. The reason behind is the pulsating power of the ac grid which would result in a flicker effect on the light output of the LED load, which is both annoying and hazardous for human beings. This is not the case for a balanced three-phase ac power grid and all the required extra stages to remove said component can be disposed of. As outstanding as this is, there are two important limitations that prevent three-phase ac-dc LED drivers from being massively used.

Firstly, the lack of voltage standardization. Unlike single-phase power grids, in which the voltage is limited between 80 and 270 V, three-phase ac power grids show a wider

range depending on the country and power of the grid. For low voltage three-phase ac power grids, the rms line-neutral voltage is nominally 347 V in Canada, 480 V in the US [1.227] or 230 V in the European Union with the exception of the UK with 240 V. Although the proposal of a universal three-phase ac-dc LED driver seems complex and inefficient, it is not such a limiting factor to use regionally designed LED drivers, when the improvement in cost and simplicity is justified. In fact, considering the scope of power for medium to high power luminaires (i.e., 50 W to 10 kW) the mobility requirement of universal PFC solutions can be completely disregarded.

And secondly, three-phase ac power grids are not as readily available as single-phase ones. This fact reduces the applicability of this solution, since household ac-dc LED drivers represent most of the current LED driver, and wiring three-phase ac power grids to household environments is costly for the benefits obtained. Therefore, three-phase ac-dc LED drivers are proposed for those places where the three-phase ac power grid is accessible, such as, commercial and industrial installations. The application can then be focused on medium power bulbs, tunnel lights, stadium spotlights, floodlights, etc. Particularly, for those luminaires of more than 250 W that require high reliability and efficiency.

These two reason are key to understand the most common way used nowadays to drive LEDs in three-phase ac power grids. The method is based on using a step-down autotransformer connecting it between line and neutral to adjust the voltage to that of a single-stage ac-dc LED driver [1.228]. This methodology requires access to neutral, limiting the use of this solution to 4-wire grids. It also reduces the efficiency of the system greatly due to the losses of the autotransformer which can achieve in the best case 95% efficiency. Furthermore, the most important aspect is the increase in size and weight that a LF autotransformer does to the whole system [1.229].

In order to solve the aforementioned issues the use of specific three-phase ac-dc converters to drive LED loads increasing both efficiency and power density while guaranteeing non-flicker performance have been proposed [1.230], [1.231]. This section will focus on the most promising solutions for LED driving based on three-phase ac-dc considering the lack of previous literature on the topic.

1.4.2.1 Single-stage solutions

Following the same principle introduced for single-phase ac-dc single-stage solutions, the aim would be to comply with Class C from IEC 61000-3-2, which as a reminder is the most restrictive of the two harmonic injection regulations that a three-phase ac-dc LED driver will need to comply with, being the other Class A from IEC 61000-3-2. Hence, the studied solutions would require sinusoidal input current waveforms in phase with their respective phase voltage. These topologies can be further divided into single-switch and multi-switch categories in accordance to the amount of active switches used. The first ones are the most attractive for LED drivers in terms of cost and reliability. Among these solutions there are two that stand out from the rest, as are the three-phase ac-dc single-switch boost converter, see Fig. 1.24. (a), and the three-phase ac-dc single-switch flyback converter, see Fig. 1.24. (b).

The three-phase ac-dc single-switch boost converter is able to achieve a quasi-LFR performance in DCM or in pseudo-BCM depending on the gain of converter (M) [1.232]-[1.237]. In fact, the higher the converter gain, the lower the THD, requiring at

least a gain of 3 and 2.2 to ensure the compliance with Class C from the IEC 61000-3-2 in DCM and pseudo-BCM, respectively. In this particular case, the LED load will be withstanding high voltages (i.e., a minimum of 1 kV for DCM and 800 V for pseudo-BCM under the European input voltage standard.) Nonetheless, this task can be alleviated with the latest technology of HV LEDs. Moreover, due to the high voltage bus the main switch will incur into higher switching losses and soft-switching will become necessary to achieve an efficient solution. Some authors have proposed the use of passive filtering the input current to achieve lower bus voltages and lower THDs at the cost of increasing weight and size which is undesirable for an LED driver [1.236].

In a similar fashion, a dc-dc flyback converter can be connected to a three-phase rectifier, by doing so, galvanic isolation is achieved. However, the LFR performance of the flyback in this configuration will make the input currents of each phase not to be ideally sinusoidal since the conduction angle is 120º, not complying with the aforementioned regulation. In order to solve this issue, an LFR performance needs to be achieved per phase. For that matter, some authors have proposed the three-phase ac-dc single-switch flyback converter, see Fig. 1.24. (b), in which a coupled inductor with two input windings is used for each phase. The upper winding conducts during the positive half line cycle of the voltage phase and the lower winding during the negative one [1.238], [1.239]. Accordingly, the operation of the driver is equivalent to the use of a flyback per phase achieving the desired operation. However, its PF roughly reaches 0.9 for the higher voltages of the European three-phase ac power grid, its efficiency is well below the desired 90% for an ac-dc LED driver, the design tolerances of the coupled inductances

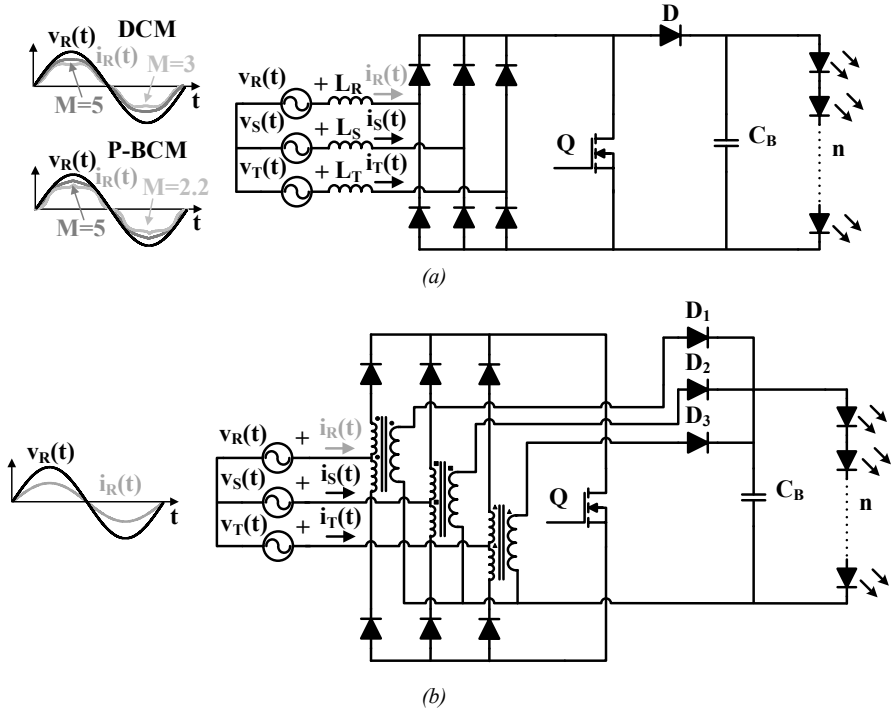


Fig. 1.24. Single-switch three-phase ac-dc solutions for LED drivers. (a) Boost converter. (b) Flyback converter.

can severely affect the current ripple on the LED load, and the main switch needs to withstand high voltages and currents [1.230]. These characteristics make this driver unfitting for luminaires of more than 200 W, which is the desired range of power for this kind of solution. Furthermore, the importance of galvanic isolation introduced for single-phase ac-dc LED drivers to meet the safety requirements, becomes inconsequential for their three-phase counterpart considering the aim for high power luminaires in inaccessible places which only authorized personnel should have access to.

Taking into account this last statement and in search of more efficient ac-dc LED drivers, multi-switch ac-dc three-phase can be considered into this study. Consequently, the simplest topology that can achieve unity PF is the multi-switch boost converter, see Fig. 1.25. (a) [1.240]-[1.243]. In fact, this topology achieves lower voltages on the output bus than the single-switch one previously introduced while keeping a sinusoidal input current. The condition to achieve unity PF requires the output voltage to be greater than the output dc voltage attained by the six diode rectifier bridge formed by the parasitic diodes of each MOSFET, which can be defined by,

$$v_o=\sqrt{6}v_N\frac{3}{\pi}, \tag{1.11}$$

where v_N defines the rms voltage of a certain phase, considering that N can either be R, S or T.

Continuing the analysis, some authors have tackled the design of three-phase multi-switch ac-dc LED drivers by means of switched capacitor converters, see Fig. 1.25. (b)

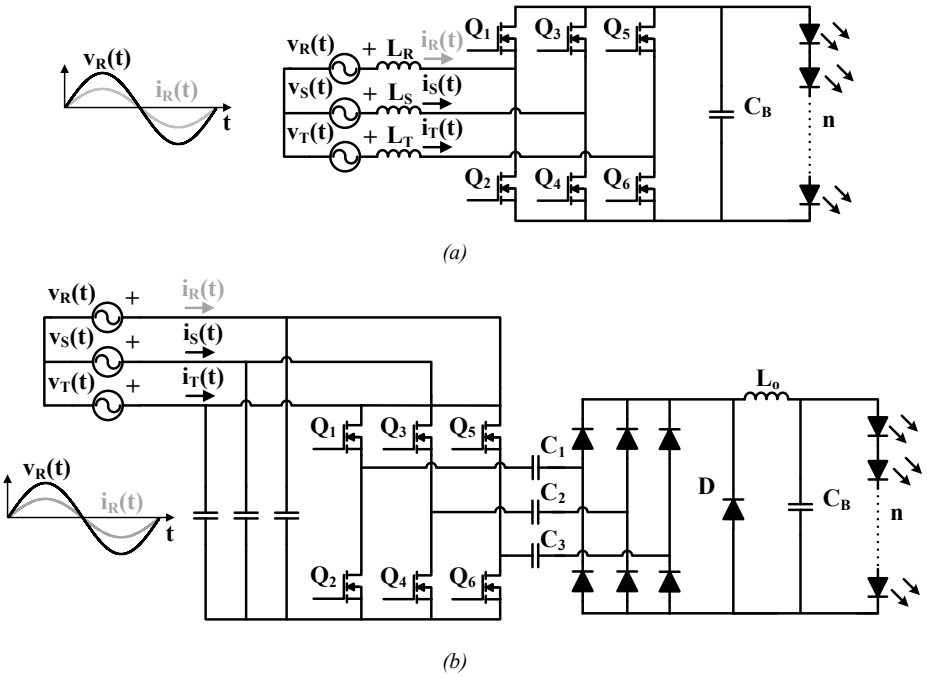


Fig. 1.25. Multi-switch three-phase ac-dc solutions for LED drivers. (a) Boost converter. (b) Resonant switched capacitor LED driver.

[1.231]. These ac-dc LED drivers can achieve high power density, high efficiency, do not require current sensing to maintain a stable light and can have lower output voltages than (1.11). In contrast, the proposal requires variable frequency operation, controls the voltage withstood by the LED load instead of its current, cannot achieve full dimming condition and require several active switches and diodes, which will hinder its reliability.

1.4.2.2 Multi-stage solutions

Another possibility to attain input sinusoidal waveforms is the use of multi-stage solutions. Unlike single-phase ac-dc multi-stage solutions, in which the isolated dc-dc converter could remove the low frequency ripple across the LED load, three-phase ac-dc LED drivers can naturally remove the low frequency ripple with a single-stage, hence, disposing the electrolytic capacitor due to the non-pulsation of the power grid on the load. Therefore, the actual use of this second stage would be focused on adapting the voltage and current levels to those required by the LED load and provide galvanic isolation. For that matter, the purpose of the second stage is closer to the post-regulator or third stage of the single-phase ac-dc multi-stage scheme. The topologies normally used for the second stage are similarly based on the ones introduced for the single-phase multi-stage LED drivers due to the requirement of a high step-down gain [1.244], [1.245] (i.e., LLC or AHB).

In regard to the first stage, it is traditionally comprised of the three-phase multi-switch ac-dc boost previously introduced, because of its higher efficiency and its ability to achieve PFC. This higher efficiency becomes necessary in order to be able to compete with single-stage based solutions as the two stages will hinder the efficiency of the three-phase ac-dc LED driver. However, one of the main advantages, which is bi-directionality, will not be leveraged with an LED load. In addition, the increased amount of components, which increment cost and diminish reliability, the arguably lower efficiency of the whole driver and the lack of purpose of the second stage responsible for removing the electrolytic capacitor for the single-phase scenario, have made the use of three-phase multi-stage ac-dc LED drivers unattractive.

1.4.2.3 Multi-cell solutions

Considering the amount of components used for the three-phase multi-stage ac-dc LED drivers, another feasible solution was proposed by Delco as a three-phase rectifier using thyristors as the main switches for a resistive load [1.245]. The approach is based on having several ac-dc converters with PFC (i.e., PFC converters), which will be defined as cells, each connected to a phase and working as an LFR, see Fig. 1.26. These ac-dc converters require galvanic isolation in order to be able to connect their outputs in parallel. By doing so, the electrolytic capacitor can be removed as there is no actual pulsation of power on the load, as has been explained several times before in this section.

The multi-cell approach is more complex from a control point of view since they add more components and are arguably more expensive than the three-phase single-switch single-stage ac-dc LED drivers, and require the use of a central control unit. This central control unit will be responsible for ensuring each of the modules processes the same amount of power and of its correct start-up, normally requiring a digital control for this purpose. In contrast, they have a better trade-off between output voltage and THD than the aforementioned three-phase single-switch single-stage ac-dc LED drivers.

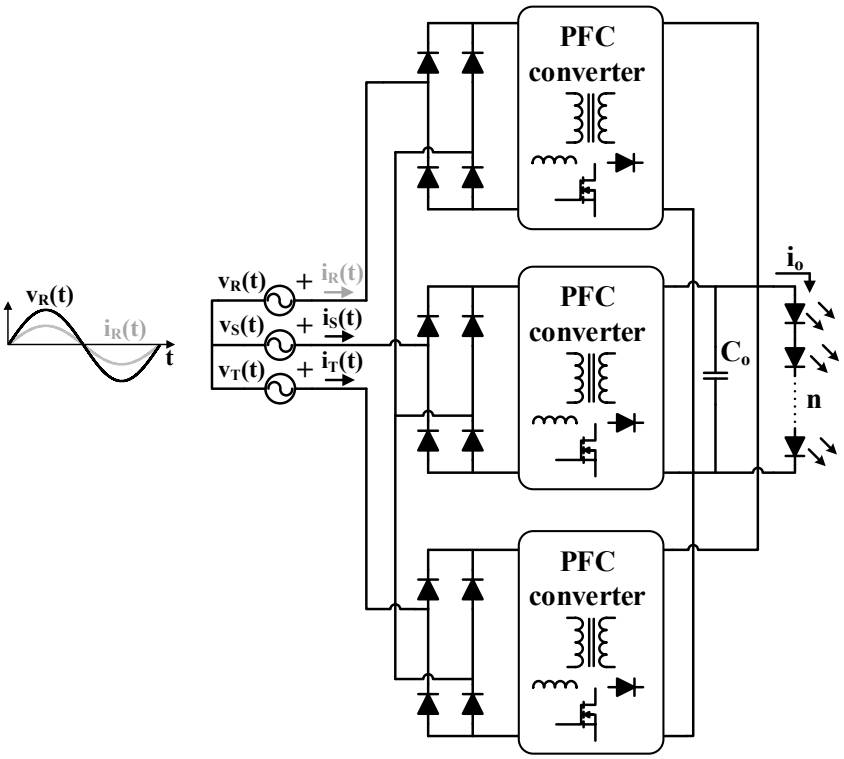


Fig. 1.26. Multi-cell three-phase rectifier based on using three single-phase PFC converters with fictional neutral connection.

Moreover, the design of each module is equivalent to that of a single-phase ac-dc converter with PFC, which simplifies and improves the power scaling of the ac-dc LED driver. As has been introduced before in Subsection 1.4.1.2.1, an LFR performance is required to attain PFC, particularly for this case with galvanic isolation. Therefore, the simplest way to achieve this performance is by means of an isolated topology from the buck-boost family working in DCM. For that matter, some authors have proposed to use the following topologies as cells, the flyback converter [1.247], [1.248], the Ćuk converter [1.249] or the SEPIC converter [1.250]. The issue is the same one introduced before regarding the low efficiencies achieved by these converters in comparison with a two-stage solution. Therefore, it is also possible as introduced by other authors, the use of a two-stage cell approach in order to achieve higher efficiencies [1.251]. In contrast, the control and amount of components included in this solution increases dramatically, becoming of interest for high power luminaires (i.e., > 1 kW).

1.5 Objectives and contributions

The objective of this dissertation is the development of more efficient solutions (i.e., > 90%) to drive LEDs in ac power grids while complying with the regulations introduced in Section 1.3, while aiming to dispose of the electrolytic capacitor in most scenarios. For that matter, the state of the art was carefully compiled and studied in order to evaluate feasible solutions in an already crowded research environment, as has been discussed throughout Section 1.4. Furthermore, the scope of the analysis has been widened from the conventional single-phase ac-dc solutions to the driving of LEDs in three-phase ac power grids.

The contributions of this work can then be summarized as,

- a multi-cell three-phase ac-dc topology based on the concept of LFRs to drive LEDs. Each diode of the conventional three-phase rectifier is connected in series with an LFR that will shape adequately the current of each phase to achieve PFC. The proposed topology is carefully studied attaining its steady state and dynamic analysis. Then, it is compared with the conventional Delco topology in order to foresee the scope of application of both topologies for LED driving in three-phase ac power grids which are naturally able to remove the electrolytic capacitor. (Chapter 2.3)
- a multi-cell three-phase ac-dc topology based on controlling independent LED loads per phase is also proposed. Each LED load is driven with high current ripple to remove the electrolytic capacitor. The pulsating light output of each phase is summed by taking advantage of the light properties and the three-phase ac power grid, rendering a constant light output due to the low frequency components being cancelled in between. (Chapter 2.4)
- a comprehensive analysis is carried out into the previous topology for the boost converter studying its performance with an LED load under low output capacitances, which causes high output current and voltage ripples. Hence, the mathematical limits between CCM and DCM need to be reevaluated as these high output current and voltage ripple conditions are not considered in the current literature. (Chapter 2.4)
- a single-stage single-phase ac-dc converter based on a dual inductor current-fed push-pull. The proposed topology is carefully studied in steady state and dynamically. The proposed control method is also studied based on interleaving adequately the main switches. (Chapter 3)
- a post-regulator stage in which the LEDs are used as the rectifier of the basic dc-dc converter that comprises the post-regulator stage. These family of converters suffer from the reverse recovery effect on the diode, hence family of converters based on full wave ZCS Quasi-Resonant Converters is also proposed to remove this undesired effect. For the latter, a mathematical analysis is carried out in order to attain a static model that can both foresee the performance and study the conditions to guarantee both ZCS operation and the diminishment of the reverse recovery effect. (Chapters 4.1 and 4.2)
- a reliability testing of experimental prototypes to determine the effects of reverse recovery effect on the lifetime of the LEDs. In the process, different current

waveforms (i.e., dc current and pulsed current) are also compared in terms of their effect on the lifetime of the LEDs. (Chapter 4.3)

As the outcome of this dissertation, several scientific papers have been published in international journals and conferences:

- I. Castro, D. G. Lamar, M. Arias, M. M. Hernando and J. Sebastian, "Multicell Three-Phase AC–DC Driver for HB-LED Lighting Applications," in IEEE Transactions on Industry Applications, vol. 53, no. 4, pp. 3803-3813, July-Aug. 2017.
- I. Castro, K. Martin, A. Vazquez, M. Arias, D. G. Lamar and J. Sebastian, "An AC–DC PFC Single-Stage Dual Inductor Current-Fed Push–Pull for HB-LED Lighting Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 1, pp. 255-266, March 2018.
- I. Castro, D. G. Lamar, M. Arias, J. Sebastian and M. M. Hernando, "Three phase converter with galvanic isolation based on Loss-Free Resistors for HB-LED lighting applications," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 822-829.
- J. Sebastian, I. Castro, D. G. Lamar, A. Vazquez and K. Martin, "High power factor modular polyphase AC/DC converters with galvanic isolation based on Resistor Emulators," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 25-32.
- I. Castro, K. Martin, D. G. Lamar, M. Arias, M. M. Hernando and J. Sebastian, "Single-stage AC/DC dual inductor BCM current-fed push-pull for HB-LED lighting applications," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8.
- I. Castro, S. Lopez, K. Martin, M. Arias, D. G. Lamar and J. Sebastian, "High frequency dc-dc AC-LED driver based on ZCS-QRCs," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, 2017, pp. 3688-3695.
- I. Castro, M. Arias, D. G. Lamar, M. M. Hernando and J. Sebastian, "Modular three-phase ac-dc converter based on summing the light output of each phase," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 1-1.

Some contributions have also been made in national conferences:

- I. Castro, D. G. Lamar, M. Arias, J. Sebastian y M. M. Hernando, "Convertidor CA/CC trifásico basado en resistencias libres de pérdidas para alimentar LED de alta eficiencia", XXIII Seminario Anual de Automática, Electrónica Industrial e Instrumentación 2016 (SAAEI'16), Elche (España) 6 al 8 de Julio de 2016.
- I. Castro, K. Martin, M. Arias, D. G. Lamar, M. M. Hernando y J. Sebastian, "Convertidor CA/CC en una única etapa para HB-LED, basado en un PUSH-PULL de doble inductancia alimentado en corriente", XXIV Seminario Anual de Automática, Electrónica Industrial e Instrumentación 2017 (SAAEI'17), Valencia (España) 5 al 7 de Julio de 2017.

- I. Castro, M. Arias, D. G. Lamar, M. M. Hernando y J. Sebastian, "Convertidor modular trifásico CA/CC para aplicaciones LED basado en la suma de luz por fase", XXV Seminario Anual de Automática, Electrónica Industrial e Instrumentación 2018 (SAAEI'18), Barcelona (España) 4 al 6 de Julio de 2017.

1.6 Chapter overview

Chapter 2 studies the feasibility of driving LED loads in three-phase ac power grids by means of multi-cell three-phase ac-dc converters. The proposal takes advantage of the intrinsic removal of the electrolytic capacitor due to the non-pulsation of the power in balanced three-phase power grid. In that respect, it proposes two ac-dc LED drivers, one with galvanic isolation based on the three-phase full-wave rectifier, and another one without galvanic isolation based on summing the light output of each phase. Furthermore, the Delco topology, see Fig. 1.26, is retrieved for this application and adjusted accordingly to operate as an ac-dc LED driver. More importantly, this chapter includes the static and dynamic analysis of all three ac-dc LED drivers with special focus on the desired LFR performance at the input of each phase. Particularly, the operation of cells in the multi-cell ac-dc LED driver based on summing the light output requires to revise the limits between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) due to the high voltage and current ripple allowed at the output of each cell. The last sections of these chapter are dedicated to the experimental results obtained for the different three-phase ac-dc LED drivers under study which are compared in between and with the state-of-the-art solutions, carefully analyzing their advantages and disadvantages while ensuring compliance with the required regulations.

In **Chapter 3** the discussion of using isolated current-fed topologies as single-phase ac-dc converters is opened, and extended to single-phase ac-dc LED drivers. These topologies from the boost family achieve an LFR performance by means of control. However, they present several drawbacks preventing them from achieving outstanding performances. For that matter, the Dual Inductor Current-fed Push-Pull (DICPP) is retrieved from literature, see Fig. 3.1, where it is used as a high step-up dc-dc converter, and studied to operate as an ac-dc converter, proposing a simple control based on one isolated measurement. In addition its intrinsic interleaving between both inductors is able to reduce the input current ripple that both inductors present due to their operation in Boundary Conduction Mode (BCM), while it simpler transformer design improves the efficiency overcoming most of the aforementioned limitations present in single-phase current-fed topologies, and achieving a performance comparable to state-of-the-art single-phase ac-dc LED drivers.

Chapter 4 presents a family of simple converters that are to be connected to a dc power grid, thus aimed to be used as the post-regulator stage of a multi-stage ac-dc LED driver. The idea behind this family of converters is based on replacing the rectifier diode of the conventional dc-dc converters with the LED load. Hence, the LED load will work both as the load and as the rectifier diode of the converter, being driven by a high frequency current whose output light human eyes render constant, and being referred in literature as AC-LED driving. In that respect, the switching performance of the LEDs needs to be studied with special focus put on the reverse recovery effect. The latter is avoided by replacing the main switch with a full-wave quasi-resonant switch rendering the actual family of converters, which is statically analyzed and experimentally validated. Finally, the chapter compares experimentally the reliability over a period of 700 hours for

the conventional dc-dc converters, the quasi-resonant AC-LED driver and its non-resonant version, focusing on observing the impact of the reverse recovery effect and the different current waveforms on the lifetime of the LEDs.

Chapter 5 concludes this work discussing the most important conclusions extracted from the theoretical and experimental analysis. This lead to the proposal of future research around the topic of this dissertation.

The **Appendices** include:

- details the closed-loop operation and design of the output feedback loop for the proposed three-phase multi-cell isolated ac-dc LED drivers. (**Appendix A**)
- the analog control circuitry and methodology for the start-up and closed-loop operation of both the two-stage Delco three-phase ac-dc LED driver and the three-phase ac-dc LED driver based on summing the light output of each phase. (**Appendix B**)
- extended information over the mathematical analysis carried out for the ZCS-QRC LED drivers in Chapter 4. (**Appendix C**)

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2

Multi-cell three-phase ac-dc LED drivers

Mistakes are, after all, the foundations of truth, and if a man does not know what a thing is, it is at least an increase in knowledge if he knows what it is not.
— Carl G. Jung.

The present chapter discusses the use of specific compact, scalable and modular solutions to drive LEDs in three-phase power grids by means of multi-cell ac-dc rectifiers. For that matter, two topologies are proposed: the first takes advantage of the LFR concept for the realization of the cells that it is comprised of, requiring their outputs to be connected in parallel, thanks to the galvanic isolation included in the cells, in order to conform the output of the driver which is then connected to the LED load without an electrolytic capacitor. And the second, following a similar concept, instead of connecting the cells in parallel, it takes advantage of the light properties to sum the light output of each phase rendering a constant and perfectly safe light output without using electrolytic capacitors. Throughout this chapter, the operation of both topologies is carefully studied, both considering the steady state analysis and the dynamic analysis in order to obtain the required tools for the correct design of both ac-dc LED drivers. In fact, for the second ac-dc LED driver in which the cells are working under very specific conditions with both high voltage and current output ripples rarely seen for ac-dc converters with PFC, a study is required in terms of the conduction limits in order to discern whether the cells are affected by this specific operation. Moreover, the proposed topologies are built and experimentally compared in between and with the ones proposed in the previous literature.

2.1 Introduction

In the previous chapter, a handful of methodologies to drive LEDs in three-phase power grids were discussed. Most of these topologies have not been actually described in literature as LED drivers but just as three-phase ac-dc rectifiers, which were considered in this dissertation as potential candidates for the task taking into account the lack of research on the topic. However, the multiple advantages of LEDs thoroughly discussed along the previous chapter, allow them to replace traditional lights in household,

commercial and industrial installations for a wide spectrum of power, ranging from a few watts to a few kilowatts. In particular, the primary availability of the three-phase power grid in commercial and industrial installations around the globe makes the use of specific three-phase solutions a possibility aiming for high power luminaires (i.e. medium power bulbs, tunnel lights, stadium spotlights, floodlights, etc.).

The most widely used method for driving LEDs in three-phase power grids has been already discussed in the previous chapter based on using a stepdown auto-transformer per phase in order to adequate the different input voltages, that could be found around the globe, to acceptable voltage levels that a single-phase ac-dc LED driver could use at its input. The drawbacks present in this technique are: the requirement of extra components to remove the electrolytic capacitor, the availability of the neutral, the low efficiency achieved due to the extra power stages and the auto-transformer, and the increase in weight and cost caused by the auto-transformer.

From the theoretical standpoint, the removal of the electrolytic capacitor from the driver can be performed naturally in a three-phase power grid due to the non-pulsation of the total input power of the grid, as long as, all the phases supply the same load. Hence, not requiring a large storage element in order to supply the load with a constant power. The only requirement to ensure this performance is achieving unity PF per phase. Consequently, if each phase demands a sinusoidal current in phase with its phase voltage, then the input current of the phases can be defined by,

$$i_N(t)=\frac{v_N(t)}{R_{LFR}}=\frac{v_{gp}}{R_{LFR}}\sin\left(\omega t\text{-}N\frac{2\pi}{3}\right), \tag{2.1}$$

where $v_N(t)$ represents the phase voltage, v_{gp} represents the peak of the input voltage, R_{LFR} represents the equivalent resistor value of the converter performing as an LFR, ω represents the angular pulsation of the grid and N represents the phase under study, R, S or T. It should be noted that R, S and T are given a fixed value to unify and simplify the analysis. Consequently, N is equal to 0 for phase R, 1 for phase S and 2 for phase T. From (2.1), it is possible to obtain the total input power demanded under the aforementioned scenario by summing the power demanded by each phase, as,

$$p_{in}(t)=\sum_{N=0}^{2}\frac{v_N^2(t)}{R_{LFR}}=\frac{v_{gp}^2}{2R_{LFR}}\left\{3\text{-}\left[\cos(2\omega t)+\cos\left(2\omega t\text{-}\frac{4\pi}{3}\right)+\cos\left(2\omega t\text{-}\frac{8\pi}{3}\right)\right]\right\}. \tag{2.2}$$

Considering that the sinusoidal terms at twice the mains frequency cancel each other, it can be concluded that the input power of the rectifier is constant, if an LFR performance is guaranteed per phase [2.1]. Hence, validating the previous premise.

The prior literature on the topic of three-phase ac-dc LED drivers focuses on two different solutions, the first one is a single switch flyback [2.2], which is attractive due to the low amount of active components, even though, it presents an efficiency about 80% not suitable for an ac-dc LED driver. And a switched capacitor converter [2.3], which is not able to achieve full diming, includes a high amount of components both active and passive and does not include galvanic isolation. Therefore, the objective is the achievement of a more efficient, compact and fully dimmable ac-dc LED driver without

electrolytic capacitor and able to work in a wide input voltage range in any of the three-phase ac power grid.

2.2 The Delco topology

One of the simplest ways in which a three-phase rectifier can be developed is by means of three ac-dc converters with PFC, which will be defined from this point onward as cells, each connected to each of the phases that comprise the three-phase ac power grid and performing as LFR. This topology was proposed by Delco Electronics in 1979 [2.4], see Fig. 1.1, and at the time had a handful of disadvantages [2.5]:

- The tolerances of the components that comprise the power circuit may vary across the three individual converters. Hence, not being able to achieve a complete removal of the six times the mains frequency harmonic as it has previously studied [2.1]. This is solved nowadays by means of a central control unit or a secondary control loop that ensures that each cell gives the same power to the load [2.6].
- A very low third harmonic component in $i_N(t)$ cannot be maintained without guaranteeing that each cell achieves a conduction angle of more than 150º, which has been solved by means of using cells performing as LFR. This distortion on the input current, translates on a significant ripple component on the current across the LED load.

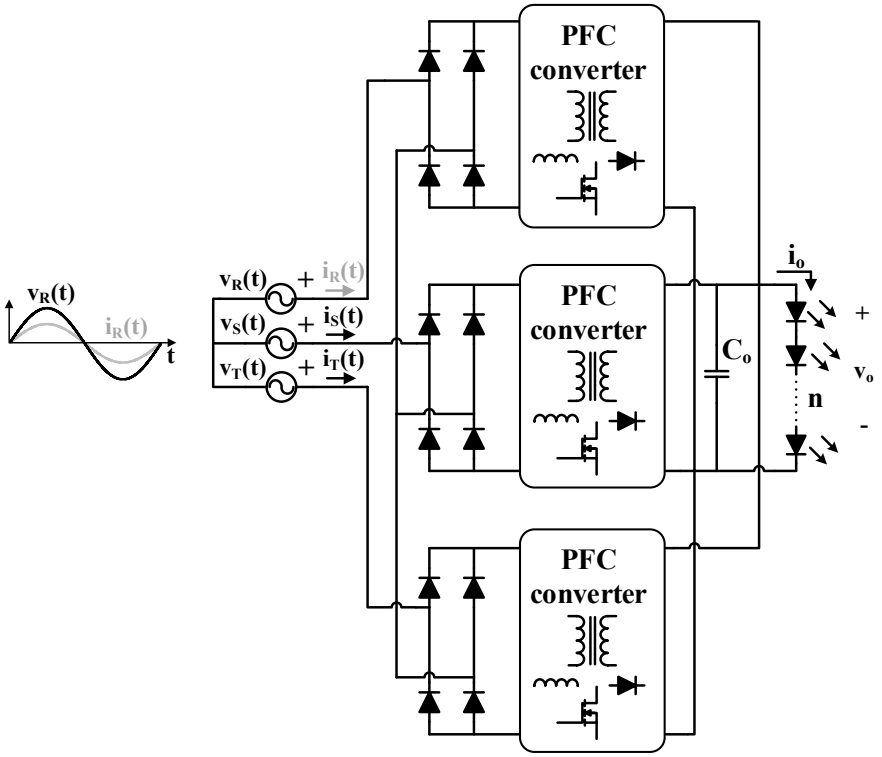


Fig. 2.1. Delco topology driving an LED load.

The main drawback present on this topology, comes from the tolerances which requires a more complex control in order to attain a constant power at the output. That being said, the advancements in capacitor technologies (i.e., MKP or MKT film capacitors) have made possible to use a laxer central control by increasing the output capacitor while guaranteeing an electrolytic capacitor free ac-dc LED driver. However, this capacitor is still large.

The topologies that could make possible the performance of the cells as LFRs have been discussed in Subsection 1.4.1.2.1. In this particular case, the necessity of galvanic isolation to connect the cells in parallel at the output limits the possible choices, which can be divided in single-stage or two-stage solutions. The latter being more complex both in terms of components and taking into consideration the extra control required due to the specific start-up of the Delco topology when using a two-stage approach for the cell in a 3-wire connection [2.7]. Most of the extra control is required to ensure the correct performance as an LFR of the boost converter with PFC (i.e., PFC boost converter) that comprises the first stage of each cell when operating as an LFR with a MBC. The reason is that this method utilizes the phase voltage to conform the sinusoidal reference that needs to be followed by the input current feedback loop, and which can become compromised without a proper start-up. Hence, this premise can be extrapolated to any topology that uses the input voltage as a mean to ensure the LFR performance of the dc-dc converter.

In order to reduce the complexity of the control, the most common cell is based on converters from the buck-boost family that include galvanic isolation working in DCM as a voltage follower. The list of converters that could be considered for cell, includes the flyback converter [2.1], [2.8], the isolated Ćuk converter [2.9] and the isolated SEPIC converter [2.10].

2.2.1 Steady state analysis

Nonetheless, for the analysis that is going to be carried out, the topology used for the cell becomes almost transparent. Considering, all the cells need to perform as LFRs for a proper operation of the Delco topology, then the condition set by (2.1) needs to be satisfied. In particular and considering the definition of LFR, the value of the resistance can be put in terms of control variable, v_c, and a certain constant, K_1, that depends on the design parameters of the converter, yielding the input current of each phase as,

$$i_N(t)=\frac{v_{gp}}{K_1} v_c \sin\left(\omega t\text{-}N\frac{2\pi}{3}\right). \tag{2.3}$$

The two aforementioned parameters, v_c and K_1, are summarized in Table 1.1 for the most common converters which could potentially work as a LFR cell and the dual inductor current-fed push-pull that will be introduced in Chapter 3. As can be seen, for the converters from the buck-boost family v_c depends on a quadratic control variable, represented by the duty cycle, whereas the ones from the boost family depend, when operating in a CCM with MBC, on the output voltage of the output voltage feedback loop, v_a, and when operating in BCM on the time during which the main switch is on (i.e., on time, t_{on}). Particularly for the parameter K_1, it can be seen that for all the converters it has a dependency with the main inductance, L, among other components but for the boost operating in CCM with MBC without using line feedforward , in which it depends on the gain introduced by the input current sensor, G_1. In addition, the Ćuk and SEPIC converters

Table 2.1. LFR parameters of different common dc-dc converters.

	v_c	K_1	L_{eq}
Flyback operating in DCM [2.11]	d^2	$\frac{2L}{T_s}$	-
Isolated Ćuk operating in DCM [2.12]	d^2	$\frac{2L_{eq}}{T_s}$	$\frac{LL_1}{n^2L+L_1}$
Isolated SEPIC operating in DCM [2.12]	d^2	$\frac{2L_{eq}}{T_s}$	$\frac{LL_1}{L+L_1}$
Boost operating in CCM with MBC [2.13]	v_a	G_1	-
Boost operating in BCM [2.14]	t_{on}	$\frac{L}{2}$	-
Dual inductor current-fed push-pull operating in BCM	t_{on}	L	-

depend on their other inductance, L_1, refer to Fig. 1.19 (b) and (c). It should be noted that these figure shows their non-isolated variants, thus the transformer turn ratio, n, needs to be taken into account for the Ćuk converter in accordance to [2.12].

In order to study the operation of the Delco topology, the simplest way is to replace each of the cells for their equivalent LFR model, as seen in Fig. 2.2, and the LED load by its equivalent model, taking into account an LED load comprised of m strings each with n LEDs. From this scenario, it is possible to differentiate between the performance at the input and at the output of this particular ac-dc LED driver. As can be seen, from the point of view of the input, the circuit can be reduced to three resistors connected in a star network to the three-phase power grid, which would guarantee that each phase would demand a sinusoidal current in phase with their respective phase voltages.

Considering the output of the ac-dc LED driver, the problem could be reduced to three parallel power sources connected to the LED load. For that matter, considering (2.2), and rewriting R_{LFR} in terms of K_1 and v_c, gives the average power consumed by the ac-dc LED driver,

$$p_{in}=\frac{3v_{gp}^2}{2K_1}v_c. \tag{2.4}$$

Replacing p_{in} with the output power, p_o, (i.e., considering 100% efficiency) in terms of v_o and r_{eq}, which represents the equivalent resistance of the LED load, and solving the equation, gives the conversion ratio of the ac-dc LED driver as,

$$M=\frac{v_o}{v_{gp}}=\sqrt{\frac{3}{2}\frac{r_{eq}}{K_1}v_c}, \tag{2.5}$$

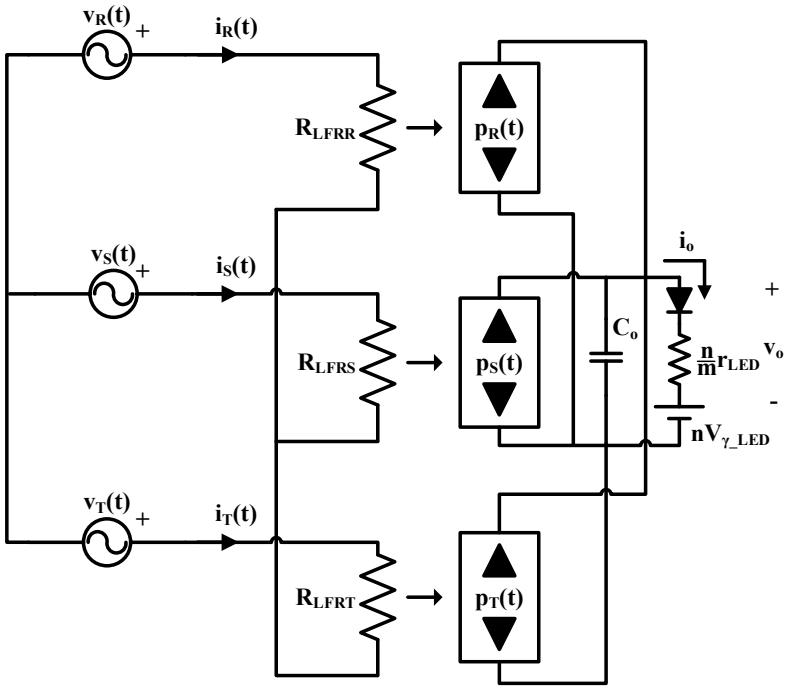


Fig. 2.2. Delco topology simplified by means of the equivalent model of the LFRs and the LED load.

being,

$$r_{eq}=\frac{nV_{\gamma\_LED}}{i_o}+\frac{n}{m}r_{LED}. \tag{2.6}$$

From (2.4), it is also possible to calculate the value which v_c should take for a certain design under a very specific output current of the ac-dc LED driver. Hence, solving for v_c with the same premise under which (2.5) was obtained, renders,

$$v_c=\frac{2}{3}\frac{K_1}{v_{gp}^2}\left(nV_{\gamma\_LED}i_o+\frac{n}{m}r_{LED}i_o^2\right). \tag{2.7}$$

Equation (2.7), shows, as expected, a direct relationship between v_c and i_o. This relationship makes possible the achievement of full dimming by means of lowering the value of v_c, thus adjusting at the same time the current across the LEDs. This fact makes possible the use of an output current feedback loop, hence, addressing one of the issues considered in the prior literature on three-phase ac-dc LED drivers.

2.2.2 Dynamic analysis

The dynamic analysis of the Delco topology needs to be studied in order to ensure a certain current level that guarantees good light quality on the LEDs (i.e., closing the output current feedback loop). This is particularly important, considering the changes that can occur in terms of the forward voltage, due to temperature swings or aging on an LED load.

From Fig. 2.2, the control of the ac-dc LED driver can be simplified as a problem of three power supplies connected in parallel supplying the same load. Many works in the previous literature have addressed the parallelization of power supplies [2.15]-[2.17]. From these works, a quick conclusion can be extracted: the most optimal way to control the power supplies (i.e., the LFR cells) is for each one of them to have their own input current loop to ensure they all demand the same amount of power. If they all receive the same vc, under ideal conditions this control loop over the input power would not be required, however, due to tolerances of the components it is the way to ensure correct power sharing between the power supplies. However, in the case under study, this will complicate the control and increase the cost, which is undesirable for an ac-dc LED driver, as a current sensor needs to be included per cell.

The reason behind this extra control stage is explained due to one of the disadvantages previously introduced for the Delco topology. As was previously stated, the tolerances of the components comprising each cell would cause a component at six times the mains frequency to appear in both output current and voltage. Although, this can seem to be particularly important considering the dependency of K_1 on the main inductor of the cell, in reality it can be easily solved by increasing the size of the output capacitor, without incurring in the use of an electrolytic capacitor. This solution will end up limiting the maximum attainable bandwidth, however, this is not seen as a drawback for an LED load, as changes will not rapidly occur.

Considering the previous facts, the R_{LFR} values of the cells will be considered to be equal in order to simplify the forthcoming analysis. Therefore, the three power sources can be combined into one, see Fig. 2.3, whose value is equal to (2.4). The proposed current feedback loop can be seen in Fig. 2.3, and is based on measuring the average output current and comparing it to a current reference that represents the desired i_o. The error resulting from this comparison will pass through the Current Regulator (CR) block whose output will be isolated and send to each cell in order to control them.

At this point and in order to design CR, it is necessary to obtain the transfer function of the Delco topology using an equivalent analysis to [2.8], by using the average small-signal analysis, presented in [2.18] for single-phase ac-dc converters. Consequently, the starting point for this analysis would be the equation that can be obtained from the circuit depicted in Fig. 2.3, which performs a constant power injection over the LED load with a paralleled capacitor. Hence,

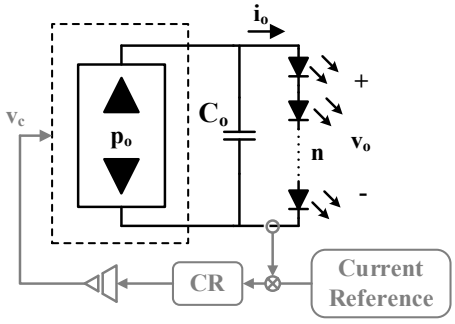


Fig. 2.3. Driving of the Delco topology for LEDs with an output current feeback loop.

$$p_o = p_{in} = C_o v_o \frac{dv_o}{dt} + v_o i_o = \frac{3v_{gp}^2}{2K_1} v_c, \tag{2.8}$$

where $v_o(t)$ can be defined by,

$$v_o = nV_{\gamma\_LED} + i_o \frac{n}{m} r_{LED}. \tag{2.9}$$

Solving (2.4) and (2.9) into (2.8), yields,

$$\begin{aligned} \frac{3v_{gp}^2}{2K_1} v_c = C_o \left(nV_{\gamma\_LED} + i_o \frac{n}{m} r_{LED}\right) \frac{n}{m} r_{LED} \frac{di_o}{dt} \\ + nV_{\gamma\_LED} i_o + i_o^2 \frac{n}{m} r_{LED}. \end{aligned} \tag{2.10}$$

Note that the variation of both v_{gp} and v_c with time is considered in (2.10), in order to study its effects. The first one due to the variation that could occur on the peak voltage of a three-phase ac power grid, considering as a simplification that these variations will occur at the same time on all three phases, and the second one, due to the variation of the control variable in order to adjust its level in accordance to a certain reference following the output feedback loop.

It should be noted that from this point until the end of this subsection, the selected notation will represent constants and variables particularized at a certain operating point in capital letters, and variables describing small-signal ac variations in lowercase with a circumflex accent, taking into account that lowercase variables without the circumflex accent have been used for the static analysis. Then, perturbing (2.10), considering $i_o = I_o + \hat{i}_o$, $v_c = V_c + \hat{v}_c$ and $v_{gp} = V_{gp} + \hat{v}_{gp}$, gives,

$$\begin{aligned} &\frac{3V_{gp}^2}{2K_1}\hat{v}_c + \frac{3V_{gp}^2 V_c}{2K_1} + \frac{3V_{gp}V_c}{K_1}\hat{v}_{gp} + \frac{3V_{gp}}{K_1}\hat{v}_{gp}\hat{v}_c + \frac{V_c}{2K_1}\hat{v}_{gp}^2 + \frac{\hat{v}_c}{2K_1}\hat{v}_{gp}^2 = \\ &C_o \left(nV_{\gamma\_LED} + I_o \frac{n}{m} r_{LED}\right) \frac{n}{m} r_{LED} \frac{d\hat{i}_o}{dt} + \left(nV_{\gamma\_LED} I_o + 2I_o \frac{n}{m} r_{LED}\right) \hat{i}_o \\ &+ C_o \left(nV_{\gamma\_LED} + \hat{i}_o \frac{n}{m} r_{LED}\right) \frac{n}{m} r_{LED} \frac{d\hat{i}_o}{dt} + nV_{\gamma\_LED} I_o \\ &+ I_o^2 \frac{n}{m} r_{LED} + \hat{i}_o^2 \frac{n}{m} r_{LED}. \end{aligned} \tag{2.11}$$

At this point, it is necessary to eliminate the second order and dc terms, attaining,

$$\begin{aligned} \frac{3V_{gp}^2}{2K_1}\hat{v}_c + \frac{3V_{gp}V_c}{K_1}\hat{v}_{gp} = C_o \left(nV_{\gamma\_LED} + I_o \frac{n}{m} r_{LED}\right) \frac{n}{m} r_{LED} \frac{d\hat{i}_o}{dt} \\ + \left(nV_{\gamma\_LED} + 2I_o \frac{n}{m} r_{LED}\right) \hat{i}_o. \end{aligned} \tag{2.12}$$

After performing the Laplace transformation to (2.12), the next expression can be derived,

$$\frac{3V_{gp}^2}{2K_1}\hat{v}_c+\frac{3V_{gp}V_c}{2K_1}\hat{v}_{gp}=C_oV_o\frac{n}{m}r_{LED}s\hat{i}_o+V_o\left(1+R_{eq}\frac{n}{m}r_{LED}\right)\hat{i}_o. \quad (2.13)$$

where V_o and R_{eq} describe the particularization of (2.6) and (2.9) at a certain point of operation, becoming,

$$R_{eq}=\frac{nV_{\gamma\_LED}}{I_o}+\frac{n}{m}r_{LED}, \quad (2.14)$$

and

$$V_o=nV_{\gamma\_LED}+I_o\frac{n}{m}r_{LED}. \quad (2.15)$$

From (2.13), it becomes possible to obtain the required relationships between $\hat{i}_o$ and $\hat{v}_c$, and $\hat{i}_o$ and $\hat{v}_{gp}$, which are necessary to correctly control the LED driver. Therefore solving for the corresponding terms, gives,

$$G_{i_ov_c}(s)=\left.\frac{\hat{i}_o}{\hat{v}_c}\right|_{\hat{v}_{gp}=0}=\frac{3V_{gp}^2}{2K_1V_o}\frac{1}{C_o\frac{n}{m}r_{LED}s+\left(\frac{n}{m}\frac{r_{LED}}{R_{eq}}+1\right)}, \quad (2.16)$$

$$G_{i_ov_{gp}}(s)=\left.\frac{\hat{i}_o}{\hat{v}_{gp}}\right|_{\hat{v}_c=0}=\frac{3V_{gp}V_c}{K_1V_o}\frac{1}{C_o\frac{n}{m}r_{LED}s+\left(\frac{n}{m}\frac{r_{LED}}{R_{eq}}+1\right)}, \quad (2.17)$$

Equations (2.16) and (2.17) conclude the mathematical analysis for any dc-dc converter performing as an LFR. Nonetheless, to attain the correct transfer function for a certain dc-dc converter it is necessary to substitute V_c and $\hat{v}_c$ in accordance to Table 2.2.

Table 2.2. Summarization of V_c and $\hat{v}_c$ for different common dc-dc converters.

	V_c	$\hat{v}_c$
Flyback operating in DCM [2.11]	D^2	$2D\hat{d}$
Isolated Ćuk operating in DCM [2.12]	D^2	$2D\hat{d}$
Isolated SEPIC operating in DCM [2.12]	D^2	$2D\hat{d}$
Boost operating in CCM with MBC [2.13]	V_a	$\hat{v}_a$
Boost operating in BCM [2.14]	T_{on}	$\hat{t}_{on}$
Dual inductor current-fed push-pull operating in BCM	T_{on}	$\hat{t}_{on}$

2.3 Multi-cell ac-dc LED driver based on the three-phase full-wave rectifier

The reason for using the Delco topology in order to attain sinusoidal input currents can be understood due to the limitations of dc-dc converters operating as LFRs in three-phase ac power grids. Unlike the single-phase scenario, in which the connection of an LFR after a full-wave rectifier shapes a sinusoidal input current, the three-phase scenario, see Fig. 2.4, is unable to achieve this feat at the input of each phase. This limitation comes from the intrinsic performance of an LFR that guarantees an input current following the shape of the input voltage, which due to the three-phase full-wave rectifier is far from being sinusoidal as only two diodes are conducting at a time, one from the upper section (i.e. D_1, D_2 or D_3) and one from the lower section (i.e. D_4, D_5 or D_6) of the rectifier. This happens, because in the upper section only the diode whose anode is connected to the highest phase voltage conducts, whereas for the lower section only the diode whose cathode is connected to the lowest phase voltage conducts. Hence, shaping a non-sinusoidal input current in each phase due to the conduction of the diodes, which has a conduction angle of 120º coincidental with the time the diodes dedicated to each phase are conducting. Furthermore, this problem is aggravated the higher the number of phases are, as the conduction angle gets lowered even further. It should be noted that the diodes dedicated for phase R are D_1 and D_4, for phase S are D_2 and D_5, and for phase T are D_3 and D_6.

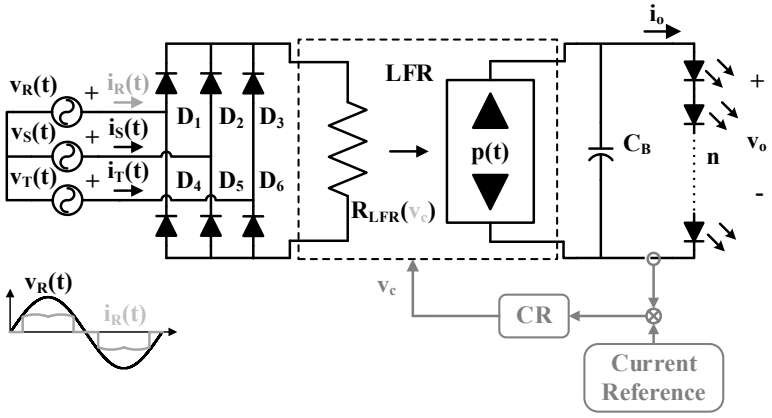


Fig. 2.4. Use of an LFR as an ac-dc LED driver at the output of a full-wave three-phase rectifier.

In order to solve this problem, a multi-cell topology is proposed and depicted in Fig. 2.5, where v_{IN}^{+} and v_{IN}^{-} define the input ports of each cell (i.e., a dc-dc converter working as an LFR) and v_o^{+} and v_o^{-} the output ports, which are connected to the LED load. The concept is based on using an LFR in series with each of the diodes that comprise the three-phase full-wave rectifier, in order to attain the required sinusoidal input waveforms. The explanation for introducing the LFRs in series can be understood when looking at the problem from a circuital point of view, as it is depicted in Fig. 2.6. If there are several voltage sources with different values connected each in series with a diode feeding the same resistive load, see Fig. 2.6 (a), only the diode connected to the highest voltage source will conduct. This scenario is equivalent to the one depicted in Fig. 2.4, which has been shown to be problematic to attain a three-phase ac-dc converter with unity PF. However, if the load is equally distributed among several resistive loads which are then connected

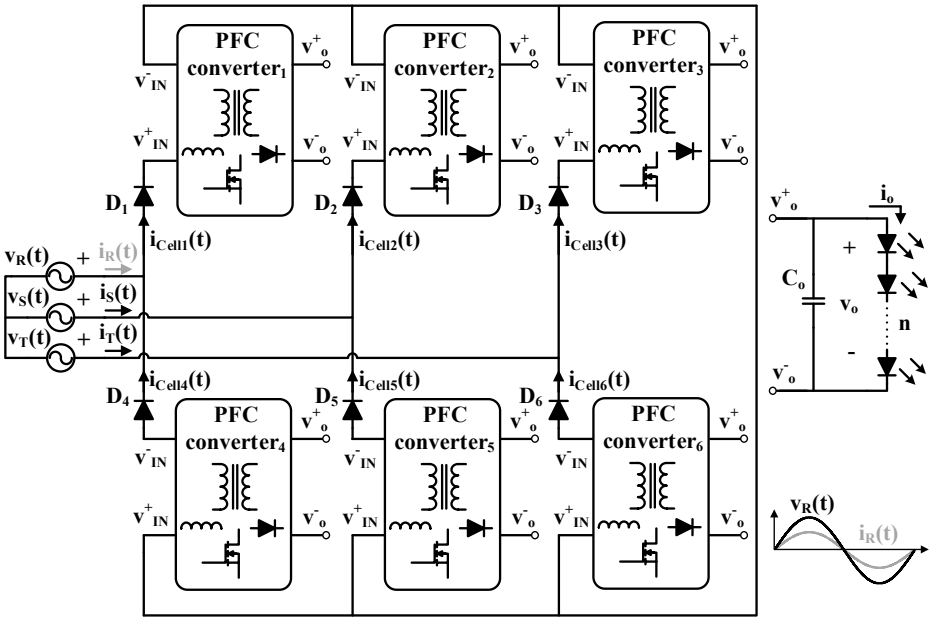
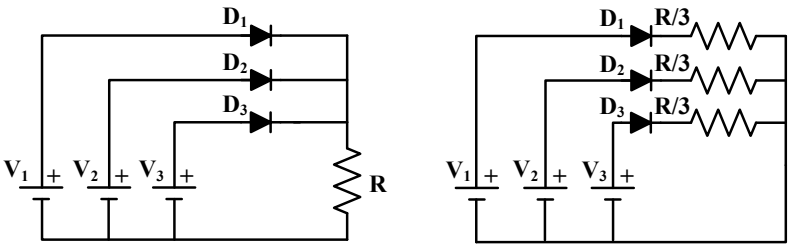


Fig. 2.5. Diagram of the multi-cell three-phase ac-dc LED driver based on the three-phase full-wave rectifier.



(a) (b)

Fig. 2.6. Illustration of voltage sources with different values, each in series with a diode, feeding (a) the same resistive load, and (b) a distributed load.

in series with their respective diode and voltage source, see Fig. 2.6 (b), then all of them will be able to conduct, as each load can be fed independently. In that sense, this scenario is equivalent to the proposed ac-dc LED driver shown in Fig. 2.5, however, having the load distributed will not be of help to eliminate the electrolytic capacitor considering all phases are required to supply the same load. For that matter, the cells will require galvanic isolation, limiting in that sense the potential solution in a similar fashion to the Delco topology, in order to feed the same load with a constant power.

The introduced ac-dc LED driver works similarly to the solution found in [2.19], whose circuit can be seen in Fig. 1.24. (b). This solution based on a single-switch three-phase flyback, requires a coupled inductor in series with each diode of the three-phase full-wave rectifier. Then, taking advantage of the flyback operation in DCM all the transformers can share the same switch to attain an LFR performance, while at the same time having an independent output per phase that is connected in parallel to feed to the

same load. Unlike [2.19] which works specifically for a flyback converter and only the transformers are modularized, the proposed ac-dc LED driver studies the use LFR cells that can be controlled independently adding some degree of freedom to the design. In addition, this independent control enables the power control of each module to reduce the effect of component tolerances, which is unavailable for the three-phase single-switch flyback as they all share the same switch.

Similarly to the analysis carried out for the Delco topology, the first step to simplify the study is replacing the PFC converters of Fig. 2.5 with their equivalent LFR model, and the LED load with its equivalent circuit, see Fig. 2.7. Then, the analysis is simplified from the point of view of the input to studying the conduction of the diodes in order to demonstrate that the multi-cell LED driver based on the full-wave rectifier is able to achieve unity PF at each of the phases, and from the point of view of the output to a problem of parallel power sources feeding the same load.

Starting from the input, and considering that all the LFR cells attain the same value to further simplify the analysis, then the problem is reduced to the aforementioned Fig. 2.6 (b). Hence, there are two diodes and two LFR cells exclusively dedicated to each of the phases. In particular, one diode and one LFR cell are dedicated to the positive values of the input phase voltage, and the other diode and LFR cell for the negative values. The previous statement means that the current demanded by phase R depends on LFR_1 and D_1 for the positive values and on LFR_4 and D_4 for the negative values, by phase S depends on LFR_2 and D_2 for the positive values and on LFR_5 and D_5 for the negative values, and by phase T depends on LFR_3 and D_3 for the positive values and on LFR_6 and D_6 for the negative values. Following this pattern, it is possible to adapt the topology to grids with a higher number of phases (i.e., multiphase grids), by adding a combination of two diodes and two LFR cells per each phase.

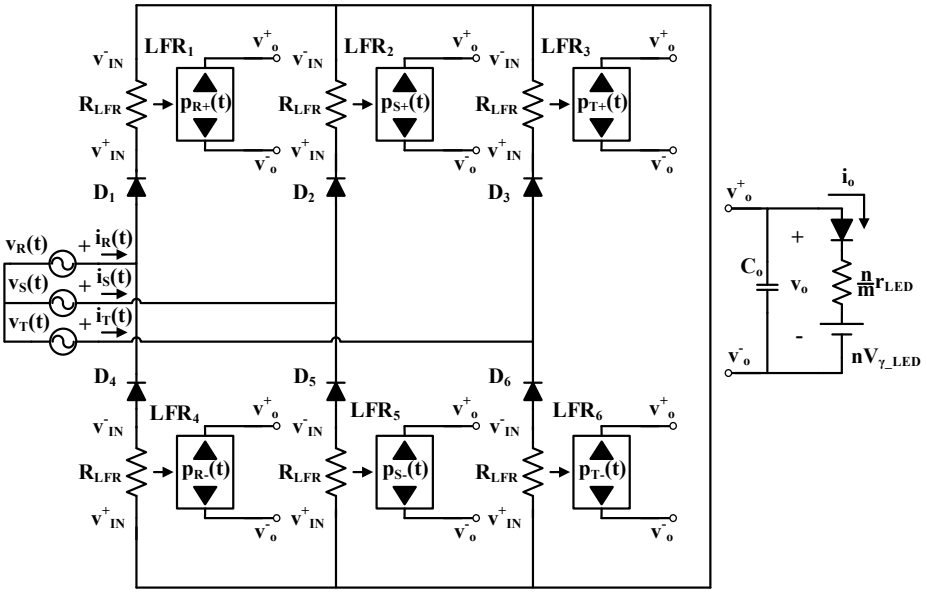


Fig. 2.7. Simplified diagram of the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier.

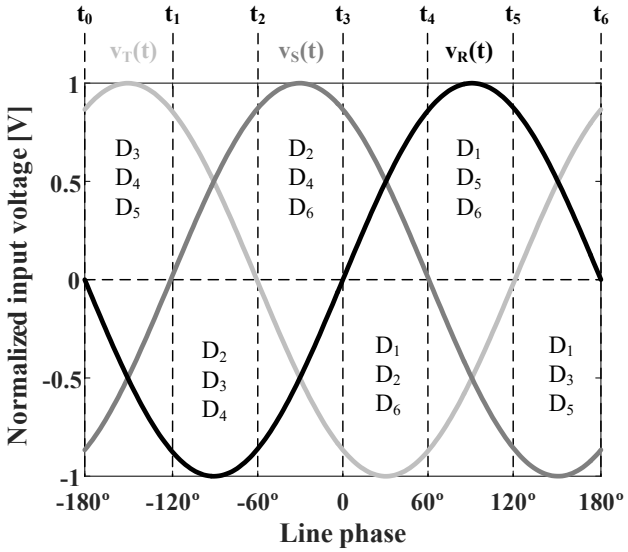


Fig. 2.8. Theoretical conduction of the low frequency diodes depending on the phase voltages, in the multicell ac-dc LED driver based on the full-wave three-phase rectifier.

Considering the introduced operation, and unlike the three-phase full-wave rectifier, where two diodes conduct at the same time, the multi-cell LED driver based on the full-wave rectifier attains conduction angles of 180º by making three diodes conduct at a time due to the distribution of the load. For that matter, Fig. 2.8, summarizes the conduction of the diodes for a whole line period. As can be seen, every 60º there is a phase that swaps between positive and negative causing one diode to stop conducting and enabling another one. Therefore, the topology can be divided into three stages for each of the diodes that comprise the three-phase full-wave rectifier.

As an example, the conduction of D_2 will be studied in detail, which corresponds to the upper diode of phase S. Hence, its conduction coincides with the positive half line cycle of said phase, in accordance to Fig. 2.8 from t_1 to t_4. During this time, there are two other diodes conducting depending on the voltages of the other two phases. From t_1 to t_2, see Fig. 2.9 (a), D_5 has stopped conducting due to phase S going from negative to positive values, causing D_2 to start. From t_2 to t_3, see Fig. 2.9 (b), it is phase T the one that goes from positive to negative causing D_3 to start conducting in detriment of D_6. The last stage from t_3 to t_4, see Fig. 2.9 (c), represents the time at which phase R goes from negative to positive causing D_4 to stop conducting and D_1 to start. This analysis is equivalent to any of the diodes, hence, reaching the simplified operation of the driver in Fig. 2.9 (d). Therefore, the operation is equivalent to Fig. 2.2, sharing both the static and the dynamic analysis carried out before in Section 2.2, for the Delco LED driver, and which will ensure the desired unity PF on any of the input currents for the multi-cell LED driver based on the three-phase full-wave rectifier.

That being said, the differences between the two topologies need to be further discussed. The first difference between them can be understood in terms of how many LF diodes conduct at the same time. In that sense, for the Delco ac-dc LED driver there will be 6 LF diodes conducting, due to single-phase full-wave rectifiers, whereas for the topology under study there will be only 3 LF diodes, as shown in Fig. 2.8 while using

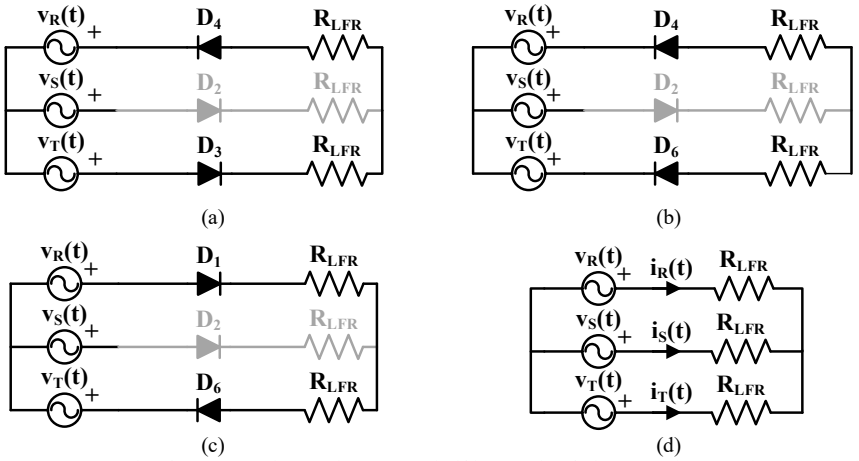


Fig. 2.9. Example of operation during the positive half line cycle of phase S. (a) Equivalent circuit during [t_1, t_2]. (b) Equivalent circuit during [t_2 , t_3]. (c) Equivalent circuit during [t_3 , t_4]. (d) Simplified operation of the driver.

three LFR cells at a time on both of them. This is an improvement as the multi-cell LED driver based on the three-phase full-wave rectifier will incur in less conduction losses than the Delco ac-dc LED driver. However, these advantages comes at the price of almost doubling the amount of components, which increases the cost and lowers the reliability of the solution in comparison to the Delco ac-dc LED driver. Nonetheless, doubling the amount of components is not necessarily bad, as has been seen, each of the LFRs only work during half line cycle, meaning that thermally the performance of each cell will be much better causing the multi-cell LED driver based on the three-phase full-wave rectifier to theoretically scale much better than the Delco ac-dc LED driver. In fact, this thermal improvement can be explained thanks to Fig. 2.10, where the power handled by each of the LFRs is depicted against the line phase, showing that the conduction of the LFRs occur over half line cycle translating in each LFR processing half of the power in comparison to the Delco ac-dc LED driver.

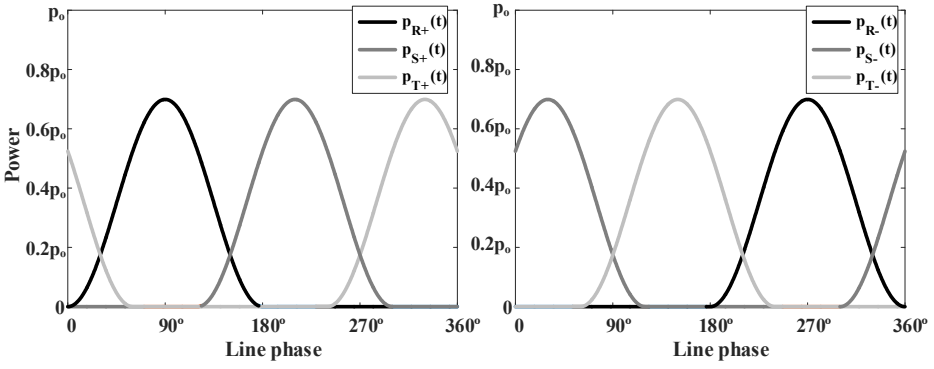


Fig. 2.10. Power handled by each LFR during a whole line cycle in terms of line phase and p_o. (a) Upper section LFRs. (b) Lower section LFRs.

Even though, the amount of components used in a multi-cell converter can be seen as a disadvantage, it can also be leveraged considering that the basic cells are scalable. The scalability is based on modularizing the cells by adding several cells and connecting them in series and/or parallel to achieve a total cell capable of processing higher powers, see Fig. 2.11. In that sense, the issue is guaranteeing an acceptable voltage and current sharing between the several cells that can comprise the total cell which can be achieved with a proper control. This method as any modular converter allows the use of optimized components to further increase the performance of the cells at the cost of increasing the complexity of the central control unit and decreasing the reliability. The aim with this modularization is to attain efficient, compact and robust cells that can be used as the building blocks of the ac-dc LED driver in order to cover a wide range of power.

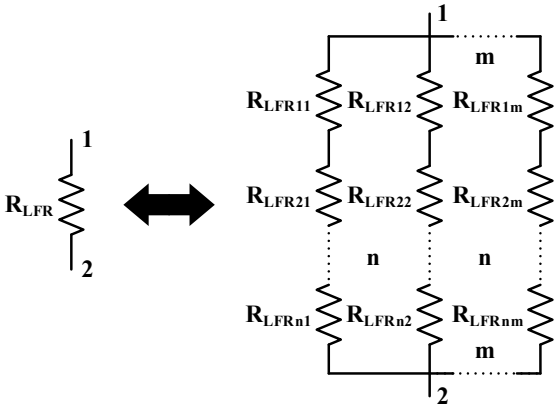


Fig. 2.11. Using several LFR cells to form a cell with higher power capabilities.

2.4 Multi-cell ac-dc LED driver based on summing the light output of each phase

The cells that comprise the two ac-dc LED drivers previously introduced, require galvanic isolation in order to remove the electrolytic capacitor and achieve an acceptable lifespan that complies with ENERGY STAR®. In fact, according to [2.20], for high power luminaires the preferred solution is a two-stage comprised of a PFC boost followed by an isolated dc-dc converter, as stated in Chapter 1. Particularizing this two-stage cell for the Delco ac-dc LED driver, see Fig. 2.12, it should be noted that the only purpose of the second stage is achieving galvanic isolation, hence, its control can be simplified to an electronic transformer with a fixed gain. In that scenario, the PFC converters would be the ones responsible for controlling how much power is given to the LED load. Nonetheless, the amount of components and cost will increase in comparison to a single-stage cell.

In this section the proposal is to completely remove the second stage and distribute the LED load between the phases, see Fig. 2.13. For each of the phases, the behaviour of the cell is equivalent to the single-stage proposed in [2.21] for driving an HV LED load. The main issue is the disposal of the electrolytic capacitor which for the aforementioned solution is based on operating in DCM while injecting a third harmonic component to the current reference, further complicating the control circuitry and hindering the compliance with the IEC 61000-3-2 Class C. Hence, it only fulfills the conditions set for Class D,

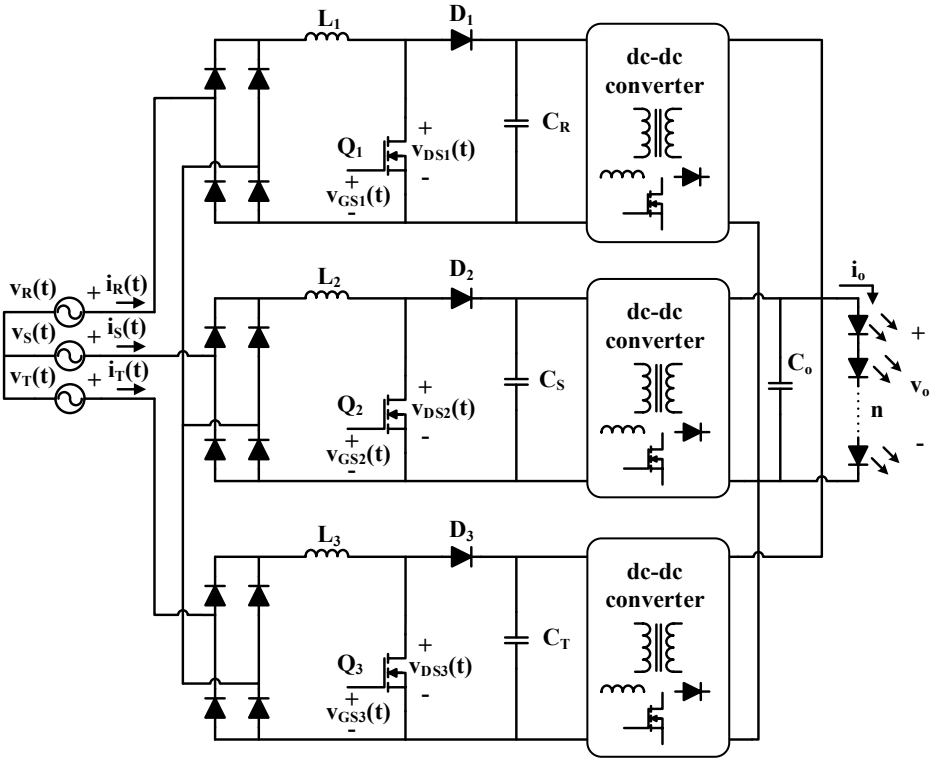


Fig. 2.12. Delco ac-dc LED driver, using a multi-stage approach for each of the cells.

limiting this solution for low power applications (i.e., below 25 W), which is not desirable for ac-dc LED drivers aimed for high power luminaires in a three-phase ac power grid.

Considering the non-pulsation of the three-phase power grid, all the previous drivers were able to dispose of the electrolytic capacitor. In this particular case reducing the size of the output capacitor of each cell (i.e., C_R, C_S or C_T, referred as C_N) to an adequate value will cause the current to not be constant incurring, in a single-phase scenario, into outputting a light with a perceptible flicker [2.22]. However, taking advantage of the light properties, the low frequency component that modulates the light will be cancelled between phases considering the light output of the LED driver as the sum of the light output of the phase and obtaining a theoretically constant light output, method which was used during the Beijing 2008 Summer Olympics in the National Stadium, also known as Bird's nest, with several spotlights each of 1.5 kW and 125,000 lm [2.23].

2.4.1 Analysis in terms of the output capacitance

Even though, the cells are particularized in Fig. 2.13 for PFC boost converters in order to illustrate the removal of the second stage, any LFR is suitable to be working as a cell of the proposed ac-dc LED driver. In fact, from this point onward the PFC boost is going to be replaced with its equivalent LFR model, considering that all of them achieve the same resistive value, and the LED loads with their equivalent circuital model, see Fig. 2.14. As can be seen from the input point of view the behaviour is the same as the previous

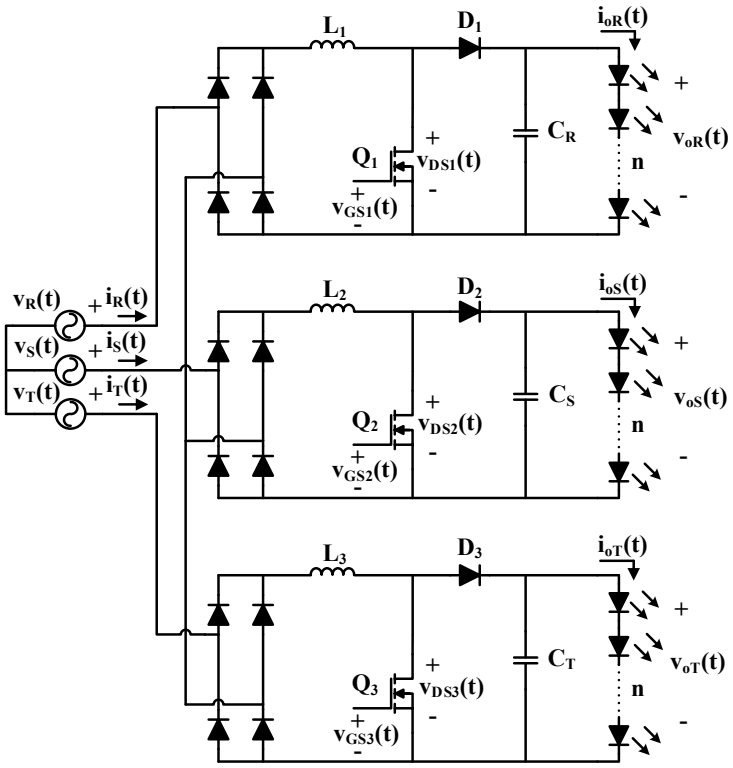


Fig. 2.13. Multi-cell ac-dc LED driver based on summing the light output of each phase.

ac-dc LED drivers, achieving a resistive star configuration that guarantees sinusoidal current waveforms as long as the LFR performance is not compromised. Then, from the point of view of the output, the problem is reduced to an ideal power source feeding both the output capacitor and a string of LEDs connected at the output of each cell.

Taking into account the premise of summing the light output of each cell, the first study carried out is to estimate the theoretical ripple of the low frequency component that modulates the total output luminance (l_o) of the ac-dc LED driver in order to foresee whether an electrolytic free ac-dc LED driver can be achieved. For that matter, $l_o(t)$ will be determined as the sum of the current through each of the LED loads that comprise the LED driver, $i_{oR}(t)$, $i_{oS}(t)$ and $i_{oT}(t)$, in accordance to its proportionality to the light supplied. Hence,

$$l_o(t)=\alpha\left(i_{oR}(t)+i_{oS}(t)+i_{oT}(t)\right), \tag{2.18}$$

where α represents a constant that takes into account the linear relationship between the low frequency modulation of the light and the current provided to the LEDs. It should be noted that the currents across each of the LED loads is pulsating in contrast to the aforementioned ac-dc LED drivers where the output current (i.e., i_o) was constant. Even though, each of the PFC boost will be driving an LED load comprised of one string of

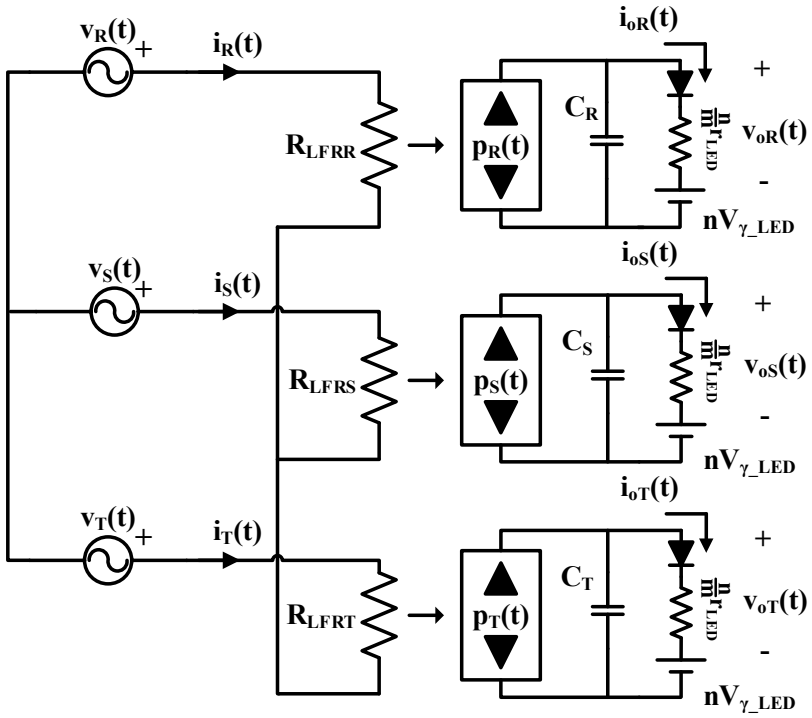


Fig. 2.14. Simplified diagram of the multi-cell LED driver based on summing the light output of each cell.

LEDs, thus working as the post-regulator stage, the forthcoming analysis will consider a matrix LED load.

2.4.1.1 Study without a capacitor at the output of the cells

This first study will shed some light on whether it is feasible to achieve a non-flicker performance when driving the LEDs with pulsating currents at double the mains frequency. The current through the LEDs of each phase can be obtained by analyzing and solving a simple circuit of a power source in parallel with an LED load. Hence,

$$p_N(t)=i_{oN}^2(t)nr_{LED}+i_{oN}(t)\frac{n}{m}V_{\gamma\_LED}. \tag{2.19}$$

Then, solving for $i_{oN}(t)$ in (2.19), yields,

$$i_{oN}(t)=\frac{-nV_{\gamma\_LED}+\sqrt{n^2V_{\gamma\_LED}^2+4\frac{n}{m}r_{LED}p_N(t)}}{2\frac{n}{m}r_{LED}}, \tag{2.20}$$

where a lossless LFR performance is considered, defining the instantaneous input power from each phase, $p_N(t)$, as,

$$p_N(t)=\frac{v_{gp}^2}{R_{LFR}}\sin^2\left(\omega t-N\frac{2\pi}{3}\right)=2p_N\sin^2\left(\omega t-N\frac{2\pi}{3}\right). \quad (2.21)$$

where, p_N is the average power consumed by each phase.

After, reaching the mathematical expression of $i_{oN}(t)$, it is possible to combine (2.18) and (2.20) to obtain $l_o(t)$. However, this is not a practical expression to draw conclusions from, unless it is processed by a numerical computing environment. In order to understand the dependencies of (2.20) it will be normalized, as follows,

$$i_{oN,norm}(t)=\frac{I_{base}}{2}\left(-1+\sqrt{1+8\frac{p_{LED}}{P_{base}}\sin^2\left(\omega t-N\frac{2\pi}{3}\right)}\right), \quad (2.22)$$

where, the newly defined parameters are,

$$I_{base}=\frac{V_{\gamma\_LED}}{r_{LED}}, \quad (2.23)$$

$$p_{LED}=\frac{p_N}{nm}, \quad (2.24)$$

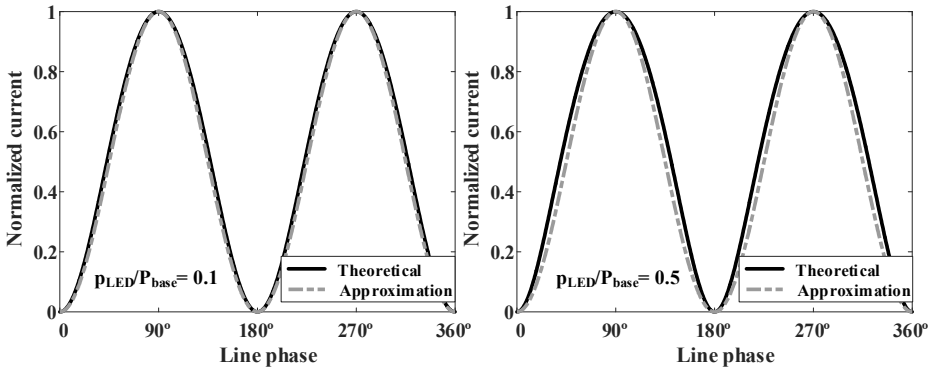
and,

$$P_{base}=V_{\gamma\_LED}I_{base}. \quad (2.25)$$

It is important to note that p_{LED} defines the power of one of the LEDs that comprise the LED load, taking into consideration that ideally all the LEDs process the same amount of power. In addition, the ratio between p_{LED} and P_{base}, which as can be seen defines the maximum amplitude of the current versus time, is defined in terms of the parameters that can be found in the LED datasheet. Hence, the values that this ratio can take are limited in accordance to the current LED technology, see Table 2.3 where p_{LED} is selected as the maximum power attainable for that particular LED. This table summarizes that the trend for the newer LEDs is minimizing the aforementioned ratio, being 0.2 in the worst case

Table 2.3. Evaluation of different commercial LEDs to attain their maximum value of the ratio p_{LED}/P_{base}

	P_{LED} [W]	V_{γ_LED}[V]	r_{LED} [Ω]	Max{p_{LED}/P_{base}}
Seoul Semi W42180 [2.24] Obsolete	2	2.5	0.625	0.2
Luxeon Rebel ES [2.25]	2.5	2.6	0.3	0.11
Luxeon 5050 [2.26]	2.5	21	25	0.14
Cree XLAMP XB-D [2.27]	2.5	2.7	0.4	0.14
OSRAM OSLON SSL 150 [2.28]	2.5	2.8	0.57	0.18



(a) *(b)*

Fig. 2.15. Comparison between the theoretical, (2.22), and the approximated, (2.26), normalized current for different values of the ratio p_{LED}/P_{base}. (a) p_{LED}/P_{base} = 0.1. (b) p_{LED}/P_{base} = 0.5.

scenario for an obsolete LED. Then, it is safe to set the maximum limit of this parameter to 0.5 taking into consideration a safety factor.

Under this assumption, and considering the periodicity of (2.22), it is possible to empirically approximate this function as,

$$i_{oN,norm}(t) \cong \frac{I_{base}}{2}\left[\left(\sqrt{1+8\frac{p_{LED}}{P_{base}}}-1\right)\left(\frac{1}{2}-\frac{1}{2}\cos\left(2\omega t-N\frac{2\pi}{3}\right)\right)\right], \tag{2.26}$$

taking into account the waveform it describes for values of p_{LED}/P_{base} lesser than 0.5 can be approximated for a constant value plus a sinusoidal component at twice the line frequency. In order to justify the aforementioned approximation (2.22) and (2.26) are compared in Fig. 2.15 for two different values of p_{LED}/P_{base}. As can be seen, for the maximum value of p_{LED}/P_{base}, previously defined, the approximation is not able to perfectly reproduce the middle values of the waveform, however, the closer this parameter gets to zero, the better the approximation is. Even so, it is safe to assume the use of the approximation within the defined limits for commercial LEDs.

By combining (2.18) and (2.26), it is possible to obtain the output luminance of the LED driver as,

$$l_{o,norm} \cong \frac{3\alpha I_{base}}{4}\left(\sqrt{1+8\frac{p_{LED}}{P_{base}}}-1\right), \tag{2.27}$$

taking into account that in a balanced three-phase power grid the components at double the line frequency cancel each other.

The approximation gets rid of a component at six times the line frequency which for the range of values set for p_{LED}/P_{base} ratio can be considered negligible, see Fig. 2.16. In this figure, (2.27) is compared to the theoretical luminance output, obtained from combining (2.18) and (2.20). As expected, the lower the value of p_{LED}/P_{base} the lower the ripple at six times the mains frequency actually is.

In addition, considering the theoretical waveform depicted in Fig. 2.16, obtained from combining (2.18) and (2.20), it is possible to obtain an analytical waveform of the output luminance, by obtaining the Fourier series coefficients under the ideal consideration of each phase outputting the exact same light out of each of the LED loads. Hence, the next expression for $l_o(t)$ can be obtained,

$$l_o(t)=\frac{L_{max}+L_{min}}{2}-\frac{L_{max}-L_{min}}{2}\cos(6\omega t), \tag{2.28}$$

where,

$$L_{min}=\alpha\frac{-nV_{\gamma\_LED}+\sqrt{n^2V_{\gamma\_LED}^2+6\frac{n}{m}r_{LED}p_N}}{\frac{n}{m}r_{LED}}, \tag{2.29}$$

and

$$\begin{aligned}L_{max}=&\alpha\frac{-nV_{\gamma\_LED}+\sqrt{n^2V_{\gamma\_LED}^2+8\frac{n}{m}r_{LED}p_N}}{2\frac{n}{m}r_{LED}}\\&+\alpha\frac{-nV_{\gamma\_LED}+\sqrt{n^2V_{\gamma\_LED}^2+2\frac{n}{m}r_{LED}p_N}}{\frac{n}{m}r_{LED}},\end{aligned} \tag{2.30}$$

are the maximum and minimum luminance of the total LED load, which are obtained from combining (2.18) and (2.20), and solving $\omega t = 0$ and $\omega t = \pi/2$, respectively.

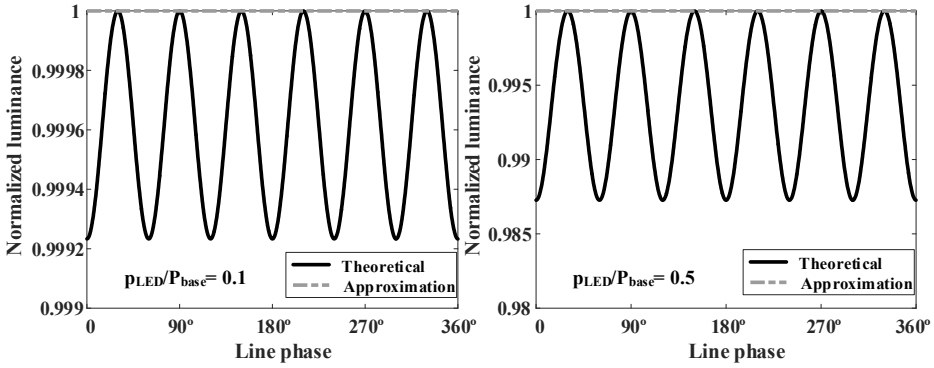


Fig. 2.16. Comparison between the theoretical and the approximated normalized output luminance for different values of the ratio p_{LED}/P_{base}. (a) $p_{LED}/P_{base} = 0.1$. (b) $p_{LED}/P_{base} = 0.5$.

In (2.28), $l_o(t)$ is defined by a dc component and a sinusoidal component at six times the mains frequency. This is the expression to be used for values p_{LED}/P_{base} higher than 0.5, and whose sinusoidal components needs to be studied in order to be able to guarantee a flicker free performance under the aforementioned conditions. Nonetheless, current LED technology ensures p_{LED}/P_{base} lower than 0.5, thus, rendering a constant light in accordance to (2.27).

In summary, this study foresees that under ideal conditions, an LFR without an output capacitor feeding an LED load, would supply, as expected, the LED load with a current pulsating at twice the line frequency between zero and a certain maximum current. Particularizing for the three-phase scenario, it is possible to attain a constant output luminance able to comply with the flicker regulation. However, the biggest disadvantage of this ac-dc LED driver comes in terms of the maximum current values that the LEDs will need to withstand due to the current pulsation, which will cause the LEDs to be oversized or duplicated in order to be able to handle it.

2.4.1.2 Study with a capacitor at the output of the cells

The aim of this section is to solve the aforementioned disadvantage, (i.e., high current ripple across the LED load) by adding a capacitor in parallel with the LED load at the output of the cells. This capacitor needs to fulfill two conditions, it needs to have a big enough capacitance to reduce the output current ripple, but have a small enough capacitance in order to have an electrolytic free ac-dc LED driver.

The study can be carried out in a similar fashion to the previous one. However, it is required to start over the mathematical analysis as the condition set in (2.19) is no longer correct due to the introduction in the circuit of an output capacitor. Hence,

$$p_N(t)=C_N v_{oN}(t)\frac{dv_{oN}(t)}{dt}+v_{oN}(t)i_{oN}(t), \tag{2.31}$$

where $v_{oN}(t)$ can be defined as,

$$v_{oN}(t)=nV_{\gamma\_LED}+i_{oN}(t)\frac{n}{m}r_{LED}. \tag{2.32}$$

Similarly, the next step is solving for $i_{oN}(t)$ in (2.31), to obtain its mathematical expression. However, (2.31) is a complex differential equation that requires knowing beforehand the mathematical expression of its solution. Fortunately, it is a well-known fact that the output current of a PFC converters follows a sinusoidal waveform at twice the line frequency with a certain dc level, in which case,

$$i_{oN}(t)=i_{ac}\sin\left(2\omega t-\varphi-\frac{2\pi}{3}N\right)+i_{dc}, \tag{2.33}$$

where i_{ac} is the peak value of the ac component, i_{dc} is the dc level of the output current and φ represents a certain phase delay.

It becomes obvious at this point that the forthcoming analysis for one of the phases, will be the same for the other two. Therefore, phase R will be the one to be studied, becoming this study equivalent for S and T.

Substituting (2.21) and (2.33) into (2.31) sets the starting point to attain the expressions of the three aforementioned parameters (i.e., i_{ac}, i_{dc} and φ) that define $i_{oN}(t)$. Hence, the next expression can be yielded,

$$\begin{aligned}2p_R\sin^2(\omega t) &= a_1 i_{ac}\cos(2\omega t-\varphi)+a_2 i_{ac}\sin(2\omega t-\varphi)\\ &+\left(\frac{i_{ac}^2}{2}+i_{dc}^2\right)\frac{n}{m}r_{LED}+i_{dc}nV_{\gamma\_LED},\end{aligned} \tag{2.34}$$

where the parameters a_1 and a_2 are defined by,

$$a_1=C_N n r_{LED} 2\omega \left(\frac{n}{m} r_{LED} i_{dc}+nV_{\gamma\_LED}\right), \tag{2.35}$$

$$a_2=\left(2\frac{n}{m} r_{LED} i_{dc}+nV_{\gamma\_LED}\right). \tag{2.36}$$

Equation (2.34) is obtained after removing the components at four times the line frequency, which are considered to be negligible, and considering that the LFR cells are lossless (i.e., $p_N = p_o$). Grouping the components of (2.34) in terms of dc and sinusoidal components at twice the line frequency gives,

$$p_R=\left(\frac{i_{ac}^2}{2}+i_{dc}^2\right)\frac{n}{m} r_{LED}+i_{dc} nV_{\gamma\_LED}\,, \tag{2.37}$$

and

$$-p_R \cos(2\omega t) = a_1 i_{ac}\cos(2\omega t-\varphi) + a_2 i_{ac}\sin(2\omega t-\varphi)\,. \tag{2.38}$$

At this point the system defined by (2.37) and (2.38) needs to be solved, unfortunately, this system of two equations contains three unknown variables, which further complicates obtaining the solutions. In order to attain a useful model from an engineering perspective, a simplification can be made taking advantage of having an LED load, which is removing i_{ac} from (2.37). This is a fine approximation that dramatically decreases the mathematical complexity of both the analysis and the expressions of the required parameters. In fact, this approximation can be performed considering that the variation in terms of output voltage produced by i_{ac} in comparison to nV_{γ_LED} and i_{dc} can be considered negligible. In addition, taking into account that the maximum achievable value of i_{ac} is i_{dc}, which is obtained in the previous scenario (i.e., Subsection 2.4.1.1) without an output capacitor, then the impact of removing this term will be higher the lower the output capacitance is. Under this assumption, i_{dc} can be easily obtained from (2.37) by solving a second degree equation, yielding,

$$i_{dc}=\frac{-nV_{\gamma\_LED}+\sqrt{n^2V_{\gamma\_LED}^2+4\frac{n}{m} r_{LED} p_R}}{2\frac{n}{m} r_{LED}}\,. \tag{2.39}$$

After obtaining i_{dc}, it is now possible to solve (2.38) for the remaining parameters. This equation can be simply tackled by applying wave superposition theory, which is widely used in other fields of study [2.29], reducing the problem to the sum of two plane waves with different amplitudes. This sum gives a sinusoidal waveform with a different amplitude and phase than the originals, thus (2.38) can be rewritten as,

$$-p_R \cos(2\omega t) = i_{ac}\sqrt{a_1^2+a_2^2}\cos\left(2\omega t-\varphi+\tan^{-1}\left(\frac{-a_2}{a_1}\right)\right). \tag{2.40}$$

Then, solving for i_{ac} and φ in (2.40) gives,

$$i_{ac}=\frac{-p_R}{\sqrt{a_1^2+a_2^2}}\ , \tag{2.41}$$

$$\varphi=\tan^{-1}\left(\frac{-a_2}{a_1}\right)\ . \tag{2.42}$$

Knowing the mathematical expressions of the required parameters, it is possible to obtain a relationship between the required output capacitance for a certain peak-to-peak current ripple (Δi_{CN}), as,

$$C_N=\frac{1}{\frac{n}{m}r_{LED}\left(\frac{n}{m}r_{LED}i_{dc}+nV_{\gamma\_LED}\right)2\omega}\sqrt{\frac{p_N^2}{4i_{dc}^2\Delta i_{CN}^2}-a_2^2}. \tag{2.43}$$

At this point, the output capacitance can be obtained, and it seems that the analysis has ended, however, it becomes necessary to study the variation of $i_{oN}(t)$ in terms of the aforementioned parameters (i.e., i_{ac}, i_{dc} and φ) to foresee the feasibility of reducing enough the ripple by utilizing low capacitance values at the output of each cell. For that matter, the expression of $i_{oN}(t)$ is going to be normalized.

The normalization is tackled by solving the generalized form for any of the phases of (2.35) and (2.36) into (2.41), as a first step, yielding,

$$i_{ac}=\frac{-p_N}{\sqrt{k_n^2\left(\frac{n}{m}r_{LED}i_{dc}+nV_{\gamma\_LED}\right)^2+\left(2\frac{n}{m}r_{LED}i_{dc}+nV_{\gamma\_LED}\right)^2}}\ , \tag{2.44}$$

where the dimensionless parameter k_n is defined by,

$$k_n=2\omega C_N\frac{n}{m}r_{LED}\ . \tag{2.45}$$

Factorizing $\frac{n}{m}r_{LED}i_{dc}$ in (2.44) yields,

$$i_{ac}=\frac{-p_N}{\frac{n}{m}r_{LED}i_{dc}\sqrt{k_n^2(i_n+1)^2+(2i_n+1)^2}}\ , \tag{2.46}$$

where the dimensionless parameter i_n is defined by,

$$i_n=\frac{i_{dc}}{i_{base}}. \tag{2.47}$$

Similarly to the ratio p_{LED}/P_{base}, introduced in the previous subsection, i_n is also a parameter dependent on the LED technology. In fact, if numerator and denominator of (2.47) are both multiplied by $nV_{\gamma\_LED,}$ the expression can approximated for the aforementioned ratio under the assumption that p_N can be considered to almost equal to nV_{γ_LED} multiplied by i_{dc}. Hence, i_n can be limited in the same way the ratio p_{LED}/P_{base} is (i.e., between 0 and 0.5).

Equation (2.37) can also be expressed in terms of i_n as,

$$p_N=i_{dc}^2\frac{n}{m}r_{LED}(1+i_n), \tag{2.48}$$

considering the previous approximation applied to it.

Then, combining (2.46) and (2.48) yields,

$$i_{ac,norm}i_{dc}=\frac{-i_{dc}(i_n+1)}{\sqrt{(2i_n+1)^2+k_n^2(i_n+1)^2}}. \tag{2.49}$$

Following the same principle, it is also possible to normalize (2.42), attaining,

$$\varphi_{norm}=\tan^{-1}\left(\frac{-(2i_n+1)}{k_n(i_n+1)}\right). \tag{2.50}$$

The next step in this analysis is factorizing (2.33) in terms of i_{dc}, yielding,

$$i_{oN}(t)=i_{dc}\left[i_{ac,norm}\sin\left(2\omega t-\varphi_{norm}-\frac{2\pi}{3}N\right)+1\right]. \tag{2.51}$$

Then solving into it both (2.49) and (2.50), gives the normalized expression of $i_{oN}(t)$ as,

$$i_{oN,norm}(t)=\left[\frac{(i_n+1)}{\sqrt{(2i_n+1)^2+k_n^2(i_n+1)^2}}\sin\left(2\omega t-\tan^{-1}\left(\frac{-(2i_n+1)}{k_n(i_n+1)}\right)-\frac{2\pi}{3}N\right)+1\right]. \tag{2.52}$$

The mathematical study carried out, which was particularized for phase R, can be used for any of the phases, and as such, (2.52) gives at a glance the variables on which the output current of an LFR cell depend. Hence, it is possible to study the impact of varying k_n, which linearly varies with the output capacitance, and i_n. On the one hand, Fig. 2.17 (a) and (b) show the normalized output current when varying the aforementioned variables, showing that the output current ripple increases as k_n decreases, which means that the ripple, as expected, increases as the output capacitance decreases. On the other hand, it also shows that i_n does not have an actual impact on the analysis, considering the lower i_n used as a feasible attainable value for the newer LEDs on the market (i.e., $i_n = 0$), and the highest considering obsolete LEDs (i.e., $i_n = 0.25$).

In summary, this analysis shows that it is possible to diminish the ripple to a certain extent without using an electrolytic capacitor, likewise, it is necessary to foresee under this conditions whether a constant luminance output of the driver is obtained. Then, substituting (2.52) into (2.18) gives,

$$l_o(t)=\alpha 3 i_{dc}, \tag{2.53}$$

taking into account that, again, the sinusoidal components at twice the line frequency in a balanced three-phase power grid cancel each other. Thus, it can be concluded that in this scenario a constant output luminance can be obtained independently of the value of the output capacitor.

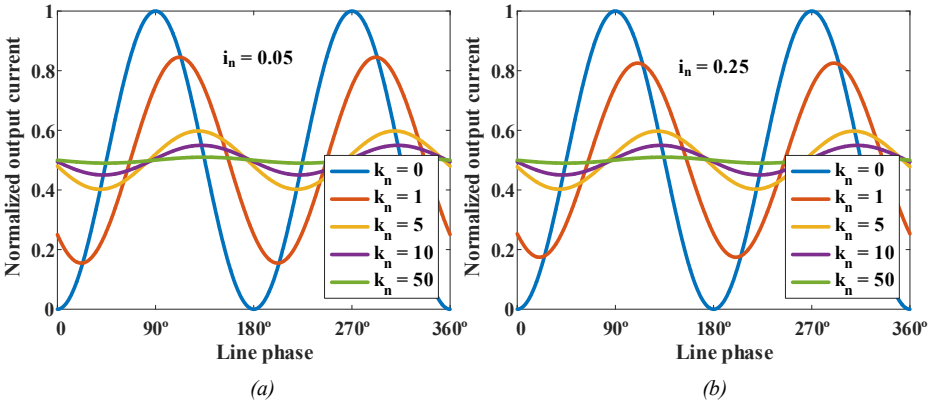


Fig. 2.17. Normalized output current versus line phase in terms of k_n for (a) i_n equal to 0.05 and (b) i_n equal to 0.25.

2.4.2 Limits between CCM and DCM

The higher ripple allowed at the output of each of the cells, both in voltage and current, does not correspond with the conventional operation of a PFC converter, in which the voltage and current are to be as constant as possible. Under the last assumption, the limits between CCM and DCM have been already studied in [2.30], hence, it is required to study the limits between CCM and DCM under high ripple conditions. In fact, this study proves to be key in order to correctly design and select the magnetic component of the LFR cells.

The importance of having a correctly designed inductor can be understood to reduce size and weight of the inductor, and thus of the ac-dc LED driver, but it is also key to ensure the correct operation of the LFR cells. For example in the case of a PFC boost, which as has already been explained can perform as an LFR cell under several operating conditions [2.14], then operation needs to be guaranteed in CCM: to diminish THD under a MBC [2.13], for one cycle control [2.31], non-linear carrier control [2.32], [2.33] or voltage ramp compensation control [2.34]. In addition, operation in DCM needs to be guaranteed on a PFC boost converter for a voltage-follower control, although it requires a high conversion ratio to achieve almost unity PF [2.35]. For that matter the first analysis to be carried out will be considering the LFR cell operating under fixed switching frequency. The other scenario analyzed in this section includes the LFR cell operating with variable switching frequency and constant on time, control under which a PFC boost is able to operate in BCM.

2.4.2.1 Fixed switching frequency

Following the analysis, similarly to [2.30], the first parameter that needs to be calculated is the voltage conversion ratio in terms of the line phase, which can be defined by relating the input and output voltages for phase R as,

$$m(\omega t)=\frac{nV_{\gamma\_LED}+i_{dc}\frac{n}{m}r_{LED}}{v_{gp}|\sin(\omega t)|}+\frac{i_{ac}\sin(2\omega t-\varphi)\frac{n}{m}r_{LED}}{v_{gp}|\sin(\omega t)|}, \tag{2.54}$$

considering as the input voltage of the LFR cell a rectified sinusoidal waveform and, again, being equivalent for the phases S and T. Moreover, in (2.54), the first term

represents the traditional component studied in [2.30], whereas the second term represents the ripple.

Then, the analysis requires obtaining the load as it is actually "seen" by the converter, which is defined by,

$$r(\omega t)=\frac{\left(nV_{\gamma\_LED}+\left(i_{ac}\sin(2\omega t-\varphi)+i_{dc}\right)\frac{n}{m}r_{LED}\right)^2}{2p_R\sin^2(\omega t)}. \tag{2.55}$$

The limits between CCM and DCM in an LFR can be studied similarly to any dc-dc converter by obtaining the mathematical expressions of $k(\omega t)$ and $k_{crit}(\omega t)$, which in accordance to [2.36], set the operating conditions for the different modes as,

$$\text{CCM: } k(\omega t) > k_{crit}(\omega t), \tag{2.56}$$

$$\text{DCM: } k(\omega t) < k_{crit}(\omega t), \tag{2.57}$$

$$\text{BCM: } k(\omega t) = k_{crit}(\omega t). \tag{2.58}$$

Although, the mathematical expression that defines $k(\omega t)$, which can be defined as,

$$k(\omega t)=\frac{2L_1}{T_s r(\omega t)}, \tag{2.59}$$

is the same for any dc-dc converter, $k_{crit}(\omega t)$ changes significantly depending on the dc-dc converter used as an LFR, see Table 2.4 for the basic dc-dc converters. Hence, from this point onward the analysis will be particularized for the boost converter by selecting its $k_{crit}(\omega t)$, taking into account it is massively used for this specific application. Nonetheless, the analysis can be extrapolated to any other converter.

Table 2.4. $k_{crit}(\omega t)$ for the basic dc-dc converters [2.30], [2.36].

	Buck	Boost	Buck-boost
$k_{crit}(\omega t)$	$1-m(\omega t)$	$\frac{m(\omega t)-1}{m(\omega t)^3}$	$\frac{1}{\left(1-m(\omega t)\right)^2}$

At this point it is possible to obtain the limits between modes under the presented conditions. Therefore, solving (2.59) and $k_{crit}(\omega t)$ of the boost converter into (2.56), yields,

$$\frac{2L_1}{T_s r(\omega t)} > \frac{m(\omega t)-1}{m(\omega t)^3}, \tag{2.60}$$

which establishes the condition to fulfill CCM operation. Then, substituting (2.54) and (2.55) into (2.60) gives,

$$\frac{4L_1 p_R \sin^2(\omega t)}{T_s\left(nV_{\gamma\_LED}+\left(i_{ac}\sin(2\omega t-\varphi)+i_{dc}\right)\frac{n}{m}r_{LED}\right)^2} > \frac{nV_{\gamma\_LED}+\left(i_{ac}\sin(2\omega t-\varphi)+i_{dc}\right)\frac{n}{m}r_{LED}-v_{gp}|\sin(\omega t)|}{\left(nV_{\gamma\_LED}+\left(i_{ac}\sin(2\omega t-\varphi)+i_{dc}\right)\frac{n}{m}r_{LED}\right)^3}\left(v_{gp}|\sin(\omega t)|\right)^2. \quad (2.61)$$

Grouping terms and simplifying (2.61) yields,

$$\frac{4L_1 p_R}{T_s v_{gp}^2} > \max\{k_2(\omega t)\}, \quad (2.62)$$

where,

$$k_2(\omega t)=\frac{v_{oN}(t)-v_{gp}|\sin(\omega t)|}{v_{oN}(t)}. \quad (2.63)$$

Maximizing $k_2(\omega t)$ in (2.62) gives the condition that guarantees CCM operation for the whole line period. This function can be easily maximized taking into account that its maximum exists when the sine reaches the zero value, then (2.62) can be rewritten as,

$$\frac{4L_1 p_R}{T_s v_{gp}^2} > 1. \quad (2.64)$$

Therefore, by solving for L_1 in (2.64), the inductor that guarantees CCM operation can be calculated as,

$$L_1 > \frac{T_s v_{gp}^2}{4p_N}. \quad (2.65)$$

In a similar fashion, to work in DCM for the whole line period, (2.57) needs to be satisfied. Thus,

$$\frac{4L_1 p_R}{T_s v_{gp}^2} < \min\{k_2(\omega t)\}. \quad (2.66)$$

Unfortunately, the minimization of $k_2(\omega t)$ is not trivial and the function needs to be studied either graphically or numerically. In that sense, to alleviate the study, (2.63) will be normalized, taking as a first step solving (2.32) and then (2.52), which gives,

$$k_2(\omega t)=1-\frac{v_{gp}|\sin(\omega t)|}{nV_{\gamma\_LED}+i_{dc}\left[\frac{i_{ac,norm}}{i_{dc}}\sin\left(2\omega t-\varphi_{norm}\right)+1\right]\frac{n}{m}r_{LED}}. \quad (2.67)$$

Next, factorizing the denominator in terms of nV_{γ_LED}, yields,

$$k_{2,norm}(\omega t)=1-\frac{v_{gn}|\sin(\omega t)|}{1+i_n\left[\frac{i_{ac,norm}}{i_{dc}}\sin\left(2\omega t-\varphi_{norm}\right)+1\right]}, \quad (2.68)$$

where,

$$v_{gn}=\frac{v_{gp}}{nV_{\gamma\_LED}}. \tag{2.69}$$

It is this dependency of $k_2(\omega t)$ on parameters that are related to the output capacitance (i.e. $i_{ac,norm}$ and φ_{norm}), which causes the difficulty of obtaining an analytical solution for its minimization. This fact marks an important difference for a DCM design when compared to the solution found in literature [2.30] with constant output voltages and currents. In fact, these changes will be seen later in this document, during the discussion of Fig. 2.18.

From (2.68), it is possible to derive a generic function for any of the phases as,

$$k_{2,norm,N}(\omega t)=1-\frac{v_{gn}\left|\sin\left(\omega t-\frac{2\pi}{3}N\right)\right|}{1+i_n\left[\frac{i_{ac,norm}}{i_{dc}}\sin\left(2\omega t-\varphi_{norm}-\frac{2\pi}{3}N\right)+1\right]}, \tag{2.70}$$

2.4.2.2 Variable switching frequency

The analysis for variable frequency focuses on studying the switching frequency limits on a boost converter. For that matter, relating the input current with the current across the inductance if an LFR performance is obtained, the input power of the phases can be defined as,

$$p_N(t)=\frac{v_{gp}^2}{L_N}t_{on}\sin^2\left(\omega t-\frac{2\pi}{3}N\right), \tag{2.71}$$

where t_{on} defines the constant on time of the main switch and the subscript N of LN refers in this particular case to its numerical value (i.e., the value phases R, S and T were assigned, 1, 2 or 3). Then, averaging (2.71) and solving for t_{on} yields,

$$t_{on}=\frac{2p_NL_N}{v_{gp}^2}. \tag{2.72}$$

Next, applying volt-second balance to the main inductor, gives,

$$\frac{v_{gp}|\sin(\omega t)|}{L_N}t_{on}+\frac{v_{oN}(t)-v_{gp}|\sin(\omega t)|}{L_N}t_{off}(t)=0, \tag{2.73}$$

where $t_{off}(t)$ defines the variable off time on the main switch. Solving for $t_{off}(t)$ in (2.73) and considering the variation of the period over a line cycle, yields,

$$T_s(t)=t_{on}+t_{off}(t)=\frac{v_{oN}(t)t_{on}}{v_{oN}(t)-v_{gp}|\sin(\omega t)|}. \tag{2.74}$$

Consequently, the switching frequency, $f_s(t)$, can be obtained from (2.74), previously solving (2.32) into it, as,

$$f_s(t)=\frac{nV_{\gamma\_LED}+i_{oN}(t)\frac{n}{m}r_{LED}-v_{gp}|\sin(\omega t)|}{\left(nV_{\gamma\_LED}+i_{oN}(t)\frac{n}{m}r_{LED}\right)t_{on}}. \tag{2.75}$$

Next, the maximum and minimum values of (2.75) are to be determined. Because of the relationship in this scenario between frequency and duty cycle, this function resembles $k_2(\omega t)$, then, (2.75) can be rewritten as,

$$f_s(t)=\frac{k_{2,norm}(\omega t)}{t_{on}}. \tag{2.76}$$

Accordingly, the maximum value of $f_s(t)$ will happen exactly at the same point as for $k_{2,norm}(\omega t)$, meaning that,

$$f_{s,max}= t_{on}. \tag{2.77}$$

Unfortunately to calculate its minimum value it is necessary to normalize the switching frequency by normalizing (2.76) even further by factorizing nV_{γ_LED}, thus obtaining,

$$f_{s,norm}(t)=\frac{k_{2,norm}(\omega t)n^2V_{\gamma\_LED}^2v_{gn}^2}{2p_NL_N}. \tag{2.78}$$

Equation (2.78) gives all the information required to understand the effect of varying several design parameters on the switching frequency of the converter. In fact, it is possible to plot (2.78) versus the line phase while varying the three normalized variables (i.e., k_n, i_n and v_{gn}), one at a time, obtaining Fig. 2.18. In addition, Fig. 2.18, serves two purposes, the first is the analysis of variation of the switching frequency, and the second is the study of the minimum value of $k_{2,norm}(\omega t)$, for the fixed frequency scenario and for this one. The latter is done through Fig. 2.18 (a), (b), (c) and (d), where v_{gn} does not vary, hence being able to discern the behaviour of the function for the other two variables.

Fig. 2.18 (a) and (b) show the variation of the switching frequency with k_n for two different values of i_n, while keeping v_{gn} to a constant adequate value. Please note that v_{gn} in a boost converter, which is the current scenario, cannot surpass the unity value as the converter is intrinsically unable to reduce its output voltage. As can be seen, for the lowest value analyzed of i_n the variation of k_n does not affect, as significantly as, in other scenarios the variation of the switching frequency. This effect can be explained due to the ripple increase of both output voltage and current caused by lowering k_n, which also means lowering C_N. The reason why it affects the higher values of i_n can be explained due to its definition, as i_n has an impact on how the current through the LED load impacts the output voltage, which as has been repeated several times depends on the LED technology. This will be better understood, by observing Fig. 2.18 (c) and (d), where v_{gn} is left untouched at the same value and k_n takes two different one with a minimum output capacitance and another one equivalent to a scenario with a bulky capacitor. As can be seen, the scenarios with low i_n values present alike switching frequency variations, whereas, those with high values of i_n differ greatly toward the minimum value, which implies that the minimum value of $k_{2,norm}(\omega t)$ needs to be studied in detail. In fact, this figure can also be used to compare the differences between $k_{2,norm}(\omega t)$ with a high output ripple in both voltage and current, see Fig. 2.18 (c), and $k_{2,norm}(\omega t)$ with constant output voltage and current, see Fig. 2.18 (d). As can be seen, the high ripple scenario has a higher minimum, which will translate in ensuring DCM operation for the whole line phase with a higher value of L_N. This can be explained considering that the minimum value coincides with the maximum of the output voltage, demagnetizing L_N faster.

Finally, Fig. 2.18 (e) and (f) show that, as expected in a boost converter operating in BCM, the variation of v_{gn} changes both the minimum and maximum values, and is key in order to select the minimum working operation frequency to be just above the 20 kHz, that defines the maximum frequency of the human audible spectrum.

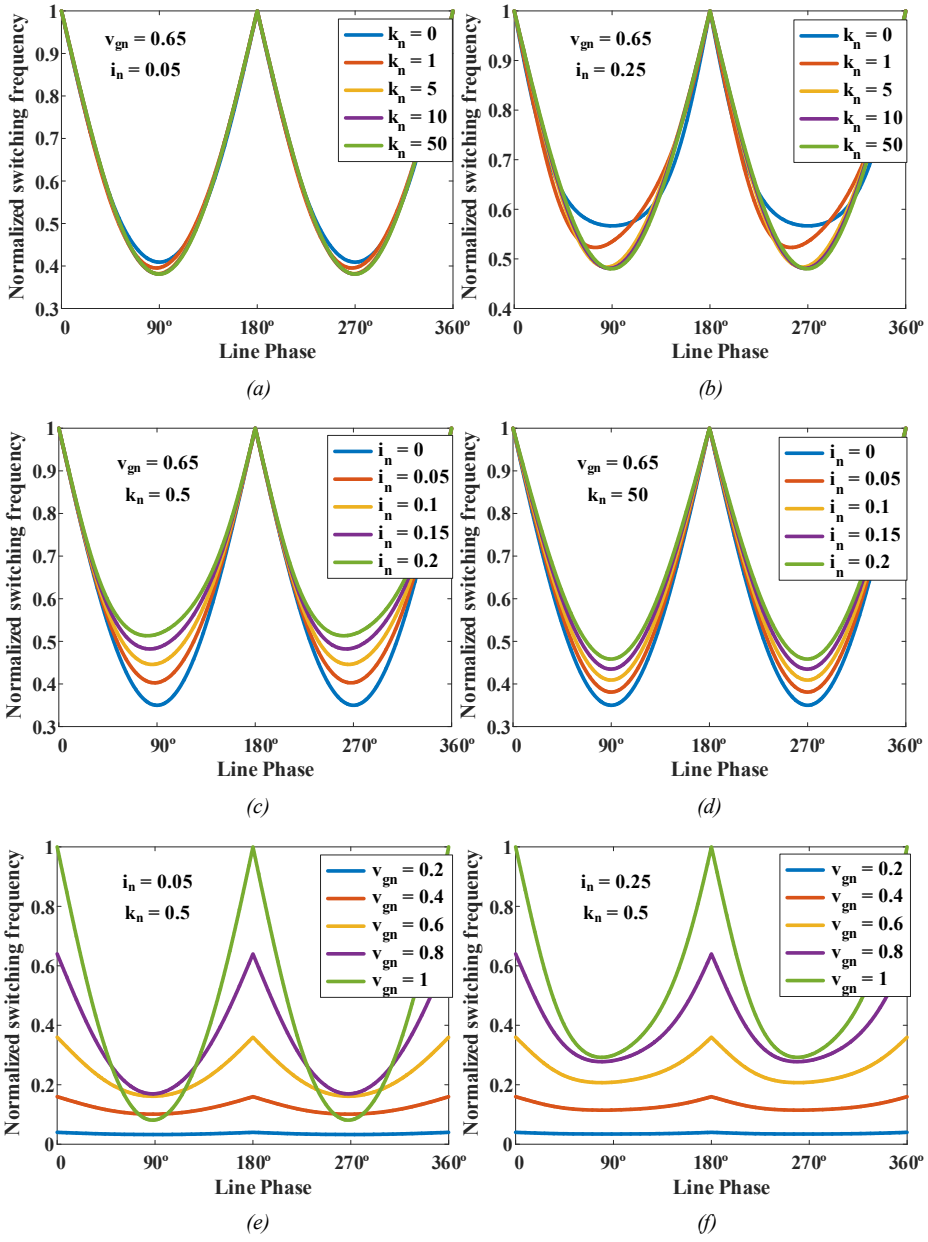


Fig. 2.18. Normalized switching frequency versus line phase in terms of: (a) k_n for v_{gn} and i_n equal to 0.65 and 0.05, respectively, (b) k_n for v_{gn} and i_n equal to 0.65 and 0.25, respectively, (c) i_n for v_{gn} and k_n equal to 0.65 and 0.5, respectively, (d) i_n for v_{gn} and k_n equal to 0.65 and 50, respectively, (e) v_{gn} for k_n and i_n equal to 0.5 and 0.05, respectively, and (f) v_{gn} for k_n and i_n equal to 0.5 and 0.25, respectively.

2.4.3 Control strategies

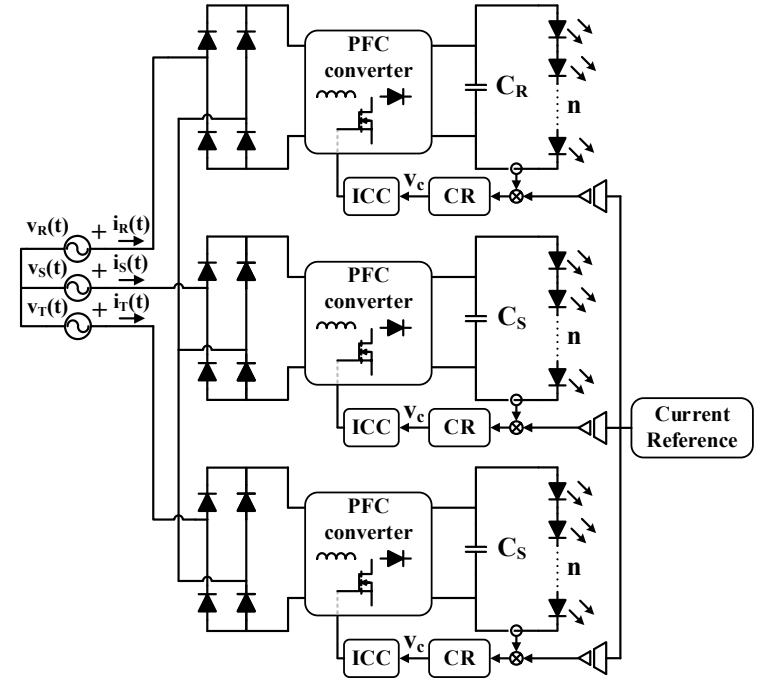
The design criteria of the cells have been discussed for different operating modes in the previous section considering the selection of an adequate inductor and output capacitor as the most relevant factors for the proposed operation of the cell. In that sense, the selection of the components will be carried out conventionally taking into account electrical stresses, cost, power losses, size, etc., as weighted by the designer. That being said, there is one factor that has not been presented yet, which is the control of the cell in order to sustain the LED load with an adequate current to ensure their driving and their capability of achieving full dimming operation, thus providing at the output of the ac-dc LED driver an acceptable light output.

2.4.3.1 Proposed schemes for closed loop operation

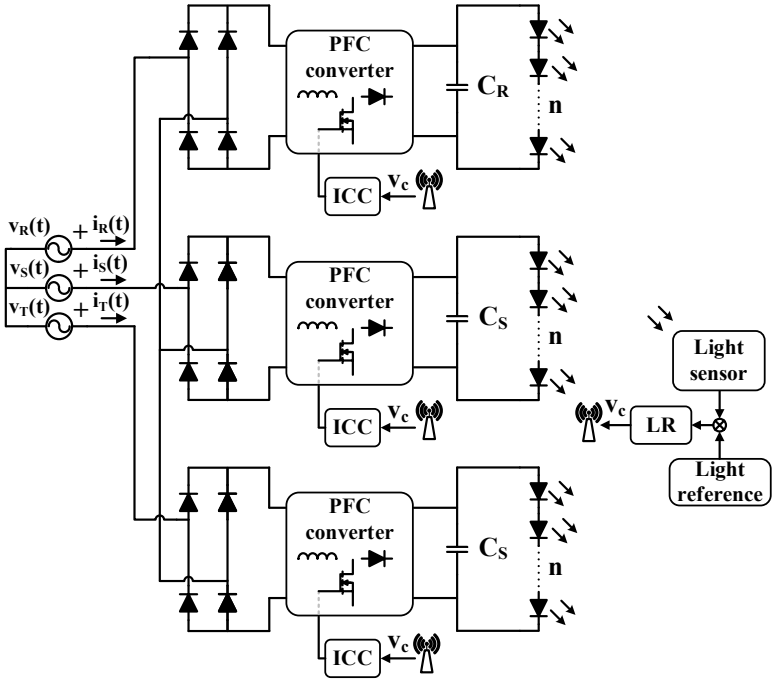
In this section, two ways are proposed for controlling the discussed ac-dc LED driver. The first one, depicted in Fig. 2.19 (a), is based on a conventional approach for a PFC converter in which the output current is controlled instead of the voltage, taking into account that each cell will have its own output current control by means of an independent CR. The CR is responsible for setting v_c, which directly impacts the R_{LFR} value of the cell, thus demanding more or less power in accordance to a current reference set by the central control. It should be noted that in each of the cells the LFR performance is ensured by means of an Input Current Controller (ICC) responsible for controlling the switches of the PFC converter to adequately shape the input current.

This proposal is simple, follows the conventional single-phase approach and ensures that the LED load is driven with a determined average current level. Consequently, the light output should be guaranteed to be constant in accordance to the previous mathematical analysis. In contrast, it is necessary to filter the low frequency components of the output current in order to control its average value, hindering in the process the maximum achievable bandwidth of a three-phase converter, which could arguably reach that of a dc-dc converter, and reducing it to the single-phase single-stage ac-dc LED driver scenario. Furthermore, the current reference value needs to be carefully isolated to be able to provide this information to each cell.

The other scheme, see Fig. 2.19 (b), controls $l_o(t)$ of the whole ac-dc LED driver. This method proposes sensing the output luminance at a fixed distance by means of a light sensor (e.g., transimpedance amplifier), which will translate the incident light to a certain voltage level in accordance to its gain [2.37]. This voltage is, then, compared to a reference in order to estimate the error which is the input of the Light Regulator (LR). The LR, similarly to the CR presented in the previous scenario, is responsible for controlling v_c, which will be sent via wireless communications to each of the modules. In that sense, this method resembles the conventional control used for three-phase modular ac-dc converters, in which the output voltage is controlled and the cells receive v_c to set the power they have to supply to the load [2.8]. Moreover, this scheme will potentially have the same theoretic bandwidth as its dc-dc converter counterpart. However, taking into account the tolerances of the components, it is normally limited to six times the mains frequency to remove the ripple that can appear due to non-idealities at the output of a multi-cell three-phase ac-dc LED driver. Even so, the bandwidth is improved in comparison with the previous scheme. The main issue comes from requiring a light sensor at a fixed distance with a wireless communication protocol to transmit information on the



(a)



(b)

Fig. 2.19. Closed loop operation of the multi-cell LED driver based on summing the light output of each phase. (a) Current closed loop per cell. (b) Light output closed loop operation per LED driver.

control variable, v_c, to the cells, fact that will increase both the cost and complexity of this solution.

A combination of both schemas could also be evaluated for a better performance, in order to remove the ripple at six times the mains frequency that may appear due to tolerances and non-idealities. However, the increase of complexity does not justify the aforementioned benefits taking into account that LEDs are a dynamically slow load.

2.4.3.2 Dynamic analysis

The two schemes previously introduced require active control loops in order to control the light output of the ac-dc LED driver. Then, it is necessary to obtain a transfer function of the ac-dc LED driver to obtain a useful tool in order to design the required feedback loops.

The dynamic analysis for this ac-dc LED driver can be tackled similarly to the one carried out in Subsection 2.2.2, but in this case considering the relationships between input and output power in a single cell. For that matter, starting from (2.31) and averaging its variables, it is possible to obtain:

$$\frac{v_{gp}^2}{2K_1} v_c = C_N v_{oN} \frac{dv_{oN}}{dt} + v_{oN} i_{oN}, \tag{2.79}$$

where, v_{oN} and i_{oN} represent the average value of $v_{oN}(t)$ and $i_{oN}(t)$, respectively, K_1 is a constant that depends on the control method used in the ICC to attain the LFR resistor and defines its gain, as explained by Table 1.1. Substituting (2.32) into (2.80), then,

$$\begin{aligned} \frac{v_{gp}^2}{2K_1} v_c = C_N &\left(n V_{\gamma\_LED} + i_{oN} \frac{n}{m} r_{LED} \right) \frac{n}{m} r_{LED} \frac{di_{oN}}{dt} \\ &+ \left(n V_{\gamma\_LED} + i_{oN} \frac{n}{m} r_{LED} \right) i_{oN}. \end{aligned} \tag{2.80}$$

Next, (2.80) is perturbed, considering $i_{oN}=I_{oN}+\hat{i}_{oN}$, $v_c=V_c+\hat{v}_c$ and $v_{gp}=V_{gp}+\hat{v}_{gp}$, and after perturbing the second order and dc terms are removed, yielding,

$$\begin{aligned} \frac{V_{gp}^2}{2K_1} \hat{v}_{gp} + \frac{V_{gp} V_c}{K_1} \hat{v}_c = C_N &\left(n V_{\gamma\_LED} + I_{oN} \frac{n}{m} r_{LED} \right) \frac{n}{m} r_{LED} \frac{d\hat{i}_{oN}}{dt} \\ &+ \left(n V_{\gamma\_LED} + 2 I_{oN} \frac{n}{m} r_{LED} \right) \hat{i}_{oN}. \end{aligned} \tag{2.81}$$

Note that, again, the lower case characters are used for the static analysis, the capitalized characters are used for constant values to particularize the equation in a determined point of operation and those lower case characters with a circumflex represent small ac variations. Now, applying the Laplace transforms gives,

$$\begin{aligned} \frac{V_{gp}^2}{2K_1} \hat{v}_{gp} + \frac{V_{gp} V_c}{K_1} \hat{v}_c = C_N &\left(n V_{\gamma\_LED} + I_{oN} \frac{n}{m} r_{LED} \right) \frac{n}{m} r_{LED} s\hat{i}_{oN} \\ &+ \left(n V_{\gamma\_LED} + 2 I_{oN} \frac{n}{m} r_{LED} \right) \hat{i}_{oN}. \end{aligned} \tag{2.82}$$

Solving for $i_{oN}(s)$ in (2.82), yields,

$$\hat{i}_{oN}=\frac{\frac{2V_{gp}V_c}{K_1}\hat{v}_{gp}+\frac{V_{gp}^2}{K_1}\hat{v}_c}{C_N\left(nV_{\gamma\_LED}+I_{oN}\frac{n}{m}r_{LED}\right)\frac{n}{m}r_{LED}s+\left(nV_{\gamma\_LED}+2I_{oN}\frac{n}{m}r_{LED}\right)}. \tag{2.83}$$

Hence, from (2.83) the transfer function that relates $\hat{i}_{oN}$ with $\hat{v}_c$ can be obtained for any of the cells that comprise the LED driver as,

$$G_{i_{oN}v_c}(s)=\left.\frac{\hat{i}_{oN}}{\hat{v}_c}\right|_{\hat{v}_{gp}=0}=\frac{A_3}{A_4s+1}. \tag{2.84}$$

where A_3 and A_4 can be defined as,

$$A_3=\frac{V_{gp}^2}{2K_1\left(nV_{\gamma\_LED}+2I_{oN}\frac{n}{m}r_{LED}\right)}, \tag{2.85}$$

$$A_4=\frac{C_N\left(nV_{\gamma\_LED}+I_{oN}\frac{n}{m}r_{LED}\right)\frac{n}{m}r_{LED}}{\left(nV_{\gamma\_LED}+2I_{oN}\frac{n}{m}r_{LED}\right)}. \tag{2.86}$$

Equation (2.84) defines the transfer function of each cell that comprises the LED driver, which should be followed to design the CR of each cell under the first scenario depicted in Fig. 2.19 (a). In order to obtain the transfer function that defines the second scenario depicted in Fig. 2.19 (b), it is required to average and linearize (2.18). Then, applying the Laplace transform, yields,

$$\hat{I}_o=3\alpha\hat{i}_{oN}. \tag{2.87}$$

Combining (2.83) and (2.87) yields,

$$\hat{I}_o=\frac{3\alpha\left(\frac{2V_{gp}V_c}{K_1}\hat{v}_g+\frac{V_{gp}^2}{K_1}\hat{v}_c\right)}{C_N\left(nV_{\gamma\_LED}+I_{oN}\frac{n}{m}r_{LED}\right)\frac{n}{m}r_{LED}s+\left(nV_{\gamma\_LED}+2I_{oN}\frac{n}{m}r_{LED}\right)}. \tag{2.88}$$

Finally, relating I_o and v_a gives the expression that defines the transfer function required to design the LR taking into account the gain an dynamic of the light sensor, as,

$$G_{I_ov_c}(s)=\left.\frac{\hat{I}_o}{\hat{v}_c}\right|_{\hat{v}_{gp}=0}=\frac{3\alpha A_3}{A_4s+1}. \tag{2.89}$$

It should be noted that (2.84) and (2.89) can be particularized for any of the PFC converters described in Table 2.2.

2.5 Experimental results for the Delco ac-dc LED driver and the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier

This section is dedicated to the experimental results of the Delco ac-dc LED driver and the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier. For that matter, both topologies have been designed and prototyped for a maximum power of 90 W in order to validate the claims of sections 2.2 and 2.3. Taking into account the power range, the flyback converter operating in DCM is the preferred solution for the cells depicted in Fig. 1.1 and Fig. 2.5 working at 100 kHz as LFRs, see Fig. 2.20. The components that are used to build each of the cells are summarized in Table 2.5, sharing the same components to accurately compare both topologies. In addition, the use of the same components is possible considering the cells are designed for the Delco ac-dc LED driver, in which each cell handles twice the power compared to the multi-cell ac-dc LED driver.

Table 2.5. Components of the experimental LFR cell built with a flyback operating in DCM.

Fig. 2.20 reference	Value
Dc_1	STTH208U
Dc_2	FES8BT-E3/45
C_1	1 µF 800 V Ceramic Cap.
C_2	100 nF 450 V Film Cap.
C_3	1 µF 50 V Film Cap.
R_1	10.5 kΩ
Q	IPP65R225C7
CI	Coilcraft Z9007-BL

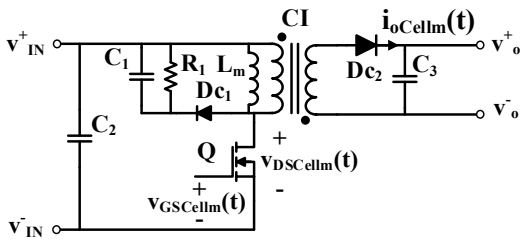


Fig. 2.20. Schematic of the LFR cell based on a dc-dc flyback converter.

Both ac-dc LED drivers receive a three-phase input voltage between 380 and 420 Vrms line-to-line, which corresponds with the European three-phase power grid. In addition, they feed five strings of 12 LEDs (i.e., n=12 and m=5, of W42189T2-SW, whose

max{p_{LED}/P_{base}} is 0.2) with their respective equalizing resistor to ensure an adequate current sharing between the strings, making this load equivalent to 1.8 A and 48 V at full load. The rest of the components that comprise the ac-dc LED driver are summarized in Table 2.6, not taking into account the circuitry used to isolate the driving signal that comes from the FPGA, more information regarding the control of both the Delco ac-dc LED driver and the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier can be found in Appendix A. The FPGA is used as the central control unit of the ac-dc LED driver due to the versatility that it provides, simplifying the start-up of this specific ac-dc LED driver as a matter of steadily increasing the duty cycle from zero to the required duty set by the control feedback loop, which is also included.

Fig. 2.21 shows a picture of both prototypes with their respective size measured in millimeters, showing their compactness. The green PCBs connected to the sides of the main PCB are the driving isolators for each of the LFR cells. It should be noted that the couple inductors are on the other side of the PCB in order to minimize its volume.

Table 2.6. Rest of components outside of the LFR cells, that comprise the ac-dc LED drivers.

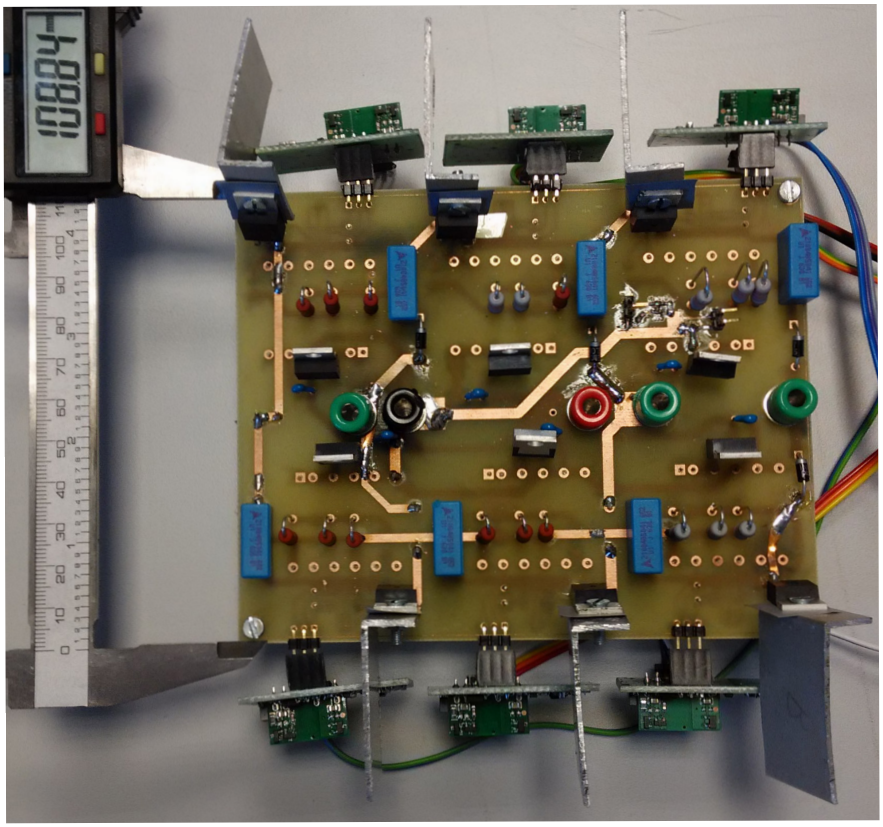
Fig. 1.1 and Fig. 2.5 reference	Value
LF diodes	1N4007
C_o	10 μF 100 V Film Cap.
FPGA	XC7A100T-1CSG324C

The main objective of this section is to demonstrate the operation of the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier, from an input perspective, taking into account the operation of the cells, and from an output perspective, considering the dimming of the LEDs, while observing the overall performance, compliance with the regulation and comparing the operation of both ac-dc LED drivers to discern adequately the recommended ranges of operation of both solutions. The input perspective is not carried out for the Delco ac-dc LED driver taking into consideration this operation is well-known for the flyback cells used in this analysis. However, the output perspective needs to be looked at to validate its operation as an ac-dc LED driver.

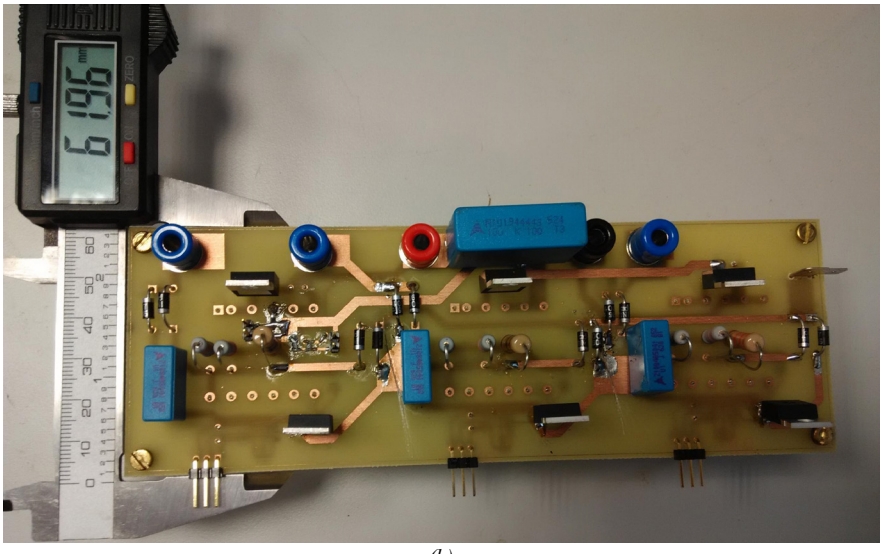
All the measurements carried out throughout this section are done in close loop operation. The details regarding control and design of the regulators are summarized in Appendix B.

2.5.1 Basic operation of the proposed multi-cell ac-dc LED driver based on the three-phase full-wave rectifier.

After having designed both prototypes, the next step was connecting them to the real three-phase power grid using an auto-transformer as the interphase between the grid and the LED drivers. In addition, the auto-transformer has granted the ability to test different input voltages while using the real three-phase power grid input waveforms in order to test the LED drivers in an environment as close as possible to reality with possibly distorted waveform. It is this distortion which justifies the shape of $v_R(t)$ in Fig. 2.22, flatting itself toward the edges of the sinusoid.



(a)



(b)

Fig. 2.21. Prototypes of the ac-dc LED drivers with their measurements in milimeters. (a) Delco ac-dc LED driver. (b) Multi-cell ac-dc LED driver based on the three-phase full-wave rectifier.

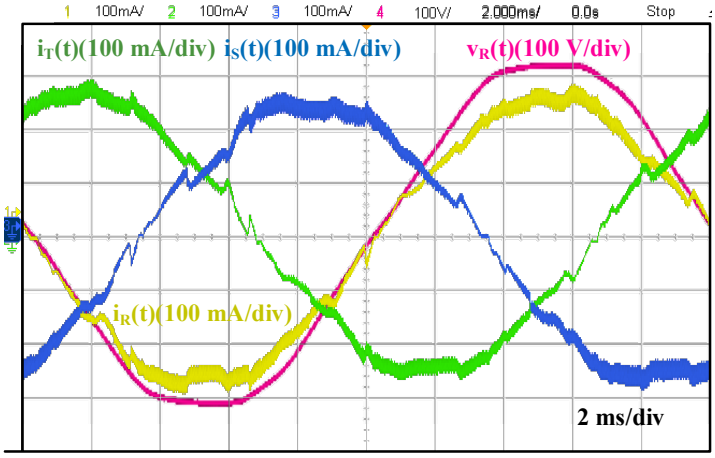


Fig. 2.22. Filtered input currents removing the high frequency component for all three phases and input voltage of phase R of the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier.

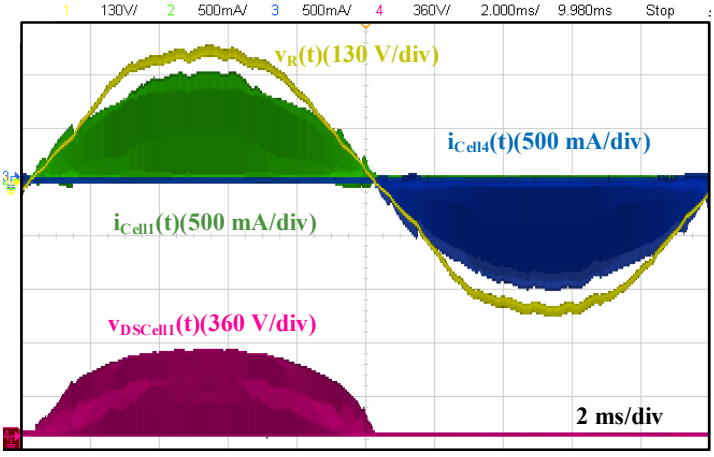
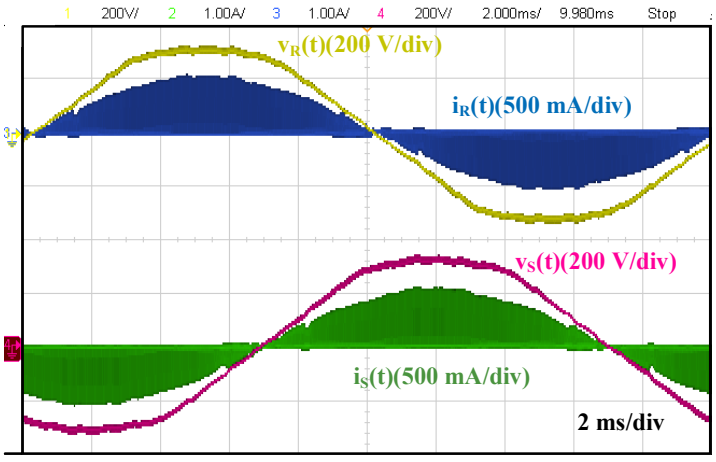


Fig. 2.23. Performance of branch R of the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier capturing: input voltage, input current on cells 1 and 4 and drain-source voltage on the main switch of cell 1.

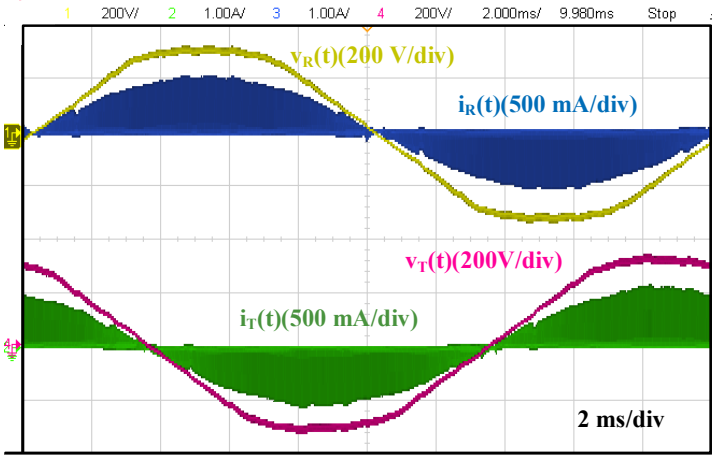
Furthermore, Fig. 2.22 shows a snapshot of the oscilloscope for the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier, where the input currents of the driver, as well as, the input voltage of phase R can be observed. As can be seen, $i_R(t)$ follows the shape of $v_R(t)$ while being in phase with each other, validating the LFR performance for this phase. Performance that can be assumed for the other two phases (i.e., $i_S(t)$ and $i_T(t)$), taking into account that they are phase shifted accordingly to a balanced three-phase power grid. It should be noted that, the presented waveforms do not show the high frequency component of the current cause by the cell as it is filtered. Then, to correctly exemplify the operation of the cells dedicated to a specific branch, Fig. 2.23 shows the most significant waveforms of phase R. As can be seen, still at line frequency, the current demanded by phase R is shown by means of the currents demanded by cells 1

and 4, correctly showing, taking v_R as a reference, that cell 1 operates during the positive half cycle and cell 4 during the negative half cycle of phase R. This performance which can be extrapolated to the other phases of the converter. In addition v_{DS} for the main switch of cell 1, $v_{DSCell1}(t)$, is also shown to demonstrate that the voltage withstood by this switch never surpasses its breakdown voltage. Therefore, assuring the correct operation of both cells in the proposed multi-cell ac-dc LED driver based on the three-phase full-wave rectifier.

Fig. 2.24 (a) and (b) show the high frequency currents measured before being filtered at the input of the cells, with their respective phase voltages. For that matter, $i_R(t)$ is equal to summing $i_{Cell1}(t)$ and $i_{Cell4}(t)$, $i_S(t)$ is equal to $i_{Cell2}(t)$ plus $i_{Cell4}(t)$, and $i_T(t)$ is equal to i_{Cell3} plus $i_{Cell6,}$ see Fig. 2.5. These figures are used to validate the achievement of close to unity PF on phases S and T.



(a)



(b)

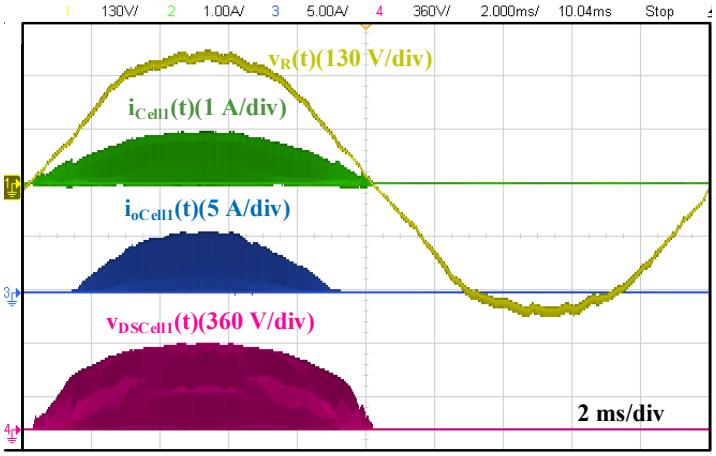
Fig. 2.24. Input voltage and input currents for (a) Phases R and S. (b) Phases R and T.

The operation of one of the cells is studied in detail in Fig. 2.25 validating the operation in DCM of the flyback converter as a cell; in this case particularized for cell 1 whose performance is equivalent to any of the cells included in the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier. As can be seen in Fig. 2.25 (a), the cell only operates during half line cycle, as expected, only supplying energy to the load during this period, see $i_{oCell1}(t)$.

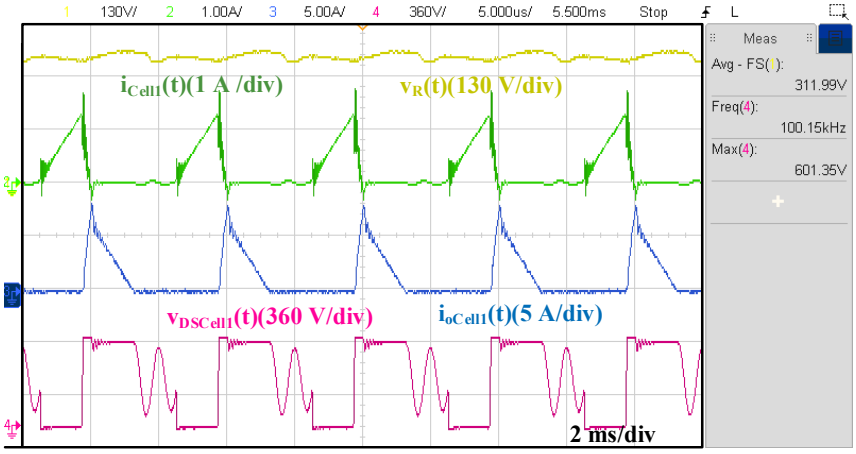
Ensuring the LFR performance of the cell is key for the implementation of the ac-dc LED drivers discussed in the current chapter. As has been previously introduced, the flyback converter is required to work in DCM for the whole line period to achieve this performance. Hence, a zoom near the peak and at 200 V of the phase voltage is done to Fig. 2.25 (a) in order to exemplify the aforementioned performance, obtaining Fig. 2.25 (b) and (c). These figures show that the cell operates at a constant frequency achieving DCM operation, as required, which is demonstrated thanks to $i_{oCell1}(t)$ due to it reaching the zero current value before the end of a switching period. Therefore, the current through the couple inductor should follow the same behaviour. Another important result that can be observed in these figures, is the clamping of $v_{DSCell1}(t)$ to a maximum of 600 V thanks to the passive snubber used in the cell, see Fig. 2.20 (i.e., C_1, R_1 and D_{c1}).

A method to clamp the drain-source voltage on the main switch of a flyback converter is mandatory to avoid the destruction of the main switch, and consequently the LFR cell. The reason can be understood with the operation of a flyback converter. Unlike, other isolated topologies the flyback converter uses its coupled inductor to store energy during the turn-on of the main switch and to attain galvanic isolating. Then, during the turn-off part of the energy stored in the magnetizing inductance is provided to the load, however, the energy stored in the leakage inductance does not have an actual path to discharge and starts charging the parasitic capacitor (i.e., C_{oss}) of the main switch, resonating with it and causing its voltage to increase, which can be problematic if it surpasses its breakdown voltage. The easiest way to patch this issue is by means of a passive circuit that is able to clamp that voltage and dispose of the extra energy stored in the leakage inductance [2.38]. Although, using a passive snubber is simple it incurs in bigger losses, when compared to active clamping methods that can recycle that energy to achieve higher efficiencies by increasing the complexity of the flyback converter [2.39], [2.40]. Nonetheless, for the scope of the tests performed in this subsection to validate and compare the ac-dc LED drivers a passive snubber suffices taking into account that any uncertainty cause by the extra switch and circuitry is eliminated.

At this point the performance of the multi-cell LED driver based on the three-phase full-wave rectifier can be concluded from the point of view of its input. It is in order to continue the tests by observing the feasibility of obtaining adequate output currents to drive the LED load. For that matter, the high frequency output currents of the cells before the capacitance C_3, are measured in Fig. 2.26 with the output voltage that the LED load needs to withstand. The currents are measured by conjoining the high frequency output currents of each the six cells in groups of two relating the currents corresponding to each phase or branch. This last statement means that phase R would be the sum of $i_{oCell1}(t)$ and $i_{oCell4}(t)$, phase S would be the sum of $i_{oCell2}(t)$ and $i_{oCell5}(t)$, and phase T would be the sum of $i_{oCell3}(t)$ and $i_{oCell6}(t)$. As can be observed, all three current measurements are extremely similar to each other, meaning that the output power provided by each cell is as well. Then, the theoretical i_o would be constant in accordance to the theoretical study previously carried out.



(a)



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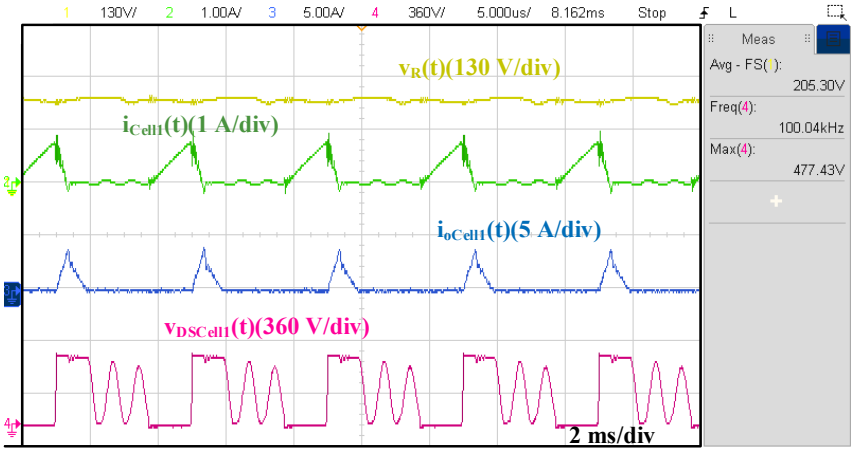


(c)

Fig. 2.25. Operation of cell 1 in the proposed converter. (a) Line frequency. (b) Zoom near the peak value of the phase voltage (i.e., 310 V) (c) Zoom at 200 V of the phase voltage.

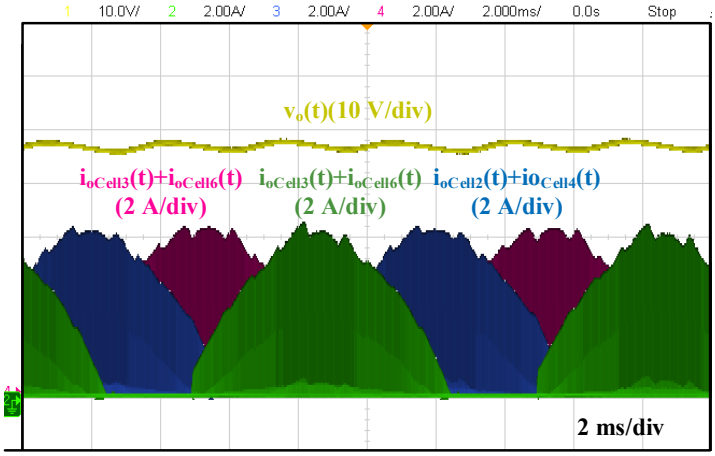


Fig. 2.26. High frequency output currents for each phase and.output voltage for the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier.

The output currents of each phase are summed due to the output parallel connection of the cells, achieving a constant i_o, as can be seen in Fig. 2.27 (a), taking in account how small sized the output capacitance is (i.e., 10 µF film capacitor). The Delco ac-dc LED driver has not been analyzed in terms of its input performance due to its well-known behaviour. However, considering its proposal as an ac-dc LED driver, the analysis of the output current is extended to the Delco ac-dc LED driver in order to validate its operation with an LED load, showing extremely similar results to the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier, as can be seen in Fig. 2.27 (b).

A six times the main frequency ripple (i.e., 300 Hz) can be seen on both v_o and i_o due to the input voltage not being a pure sinusoidal waveform, as it is in fact cropped toward the peak. Hence, the input power cannot be considered constant against what was derived in (2.2), meaning that some degree of variation should occur at the load. Furthermore, the tolerance of the components aggravates this issue. Nonetheless, the current ripple can be reduced by further increasing the output capacitance without including an electrolytic capacitor, but before rushing into conclusions the flicker regulation has to be carefully studied. Please note that all the results have been obtained for both drivers while operating in closed loop, which has been designed digitally on the FPGA avoiding limit cycling following the conditions set in [2.41] for PFC, see Appendix A.

2.5.2 Compliance with the LED driver regulations

In the previous subsection, several sets of waveforms have been obtained validating the performance of the two ac-dc LED drivers under study. These waveforms have been extracted from the oscilloscope as data and processed with MATLAB in order to study the different parameters that are required to validate the regulations that an ac-dc LED driver needs to comply and that were discussed in detail in Chapter 1. For that matter, the THD and PF have been summarized in Table 2.7 and Table 2.8 for both ac-dc LED drivers, after having analyzed the input currents of each LED driver at three different output current levels, showing an almost unity PF which ensures compliance with ENERGY STAR® [2.42].

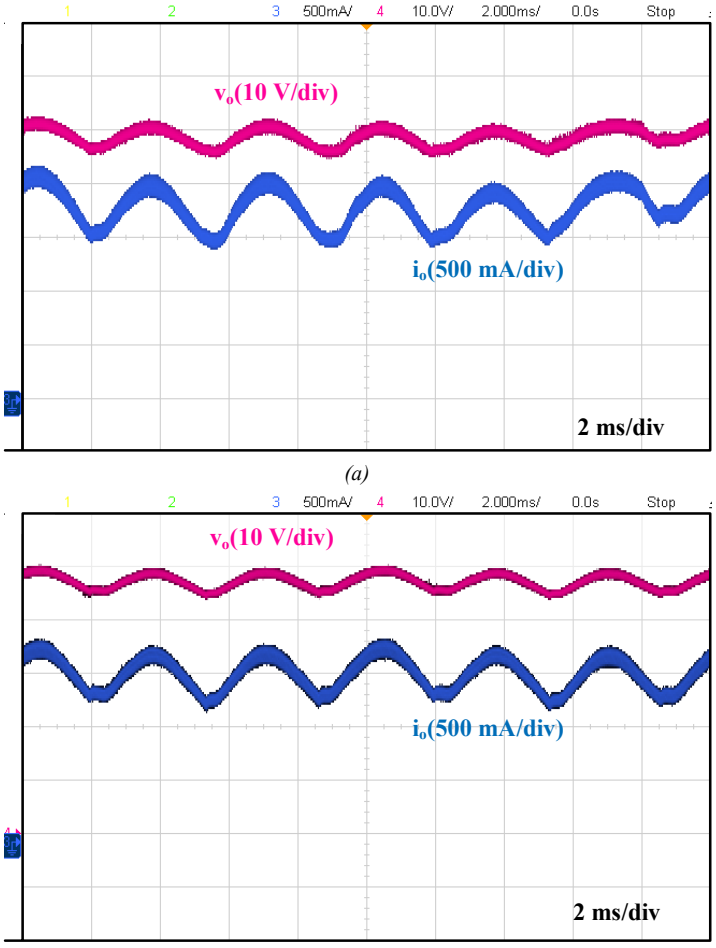


Fig. 2.27. Output current and voltage for (a) the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier when fully loaded and (b) Delco ac-dc LED driver.

In terms of THD, the results are extremely similar having slightly better results for the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier, which can be explained due to the tolerances of the components that comprise the LFR cells. This can be understood, by taking a closer look at the difference between phases in the same ac-dc LED driver in Table 2.7and Table 2.8. As can be seen, at the same output current on the Delco ac-dc LED driver, there is a discrepancy of two points between the THD on phases R and S. Then it is understandable for that same behaviour to happen between the two LED drivers due to tolerances taking into consideration they use the same LFR cell.

The other limit introduced by ENERGY STAR® is in terms of the minimum lifetime of the LED driver [2.42], which excludes several technologies from being used as the components of the driver. The implication being that to obtain this seal of approval, the solution needs to dispose of the electrolytic capacitor. In that sense, both LED drivers analyzed in this subsection are able to achieve this requirement, as can be seen in Fig. 2.23, Table 2.5 and Table 2.6.

Table 2.7. Summary of THD and PF for three different output current for the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier

Output current/Phase		1.8 A	0.9 A	0.45 A
R	PF [%]	99.81	99.72	99.56
	THD [%]	5.71	6.97	8.03
S	PF [%]	99.87	99.75	99.59
	THD [%]	4.62	6.96	7.71
T	PF [%]	99.85	99.73	99.58
	THD [%]	5.26	6.86	7.97

Table 2.8. Summary of THD and PF for three different output current for the Delco ac-dc LED driver.

Output current/Phase		1.8 A	0.9 A	0.45 A
R	PF [%]	99.69	99.62	99.12
	THD [%]	6.97	7.42	10.03
S	PF [%]	99.73	99.65	99.50
	THD [%]	4.87	5.44	8.21
T	PF [%]	99.77	99.59	99.32
	THD [%]	5.22	7.07	9.51

Continuing the analysis of the input currents of the ac-dc LED drivers under study, the next step is validating whether the harmonic content of the input current of each phase falls within the limits of Class C IEC 61000-3-2 [2.43]. As a reminder, the ac-dc LED drivers analyzed in this section need to comply with the aforementioned regulation due to their input power being higher than 25 W. Fig. 2.28 (a) and (b) show that the harmonic content of the input currents at full load and nominal input voltage for both drivers fall within the limits of the regulation assuring its compliance, as expected taking into account how sinusoidal the input currents are.

Finally, the last regulation that needs to be dealt with is the Practice 1 of the flicker regulation, IEEE Std. 1789-2015. Accordingly, the instantaneous output luminance of each driver has been measured, and the harmonic content has been obtained considering the line frequency as the fundamental frequency of the analysis. Then, the Mod. (%) of each of the harmonics can be obtained and compared with the limits set by the regulation, which gives Fig. 2.29. As can be seen, both ac-dc LED drivers are able to comply the aforementioned regulation, obtaining similar results and ensuring good light quality at the output of both LED drivers. Perhaps slightly better for the Delco ac-dc LED driver due to the less amount of different cells used, however, the changes are not significant and the most limiting harmonic would be for both the one at six times the mains frequency (i.e., 300 Hz for the European three-phase ac power grid).

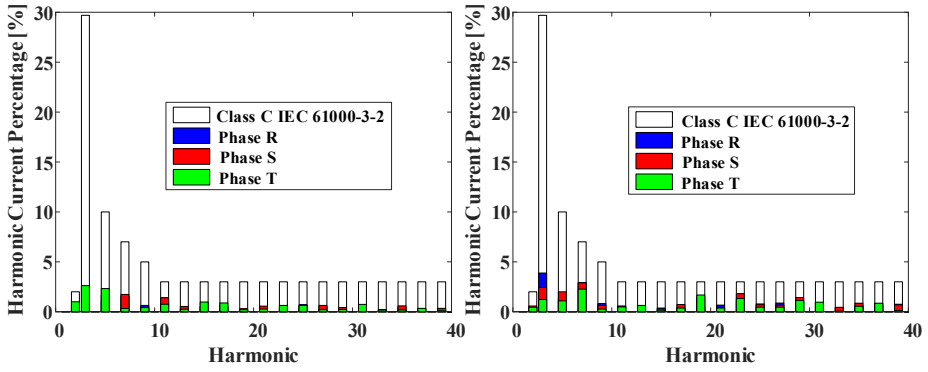


Fig. 2.28. Harmonic content of each phase for (a) the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier and (b) the Delco ac-dc LED driver, compared with the harmonic limits set by Class C from the IEC 61000-3-2 [2.43].

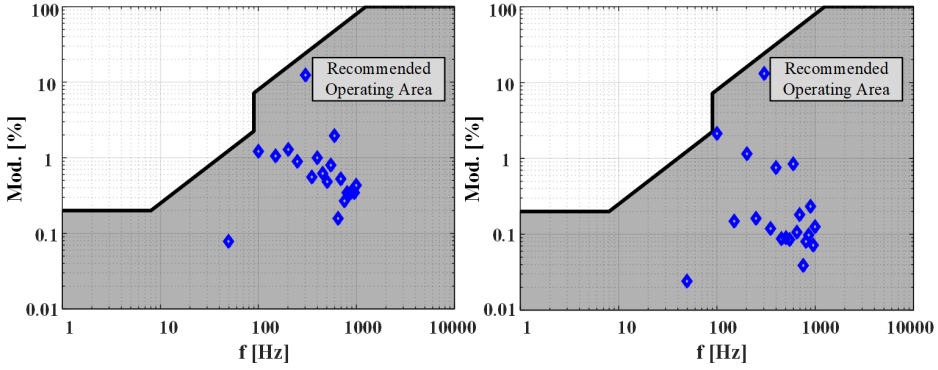


Fig. 2.29. Harmonic content of the instanteneaous output luminances of (a) the multi-cell LED driver based on the three-phase full-wave rectifier and (b) the Delco LED driver, compared with the harmonic limits set by Practice 1 from the IEEE Std. 1789-2015 [2.45].

2.5.3 Dimming validation and comparison of the LED drivers

After having demonstrated the compliance with the required regulations, it is necessary to test the performance of both ac-dc LED drivers under dimming conditions. Table 2.7 and Table 2.8 have summarized some results under different output currents to validate the performance of the LED drivers from the input current perspective, as has been previously seen increasing the THD the lower the output current is.

Under these conditions, the efficiency of both ac-dc LED drivers have been measured and compared without taking into account the driving losses, showing a slightly better performance for the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier, as can be seen in Fig. 2.30. The differences in efficiency can be explained due to the advantages that the multi-cell LED driver based on the three-phase full-wave rectifier has over the Delco ac-dc LED driver and that. These facts are related, as a reminder, to the amount of LF diodes conducting at a time and due to the cells working

half of the time. The latter, leads to a significant difference in temperature as shown in Fig. 2.31, where the maximum temperature achieved by the Delco ac-dc LED driver almost doubles the maximum temperature attained by the multi-cell at full load. For that matter, by increasing the power in both prototypes the difference in efficiency will continue on increasing becoming clearer the advantage of the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier. Nonetheless, the proposed comparison between the ac-dc LED drivers can be considered unfair taking into account that the LFR cell used for the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier is not optimized. The optimization of the flyback will impact both the size and selected components of the cell, considering that each cell processes half the power in comparison with the Delco ac-dc LED driver, arguably making the difference in efficiency more significant. The reason for using the same LFR cells can be explained to demonstrate its better performance under non-ideal conditions, as this analysis would lastly depend on the application and technology of the components.

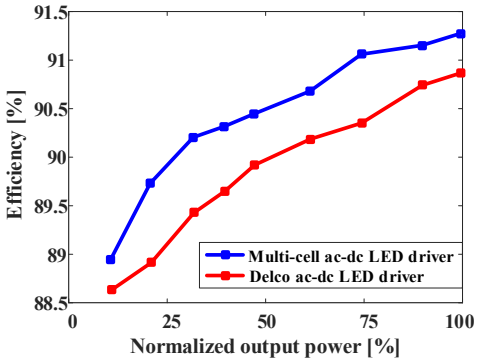
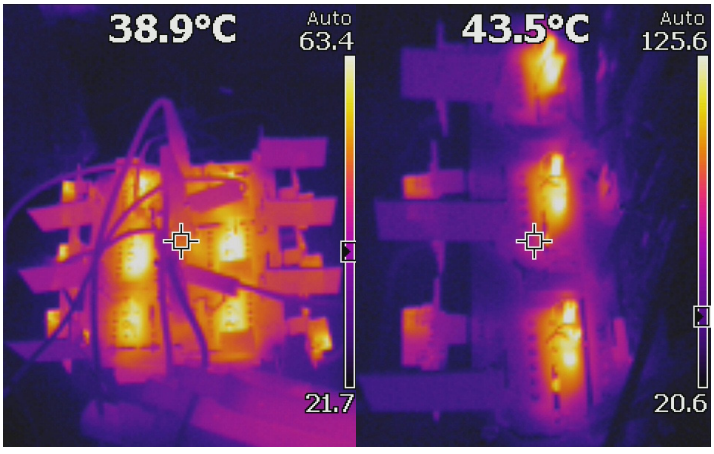


Fig. 2.30. Efficiency versus output current for the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier and the Delco LED driver, not taking into account driving losses.



(a) *(b)*

Fig. 2.31. Thermal performance of (a) the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier and (b) the Delco ac-dc LED driver.

Finally, it can be seen that the efficiency decreases with the output power, being roughly 88% at the full dimming point. This efficiency can be considered low for an ac-dc LED driver, as the optimization of the cell was not taken into account when designing these ac-dc LED driver and the aim was validating the concept of feeding LEDs in three-phase ac power grids in conjunction with validating the proposed topology. For that matter, dc-dc flyback converters were used as the cells considering how easily it is to achieve an LFR performance with them.

2.6 Experimental results for the two-stage Delco ac-dc LED driver

The previous section tested and compared the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier and the Delco ac-dc LED driver. However, the efficiency achieved by a flyback based cell can be a limiting factor when designing an ac-dc LED driver for a high power luminaire.

Consequently, the approach used in single-phase solutions seems to be the most attractive for high power luminaires, basing the design of the cell on a two-stage power converter, as the one depicted in Fig. 2.12. In addition, the ac-dc LED driver needs to dispose of the electrolytic capacitor, guaranteeing a flicker free operation, included at the intermediate bus (i.e., C_R, C_S or C_T). However, the traditional approach is based on using the second stage to perform this feat by means of control allowing a certain ripple to appear in the intermediate bus, which further complicates and increases the cost of the solution, as has been introduced in Chapter 1.

Nonetheless, taking into account the intrinsic performance of a balanced three-phase ac-dc LED driver, where the power is not going to pulsate at its output. Then, it should be possible to remove the electrolytic capacitor without including extra components. The conventional approach for this two-stage cell is based on having an output voltage loop that controls the voltage at the intermediate bus of each cell, also requiring an output current feedback loop for each of the dc-dc converter which controls the current fed to the load [2.6], [2.7]. It should be noted that with these two feedback loops the electrolytic capacitor is not removed, as every PFC converter works independently. This means each PFC converter controls its output voltage, which is required to be constant, hence, using an electrolytic capacitor. In addition, a third feedback loop responsible for the output voltage of the power converter will also be required, which in the case of LEDs is not necessary, as the preferred control is based on measuring the output current [2.46].

The proposal is depicted in Fig. 2.32, where there is only one feedback loop responsible for the current fed to the LED load, and in fact is the only one required. Reaching to this conclusion is rather simple by taking a look back at the analysis performed in Section 2.2 based on the Delco topology. By replacing the PFC converters with their equivalent LFR model, and considering that the dc-dc converter should behave as an ideal transformer with a fixed gain. Then, the dc-dc converter can be considered as a gain that will not have an impact on demanding more or less power from the grid. Mainly, due to the fact that the power consumption relies entirely on the value taken by v_c. Hence, controlling v_c will suffice to determine how much current is required to feed the LED load with in accordance to the scheme proposed in Fig. 2.32.

Then, the CR, shown in Fig. 2.32, can be obtained from a transfer function that is obtained following the same analysis carried out in Subsection 2.2.2, taken into account the characteristics of the PFC converter and a dc-dc isolated converter as an LFR.

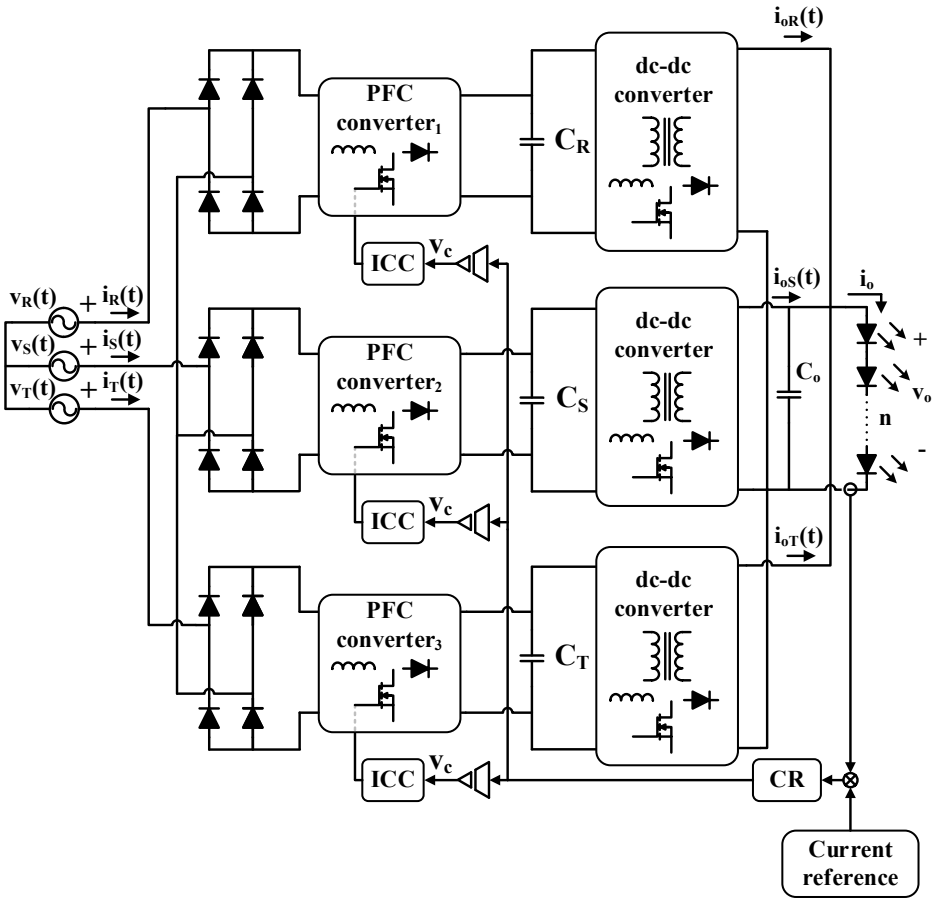


Fig. 2.32. Proposed control for the Delco ac-dc LED driver based on a two-stage cell.

The other issue with this approach, based on a two-stage cell, has been tackled in the previous literature and affects the start-up of the Delco topology in a three-wire connection to the three-phase power grid, when the LFR performance of the PFC converter is obtained by an MBC [2.7], being specific and complex for this application.

2.6.1 Start-up procedure of a two-stage Delco LED driver with MBC

It is a well-known fact that for a PFC converter to work as an LFR with a MBC, a sinusoidal reference is necessary. This sinusoidal reference is conventionally based on the input voltage of PFC converter [2.13], which in terms of practicality is convenient as it is the reference that is required to be followed to achieve an LFR performance. Then, it can be assumed that the start-up procedure would be similar to a single-phase one, in

which the voltage is steadily increased on the intermediate bus and then followed by the start-up of the dc-dc converter.

However, the issue becomes more complex in a three-wire connection in a three-phase ac power grid due to the lack of connection to the neutral, which will be able to take care of any unbalance that could happen during the start-up of the ac-dc LED driver. In fact, this unbalance comes in the form of couplings between the three cells, which can cause the input voltage and currents of each cell to change abruptly. This is critical when an MBC is used, as an abrupt change in its input voltage will cause the control to misbehave aggravating the problem even further.

In order to overcome the presented issue, [2.7] details the required start-up control for a three-wire Delco topology with a cell based on a PFC converter with MBC. The start-up takes care of controlling the intermediate bus voltage in each cell in order to ensure that all the cells demand the same amount of power guaranteeing the input voltage of each cell to be sinusoidal.

The start-up procedure is based on carefully following four stages, which modify the intermediate bus voltage of one the cells (i.e., voltage on C_N) in accordance to Fig. 2.33. The first stage takes place from t_0 to t_1, during which time neither the PFC converters nor the dc-dc converters are being controlled, and C_R, C_S and C_T are being charged to half the peak value of the phase-to-phase voltage. Basically during this time the intermediate bus capacitors are being charged by being directly connected to the three-phase power grid, which can cause current spikes on the input. For that matter, a pre-charging diode will suffice in most scenarios. However, in those that not, the current spikes are reduced controlling the conduction angle of the phases by means of thyristors [2.7].

The first stage ends when all three capacitor reach their maximum attainable voltage value. Point at which, the second stage from t_1 to t_2, starts by controlling the PFC converters with no load. Hence, the intermediate bus capacitor is able to be charged to higher values than the half peak value of the phase-to-phase voltage. This stage finishes whenever the voltage of the intermediate bus capacitor in any of the cells reaches the steady state voltage value set by the design, point at which the dc-dc converter of that cell will start operating.

It should be noted that for the proposal of removing the electrolytic capacitor in a two-stage cell, whenever the first dc-dc converter is started-up, the load is instantly connected to that cell discharging the intermediate bus capacitor. Since the capacitance is lower than for an electrolytic capacitor, the energy stored will also be low, causing with this connection a diminishing of the intermediate bus voltage that can be counter-productive. Therefore, a soft-start is absolutely required to guarantee a correct operation, which is the only start-up specification that the dc-dc converter will require.

The next stage from t_2 to t_3, represent the time it takes for all the cells to have their dc-dc converter operating. Time after which the ac-dc LED driver will be correctly operating in steady state after overcoming the transients that occur during the last stage from t_3 to t_4.

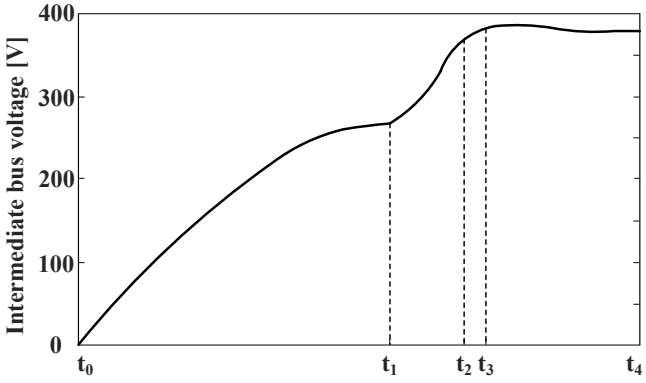


Fig. 2.33. Intermediate bus voltage during the start-up procedure of one of the two-stage cells of the Delco ac-dc LED driver.

2.6.2 Basic operation of the two-stage Delco ac-dc LED driver

In order to test the previous affirmations, a prototype has been designed and built based on three building blocks. The first block represents the PFC converter which is designed by means of a boost converter achieving an LFR performance with a MBC receiving an input voltage in the European three-phase voltage range. The second block is based on a fixed ratio dc-dc converter from VICOR (i.e., BCM384F480T325A00) [2.47]. The VICOR module is a ZVS/ZCS resonant sine amplitude converter that receives a voltage of 384 V and outputs 48 V at maximum load with a fixed ratio of 1/8. The maximum power that this module is able to process is 325 W, if its temperature is correctly controlled. And the third block, is the central control unit that takes care of the start-up of the converter, the auxiliary voltage supply of the control of each cell and the central control that isolates and sets the v_c value of each PFC converter.

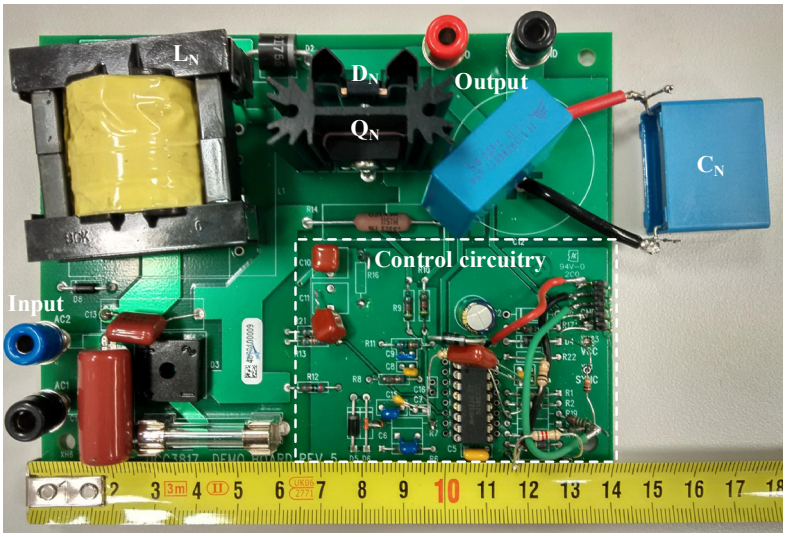
It should be noted, that in this particular case, and unlike the previous scenario, all the control has been carried out by means of analog circuitry. In addition, not all the control is inside the central control unit in order to have independent building blocks, see Appendix B for more information. For that matter, the first block, see Fig. 2.34 (a), also includes all the circuitry related to achieving an LFR performance. This building block is based on a commercial evaluation board, UCC3817EVM [2.48], which has been modified to the needs of the design while keeping the same ICC based on the UCC3817 switching

Table 2.9. Components of the PFC boost converter.

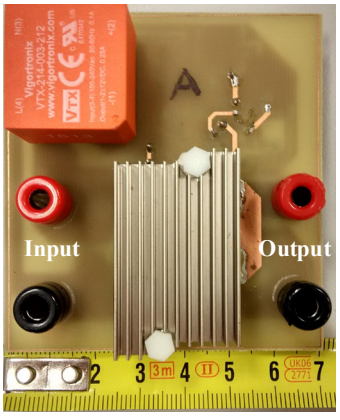
Fig. 2.12 reference	Value
L_1, L_2 and L_3	1.7 mH – ETD39 – 3F3
Q_1, Q_2 and Q_3	IPW65R190C7
D_1, D_2 and D_3	IDH06SG60C
C_R, C_S and C_T	10 µF 100 V Film Cap.

at 100 kHz. Consequently, changes have been made to the power stage in order to make it more efficient, and whose components are summarized in in Table 2.9. The control stage of the cell has also needed to undergone some changes to efficiently communicate to the central control unit in order receive an auxiliary isolated voltage supply to feed the control, a signal to start the control in accordance to the start-up procedure previously detailed and v_c, while sending the intermediate bus voltage data.

Furthermore, the second building block depicted in Fig. 2.34 (b) is not only comprised of the VICOR module, but it also includes some analog circuitry that decides when the VICOR module should start-up conditioned to its input voltage. In that sense, a comparator followed by an R-S latch is used, the comparator decides when the input voltage is enough to start-up the module, whereas the R-S latch guarantees that the first moment the comparator output its set to '1' the module will be working indefinitely, in order to avoid false activations and deactivations of the VICOR module. Unless, of



(a)



(b)

Fig. 2.34. Designed two-stage cell for a Delco ac-dc LED driver. (a) PFC boost converter based on the UCC3817EVM. (b) Isolated dc-dc converter based on the BCM384F480T325A00.

course, a malfunction is detected and the module is turned-off. More information regarding the analog control and its operation can be found in Appendix B.

The whole Delco ac-dc LED driver based on a two-stage approach is depicted in Fig. 2.35, showing all three cells and the central control unit. The latter is comprised of the isolated power supplies that feed the control of all three cells, a comparator per cell that decides when to start-up the PFC converters based on their intermediate bus voltage and the control loop responsible for setting v_c for all of the cells. Please note that all the signal that are send and received from the cells are carefully isolated for a correct operation of the ac-dc LED driver, see Appendix B for more information.

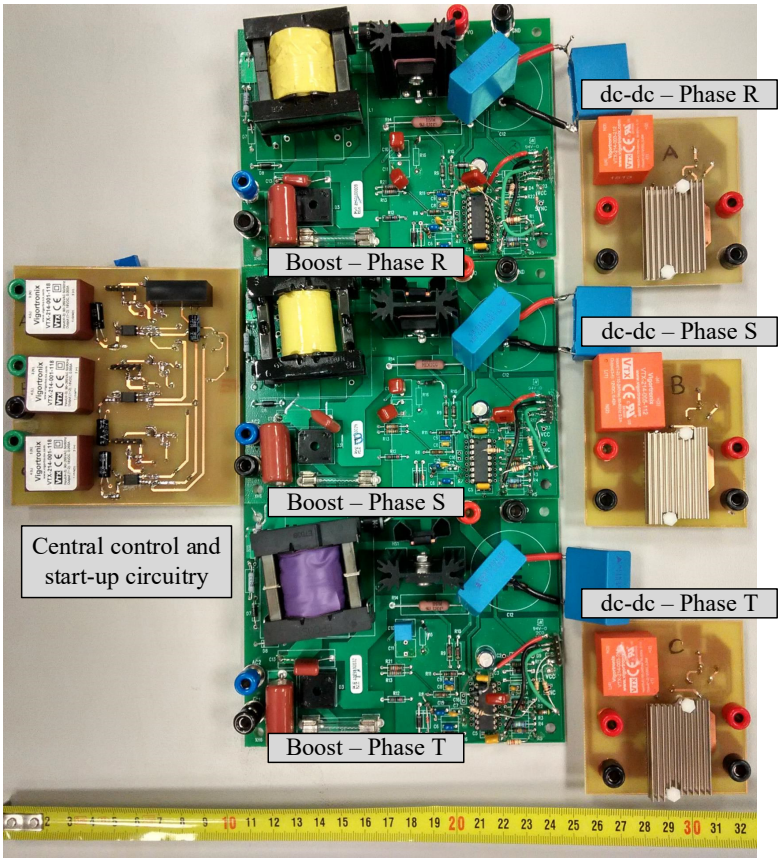


Fig. 2.35. Prototype of the Delco ac-dc LED driver based on two-stage approach per cell, with its central control unit.

The ac-dc LED driver is designed for a total power of 1 kW, however, due to the temperature limitations of the VICOR modules it has been tested up to 400 W, connected to the real three-phase power grid, with an auto-transformer as the interface, feeding a resistive load. The reason for using a resistive load to test the two-stage Delco ac-dc LED driver was to avoid building a bulky LED load, as the flicker performance of the Delco LED driver has already been validated in Subsection 2.5.3 and the aim of the current subsection is detailing the operation of the two-stage that comprise each cell.

The first test carried out has been at 400 W measuring the input currents of each phase and the phase voltage of phase R, see Fig. 2.36. As can be seen, $i_R(t)$ follows adequately the shape of $v_R(t)$ guaranteeing an almost unity PF. Accordingly, the almost unity PF can be assumed for the other two phases considering they are adequately phase shifted at the mains frequency. For the sake of completion, Fig. 2.37 (a) and (b) show the input currents and phase voltage for all the phases of the ac-dc LED driver taking phase R as a reference to correctly exemplify the achievement of an LFR performance of all the cells that comprise the two-stage Delco ac-dc LED driver. As can be seen, all phases demand very similar waveforms in phase with their voltages, which also ensures that the power demanded by each phase is extremely similar.

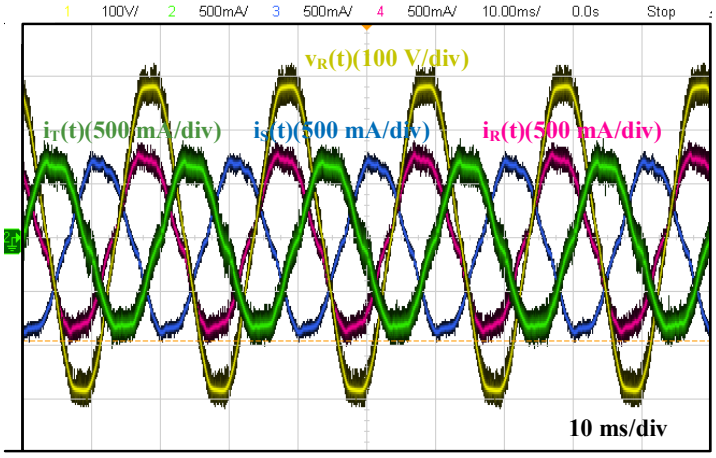


Fig. 2.36. Input currents for all three phases and input voltage of phase R of the two-stage Delco ac-dc LED driver.

This last statement is of utter importance when considering the removal of the electrolytic capacitor in a three-phase ac-dc LED drivers. In fact, in comparison with the flyback cell discussed through Section 2.5, a PFC converter with an MBC suffers much less from the tolerances of the components. The reason can be easily understood by observing Table 1.1, as can be seen, most of the converters summarized have a dependency of K_1 with their inductance or coupled inductance whereas the PFC boost converter with MBC just depends on G_1, which is the gain of the current sensing method. The tolerances of the magnetic components used in power electronics, whether they are custom designed or bought commercially tend to have a 10-20% tolerance. In contrast, cheap sensing methods with 1-5% tolerances can be found commercially, even those based on resistive components. Hence, it is easier to design PFC boost converters based on MBC with similar R_{LFR} values than it is for flyback converter.

In fact, the similar R_{LFR} values between the three cells translate in an almost constant output voltage as can be seen in Fig. 2.38. Taking into account that the power demanded by each phase is pulsating at twice the mains frequency, it is only reasonable for the output current of each phase to pulsate at that same frequency. Hence, demonstrating the correct operation of this Delco ac-dc LED driver without electrolytic capacitor.

Finally, Fig. 2.39 shows the implemented start-up of the driver following the method introduced in the previous subsection to exemplify is correct operation. As can be seen,

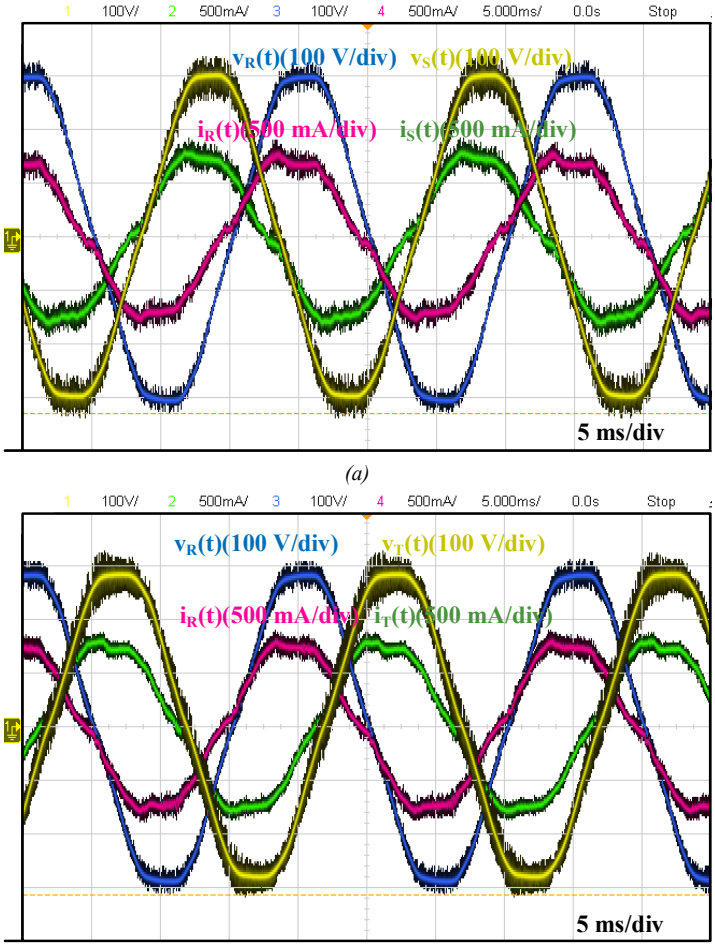


Fig. 2.37. Input currents and phase voltages for all three phases of the two-stage Delco ac-dc LED driver. (a) Phases R and S. (b) Phases R and T.

the control of the PFC converters does not start-up until a certain voltage is reached on the intermediate bus voltage, $v_{CN}(t)$, of all the cells. Point from which the PFC converters are soft-started accordingly. Then, when $v_{CN}(t)$ reaches 380 V, the dc-dc converter is started as the dc-dc start-up signal is turned-on, which explains the voltage drop that occurs on $v_{CN}(t)$, see Fig. 2.39. After this time, the transient caused by the control occurs and the ac-dc LED driver is properly operating.

2.6.3 Evaluation and compliance with regulations of the two-stage Delco ac-dc LED driver

After having exemplified the correct electrical operation of the two-stage Delco ac-dc LED driver, it is necessary to check different parameters of interest to further validate the operation of this topology as an ac-dc LED driver. For that matter, the waveforms shown

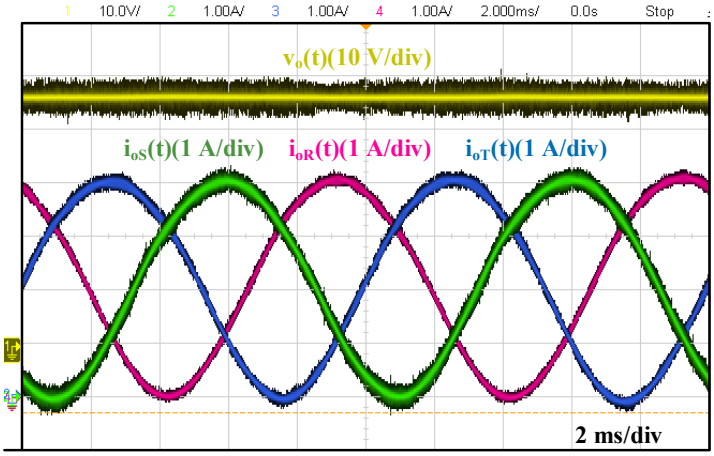


Fig. 2.38. Output voltage and currents of the two-stage Delco ac-dc LED driver.

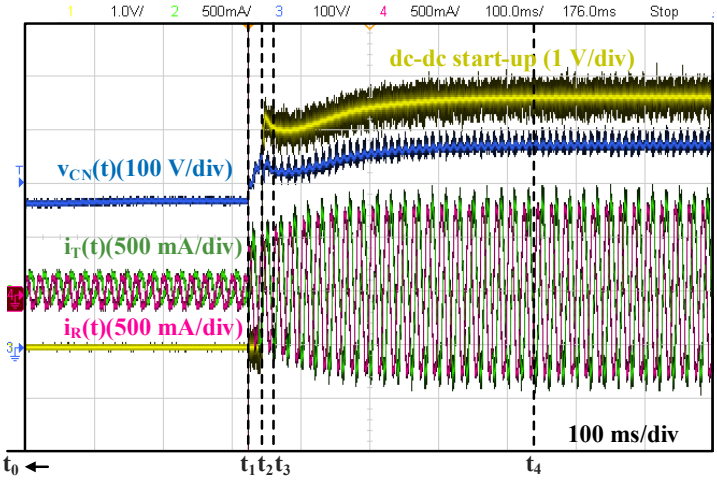


Fig. 2.39. Validation of the start-up procedure for the two-stage Delco ac-dc LED driver.

in the previous graphs will be extracted from the oscilloscope as data and will be carefully analyzed.

The first analysis is carried out by extracting the input currents to establish whether the Delco ac-dc LED driver with a two-stage cell complies with the harmonic injection regulation. For that matter, each of the harmonics have been extracted and compared to the limits set by the regulation, see Fig. 2.40. As expected, the LED driver has no problem complying with the IEC 61000-3-2 [2.43].

In addition, Table 2.10 summarizes THD, PF and efficiency when the input line voltage is varied within the limits set by the European three-phase power grid for each of the three-phases. As can be seen, the results obtained between the three-phases in terms of THD and PF are alike, validating the idea of this kind of cell having much similar R_{LFR} values without including more complex control methods. It should also be noted that the

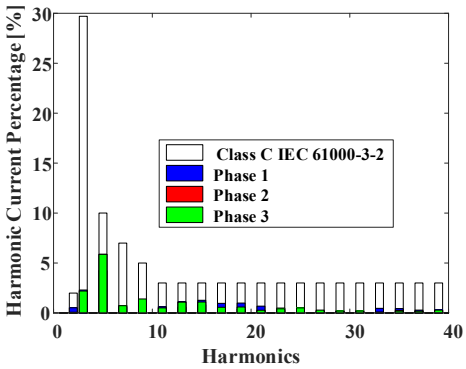


Fig. 2.40. Harmonic content of each phase for the Delco ac-dc LED driver based on a two-stage cell, compared with the harmonic limits set by Class C from the IEC 61000-3-2 [2.43].

efficiency, is higher than it was for the previous three-phase ac-dc LED drivers, at the cost of including more components.

Nonetheless, the efficiency plummets much faster when reducing the output load than in the previous scenario, particularly due to the lower efficiencies that the dc-dc converter of VICOR provides under low load scenarios, see Fig. 2.41. It should be noted that in order to obtain Fig. 2.41 all the losses have been considered (i.e., auxiliary supplies, driving, power stage, etc.)

In summary, the two-stage ac-dc LED driver, as it was the case for single-phase ac-dc LED drivers, should be considered when a more efficient drivers is to be obtained when the cost is not the most limiting factor.

2.7 Experimental results for the multi-cell ac-dc LED driver based on summing the light output of each phase

After having tested the Delco ac-dc LED driver with a two-stage cell, this section analyzes the ac-dc LED driver derived from removing the dc-dc converter of the cell. Hence, the cell is comprised of a PFC converter and an LED string connected at its output. Consequently, the experimental prototype of the PFC converter is the same one introduced in the previous section, see Fig. 2.34 (a), taking into account the modifications introduced for the power stage in Table 2.9.

The ac-dc LED driver is designed in such a way that each cell requires to drive an LED load comprised of two strings in parallel that contain 20 LEDs (i.e., Luxeon 5050 L150-5770502400000 with $\max\{p_{LED}/P_{base}\}$, see Table 2.3), which are equivalent to 490 V at 100 W (i.e., $v_{gn} = 0.65$ and $i_n = 0.12$). In fact, the number of LEDs connected in series on a string is not done at random, and is picked ensuring that the sum of knee voltages from the LEDs at the operating temperature is higher than the maximum input voltage in the worst case scenario of the three-phase power grid, which is around 420 V for the European three-phase power grid. This fact is of utter importance as inherently a boost converter is only capable of increasing its output voltage. Otherwise, the ac-dc LED driver under study would not be able to guarantee full dimming operation, as there would exist a phase angle at which the LED load would be conducting all the time due to the phase voltage being higher than the knee-voltage of the LED load.

Table 2.10. Summary of THD, PF and efficiency for different input line voltages for the two-stage Delco ac-dc LED driver.

Phase/ Max. input voltage		R	S	T
380 Vrms	THD [%]	6.5	6.63	6.77
	PF	0.997	0.996	0.997
	Efficiency [%]		92.3	
400 Vrms	THD [%]	6.8	6.85	7
	PF	0.996	0.996	0.996
	Efficiency [%]		92.9	
420 Vrms	THD [%]	7.1	7.2	7.32
	PF	0.993	0.992	0.992
	Efficiency [%]		93.4	

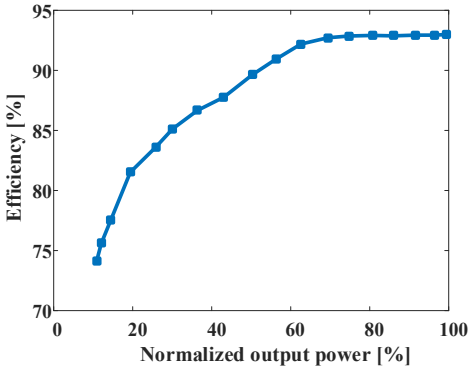


Fig. 2.41. Efficiency versus output power for the Delco ac-dc LED driver based on a two-stage cell.

Fig. 2.42, shows a photograph of the designed prototype to validate the idea of using the light output of each cell to drive an LED load. In particular, in the photograph the three cells can be observed, as well as, the central control unit and the designed LED load. The latter has its strings distributed as shown in the figure to ensure a better blend of the light coming from each the phases.

Similarly to the Delco ac-dc LED driver based on a two-stage cell, the central control unit takes care of both the start-up of the LED driver, and giving the command to each cell to feed the LED loads with the same amount of current. Particularly, the implementation of the start-up is exactly the same, but taking into account that the dc-dc converter is non-existent in the cell. Then, that step is to be skipped (i.e., the interval between t_2 and t_4 in Fig. 2.33). In reality only an isolated signal is required to be given to each of the cells to start-up the PFC converters. More information on this matter can be found on Appendix B.

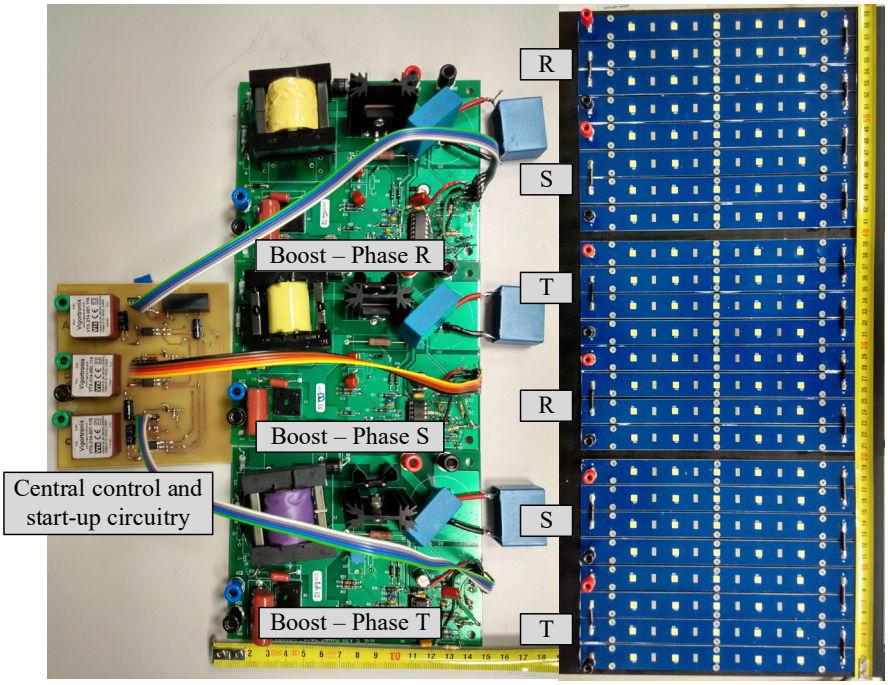


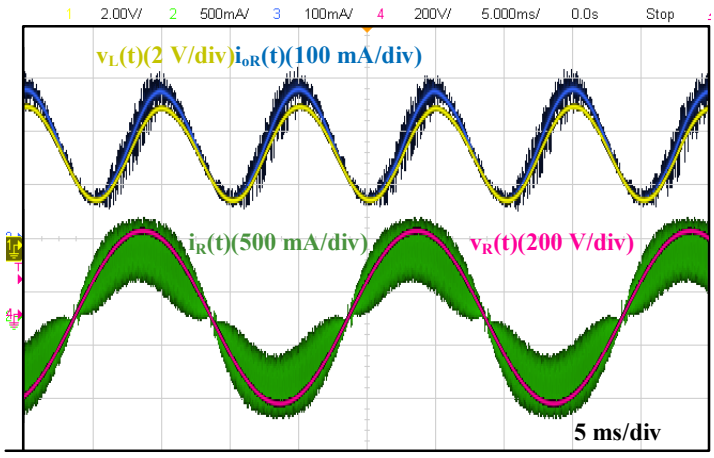
Fig. 2.42. Protype of the multi-cell ac-dc LED driver based on summing the light output of each phase.

Operation of the cell in terms of its output capacitance

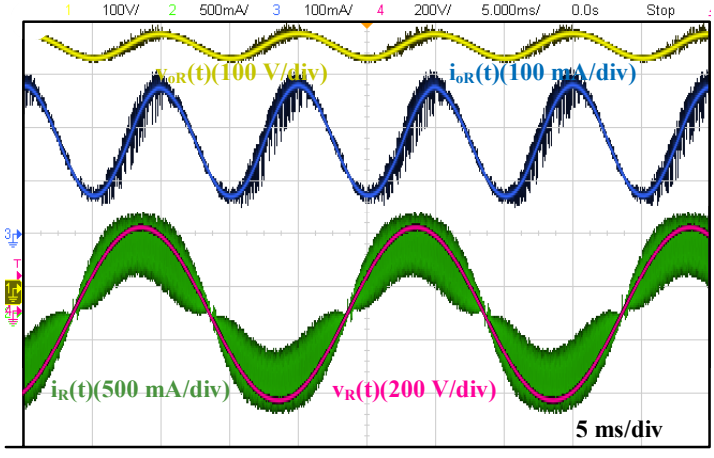
The first experimental test carried out for this prototype was performed to validate the operation of one of the cells by connecting it to a single-phase power grid at its input and an LED string at its output allowing a high current and voltage ripple under low output capacitance.

In that sense, Fig. 2.43 shows that the input current is adequately in phase with the input voltage ensuring, as expected, an LFR performance at the maximum output power of the cell while working in CCM. It should be noted that, Fig. 2.43 (a) depicts the high output current ripple due to the use of a 10 µF capacitor and the light output measured with a transimpedance amplifier (i.e., TSL-257), located at a fixed distance of 20 cm. The transimpedance amplifier supplies at its output a certain voltage, $v_L(t)$, proportional the light falling upon the photodiode. As can be seen, the output current and luminance follows an almost linear relationship, validating the required condition supposed for the sum of the lights of each phase.

In contrast, Fig. 2.43 (b) shows the voltage withstood by the LED load, in which the lowest voltage never falls below the 400 V mark set before. However, this is the best-case scenario, as the lowest current is far from being zero, to test whether the selection of the LED load is acceptable. In order to validate an adequate performance in terms of its output voltage, Fig. 2.44 shows a snapshot of the oscilloscope when dimming the driver to an output power of 25 W, in which it can be seen that the output current reaches the zero value. Point at which the minimum output voltage of the LED load is reached being



(a)



(b)

Fig. 2.43. Standalone operation of one of the cells that comprise the multi-cell ac-dc LED driver based on summing the light output of each phase at maximum power, depicting both input and output current, input voltage and (a) measured luminance and (b) output voltage.

slightly higher than 400 V, guaranteeing that its value is always higher than the maximum peak voltage of the grid.

Although the operation for the designed LED load has been validated, the analysis carried out in terms of the output capacitor has not. For that matter, Fig. 2.45 summarizes three different measurements of current across the LED load performed at maximum output power considering that the output capacitor value is the only thing that varies between the measurements. In order to be able to compare them in between and with the theoretical model previously presented in Subsection 2.4.1.2, these measurements were extracted from the oscilloscope as data. As can be seen, the higher the value of the output capacitor, the lower the current ripple. Furthermore, the comparison with the theoretical model show that it is extremely accurate.

2.7.1 Basic operation of the multi-cell ac-dc LED driver based on summing the light output of each phase in a real three-phase power grid

After having validated the operation of the cells individually, the ac-dc LED driver has been assembled and connected to the real three-phase power grid, again, by means of an auto-transformer used as the interphase between the grid and the LED driver. Under these conditions the waveforms presented in Fig. 2.46 have been obtained from the oscilloscope at maximum load (i.e., 300 W). Fig. 2.46 (a) depicts the input waveforms of the three-phase LED driver, to exemplify the LFR performance of each of the PFC converters. Particularly, it can be seen that the input voltage of phase R is followed by the

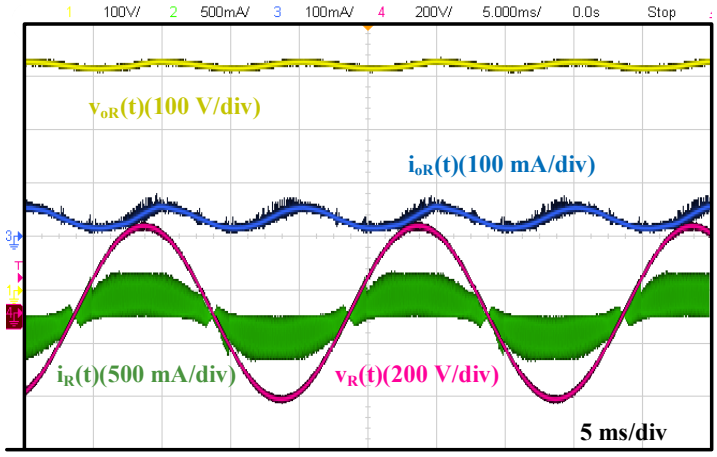


Fig. 2.44. Standalone operation of one of the cells that comprise the multi-cell ac-dc LED driver based on summing the light output of each phase at a quarter of the maximum output power.

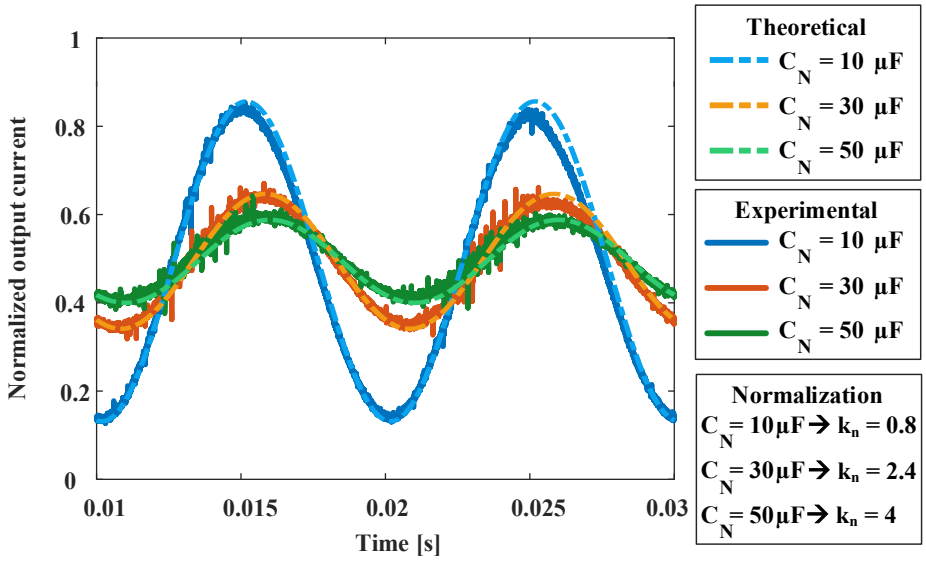
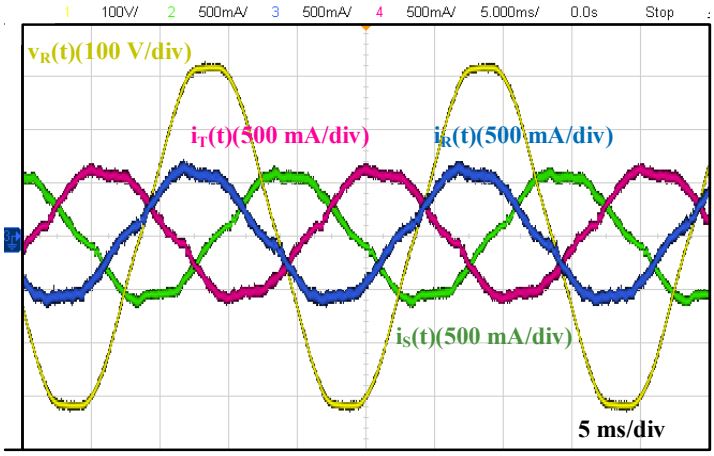


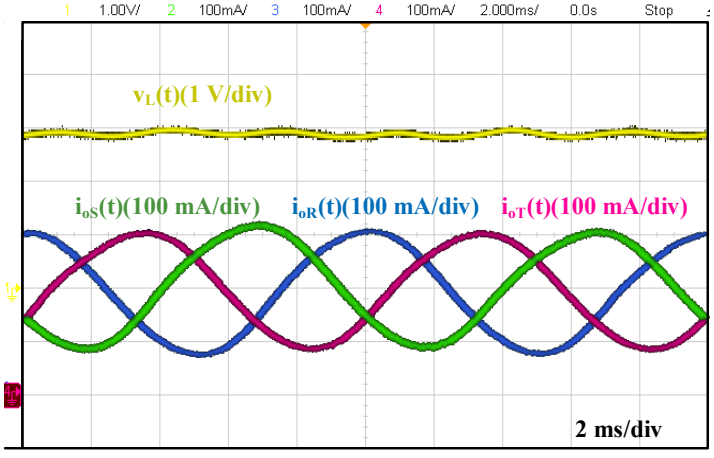
Fig. 2.45. Output current across the LED load of a cell when varying the output capacitor of the cell.

input current demanded by the same phase. In addition, taking into account that the ac-dc LED driver input performance is exactly the same as the one shown in Section 2.6, it can be concluded that unity PF is achieved.

From the point of view of the output, Fig. 2.46 (b) displays the current across the LED load of each cell while processing the same amount of power, hence why the current across them show extremely similar current levels. Its sum, measured again with a transimpedance amplifier in this case at a fixed distance of 60 cm, is comprised of a dc level with a low frequency ripple at 300 Hz. Considering the amplitude of this ripple the light output of the driver can be considered to be constant. In fact, Fig. 2.47 displays a snapshot showing the performance of this ac-dc LED driver at 25 W, where it can also be seen the similarity between the output currents with the adequate phase-shift between the phases and an almost constant output luminance.



(a)



(b)

Fig. 2.46. Experimental waveforms of the multi-cell ac-dc LED driver based on summing the light output of each phase at maximum load. (a) Input voltage and currents. (b) Output currents and measured luminance.

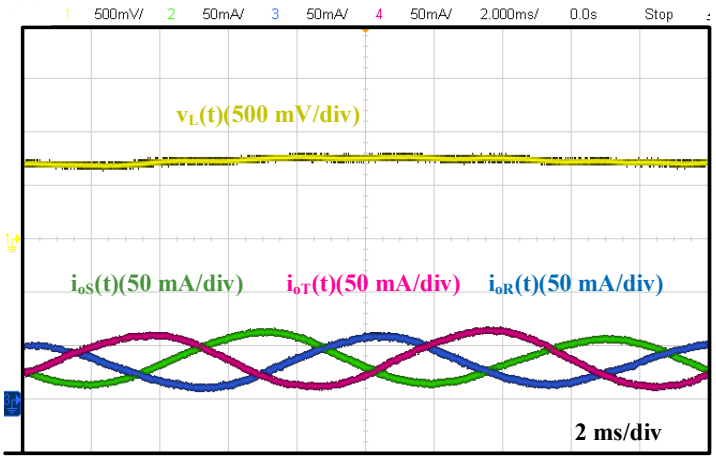


Fig. 2.47. Experimental output waveforms of the multi-cell ac-dc LED driver based on summing the light output of each phase at a quarter of the maximum load.

2.7.2 Evaluation and compliance with the LED regulation of the multi-cell ac-dc LED driver based on summing the light output of each phase in a real three-phase power grid

The almost constant measured luminance of the driver validates the mathematical analysis carried out in Subsection 2.4.1. However, the low frequency ripple needs to be evaluated in detail to ensure a flicker free performance. In that respect, compliance with the IEEE standard 1789-2015 is used to determine whether this LED driver can output a flicker free light output. Thus, v_L has been extracted from the oscilloscope and has been carefully analyzed to determine its harmonics. As can be seen in Fig. 2.48, each Mod.[%] harmonic falls within the shaded region defined in [2.45], ensuring a flicker free performance.

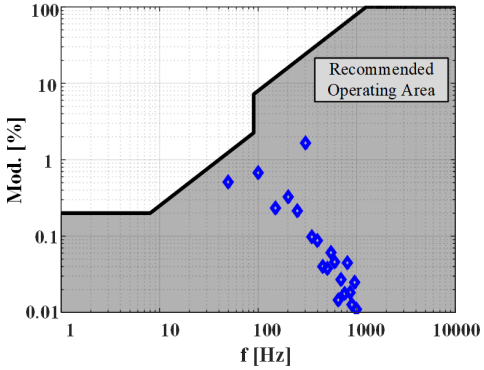


Fig. 2.48. Recommended flicker operation operatio for the multi-cell ac-dc LED driver based on summig the light output of each phase [2.45].

After having validated the flicker free performance of this LED driver, there are two characteristics that need to be evaluated in order to close the analysis. The first one is the compliance with the harmonic injection regulation IEC 61000-3-2. Again, the harmonic

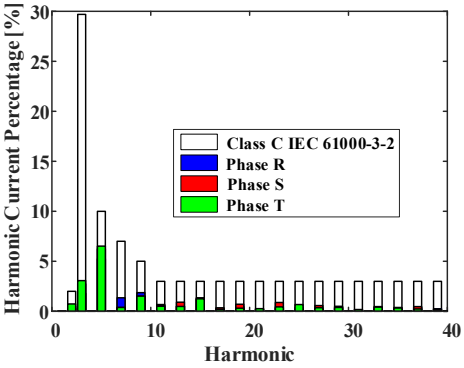


Fig. 2.49. Harmonic content of each phase for the multi-cell ac-dc LED driver based on summing the light output of each phase, assuring compliance with Class C IEC 61000-3-2 [2.43].

content of the input currents have been extracted from the waveforms and have been compared to the limits, showing their compliance, as can be seen in Fig. 2.49.

The second characteristic is the efficiency of the driver, which has been measured under different dimming conditions at 400 Vrms line to line. This measurement is not trivial as there is a quite heavy ac component at the output of each cell. Thus, the input power has been measured for each of the phase and the output power has been calculated as the product of the voltage withstood by the LED load multiplied by the current across it and averaged within a line period to attain the average power consumed by the LED load. Then, summing the input power and output power and dividing them renders the actual efficiency of the ac-dc LED driver considering all the actual losses of the prototype, see Fig. 2.50. As can be seen the driver attains a maximum electrical efficiency of 97.5% at full load, which is equivalent to 42.000 lm, outputting a luminous efficacy of 140 lm/W.

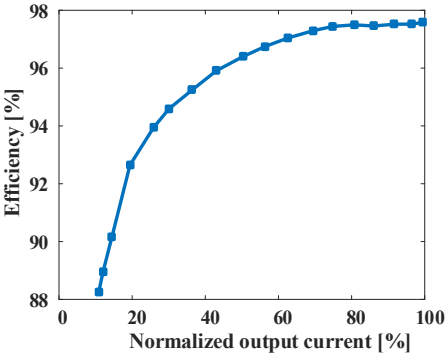


Fig. 2.50. Electrical efficiency measured under different dimming condiations at 400 Vrms line to line for the multi-cell ac-dc LED driver based on summing the light output of each phase.

Finally there is another set of parameters that are of interest and which are summarized in Table 2.11 at full load for three different line to line voltages. These parameters are THD, PF and electrical efficiency, and as can be seen the measured THD is about 7%, a unity PF is attained and the minimum electrical efficiency achieved is 96.9% for the

lowest line to line voltage, while the highest is achieved for the maximum input voltage attaining a 98.2% electrical efficiency.

Table 2.11. Summary of THD, PF and efficiency for different input line voltages for the multi-cell ac-dc LED driver based on summing the light output of each phase..

Phase/ Max. input voltage		**R**	**S**	**T**
380 Vrms	THD [%]	6.7	6.8	7
	PF	0.997	0.997	0.997
	Efficiency [%]		96.9	
400 Vrms	THD [%]	6.7	7.1	7.3
	PF	0.995	0.995	0.995
	Efficiency [%]		97.5	
420 Vrms	THD [%]	7.4	7.6	7.9
	PF	0.992	0.992	0.997
	Efficiency [%]		98.2	

2.8 Conclusions

This chapter concludes the proposition of three different ac-dc LED drivers, which in accordance to the classification made in Chapter 1 fall under the three-phase multi-cell category. In addition, these drivers are able to remove the most limiting component in terms of lifetime as is the electrolytic capacitor, and can be further divided in terms of their achievement of galvanic isolation or not.

The ones that achieve galvanic isolation which are the Delco ac-dc LED driver and the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier have been adequately analyzed and experimentally validated complying with the required regulations. The Delco ac-dc LED driver is based on the Delco topology, which is commonly used for ac-dc three-phase power converts, whereas the other is an original topology. Because of their similarities regarding their modularity both topologies have been compared using flyback converters as the LFR cells of either of the ac-dc LED drivers as a first approach to validate their operation.

In terms of efficiency the study showed a slight improvement of performance for the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier over the Delco ac-dc LED driver, which is achieved due to two advantages:

- The lower number of low frequency diodes conducting at the same time.
- The operation of the cells during half-line cycle, which is able to achieve lower operating temperatures on the cells. Thus, improving their overall performance.

However, these advantages do not come freely as there are another two disadvantages to take into account:

- There is a necessary increase of components, in fact almost doubling the amount of the Delco LED driver, taking into consideration that it uses a double amount of LFR cells.
- The increased amount of LFR cells directly affects the reliability of the systems as the mean time between failures is theoretically reduced.

Nonetheless, the disadvantages can be justified specially in terms of cost when designing high-power spotlights up to 10 kW as the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier scales better than the Delco ac-dc LED driver. It should be noted that for these higher spotlights, there are some changes that need to be made on the ac-dc LED driver, as the LFR cell based on a flyback converter will not be suitable due to the efficiency limitation, thus, limiting the maximum power.

In that sense, there are two strategies that can be used or even combined:

- The use of a more suitable LFR cell based on a two-stage approach.
- The use of several LFR cells by means of their serialization or parallelization. This approach considers the LFR cells as building blocks, then, it is a matter of designing a highly efficient cell and multiply it as required for the ac-dc LED driver design.

However, the use of a two-stage approach complicates the start-up of the ac-dc LED driver requiring more control for a three-wire connection to the three-phase power grid. Then, the selection between the two methods or its combinations ends up being a trade-off between number of components, efficiency, reliability and cost.

Taking into consideration the previous statements and under the assumption of an optimized cell the recommendation is to use the Delco ac-dc LED driver for low power luminaires, and the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier for high power and high performance luminaires. The limit between one solution and the other needs to be further studied in terms of the required design.

The other proposed topology, in this case without galvanic isolation, is the multi-cell ac-dc LED driver based on summing the light output of each phase. The approach taken is quite similar to the two-stage Delco ac-dc LED driver, but in this case the second stage is removed driving the LED loads with high voltage and current ripple. By leveraging the properties of the light, the light output of each phase is blended together attaining an almost constant light output without the use of an electrolytic capacitor. Even though, any PFC converter can be used for this ac-dc LED driver, disregarding whether the PFC converter achieves galvanic isolation, the proposed implementation is based on boost converters with PFC. This implementation of the cell is only possible thanks to HV LED loads, which are made simpler due to HV LEDs.

The multi-cell ac-dc LED driver based on summing the light output of each phase has a handful of advantages over its galvanic isolated counterparts or the previous works introduced in literature:

- It is able to achieve higher efficiencies.
- It is able to drive high power luminaries with a lower component count.
- Any topology able to work as an LFR is prone to be used as the cell of the ac-dc LED driver.

Furthermore, in comparison to the HV LED driving proposed on single-phase ac-dc LED drivers [2.21], it does not require the use of more complex control methods, such as the injection of the third harmonic, as long as an LFR performance of the cell is guaranteed.

As any of the presented multi-cell ac-dc LED drivers, the main drawback comes in terms of controlling the LFR cells to demand the same amount of power and its reliability, however, with a MBC the tolerances almost have no impact on the light output of the ac-dc LED driver, achieving a better performance in terms of flicker. In fact, as has been studied, the use of an output capacitor on the cells is only a matter of reducing the current ripple through the LED load. Otherwise, the amount of LEDs comprised in the LED load might need to be increased to satisfy the operation at the peak current values, which could be much higher than their maximum ratings. In addition, the low frequency current ripple that does not pose a drawback in terms of luminous efficacy, needs to be further studied to foresee how it affects the lifetime of the LEDs.

In conclusion, the ac-dc LED drivers introduced in this chapter, are proposed for stadiums, industrial, or commercial environments, where high-power spotlights are required and three-phase grids are available. The availability of the three-phase power grid is in fact key, as the aim of proposing the use of three-phase ac-dc LED driver is not to replace the current single-phase power grid massively used in household environments, but use the readily available one for high power luminaires.

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3

Single-phase single-stage current-fed ac-dc LED driver: dual inductor current fed push-pull

We tend to have the fond idea that scholarship is always marching forward in its evolutionary stride, constantly progressing. The reality is that it's like a tide — sweeping in and out with the waves of fashion, throwing up beautiful shells on the beach along with garbage and then sucking them back into the ocean.

— Reality, Peter Kingsley.

The present chapter discusses the use of current-fed topologies to drive LEDs in single-phase power grids. Current-fed topologies are isolated variants of the PFC boost converters, and in contrast to the PFC boost converter they have rarely being used as PFC converters due to their several limitations. Overcoming their limitations is the aim of this chapter in order to attain topological solutions that improve the current single-stage power converters found in literature. Thus, the dual inductor current-fed push-pull has been retrieved and studied in detail. Unlike, its conventional operation as a high gain step-up dc-dc converter, its feasibility as a PFC converter needs to be carefully analyzed both statically and dynamically due to their promising features. This analysis proves to be key in order to propose an adequate method for its control as a PFC converter while only requiring a single sensing point in the circuit. Furthermore, the proposed operation is based on operating both inductors in BCM, achieving a lower ripple input current taking advantage the intrinsic interleaving of the topology . In fact, taking into account all of the advantages and overall outstanding characteristics of this topology, the proposal is using it as a single-phase single-stage ac-dc LED driver. This ac-dc LED driver is constructed and experimentally validated at the end of the chapter feeding several LED strings operating for the full input voltage range of the US ac power grid.

3.1 Introduction

Chapter 1 introduced and detailed several single-stage ac-dc topologies used for the task of driving LEDs from single-phase ac power grids. All of these different topologies, methodologies and strategies reassure the importance of this research topic. Particularly, for LED luminaires with primary access to single-phase ac power grids requires the use of an ac-dc power converter with a high efficiency, a long lifespan, able to achieve PFC, while also feeding the LED load with a constant current.

The requisite of achieving PFC, as a reminder, is key to comply with both, ENERGY STAR® and IEC 61000-3-2, which stablish very strict harmonic content limitations of the line current of an ac-dc LED driver used to drive LED luminaires [3.1], [3.2]. Traditionally, the approach to comply with the aforementioned regulations is based on using a converter able to operate as an LFR, which normally includes galvanic isolation for safety reasons. Taking into account that single-stages are used when the cost and simplicity of the ac-dc LED driver are the main concern, isolated buck-boost topologies, such as the flyback converter operating in DCM are massively used for this application [3.3]-[3.7]. However, a traditional flyback converter suffers from low efficiencies and has an inability of removing the electrolytic capacitor. The latter, of course, is an impossibility on most single-stage ac-dc power converters, unless one of the methods introduced for this particular task in Chapter 1 is used, turning that single-stage into a quasi-single-stage [3.8]-[3.10].

The other massively used strategy to comply with the regulations, which has also been discussed in Chapter 1, is the use of a two-stage ac-dc converter comprised of a PFC boost converter followed by an isolated dc-dc converter. The PFC boost converter is able to attain an LFR performance under different control methodologies, thus, its isolated counterparts (i.e., current-fed isolated converters) should operate accordingly, being able to achieve unity PF. However, current-fed isolated converters are rarely used in PFC due to the several drawbacks they present: complex transformer design, low efficiencies, the requirement of a demagnetizing path to protect the main switches in case of a control failure and the lack of analog ICs capable of generating their control signals [3.11]. The latter has been solved, nowadays, by means of digital control.

Nevertheless, previous literature does include some papers on single-phase single-stage current-fed ac-dc converters, such as, the push-pull converter [3.12] or the full-bridge converter [3.13] both operating in CCM with an MBC, which, as expected, underperform in terms of efficiency in comparison to the current state-of-the-art single-phase single-stage ac-dc LED drivers, while not addressing any of the issues of current-fed topologies.

Among the current-fed push-pull topologies, the Dual Inductor Current-fed Push-Pull (DICPP), see Fig. 3.1, proposed in [3.14] as a dc-dc converter. The DICPP shows significant advantages in terms of efficiency, voltage stress or output capacitor size (i.e., at switching frequency and not at the mains frequency), in comparison to the traditional current-fed push-pull (CPP). In accordance to [3.15], which compares these two topologies, the advantages, in efficiency, come from the better utilization of magnetic components due to:

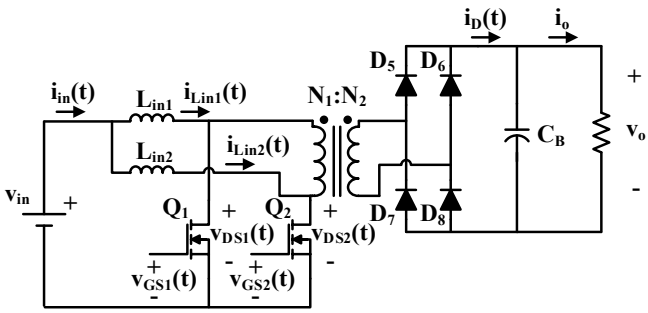


Fig. 3.1. Conventional DICPP topology working as a dc-dc converter with a resistive load.

- Each inductor having less current stress considering that the input current is equally distributed between the two.
- The transformer design being reduced in size according to the lower volt-ampere rating, in comparison to the CPP. In addition, the simpler transformer of the DICPP (i.e., two windings one for the primary and another for the secondary side) allows a better optimization of its design, however, this is not the only reason. The other reason comes from the main switches withstanding half the voltage of the CPP, which translate in a transformer that requires by design less isolation.

All the advantages that the DICPP presents come at the cost of only adding an extra magnetic component, and they are of utter importance to reduce the parasitic components of the transformer. These parasitic components are, in fact, the ones that hinder the performance of single-phase single-stage current-fed ac-dc converters, thus, reducing their values by improving the transformer design will also remove the main drawback of this topologies for PFC.

The reason for the previous statement, can be understood taking into account that conventionally current-fed topologies are used for high gain step-up applications, in which, the transformer is but another tool to help increase the gain, such are fuel cells, battery storage, photovoltaic or electric vehicle applications [3.16]-[3.19]. Particularly, these applications operate with high currents on the primary side and low currents but high voltages on the secondary side. In contrast, for low output voltage PFC applications, such as ac-dc LED drivers, the requirement is just the complete opposite, and the power converter needs to step-down the input voltage to the required by the load, which is achieved using the transformer gain. This causes a low input current in the primary side of the converter, which in conjunction with the leakage inductance and the primary lumped parasitic capacitance causes a resonant output current to appear, as analyzed in [3.20] for the CPP. It is, in fact, this resonance the one that causes no power transfer to occur for the lower input voltages of the power grid, hindering the efficiency of the solutions. Therefore, by lowering this two parasitic parameters this issue can be completely avoided.

The aim of this chapter is to retrieve and revise the most promising of the current-fed topologies (i.e., the DICPP) for operation as a single-phase single-stage ac-dc LED driver. Therefore, it is necessary to carefully study its operation in order to achieve an efficient

and simple solution that could operate as a single-stage for high output power in the ac-dc LED driver field (i.e., > 50 W). It should be noted that being the aim the design of a single-phase single-stage ac-dc LED driver, the removal of the electrolytic capacitor would not be possible unless any of the methods discussed in Chapter 1 its applied. Although, this fact has been the aim of this dissertation, for this particular ac-dc LED driver it would not be tackled.

3.2 Dual inductor current-fed push-pull: working principle

The working principle that is going to be discussed throughout this section is based on operating both input inductors with currents equivalent to the current across the inductance in BCM (i.e., equivalent BCM), with the aim of powering LED loads in the range of hundreds of watts, increasing the scope of the topology to operate as an ac-dc converter. As has been explained, a PFC boost converter is able to perform as an LFR by operating in BCM [3.21], thus, the DICPP should be able to achieve the same performance, as it is a converter of the boost family. For that matter, the topology needs to be analyzed in terms of both switching and line frequency.

3.2.1 Static analysis

The operation of the DICPP ac-dc LED driver with both inductors working in equivalent BCM is summarized in Fig. 3.2 and Fig. 3.3. Fig. 3.2, shows the three different equivalent circuits that the DICPP ac-dc LED driver undergoes during a switching period, T_S, while Fig. 3.3 represents the most important waveforms to correctly understand its operation, both at line and switching period. It should be noted that the equivalent circuits depicted in Fig. 3.2 correspond with the waveforms and time intervals represented in Fig. 3.3 (b). In addition, the elements of the circuits that are not operating are shaded accordingly in each of the equivalent circuits. It should also be noted that the driving signals of the main switches (i.e., $v_{GS1}(t)$ and $v_{GS2}(t)$) are equivalent to the ones in the traditional CPP.

The first stage depicted in Fig. 3.2 (a) represents the equivalent circuit during the time intervals from t_0 to t_1 and from t_2 to t_3, when the two main switches (i.e., Q_1 and Q_2) are turned-on and the primary side of the transformer is short-circuited. During these time intervals, both inductors are being magnetized at $v_{in}(t)$ giving no power to the LED load, thus the LED load is being fed from the energy stored in the bulk capacitor, as shown in Fig. 3.3 (a).

The next time interval, from t_1 to t_2, see Fig. 3.2 (b), represents the operation when Q_1 is turned-on and Q_2 is turned-off. Therefore, L_{in1} keeps being magnetized at $v_{in}(t)$, but as Q_2 is turned-off the transformer is no longer short-circuited and power flows to the LED load, due to L_{in2} being demagnetized through the transformer by the reflected output voltage, D_6 and D_7, see Fig. 3.2 (b). Chronologically, the next stage would be the one from t_2 to t_3, however, this stage has already been discussed, as it is the one discussed first when the conduction of Q_1 and Q_2 overlaps, see Fig. 3.2 (a). Thus, the last stage to be considered in this analysis is the one from t_3 to t_4 shown in Fig. 3.2 (c). During this time interval, Q_1 is turned-off and Q_2 is turned-on, thereby magnetizing L_{in2} and demagnetizing L_{in1} by giving power to the LED load, again, through the transformer, D_5 and D_8, as shown in Fig. 3.3 (b). Therefore, this stage is the same as the one depicted in Fig. 3.2 (b), but with Q_1 and Q_2 swapping their roles.

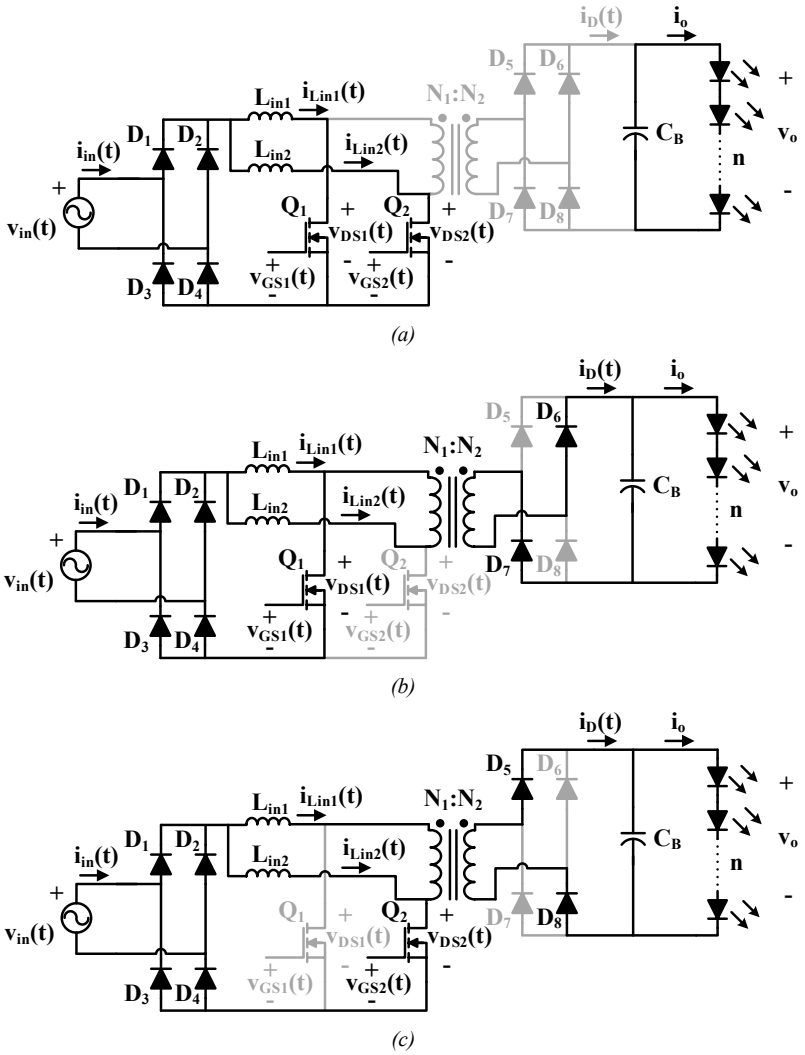
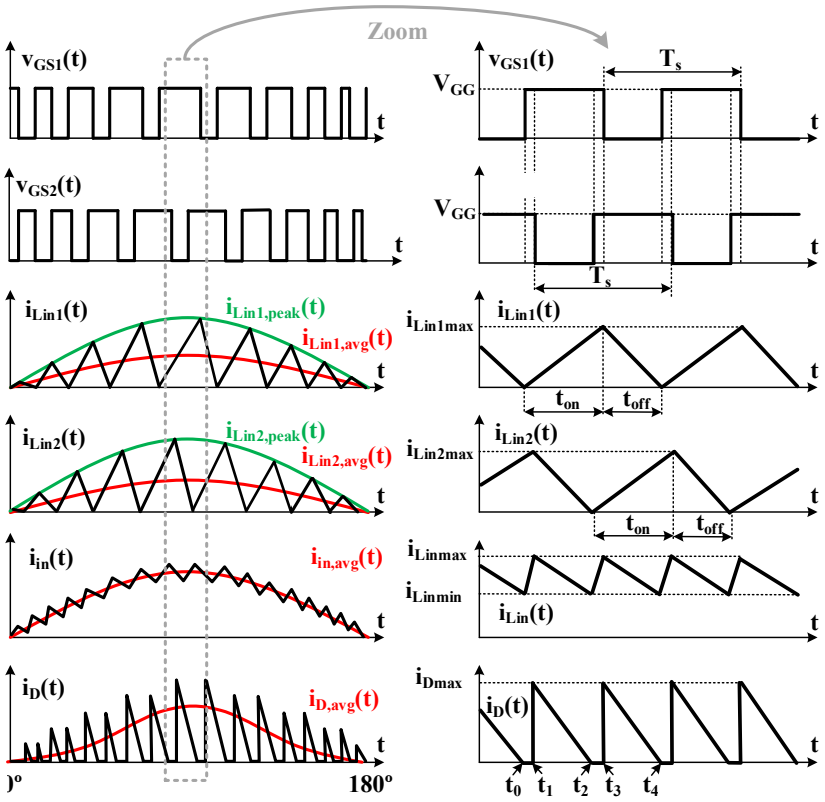


Fig. 3.2. Equivalent circuits of the DICPP for each time interval represented in Fig. 3.3 (b). (a) [t_0, t_1] and [t_2, t_3] time intervals: both Q_1 and Q_2 are turned-on. (b) [t_1, t_2] time interval: Q_1 is turned on and Q_2 is turned-off. (c) [t_2, t_3] time interval: Q_1 is turned-off and Q_2 is turned-on.

Fig. 3.3 (a) shows in red the input and output currents averaged at switching frequency during half line cycle, while Fig. 3.3 (b) shows a zoom of these waveforms to exemplify the switching operation of the DICPP ac-dc LED driver. In fact, in Fig. 3.3 (b), it can be seen at a glance that the time L_{in1} is being magnetized is exactly the same as the on-time of Q_1 and that for the magnetization of L_{in2} this time is coincidental with the on-time of Q_2. In addition, it should be noted that L_{in1} magnetizes regardless of the on-time of Q_2, being the same true for L_{in2} and Q_1. Therefore, the topology can be easily modelled as two independent boost converters interleaved with a 180º phase-shift at switching period introducing galvanic isolation. Please note, this last statement does not imply that the



(a) *(b)*

Fig. 3.3. Most representative waveforms of the DICPP LED driver at (a) Line period and (b) switching period.

DICPP ac-dc LED driver can work with one of its switches always turned-off, as both are necessary for its correct operation.

The interleaving between the two inductor currents translates in a reduction of the overall input current ripple of the DICPP ac-dc LED driver, improving the performance considering the EMI filter is not as penalized in size as in other single-phase single-stage ac-dc power converters operating in either DCM or BCM [3.22].

The control of the main switches (i.e., Q_1 and Q_2) requires either of the two to be turned-on, considering that dead times must be avoided since there is no path to correctly demagnetize L_{in1} or L_{in2}. Under this scenario, the voltages $v_{DS1}(t)$ and $v_{DS2}(t)$ will increase, potentially leading to the destruction of Q_1 or Q_2. Hence, the duty cycle, d(t), on each switch should always be higher than 50%. This is an intrinsic characteristic in current-fed converters, requiring a stage that overlaps both control signals, see Fig. 3.2 (a), in order to be able to swap between turning-on Q_1 and Q_2. As regards the aforementioned equivalent circuits, the converter relationship between output and input voltage in

equivalent BCM can be attained by studying the volt-second balance in either of the inductors. The converter gain can thus be defined by,

$$m(\omega t)=\frac{v_o}{v_{in}(\omega t)}=\frac{N_2}{N_1(1\text{-}d(\omega t))}\ , \tag{3.1}$$

where ω is angular frequency of the mains, v_o is the output voltage, $v_{in}(\omega t)$ is the input voltage, and N_2 and N_1 are the number of turns of the secondary and primary windings, respectively.

The independent magnetization of each inductor with their respective switch marks the operations of the DICPP ac-dc LED driver. Therefore, if L_{in1} and L_{in2} are considered of equal value (i.e., $L_{in1} = L_{in2} = L$), by studying the voltage balance on each inductor under equivalent BCM operation, the inductor peak currents (i.e., $i_{Lin1,peak}(t)$ and $i_{Lin2,peak}(t)$) can be defined as,

$$i_{L_{in1},peak}(t)=\frac{v_{gp}}{L}\sin(\omega t)t_{on}, \tag{3.2}$$

and,

$$i_{L_{in2},peak}(t)=\frac{v_{gp}}{L}\sin\left(\omega\left(t\text{-}\frac{T_s}{2}\right)\right)t_{on}, \tag{3.3}$$

where v_{gp} is the peak value of the input voltage and t_{on} is the on-time of each driving signal, which coincides with the magnetizing time of each inductor. Then, averaging (3.2) and (3.3) in a switching period, the average currents through the inductors, pulsating at line frequency can be expressed as,

$$i_{L_{in1},avg}(t)=\frac{v_{gp}}{2L}\sin(\omega t)t_{on}, \tag{3.4}$$

and,

$$i_{L_{in2},avg}(t)=\frac{v_{gp}}{2L}\sin\left(\omega\left(t\text{-}\frac{T_s}{2}\right)\right)t_{on}\,. \tag{3.5}$$

Therefore, the current through both branches will be sinusoidal following the input voltage; in this case, phase shifted 180º from the point of view of the switching period. Accordingly, the input current demanded by the DICPP ac-dc LED driver will be sinusoidal because of being the sum of two sinusoidal waveforms, given that the phase-shift that occurs between them can be considered negligible at line frequency, as shown in Fig. 3.3 (a). Consequently, the average input current at switching frequency can be expressed as,

$$i_{in,avg}(t)=i_{L_{in1,avg}}(t)+i_{L_{in2,avg}}(t)=$$
$$\frac{v_{gp}}{2L}t_{on}\sin(\omega t)+\frac{v_{gp}}{2L}t_{on}\sin\left(\omega\left(t\text{-}\frac{T_s}{2}\right)\right)\cong\frac{v_{gp}}{L}t_{on}\sin(\omega t). \tag{3.6}$$

It is a well-known fact, for a correct operation in BCM, that t_{on} needs to be kept constant at a certain value to guarantee that the converter will demand a certain amount of power, while only varying the off-time of the driving signal, t_{off}. The variation of t_{off} is required to achieve BCM operation as the demagnetizing time of each of the inductors will vary depending on the voltage at which they are being magnetized, taking into account that the magnetizing time is constant. Thus, the control is conventionally based on detecting the zero current value to determine the off-time, by means of a Zero Current Detection (ZCD) circuit (i.e., constant on-time and variable switching frequency).

Given that the average input current will be sinusoidal, as stated in (3.6), by multiplying it by $v_{in}(t)$, the instantaneous input power can thus be defined by,

$$p_{in}(t)= \frac{v_{gp}^2}{L} t_{on} \sin^2(\omega t). \tag{3.7}$$

Then, by averaging (3.7) at line frequency, the average input power processed by the DICPP ac-dc LED driver can be yielded,

$$p_{in}= \frac{v_{gp}^2}{2L} t_{on}. \tag{3.8}$$

Solving for ton in (3.8), gives,

$$t_{on}= \frac{2p_{in}L}{v_{gp}^2} \ , \tag{3.9}$$

which relates t_{on} with several well-known design parameters. From (3.9), it is possible to attain the LFR value of the DICPP ac-dc LED driver considering that,

$$R_{LFR}= \frac{p_{in}}{v_{gp}^2} \ , \tag{3.10}$$

thus,

$$R_{LFR}= \frac{L}{t_{on}} . \tag{3.11}$$

Equation (3.11) shows that with an adequate control method to ensure equivalent BCM operation on each inductor, the DICPP ac-dc LED driver is able to perform as a resistor from an input perspective. Therefore, the input current will follow the input voltage, which will result in achieving, as desired, almost unity PF.

The operation based on having a constant on-time and variable off-time, implies that the switching period will vary. It is in order, to study the switching frequency variation of the DICPP ac-dc LED driver. In that respect, the first step is applying voltage balance to either of the inductors, obtaining,

$$\frac{v_{gp}}{L} t_{on}= \frac{\frac{N_1}{N_2} v_o - v_{in}(t)}{L} t_{off}(t). \tag{3.12}$$

From (3.12), it is possible to solve $t_{off}(t)$ as,

$$t_{off}(t) = \frac{v_{gp}}{\frac{N_1}{N_2}v_o - v_{in}(t)} t_{on}. \tag{3.13}$$

Then, the variation of the switching period versus time can be obtained as,

$$T_s(t) = t_{on} + t_{off}(t) = \frac{\frac{N_1}{N_2}v_o}{\frac{N_1}{N_2}v_o - v_{gp}|\sin(\omega t)|} t_{on}, \tag{3.14}$$

Finally from (3.14) the switching frequency can be obtained as the inverse of the switching period, yielding,

$$f_s(t) = \frac{\frac{N_1}{N_2}v_o - v_{gp}|\sin(\omega t)|}{\frac{N_1}{N_2}v_o} \frac{1}{t_{on}} \quad . \tag{3.15}$$

The switching frequency values are of utter importance for the correct design (i.e., selection of main switches, magnetics and t_{on}). Particularly, the maximum and minimum frequency values, which considering the dependency of (3.15) with a sine wave, can be obtained for the maximum and minimum values of the sinusoidal as,

$$f_{s,min} = \frac{1}{t_{on}}, \tag{3.16}$$

and,

$$f_{s,max} = \left(1 - \frac{N_2}{N_1}\frac{v_{gp}}{v_o}\right)\frac{1}{t_{on}}. \tag{3.17}$$

3.2.2 Design criteria of the DICPP ac-dc LED driver

Focusing on the design of the DICPP ac-dc LED driver, some steps are required to be followed for a correct design, and are summarized below:

1. The transformer turns ratio (i.e., N_2/N_1) needs to be obtained from (2.1), considering v_{gp} as the maximum value that the input voltage can take (i.e., V_{gpmax}), v_o as the output voltage at the full dimming point, which is equal to nV_{γ_LED}, and d as the minimum duty cycle allowed, which should always be higher than 0.5, thus for safety reasons it is recommended to be selected at 0.55.
2. Having obtained the transformer turns ratio, it is required to calculate d under nominal conditions. The duty cycle and the desired switching frequency can then be used to obtain the required inductance from (3.8), considering that $t_{on} = dT_s$. If the calculated inductance has an acceptable value, (3.16) and (3.17) are to be used in order to check whether the frequency range is acceptable as well. If not, the inductance value needs to be adjusted to meet the design requirements. Please note that a frequency higher than 20 kHz for $f_{s,min}$ constitutes a good practice to avoid any audible noise on the converter.

3. The next step is the selection of the main switches (i.e., Q_1 and Q_2). In that respect, the current and voltage values that they will have to withstand need to be calculated. Considering that the voltage withstood is equal to the voltage withstood by the primary side of the transformer then from (2.1) the maximum voltage can be defined as,

$$V_{Qmax}= \frac{V_{gpmax}}{1-d_{min}}. \tag{3.18}$$

As regards the current it is equal to the maximum current through either of the inductors because of it reaches the maximum value when the switch referenced to that inductor reaches the end of the on-time. Then it can be obtained from (3.2) at the peak value of the sinusoid for the minimum voltage peak value of the power grid (i.e, V_{gpmin}),

$$I_{Qmax}= \frac{p_{in}}{V_{gpmin}}. \tag{3.19}$$

As can be seen in (3.18), the maximum voltage withstood by the Q_1 and Q_2 entirely relies on the maximum input voltage and the minimum duty cycle allowed. Considering that the minimum duty cycle is set as a constant at 0.55, the maximum voltage withstood by the switches will increase linearly with the input voltage. Therefore, for operation in the European power grid, the switches will require high breakdown voltages (i.e., 900/1200 V), which would mean the use of Silicon Carbide (SiC). In addition, the main switches need a demagnetization circuit and a clamping snubber for overvoltage protection. The demagnetization circuit is required during an unexpected shut down of the ac-dc LED driver, requiring an extra winding as any other current-fed topology.

4. The last step is the selection of the high frequency rectifier (i.e., D_5-D_8). Similarly the maximum withstood values are to be calculated. The maximum voltage depends on the maximum output voltage and the voltage withstood on the secondary side of the transformer. Hence,

$$V_{Dmax}= V_o- \frac{N_2}{N_1} V_{gpmin}, \tag{3.20}$$

In that sense, the maximum current is the maximum current through the secondary side of the transformer, which is the same as the one withstood by Q_1 and Q_2 taking into account the turn ratio of the transformer. Hence,

$$I_{Dmax}= \frac{N_1}{N_2} \frac{p_{in}}{V_{gpmin}}, \tag{3.21}$$

The selection of the high frequency diode bridge ends the design of DICPP ac-dc LED driver as the selection of the low frequency diode bridge can be performed similarly to any other single-phase single-stage ac-dc power converter. In fact, this low frequency diode bridge can be removed turning the DICPP LED driver into a bridgeless topology with the right technology for Q_1 and Q_2. This statements means using true bidirectional switches that are able to block current in both directions, unlike MOSFETs. And even if

it is doable by means of MOSFETs it complicates the driving stage, requiring the duplication of Q_1 and Q_2.

3.2.3 Transformer design

Briefly along the introduction, the importance of the transformer design for current-fed topologies was mentioned. In fact, it is of such importance that it requires its own section.

In current-fed converters, where the current through the primary transformer winding is abruptly changed whenever a transistor switches, the leakage inductance needs to be minimized. Otherwise, each switching instant will produce a significant voltage spike, making the use of higher voltage rated transistor or protective clamps necessary, hindering in the process the efficiency of the solution, particularly, if they are resistive based.

Consequently, the minimization of the leakage inductance is an objective which can be performed by the well-known procedure of winding interleaving between primary and secondary windings. However, as a side effect of adding a high number thinner sub-windings, a low leakage inductance can be obtained at the cost of higher parasitic capacitances. This has proved to be troublesome when voltage spikes are negligible with a good leakage inductance design, but the transformer resonates due to its lumped capacitance. These recirculating currents not only hinder the efficiency of the converter, but they also make it more difficult to detect events to properly operate each inductor in equivalent BCM, requiring complex filters.

The transformer resonance in a CPP has been analyzed in [3.20], where it is studied the impact of both leakage inductances and lumped capacitance in improving the efficiency of the converter. In fact, for a DICPP the analysis is comparable taking into account the similarity of the equivalent circuits. That being said, an empiric rule has been developed for a well-designed transformer: the leakage needs to be at least a thousand times lower than the transformer magnetizing inductance. The latter needs to be at least five times higher than the inductances value for it not to impact on their magnetization. Then, truthfully the relationship occurs between the input inductances and the leakage inductance of the transformer. In addition the lumped capacitance of the primary side needs to be limited in the design, however, this parameter is not as critical as ensuring a low leakage inductance. The reason being that even if it can be considered negligible, the impact of the C_{OSS} of Q_1 and Q_2 will need to be taken into account when analyzing the resonance and recirculating currents.

In order to solve the aforementioned issues, the use of planar magnetic technologies could be a feasible option, taking into account their implementation ease of interleaved windings and their process predictability and repeatability [3.23], [3.24]. However, attaining a low leakage inductance with this technologies requires a heavy amount of PCB layers, which rapidly increase the cost, complexity and the lumped capacitance of the transformer. The latter is of utter importance, and even though some techniques have been implemented in planar transformers to reduce their parasitic capacitance, some traditional transformer options will be studied to simplify the design of both the transformer and the PCB in this dissertation.

The design of the transformer is based on the previous design equations attaining an 11:1 turn ratio, for the US input voltage in a single-phase ac power grid, and aiming for low losses in a relatively wide frequency range around 150 kHz. As has been previously stated its magnetizing inductance is not critical as long as it is much higher than L_{in1} and L_{in2}. After studying the size and losses of several cores and magnetic components from different manufacturers with ANSYS® PExprt, the EPCOS RM12 was selected for optimization with N49 as its magnetic material [3.25]. Several designs were simulated using ANSYS® Maxwell, PExprt and PEmag to accurately and rapidly test the feasibility of the design, whose maximum allowed parameters are stated in Table 1.1. In this table, there are also shown the most noteworthy results of the simulations obtained for three different implementation: no interleaving between primary and secondary with twisted wire, interleaving between primary and secondary with twisted wire and interleaving with a foil-based wire.

The simplest design which is the non-interleaved one, is not feasible due to its large leakage inductance surpassing the maximum allowed values, see Table 1.1, whereas the foil-based one achieves an extremely low leakage at the cost of a higher lumped capacitance. Thus, the most promising solution is the interleaved one, which can be easily manufactured in comparison to the foil-based and meets the desired specifications.

As can be seen in Fig. 3.4, the winding arrangement is kept rather simple in order to be able to easily assemble and replicate the transformer with regular manufacturing techniques and machinery. The primary windings consists of 8 different sub-windings, each of 66 turns of AWG 35 copper wire, all of them connected in parallel and arranged as shown in yellow in Fig. 3.4 (a).

The secondary winding, depicted in Fig. 3.4 (a) in red consists of 6 different sub-windings each of 6 turns arranged in two layers, interleaved with the primary. In fact, each layer contains three sub-windings distributed in accordance to Fig. 3.4 (b). Note that unlike the primary, the current is significantly high, thus, the wire used is comprised of 10 AWG 35 wires combined into a twisted wire. Therefore, the total thickness is small enough to distribute the sub-windings evenly along the window height, reducing the leakage inductance even further.

Table 3.1. Transformer parasitic components for different implementations.

	Lumped capacitance	Leakage inductance
Maximum	100 pF	21 µH
No interleaving	10.99 pF	47.589 µH
Interleaving	20.73 pF	5.498 µH
Foil-based	58.36 pF	0.606 µH
Interleaved prototype	45.80 pF	3.020 µH

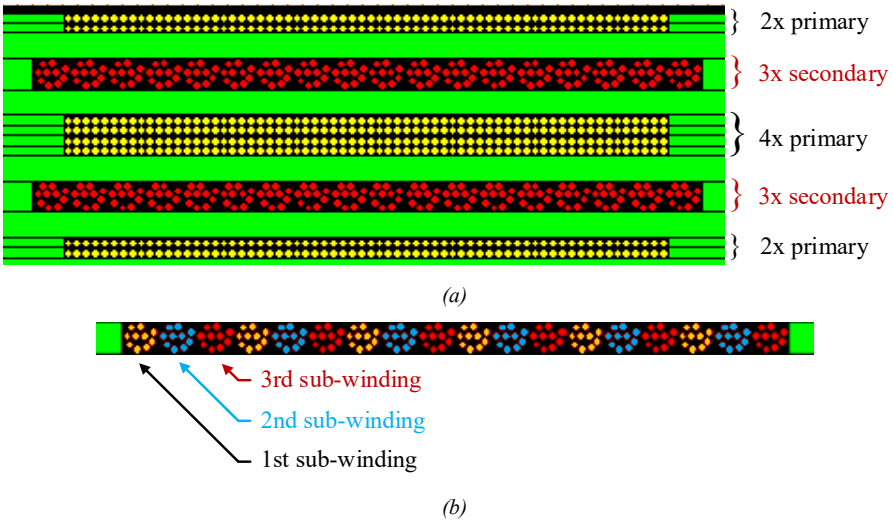


Fig. 3.4. Design of the implemented magnetic. (a) Transformer cross section. (b) Detail of the transformer secondary sub-windings, where each color represents a different sub-winding in the same layer.

As can be seen in Table 1.1 different implementations, regarding the wire, were considered for the secondary winding. The use of copper foil is an interesting alternative, but its benefit does not justify the increase in manufacturing difficulty, requiring custom foil thickness, or even laser cutting machinery for fitting the required turns in just one layer.

Please note, the copper windings do not fill the winding area completely and polyester film insulating tape layers are added between them [3.26]. These layers are depicted in green in Fig. 3.4 (a) leaving the black parts of the figure as air. This serves a dual purpose: fixing and insulating the primary and secondary layers, and creating wider spaces between them, thus lowering the inter-winding capacitance.

3.3 Dual inductor current-fed push-pull ac-dc LED driver: small-signal analysis and control strategies

As any of the ac-dc LED drivers discussed throughout this dissertation the DICPP ac-dc LED driver needs to control the current through the LEDs to ensure an adequate control of the light. In that respect, Fig. 3.5 shows a diagram of the proposed control with its control feedback loop for the DICPP ac-dc LED driver in red, including in blue the required circuitry for the demagnetization path. The proposed control is based on sensing the current at the output of the high frequency diode bridge, $i_D(t)$, with the aid of a simple current transformer. The reason for sensing only $i_D(t)$ is due to it containing all the required information for the control, as it includes the information on when either of the inductors reaches the zero current value, and the information on the current supplied to the LED load, see Fig. 3.3 (b). Nonetheless, a low-pass filter is required to actually obtain the current through the LED load, which is the average of $i_D(t)$. This sensing method obtains all the required information from the same isolated measurement that can be referred to the primary to further simplify the control of the ac-dc LED driver.

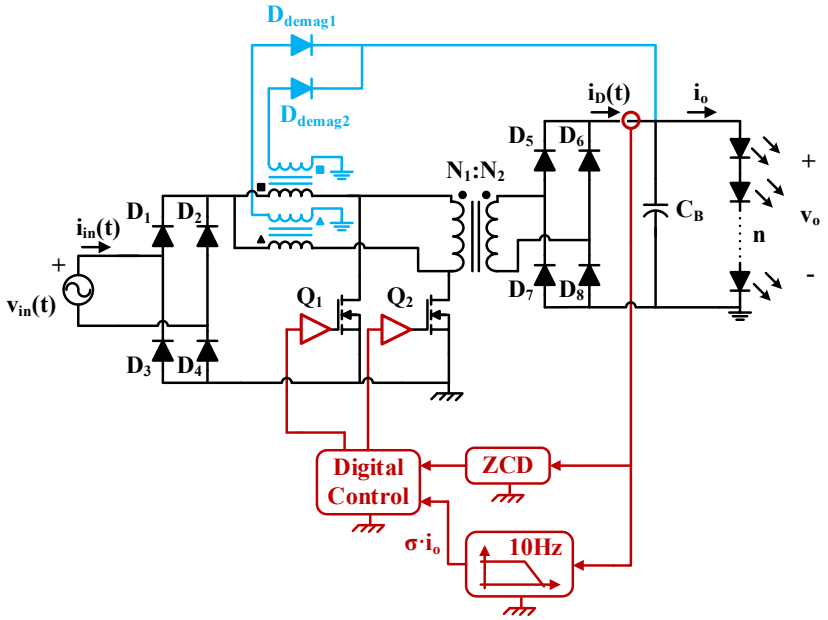
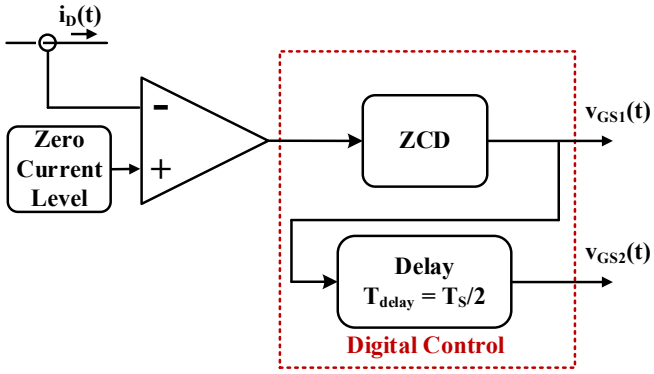


Fig. 3.5. Diagram of the output current feedback loop for the DICPP ac-dc LED driver including the demagnetization circuitry.

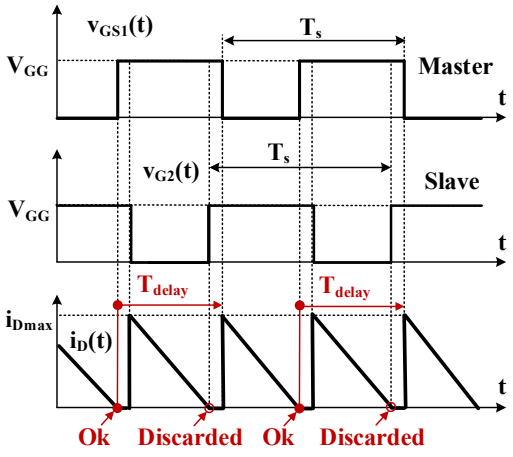
However, by measuring $i_D(t)$ instead of the current through each inductors, as many interleaved PFC boost converters do, the control needs to be able to discern which switch to trigger. For that matter, Fig. 3.6 summarizes the proposed methodology used to achieve variable switching frequency control in open loop on the DICPP ac-dc LED driver. Please note that the t_{on} variation that would occur due to the output current feedback loop used to control i_o is not taken into account in this figure.

The proposed control is based on detecting the moment $i_D(t)$ reaches zero (i.e., Zero Current Level, ZCL), by means of an analog comparator and sending the signal to the central control unit, see Fig. 3.6 (a), which will be responsible for discerning which switch to turn-on. The discerning of the zeroes is performed taking into account that the inductors reach the zero value sequentially, which means that after $i_{Lin1}(t)$ reaches zero it should be $i_{Lin2}(t)$ the one reaching the zero value. Hence, the control considers one zero and discards the next one. That is, it generates the driving signal for Q_1 from the ZCD circuit, and the driving signal of Q_2 by phase shifting 180º the driving signal of Q_1. However, this is not trivial as the switching period is constantly changing, thus a Phased Lock Loop (PLL) needs to be used to adequately phase-shift the signal generated for Q_1 to drive Q_2, taking into account the previous switching period (i.e., the calculation of T_{delay}). It should be noted that it is not a problem to consider the previous switching period taking into account that the changes on the switching period happen slowly, as they change along an LF input voltage waveform.

This methodology is regarded in literature as open-loop interleaving and is based on setting one of the PFC boost converters as the master and the rest as slaves with their adequate phase-shift [3.27], [3.28]. Particularly for the DICPP ac-dc LED driver it is a



(a)



(b)

Fig. 3.6. Zero current detection methodology. (a) Basic control diagram. (b) Characteristic waveforms used in zero current detection.

matter of setting one of the switches as the master and the other as the slave. The master will be selected at the start-up of the DICPP ac-dc LED driver being either Q_1 or Q_2, and it will not abandon its master status during the entire operation of the ac-dc LED driver. It is important to note that once a master is selected, the next zero detection will be discarded, in accordance to Fig. 3.6 (b), as it will be related to the slave.

The correct detection of the zeroes ensures an adequate operation of each inductor under equivalent BCM, guaranteeing in the process an LFR performance of the DICPP ac-dc LED driver. Nonetheless, as any LFR it needs to control how much power is fed to the LED load. For that matter a low pass filter with a 10 Hz bandwidth is used to filter $i_D(t)$ thus obtaining i_o scaled by a constant, σ, which will, then, be compared to a reference within the digital control in order to regulate the output of the ac-dc LED driver. This implies there needs to be a variable to regulate.

As a reminder and similarly to the analysis carried out in Chapter 2, the selected notation for the forthcoming mathematical analysis will represent constants and variables particularized at a certain operating point in capital letters. In addition, variables describing small ac variations in lowercase with a circumflex accent, taking into account that lowercase variables without the circumflex accent have been used for the static analysis.

Equation (3.8), shows the dependency of p_{in} on several parameters, being t_{on} the only controllable one as the rest are based on design conditions. Then, it is possible to apply a small-signal analysis to the DICPP ac-dc LED driver to model its transfer function, which can be carried out similarly to any interleaved PFC boost converter [3.29], considering the equivalent circuit of the LED load. Then, relating (3.8) in terms of i_o, gives,

$$i_o = \frac{v_{gp}^2}{2Lv_o} t_{on} \,. \tag{3.22}$$

At this point, in accordance to [3.30] and considering (3.22) is already averaged, it is required to linearize and particularize at a certain operating point in order to obtain the small-signal model. Thus, obtaining:

$$\left.\frac{\partial i_o}{\partial t_{on}}\right|_P = \frac{V_{gp}^2}{2LV_o} = g_{ioon}, \tag{3.23}$$

$$\left.\frac{\partial i_o}{\partial v_{gp}}\right|_P = \frac{V_{gp}}{2LV_o} T_{on} = g_{iogp}, \tag{3.24}$$

and,

$$\left.\frac{\partial i_o}{\partial v_o}\right|_P = -\frac{V_{gp}^2}{2LV_o^2} T_{on} = -\frac{I_o}{V_o} = \frac{1}{r_o}, \tag{3.25}$$

where g_{ioon}, g_{iogp} and r_o represent the values depicted in Fig. 3.7.

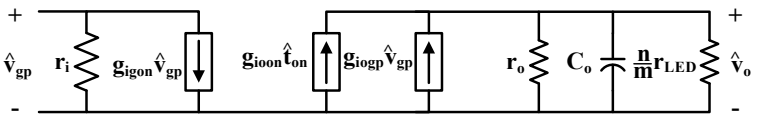


Fig. 3.7. Equivalent small-signal circuit model of the DICPP ac-dc LED driver.

This, completes the analysis from the point of view of the output current. In order to complete the small-signal analysis it is necessary to obtain the averaged input current input current. Thus, from (3.6) and averaging at line frequency a rectified sinusoid,

$$i_{in} = \frac{2v_{gp}}{\pi L} t_{on}. \tag{3.26}$$

As it was previously done for the input current, the next step is linearizing and particularizing at a certain operating point, obtaining,

$$\left.\frac{\partial i_{in}}{\partial v_{gp}}\right|_{P}=\frac{2T_{on}}{\pi L}=\frac{1}{r_i}, \tag{3.27}$$

and,

$$\left.\frac{\partial i_{in}}{\partial t_{on}}\right|_{P}=\frac{2V_{gp}}{\pi L}=g_{igon}. \tag{3.28}$$

After obtaining (3.28) the circuit shown in Fig. 3.7 is complete, thus being able to attain the required transfer function. For that matter, i_o and t_{on} can be related as,

$$G_{i_o t_{on}}(s)=\left.\frac{\hat{i}_o}{\hat{t}_{on}}\right|_{\hat{v}_{gp}=0}=\frac{\dfrac{g_{ioon}r_o}{\dfrac{n}{m}r_{LED}+r_o}}{1+\dfrac{sC_o\dfrac{n}{m}r_{LED}r_o}{\dfrac{n}{m}r_{LED}+r_o}}. \tag{3.29}$$

From (3.29) it is now possible to obtain a compensator that satisfies the design of the DICPP ac-dc LED driver. Particularly, taking into account the line frequency component on the output, the bandwidth of the compensator needs to be sufficiently low to filter this component that appears due to the pulsating input power. The expression that relates variations on the input voltage to the output current can also be attain from Fig. 3.7 as,

$$G_{i_o v_{gp}}(s)=\left.\frac{\hat{i}_o}{\hat{v}_{gp}}\right|_{\hat{i}_o=0}=\frac{\dfrac{g_{iogp}r_o}{\dfrac{n}{m}r_{LED}+r_o}}{1+\dfrac{sC_o\dfrac{n}{m}r_{LED}r_o}{\dfrac{n}{m}r_{LED}+r_o}}. \tag{3.30}$$

3.4 Dual inductor current-fed push-pull: experimental results

The DICPP ac-dc LED driver has been theoretically analyzed throughout the previous sections of this chapter. It is in order to validate its performance by means of an experimental prototype. Therefore, a prototype has been designed following the design criteria introduced in Subsection 3.2.2 for a maximum output power of 100 W, in the full range of the US single-phase ac power grid line voltage (i.e., from 80 Vrms to 140 Vrms), feeding an LED load comprised of five strings of 12 LEDs each (i.e., n = 12 and m = 5 of W42180T2-SW) with their respective equalizing resistors, which are equivalent to 48 V and 1.8 A at full load. Accordingly, the switching frequency has been selected to vary from 55 kHz at the lowest line voltage peak to 225 kHz at the zeroes of the maximum line voltage, considering that the lowest frequency should be out of the human audible band and that the highest frequency does not impact the efficiency, negatively, due to switching losses on the main switches.

That being said, all the selected components used in the prototype of the DICPP ac-dc LED driver have been summarized in Table 3.2. Note that the selected MOSFETs to test the prototype are 600 V superjunction MOSFET, as it needs to withstand around 450 V considering the input voltage values. As regards the high frequency diode bridge, it is comprised of 60 V/10 A fast-recovery Schottky silicon diodes with ultra-low forward voltage, which is enough considering that the HF diode bridge withstand the same voltage

as the LED load. In addition, the digital control of the entire DICPP ac-dc LED driver has been implemented in an FPGA due to the simplicity and versatility that this platform offers, which is particularly important for the proposed master-slave technique. Fig. 3.8 shows a picture of the prototype that has been built to validate the analysis carried out along the previous section. Please note that this prototype has the purpose of validating the idea and even though the selection of components has been done carefully to obtain the best possible performance, this prototype is not optimized in terms of size to be able to perform changes as they were required.

Table 3.2. Components use in the DICPP LED driver.

Fig. 3.1 reference	Value
D_1-D_4	1N4007
D_5-D_8	FSV1060V
L_{in1} and L_{in2}	760 µH – RM8 – EPCOS N49
S_1-S_2	IPP65R225C7
FPGA	XC7A100T-1CSG324C
C_o	60V, 2.2mF Electrolytic Capacitor

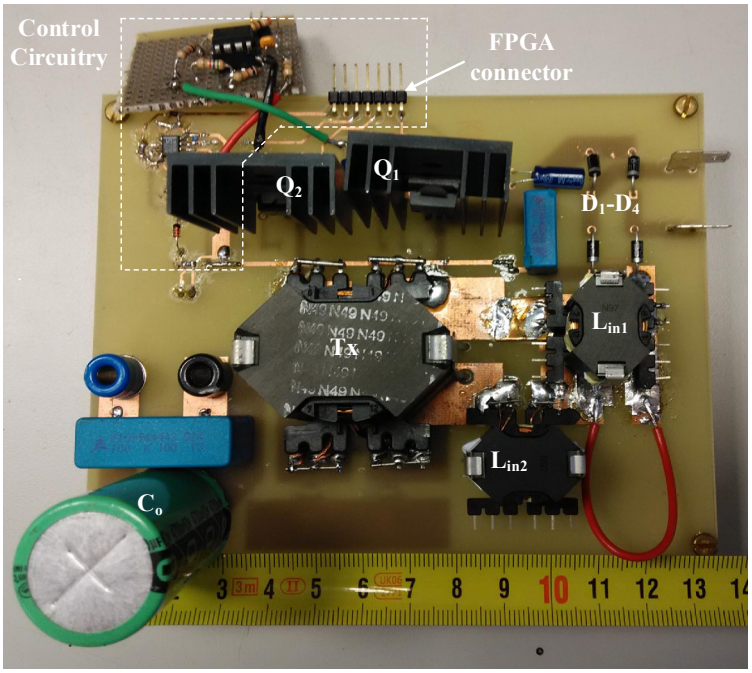


Fig. 3.8. Experimental prototype of the DICPP ac-dc LED driver.

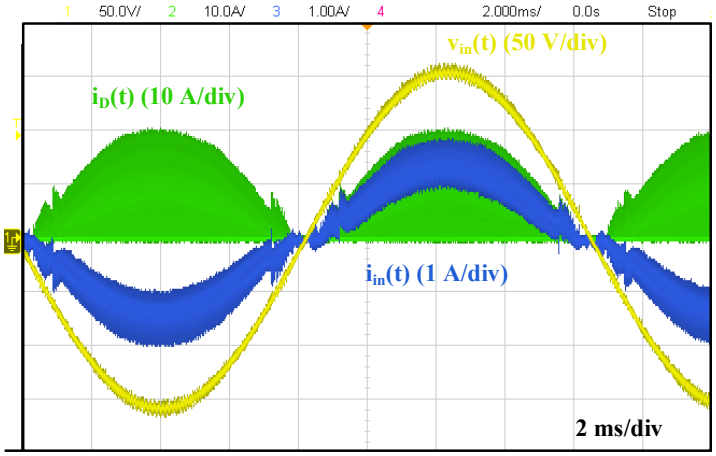
3.4.1 Basic operation

The first step to validate the theoretical analysis and thus the experimental prototype of the DICPP ac-dc LED driver is checking if it can achieve an LFR performance. As regards that, Fig. 3.9 (a) shows a snapshot of the oscilloscope for an input voltage of 110 Vrms at 60 Hz, measured before the EMI filter to exemplify the low high frequency ripple of the input current. As can be seen, the current follows, adequately, the input voltage, demonstrating the LFR performance, and validating the theoretical analysis by achieving almost unity PF. Furthermore, the input current presents a low switching frequency ripple in spite of having its two inductors operating in equivalent BCM, exemplifying the interleaving that the DICPP ac-dc LED driver achieves intrinsically. It should be noted that all the signals depicted along this section, correspond to the references introduced in Fig. 3.2.

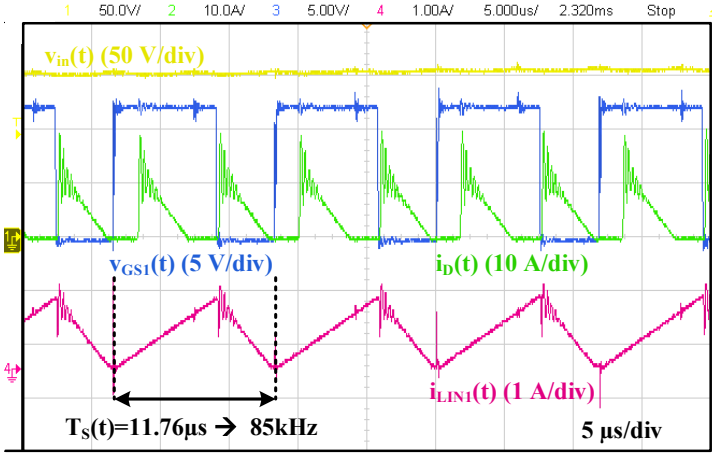
In order to show the operation of the prototype at switching frequency in detail, Fig. 3.9 (b), depicts a zoom of Fig. 3.9 (a) at the peak of the sine wave of the input voltage. As can be seen, $v_{GS1}(t)$ triggers every two zero current values of $i_D(t)$, which are at the same time coincidental with the zeroes of $i_{Lin1}(t)$. Therefore, validating the analog circuitry to detect the zero value of the current and the driving of the master MOSFET (i.e., Q_1 in this scenario). In fact, considering the waveform of $i_D(t)$ it can be supposed that the central control is generating adequately the signal to drive Q_2 from the master signal. The high frequency ripple that appears on $i_D(t)$ happens due to the transformer resonances, which is required to be of a high frequency in order for the filter not to affect the ZCD negatively in terms of delays.

In addition, the ac-dc DICPP LED driver needs to be able to vary its frequency. In order to exemplify this operation, Fig. 3.9 (c) shows a lower input voltage operating point at which the switching frequency of $v_{GS1}(t)$ increases, being the same true for $v_{GS2}(t)$, validating in the process the correct operation of the proposed control. It should be noted that $i_{Lin1}(t)$ is shown to exemplify the achievement of equivalent BCM on this inductor under both scenarios (i.e., Fig. 3.9 (b) and Fig. 3.9 (c)). The operation on equivalent BCM of the other inductor can be deduced, again, by taking a look at the shape of the output current. In fact, it is thanks to this output current with a frequency at twice the switching frequency, that the capacitance can be lowered in comparison to the CPP, however, this fact is irrelevant for an ac-dc power converter as the pulsating power at line frequency needs to be filtered. In order to filter that low frequency component an electrolytic capacitor of 2.2 mF is used to obtain the waveforms depicted in Fig. 3.10. The capacitor selection is done in order to achieve a current whose ripple is low enough to guarantee a flicker free operation. The removal of the electrolytic capacitor in the DICPP ac-dc LED driver cannot be easily accomplished and one of the methods discussed in Chapter 1 should be applied for that matter, achieving a quasi-single-stage topology (i.e., using a bidirectional dc-dc converter, a multi-output ripple cancellation or the integration of a post-regulator into the single stage, sharing its active components).

This analysis concludes the validation of the operation of the DICPP ac-dc LED driver. However, there are still several parameters that need to be studied with further detail. In that respect, several waveforms have been extracted from the oscilloscope as data and processed with MATLAB® to properly analyze them. Again the parameters that need to be studied are efficiency, THD, PF, and compliance with Class C IEC 61000-3-2 [3.2].



(a)



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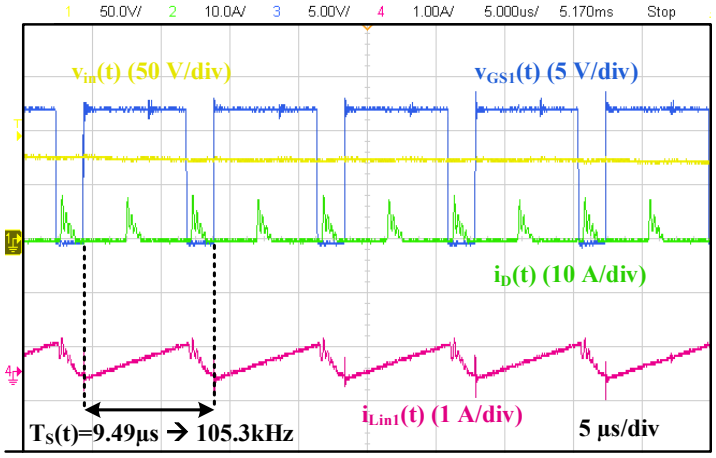

(c)

Fig. 3.9. Input waveforms of the DICPP ac-dc LED driver. (a) Input current and voltage, and i_D(t) at 110 Vrms. (b) Zoom at the peak of v_{in}(t). (c) Zoom at a lower input voltage of v_{in}(t).

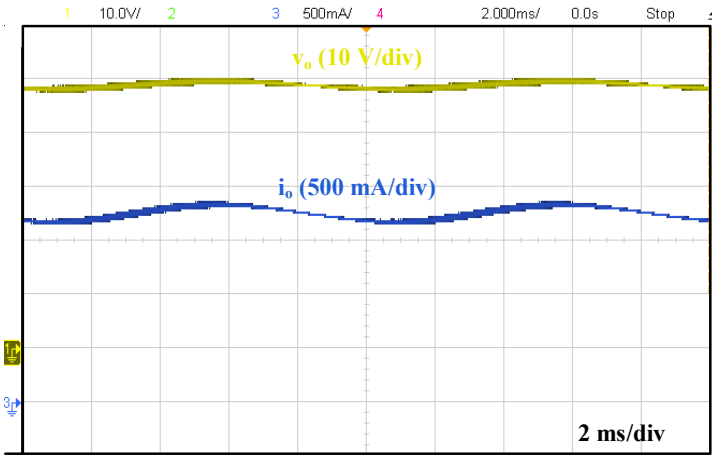

Fig. 3.10. Output voltage and current at full load in the DICPP ac-dc LED driver.

3.4.2 Electrical characteristics and compliance with the regulation

The efficiency, THD and PF of the DICPP ac-dc LED driver are summarized in Table 3.3 as a variation of the line voltage. For the nominal conditions presented in Fig. 3.9 (a), the efficiency almost reaches 92% with a THD about 8% and a 0.99 PF, all of which comply with the ENERGY STAR® regulation [3.1], of course in spite of removing the electrolytic capacitor. Note that the efficiency at full load does not fall below the 90% even for the worst case scenario.

The THD shown in Table 3.3 has been improved by three points by means of a practical implementation. Considering that toward the zero crossing value of the input voltage sinusoid the analog ZCD circuit tends to fail on the detection of the zeroes, then, the proposal is setting the operation at a fixed frequency forcing each inductor to operate with a current equivalent to DCM for a certain voltage range. This implementation stops the current from having a reduced conduction angle, thus improving power transfer and THD.

The efficiency of the DICPP ac-dc LED driver is summarized under nominal conditions (i.e., 110 Vrms) in Fig. 3.11, taking into account all the power losses including control and driving. As can be seen, the efficiency stays above 90% from full load to half load. At lower loads, however, the DICPP ac-dc LED driver suffers a drop on its

Table 3.3. THD, PF and efficiency varying the input peak voltage for the DICPP ac-dc LED driver.

V_{IN} [V_{RMS}]	THD [%]	PF	Efficiency [%]
80	8.5	0.99	90.6
110	8	0.99	91.9
140	7.5	0.99	93.4

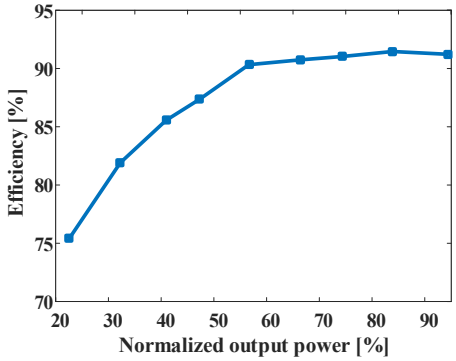

Fig. 3.11. Efficiency of the DICPP LED driver at 110 Vrms versus the output power consumption.

efficiency due to the lower currents circulating on the primary side, causing the detection on the secondary side to fail more often. The latter greatly affects the performance of the DICPP ac-dc LED driver, as seen on the efficiency graph.

In order to understand the most limiting elements on the DICPP ac-dc LED driver the power losses have been carefully studied. In fact, the magnetic components present more than 50% of the total losses of the converter, as shown in Fig. 3.12. Their losses have been estimated using Finite Element Analysis (FEA) via ANSYS® Electromagnetics Suite. As regards the input rectifier only the conduction losses are considered, whereas for the output rectifier both conduction and switching losses are taken into account due to the high frequency switching of this components.

Focusing on the most difficult elements to predict the losses, the control has been measured on the experimental prototype to correctly estimate its consumption, otherwise it becomes a matter of defining and estimating the losses for the elements, which is not only inaccurate but extremely tedious. The other element that shows a certain degree of difficulty and for which several technical papers have been dedicated in literature are the main switches. For that matter, and considering that they are superjunction MOSFETs an analytical model particularized for this technology has been used [3.31]. This model is

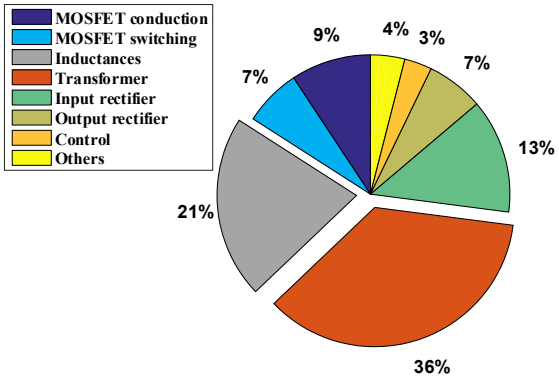

Fig. 3.12. Distribution of losses in the experimental prototype of the DICPP LED driver under nominal conditions.

specified for dc-dc power converter, then, some adjustments had to be made to estimate accurately estimate the losses. The losses have been estimated in nominal conditions at the peak of the sinusoid and then they have been averaged over a line period.

From the distribution of losses depicted in Fig. 3.12 can be seen that by removing the input rectifier, with the use of a bidirectional switch as has been previously explained, it is possible to improve the efficiency of the DICPP ac-dc LED driver in more than 1% efficiency.

At this point, the validation of the driver requires compliance with Class C IEC 61000-3-2 harmonic limits. Thus, the harmonic content of the input current has been extracted and compared to the one set by the regulation, as shown in Fig. 3.13. As has been expected, the DICPP ac-dc LED driver complies with the aforementioned regulation.

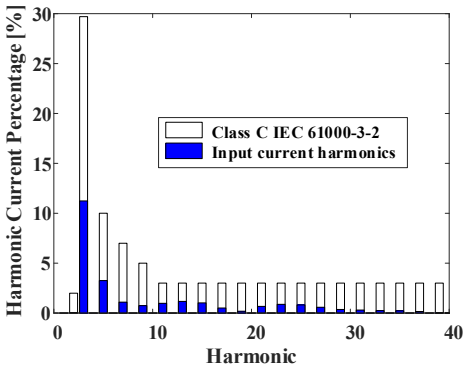

Fig. 3.13. Harmonic content of the input current of the DICPP ac-dc LED driver compared with the harmonic limits set by Class C from the IEC-61000-3-2 [3.2].

After having complied with IEC 61000-3-2, only the flicker regulation is left to test its compliance. Similarly, to the input current, the harmonic content of the instantaneous output luminance has been obtained, from which, each Mod. (%) has been calculated, in accordance to the method introduced in Chapter 1. The Mod. (%) for each of the harmonics has then been compared to the limits set by Practice 1 from the IEEE Std. 1789-2015, as shown in Fig. 3.14. As can be seen, compliance is ensured, being, as expected, the most limiting harmonic the one at twice the line frequency. This implies that for a flicker-free operation a correct selection of the output capacitance needs to be made. For this particular LED driver it is a matter of using an electrolytic capacitor.

3.4.3 Comparison with state-of-the-art solutions

The previous subsections have validated the operation and compliance with the required regulations, however, and taking into account the study carried out throughout Chapter 1, it is a good practice to compare the DICPP ac-dc LED driver with the most promising single-phase single-stage ac-dc LED drivers that can be found in literature within a certain power range. In that respect, Table 3.4 shows a brief comparison of the DICPP LED driver with state-of-the-art single-phase single-stage ac-dc LED drivers, in which several important parameters are compared, such as, output power, efficiency,

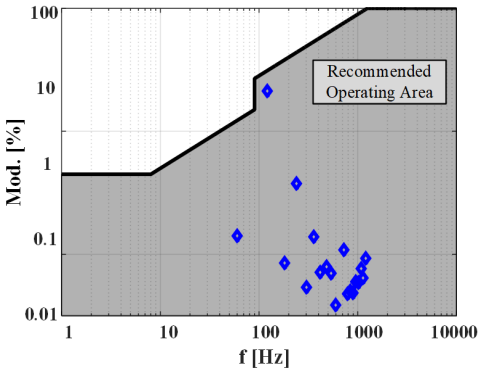

Fig. 3.14. Harmonic content of the instantaneous output luminance of the DICPP ac-dc LED driver, compared with the harmonic limits set by Practice 1 from the IEEE Std. 1789-2015 [3.32].

Table 3.4. Comparison of the state-of-the-art single-stage ac-dc LED drivers with the DICPP ac-dc LED driver.

		References				
	DICPP	[3.7]	[3.10]	[3.33]	[3.34]	[3.35]
Output Power [W]	100	35	35	81	100	12
Quasi-single-stage	No	Yes	Yes	Yes	Yes	Yes
Efficiency [%]	91.5	87	90.5	90.69	91.7	86.1
THD [%]	8	-	-	3.32	5.7	-
Class C IEC 61000-3-2 compliance	Yes	Yes	Yes	Yes	Yes	No
Switching frequency [kHz]	55-225	-	140	67	90	100
Output capacitor [μF]	2200	470	4.7	-	220	2
Output current ripple [%]	10	10	20	20	10	17.85
Output capacitor reduction	No	Yes	Yes	No	Yes	Yes
Reduced input cur. ripple	Yes	No	No	Yes	No	No
Number of MOSFETs	2	3	3	2	2	1
Number of HF diodes	4	2	2	2	6	3
Number of transformers	1	1	1	2	1	1
Number of inductances	2	1	2	0	3	1

THD, size of the output capacitance, etc. As can be seen, the DICPP LED driver shows an outstanding performance with its biggest disadvantages being its variable frequency operation and the need of an electrolytic capacitor. However, the other presented ac-dc LED driver, remove the electrolytic capacitor at the cost of adding more components and increasing the complexity of the solution by turning from a single-stage ac-dc LED driver into a quasi-single-stage, performance that it is also possible for the DICPP ac-dc LED driver by applying any of the methodologies discussed in Chapter 1 for this matter. It should also be noted, that unlike some of the solutions the proposed in Table 3.4, the DICPP ac-dc LED driver is able to drive high power luminaires, complying with Class C IEC 61000-3-2 and achieving a high efficiency. This benefits are possible with an increased amount of elements in comparison to a traditional flyback ac-dc LED driver, however, this topology would not be able to achieve such performance at the power levels aimed for the proposed DICPP ac-dc LED driver.

3.4.4 Dynamic validation

Please note that all the measurements shown in this section have been measured in closed loop by controlling the output current of the DICPP ac-dc LED driver, thus allowing t_{on} to vary. In order to design the regulator, the open loop response of the DICPP ac-dc LED driver relating t_{on} to i_o has been measured by means of a Venable® 6320 frequency response analyzer [3.36]. In that respect, the measuring setup, depicted in Fig. 3.15, disconnects the output current feedback loop and uses the signal generator of the Venable to generate an external value for t_{on} that is then transmitted to the digital control after going through an Analog-Digital Converter (ADC), thus it needs to be scaled accordingly (κ). This external value has a dc component that sets the operating point of the DICPP ac-dc LED driver which also varies accordingly with several tones to

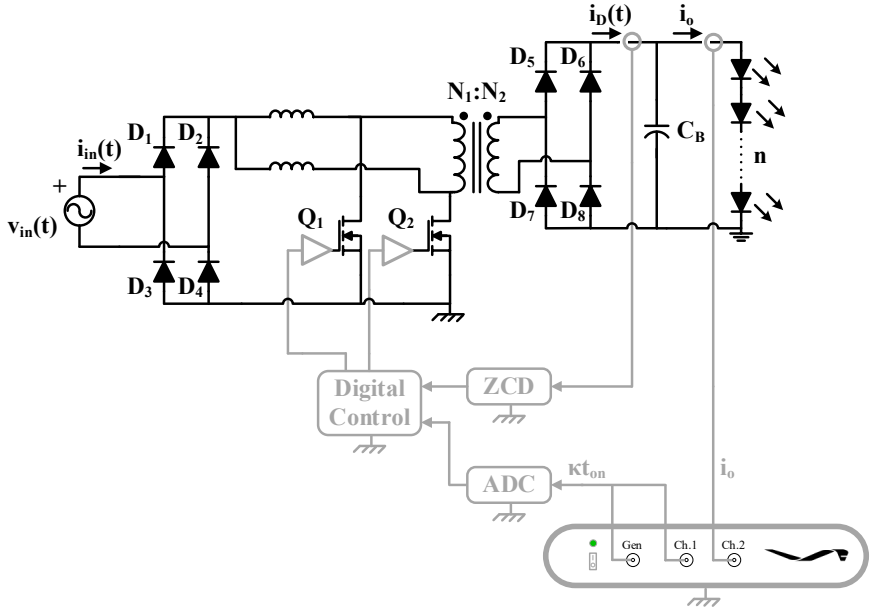

Fig. 3.15. Measuring setup for the open loop response relating t_{on} and i_o on the DICPP ac-dc LED driver, based on a Venable® 6320 frequency analyzer.

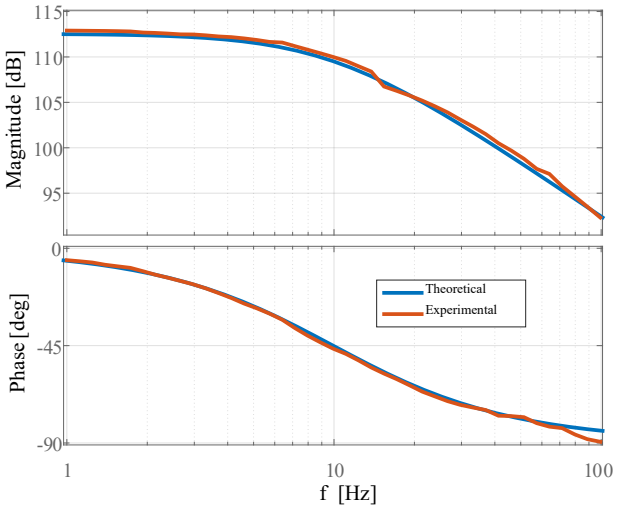

Fig. 3.16. Comparison of the theoretical and experimental measurements of the t_{on} to i_o transfer function (3.29).

adequately obtain the frequency response. The frequency response in this case is obtained by measuring i_o with a current probe in the second channel and the signal generated by the Venable with the first channel.

It is important to note that in order to accurately compare the theoretical response with the experimental data the gain from the ADC and the required scaling of t_{on} need to be taken into account in conjunction with the gain of the current probe. Thus, obtaining Fig. 3.16, where the obtained response is compared with (3.29). The values used to represent (3.29) in Fig. 3.16 are summarized in Table 3.5 corresponding with the values assigned to the components of the experimental prototype. As can be seen the theoretical model matches the experimental result, showing a low bandwidth caused by the low dynamic of the electrolytic capacitor. In fact, in this case the design of the regulator is straightforward and is extremely similar to any ac-dc converter output loop, which can be accomplished with a simple PI [3.37].

Table 3.5. Values used to obtain the theoretical waveform of (3.29).

	Value
V_{gp}	110 Vrms
L	860 µH
T_{on}	7.1 µs
C_o	2.2 mF
$\frac{n}{m} r_{LED}$	5.5 Ω
V_o	48 V

3.5 Conclusions

The present chapter presents a simple, single-phase, single-stage, isolated, ac-dc, LED driver with two switches referenced to the same ground based on a current-fed topology retrieved from literature. In fact, the DICPP ac-dc LED driver is able to deal with most of the issues that limited current-fed ac-dc converters when performing PFC: switches withstanding extremely high voltages, complex transformer designs and low efficiency.

In addition, the DICPP ac-dc LED driver shows a handful of advantages when it is compared against some of the conventional single-phase, single-stage, ac-dc, LED drivers, from Table 3.4:

- It is able to achieve high efficiencies for an isolated single-stage.
- It is able to reduce the traditionally high input current ripple of a converter operating in BCM with the use of a single transformer, by using the in-built interleaving between the two branches that comprise the topology.
- The presented control of both inductors in equivalent BCM helps on obtaining a simple LFR performance. In fact, with the proposed implementation it is possible to accurately control the ac-dc LED driver from a single isolated measurement.

These advantages come at the prize of including two more magnetic components, another active switch reference to the primary ground and a high frequency diode bridge, in comparison to a conventional flyback converter. As regards the reduction of the input current ripple, the addition of more branches is not scalable for a single ac-dc LED driver. In that sense, the solution is the interleaving of more DICPP ac-dc LED drivers with an adequate phase-shift in between, again, keeping one switch as the master and the rest as the slaves.

Nevertheless, the DICPP ac-dc LED driver has some drawbacks:

- It still requires a demagnetization circuit to prevent the switches from destruction in case of a control failure. Fact that is intrinsic to current-fed based topologies.
- It is unable to remove the electrolytic capacitor present in single-phase, single-stage, ac-dc LED drivers that require a high PF.
- Even though, it has a significant voltage stress reduction on its main switches in comparison to the traditional CPP, being a converter from boost family, which uses the transformer as a mean to reduce its output voltage, its switches still show significant voltage stress that require the use of SiC for universal or European input voltage solutions.
- The proposed control is based on equivalent BCM, which implies that the frequency varies during its operation. Even though the high ripple is reduced, and this fact affects positively the design of the EMI filter, the variable frequency still impacts its size and complexity negatively in comparison to other solutions that operate with fixed frequency. In that sense, and considering the impact of

losses of both inductors and transformer, the operation of the DICPP ac-dc LED driver can be benefitted from operating in CCM.

Not being able to dispose of the electrolytic capacitor is the most troublesome of the drawbacks for an LED driver that require a long lifespan. However, this is the price to pay for a simple, cost efficient, single-phase, single-stage, ac-dc LED driver at these power levels, which can be easily fixated by turning it into a quasi-single-stage applying any of the well-known methodologies discussed along Chapter 1.

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4

High-frequency AC-LED drivers based on ZCS-QRCs

I decided that the most terrible enigmas are the ones that mask themselves as madness. But now I have come to believe that the whole world is an enigma, a harmless enigma that is made terrible by our own mad attempt to interpret it as though it had an underlying truth.

— Foucault's Pendulum, Umberto Eco.

The present chapter discusses the use of the LED load as the rectifier of the power converter, replacing in the process the rectifier diode required in the conventional dc-dc power converters. This proposal removes not only the conventional rectifier but the required output capacitance, driving the LED load with a high frequency current similarly to a PWM driving. However, to be able to introduce this change, the switching performance of a lighting LED has to be carefully studied and validated, with special focus on the reverse-recovery effect. In that respect, to remove the reverse-recovery effect on the LED load, the main switch of the proposed topologies is replaced with a full-wave resonant switch making possible to reduce the di/dt during the turn-off of the LED load, therefore eliminating said effect. In addition, for the proposed quasi-resonant LED drivers full dimming is achieved by means of changing the switching frequency, varying the turn-off while keeping a constant turn-on time. This conclusion is reached after a thorough analytical study of the quasi-resonant LED drivers, which is further validated with the construction of two experimental prototypes. As a part of the experimental validation, a reliability study comparing the conventional LED drivers with the two proposed solutions for two different dimming points has been carried out over 700 h, with the aim of studying the impact of the reverse-recovery effect on the lifetime of the LEDs.

4.1 Introduction

Traditionally, ac-dc LED drivers, when cost is not the main concern and their reliability and efficiency are of the utmost importance, use a two-stage [4.1] or a multi-stage approach [4.2]. Particularly for multi-stage ac-dc LED drivers the last stage is normally used for the sole purpose of controlling the current across the LED load, in such a way that dimming can be achieved. This last stage is normally referred in literature as post-regulators. A post-regulator is normally used to control the current across each LED string that comprises the LED load, which requires the post-regulator stage to be cheap and highly efficient, while achieving a high power density [4.3]-[4.6].

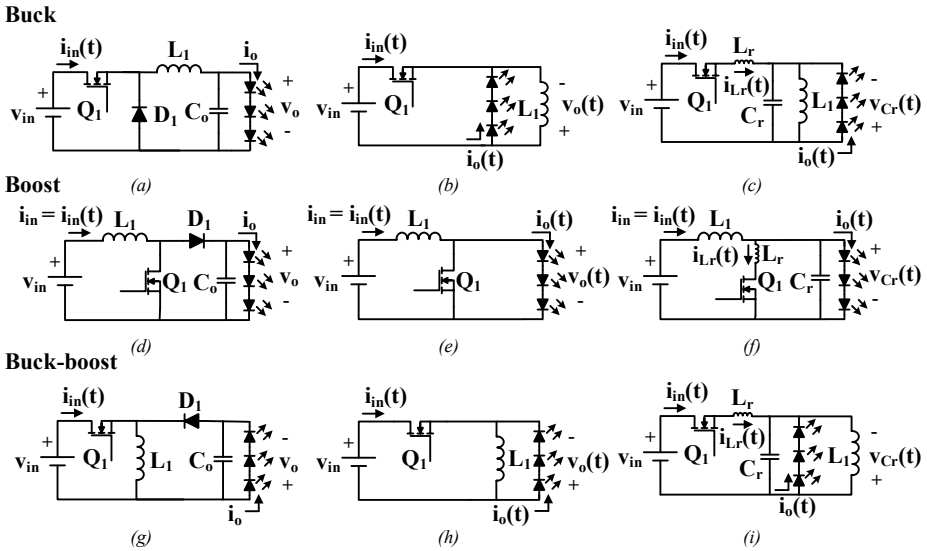


Fig. 4.1. Basic topologies used as post-regulators and their proposed derivations. (a) Buck converter. (b) DL//L AC-LED driver. (c) DL//L ZCS-QRC AC-LED driver. (d) Boost converter. (e) DL//S AC-LED driver. (f) DL//S ZCS-QRC AC-LED driver. (g) Buck-boost converter. (h) DL//L AC-LED driver. (i) DL//L ZCS-QRC AC-LED driver.

The idea presented in this chapter is based on using the basic dc-dc power converter topologies (i.e., buck, boost and buck-boost), which are depicted in Fig. 2.2 (a), (d) and (g), and replacing their rectifier diode, D_1, with the LED load while short-circuiting their output, thus removing the output capacitance from the circuit. As a result, two different converters can be derived, considering that both the buck and the buck-boost render the same topology. The derived topologies are: LED parallel with switch (i.e., DL//S AC-LED driver, see Fig. 2.2 (e)) and LED paralleled with the converter inductor (i.e., DL//L AC-LED driver, see Fig. 2.2 (b) and (h)). It should be noted, that while in the conventional buck, boost and buck-boost converters, the LED load is supplied with a constant current, in the DL//S and DL//L AC-LED drivers, however, the LED load is supplied with a pulsed current, which is pulsing at the same frequency as the main switch (i.e., Q_1). This performance is to be expected taking into consideration that the LED load is to be driven by the high frequency rectifier current, which should not be problematic for the human eye as these high frequency modulations of the light will be filtered. In fact, the operation of LEDs at high frequencies, higher than 100 kHz, acting as the rectifier diode of power converters, and referred in literature as high-frequency AC-LED

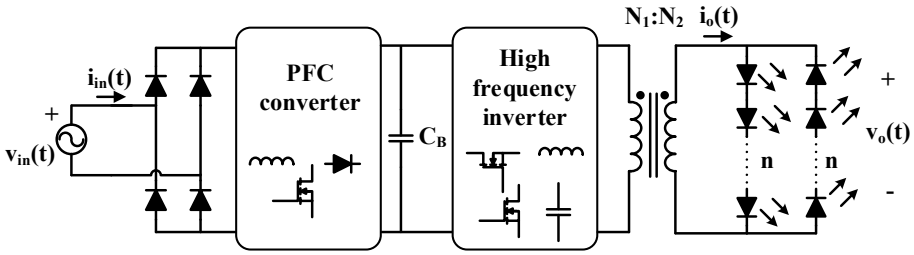


Fig. 4.2. Typical block diagram of a two-stage isolated AC-LED driver based on a high frequency inverter.

driving, has been studied by means of resonant isolated half bridges applying a sinusoidal high frequency current waveform to the LED load [4.7]-[4.9], see Fig. 4.2 for a simplified diagram of the aforementioned ac-dc LED driver. Other authors proposed the high frequency driving with a flyback converter operating in DCM [4.10] or even by means of self-oscillating topologies [4.11]. Nevertheless, none of this works provide factual evidence on how will the LEDs perform under a high frequency sinusoid or triangular current waveforms in terms of light quality, reliability or CCT.

For that matter, some studies have been dedicated to the driving of LEDs under different current waveforms (i.e., sinusoidal, square and triangular) at 50 Hz [4.12] or up to 1 MHz with square waveforms [4.13], [4.14]. Some important conclusions can be extracted from these works. First, the increase of frequency in a square current waveform from 100 Hz to 300 kHz does not have a negative impact on either junction temperature or luminous efficacy. Second, pulsed current driving shows an improvement on the lifetime of the LEDs in comparison with dc current driving. Third, dimming performance achieved with pulse current driving, as long as the peak current level is maintained the same, shows less chromaticity shifts in comparison with dc current driving [4.15]. And fourth, switching an LED at frequencies higher than 3 kHz presents no visible flicker or harmful effects to human viewers [4.16].

If the aforementioned facts on pulse current driving are taken into account, it can be concluded that high frequency AC-LED driving seems promising, however, there is no factual prove either, as how well an LED would operate as a rectifier. This happens because of the lack of dynamic characterization provided by white LED manufacturers in their datasheets. In previous literature, some studies have characterized the frequency response of white LEDs for Visible Light Communications (VLC) [4.17], showing a bandwidth of up to 3 MHz for regular white light. However, this study does not give any insight on how fast can a white LED truly switch. Thus, a study to characterize the LED load under high frequency switching operation is required to observe, whether the well-known phenomenon of reverse recovery could occur in the proposed topologies when using LEDs as the rectifier diode of the topology [4.18]. Considering that the latter can occur and that its implications are not clear, it is necessary to search for ways to diminish or even eliminate its effects. In that regard, the approach is decreasing the di/dt during the turn-off of the LEDs, performed in literature by increasing the amount of switches [4.19], which is not desired, or by means of Zero-Current-Switched Quasi-Resonant Converters (ZCS-QRCs) [4.20]-[4.23]. The di/dt reduction during the turn-off of the rectifier diode occurs in a ZCS-QRC, due to the inclusion of an inductor in the path of the main switch, causing the current through the rectifier to diminish steadily to the zero value, in contrast

to the traditional dc-dc topology where it is drained as rapidly as possible. Therefore, taking into account this performance of ZCS-QRCs and replacing the main switch of the DL//L AC-LED driver and DL//S converters with the full-wave resonant switch, renders two AC-LED drivers: the DL//L ZCS-QRC AC-LED driver, see Fig. 2.2 (c) and (i) and the DL//S ZCS-QRC AC-LED driver, see Fig. 2.2 (f).

The proposed AC-LED drivers are aimed to be used as the post-regulator stage of an ac-dc LED driver, and as such, their operation needs to be carefully analyzed, in order to understand the dependency of the output current on their different design parameters.

4.2 Operating principle

The presented AC-LED drivers are based on using the LEDs as the rectifier diode of a dc-dc converter in conjunction with a full-wave resonant switch and no output capacitor, thus generating an ac output voltage and current plus a dc component. The main reason for using a full-wave resonant switch in spite of a half-wave resonant switch, comes from the necessity of achieving full dimming capabilities. It is a well-known fact that the dynamic response between the control variable and the output, greatly varies with the load in half-wave ZCS-QRC [4.20]. Therefore, in an LED driver in which the output current is to be not only controlled but able to vary from zero to maximum current, the huge dynamic variation with the load will unnecessarily complicate its control.

In the forthcoming analysis, there are some previous considerations that need to be made in order to understand the operation of the AC-LED drivers and to attain a useful model to predict their performance. The LED load equivalent circuit with its dynamic resistance and knee voltage source will be considered taking into account that only one string will be fed in this scenario, considering the aim as post-regulators to ensure current sharing. In addition, the main switch, Q_1, will be considered as ideal and the main inductor, L_1, will be considered to be much larger than the resonant inductor, L_r, so L_1 does not affect the resonance between L_r and the resonant capacitor, C_r. The latter is a well-known fact in ZCS-QRCs and it is also considered as the starting point of the analysis carried out in [4.20]. Particularly, for the proposed topology, L_1 needs to be large enough to satisfy that the current ripple is also as small as possible, thus being able to consider the output current as constant during the conduction of the LEDs ($i_{in}(t) = i_{in}$, see Fig. 4.3). This reason is what makes the increase of the switching frequency attractive to diminish the size of L_1, which is the most limiting element in terms of volume. In that respect, the increase of frequency makes also attractive the use of soft-switching techniques to diminish the switching losses.

Then, taking into account the aforementioned considerations, the resonant tank comprised by L_r and C_r, will have an angular frequency of,

$$\omega_n = \frac{1}{\sqrt{L_r C_r}} \ . \tag{4.1}$$

In addition, the characteristic impedance can be defined as,

$$Z_n = \sqrt{\frac{L_r}{C_r}} \ . \tag{4.2}$$

It is possible, after taking into account all the previous considerations, to start the analysis of the DL//S ZCS-QRC and the DL//L ZCS-QRC AC-LED drivers, which will be carried out independently.

4.2.1 Static analysis of the DL//S ZCS-QRC AC-LED driver

The working principle will be studied by understanding the four equivalent circuits that the DL//S ZCS-QRC AC-LED driver undergoes during its operation, which are depicted in Fig. 4.3. Accordingly, Fig. 4.4 shows the most representative waveforms depicting the same time intervals as the previous figure, in order to exemplify the achievement of ZCS on the main switch under a correct operation of the DL//S ZCS-QRC AC-LED driver. For that matter, each of the stages will be analyzed individually obtaining the behaviour over time of the most representative variables by solving the state equations defined by each of the equivalent circuits.

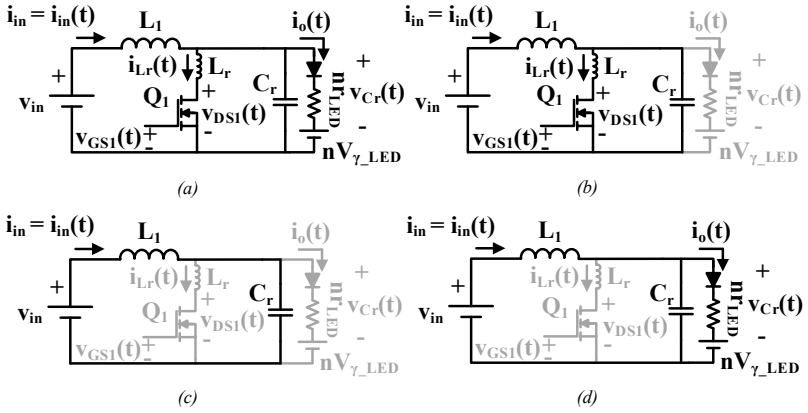


Fig. 4.3. Equivalent circuits of the DL//S ZCS-QRC AC-LED driver. (a) [t_0, t_1] Linear stage. (b) [t_1, t_2] Resonant stage. (c) [t_2, t_3] Delay stage. (d) [t_3, t_4] Lighting stage.

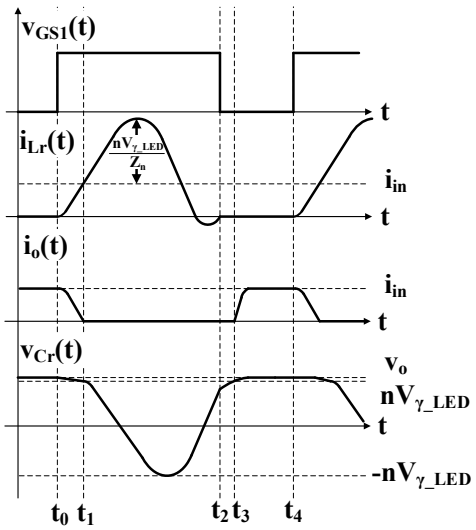


Fig. 4.4. Most representative waveforms to understand the operation of the DL//S ZCS-QRC AC-LED drivers.

Linear stage, from t_0 to t_1, see Fig. 4.3 (a): Coming from the stage where the LED load is supplied with a constant current, this stage starts when Q_1 is turned-on by the control signal. At the time Q_1 is turned-on, $i_{Lr}(t)$ will start increasing steadily in accordance to the magnetization of L_r, causing $i_o(t)$ to decrease with the same slope, until it reaches the zero current value. The latter marks the end of this stage.

The initial conditions for this stage are $i_o(0) = i_{in}$, $i_{Lr}(0) = 0$ and $v_{Cr}(0) = v_o$, and the state equations are defined by,

$$\begin{cases} i_{in}=i_{L_r}(t)+C_r\dfrac{dv_{C_r}(t)}{dt}+i_o(t) \\ v_{C_r}(t)=i_o(t)nr_{LED}+nV_{\gamma\_LED}\,, \\ L_r\dfrac{di_{L_r}(t)}{dt}=v_{C_r}(t) \end{cases} \tag{4.3}$$

where i_{in} represents the input current considered as a constant due to the larger value of L_1, $i_{Lr}(t)$ represents the current through L_r, $i_o(t)$ represents the current through the LED load and $v_{Cr}(t)$ represents the voltage withstood by the LED load and v_o is the maximum voltage withstood by the LED load during its operation, which is defined by,

$$v_o=i_{o,max}nr_{LED}+nV_{\gamma\_LED}\,, \tag{4.4}$$

and where $i_{o,max}$ is the maximum output current.

By solving (4.3), the analytical waveforms for this stage can be obtained as,

$$v_{C_r}(t)=L_r\left(i_{in}+\frac{V_{\gamma\_LED}}{r_{LED}}\right)a(t)+v_o b(t), \tag{4.5}$$

$$i_{L_r}(t)=\frac{v_o}{L_r}a(t)+\left(i_{in}+\frac{V_{\gamma\_LED}}{r_{LED}}\right)c(t), \tag{4.6}$$

where a(t), b(t) and c(t) are defined as follows,

$$a(t)=\frac{1}{2\omega_n\sqrt{\xi^2-1}}\left(e^{-\left(\xi-\sqrt{\xi^2-1}\right)\omega_n t}-e^{-\left(\xi+\sqrt{\xi^2-1}\right)\omega_n t}\right), \tag{4.7}$$

$$b(t)=\frac{1}{2\sqrt{\xi^2-1}}\left[\left(\xi+\sqrt{\xi^2-1}\right)e^{-\left(\xi+\sqrt{\xi^2-1}\right)\omega_n t}-\left(\xi-\sqrt{\xi^2-1}\right)e^{-\left(\xi-\sqrt{\xi^2-1}\right)\omega_n t}\right], \tag{4.8}$$

$$c(t)=1+\frac{1}{2\sqrt{\xi^2-1}}\left[\left(\xi-\sqrt{\xi^2-1}\right)e^{-\left(\xi+\sqrt{\xi^2-1}\right)\omega_n t}-\left(\xi+\sqrt{\xi^2-1}\right)e^{-\left(\xi-\sqrt{\xi^2-1}\right)\omega_n t}\right], \tag{4.9}$$

and where ξ is defined by,

$$\xi = \frac{1}{2r_{LED}}\sqrt{\frac{L_r}{C_r}}. \tag{4.10}$$

From (4.3) and (4.5), $i_o(t)$ can be derived, which can then be used to determine the duration of this stage taking into consideration it finishes when $i_o(t)$ reaches the zero value. However, it would be unpractical to use the aforementioned equations in this calculation. Therefore, a practical approximation is required to increase the practicality of the analysis. For that matter, $v_{Cr}(t)$ will be considered as a constant voltage, taking into account that during this stage the voltage on the LED load diminishes until it reaches nV_{γ_LED}, in accordance to (4.3), voltage at which $i_o(t)$ reaches zero. The approximation can be applied considering that nV_{γ_LED} is the most significant term of $v_{Cr}(t)$. Then, using this approximation, (4.3) can be simplified to,

$$L_r\frac{di_{L_r}(t)}{dt} = v_o, \tag{4.11}$$

$$i_o(t) = i_{in} - i_{L_r}(t). \tag{4.12}$$

Solving for $i_o(t)$ in the system comprised of (4.11) and (4.12), yields,

$$i_o(t) = i_{in} - \frac{v_o}{L_r}t\,, \tag{4.13}$$

which, then, taking into consideration that $i_o(t_1) = 0$, gives the approximated duration of this stage as,

$$t_1 - t_0 = \frac{L_r i_{in}}{v_o}. \tag{4.14}$$

As can be seen the value of L_r controls the duration of this stage, because of it being the one that prevails over the other design parameters. Therefore, with an adequate selection of the value of L_r the di/dt of $i_o(t)$ can be selected to reduce or even eliminate the effect of the reverse recovery caused by the LEDs due to their operation as rectifiers. This makes this stage key for the correct operation of the DL//S ZCS-QRC AC-LED driver, marking (4.14) as the first design criteria, which will define the minimum value of L_r.

Resonant stage, from t_1 to t_2, see Fig. 4.3 (b): The second stage starts right after the previous one, exactly at the time when the LED load is turned-off, and it ends in a resonant period when Q_1 is turned-off. It should be noted that due to the main switch being a full-wave resonant switch, the current $i_{Lr}(t)$ is allowed to become negative. This fact implies that the driving signal of Q_1 is no longer in control of the flow of the current, as the parasitic diode will be the one conducting when the control signal is turned-off, causing inaccuracies to occur in terms of the on time, t_{on}. If the last scenario were the case, then the stage will finish when the current through the main switch reaches the zero value again. In this stage, the state equations are similar to those of the boost ZCS-QRC [4.20], which are defined by,

$$\begin{cases} L_r \dfrac{di_{L_r}(t)}{dt} = v_{C_r}(t) \\ C_r \dfrac{dv_{C_r}(t)}{dt} = i_{in} - i_{L_r}(t) \end{cases}, \tag{4.15}$$

and whose initial conditions are: $v_{Cr}(t_1) = nV_{\gamma\_LED}$ and $i_{Lr}(t_1)$ defined by (4.6) at the end of the linear stage.

From (4.15), the waveforms of the most representative variable can be derived as,

$$i_{L_r}(t) = i_{in} + \frac{nV_{\gamma_{LED}}}{Z_n}\sin(\omega_n t) + \left(i_{L_r}(t_1) - i_{in}\right)\cos(\omega_n t), \tag{4.16}$$

and,

$$v_{C_r}(t) = nV_{\gamma_{LED}}\cos(\omega_n t) - Z_n\left(i_{L_r}(t_1) - i_{in}\right)\sin(\omega_n t), \tag{4.17}$$

by solving the system.

The duration of this stage can be obtained considering that at the end of the stage $i_{Lr}(t_2)$ needs to be equal to zero, and that the term $\left(i_{L_r}(t_1) - i_{in}\right)$ is negligible in comparison to the other terms of (4.16), as by the end of the linear stage most of the input current goes across L_r. Thus,

$$t_2 - t_1 = \frac{\alpha_n}{\omega_n}, \tag{4.18}$$

where α_n is defined by,

$$\alpha_n = \arcsin\left(\frac{-i_{in}Z_n}{nV_{\gamma\_LED}}\right), \quad \frac{3\pi}{2} < \alpha_n < 2\pi. \tag{4.19}$$

It should be noted that the range of values defined for α_n in (4.19), ensures that $i_{Lr}(t_2)$ equals zero at the second time $i_{Lr}(t)$ crosses the zero value. The reason can be explained with (4.16), because in order to make $i_{Lr}(t)$ equal to zero the sine must be negative, thus $\omega_n t$ needs to vary from π to 2π. For that matter, the first time $i_{Lr}(t)$ crosses the zero value would be between π and $3\pi/2$, making the range from $3\pi/2$ to 2π the one during which the second zero crossing would happen.

Delay stage, from t_2 to t_3, see Fig. 4.3 (c): This stage happens if by the end of the resonant stage the voltage on C_r is lower than nV_{γ_LED}, thus requiring C_r to be charged to the aforementioned voltage value in order to transit into the last stage. The initial conditions set for this stage are only applicable to $v_{Cr}(t)$, taking the value provided by the previous stage, $v_{Cr}(t_2)$. In comparison to the other stages the analysis of the current stage is quite simple, as it is defined by,

$$C_r \frac{dv_{C_r}(t)}{dt} = i_{in}. \tag{4.20}$$

Therefore, $v_{Cr}(t)$ follows the next expression,

$$v_{C_r}(t)=\frac{i_{in}}{C_r}t+v_{C_r}(t_2), \tag{4.21}$$

which defines that C_r is being charged linearly. From (4.21), the duration of the stage can be obtained by considering $v_{Cr}(t_3) = nV_{\gamma\_LED}$. Then,

$$t_3-t_2=\frac{C_r\left(nV_{\gamma\_LED}-v_{C_r}(t_2)\right)}{i_{in}}. \tag{4.22}$$

Eq. (4.22) states that the higher the value of C_r, the longer it will take for this stage, which also translates in a delay for the LED load to start illuminating, hence the name of the stage. Therefore, (4.22) marks another key equation for the design of the DL//S ZCS-QRC AC-LED driver.

Lighting stage, from t_3 to t_4, see Fig. 4.3 (d): The last stage is reached when $v_{Cr}(t_3) = nV_{\gamma\_LED}$, which as has been said, marks the end of the delay stage. This stage represents the one, during which, the LED load is actually turned-on emitting light, and whose state equations are defined by,

$$\begin{cases} i_{in}=i_o(t)+C_r\dfrac{dv_{C_r}(t)}{dt} \\ v_{C_r}(t)=i_o(t)nr_{LED}+nV_{\gamma\_LED} \end{cases}. \tag{4.23}$$

The initial conditions for this stage are defined by $i_o(t_3) = 0$ and $v_{Cr}(t_3) = nV_{\gamma\_LED}$.

Solving the system defined in (4.23) with the aforementioned initial conditions, renders,

$$v_{C_r}(t)=i_{in}nr_{LED}\left(1-e^{-\frac{1}{nr_{LED}C_r}t}\right)+nV_{\gamma\_LED}, \tag{4.24}$$

and

$$i_o(t)=i_{in}\left(1-e^{-\frac{1}{nr_{LED}C_r}t}\right), \tag{4.25}$$

where it can be seen that $i_o(t)$ increases exponentially until it reaches its steady state value, defined by i_{in}. The time it takes $i_o(t)$ to reach i_{in} can be approximated by,

$$t_d-t_3=5nr_{LED}C_r, \tag{4.26}$$

considering that it will take five times the time constant to reach said value, and where t_d defines the time i_{in} is reached by $i_o(t)$. This time is completely dependent on C_r, marking a key equation for the selection of this component. In fact, the designer needs to choose between the most restrictive of (4.22) and (4.26) as both determine the turn-on delay of the LED load, depending mostly on the selected LEDs.

The end of this stage happens when Q_1 is turned-on again, thus, entering once more in the linear stage. In that respect the time duration of this stage can be defined considering the time of the rest of the stages. Then,

$$t_4-t_3=T_s-t_3+t_0. \tag{4.27}$$

where T_s is the switching period.

After the thorough analysis carried out for the four stages that comprise the full operation of the DL//S ZCS-QRC AC-LED driver, which is further detailed in Appendix C, a relationship needs to be established between the input and the output current. This is to correctly understand, in this topology, how to control $i_o(t)$. For that reason, the average value of $i_o(t)$ will be calculated by integrating it in a whole switching period, taking into consideration that for practical reasons the linear and the delay stages are negligible, in comparison to the duration of the resonant and lighting stages. For that matter the duration of the lighting stage will be considered as T_s-T_n. Hence,

$$i_o=\frac{1}{T_s}\int_0^{T_s-T_n} i_o(t)dt= i_{in}\left(\frac{T_s-T_n}{T_s}-\frac{nr_{LED}C_r}{T_s}\right), \tag{4.28}$$

where i_o is the average value of the output current and T_n is the resonant period. In (4.28), the term that depends on $nr_{LED}C_r$, which defines the time constant of the exponential that describes $i_o(t)$ during the lighting stage, can be considered negligible, see Fig. 4.4. Therefore,

$$i_o=i_{in}(1-\mu) \tag{4.29}$$

where μ is the variable capable of controlling the current given to the LED load, being defined as,

$$\mu=\frac{T_n}{T_s}=\frac{f_s}{f_n}, \tag{4.30}$$

where f_s is the switching frequency and f_n is the resonant frequency.

This analysis concludes that the DL//S ZCS-QRC AC-LED driver can control its average output current by varying the switching frequency while keeping a constant on-time coincidental with the duration of the resonant stage, similarly to a dc-dc full-wave boost ZCS-QRC. In that respect, Fig. 4.5 shows a comparison between the dc-dc full-wave boost ZCS-QRC and the DL//S ZCS-QRC AC-LED driver, in terms of the

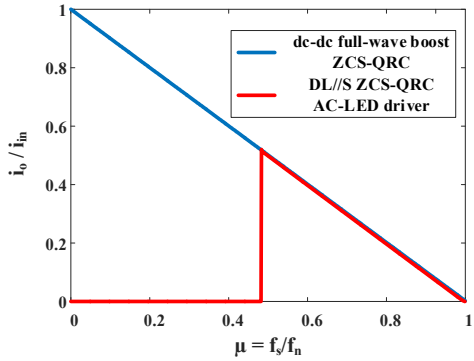


Fig. 4.5. Comparison of i_o/i_{in} versus μ for the dc-dc full-wave boost ZCS-QRC and the DL//S ZCS-QRC AC-LED driver.

relationship between i_o and i_{in} when varying μ. As can be seen, the behaviour of the DL//S ZCS-QRC AC-LED driver is extremely similar to the dc-dc full-wave boost ZCS-QRC, except for low values of μ. The reason can be explained due to the delay stage, as for the lower values of μ, $v_{Cr}(t)$ will never surpass nV_{γ_LED} and the DL//S ZCS-QRC AC-LED driver will be unable to enter into the lighting stage. Therefore, no current will be flowing across the LED load. It should be noted that the value at which the LED will stop lighting will depend on the design, which happens to be around μ equal to 0.5 for the scenario depicted in Fig. 4.5.

The last part of the analysis carried out for the DL//S ZCS-QRC AC-LED driver is to study the condition that ensures the achievement of ZCS on Q_1. For that reason, (4.16) and (4.19) need to be studied in order to attain the ZCS condition. In order to achieve ZCS, the $i_{Lr}(t)$ during the resonant stage needs to reach the zero value, meaning that the amplitude of the sinusoid needs to be, at least, equal to i_{in}. Therefore,

$$\frac{nV_{\gamma\_LED}}{Z_n} \geq i_{in}. \tag{4.31}$$

4.2.2 Static analysis of the DL//L ZCS-QRC AC-LED driver

The static analysis of the DL//L ZCS-QRC AC-LED driver can be carried out in a similar fashion to the one that has been performed for the DL//S ZCS-QRC AC-LED driver. In addition, the current through L_1 will also be considered as a constant to simplify the analysis, considering L_1 will be selected to be much larger than L_r and to have as little ripple as possible at the output current during the conduction of the LED load.

It should be noted that the topology selected to carry out this subsection is not the one depicted in Fig. 2.2 (c) and (i), but an equivalent with its main switch referred to the ground of the input voltage, see Fig. 4.6 (a). This practical change simplifies the driving of the main switch, not requiring an isolated driver and is made possible due to having an LED based load.

In order to properly analyze the topology it will be divided into the four equivalent circuits that the DL//L ZCS-QRC undergo during its operation, see Fig. 4.6. Furthermore, the most representative waveforms to exemplify the operation are presented in Fig. 4.7, sharing the same time basis as the equivalent circuits of Fig. 4.6. From these figures it can be seen at a glance how similar the operation is to the DL//S ZCS-QRC AC-LED driver.

Linear stage, from t_0 to t_1, see Fig. 4.6 (a): This stage starts when Q_1 is turned-on, opening a path for the input current and draining steadily the current that is being fed to the LED load. Therefore, $i_{Lr}(t)$, which happens to be the same as $i_{in}(t)$, will start to increase making $i_o(t)$ to decrease accordingly.

From Fig. 4.6 (a), the state equations can be defined by,

$$\begin{cases} C_r \dfrac{dv_{C_r}(t)}{dt} = -i_{in}(t) + i_L - i_o(t) \\ v_{C_r}(t) = i_o(t) nr_{LED} + nV_{\gamma\_LED} \\ L_r \dfrac{di_{in}(t)}{dt} = V_{in} + v_{C_r}(t) \end{cases}. \tag{4.32}$$

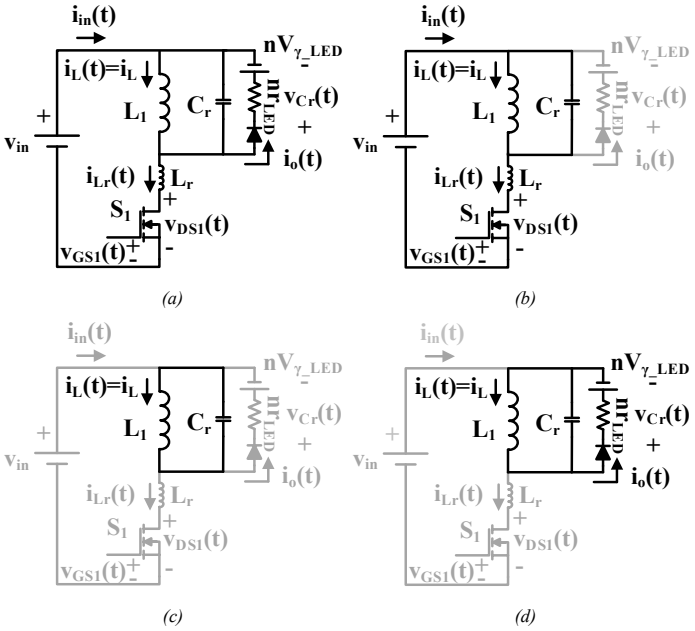


Fig. 4.6. Equivalent circuits of the DL//L ZCS-QRC AC-LED driver. (a) [t_0, t_1] Linear stage. (b) [t_1, t_2] Resonant stage. (c) [t_2, t_3] Delay stage. (d) [t_3, t_4] Lighting stage.

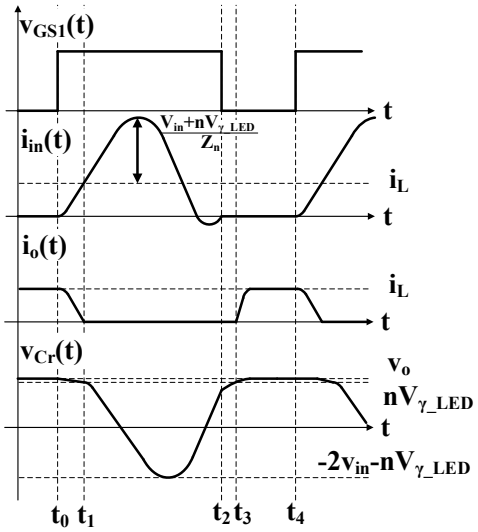


Fig. 4.7. Most representative waveforms to understand the operation of the DL//S ZCS-QRC AC-LED driver.

Solving the system in (4.32) for $v_{Cr}(t)$ and $i_{in}(t)$, considering the next initial conditions: $i_o(0) = i_L$, $i_{in}(0) = 0$ and $v_{Cr}(0) = v_o$, yields,

$$v_{C_r}(t)=v_{in}+L_r\left(i_L+\frac{nV_{\gamma\_LED}-v_{in}}{nr_{LED}}\right)a(t)-\left(v_{in}+v_o\right)b(t), \tag{4.33}$$

and,

$$i_{in}(t)=\frac{v_{in}+v_o}{L_r}a(t)-\left(i_L+\frac{nV_{\gamma\_LED}-v_{in}}{nr_{LED}}\right)c(t). \tag{4.34}$$

Note that a(t), b(t) and c(t) correspond to (4.7), (4.8) and (4.9), respectively.

Both, (4.33) and (4.34), define an accurate model during this stage for both $v_{Cr}(t)$ and $i_{in}(t)$, however, to estimate the practical duration of this stage, $v_{Cr}(t)$ will be, once again, considered constant at v_o. Redefining the system of (4.32) as,

$$\begin{cases} i_L=i_{in}(t)+i_o(t) \\ L_r\dfrac{di_{in}(t)}{dt}=v_{in}+v_o \end{cases}, \tag{4.35}$$

From (4.35), it becomes simple to attain the behaviour over time for $i_o(t)$ during this stage as,

$$i_o(t)=i_L-\frac{v_{in}+v_o}{L_r}t. \tag{4.36}$$

The time duration of this stage can be obtained considering that $i_o(t_1)$ needs to reach the zero current value by the end of this stage. Thus,

$$t_1-t_0=\frac{L_r i_L}{v_{in}+v_o}. \tag{4.37}$$

In this case, once again, it can be seen that this stage defines the di/dt of the LED load turn-off, which is controlled with the value of L_r. Thus, making it key for a correct design of the DL//L ZCS-QRC AC-LED driver.

Resonant stage, from t_1 to t_2, see Fig. 4.6 (b): This stage defines the resonant transition, which occurs between C_r and L_r. The start of this stage is marked by the LED load turn-off, finishing for the full-wave resonant switch in a resonant period whenever $i_{Lr}(t)$ crosses zero a second time. The state equations are defined by,

$$\begin{cases} L_r\dfrac{di_{in}(t)}{dt}=v_{in}+v_{C_r}(t) \\ C_r\dfrac{dv_{C_r}(t)}{dt}=i_L-i_{in}(t) \end{cases}, \tag{4.38}$$

with its initial conditions being: $v_{Cr}(t_1) = nV_{\gamma\_LED}$ and $i_{in}(t_1)$, which are derived from (4.33) and (4.34) at the end of the previous stage.

Therefore, solving (4.38) gives,

$$i_{in}(t)=i_L+\frac{v_{in}+nV_{\gamma\_LED}}{Z_n}\sin(\omega_n t)+(i_{in}(t_1)-i_L)\cos(\omega_n t), \tag{4.39}$$

and,

$$v_{C_r}(t)=v_{in}-\left(v_{in}+nV_{\gamma\_LED}\right)\cos(\omega_n t)+Z_n\left(i_{L_r}(t_1)-i_L\right)\sin(\omega_n t). \tag{4.40}$$

In a similar fashion, the analysis carried out for the DL//S ZCS-QRC AC-LED driver can be applied to estimate the duration of this stage. Hence, it can be approximated by,

$$t_2-t_1=\frac{\beta_n}{\omega_n}, \tag{4.41}$$

taking into account that the term $(i_{in}(t_1)-i_L)$ can be considered to be negligible in comparison to the other terms defined in (4.39) and (4.40), as has been explained for the DL//S ZCS-QRC AC-LED driver, and where β_n can be defined by,

$$\beta_n=\arcsin\left(\frac{-i_L Z_n}{v_{in}+nV_{\gamma\_LED}}\right), \quad \frac{3\pi}{2}<\beta_n<2\pi. \tag{4.42}$$

within the range that guarantees the second zero crossing of $i_{in}(t)$ during this stage, in order to achieve ZCS on Q_1.

Delay stage, from t_2 to t_3, see Fig. 4.6 (c): This stage defines the time required to continuously charge C_r until $v_{Cr}(t)$ reaches nV_{γ_LED}. This event marks the end of this stage. The only initial condition is set for $v_{Cr}(t)$, whose initial value is defined by (4.40) at time instant t_2. The state equation is defined by,

$$C_r\frac{dv_{C_r}(t)}{dt}=i_L. \tag{4.43}$$

Hence, C_r gets charged following the next expression,

$$v_{C_r}(t)=\frac{i_L}{C_r}t+v_{C_r}(t_2). \tag{4.44}$$

As can be seen $v_{Cr}(t)$ increases linearly, in accordance to (4.44). Considering the end of this stage is marked by $v_{Cr}(t)$ reaching the knee voltage of the LED load (i.e., nV_{γ_LED}), then, (4.44) can be used to attain the duration of this stage. Thus,

$$t_3-t_2=\frac{C_r\left(nV_{\gamma\_LED}-v_{C_r}(t_2)\right)}{i_L}. \tag{4.45}$$

Lighting stage, from t_3 to t_4, see Fig. 4.6 (d): After having reached nV_{γ_LED} on $v_{Cr}(t)$ at the end of the delay stage, the LED load will start illuminating, and for that matter, it will move into the lighting stage. The end of this stage, is marked again by the turn-on of Q_1, which brings the DL//L ZCS-QRC AC-LED driver back into the linear stage. The state equations defined by this stage are summarized as,

$$\begin{cases} i_L = i_o(t) + C_r \dfrac{dv_{C_r}(t)}{dt} \\ v_{C_r}(t) = i_o(t) nr_{LED} + nV_{\gamma\_LED} \end{cases}. \tag{4.46}$$

The initial conditions for this stage are: $v_{Cr}(t_3) = nV_{\gamma\_LED}$ and $i_o(t) = 0$.

In fact, taking into account the system defined in (4.46) and the aforementioned initial conditions, the next expressions for $v_{Cr}(t)$ and $i_o(t)$ can be derived,

$$v_{C_r}(t) = i_L nr_{LED}\left(1 - e^{-\frac{1}{nr_{LED}C_r}t}\right) + nV_{\gamma\_LED}, \tag{4.47}$$

and

$$i_o(t) = i_L\left(1 - e^{-\frac{1}{nr_{LED}C_r}t}\right), \tag{4.48}$$

where it can be seen the exponential increase of $i_o(t)$ until it reaches i_L. In this case as well, the time it takes to reach the steady state of (4.48) is defined by (4.26) following the same reasoning, explained for the DL//S ZCS-QRC AC-LED driver. Hence, making (4.26) and (4.45) key equations for the selection of C_r in the DL//L ZCS-QRC AC-LED driver.

At this point of the analysis, it is necessary to study the relationship between the average input current and the average output current. The followed process will be similar to the DL//S ZCS-QRC AC-LED driver, thus, the first step is obtaining the average output current, taking again into consideration that both the linear and the delay stages can be considered negligible in comparison to the other two. For that matter, integrating (4.48) with a switching period gives,

$$i_o = \frac{1}{T_s}\int_0^{T_s - T_n} i_o(t)dt = i_L\left(\frac{T_s - T_n}{T_s} - \frac{nr_{LED}C_r}{T_s}\right). \tag{4.49}$$

Unlike the DL//S ZCS-QRC AC-LED, i_o depends on i_L, so a relationship between input and output cannot be made at a glance. In addition, $i_{in}(t)$ is no longer constant, and as such, it needs to be integrated within a switching period following the same principle and considerations given to (4.49). Thus, integrating (4.39) gives,

$$i_{in} = \frac{1}{T_s}\int_0^{T_n} i_{in}(t)dt = i_L\frac{T_n}{T_s}. \tag{4.50}$$

Then, a relationship between i_{in} and i_o can be made, by substituting (4.50) into (4.49). In fact, if again, the term $nr_{LED}C_r$ is neglected, then,

$$i_o = i_{in}\frac{(1-\mu)}{\mu}. \tag{4.51}$$

From this analysis, it can be seen that the control of the DL//L ZCS-QRC AC-LED driver can be performed by varying the switching frequency while keeping a constant t_{on}, similarly to the traditional ZCS-QRCs and in particular to the previously introduced DL//S ZCS-QRC AC-LED driver. In this particular case, the DL//L ZCS-QRC AC-LED driver resembles a convention dc-dc full-wave buck-boost ZCS-QRC. For this reason,

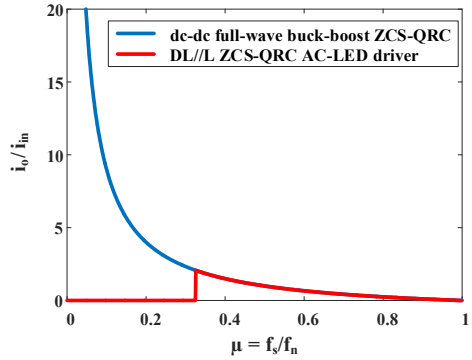


Fig. 4.8. Comparison of i_o/i_{in} versus μ for the dc-dc full-wave buck-boost ZCS-QRC and the DL//L ZCS-QRC AC-LED driver.

these two topologies are compared in Fig. 4.8 showing the similarities between the two, while taking into consideration that no output current can be given to the LED load, if the LED driver is unable to reach the lighting stage.

The last part of the analysis is to study the conditions that guarantee the achievement of ZCS on Q_1. Then, following the same principle as for the DL//S ZCS-QRC AC-LED driver, the condition needs to guarantee that (4.39) reaches the zero current value a second time. As has been previously explained, it would be necessary for i_L to be at least the same value as the variables multiplying the sinusoidal wave in the aforementioned equation. Hence, yielding,

$$\frac{v_{in}+nV_{\gamma\_LED}}{Z_n} \geq i_L, \tag{4.52}$$

which combined with (4.51) gives a much more practical equation:

$$\frac{v_{in}+nV_{\gamma\_LED}}{Z_n} \geq \frac{i_{in}}{\mu}. \tag{4.53}$$

4.2.3 Design criteria of the ZCS-QRC AC-LED drivers

A correct design of the aforementioned ZCS-QRC AC-LED drivers requires the following of several steps that are detailed below:

1. The value of L_r needs to be selected adequately to guarantee that the time the linear stage lasts is long enough to remove the reverse recovery effect on the LED load (i.e., decreasing the turn-off di/dt of the LED load), in accordance to (4.14) and (4.37) for the DL//S and the DL//L ZCS-QRC AC-LED drivers, respectively. This effect is completely reliant on the selected LEDs, and aiming for a turn-off di/dt of 500 A/ns or lower can be considered a good design practice for the newer LEDs on the market, as long as the time duration of this stage can be considered negligible at the switching period. It should be noted that the aforementioned turn-off di/dt value has been selected empirically, and would need to be revised by the designer considering it would entirely depend on the selected LED load.

2. Once L_r has been selected, the next step is selecting C_r. This case, however, depends on more than one equation and a trade-off between the duration of the delay stage, the start of the lighting stage and the compliance with the ZCS condition. In most scenarios, the most restrictive equation would be (4.31) and (4.53) for the DL//S and the DL//L ZCS-QRC AC-LED drivers, respectively. The issue of having long durations on the delay stage or at the start of the lighting stage, cause the lighting stage duration to be reduced. The reduction of the lighting stage causes the driving of the LED load to be performed with higher peak currents to achieve the same average output current in comparison to a scenario with higher effective times of the lighting stage. One of the solutions to avoid this performance is decreasing the switching frequency, however, it might not always be possible due to design restrictions. In those cases the best option is to avoid the compliance with the ZCS condition, aiming to reduce the duration of the problematic stages.
3. The selection of L_r and C_r determines the value of f_n, which at the same time will set the required switching frequency in accordance to μ. At this point, it is important to understand the variation of the switching frequency in ZCS-QRC AC-LED drivers with both power and the LED parameters. However, there are some previous steps to take into consideration before, as it is necessary to elucidate the dependencies of the switching frequency in the AC-LED drivers under study.
   For this reason, the average input power of the AC-LED driver can be defined by,

$$p_{in}=i_{in}v_{in}. \tag{4.54}$$

In addition, the maximum output power can be defined by,

$$p_{o,max}=i_{o,max}^2 nr_{LED}+i_{o,max}nV_{\gamma\_LED}. \tag{4.55}$$

Solving for $i_{o,max}$ in (4.55), gives,

$$i_{o,max}=\frac{-nV_{\gamma\_LED}+\sqrt{n^2V_{\gamma\_LED}^2+4p_{o,max}nr_{LED}}}{2nr_{LED}}. \tag{4.56}$$

Now, $i_{o,max}$ can be replaced with its average value and then with either (4.29) or (4.51), depending on the ZCS-QRC AC-LED driver under study. As an example, (4.29) will be substituted in (4.56), yielding,

$$\frac{(1-\mu)}{\mu}i_{in}=\frac{-nV_{\gamma\_LED}+\sqrt{n^2V_{\gamma\_LED}^2+4p_{o,max}nr_{LED}}}{2nr_{LED}}. \tag{4.57}$$

Next, considering an ideal power transfer between input and output, that is, 100 % efficiency, and solving for μ, gives,

$$\mu=\frac{f_s}{f_n}=1-\frac{v_{in}}{p_{o,max}}\frac{-nV_{\gamma\_LED}+\sqrt{n^2V_{\gamma\_LED}^2+4p_{o,max}nr_{LED}}}{2nr_{LED}}, \tag{4.58}$$

which is an expression that directly relates the frequency of the DL//S ZCS-QRC AC-LED driver with the power consumed and the LED characteristics. Then, normalizing f_s gives,

$$f_{s,norm}=1-\frac{v_{in}}{p_{o,max}}\frac{I_{base}}{2}\left(-1+\sqrt{1+4\frac{p_{o,max}}{nP_{base}}}\right), \tag{4.59}$$

where, as a reminder,

$$P_{base}=V_{\gamma\_LED}I_{base}, \tag{4.60}$$

and,

$$I_{base}=\frac{V_{\gamma\_LED}}{r_{LED}}. \tag{4.61}$$

Following the same process for the DL//L ZCS-QRC AC-LED driver, yields,

$$f_{s,norm}=\frac{1}{1+\frac{v_{in}}{p_{o,max}}\frac{I_{base}}{2}\left(-1+\sqrt{1+4\frac{p_{o,max}}{nP_{base}}}\right)}. \tag{4.62}$$

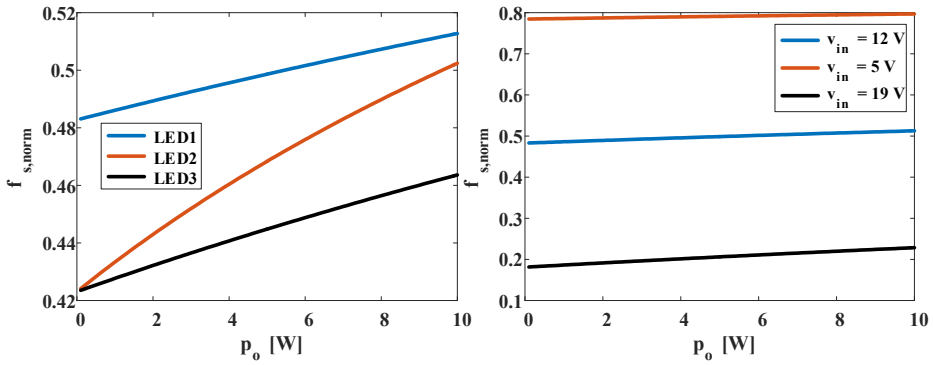
It is now possible to understand with which parameters f_s depends on, as are the maximum output power, the input voltage, and the LED characteristics. Therefore, in order to understand the implications of each one, the variation of f_s versus p_o will be plotted when varying at the same time the LED characteristics or the input voltage. For that matter, three different LEDs, forming with each an LED load comprised of 8 LEDs (i.e., n = 8), are compared in Fig. 4.9 (a) and Fig. 4.10 (a), whose characteristic values are summarized in Table 1.1. In addition, the analysis is extended to three different input voltages compared in Fig. 4.9 (b) and Fig. 4.10 (b).

As can be seen, in both Fig. 4.9 (a) and Fig. 4.10 (a), r_{LED} determines the wideness of the frequency range, whereas V_{γ_LED} determines the starting frequency. In what respects to Fig. 4.9 (b) and Fig. 4.10 (b), it can be seen that for the same LED load, lower input voltages imply the use of higher switching frequencies, whereas higher input voltages imply the use of lower switching frequencies.

4. The previous step showed a glimpse of the importance of selecting the correct LED load in order to attain an adequate operating range for f_s. Nonetheless, there are some cases in which the designer would not be able to have this degree of freedom, and would need to consider the implication of using higher or lower switching frequencies. In that sense, the maximum ratings are of utter importance, Table 4.2 summarizes the maximum ratings for all semiconductor devices (i.e., LED load and Q_1), which were obtained by carefully analyzing the previous equations. As can be seen, the LED load in the ZCS-QRC AC-LED drivers needs to withstand reverse voltages, which is an undesired performance. Nonetheless, and according to LED manufacturers, an LED is able to withstand a reverse voltage equal to its

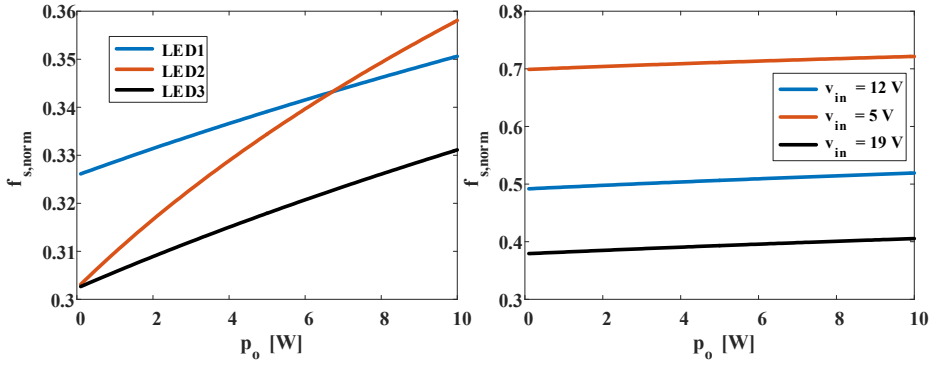
Table 4.1. Characteristic of the LEDs under study.

	V_{γ_LED}[V]	r_{LED}[Ω]	I_{base}	P_{base}
LED1	2.9	0.44	6.59	19.11
LED2	2.6	1	2.6	6.76
LED3	2.6	0.44	5.90	15.36



(a) *(b)*

Fig. 4.9. Comparison of f_s versus p_o for the DL//S ZCS-QRC AC-LED driver. (a) Different LED loads for an input voltage of 12 V. (b) Different input voltages for the same LED load.



(a) *(b)*

Fig. 4.10. Comparison of f_s versus p_o for the DL//L ZCS-QRC AC-LED driver. (a) Different LED loads for an input voltage of 24 V. (b) Different input voltages for the same LED load.

maximum forward voltage [4.24], which complies with the DL//S ZCS-QRC AC-LED driver, but unfortunately not for the DL//L ZCS-QRC AC-LED driver. In addition, the current stress on Q_1 becomes much higher than in the conventional topologies.

Table 4.2. Maximum semiconductor ratings for both DL//S and DL//L ZCS-QRC AC-LED drivers.

Maximum ratings	DL//S ZCS-QRC AC-LED driver	DL//L ZCS-QRC AC-LED driver
LED load reverse voltage	$-nV_{\gamma\_LED}$	$-2v_{in}-nV_{\gamma\_LED}$
LED load current	$\frac{i_o}{1-\mu}$	$\frac{i_o}{1-\mu}$
Q_1 breakdown voltage	v_o	v_o
Q_1 current	$\frac{i_o}{1-\mu}+\frac{nV_{\gamma\_LED}}{Z_n}$	$\frac{i_o}{1-\mu}+\frac{v_{in}+nV_{\gamma\_LED}}{Z_n}$

5. At this point of the design, there is only one more element that needs to be selected, which is the main inductance, L_1. The determination of its value can be done considering that its magnetization happens during t_{on}, being this fact the same for both ZCS-QRC AC-LED drivers. Thus, the current ripple across the main inductance can be defined by,

$$\Delta i_L=\frac{v_{in}}{L_1}t_{on}. \tag{4.63}$$

Then, considering t_{on} equal to T_n, as the linear stage can be neglected due to its low duration, yields the expression to determine L_1 in a DL//S ZCS-QRC AC-LED driver as,

$$L_1=\frac{v_{in}^2}{2p_{in}\Delta i_{\%}f_n}, \tag{4.64}$$

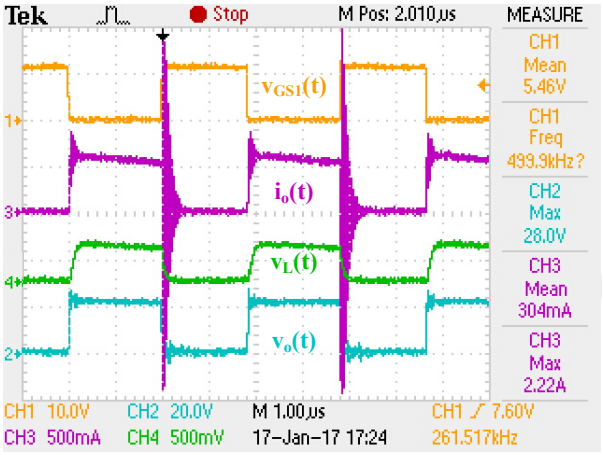
and L_1 in a DL//L ZCS-QRC AC-LED driver as,

$$L_1=\frac{v_{in}^2 f_s}{2p_{in}\Delta i_{\%}f_n^2}, \tag{4.65}$$

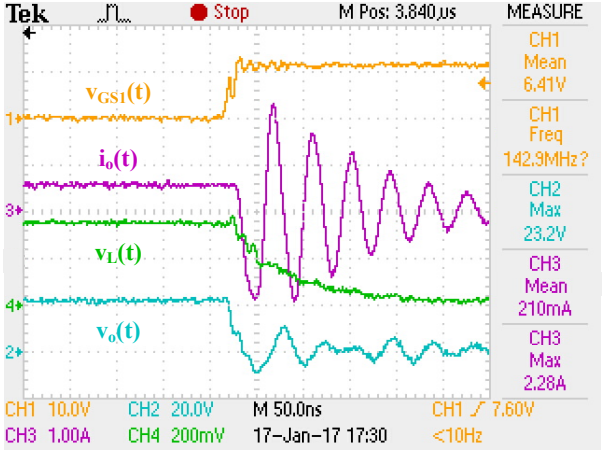
where $\Delta i_{\%}$ is the percentage ripple peak-to-peak of the input current.

4.3 Experimental results

The first analysis carried out, before validating the mathematical analysis of both ZCS-QRC AC-LED, drivers has been dedicated to the observation of the reverse recovery effect on the LED load on a DL//S AC-LED driver. For that reason, a DL//S AC-LED driver has been designed and built for a maximum power of 7.5 W driving a load comprised of 8 LEDs (i.e., Lumiled LXML-PWC2) in series. The most important waveform of the DL//S AC-LED driver are summarized in Fig. 4.11 switching at 500 kHz. As can be seen in Fig. 4.11 (a), $i_o(t)$ presents an undesirable ringing toward the turn-off of the LED load, while the rest of the waveforms are shown to be ideal. In fact, if this area is zoomed, see Fig. 4.11 (b), it can be seen that the ringing is caused by the huge reverse recovery effect of the LED load. In order to evaluate its impact on the light



(a)

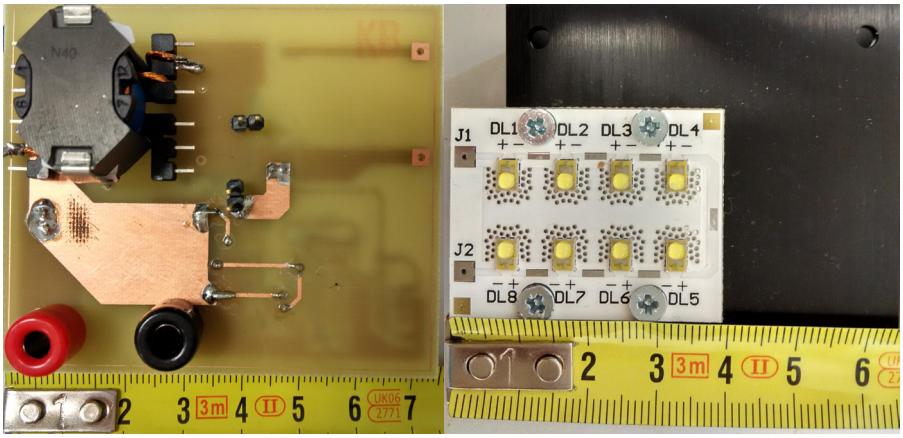


(b)

Fig. 4.11. Most representative waveforms of the DL//S AC-LED driver. (a) Steady state operation during three switching periods. (b) Zoom toward the turn-off of the LED load to study the reverse recovery effect.

output, the luminance over time has been measured with a high bandwidth photodiode (i.e., S5972) used in conjunction with a transimpedance amplifier [4.17]. In that respect, the green waveform, represents the voltage measured by the transimpedance amplifier, $v_L(t)$, which coincides with the current supplied to the LED load. However, in terms of the light, the behaviour seen is not ideal and there is a longer fade out period than expected, which happens due to the several activations caused by the ringing. The effect cannot be correctly measured by the photodiode due to the high frequency of the ringing (i.e. 24 MHz) that exceeds the bandwidth of the photodiode. Nonetheless, this effect is not significant in terms of light, but it is in terms of losses, as the LED load undergoes an increase of more than 15ºC when compared with a conventional dc-dc boost converter feeding the same LED load. The temperature increase is the main reason why the ZCS-QRC AC-LED drivers have been proposed to diminish the undesirable effect of the reverse recovery.

The objective of this section is to summarize the most important experimental results for both QRC-ZCS AC-LED drivers under study, which have been designed and experimentally tested for a maximum power of 7.5 W, feeding the aforementioned LED load for the DL//S ZCS-QRC AC-LED driver and an LED load comprised of two parallelized strings of 4 LEDs in series for the DL//L ZCS-QRC AC-LED driver. Fig. 4.12, shows a picture if a DL//S ZCS-QRC AC-LED driver with its LED load and their size measured in cm. The other designed LED drivers, for the rest of the chapter, will follow a very similar pattern, ensuring the same measurements as the ones depicted in Fig. 4.12 (a).



(a) *(b)*

Fig. 4.12. Constructed prototypes. (a) DL//S ZCS-QRC AC-LED driver. (b) LED load based on the recommended design for the Lumiled LXML-PWC2.

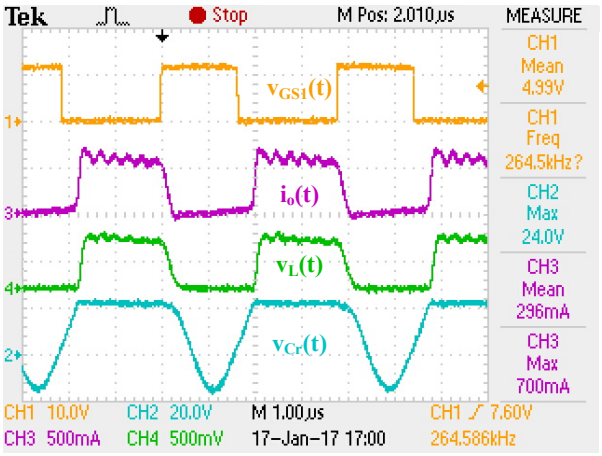
4.3.1 Steady state operation of the DL//S ZCS-QRC AC-LED driver

The specific design for the DL//S ZCS-QRC AC-LED driver has been carried out following the design criteria introduced in Section 4.2.3 for an input voltage of 12 V, feeding an LED load equivalent to 24 V and 300 mA. Furthermore, Table 4.3 summarizes the values selected for the design, which have been selected to completely eliminate the reverse recovery effect while achieving ZCS on Q_1. As regards the switching frequency, it has been selected in the range between 235 kHz and 265 kHz, taking into account that the lowest switching frequency happens at full dimming and the highest switching frequency at full load (i.e., the highest the switching frequency the highest the effective duty cycle on the AC-LED driver).

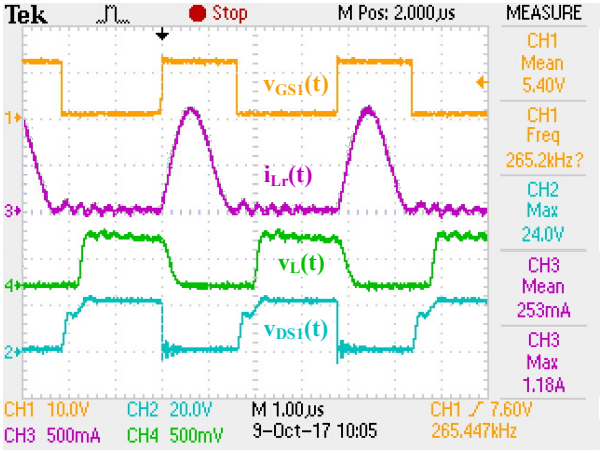
Fig. 4.13 (a) depicts a snapshot of the oscilloscope showing the most representative waveforms from the point of view of the LED load, being $i_o(t)$ the current across them, $v_{Cr}(t)$ the voltage withstood by them and $v_L(t)$ their emitted luminance, with $v_{GS1}(t)$ as a reference. As can be seen, the DL//S ZCS-QRC AC-LED driver does not show any reverse recovery effect, which matches correctly $i_o(t)$ with the emitted luminance. In addition, Fig. 4.13 (b) is used to show the correct achievement of ZCS on Q_1 by showing both the resonant current, $i_{Lr}(t)$, and the voltage withstood by Q_1. In summary, Fig. 4.13 correctly exemplifies the operation of the DL//S ZCS-QRC AC-LED driver in accordance to the mathematical analysis of Subsection 4.2.1.

Table 4.3. Components of the experimental prototype of the DL//S ZCS-QRC AC-LED driver.

Fig. 4.3 (a) reference	Value
L_1	220 µH – N49 – RM8
L_r	10 µH
C_r	10 nF
Q_1	FDMS86105



(a)



(b)

Fig. 4.13. Most representative waveforms of the DL//S ZCS-QRC AC-LED driver. (a) Output current, light and reference waveforms. (b) Resonant current, drain-source voltage of Q_1 and reference waveforms.

4.3.2 Steady state operation of the DL//L ZCS-QRC AC-LED driver

In a similar fashion, a prototype of the DL//L ZCS-QRC AC-LED driver has been designed in order to eliminate the reverse recovery effect while achieving ZCS. Then, by fulfilling the design requirements the value of its components have been obtained and summarized in Table 4.4 for an input voltage of 24 V feeding two strings of 4 LEDs that are equivalent to 12 V and 600 mA at full load.

Table 4.4. Components of the experimental prototype of the DL//L ZCS-QRC.

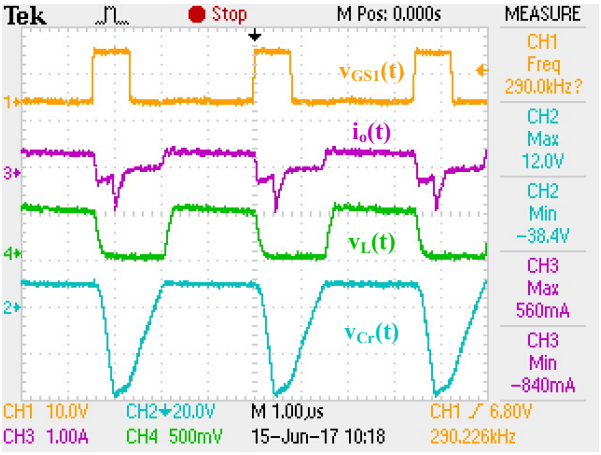
Fig. 4.6 (a) reference	Value
L_1	400 µH – N49 – RM8
L_r	4.7 µH
C_r	6.8 nF
Q_1	FDMS86105

Once again, the next step is validating its operation by analyzing the waveforms attained from the oscilloscope. Fig. 4.14, shows the most representative waveforms for the DL//L ZCS-QRC AC-LED driver. As can be seen, Fig. 4.14 (a), shows the waveforms related to the LED load as are: $i_o(t)$, $v_L(t)$ and $v_{Cr}(t)$. Particularly, $i_o(t)$ presents an undesired negative current peak in the middle of the duration of the turn-off due to the high reverse voltage withstood by the LED load, that causes the LED to start conducting inversely. Although this current peak does not have any impact on the emitted light, as can be seen on $v_L(t)$, it heavily decreases both the lifetime and the luminous efficacy of the LEDs. This conclusion can be extracted from a test over time that has been carried out for the DL//L ZCS-QRC AC-LED driver, in order to observe the implications of applying negative voltages to the LED load, whcih severely surpass the limits set by the manufacturer, and whose results are depicted in Fig. 4.15. As can be seen, in the span of an hour the LED load is rendered useless.

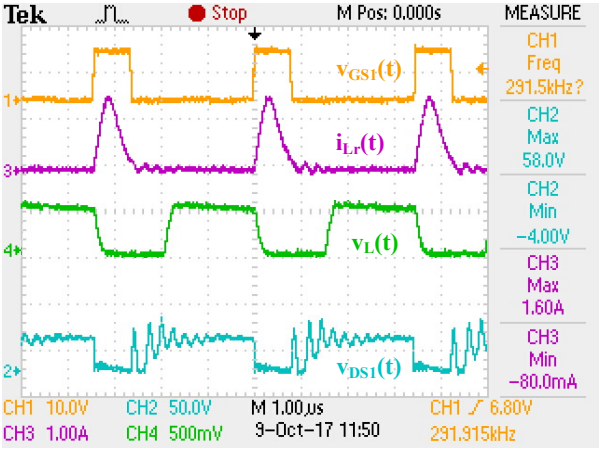
Furthermore, this undesired current peak, implies that the DL//L ZCS-QRC AC-LED driver is unable to achieve ZCS on Q_1, as during that time the driver goes into another stage that has not been analyzed in the theoretical analysis as it should not exist. In fact, this limitation cannot be simply overcome without adding more components to the circuit, which will further hinder the efficiency of the driver. Therefore, the DL//L ZCS-QRC AC-LED driver is discarded for LED driving, unless LEDs with higher blocking reverse voltage blocking capabilities are available, considering that its use is not feasible with current LED technology.

4.3.3 Control strategy

The last part of this chapter will include a reliability test between different LED drivers to understand the implications of high-frequency AC-LED driving or whether the reverse recovery effect impacts the lifetime of the LEDs. For that matter, and in order to ensure a proper test scenario, it is necessary to control the average current across the LED load or the light output [4.25].



(a)



(b)

Fig. 4.14. Most representative waveforms of the DL//L ZCS-QRC AC-LED driver. (a) Output current, light and reference waveforms. (b) Resonant current, drain-source voltage of Q_1 and reference waveforms.

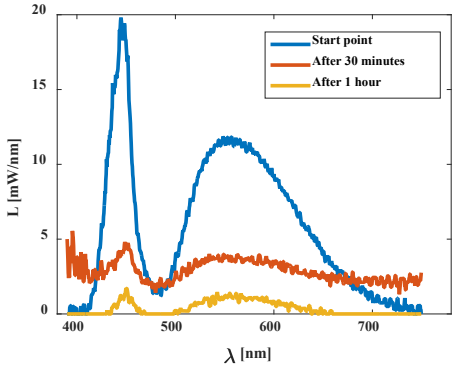


Fig. 4.15. Luminance versus wavelength in the visible spectrum for different time instants DL//L ZCS-QRC AC-LED driver.

The solution to control the proposed ZCS-QRC AC-LED drivers needs to be simple and cost efficient, as otherwise it will not be suitable for the application. Therefore, a commercial analog Integrated Circuit (IC) capable of switching up to 1 MHz is going to be used (i.e., MC33023). However, unlike a conventional dc-dc converter or the presented AC-LED converters, the ZCS-QRC AC-LED drivers require for their switching frequency to be controlled in order to regulate $i_o(t)$. Previous works have tackled this topic on ZCS-QRCs, by adding a simple external circuit to commercial ICs in order to have a constant on time while controlling the duration of the off-time [4.26], [4.27].

Fig. 4.16, shows the proposed circuitry to control the off-time, particularized for the MC33023, which is equivalent to the renowned UC3823 [4.28]. The idea is based on taking advantage of how the ramp is generated in most commercial ICs. In that respect, an external capacitor (i.e., C_T) and an external resistance (i.e., R_T) are used in conjunction to generate the ramp as the current across the resistance is the one used to charge the capacitor until it reaches a certain voltage, point after which C_T will start discharging in accordance to a current sink defined by the NPN Bipolar Junction Transistor (BJT) internally connected to pin 6, Q_2. It should be noted that t_{on} and t_{off} will be defined after the comparison of the ramp with a certain voltage, traditionally set by the outer voltage loop. However, for this scenario, this voltage is set to its admissible maximum, forcing the charging time of C_T to be defined as t_{on}, and the discharge as t_{off}. Thus, with an adequate selection of C_T and R_T, it is possible to attain a driving signal for Q_1 with the desired switching frequency and t_{on} duration.

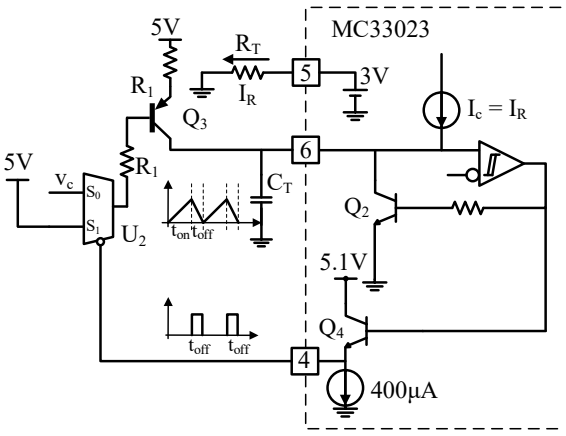


Fig. 4.16. Diagram of the external circuitry to control the off-time in ZCS-QRC AC-LED drivers.

Even though, this driving signal has a fixed frequency, it is possible to attain a variable t_{off} with the external circuitry depicted in Fig. 4.16 (i.e., Q_3 and U_2). The idea is using a PNP BJT operating in the linear region as a controllable current source. This achievement, is the cornerstone to control the discharge of C_T and thus t_{off}. However, Q_3 needs to operate as a current source only during t_{off}. For that matter, the analog multiplexer, U_2, is added to the circuit to be responsible for switching Q_3 between the cut-off region and the linear region by selecting between the two voltages at its input. This selection is performed on U_2 thanks to the signal generated by the IC on its fourth pin that sets its value to high whenever the ramp reaches its maximum voltage threshold, and goes back

to low when it reaches its minimum threshold, coinciding with t_{off}. Then, by controlling v_c, it is possible to vary the switching frequency to control the ZCS-QRC AC-LED drivers.

The aforementioned control circuitry has been validated in open loop by controlling the driver switching frequency with an external power supply assuring that i_{in} and i_o follow the relationship introduced in both (4.29) and (4.51) for the whole range of operation. It is important to note, that in the ZCS-QRC AC-LED drivers the LEDs are dimmed by varying the switching frequency of the converters. At the same time the converter demands less power causing the input current to decrease, which in the end causes the peak current across the LEDs to diminish. This behaviour can be observer in Fig. 4.17 for a DL//S ZCS-QRC AC-LED driver operating at different dimming conditions. This figure, has been obtained by extracting from the oscilloscope the different measurements and plotting them all together to be able to compare them. This implies that there are two degrees of freedom in order to control the ZCS-QRC AC-LED drivers, however, in the case of study the input current is completely reliant on the switching frequency, so only the switching frequency is required to be controlled.

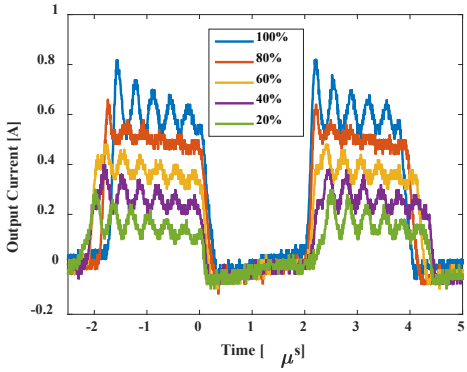


Fig. 4.17. Current across the LEDs on the DL//S ZCS-QRC AC-LED driver for different dimming points.

In order to study the design of the compensator, the open loop gain of the DL//S ZCS-QRC AC-LED driver has been measured by means of a Venable® 6320 frequency analyzer, see Fig. 4.18. The objective is to attain the real response between v_c and i_o, taking into consideration the dynamics of the t_{off} control circuitry and the low pass filter (i.e., LP Filter) used to attain the average value of $i_o(t)$, which is also scaled by a certain factor, ζ. It should be noted that for better results, a voltage follower is introduced between the Venable generator and the circuit to achieve a high impedance interface less intrusive for the operation of the DL//S ZCS-QRC AC-LED driver.

The results of this measurements are summarized in Fig. 4.19 for four different load points (i.e., 100%, 80%, 50% and 20% of the maximum load), where it can be observed that the most restrictive condition is set at full load. Hence, a compensator been designed to ensure stability for all the range of operation with a crossover frequency of 10 kHz, a gain margin of 22.5 dB and a phase margin of 62º.

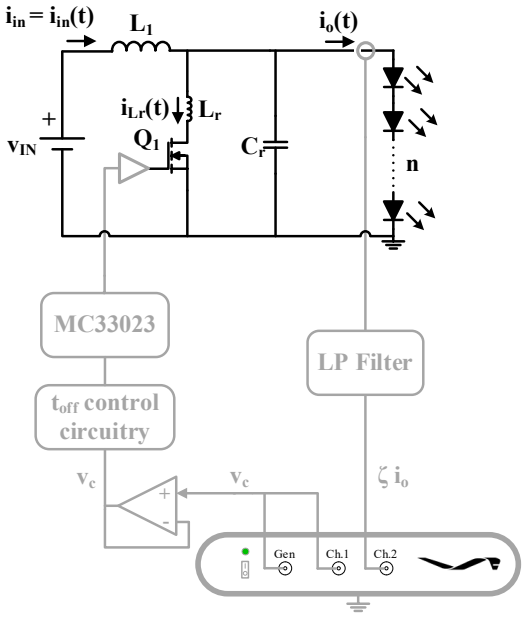


Fig. 4.18. Measuring setup for the open loop response relating v_c and i_o on the DL//S ZCS-QRC AC-LED driver, based on a Venable® 6320 frequency analyzer.

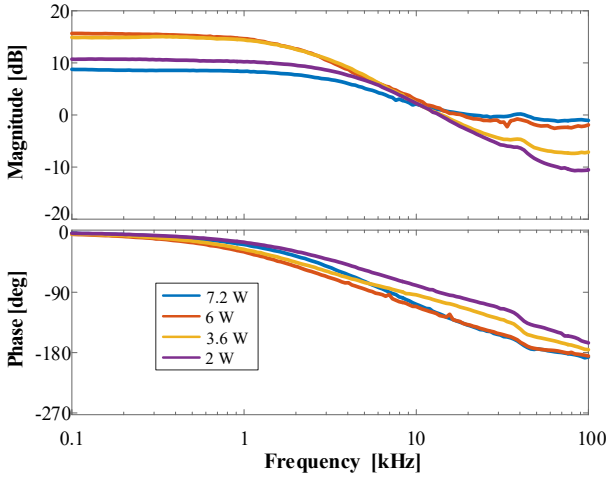


Fig. 4.19. Open loop gain of the DL//S ZCS-QRC AC-LED driver for different dimming conditions.

4.3.4 Comparison and reliability testing

After having experimentally validated the closed loop operation of the DL//S ZCS-QRC AC-LED driver, four prototypes have been built with the same specifications and components, setting two of them at full load conditions and the other two at half load. The idea is to study their operation over a long period of time while measuring the luminous efficacy, which will be measured in lm/W taking into account the losses of the control circuitry, and the CCT. The latter is calculated from McCamy's formula [4.29] after obtaining the (x, y) coordinates in accordance to the CIE 1931 standard from the spectral power distribution of the light emitted by the LEDs [4.30], [4.31].

At the same time four prototypes of a conventional boost dc-dc converter and another four of a DL//S AC-LED driver, feeding each the same LED load have been built in order to compare them with the DL//S ZCS-QRC AC-LED driver and to study the implications of the reverse recovery of the LEDs on their lifetime. The design has been done following the same specifications and keeping the same components when possible. It should be noted that for the conventional dc-dc boost LED driver an additional power diode and an output capacitor of 10 µF will be used. The electrical efficiency of these three different LED drivers will not be compared, as the luminous efficacy makes for a fairer comparison, taking into account that it becomes a challenge to accurately measure the electrical efficiency of the current though the LED load which is pulsating at high frequencies.

The test has been carried out by using an integrating sphere, see Fig. 4.20, in conjunction with a spectrophotocolorimeter from LabSphere Inc. Before starting the reliability testing, the three LED different LED drivers have been measured in terms of their luminous efficacy and CCT. The results are compared and shown in Fig. 4.21, where they have been normalized at the value taken at the point of maximum output current for each of the drivers in order to be able to compare their tendencies. Otherwise, the disparity of the values would make this comparison to be impossible. As can be seen in Fig. 4.21

Fig. 4.20. Integrating sphere and spectrophotocolorimeter from LabSphere Inc. used for the luminous efficacy and CCT measurements.

(a) the DL//S ZCS-QRC AC-LED driver presents the least variation in terms of luminous efficacy for the different dimming conditions. However, the differences are not significant for any of the LED drivers. As regards CCT, Fig. 4.21 (b), shows that the least variation happens for the conventional dc-dc boost converter, however, there are not significant difference either.

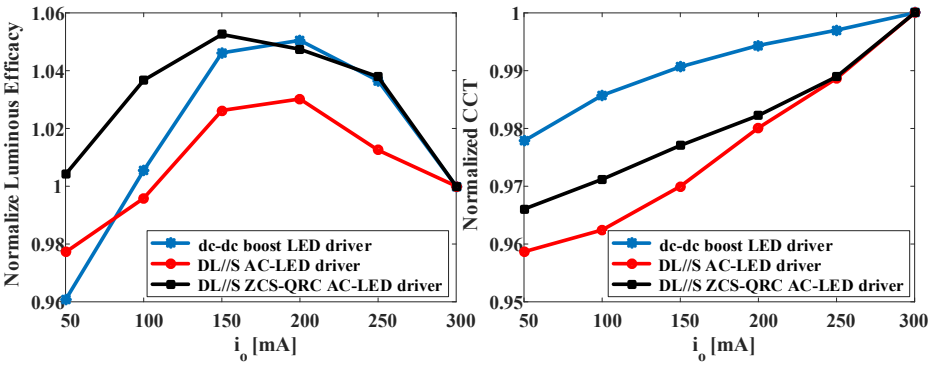


Fig. 4.21. Initial measurements for the three LED drivers under study. (a) Normalized luminous efficacy vs i_o.(b) Normalized CCT vs i_o.

After having compared and checked the operation of all twelve prototypes, the next step is leaving them operating uninterruptedly for 700 h. Nonetheless, in order to ensure a correct operation, their temperature has been monitored along the 700 h in order to avoid bad samples or misbehaviours. Fig. 4.22 shows the LED driver temperature, after several operating hours and in steady state. As can be seen there is a significant difference between the DL//S AC-LED driver and the other two drivers in terms of temperature, which can only be explained due to the reverse recovery effect. However, this temperature increase should not directly impact the LEDs as they are far from the temperatures that could cause significant damage to their luminous efficacy.

Then, the LED drivers were measured every 175 h in the integrating sphere in order to see the pattern of degradation over time if any, and to check if they were operating correctly. The results of these measurements are summarized for the two load points of study in Fig. 4.23 and Fig. 4.24. As can be seen in Fig. 4.23, the luminous efficacy of the DL//S AC-LED driver plummets becoming irreversibly less efficient than the DL//S ZCS-QRC AC-LED driver in roughly 600 h due to the reverse recovery effect. In fact, taking into consideration this is quite a short time, considering the lifetime of the LEDs, the DL//S AC-LED driver is a topology to be avoided unless aiming for cheap solutions with low specifications. In addition, the dc-dc boost LED driver, which presents a much higher luminance efficacy than the other solutions, degrades faster than the DL//S ZCS-QRC AC-LED driver, fact that has been proved in other studies that compared dc and pulsed LED current driving [4.13]. And, even though, the difference is not as high as for the DL//S AC-LED driver, this fact can arguably make the DL//S ZCS-QRC AC-LED driver a solution able to achieve longer lifespans at the cost of a lower luminous efficacy.

It should also be noted that at higher currents the drivers degrade with a higher ratio, however, this is not noticeable over the period of time that was studied. As regards, the difference in luminous efficacy between the DL//S AC-LED driver and the DL//S

ZCS-QRC AC-LED driver, it can be explained due to the extra components required for closed feedback loop operation (i.e., extra control circuitry, see Fig. 4.16), which as can be seen in Fig. 4.22 (a) present the maximum temperature of the prototype.

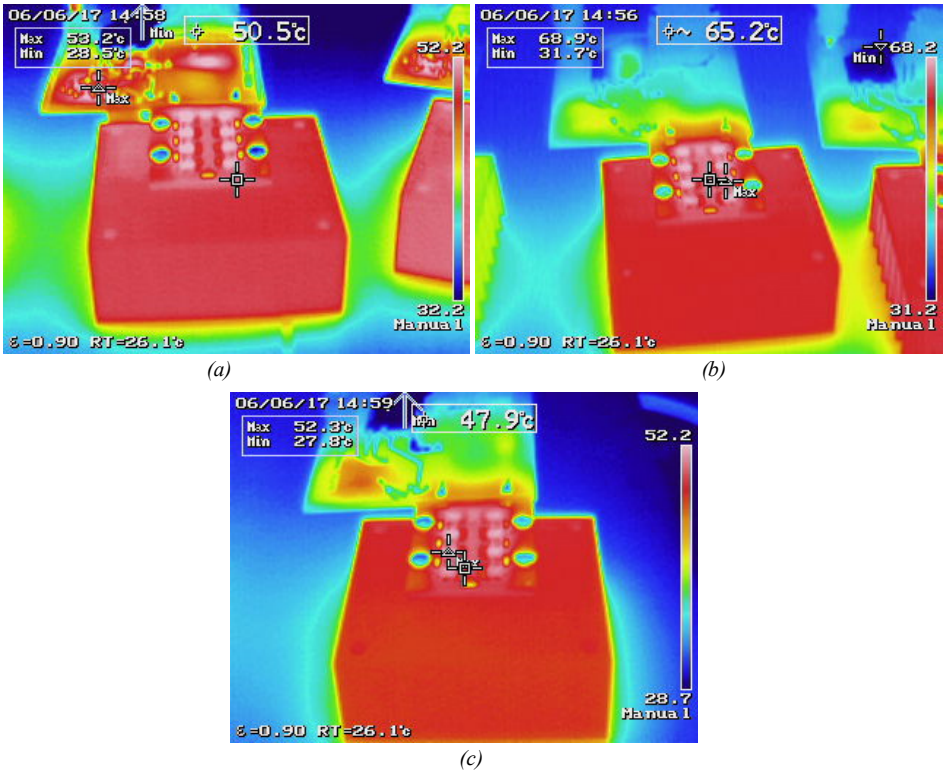


Fig. 4.22. Temperature in steady state for the three LED drivers under study. (a) DL//S ZCS-QRC AC-LED driver. (b) DL//S AC-LED driver and (c) dc-dc boost LED driver.

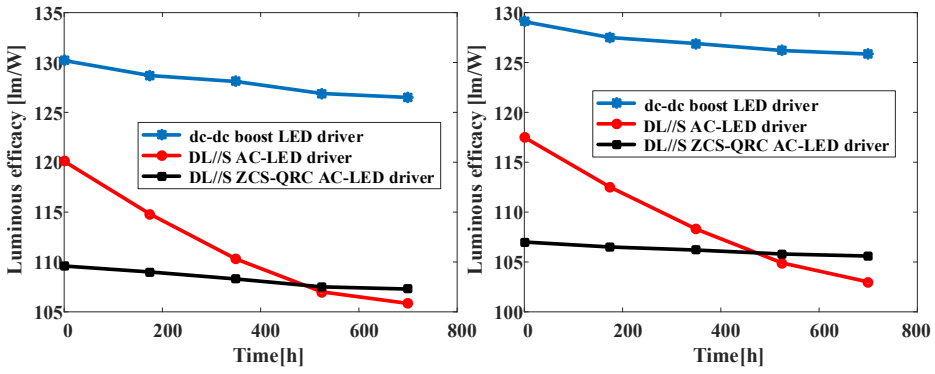


Fig. 4.23. Measurements of luminous efficacy over time for the three LED drivers under study. (a) At half load. (b) At full load.

Finally, Fig. 4.24, shows that there is no significant variation in terms of CCT over time for any of the LED drivers under study, considering the two different load conditions and taking into account that these differences are within the range of the tolerances of the LED.

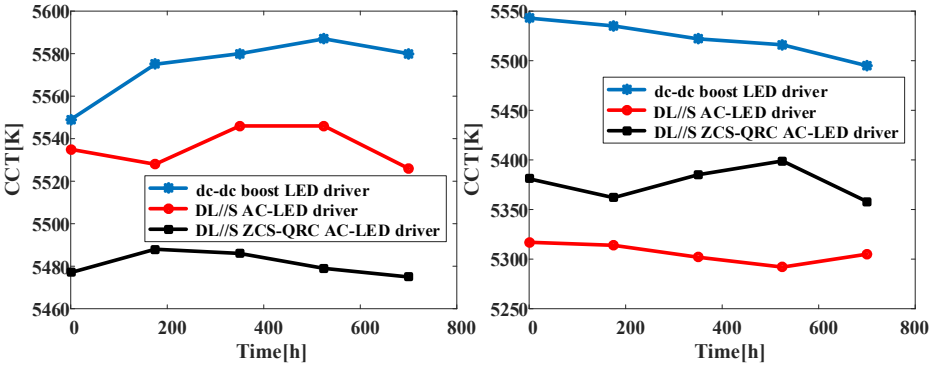


Fig. 4.24. Measurements of CCT over time for the three LED drivers under study. (a) At half load. (b) At full load.

4.4 Conclusions

This chapter proposes the use of LEDs as the rectifier diode and load in conventional dc-dc converters. However simple this statement seems to be, discerning the feasibility of using LEDs under such conditions is not due to the lack of information in the manufacturer datasheets. For that matter, the switching performance was carefully studied along with a reliability test, concluding that:

- LEDs are able to switch at high frequencies up to 2 MHz.
- LEDs present a huge reverse recovery peak under the aforementioned operation, which decreases their luminous efficacy over a short period of time, and thus their lifetime.

A method to remove the reverse recovery effect on the LED load has been discussed by means of using a full-wave resonant switch, yielding two LED drivers that receive a dc voltage at their input and drive the LEDs with pulsated currents: the DL//S ZCS-QRC and DL//L ZCS-QRC AC-LED driver. In accordance to the mathematical analysis carried out, it is possible to control the di/dt during the turn-off of the LEDs and achieve ZCS on the main switch. It is this control of the di/dt during the turn-off which allows the elimination of the reverse recovery effect.

Both topologies were built and experimentally tested, observing that the DL//L ZCS-QRC AC-LED driver is unable to operate as studied due to the high reverse voltage that the LEDs need to withstand, which causes the topology not only to misbehave but to dramatically reduce the lifetime of the LEDs, as they start conducting inversely. In that respect, this topology is discarded unless newer technologies of LEDs able to withstand those voltages are manufactured.

As regards the DL//S ZCS-QRC AC-LED driver, its experimental performance correctly corresponds to the mathematical analysis carried out achieving the removal of the reverse recovery effect and ZCS on the main switch. In addition, it achieves full dimming conditions under output current feedback loop operation with a simple control method that varies the switching frequency of the LED driver. This control method requires a PNP BJT to be added to the circuit working in the linear region as a current source and an analog multiplexer that switches the PNP BJT between the cut-off and the linear region, in order to keep a constant on-time while varying the off-time.

Furthermore, the DL//S ZCS-QRC AC-LED driver has been studied and compared to a conventional dc-dc boost LED driver in a reliability test, showing that even though its luminous efficacy is lower, it is able to achieve higher lifespans. Nonetheless, the difference in luminous efficacy can be understood due to:

- the dc driving of LEDs being more efficient than pulsed driving.
- the losses introduced by the extra components required for the control of its off-time.
- the high RMS current across the resonant inductor, L_r.

In summary, the DL//S ZCS-QRC AC-LED driver shows several advantages that makes it prone to be operated as a post-regulator stage in spite of the traditional dc-dc boost LED driver:

- better performance in terms of lifetime.
- removal of the rectifier diode.
- size reduction of the output capacitor, as it is changed for the resonant capacitor, C_r.
- ability to reach high switching frequencies due to the achievement of ZCS on the main switch.

Nevertheless, it presents several disadvantages in comparison:

- lower initial luminous efficacy.
- variable switching frequency.
- higher RMS current across the main switch, Q_1, and the resonant inductor, L_r.
- increased complexity of the control circuitry.

4.5 References

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5

Conclusions

And once the storm is over, you will not remember how you made it through, how you managed to survive. You will not even be sure, whether the storm is really over. But one thing is certain, when you come out of the storm, you will not be the same person who walked in.

— Umibe no Kafuka, Murakami Haruki.

The present chapter discusses the most important conclusions that can be extracted from this dissertation, emphasizing its original contributions to power electronics in the topic of LED driving. In addition, the discussion is extended to some research topics, which can be further studied to continue the work developed throughout this dissertation.

5.1 Conclusions and contributions

The present dissertation has investigated the development of more efficient power topologies to drive high power LED loads of more than a 100 W in ac power grids complying with the most important regulations and norms defined for this specific application. For that matter, and after carefully considering the current literature, summarized in Chapter 1, the focus has been put on the study of three-phase multi-cell ac-dc LED drivers based on a modular approach in order to demonstrate whether these solutions could improve those proposed in the state-of-the-art. In addition, the study was extended to a more conventional approach, evaluating single-phase ac-dc LED drivers based on using current-fed topologies that could potentially provide isolation and high efficiencies with a single-stage. The previous approaches focus on controlling a high amount of LED strings at the same time taking into consideration an ideal current sharing between the strings that could potentially comprise the LED load. However, in some cases that require a high performance, a post-regulator stage is required per string to ensure an adequate current sharing between them. In that sense, a post-regulator stage has also been proposed using a pulsed current through the LEDs and aiming to reduce its cost while improving its performance over the more conventional approaches. These three different scenarios summarize the topics in which this dissertation has made its contributions which are further detailed throughout this chapter.

Firstly, in Chapter 2, the concept of intrinsically removing the electrolytic capacitor in a three-phase ac-dc LED driver has been analyzed and obtained under certain conditions: the current demanded by all three-phases needs to achieve unity PF and the input power of each phase needs to be fed to the same load. The removal of this component has proved to be critical to improve the lifetime of ac-dc LED drivers and is one of the main topics in the current literature. For that matter, this chapter has analyzed the Delco topology in Section 2.2 with the aim of achieving a simple and efficient ac-dc LED driver able to operate under full dimming conditions by using as the cells of the ac-dc LED driver converters behaving as an LFR. Following the LFR concept, a three-phase ac-dc topology has been proposed based on the full-wave three-phase rectifier. In fact, taking into consideration the similarity with the Delco LED driver, as they both reach the exact same equivalent circuit, they have been compared experimentally using flyback converters operating as LFRs. This comparison concludes that:

- both topologies can be used as ac-dc LED drivers, achieving full dimming, and complying with the most restrictive of regulations.
- the efficiency of the full-wave three-phase ac-dc LED driver is higher than the Delco, in spite of its power density.
- the higher amount of components required for the full-wave three-phase ac-dc LED driver does not justify its use for the lower power range of LED luminaires.
- the efficiency is completely reliant on the selected topology used to defined the cell.

In fact, this last statement introduced the study of a Delco topology based on more efficient cells, which was carried out in Section 2.6 using the traditional two-stage solutions used in single-phase ac-dc converters, proposing a control method that guarantees the full removal of the electrolytic capacitor. However, this two-stage Delco ac-dc LED driver presented two important drawbacks:

- a high cost due to the amount of components used, taking into consideration not only the power stage but all the control required for the system.
- the efficiency at full load which is greatly improved over the previous flyback cells, still presents a poor performance under dimming conditions, which are attributed to the operation of the second stage of each cell. It should be noted that this performance greatly depends on the selected isolated dc-dc converter used for the second stage.

Keeping in mind these drawbacks, the last solution proposed in Section 2.4 is the complete removal of the second stage. However, to ensure a constant and conventional driving of the LED load, an electrolytic capacitor is required. Thus, a study is carried out to drive the LED loads with low frequency pulsating current while guaranteeing a constant light output. This is only possible by taking advantage of one of the light properties that allows for the light output of each phase to be blended. This method is further validated with experimental results by means of PFC boost cells measuring the light output at a fixed distance. Even though, this method does not provide galvanic isolation, it presents higher efficiencies, even under dimming conditions, with a low

component count. Its main drawback is that it requires for the LED loads to be positions adequately in order to assure that the light output is rendered constant.

In the aim of achieving more efficient single-stage single-phase ac-dc LED drivers which could be used standalone in a single-phase ac power grid or as part of a multi-cell ac-dc LED driver. Chapter 3, evaluates the use of current-fed topologies as ac-dc converters. The conventional limitations of these topologies have prevented them from achieving the required performance for an ac-dc LED driver, however the proposed dual inductor current-fed push-pull is able to overcome those limitations due to its simpler transformer design. In addition, due to the interleaving that occurs intrinsically between its two inductors, it is able to obtain a reduced input current ripple in comparison to other topologies. The static analysis of this topology is further detailed in Subsection 3.2.1, which is experimentally validated in Section 3.4.

Although its transformer design is simpler, it still requires a careful design in order to avoid its parasitic inductance and capacitor from affecting the performance of the topology. For that matter, and in order to attain the best performance out of this ac-dc LED driver, the design requirements and procedure is proposed along Subsections 3.2.2 and 3.2.3.

The aforementioned statements cover the design of the power stage, but special focus is put in the proposed control of the topology, which is summarized in Section 3.3. In fact, the significant characteristic of this control is that only a single isolated measurement is necessary, being able to control both the current across the LED load and perform the required control for BCM operation sensing the current after the high frequency diode bridge. Furthermore, the small-signal analysis is performed and experimentally validated. The prototype built has shown outstanding characteristics that compares it with the most efficient isolated single-stage single-phase ac-dc LED drivers, at the cost of requiring a demagnetization circuit for its both inductors to prevent the destruction of its switches in case of a malfunctioning event, using variable frequency and requiring switches with higher breakdown voltages in comparison to other topologies to operate in European input voltage range.

The previous chapters focused on the development of ac-dc LED drivers. In contrast, Chapter 4, proposes the improvement of the post-regulator stage used in single-phase multi-stage ac-dc LED drivers. The idea is based on using the LED load as the rectifier of conventional dc-dc converters aiming to reduce the cost of this topology by removing the rectifier diode and the output capacitor. In these topologies the LEDs operate with pulse current, yielding an AC-LED driver. However, present white LEDs available on the market are not prepared for this operation switching at high frequencies and show a significant reverse recovery effect. For that matter, the proposal is to use a full-wave quasi-resonant switch yielding the ZCS-QRC AC-LED drivers. These AC-LED drivers are able to remove the reverse recovery effect in accordance to the proposed theoretical analysis and the proposed design criteria introduced in Section 4.2.

Moreover, this chapter validates experimentally the operation of the DL//S ZCS-QRC AC-LED driver, unfortunately due to the reverse conduction limitation of white LEDs the DL//L ZCS-QRC AC-LED driver is not a feasible solution at the present time. The DL//S ZCS-QRC AC-LED driver is further compared with a DL//S AC-LED driver and a dc-dc boost LED driver over a 700 h reliability test along Section 4.4. During this test

the DL//S AC-LED driver luminous efficacy plummeted due to the reverse recovery effect, discarding this topology. As regards the DL//S ZCS-QRC AC-LED driver it shows some advantages over the conventional dc-dc boost LED driver:

- better performance in terms of lifetime.
- removal of the rectifier diode.
- size reduction of the output capacitor.
- ability to achieve higher frequencies due to the achievement of soft-switching on the main switch.

Summarizing, this dissertation has presented several power topologies to be used as LED drivers in order to improve the performance of those proposed in the state-of-the-art while complying with the most restrictive regulations.

5.2 Outlook

Future research on the proposed LED drivers can be performed with special focus on their optimization, which is the constant pattern in the solutions presented in the latest works available in the state-of-the-art. For that matter, the optimization can be performed either in terms of the efficiency of the power stage or by developing better control methodologies.

5.2.1 Multi-cell three-phase ac-dc LED drivers

As regards the analysis of three-phase ac-dc LED drivers, the optimization of the cell is key to attain more efficient solutions aiming to achieve higher power densities. This optimization can be done studying whether a single-stage or a two stage approach for the cell is the most optimal for the application. Particularly emphasizing:

- the use of bridgeless PFC converters, that will further increase the efficiency by removing the lousy low frequency diodes in all converters.
- the use of resonant dc-dc isolated converters with optimized efficiencies keeping the efficiency high even at low loads by extending the operation range of the soft-switching techniques applied to the switches.
- the study of the optimal amount of cells required. This means serializing or parallelizing cells taking into consideration the voltage and current range of the semiconductors.

Furthermore, there are some improvements that can be performed to the control of multi-cell ac-dc LED drivers which will not exclude those performed for the power stage, as are the addition of:

- a feedback loop at the input that ensures that each cell demands the same amount of power, can contribute to reduce the six times the mains frequency ripple at the output. This improvement can further diminish the size of the output capacitor.

- a balancing feedback loop at the input of the multi-cell converter can also help deal with undesired voltage spikes on the three-phase power grid that can cause current changes on the LED load.

5.2.2 Single-phase single-stage current-fed ac-dc LED driver: DICPP

The dual inductor current-fed push-pull presented several characteristics that made the converter comparable with the most efficient solutions currently proposed in the state-of-the-art for single-phase ac-dc LED drivers. However, the designed converter was not optimized in terms of either size or losses. In that regard, future work can look into:

- further studying the design of magnetic components. As has been seen in the distribution of losses, the magnetic components contributed to half of the losses of the DICPP ac-dc LED driver. For this reason, the use of CCM equivalent current across each of the inductances can reduce the losses due to the lower RMS of the current across them. This operation can be easily performed by controlling the DICPP ac-dc LED driver with a MBC.

- studying the design of EMI filters and compare them in terms of size with other state-of-the-art topologies, considering the compliance with limits set by the EMI lighting regulation (i.e., EN 55015:2013).

In addition, and taking into account the possibility of making a bridgeless variation of this ac-dc LED driver, its efficiency can be further improved using truly bi-directional switches able to block in both directions when they are turned-off, while keeping the same operation discussed along Chapter 3. Continuing the discussion on the selected semiconductors, it is also possible to study the development of a universal voltage range DICPP ac-dc LED driver using switches able to block 1.2 kV taking into account the design criteria introduced in (3.18).

As regards the removal of the electrolytic capacitor, any of the several methods discussed in Chapter 1 can contribute to perform this feat, rendering a highly efficient, quasi-single-stage, current-fed, ac-dc LED driver.

5.2.3 High-frequency AC-LED drivers based on ZCS-QRCs

Chapter 4, discussed the use of LEDs as the rectifier diode of conventional dc-dc converters. The proposed future work for the AC-LED drivers can be summarized into two different points:

- The further study of high-frequency AC-LED drivers operating in DCM or BCM and achieving the removal of the reverse recovery effect that made their luminous efficacy to plummet over time, thanks to the reduced di/dt during the turn-off of the LEDs. Under this scenario, the LEDs will be driven by a triangular pulsating waveform. This operation requires to be studied in detail and will need to undergo a similar reliability analysis to the one performed in Chapter 4.

- The study of the dynamic analysis of the ZCS-QRC AC-LED drivers. The closed loop operation of the drivers was developed after measuring the frequency response with a frequency analyzer. For that matter, a mathematical analysis is required to obtain the small-signal analysis that can help designing the proposed

AC-LED drivers. For the sake of completion, the aforementioned analysis will need to be experimentally validated.

5.3 Funding

This disseration has been supported mainly by the Principality of Asturias under Severo Ochoa grant BP14-140. The rest of the support has been granted in part by the Spanish Government under Projects MINECO13-DPI2013-47176-C2-2-R and MINECO-17-DPI2016-75760-R, the Principality of Asturias under Project FC-15-GRUPIN14-143, and in part by the European Regional Development Fund grant.

5

Conclusiones

El presente capítulo presenta las conclusiones más importantes que han sido obtenidas de este trabajo de Tesis, poniendo especial énfasis en las contribuciones originales a la electrónica de potencia en la temática de los drivers de LED. Además, este capítulo también aborda aquellos trabajos futuros que pueden ser retomados como continuación de esta Tesis.

5.1 Conclusiones y contribuciones

Esta Tesis se ha encargado de investigar el desarrollo de nuevas topologías de potencia más eficientes en el ámbito de la alimentación de cargas de LEDs de alta potencia de más de 100 W, y cuyo objetivo es la conexión a la red de distribución de corriente alterna. En su diseño se ha tenido en cuenta que estas topologías cumplan con las regulaciones y normativas más importantes, y que a la par son de necesario cumplimiento para este tipo de equipos. Por este motivo, y después de haber estudiado el estado del arte en el Capítulo 1, se ha enfatizado el estudio de los *drivers* de LED ca-cc trifásicos multi-celda que están basados en una topología modular con el objetivo de mejorar los resultados de aquellos propuestos en el estado del arte. A continuación, el análisis topológico fue extendido a los *drivers* de LED ca-cc monofásicos mediante el uso de topologías alimentadas en corriente aisladas galvánicamente, que puedan alcanzar un alto rendimiento. Estos dos estudios se centran en el control de un número elevado de cadenas de LEDs al mismo tiempo, considerando un reparto de corrientes ideal entre todos los LED que conforman la carga. Sin embargo, en aquellos casos en los que se requiera un alto rendimiento y mayor control de la corriente a través de cada una de las cadenas de LED, una etapa post-reguladora es necesaria por cada una de las cadenas de LEDs para asegurar un reparto adecuado de la corriente. En ese sentido, se propone un post-regulador mediante el uso de una corriente pulsada de alta frecuencia a través de la cadena de LEDs y con el objetivo de reducir el coste y mejorar el rendimiento en comparación con aquellas topologías más tradicionales. Las tres propuestas descritas, resumen las temáticas en las que la presente Tesis ha realizado sus contribuciones, y que son detallados a lo largo de este capítulo.

En primer lugar, el Capítulo 2 parte del concepto de eliminar el condensador electrolítico de manera natural en los *drivers* de LEDs ca-cc trifásicos. La eliminación de

este componente se puede llevar a cabo siempre y cuando se cumplan dos condiciones: la corriente demandada por todas las fases debe alcanzar Factor de Potencia (FP) unidad y la potencia de entrada de cada una de las fases debe ser entregada a la misma carga de LEDs. De hecho, la eliminación del condensador electrolítico es un aspecto crítico cuando se quiere obtener un *driver* de LEDs con una larga vida útil. Por este motivo, este capítulo analiza la topología de Delco en la Sección 2.2 con el objetivo de proponer un *driver* de LEDs simple y eficiente, que además sea capaz de trabajar en condiciones de atenuación total o *dimming* total en su terminología anglosajona. Como celdas de esta topología se han utilizado convertidores que se comporten como LFRs. Es más, siguiendo un diseño modular basado en convertidores actuando como LFRs, se presenta también una topología ca-cc trifásica basada en el rectificador trifásico de onda completa. Teniendo en cuenta la similitud con el *driver* de LEDs de Delco, ya que ambos llegan al mismo circuito equivalente, las dos topologías han sido comparadas como *drivers* de LEDs mediante el uso de convertidores flyback a nivel de celda comportándose como LFRs. De esta comparativa se concluye que:

- ambas topologías pueden ser usadas como *drivers* de LEDs conectados a una red de distribución trifásica, alcanzando la correcta operación en condiciones de *dimming* total y cumpliendo incluso las normativas más restrictivas.

- el rendimiento del *driver* de LEDs basado en el rectificador trifásico de onda completa es mayor que el *driver* de LEDs de Delco, sin tener en cuenta su densidad de potencia.

- el mayor número de componentes necesario para el *driver* de LED basado en el rectificador trifásico de onda completa, no justifica su uso para aquellas luminarias LED de menor potencia.

- el rendimiento depende completamente en la topología seleccionada para construir la celda.

Este último punto, es el que lleva al análisis de *driver* de LED de Delco basado en celdas más eficientes que utilizan una doble etapa, tal y como se describió en la Sección 2.6. La metodología de control propuesta también permite en este caso eliminar el condensador electrolítico. Sin embargo, presenta dos desventajas importantes:

- su alto coste debido a la cantidad de componentes utilizados, teniendo también en cuenta la circuitería de control y la etapa de potencia.

- la mejora del rendimiento a plena carga frente al uso de celdas basadas en convertidores flyback, es mejorable debido a su bajo rendimiento en condiciones de *dimming*. Esta caída del rendimiento, ase atribuye al bajo rendimiento de la segunda etapa incluida en cada celda, en condiciones de baja carga.

Estos motivos son los que llevan a la última solución propuesta en la Sección 2.4, y que está basada en la eliminación de la segunda etapa. Sin embargo, asegurar una corriente constante para controlar los LED en una sola etapa implica el uso de un condensador electrolítico. Por lo tanto, se llevó a cabo un estudio para observar como la luz total del *driver* es constante, pese a que pulsa en cada una de las celdas. Esta operación es posible gracias a las características de la luz que permiten que la luz proporcionada por

cada una de las tres fases se sume. Es más, este método es validado experimentalmente mediante el uso de celdas basadas en elevadores con PFC y midiendo la luz total a una distancia determinada. Aunque este método, no proporciona aislamiento galvánico, es capaz de solucionar los problemas de rendimiento a baja carga y mejorarlo, incluso a plena carga. Su principal desventaja es que necesita que las cargas de LEDs de cada una de las celdas estén dispuestas de una manera adecuada para garantizar que la luz se combine obteniendo así una luz constante.

Siguiendo el objetivo de obtener soluciones más eficientes en una sola etapa para *drivers* de LEDs ca-cc monofásicos, que puedan ser utilizados de forma independiente o como parte de un *driver* de LEDs multi-celda, el Capítulo 3 evalúa el uso de topologías alimentadas en corriente como convertidores ca-cc. Las limitaciones de estos convertidores tradicionalmente han evitado que puedan alcanzar altos rendimientos necesarios para *drivers* de LEDs. Sin embargo, la propuesta basada en un *push-pull* de doble inductancia alimentado en corriente es capaz de solucionar estos límites debido al sencillo diseño de su transformador. Además, es capaz de reducir el rizado de alta frecuencia que existe en sus inductancias debido al entrelazado (o *interleaving* en su terminología anglosajona) que ocurre entre ellas. El análisis estático se ha detallado en la Subsección 3.2.1, siendo experimentalmente validado en la Sección 3.4.

Aunque el diseño del transformador es simple, sigue necesitando de un diseño cuidadoso para evitar que las inductancias y condensadores parásitos afecten al rendimiento de la topología. Esta temática se aborda con detalle en los criterios de diseño de las Subsecciones 3.2.2 y 3.2.3.

Las propuestas anteriormente mencionadas, se centran en el diseño de la etapa de potencia, pero también se han realizado aportaciones en el control del *push-pull* de doble inductancia alimentado en corriente, a lo largo de la Sección 3.3 en la propuesta de control para esta topología. De hecho, la principal característica de este control es que solo necesita de una medida aislada que se encarga de controlar que la corriente a través de los LED sea la adecuada, mientras ambas inductancias trabajan en modo de conducción frontera equivalente. Además, un simple análisis de pequeña señal validado experimentalmente, demuestra la sencillez del diseño de su lazo de control. Teniendo todo esto en cuenta, se procedió al diseño de un prototipo que demostró tener las características necesarias para ser usado como un eficiente *driver* de LED ca-cc monofásico de una sola etapa, capaz de compararse con las propuestas más eficientes del estado del arte. Sus inconvenientes están relacionados con la necesidad un circuito de desmagnetización para ambas inductancias que evite la destrucción de los interruptores en caso de que ocurra algún fallo en el control, el uso de frecuencia variable para su control o la necesidad de interruptores con tensiones de ruptura más elevadas para poder operar en el rango de tensiones europeo de la red de distribución de corriente alterna.

Los capítulos anteriores se centran en el diseño de *drivers* de LED ca-cc. Por el contrario, el Capítulo 4 propone la mejora de la etapa post-reguladora usada en aquellos *drivers* de LED ca-cc monofásicos multi-etapa. La idea se basa en utilizar la carga de LEDs como el propio rectificador de los convertidores cc-cc convencionales, de manera que se consiga reducir el coste eliminando el diodo rectificador y el condensador de salida. Es por ello, que en estas topologías los LEDs operan con una corriente pulsada de alta frecuencia, siendo este el motivo que los hace denominarse *drivers* AC-LED. Sin embargo, los LEDs de luz blanca disponibles en el mercado no están preparados para esta

conmutación a alta frecuencia y muestran un efecto de recuperación inversa muy significativo. Este es el motivo que lleva a proponer el uso del interruptor de onda completa cuasi-resonante dando lugar a la familia de *drivers* ZCS-QRC AC-LED. Estos *drivers* AC-LED son capaces de eliminar el efecto de recuperación inversa tal y como se propuso en el análisis estático de la Sección 4.2.

Es importante tener en cuenta que este capítulo valida experimentalmente la operación del DL//S ZCS-QRC AC-LED *driver*. Aunque el DL//L ZCS-QRC AC-LED *driver* funcione teóricamente, debido a la alta tensión en inversa soportada por los LEDs presenta serios problemas que hacen imposible la implementación práctica de esta solución. Es por ello que solamente se somete al DL//S ZCS-QRC AC-LED *driver* en la Sección 4.4 a una prueba de fiabilidad en un periodo de 700 h comparándolo con un DL//S y un elevador cc-cc. Durante esta prueba se pudo observar como el rendimiento lumínico del DL//S AC-LED *driver* disminuía rápidamente con el tiempo debido al efecto de recuperación inversa en los LEDs, lo que acabó descartando la topología. Finalmente, el DL//S ZCS-QRC AC-LED *driver* muestra ventajas sobre el elevador cc-cc convencional:

- mejor rendimiento en términos de vida útil.
- eliminación del diodo rectificador.
- reducción del tamaño del condensador de salida.
- la habilidad de operar a más alta frecuencia debido a que es capaz de obtener conmutaciones suaves en el interruptor principal.

En resumen, la presente Tesis se ha encargado de presentar varias topologías de potencia que pueden ser usadas como *drivers* de LED que cumplen las normativas más restrictivas y mejoran el rendimiento de aquellas propuestas en el estado del arte.

5.2 Trabajo futuro

El futuro de la investigación propuesta para los *drivers* de LED propuestos en esta tesis, se puede realizar centrar en su optimización, lo que ha sido una constante en las soluciones presentadas en los últimos trabajos dentro de esta temática. La optimización se puede enfocar en mejoras de la etapa de potencia o bien mediante la mejora de la metodología de control.

5.2.1 *Driver* de ca-cc LEDs trifásicos y multi-celda

En lo que respecta al análisis de los drivers de LED ca-cc trifásicos, la optimización de la celda es la clave para obtener soluciones más eficientes que tengan como objetivo alcanzar altas densidades de potencia. Esta optimización se puede enfocar hacia las celdas basadas en una sola etapa o en una doble etapa. En concreto mediante:

- el uso de convertidores con PFC sin puente rectificador, que incrementen su rendimiento al eliminar los diodos de baja frecuencia de la entrada del convertidor.
- el uso de convertidores cc-cc aislados y resonantes que tengan un rendimiento optimizada para las bajas cargas, de tal manera que se extienda su rango de operación.

- el estudio del número óptimo de celdas. Lo que implica un estudio sobre el serializado y paralelizado de celdas de menores tensiones y corrientes, con el objetivo de seleccionar los dispositivos semiconductores óptimos.

Además, se pueden realizar también sendas mejores en términos del control del *driver* de LEDs ca-cc multi-celda que, por supuesto, no excluye aquellas mejoras que se hayan hecho a la etapa de potencia, como son:

- la inclusión de un lazo de control a la primera etapa de cada una de las celdas, que se asegure que todas ellas demanden la misma potencia, contribuyendo así a reducir el de seis veces la frecuencia de red rizado presente en la salida. Esto mejorará por tanto la capacidad de disminuir el tamaño del condensador de salida.

- la inclusión de un lazo de control de balanceo que se asegure que frente a cambios en la tensión de entrada no existe efecto alguno en la potencia demandada o en la corriente que circular a través de la carga de LEDs.

5.2.2 *Push-pull* de doble inductancia alimentado en corriente

Como se ha comentado previamente el convertidor *push-pull* de doble inductancia alimentado en corriente, presenta muchas ventajas que le hacen poder compararse con las soluciones más eficientes presentes en el estado del arte. Sin embargo, el diseño del convertidor construido está lejos de ser el óptimo, ya sea en términos de pérdidas o tamaño. En este sentido, el trabajo futuro se podría centrar en:

- el diseño de componentes magnéticos. Como se ha podido comprobar en la distribución de pérdidas, los componentes magnéticos contribuyen a la mitad de las pérdidas de este *driver* de LEDs. Por este motivo, se plantea evaluar su operación en modo de conducción continuo, para reducir así las pérdidas en los componentes magnéticos, y que son debidas a la corriente eficaz más alta por su operación en modo de conducción frontera equivalente.

- el estudio del diseño del filtro EMI y su comparación en términos de su tamaño con otras topologías presentes en el estado del arte, considerando además el cumplimiento de los límites impuestos por la normativa EMI en luminarias y que es descrita en EN 55015:2013.

Asimismo, y teniendo en cuenta la posibilidad de poder transformar esta topología en un convertidor sin puente rectificador, su rendimiento puede ser mejorado mediante el uso de interruptores bi-direccionales que sean capaces de bloquear en ambas direcciones. La inclusión de estos interruptores no afectará a la operación discutida a lo largo del Capítulo 3. Por otro lado, se propone estudiar el desarrollo de un driver de LED para rango de tensión universal basado en el DICPP mediante el uso de interruptores que sean capaces de bloquear 1.2 kV, siguiendo el criterio descrito en (3.18).

Finalmente, en lo que respecta a la eliminación del condensador electrolítico, esto se puede concretar mediante cualquier de los métodos discutidos en el Capítulo 1, obteniendo así un *driver* de LEDs ca-cc monofásico y de casi una sola etapa, con un alto rendimiento.

5.2.3 *Drivers* de alta frecuencia AC-LED

El Capítulo 4, plantea el uso de los LEDs como el diodo rectificador de un convertidor cc-cc convencional. En ese sentido el trabajo futuro puede dividirse para este tipo de *drivers* de LEDs en dos vertientes:

- el estudio de los *drivers* de alta frecuencia AC-LED operando en modo de conducción discontinuo o en modo de conducción frontera, que sean capaces de eliminar el efecto de recuperación inversa. De esta manera se evitaría que cayera la eficacia lumínica con el tiempo, debido a la reducción del di/dt en los LEDs durante su apagado en los modos de operación mencionados con anterioridad. En este caso, a través de los LEDs circulará una corriente de tipo triangular y pulsada, lo que requiere un estudio detallado con un test de fiabilidad como el desarrollado en el Capítulo 4.

- el estudio del análisis dinámico de los *drivers* ZCS-QRC AC-LED. La operación en lazo cerrado de estos *drivers* fue desarrollada a través de las medidas experimentales de la planta y realizadas con un analizador de frecuencias. Por este motivo, y en visos de completar el análisis matemático, se propone realizar el análisis de pequeña señal, que además ayude al diseño de estos *drivers* AC-LED. Además, se deberá realizar una validación experimental del modelo obtenido en condiciones de *dimming*.

5.3 Financiación

Este trabajo de Tesis ha sido financiado principalmente por el Principado de Asturias mediante la beca pre-doctoral Severo Ochoa BP14-140. Asimismo, otros patrocinadores incluyen al Gobierno de España mediante los proyectos MINECO13-DPI2013-47176-C2-2-R y MINECO-17-DPI2016-75760-R, al Principado de Asturias mediante el proyecto FC-15-GRUPIN14-143 y a los Fondos Europeos de Desarrollo Regional (FEDER).

A

Closed loop operation of the three-phase multi-cell ac-dc LED drivers

The objective of Appendix A is detailing the steps to design the compensator for both the Delco LED ac-dc driver and the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier.

A.1 Detailed description of the designed current loop

The required compensator is responsible for controlling the current across the LED load depending on the value taken by the current reference. In addition, this reference can vary its value in order to achieve the different dimming conditions.

The starting point to close the loop in terms of the current across the LED load for both the Delco ac-dc LED driver and the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier is obtaining the transfer function that relates $\hat{i}_o$ and $\hat{d}$. Therefore by particularizing (2.13) for the flyback converter used in the experimental validation of both prototypes,

$$G_{i_o d}(s)=\left.\frac{\hat{i}_o}{\hat{d}}\right|_{\hat{v}_{gp}=0}=\frac{3v_{gp}^2 DT_s}{2LV_o}\frac{1}{C_o\frac{n}{m}r_{LED}s+\left(\frac{n}{m}\frac{r_{LED}}{R_{eq}}+1\right)}, \tag{A.1}$$

can be obtained. Then, (A.1) can be particularized at maximum load, which is the most restrictive operating point, in accordance to the values set in Table 2.9 in order to model the experimental prototype, yielding,

$$G_{i_o d}(s)=\frac{5.979}{0.1152s+4500}. \tag{A.2}$$

Table A.1. Values used to model the dynamic response at full load of the LED drivers under study.

	Value
V_{gp}	325 V
D	0.3
T_s	1 μs
L	760 μH
V_o	48 V
C_o	10 μF
r_{LED}	1.2 Ω
n	12
m	5
R_{eq}	23.04 Ω

Subsequently, (A.2) is discretized at the switching frequency using the Tustin approximation that provides a good matching between the continuous system and its discretized approximation [A.1]. Hence,

$$G_{i_o d}(z)=\frac{2.171\cdot10^{-4}}{z-0.6732}. \tag{A.3}$$

The discretization is necessary to implement the compensator inside the digital controller, in this particular case an FPGA. Nonetheless, there are several components that need to be taken into account before proceeding into the compensator design. For that matter, Fig. 2.50 shows a simplified diagram of the proposed control for both ac-dc LED drivers under study. As can be seen, the current across the LED load is measured with a shunt followed by an amplifier that adjusts the voltage drop on the shunt within the limits of the ADC. The data from the ADC is, then, provided to the FPGA, where it will be compared to the current reference generating an error signal. The obtained error signal will be processed by the compensator and the digital PWM module, generating a PWM signal that is then sent isolated to each of main switches of the cells. By going this it is possible to vary v_c, varying at the same time the power supplied to the LED load, in accordance to the control feedback loop.

The block diagram depicted in Fig. A.2, shows a simplified diagram of the system for which the compensator, C(z), needs to be design. This systems takes into account, the gains the shunt and its amplifier circuit, H_R, the gain of the ADC, H_{AD}, and the gain related to the digital PWM ramp inside the FPGA whose value is set by the peak value of said ramp, H_{ramp}.

Another important fact that needs to be taken into account for the design of the compensator is related to the bandwidth of the system. In this particular case, and

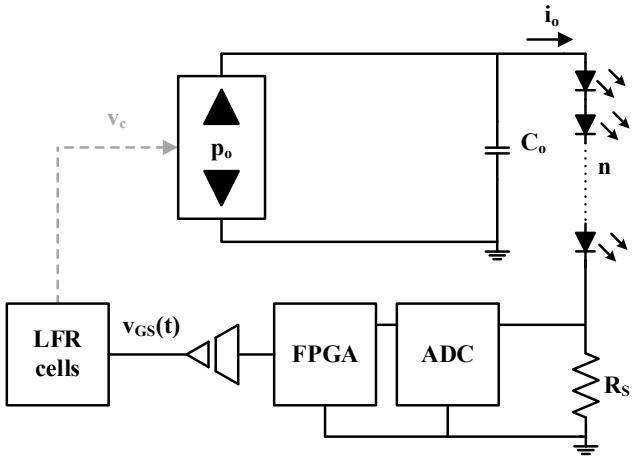


Fig. A.1. Simplified control diagrama of the three-phase multi-cell ac-dc LED drivers.

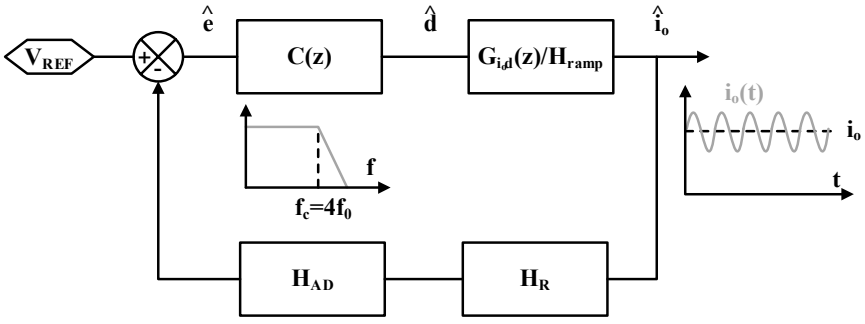


Fig. A.2. Block diagram of the digital control feedback loop.

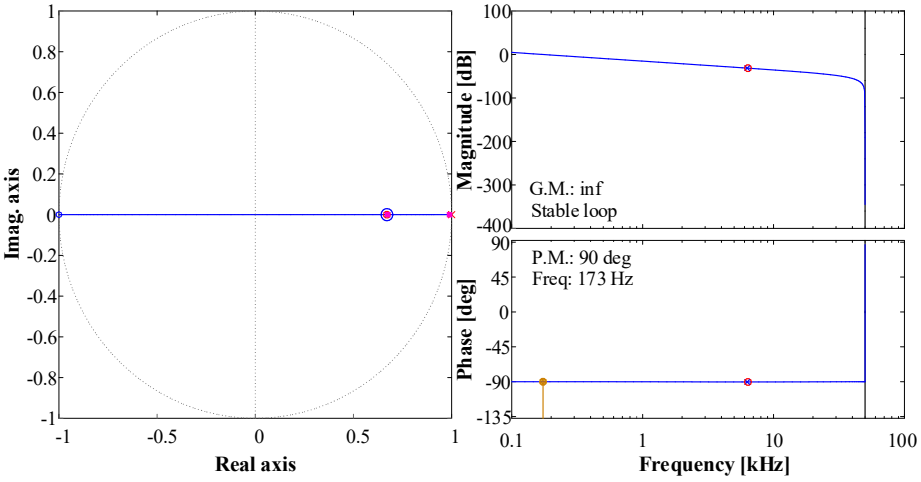
considering that, as has been seen in Section 2.6, the non-idealities of the cells of the ac-dc LED drivers and the power grid translate into an undesired ripple on the current across the LED load at six times the line frequency, f_0. Then, the compensator needs to be designed to filter those components similarly to a conventional compensator for a single-phase LED driver whose crossover frequency, f_c, needs to be well below the twice the line frequency component. For that matter, setting f_c in this particular case at four times f_0 is a good design practice.

The last aspects that need to be looked into before starting the design of the compensator are inherent to digital control, as are: quantization effects and limit cycling [A.2]. Limit cycling can introduce undesired variations at the output of the ac-dc LED driver at frequencies lower than f_s, which if large, can introduce undesired oscillations on the output current that could potentially harm the LED load. The reason for their appearance is normally due to quantizers such as, ADC or digital PWM modules. In order to avoid this issue, there are a detailed set of conditions which are particularized for PFC in [A.3]. These conditions are necessary but not sufficient to avoid limit cycling, but they are nonetheless followed for the design of the compensator and the whole system, as there are some changes that can impact the ramp and the number of bits used by the ADC.

At this point, it is possible to start the design of the compensator. The first step is adding an integrator in order to guarantee that in steady state the error is zero. Then, a real zero is added to cancel the pole in order to keep a phase margin of 90º. Finally, the gain is adjusted for the desired bandwidth of 173 Hz. In order to show the stability of the system Simulink Control Design™ has been used, representing in Fig. A.3, both the root locus and the Bode diagram of the open loop gain of the ac-dc LED driver, considering all the gains and the limit cycling conditions, attaining the next compensator:

$$C(z)=\frac{24.8(z-0.6732)}{z-1}, \tag{A.4}$$

The control loop is not particularly fast in its response as seen in Fig. A.4 for a current reference step that translates in the current across the LED load going from 0 to 1 A (i.e., from no load to half load in this particular design) with a 3.5 ms settling time. However,



(a) *(b)*

Fig. A.3. Stability study of the digital control feedback loop of the multi-cell ac-dc LED drivers. (a) Root locus. (b) Bode diagram.

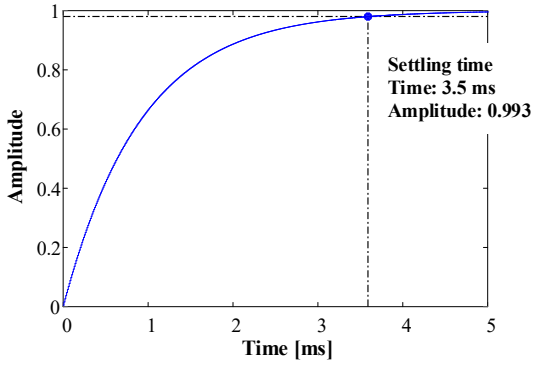


Fig. A.4. Current reference step response under closed loop operation.

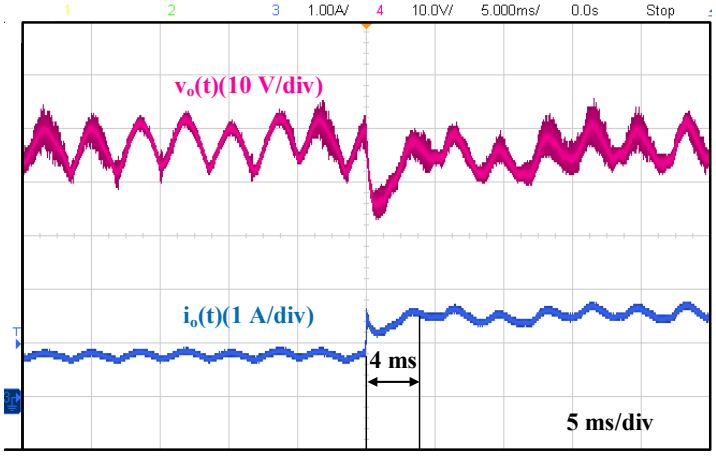
this fact is not significant for an ac-dc LED driver aimed just to be an illumination product, as in this application the LEDs are considered a slow load taking into account that the user will not be able to observe fast changes on the light.

A.2 Experimental results

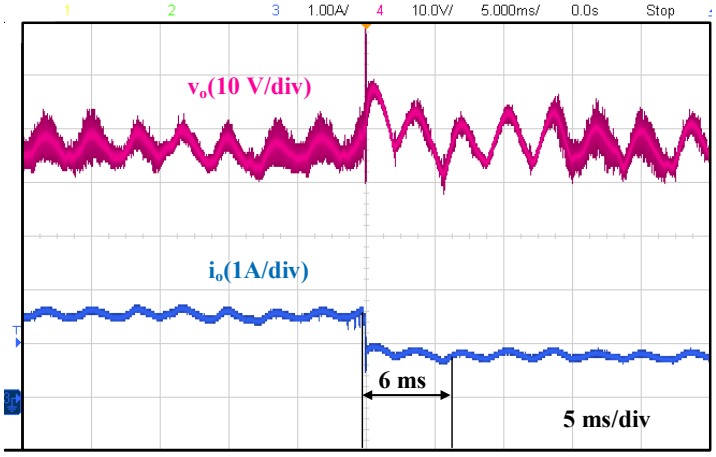
In order to validate the design of the compensator, the prototypes and setup thoroughly described in Section 2.5 will be used. The designed compensator has been coded in VHDL and programmed into an Artix®-7 from Xilinx (i.e., XC7A100T-1CSG324C) [A.4], in conjunction with a digital PWM and the code that controls the ADC and its data extraction.

The aim is doing current reference steps to observe the transient response in terms of the current across the LED load while keeping the current across the LED load regulated to a certain current level. For that matter, Fig. A.5 (a) shows the transient when the current goes from half to full value, while Fig. A.5 (b) goes from full to half value. As can be seen, the settling time in Fig. A.5 (a) coincides with the expected result shown theoretically in Fig. A.4.

It should be noted that these measurements have been performed for both isolated multi-cell ac-dc LED drivers obtaining similar results. For that matter, the results of Fig. A.5 correspond to the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier.



(a)



(b)

Fig. A.5. Current reference step transient response for the multi-cell ac-dc LED driver based on the three-phase full-wave rectifier. (a) Half load to full load. (b) Full load to half load.

A.3 References

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B

Control circuitry for the multi-cell ac-dc LED drivers based on a boost LFR cell

This appendix details the analog control circuitry used to correctly operate the two-stage Delco ac-dc LED driver, and the multi-cell LED driver based on summing the light output of each phase, considering its two control variants. The proposal considers its start-up by means of analog circuitry when a PFC boost converters based on an MBC is used as the front-end converter of the cell. The proposed control is decentralized when possible in order to achieve plug and play cells.

B.1 Control circuitry for the two-stage Delco LED driver

Along Section 2.6 the use of a two-stage Delco LED driver was introduced in an attempt to improve the efficiency of the previously introduced flyback cells. The proposed control, which was depicted in Fig. 2.31, focused at the time on the variables to control in order to remove the electrolytic capacitor. The aim of this appendix is detailing the whole control circuitry, particularly focusing on the circuitry required for the start-up of the ac-dc LED driver.

The cell introduced in Section 2.6 is based on a PFC boost converter followed an isolated dc-dc converter. In accordance to said analysis, the PFC boost converter needs to receive v_c, which sets the amount of power demanded by said converter, and a signal that tells the IC to be enabled, in order to comply with the start-up methodology. Fig. B.1, details the proposed control methodology for this part of the two-stage cell. As can be seen, the UCC3817 is responsible for ensuring an LFR performance by means of its ICC, which as a reminder is the input current control loop. This LFR performance is achieved with an MBC by measuring the input current and comparing it with a sinusoidal voltage reference that is generated from the input voltage of the cell.

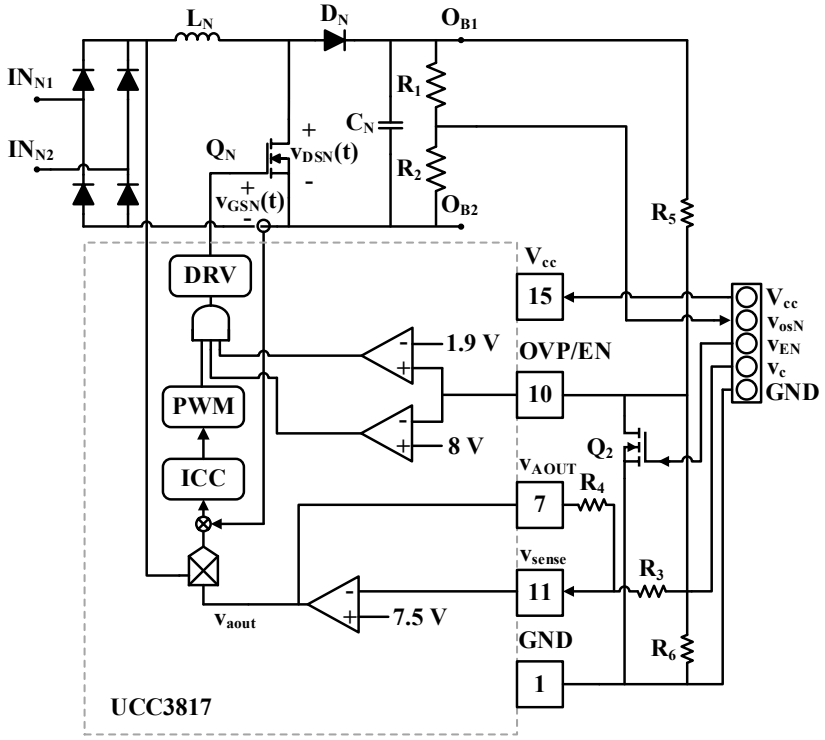

Fig. B.1. Control circuitry of the boost PFC converter used as the front-end converter of the two-stage cell.

Takin into account the aforementioned operation required for the PFC boost converter, some adjustments were required on the UCC3817EVM evaluation board [2.48]. For that matter, and as shown in Fig. B.1, the evaluation board has a five pin connector added, that receives: the supply voltage for the control, V_{cc}, the enable signal, v_{EN}, the control signal, v_c and the control ground, GND, while only sending the information on the output voltage, v_{os}, which will be used to detect on the central control unit when does the output voltage reach a certain mark. In this same figure, there can be seen the input and output terminals of the PFC boost converter, being IN_{N1} and IN_{N2} the input terminals, which are to be connected to the grid, and O_{B1} and O_{B2} the output terminals, which are to be connected to the VICOR module.

The enable signal, v_{EN}, is used to drive Q_2. Thus, by setting v_{EN} to '1', the tenth pin of the UCC3817 (i.e., OVP/EN) will be connected to GND, disabling the driver as this voltage does not surpass the minimum voltage of 1.9 V set internally by the IC. On the contrary when v_{EN} is '0' the voltage on OVP/EN will be set to a certain amount determined by the output voltage of the PFC boost converter. This voltage should be below the 8 V mark to avoid triggering the overvoltage protection of the IC and a resistive divider needs to be designed adequately (i.e., R_5 and R_6).

As regards v_c, this control signal is received from the central control unit that determines its value in accordance to the current regulator and the current across the LED load, as can be seen in Fig. B.2 (b). This value is then sent to the eleventh pin of the

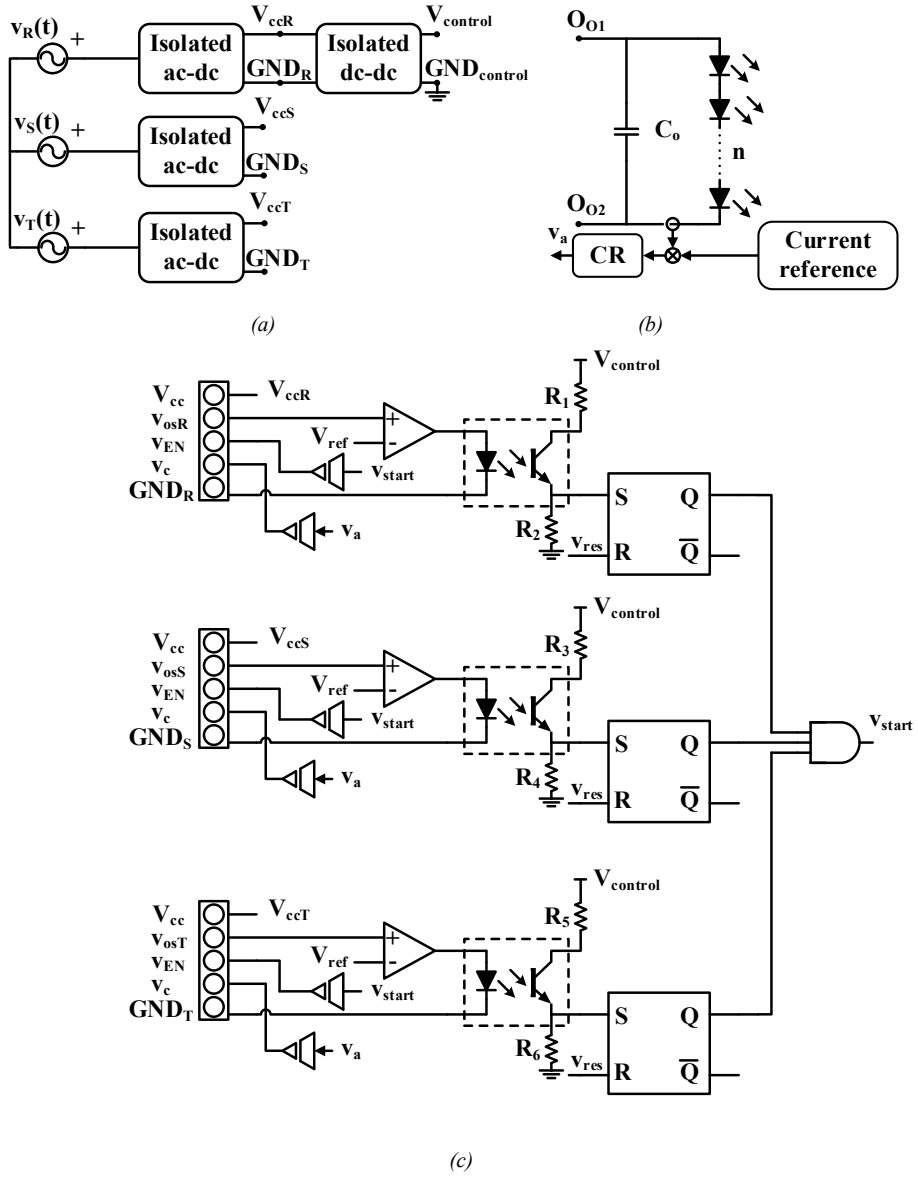

Fig. B.2. Detailed control circuitry of the central control unit on the two-stage Delco ac-dc LED driver. (a) Auxiliary power supplies. (b) LED load and current regulator. (c) Start-up circuitry.

UCC3817 (i.e., v_{sense}) that is connected to the negative pin of the internal operational amplifier, traditionally used for the output voltage regulator. In this particular case and considering that the output current control loop is on the central control unit, the operational amplifier just needs to pass on the information to the ICC, to control the power demanded by the PFC boost converter. For that matter, the operational amplifier is set as a differential amplifier, whose output voltage, v_{aout}, follows the next expression in function of v_c:

$$v_{aout}=2v_c-7.5\ V, \tag{B.1}$$

considering that R_3 is equal to R_4. It should be noted, that even if R_3 and R_4 seem to be included internally in the IC due to the diagram shown in Fig. B.1, in actuality they are not as they are connected externally to their respective pins.

Continuing with the central control unit, Fig. B.2 shows all the included circuitry required for the control of the cells. As can be seen, there are three isolated ac-dc converters that process 1 W each in order to supply the control circuitry of each of the cells, see Fig. B.2 (a), and working as the auxiliary power supply of each of the boost LFR cells. Then, there is an isolated dc-dc converter following one of the isolated ac-dc au responsible for supplying the control circuitry included in the central control unit.

As regards the current regulator, which is also included in the central control unit, it generates the control action, v_a, for all the boost LFR cells. This signal is isolated before sending it to any of the aforementioned LFR cells.

Moreover, the central control unit receives the five aforementioned signals from each of the PFC boost converters. As a reminder, for the start-up of the Delco ac-dc LED driver based on a two-stage solution for each cell, the first condition, in order to enable all the PFC boost converters at the same time, requires for the voltage on all three bus capacitors (i.e., C_R, C_S and C_T) to reach its maximum value, which depends on the maximum peak voltage of the three-phase power grid [B.2]. This is implemented by comparing the value of v_{osN} received from each of the PFC boost converters with a voltage reference V_{ref}. Once v_{osN} surpasses V_{ref}, the output voltage of the comparator will take a high value. This information is then isolated and sent to an SR latch with the help of an optocoupler polarized adequately. The task performed by the SR latch is keeping the signal received from the comparator at a high level, in order to avoid deactivations caused by noise. The SR latches will only be restarted whenever the driver needs be rearmed after an error has been detected. In this case the signal v_{res}, will be set to a high value. The Q signals from each of the three SR latches meet in an AND logic gate, that is used to determine when all of the Q signals have reached a high value. The output of this AND logic gate, v_{start}, is then isolated and sent to each of the PFC boost converters in order to enable or disable them, depending on its value.

Once all PFC boost converters are enabled, the next step in the start-up procedure is enabling the isolated dc-dc converters, however, this cannot be done immediately and the voltage on the bus capacitor is required to reach a 90% of the nominal voltage on the bus capacitors. Unlike the previous scenario when all three PFC boost converters needed to be started at the same time, in this step the isolated dc-dc converters will be started whenever the aforementioned condition is reached on each bus. Therefore, the start-up procedure can be performed individually and the control circuitry can be included within the isolated dc-dc converter, see Fig. B.3.

The condition on the required bus voltage is met with the help of a comparator followed by a SR latch in a similar fashion to which was developed for the central control unit. Particularly, the isolated dc-dc converter based on the BCM384F480T325A00 from VICOR [2.47] can be enabled or disabled by setting the PC pin to high or low, respectively. It should be noted, that in case of a reset or malfunction the signal v_{res} will be put to high level, to disable the isolated dc-dc converter.

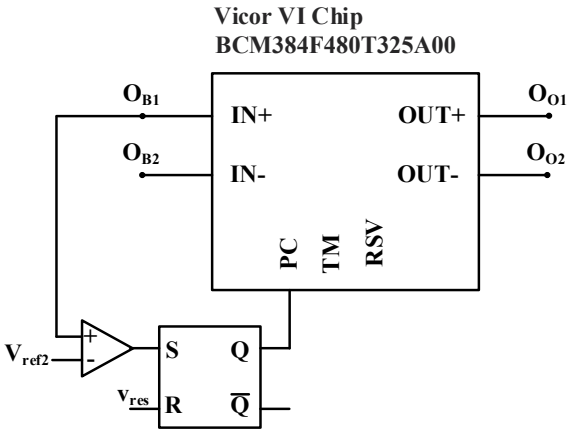

Fig. B.3. Control circuitry for the isolated dc-dc converter of the cell, based on the BCM384F480T325A00.

Another important feature that the isolated dc-dc converter needs to achieve is an adequate soft-start. In the aim of reducing the electrolytic capacitor of the cell, the hold-up time decreases dramatically, meaning that if the isolated dc-dc converter is enabled instantly at full load without care, the bus voltage can plummet almost instantly causing the ac-dc LED driver to misbehave. This means that the voltage drop causes the UCC3817 to stop operating as the voltage on PIN 10 can go below 1.9 V, requiring to restart the start-up of the ac-dc LED driver.

B.2 Control circuitry for the multi-cell ac-dc LED driver based on summing the light output of each phase

Along Section 2.4, two different control techniques were proposed for the multi-cell ac-dc LED driver based on summing the light output of each phase. The one used for the experimental results summarized in Section 2.7, was the conventional technique based on having an independent current loop per PFC boost converter. However, similar this control may be compared to the previous subsection of this appendix, it still required some changes to both the PFC boost converter, the central control unit and the start-up methodology.

In this particular case, the PFC boost converter needs to include the CR in order to regulate the average current across the LED load. Even though, the internal operational amplifier of the UCC3817 can be used for this task, it is avoided due to the complications introduced by the internal voltage reference of the IC. Therefore, an external circuitry is used for the CR as can be seen in Fig. B.4, and the output of CR, v_c, will be sent to the IC similarly to the previous scenario.

As regards the start-up procedure, in this particular case all PFC boost converters are required to reach the maximum attainable voltage when disabled on their output capacitances. After this condition is reached, all of them will be enabled. In summary, the extra conditions required for the isolated dc-dc converter are removed with said power stage.

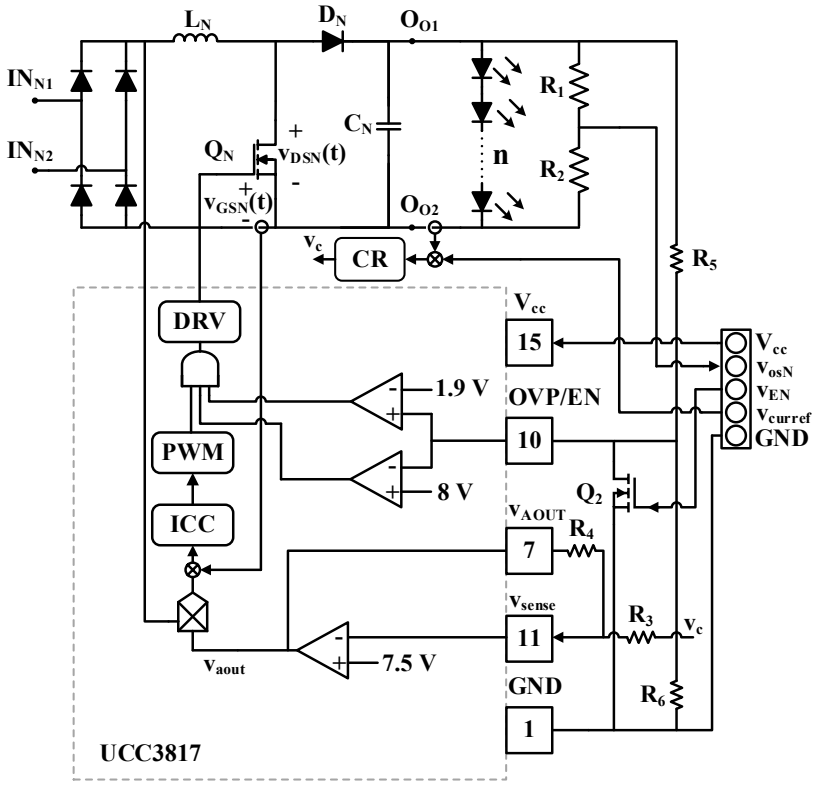

Fig. B.4. Control circuitry of the boost PFC converter used as the cell of the multi-cell ac-dc LED driver based on summing the light output of each phase with the conventional current loop regulator.

Keeping this start-up procedure in mind, Fig. B.5, shows the detailed control circuitry included in the central control unit. As can be seen, the proposed circuitry is exactly the same as in the two-stage Delco ac-dc LED driver, but for the output current feedback loop, that in this case is replaced with the current reference used to attain dimming conditions in all three PFC boost converters at the same time.

For the other proposed control methodology based on measuring the light output at a fixed distance, the PFC boost converter cell will be the same in terms of blocks, as the one depicted in Fig. B.1. The singularities in this particular case come from the central control unit, as instead of having a control current loop like Fig. B.2, it receives with the help of a wireless connection the information of v_a from the control circuitry depicted in Fig. B.6. Nonetheless, the rest of the control circuitry is the same as the one depicted in the aforementioned figure, and the start-up will follow the same principle.

Fig. B.6 shows the transimpedance amplifier used to convert the measured light into a voltage level that is then compared to a reference before going through the LR to control the light output of the LED driver. This circuit is rather simple and reliable, the only problem comes from the requirement of being positioned at a fixed distance without power supplies in reach. The use of batteries with solar panels or harvesting techniques can be evaluated in conjunction with a very low consumption module in order to simplify reduce the cost and increase the viability of this solution.

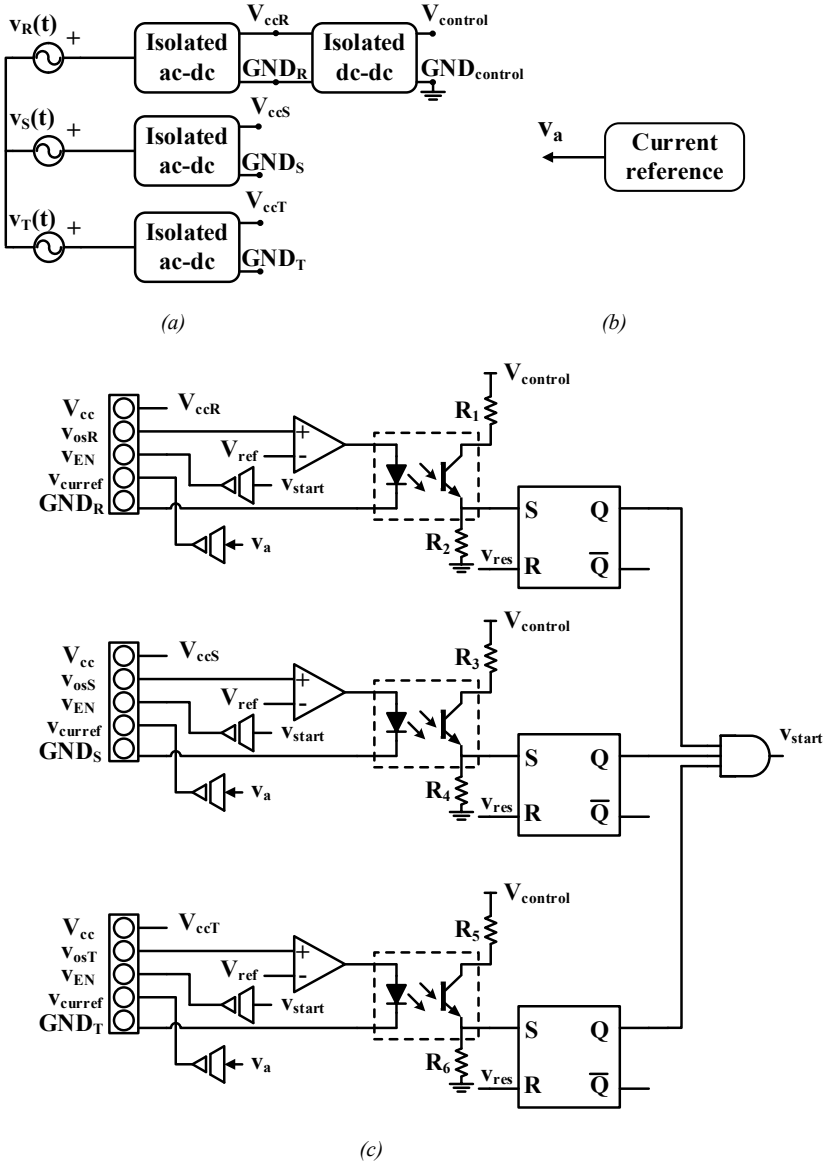

Fig. B.5. Detailed control circuitry of the central control unit for the multi-cell ac-dc LED driver based on summing the light output of each phase with the conventional current loop regulator. (a) Auxiliary power supplies. (b) Current reference. (c) Start-up circuitry.

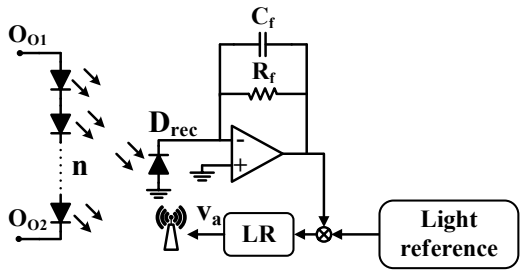

Fig. B.6. Control circuitry to measure the light output of the multi-cell ac-dc LED driver based on summing the light output of each phase.

B.3 References

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[B.2] M. Kumar, L. Huber and M. M. Jovanovic, "Startup procedure for three-phase three-wire isolated ac-dc converter implemented with three single-phase converter modules," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 46-53.

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C

Mathematical analysis of the ZCS-QRC AC-LED drivers

The objective of Appendix C is detailing the steps to obtain the mathematical expressions developed to model both ZCS-QRC AC-LED drivers, which were discussed in Chapter 4.

C.1 Mathematical analysis of the DL//S ZCS-QRC AC-LED driver

C.1.1 Linear stage

The state equations that define the linear stage are,

$$\begin{cases} i_{in}=i_{L_r}(t)+C_r\dfrac{dv_{C_r}(t)}{dt}+i_o(t) \\ v_{C_r}(t)=i_o(t)nr_{LED}+nV_{\gamma\_LED}, \\ L_r\dfrac{di_{L_r}(t)}{dt}=v_{C_r}(t) \end{cases} \tag{C.1}$$

with the next initial conditions: $i_o(0) = i_{in}$, $i_{Lr}(0) = 0$ and $v_{Cr}(0) = v_o$.

The first step is applying the Laplace transform to (4.3), yielding,

$$\frac{i_{in}}{s}=i_{L_r}(s)+C_r\left(sv_{C_r}(t)-v_{C_r}(0)\right)+i_o(s), \tag{C.2}$$

$$v_{C_r}(s)=i_o(s)nr_{LED}+\frac{nV_{\gamma\_LED}}{s}, \tag{C.3}$$

and,

$$L_r s i_{L_r}(s)=v_{C_r}(s). \tag{C.4}$$

The aim is solving first for $i_{Lr}(s)$, however, some previous steps are required. Thus, solving (C.3) into (C.2), gives,

$$\frac{i_{in}}{s}=i_{L_r}(s)+C_r\left(sv_{C_r}(t)-v_{C_r}(0)\right)+\frac{1}{nr_{LED}}\left(v_{C_r}(s)-\frac{nV_{\gamma\_LED}}{s}\right), \tag{C.5}$$

and, then substituting (C.4) into (C.5), yields,

$$\frac{i_{in}}{s}=i_{L_r}(s)+C_r\left(L_rs^2i_{L_r}(s)-v_{C_r}(0)\right)+\frac{1}{nr_{LED}}\left(L_rsi_{L_r}(s)-\frac{nV_{\gamma\_LED}}{s}\right). \tag{C.6}$$

At this point it is possible to solve for $i_{Lr}(s)$ obtaining,

$$C_rL_r\left(s^2+\frac{s}{nr_{LED}C_r}+\frac{1}{L_rC_r}\right)i_{L_r}(s)=\frac{i_{in}}{s}+C_rv_{C_r}(0)+\frac{nV_{\gamma\_LED}}{nr_{LED}s}. \tag{C.7}$$

In order to simplify the analysis (C.7) can also be rewritten as,

$$\frac{1}{\omega_n^2}\left(s^2+2\xi\omega_ns+\frac{1}{\omega_n^2}\right)i_{L_r}(s)=\frac{1}{s}\left(i_{in}+\frac{V_{\gamma\_LED}}{r_{LED}}\right)+C_rv_{C_r}(0), \tag{C.8}$$

where

$$\omega_n=\frac{1}{\sqrt{L_rC_r}}\ , \tag{C.9}$$

and,

$$\xi=\frac{1}{2r_{LED}}\sqrt{\frac{L_r}{C_r}}. \tag{C.10}$$

From (C.8) it is now possible to attain $i_{Lr}(t)$ by performing the inverse Laplace transform. In this particular case, the inverse Laplace transform can be performed to the two different terms that appear in the equation applying the linear property of this transformation. Therefore,

$$\begin{aligned} i_{L_r}(t)=\mathcal{L}^{-1}&\left\{\frac{1}{s\left(\frac{1}{\omega_n^2}\left(s^2+2\xi\omega_ns+\frac{1}{\omega_n^2}\right)\right)}\left(i_{in}+\frac{nV_{\gamma\_LED}}{nr_{LED}}\right)\right\}+\\ &\mathcal{L}^{-1}\left\{\frac{C_rv_{C_r}(0)}{\frac{1}{\omega_n^2}\left(s^2+2\xi\omega_ns+\frac{1}{\omega_n^2}\right)}\right\}, \end{aligned} \tag{C.11}$$

Fortunately, these are well-known transformations,

$$\mathcal{L}^{-1}\left\{\frac{1}{(s+a)(s+b)}\right\}=\frac{1}{b-a}\left(e^{-at}-e^{-bt}\right), \tag{C.12}$$

and,

$$\mathcal{L}^{-1}\left\{\frac{1}{s(s+a)(s+b)}\right\}=\frac{1}{ab}\left[1-\frac{1}{b-a}\left(be^{-at}-ae^{-bt}\right)\right], \tag{C.13}$$

where for the particular case of (C.11), a and b are,

$$a=\left(\xi+\sqrt{\xi^2-1}\right)\omega_n, \tag{C.14}$$

and,

$$b=\left(\xi-\sqrt{\xi^2-1}\right)\omega_n. \tag{C.15}$$

For that matter, applying (C.12) and (C.13) to (C.11), yields,

$$i_{L_r}(t)=\frac{v_o}{L_r}a(t)+\left(i_{in}+\frac{V_{\gamma\_LED}}{r_{LED}}\right)c(t), \tag{C.16}$$

where,

$$a(t)=\frac{1}{2\omega_n\sqrt{\xi^2-1}}\left(e^{-\left(\xi-\sqrt{\xi^2-1}\right)\omega_n t}-e^{-\left(\xi+\sqrt{\xi^2-1}\right)\omega_n t}\right), \tag{C.17}$$

and,

$$c(t)=1+\frac{1}{2\sqrt{\xi^2-1}}\left[\left(\xi-\sqrt{\xi^2-1}\right)e^{-\left(\xi+\sqrt{\xi^2-1}\right)\omega_n t}-\left(\xi+\sqrt{\xi^2-1}\right)e^{-\left(\xi-\sqrt{\xi^2-1}\right)\omega_n t}\right]. \tag{C.18}$$

After having obtained $i_{Lr}(t)$, it is just a matter of differentiating its expression to obtain $v_{Cr}(t)$ as,

$$v_{C_r}(t)=L_r\left(i_{in}+\frac{nV_{\gamma\_LED}}{nr_{LED}}\right)a(t)+v_o b(t), \tag{C.19}$$

where,

$$b(t)=\frac{1}{2\sqrt{\xi^2-1}}\left[\left(\xi+\sqrt{\xi^2-1}\right)e^{-\left(\xi+\sqrt{\xi^2-1}\right)\omega_n t}-\left(\xi-\sqrt{\xi^2-1}\right)e^{-\left(\xi-\sqrt{\xi^2-1}\right)\omega_n t}\right]. \tag{C.20}$$

Finally, the expression that defines the output current can be obtained by substituting (C.19) into (4.3), yielding,

$$i_o(t)=\frac{1}{nr_{LED}}\left(L_r\left(i_{in}+\frac{nV_{\gamma\_LED}}{nr_{LED}}\right)a(t)+v_o b(t)-nV_{\gamma\_LED}\right). \tag{C.21}$$

C.1.2 Resonant stage

The initial conditions for this stage are defined by: $v_{Cr}(t_1) = nV_{\gamma\_LED}$ and $i_{Lr}(t_1)$ defined at the end of the linear stage. In addition its state equations are defined as,

$$\begin{cases} L_r \dfrac{di_{L_r}(t)}{dt} = v_{C_r}(t) \\ C_r \dfrac{dv_{C_r}(t)}{dt} = i_{in} - i_{L_r}(t) \end{cases}. \tag{C.22}$$

Following the same reasoning, the first step is applying the Laplace transform to (C.22), yielding,

$$L_r\left(s i_{L_r}(s) - i_{L_r}(t_1)\right) = v_{C_r}(s), \tag{C.23}$$

and,

$$C_r\left(s v_{C_r}(s) - v_{C_r}(t_1)\right) = \frac{i_{in}}{s} - i_{L_r}(s). \tag{C.24}$$

Now, substituting (C.23) into (C.24), gives,

$$C_r\left(sL_r\left(s i_{L_r}(s) - i_{L_r}(t_1)\right) - v_{C_r}(t_1)\right) = \frac{i_{in}}{s} - i_{L_r}(s). \tag{C.25}$$

Subsequently, solving for $i_{Lr}(s)$, yields,

$$(C_r L_r s^2 + 1) i_{L_r}(s) = \frac{i_{in}}{s} + sC_r L_r i_{L_r}(t_1) + C_r v_{C_r}(t_1). \tag{C.26}$$

To (C.26) the inverse Laplace transform can be applied, again, considering its linear property,

$$i_{L_r}(t) = \mathcal{L}^{-1}\left\{\frac{i_{in}\omega_n^2}{s(s^2+\omega_n^2)}\right\} + \mathcal{L}^{-1}\left\{\frac{s i_{L_r}(t_1)}{(s^2+\omega_n^2)}\right\} + \mathcal{L}^{-1}\left\{\frac{v_{C_r}(t_1)}{L_r(s^2+\omega_n^2)}\right\}. \tag{C.27}$$

These are also well-known transformations, that are defined by,

$$\mathcal{L}^{-1}\left\{\frac{1}{s(s^2+\omega_n^2)}\right\} = \frac{1}{\omega_n^2}\,(1 - \cos(\omega_n t)), \tag{C.28}$$

$$\mathcal{L}^{-1}\left\{\frac{s}{(s^2+\omega_n^2)}\right\} = \cos(\omega_n t), \tag{C.29}$$

and,

$$\mathcal{L}^{-1}\left\{\frac{\omega_n}{(s^2+\omega_n^2)}\right\} = \sin(\omega_n t), \tag{C.30}$$

Applying the introduced inverse Laplace transformations (i.e., (C.28), (C.29) and (C.30)) to (C.26), gives,

$$i_{L_r}(t)=i_{in}+\frac{nV_{\gamma_{LED}}}{Z_n}\sin(\omega_n t)+\left(i_{L_r}(t_1)-i_{in}\right)\cos(\omega_n t). \tag{C.31}$$

Once $i_{Lr}(t)$ expression is obtained, by differentiating in accordance to (C.22), $v_{Cr}(t)$ can be obtained as,

$$v_{C_r}(t)=nV_{\gamma_{LED}}\cos(\omega_n t)-Z_n\left(i_{L_r}(t_1)-i_{in}\right)\sin(\omega_n t). \tag{C.32}$$

C.1.3 Lighting stage

The delay stage will be overlooked considering its analysis is rather simple, as the equivalent circuit is defined by a capacitance. Then, the initial conditions for the lighting stage can be defined by: $i_o(t_3) = 0$ and $v_{Cr}(t_3) = nV_{\gamma\_LED}$. In addition its state equations are defined as,

$$\begin{cases} i_{in}=i_o(t)+C_r\dfrac{dv_{C_r}(t)}{dt} \\ v_{C_r}(t)=i_o(t)nr_{LED}+nV_{\gamma\_LED} \end{cases}. \tag{C.33}$$

This last stage can be analyzed by performing the Laplace transformation on (C.33), yielding,

$$\frac{i_{in}}{s}=i_o(s)+C_r\left(sv_{C_r}(s)-v_{C_r}(t_3)\right), \tag{C.34}$$

and,

$$v_{C_r}(s)=i_o(s)nr_{LED}+\frac{nV_{\gamma\_LED}}{s}. \tag{C.35}$$

Solving (C.35) into (C.34), gives,

$$\frac{i_{in}}{s}=i_o(s)+C_r\left(s\left(i_o(s)nr_{LED}+\frac{nV_{\gamma\_LED}}{s}\right)-v_{C_r}(t_3)\right). \tag{C.36}$$

Afterwards, solving for $i_o(s)$, gives,

$$\frac{i_{in}}{s}+C_r\left(v_{C_r}(t_3)-nV_{\gamma\_LED}\right)=i_o(s)\left(1+sC_r nr_{LED}\right). \tag{C.37}$$

Then, applying the inverse Laplace transform, considering the linear property,

$$i_o(s)=\mathcal{L}^{-1}\left\{\frac{i_{in}}{s(1+sC_r nr_{LED})}\right\}+\mathcal{L}^{-1}\left\{\frac{C_r\left(v_{C_r}(t_3)-nV_{\gamma\_LED}\right)}{(1+sC_r nr_{LED})}\right\}. \tag{C.38}$$

These expressions are also well-know and can the inverse Laplace transform can be easily applied,

$$\mathcal{L}^{-1}\left\{\frac{1}{s(s+c)}\right\}=\frac{1}{c}(1-e^{-ct}), \tag{C.39}$$

and,

$$\mathcal{L}^{-1}\left\{\frac{1}{(s+c)}\right\}=e^{-ct}, \tag{C.40}$$

where,

$$c=\frac{1}{C_r nr_{LED}}, \tag{C.41}$$

for this particular scenario.

Subsequently, taking into account the aforementioned inverse Laplace transforms, $i_o(t)$ can be obtained as,

$$i_o(t)=i_{in}\left(1-e^{-\frac{1}{nr_{LED}C_r}t}\right), \tag{C.42}$$

Consequently, substituting (C.42) into (C.33), gives,

$$v_{C_r}(t)=i_{in}nr_{LED}\left(1-e^{-\frac{1}{nr_{LED}C_r}t}\right)+nV_{\gamma\_LED}, \tag{C.43}$$

ending the mathematical analysis.

C.2 Mathematical analysis of the DL//L ZCS-QRC AC-LED driver

C.2.1 Linear stage

The state equations that define the linear stage are,

$$\begin{cases} C_r \dfrac{dv_{C_r}(t)}{dt} = -i_{in}(t) + i_L - i_o(t) \\ v_{C_r}(t) = i_o(t) nr_{LED} + nV_{\gamma\_LED} \\ L_r \dfrac{di_{in}(t)}{dt} = v_{in} + v_{C_r}(t) \end{cases}. \tag{C.44}$$

with the next initial conditions: $i_o(0) = i_{in}$, $i_{Lr}(0) = 0$ and $v_{Cr}(0) = v_o$.

The analysis carried out below is exactly the same one carried out for the DL//S ZCS-QRC AC-LED driver, and it starts by applying the Laplace transformation to (C.44), obtaining,

$$C_r\left(sv_{C_r}(s) - v_{C_r}(0)\right) = -i_{in}(s) + \frac{i_L}{s} - i_o(s), \tag{C.45}$$

$$v_{C_r}(s) = i_o(s) nr_{LED} + \frac{nV_{\gamma\_LED}}{s}, \tag{C.46}$$

and,

$$L_r(si_{in}(s) - i_{in}(0)) = \frac{v_{in}}{s} + v_{C_r}(s). \tag{C.47}$$

Solving (C.46) into (C.45), yields,

$$C_r\left(sv_{C_r}(s) - v_{C_r}(0)\right) = -i_{in}(s) + \frac{i_L}{s} - \frac{1}{nr_{LED}}\left(v_{C_r}(s) - \frac{nV_{\gamma\_LED}}{s}\right), \tag{C.48}$$

then, solving (C.47) into (C.48), gives,

$$\begin{aligned} C_r\left(s^2 L_r i_{in}(s) - \frac{v_{in}}{s} - v_{C_r}(0)\right) &= -i_{in}(s) + \frac{i_L}{s} \\ - \frac{1}{nr_{LED}}\left(s^2 L_r i_{in}(s) - \frac{v_{in}}{s} - \frac{nV_{\gamma\_LED}}{s}\right). & \end{aligned} \tag{C.49}$$

At this point, it is possible to solve for $i_{in}(s)$ in (C.49), obtaining,

$$\left(L_r C_r s^2 + \frac{L_r}{nr_{LED}} s + 1\right) i_{in}(s) = \frac{v_{in}\left(C_r s + \dfrac{1}{nr_{LED}}\right)}{s} + C_r v_{C_r}(0) - \frac{i_L}{s} - \frac{nV_{\gamma\_LED}}{nr_{LED} s}, \tag{C.50}$$

which can be rewritten as,

$$i_{in}(s)=\frac{C_r\left(v_{in}+v_{C_r}(0)\right)}{\frac{1}{\omega_n^2}\left(s^2+2\xi\omega_n s+\frac{1}{\omega_n^2}\right)}+\left(\frac{nV_{\gamma\_LED}-v_{in}}{nr_{LED}}+i_L\right)\frac{1}{s}\frac{\omega_n^2}{\left(s^2+2\xi\omega_n s+\frac{1}{\omega_n^2}\right)}, \tag{C.51}$$

considering ω_n and ξ relationships with L_r, C_r and r_{LED}, as stated in (C.9) and (C.10).

Subsequently, $i_{in}(t)$ can be obtained by applying the inverse Laplace transform taking into account its linear property. Thus, applying (C.12) and (C.13) to,

$$\begin{aligned} i_{in}(t)=&\mathcal{L}^{-1}\left\{\frac{C_r\left(v_{in}+v_{C_r}(0)\right)}{\frac{1}{\omega_n^2}\left(s^2+2\xi\omega_n s+\frac{1}{\omega_n^2}\right)}\right\}+\\ &\mathcal{L}^{-1}\left\{\left(\frac{nV_{\gamma\_LED}-v_{in}}{nr_{LED}}+i_L\right)\frac{1}{s}\frac{\omega_n^2}{\left(s^2+2\xi\omega_n s+\frac{1}{\omega_n^2}\right)}\right\}, \end{aligned} \tag{C.52}$$

yields,

$$i_{in}(t)=\frac{v_{in}+V_o}{L_r}a(t)-\left(i_L+\frac{nV_{\gamma\_LED}-v_{in}}{nr_{LED}}\right)c(t). \tag{C.53}$$

From $i_{in}(t)$, $v_{Cr}(t)$ can be obtained by differentiation in accordance to (C.44) as,

$$v_{C_r}(t)=v_{in}+L_r\left(I_L+\frac{nV_{\gamma\_LED}-v_{in}}{nr_{LED}}\right)a(t)-\left(v_{in}+V_o\right)b(t). \tag{C.54}$$

Finally, $v_{Cr}(t)$ can be used to attain io(t) as,

$$i_o(t)=\frac{1}{nr_{LED}}\left(v_{in}+L_r\left(I_L+\frac{nV_{\gamma\_LED}-v_{in}}{nr_{LED}}\right)a(t)-\left(v_{in}+V_o\right)b(t)-nV_{\gamma\_LED}\right), \tag{C.55}$$

being a(t), b(t) and c(t) defined by (C.17), (C.20) and (C.18), respectively.

C.2.2 Resonant stage

The initial conditions for this stage are defined by: $v_{Cr}(t_1) = nV_{\gamma\_LED}$ and $i_{Lr}(t_1)$ defined at the end of the linear stage. In addition its state equations are defined as,

$$\begin{cases} L_r\dfrac{di_{in}(t)}{dt}=v_{in}+v_{C_r}(t) \\ C_r\dfrac{dv_{C_r}(t)}{dt}=i_L-i_{in}(t) \end{cases}, \tag{C.56}$$

Following the same reasoning, the first step is applying the Laplace transform to (C.56), yielding,

$$L_r\left(si_{in}(s)-i_{L_r}(t_1)\right)=\frac{v_{in}}{s}+v_{C_r}(s), \tag{C.57}$$