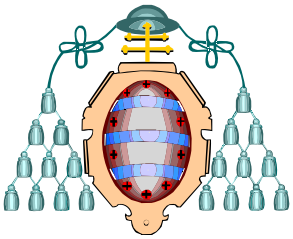


UNIVERSIDAD DE OVIEDO

Department of Electrical, Electronics, Computers
and Systems Engineering

PhD Thesis

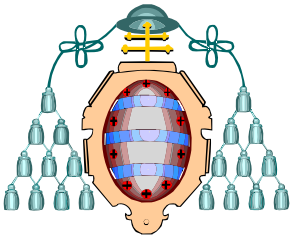
A Hybrid Solution for Distributed Energy Storage for Microgeneration in Microgrids: Design of the Electronic Power and Control System

by

Ramy Georgious Zaher Georgious

Energy and Process Control PhD Program

July 2018



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A Hybrid Solution for Distributed Energy Storage for Microgeneration in Microgrids: Design of the Electronic Power and Control System

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Submitted in Fulfillment of the Requirements for the Degree

of Doctor of Philosophy in

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Thesis Supervisor: Jorge García García

July 2018

To my parents ...

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Abstract

This PhD thesis is focused on the study, analysis, design, and validation of power topologies and control strategies for Power Electronic Converters (PECs) used to interface Hybrid Energy Storage Systems (HESSs) to Direct Current (DC) microgrids and nanogrids. In such type of power systems, a DC bus acts as the power link between the grid Voltage Source Inverter (VSI) converter, the energy storage DC/DC converters and the rest of the DC microgrid. The HESS under analysis consists of two energy storage units with significantly different ratings and characteristics. In the particular case of study, the technologies involved in the storage devices at the Hybrid Systems are an electrochemical Battery Bank (BB) and a Supercapacitor Module (SM). The former device aims to provide long-term energy support to the system, while the latter intends to supply/absorb fast, transient high peak power demands. These devices need to be tightly coordinated to achieve a high-energy and high-power combined storage system, with complementary properties. The storage units are interfaced to the main system through dedicated power converters. The control schemes implemented in these converters need to be coordinated as to manage the power flows according to the system performance requirements.

The main objective of the research is, thus, to propose and compare different topologies and control strategies that provide an adequate system performance during both islanding mode and grid-connected mode. One of the primary purposes of the control stage is to decrease the DC bus voltage variations simultaneously and to perform a fast DC bus recovery, upon fast, relatively large load variations. Also, the control scheme is aimed at increasing the lifetime and State of Health (SoH) of the BB, thus increasing the system reliability and robustness. Al these solutions have been studied, analyzed, demonstrated and validated through simulations and experimental results.

Thesis Supervisor: Jorge García García
Title: Associate Professor

Una Solución Híbrida de Almacenamiento de Energía de Forma Distribuida Aplicado a Microgeneración en Microrredes Redes Eléctricas: Diseño del Sistema Electrónico de Potencia y Control

por

Ramy Georgious Zaher Georgious

Presentada en cumplimiento de los requisitos para la obtención del título de
Doctor en el Programa de Doctorado en Energía y Control de Procesos

Resumen

La presente Tesis Doctoral se centra en el estudio, análisis, diseño y validación de Sistemas de Almacenamiento de Energía Híbridos (HESS por sus siglas en inglés) a microrredes y nanorredes de CC. En dichos sistemas, un bus de CC actúa como punto de intercambio de potencia entre el convertidor de red de CA/CC en el Punto de Acoplamiento Común (PCC), los convertidores de CC/CC del HESS y el resto de la microrred. El HESS objeto de estudio consta de dos unidades de almacenamiento de distintas tecnologías, con especificaciones significativamente diferentes. En el caso considerado, las tecnologías involucradas en los dispositivos de almacenamiento son una Batería electroquímica (BB), que proporciona la energía necesaria para el funcionamiento a largo plazo, más un Módulo de Supercondensadores (SM), dispuesto para suministrar/absorber demandas de alta potencia transitorias y rápidas. Estos dispositivos deben estar estrechamente coordinados para lograr un sistema combinado que presente características complementarias de energía y potencia. Los esquemas de control implementados en los convertidores electrónicos de potencia que interconectan estos dispositivos con la microrred, necesitan ser coordinados para gestionar los flujos de potencia de acuerdo con los requisitos de funcionamiento del sistema.

El objetivo principal de la investigación es proponer y comparar diferentes topologías y estrategias de control para proporcionar un comportamiento adecuado del sistema, tanto en modo aislado como en modo de conexión a la red. También se considera el funcionamiento del sistema en caso de fallo de cortocircuito en el bus CC, así como el rearme del sistema tras la reparación del fallo. Los resultados teóricos obtenidos son validados mediante simulaciones y resultados experimentales realizados en un prototipo de laboratorio.

Director de Tesis: Jorge García García
Categoría: Profesor Titular

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First of all, I would like to thank my PhD thesis supervisor Professor Jorge García García for his guidance, supervision, encouragement, and support during the research.

I do not want to forget my stay in the Department of Electrical and Electronic Engineering with Power Electronics, Machines and Control (PEMC) research group at the University of Nottingham in the United Kingdom, where part of the work was carried out there. I would like to thank Professor Mark Sumner for his supervision during the stay at the University of Nottingham.

I take this opportunity to express gratitude to all my colleges in the laboratory for Electrical Energy Management Unified Research (LEMUR) research group for their support.

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Above of all, I would like to thank my parents as they taught me how to work hard and never give up. Many thanks to my mother for her support, encourage and her prayers for me. I dedicate my thesis to the soul of my father.

Contents

List of Figures

List of Tables

List of Acronyms

AC	Alternating Current
ADC	Analog-to-Digital Converter
ALTESS	Aquiferous Low-Temperature Energy Storage System
BB	Battery Bank
CAESS	Compressed Air Energy Storage System
CESS	Cryogenic Energy Storage System
D	Diode
DAB	Dual Active Bridge
DC	Direct Current
DG	Distributed Generation
DNO	Distribution Network Operator
DoD	Depth of Discharge
DSP	Digital Signal Processor
EDLC	Electric Double-Layer Capacitor
ESR	Equivalent Series Resistance
ESS	Energy Storage System
FBC	Full Bridge Connection
FC	Fuel Cell
Fe-Air	Iron-Air
FESS	Flywheel Energy Storage System
FET	Field Effect Transistor
FF	Form Factor
FT	Fault-Tolerant
FTPC	Fault-Tolerant Parallel Connection

GaN	Gallium Nitride
H_2ESS	Hydrogen Energy Storage System
HESS	Hybrid Energy Storage System
HF	High Frequency
HPF	High Pass Filter
HTTESS	High-Temperature Thermal Energy Storage System
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
Li-Ion	Lithium-Ion
Li-Poly	Lithium-Polymer
$LiFePO_4$	Lithium-Iron Phosphate
LPF	Low Pass Filter
LTTESS	Low-Temperature Thermal Energy Storage System
MOSFET	Metal Oxide Silicon Field Effect Transistor
MPPT	Maximum Power Point Tracking
MSS	Molten Salt Storage
NaNiCl	Sodium Nickel Chloride
NaS	Sodium-Sulfur
NiCd	Nickel-Cadmium
NiFe	Nickel-Iron
NiH_2	Nickel-Hydrogen
NiMH	Nickel-Metal Hydride
NiZn	Nickel–Zinc
p.u.	per unit
PC	Parallel Connection
PCB	Printed Circuit Board
PCC	Point of Common Coupling

PEC	Power Electronic Converter
Ph-Acid	Lead-Acid
PHESS	Pumped Hydro Energy Storage System
PI	Proportional Integral
PLL	Phase Locked Loop
PSB	Polysulfide-Bromide
PSM	Phase Change Material
PV	Photovoltaic
PWM	Pulse Width Modulation
RES	Renewable Energy Source
RMS	Root Mean Square
RTIL	Room Temperature Ionic Liquids
S	Switch
SC	Series Connection
Si	Silicon
SiC	Silicon Carbide
SM	Supercapacitor Module
SMESS	Superconducting Magnetic Energy Storage System
SNG	Synthetic Natural Gas
SoC	State of Charge
SoH	State of Health
SPC	Series-Parallel Connection
TAB	Triple Port Active Bridge
VRFB	Vanadium Redox Flow Battery
VSI	Voltage Source Inverter
WT	Wind Turbine
Zn-Air	Zinc-air
ZnAg	Zinc Silver Oxide
ZnBr	Zinc-Bromine
ZnCe	Zinc-Cerium
ZnMn	Alkaline Zinc-Manganese Dioxide

List of Symbols

A	is the matrix to transform from abc axes to dq axes
A_{c_max}	is the maximum limit for buck carrier
A_{c_min}	is the minimum limit for boost carrier
Bw_{i_BB}	is the bandwidth of the PI controller of the BB current control in Hz
$Bw_{i\_G\_d}$	is the bandwidth of the PI controller of the d-axis grid current control in Hz
$Bw_{i\_G\_q}$	is the bandwidth of the PI controller of the q-axis grid current control in Hz
Bw_{i_SM}	is the bandwidth of the PI controller of the SM current control in Hz
Bw_v	is the bandwidth of the PI controller of the DC bus voltage control in Hz
C_{BB_nom}	is the nominal capacity of the BB in Ah.
C_{BB_rate}	is the discharge current rate of the BB in Amp.
C_{DC_1}	is the capacitance of the upper half of the DC bus's capacitor in Farads
C_{DC_2}	is the capacitance of the lower half of the DC bus's capacitor in Farads
C_{DC}	is the DC bus capacitor's capacitance in Farads
C_{SM}	is the SM capacitance in Farads
E	is the error of the PI controller
ESR_{DC}	is the maximum DC ESR in Ohms
$E[k-1]$	is the value of the error obtained in the previous sample
$E[k]$	is the present value of the error
E_{BB}	is the nominal energy storage in the BB in Watt-hr
E_{SM}	is the SM energy storage in Joules or Watt-secs
E_{off}	is the energy loss at IGBT turn off in Joules Watt-Secs
E_{on}	is the energy loss at IGBT turn on in Joules or Watt-Secs
E_{rec}	is the energy loss of the reverse recovery of the anti-parallel diode in Joules or Watt-Secs
$G_{C_{DC}}$	is the transfer function of the DC bus capacitor

G_{L_1}	is the transfer function of the inductor connected with the BB
G_{L_2}	is the transfer function of the inductor connected with the SM
$G_{L_{f_d}}$	is the transfer function of the filter inductor in d-axis
$G_{L_{fq}}$	is the transfer function of the filter inductor in q-axis
I_{BB_max}	is the maximum BB current (the maximum BB discharging current) in Amps
I_{BB_min}	is the minimum BB current (the maximum BB charging current) in Amps
I_{BB_ref}	is the BB current reference in Amps
I_{BB}	is the BB current in Amps
$I_{C_{DC}\_max}$	is the maximum DC bus capacitor current in Amps
$I_{C_{DC}\_min}$	is the minimum DC bus capacitor current in Amps
$I_{C_{DC}}$	is the DC bus capacitor's current in Amps
$I_{ESS_{DC}}$	is the sum of the currents of the ESS converters at the DC bus side in Amps
I_{G_max}	is the maximum grid current in Amps
I_{G_min}	is the minimum grid current in Amps
$I_{G_{DC}}$	is the grid current delivered/absorbed to/from the DC microgrid in the DC side in Amps
$I_{G_{abc}}$	is the grid current in abc axes in Amps
I_{G_a}	is the grid current in a-axis in Amps
I_{G_b}	is the grid current in b-axis in Amps
I_{G_c}	is the grid current in c-axis in Amps
$I_{G_{dq}}$	is the grid current in dq axes in Amps
$I_{G_{d\_max}}$	is the maximum grid current reference in d-axis in Amps
$I_{G_{d\_min}}$	is the minimum grid current reference in d-axis in Amps
$I_{G_{d\_ref}}$	is the grid current reference in d-axis in Amps
I_{G_d}	is the grid current in d-axis in Amps
$I_{G_{q\_max}}$	is the maximum grid current reference in q-axis in Amps
$I_{G_{q\_min}}$	is the minimum grid current reference in q-axis in Amps
$I_{G_{q\_ref}}$	is the grid current reference in q-axis in Amps
I_{G_q}	is the grid current in q-axis in Amps
$I_{L_1\_avg}$	is the average value of the current through inductor connected with the BB (L_1) in Amps

$I_{L_1\_f\_ref}$	is the fault current reference in Amps
$I_{L_1\_ref}$	is the current reference in the inductor connected with the BB (L_1) in Amps
I_{L_1}	is the current in the inductor connected with the BB in Amps
$I_{L_2\_avg}$	is the average value of the current through inductor connected with the SM (L_2) in Amps
$I_{L_2\_ref}$	is the current reference in the inductor connected with the SM (L_2) in Amps
I_{L_2}	is the current in the inductor connected with the SM in Amps
$I_{L_{f_{abc}}}$	is the current in the inductor in abc axes in Amps
$I_{L_{f_{dq}}}$	is the current in the inductor in dq axes in Amps
$I_{L_{f_d}\_ref}$	is the current reference in the filter inductor in d-axis in Amps
$I_{L_{f_d}}$	is the current in the filter inductor in d-axis in Amps
$I_{L_{fq}\_ref}$	is the current reference in the filter inductor in q-axis in Amps
$I_{L_{fq}}$	is the current in the filter inductor in q-axis in Amps
I_{N_max}	is the maximum current delivered by the rest of the microgrid in Amps
I_{N_min}	is the minimum current delivered by the rest of the microgrid in Amps
I_N	is the Norton current modeling the behavior of the rest of the microgrid in Amps
$I_{O_{DC}\_meas}$	is the measured output current at the acrshordc bus side drawn by the rest of the microgrid in Amps
$I_{O_{DC}}$	is the output current at the DC bus side drawn by the rest of the microgrid in Amps
I_{R_N}	is the current drawn by the load resistance (R_N) in Amps
I_{SM_max}	is the maximum SM current (the maximum SM discharging current) in Amps
I_{SM_min}	is the minimum SM current (the maximum BB charging current) in Amps
I_{SM_ref}	is the SM current reference in Amps
I_{SM}	is the SM current in Amps
I_{S_1}	is the current of S_1 in Amps
I_{S_2}	is the current of S_2 in Amps
I_{S_3}	is the current of S_3 in Amps
I_{S_4}	is the current of S_4 in Amps

I_{avg}	is the average current of a periodic square waveform of swtiching period in Amps
I_{c_max}	is maximum collector pulse current (Current through IGBT) in Amps
I_{c_max}	is minimum collector pulse current (Current through diode) in Amps
I_c	is the on-state collector current of the IGBT in Amps
I_{pk}	is the peak current of a periodic square waveform of swtiching period in Amps
I_p	is the primary current of volatge or current transuducer in Amps
I_p^{LA55-P}	is the primary current of current transuducer in Amps
I_p^{LV25-P}	is the primary current of voltage transuducer in Amps
I_{rms}	is the RMS current of a periodic square waveform of swtiching period in Amps
I_s	is the secondary current of volatge or current transuducer in Amps
K_{f_3}	is the FF of the current for the S_3
K_{f_4}	is the FF of the current for the S_4
K_f	is the FF of the current in the switch
$K_{p\_i\_G\_d}$	is the proportional gain of the PI controller of the d-axis grid current control
$K_{p\_i\_G\_q}$	is the proportional gain of the PI controller of the q-axis grid current control
$K_{p\_i\_SM}$	is the proportional gain of the PI controller of the SM current control
$K_{p_{i\_BB}}$	is the proportional gain of the PI controller of the BB current control
K_{p_v}	is the proportional gain of the PI controller of the DC bus voltage control
K_p	is the proportional gain of the PI controller
L	is the inductance of the inductor in Henries
L_1	is the inductance of the inductor connected with the BB in Henries
L_2	is the inductance of the inductor connected with the SM in Henries
L_f	is the inductance of the filter in Henries
N_{SM}	is the number of cells of the SM
$P_{BB\_ps\_ref}$	is the BB power reference from peak shaving in Watts
$P_{BB\_tr\_ref}$	is the BB transient power reference in Watts
P_{BB_max}	is the maximum power of the BB (the maximum BB discharging power) in Watts

P_{BB_min}	is the minimum power of the BB (the maximum BB charging power) in Watts
P_{BB_ref}	is the power reference of the BB in Watts
$P_{BB\_ref}[k-1]$	is the value of the BB power reference obtained in the previous sample in Watts
$P_{BB\_ref}[k-1]$	is the value of the ESS transient power reference obtained in the previous sample in Watts
$P_{BB\_ref}[k-1]$	is the value of the SM transient power reference obtained in the previous sample in Watts
$P_{BB\_ref}[k]$	is the present value of the BB power reference in Watts
$P_{BB\_ref}[k]$	is the present value of the ESS transient power reference in Watts
$P_{BB\_ref}[k]$	is the present value of the SM transient power reference in Watts
$P_{C_{DC}}$	is the power of the DC bus capacitor in Watts
P_{ESS_max}	is the transient peak power supported by the ESS in Watts
P_{ESS_sus}	is the sustained power supported by the HESS in islanding mode in Watts
$P_{ESS\_tr\_ref}$	is the ESS transient power reference in Watts
P_{ESS_ref}	is the power reference of the ESS in Watts
$P_{ESS\_ref}[k-1]$	is the value of the ESS power reference obtained in the previous sample in Watts
$P_{ESS\_ref}[k-1]$	is the value of the measured power of the load obtained in the previous sample in Watts
$P_{ESS\_ref}[k]$	is the present value of the ESS power reference in Watts
$P_{ESS\_ref}[k]$	is the present value of the measured output power delivered to the rest of the microgrid in Watts
P_{ESS}	is the power of the ESS in Watts
$P_{G\_ss\_ref}$	is the steady-state active grid power reference in Watts
$P_{G\_ss\_ref}[k-1]$	is the value of the steady-state active grid power reference obtained in the previous sample in Watts
$P_{G\_ss\_ref}[k]$	is the present value of the steady-state active grid power reference in Watts
P_{G_max}	is the maximum active grid power (the maximum power delivered from the grid) in Watts
P_{G_min}	is the minimum grid active power (the maximum power absorbed from the grid) in Watts
P_G	is the active grid power in Watts
P_{Loss_PC}	is the power losses of the PC in Watts

P_{Loss_SPC}	is the power losses of the SPC in Watts
P_{MG}	is the rated microgrid power in Watts
P_{N_max}	is the maximum power delivered by the rest of the microgrid in Watts
P_{N_min}	is the minimum power delivered by the rest of the microgrid in Watts
P_{O_max}	is the maximum active output power delivered to the rest of the microgrid in Watts
P_{O_meas}	is the measured active power of the load in Watts
P_{O_min}	is the minimum active output power delivered to the rest of microgrid in Watts
$P_{O\_ref}[k-1]$	is the value of the output power refernce dekivered to the rest of microgrid in the previous sample in Watts
$P_{O\_ref}[k]$	is the present value of the ouput power refernce delivered to the rest of microgrid in Watts
P_O	is the active power delivered to the rest of the microgrid in Watts
$P_{R_N\_max}$	is the maximum load power in Watts
$P_{R_N\_min}$	is the minimum load power in Watts
P_{R_N}	is the load power in Watts
$P_{SM\_ps\_ref}$	is the SM power reference from peak shaving in Watts
P_{SM_max}	is the maximum power of the SM (the maximum SM discharging power) in Watts
P_{SM_min}	is the minimum power of the SM (the maximum SM charging power) in Watts
P_{SM_ref}	is the power reference of the SM in Watts
$P_{avg\_cond\_D}$	is the average conduction losses of the anti-parallel diode in Watts
$P_{avg\_cond\_IGBT}$	is the average conduction losses of the IGBT in Watts
P_{avg_cond}	is the average conduction losses of the switch in Watts
P_{rec_D}	is the reverse recovery losses of the anti-parallel diode in Watts
P_{sw_IGBT}	is the switching losses of the IGBT in Watts
P_{sw}	is the switching losses of the switch in Watts
Q_{BB}	is the nominal capacity of the BB in Amp-hr
Q_{G_max}	is the maximum reactive grid power in Volt-Amps-Reactive
Q_{G_max}	is the minimum reactive grid power in Volt-Amps-Reactive
Q_{G_ref}	is the reactive grid power reference in Volt-Amps-Reactive
Q_G	is the reactive grid power in Volt-Amps-Reactive

R	is the transfer function of the PI controller
R_1	is the parasitic resistance of the inductor connected with the BB in Ohms
R_2	is the parasitic resistance of the inductor connected with the SM in Ohms
$R_{C_{DC}}$	is the transfer function of the PI controller for the DC voltage control
R_{L_1}	is the transfer function of the PI controller for the BB current control
R_{L_2}	is the transfer function of the PI controller for the SM current control
R_N	is the load resistance in Ohms
R_f	is the resistance of the filter in Ohms
SOC_{BB_max}	is the maximum SoC of the BB
SOC_{BB_min}	is the minimum SoC of the BB
SOC_{BB}	is the SoC of the BB
SOC_{SM_max}	is the maximum SoC of the SM
SOC_{SM_min}	is the minimum SoC of the SM
SOC_{SM}	is the SoC of the SM
SOH_{BB}	is the SoH of the BB.
S_G	is the apparent grid power in Volt-Amps
$T_{BB_{LPF}}$	is the time constant of the LPF of the BB power in Secs
$T_{ESS_{HPF}}$	is the time constant of the HPF of the ESS power in Secs
$T_{G_{LPF}}$	is the time constant of the LPF of the active grid power in Secs
$T_{SM_{HPF}}$	is the time constant of the HPF of the SM power in Secs
$T_{i_{i\_BB}}$	is the integral time constant of the PI controller of the BB current control in Secs
$T_{i_{i\_G\_d}}$	is the integral time constant of the PI controller of the d-axis grid current control in Secs
$T_{i_{i\_G\_q}}$	is the integral time constant of the PI controller of the q-axis grid current control in Secs
$T_{i_{i\_SM}}$	is the integral time constant of the PI controller of the SM current control in Secs
T_{i_v}	is the integral time constant of the PI controller of the DC bus voltage control in Secs
T_i	is the integral time constant of the PI controller in Secs
T_{off_S1}	is the off time of the upper switch (S_1) for the SM converter in Secs
T_{off_S3}	is the off time of the upper switch (S_3) for the SM converter in Secs

T_{on_S1}	is the on time of the upper switch (S_1) for the SM converter in Secs
T_{on_S3}	is the on time of the upper switch (S_3) for the SM converter in Secs
T_{on}	is the interval of the waveform that the current value equals peak value in Secs
T_s	is the switching time in Secs
U	is the output of the PI controller after the limiter
$U[k-1]$	is the value of the controller obtained in the previous sample
$U[k]$	is the present value of the controller
U^{PI}	is the output of the PI controller before the limiter
U_{min}	is the minimum value of the PI controller output
U_{min}	is the minimum value of the PI controller output
V_{BB_fl}	is the float voltage of a battery in Volts.
V_{BB_nom}	is the nominal voltage of the BB in Volts.
V_{BB_max}	is the maximum BB voltage in Volts
V_{BB_meas}	is the measured BB voltage in Volts
V_{BB_min}	is the minimum BB voltage in Volts
V_{BB}	is the BB voltage in Volts
V_{CE_2}	is the collector-emitter voltage of the $IGBT_2$ in Volts
V_{CE_4}	is the collector-emitter voltage of the $IGBT_4$ in Volts
$V_{DC\_f\_max}$	is the maximum DC bus voltage threshold in volts
$V_{DC\_f\_min}$	is the minimum DC bus voltage threshold in Volts
V_{DC_max}	is the maximum DC bus voltage in Volts
V_{DC_meas}	is the measured DC bus voltage in Volts
V_{DC_min}	is the minimum DC bus voltage in Volts
V_{DC_ref}	is the DC bus voltage reference in Volts
V_{DC}	is the DC bus voltage in Volts
V_{DSP}	is the input ADC voltage at the DSP in Volts
V_D	is the on-state forward voltage of the anti-parallel diode in Volts
V_{GE}	is the gate-emitter voltage of the IGBT in Volts
$V_{G_{abc}}$	is the grid voltage in abc axes in Volts
V_{G_a}	is the grid voltage in a-axis in Volts
V_{G_b}	is the grid voltage in b-axis in Volts

V_{G_c}	is the grid voltage in c-axis in Volts
$V_{G_{dq}}$	is the grid voltage in dq axes in Volts
$V_{G_{d\_meas}}$	is the measured grid voltage in d-axis in Volts
V_{G_d}	is the grid voltage in d axes in Volts
$V_{G_{q\_meas}}$	is the measured grid voltage in q-axis in Volts
V_{G_q}	is the grid voltage in q-axis in Volts
$V_{L_{1\_max}}$	is the maximum voltage across the inductor connected with the BB in Volts
$V_{L_{1\_min}}$	is the minimum voltage across the inductor connected with the BB in Volts
V_{L_1}	is the voltage across the inductor connected with the BB in Volts
$V_{L_{2\_max}}$	is the maximum voltage across the inductor connected with the SM in Volts
$V_{L_{2\_min}}$	is the minimum voltage across the inductor connected with the SM in Volts
V_{L_2}	is the voltage across the inductor connected with the SM in Volts
$V_{L_{f_{abc}}}$	is the voltage across the inductor in abc axes in Volts
$V_{L_{f_{dq}}}$	is the voltage across the inductor in dq axes in Volts
$V_{L_{f_{d\_max}}}$	is the maximum voltage across the filter inductor in d-axis in Volts
$V_{L_{f_{d\_min}}}$	is the minimum voltage across the filter inductor in d-axis in Volts
$V_{L_{f_d}}$	is the voltage across the filter inductor in d-axis in Volts
$V_{L_{f_{q\_max}}}$	is the maximum voltage across the filter inductor in q-axis in Volts
$V_{L_{f_{q\_min}}}$	is the minimum voltage across the filter inductor in q-axis in Volts
$V_{L_{f_q}}$	is the voltage across the filter inductor in q-axis in Volts
V_L	is the inductor's voltage in Volts
V_{SM_max}	is the maximum SM voltage in Volts
V_{SM_meas}	is the measured SM voltage in Volts
V_{SM}	is the SM voltage in Volts
V_{abcm}	is the three-phase voltage referred to the middle point of the DC bus in abc axes in Volts
V_{ce}	is the on-state collector-emitter voltage of the IGBT in Volts
Z_{BB}	is the internal impendance of a battery in Ohms
ΔI_{L_1}	is the current ripple of the inductor connected with the BB (L_1) in Amps
ΔI_{L_2}	is the current ripple of the inductor connected with the SM (L_2) in Amps

ΔI_L	is the current ripple of the inductor in Amps
ΔP_{Loss}	is the difference in power loss between PC and SPC in Watts
ΔT	is the time duration in Secs
ΔV_{DC}	is the DC bus voltage ripple in Volts
δI_{L_1}	is the p.u. value of the peak to peak current ripple at the inductor connected with the BB L_1
δI_{L_2}	is the p.u. value of the peak to peak current ripple at the inductor connected with the SM L_2
δV_{DC}	is the p.u. value of the peak to peak voltage ripple at the DC bus capacitor C_{DC}
$\frac{dI_L}{dt}$	is the rate of inductor current change in Amps/Sec
$\frac{dV_{DC}}{dt}$	is the rate of DC bus voltage change in Volts/Sec
η_{PC}	is the efficiency of PC of two bidirectional buck converters
η_{SPC}	is the efficiency of SPC of two bidirectional buck converters
$\hat{I}_{C_{DC}}$	is the estimated DC bus capacitor current after the limiter in Amps
$\hat{V}_{L_1}$	is the estimated voltage across the inductor connected with the BB after the limiter in Volts
$\hat{V}_{L_1}^{PI}$	is the estimated voltage across the inductor connected with the BB before the limiter in Volts
$\hat{V}_{L_2}$	is the estimated voltage across the inductor connected with the SM after the limiter in Volts
$\hat{V}_{L_2}^{PI}$	is the estimated voltage across the inductor connected with the SM before the limiter in Volts
$\hat{V}_{L_{f_d}}$	is the estimated voltage across the filter inductor in d-axis after the limiter in Volts
$\hat{V}_{L_{f_d}}^{PI}$	is the estimated voltage across the filter inductor in d-axis before the limiter in Volts
$\hat{V}_{L_{f_q}}$	is the estimated voltage across the filter inductor in q-axis after the limiter in Volts
$\hat{V}_{L_{f_q}}^{PI}$	is the estimated voltage across the filter inductor in q-axis before the limiter in Volts
ω	is the angular frequency of f in rads/sec
ω_e	is the grid frequency in rads/sec
ω_n	is the undamped natural frequency in rads/sec

ζ	is the damping ratio
d	is the duty cycle for a given switch
d_{10}	is the duty cycle of the $IGBT_{10}$
d_1	is the duty cycle of the $IGBT_1$
d_2	is the duty cycle of the $IGBT_2$
d_3	is the duty cycle of the $IGBT_3$
d_4	is the duty cycle of the $IGBT_4$
d_5	is the duty cycle of the $IGBT_5$
d_6	is the duty cycle of the $IGBT_6$
d_7	is the duty cycle of the $IGBT_7$
d_8	is the duty cycle of the $IGBT_8$
d_9	is the duty cycle of the $IGBT_9$
d_{G_a}	is the duty cycle of phase a
d_{G_b}	is the duty cycle of phase b
d_{G_c}	is the duty cycle of phase c
$d_{G_{dq}}$	is the duty cycle in dq axes
d_{G_d}	is the grid duty cycle in d-axis
d_{G_q}	is the grid duty cycle in q-axis
d_{abc}	is the duty cycle in abc axes
d_m	is the modified duty cycle for a given switch
f	is any of the electrical variables, and it could be voltage or current
$f_{BB_{LPF}}$	is the cutoff frequency of the LPF of the BB power in Hz
$f_{ESS_{HPF}}$	is the cutoff frequency of the HPF of the ESS power in Hz
$f_{G_{LPF}}$	is the cutoff frequency of the LPF of the active grid power in Hz
$f_{SM_{HPF}}$	is the cutoff frequency of the HPF of the SM power in Hz
f_a	is the cutoff frequency of the anti-aliasing filter in Hz
f_e	is the grid frequency in Hz
f_m	is the amplitude of f
f_{sa}	is the sampling frequency in Hz
f_s	is the switching frequency in Hz
s	is the Laplace complex variable $s = \sigma + j\omega_d$
t_1	is the instant which the load increases in Secs

t_2	is the instant which the load decreases in Secs
t_3	is the instant which the load decreases in Secs
t_4	is the instant which the load increases in Secs
t_8	is the specific time in Secs
t_D	is the dead time of the swtiching in Secs

Chapter 1

Outline of the Research, Objectives, Methodology and Structure

Contents

1.1 Outline of the Research

This PhD thesis is framed within the scope of electrical engineering, specifically in the disciplines of electrical power systems, power electronics and control systems. The recent developments in new power converter and energy storage devices technologies, together with advances in control strategies and systems, are leading a technological revolution to boost the growth of the Distributed Generation (DG) paradigm. This paradigm is founded on the integration of distributed resources into the transmission and distribution electrical systems, as to maximize the energetic efficiency of the full power grid.

The conventional, centralized generation scheme of power systems assumes Alternating Current (AC) transmission and distribution lines, as to provide an AC mains facility to the end users and consumers. Also, it usually implies that these users are always power consumers. However, as the penetration of renewable energy systems in the grid increases, as electronic loads at the user premises turn out more and more relevant, and as energy storage enters as a term in the equation, the coordination requirements and complexity of the full electrical power system increases significantly. Microgrids and nanogrids emerge as a solution that eases the energy management at local levels, allowing for seamless integration of renewable and distributed resources. In particular, Direct Current (DC) and hybrid AC/DC microgrids or nanogrids are turning a feasible option for increasing the overall efficiency of modern power grids.

As mentioned, Energy Storage Systems (ESSs) are turning into one of the key technologies in power electronics related disciplines. Indeed, by using these systems, there is a reported improvement in the performance at leading applications such as integration in the distribution network of stochastic power generators, grid stability and power quality support upon line contingencies, management of fast-dynamics high-power loads at the power-train in electric-hybrid vehicles, and a manifold of industrial applications with a load profile of large transient characteristics, among others.

One particular case of these systems is the Hybrid Energy Storage Systems (HESSs). Generally speaking, these HESS interface a fast-dynamics high-power storage device, plus a slower, bulk-energy storage unit, to the original power system under consideration. The design of the full hybrid system involves the selection of adequate energy and power ratings in its elements and parts, as well as the design of a control scheme that manages the involved power flows appropriately. The final design must ensure that the resulting HESS shows an overall enhanced performance, providing the energy ratings of the main energy storage device, but simultaneously maintaining the power ratings of the fast-dynamics one. The management of the power flows in the system is generally implemented through power converters that enable synchronized control and operation of the involved storage units.

The main objective of the research conducted along this work is to propose, analyze, compare and test different solutions to provide an adequate system performance during the

most relevant system operation modes. Each solution considers jointly the design of the power topology of the electronic converter and the control strategy implemented to ensure the desired power flows, which depends as well on the operation modes in the system. The operating conditions considered for the microgrid include both a grid-connected operation mode and an islanding operation mode. The performance of the system upon faults is also covered, as a fault ride through capability is one of the key system requirements. The main target of the control stages is simultaneously to decrease the DC bus voltage variations and to perform a fast DC bus recovery upon fast, relatively large load variations. Also, the control strategy is aimed at increasing the system reliability and robustness.

In order to achieve this main goal, a set of objectives have been established in next section. Then, the methodology for the fulfillment of these objectives is discussed, and finally, the structure of the PhD thesis is outlined.

1.2 Objectives of the Research

In order to accomplish these main goals, a number of objectives have been identified. These objectives will be targeted along the following chapters, and its fulfillment will be assessed at the final stages of the document. The objectives can be expressed as:

- Definition of the system under study, its constraints in terms of applications, power levels, voltage ratings and its expected performance and behavior.
- Characterization of the state-of-the-art of HESS for DC microgrids and nanogrids.
- Definition of the power electronic topologies suitable for HESS in DC microgrids and nanogrids, and selection of the base case topology.
- Analysis of the main healthy operating conditions of the HESS. Definition of the operation modes: islanding operation and grid-connected operation.
- Study of the control schemes for the HESS in the baseline case, for every operation mode. Definition of the control strategies: islanding control strategy, independent control strategy, and full control strategy.

- Analysis of the operating limitations of the baseline case for the voltage rating constraints.
- Proposal of contributions for dealing with issues related to voltage rating constraints.
- Analysis and operating issues of the HESS upon DC bus short-circuit fault conditions.
- Proposal of contributions for fault ride-through operation of the system.
- Establishment of a design methodology for validation and implementation of the proposed solutions.
- Validation of the proposed solutions through the simulations and the experimental test in laboratory prototypes.
- Critical analysis of the conclusions and establishment of future developments.

1.3 Methodology of the Research

The undertaken methodology starts by a revision of state-of-the-art solutions for the implementation of HESS in DC microgrids, considering, among other aspects, the storage technologies, the power topologies issues, the control methods and strategies, and the operation in healthy and faulty conditions of the microgrid. Then, a comparison of the main technologies, topologies and control strategies is carried out, in order to establish a baseline case that will be the basis of the research carried out onwards. The performance of this baseline case will be assessed in all the operating modes, conditions and control strategies. Also, the limitations of this baseline will be deeply analyzed, and the critical aspects of the operation will be identified.

Feasible alternate proposals will be presented then, in order to overcome the identified limitations of the baseline case, and these proposals will be theoretically analyzed for all the operation modes and strategies required. This methodology allows for performing a critical comparison of the performance of the proposed solutions against the baseline case.

So as to evaluate the feasibility of the proposal, these solutions must be assessed and validated. In order to do so, a design procedure, for a given set of conditions and constraints, for both the baseline case and the proposed solutions, will be carried out. This design method will be refined by the assessment of the system's performance by means of simulations, that will include complex models of the elements and devices in the system. And finally, these results will be compared against experimental results on a laboratory prototype of the HESS system, with the same conditions and constraint of the design and simulation results.

After that, a critical analysis of the conclusions derived from the research will be carried out. The degree of fulfillment of the objectives settled above will also be discussed in the final Chapter of the document.

1.4 Structure of the Thesis

The following shows the structure of the PhD thesis, intended for fulfilling the established objectives by means of the implementation of the discussed methodology.

Chapter 2 introduces and clearly defines the scope and framework of the research conducted in this work. The DG paradigm is discussed, and the concept of microgrid and nanogrid is briefly presented. It also explains the ESS in power systems, classifying the different technologies as a function of the main relevant technical parameters. By the study of the difference of these parameters for various devices, the concept of HESS is introduced and justified. Finally, this chapter carries out a study and comparison of HESS structures for interfacing the storage units to the DC bus at DC microgrids and nanogrids. The final hybrid storage system is formed by an electrochemical Lithium-Ion (Li-Ion) battery and a supercapcitor.

After that, **Chapter 3** studies the most relevant topologies for power electronic converters applied to HESSs. Several options for three-port circuits are evaluated when interfacing a DC bus with two distinct electrical energy storage units. Firstly, the most significant candidate options for non-isolated power electronics topology configurations in microgrids and nanogrid applications are selected. From this study, a baseline solution for a three-port bidi-

rectional converter for implementing HESS in DC microgrids is established. This topology, based on the bidirectional DC/DC buck converter, is deeply analyzed. This chapter also defines the operation modes of the HESS, i.e., the islanding mode and the grid-connected mode. Finally, in this chapter, the implementation of two distinct control strategies for the HESS is also described. These control strategies are the islanding control strategy (that keeps the DC bus voltage constant), the independent control strategy (which, in turn, considers the storage subsystem as an autonomous control scheme) and the full control strategy (that takes into consideration also the references for the grid interfacing converter of the microgrid).

The major drawbacks of the baseline solution are described in **Chapter 4**. In order to cope with the limitations due to high voltage mismatch in the storage devices ratings, a novel scheme for implementing a non-isolated solution for interfacing the ESS devices to the DC bus is proposed. Then, a critical comparison is carried out among the two main possibilities: the first one based on Parallel Connection (PC) of independent bidirectional buck converters for each device, the second one based on the Series-Parallel Connection (SPC) of the storage units. The proposed SPC is particularly useful in case of a large voltage mismatch between one of the ESS units and the DC bus.

Then, the basic control strategies (islanding control, independent control and full control) are discussed at both operation modes of the microgrid (islanding mode and grid-connected mode). This allows to compare the performance of the proposed solution against the baseline option, considering static aspects, such as gain limitations, efficiency or power density, but also regarding the dynamic behavior. The resulting structure is thoroughly compared against the most significant direct alternatives. The analysis carried out on the switching and conduction losses in the power switches of the target solution states the design constraints at which this solution shows a performance improvement. This work demonstrates how the proposed structure, referred to as SPC, performs as a simple, compact and reliable approach, based on a modification of the H-bridge configuration. The main advantage of this solution is that a sufficient large voltage gain, to some extent, at one of the ports is attained by means of a simple topology, preventing the use of multilevel or galvanic-isolated power stages. As a conclusion, the SPC shows a better performance in

terms of reliability and controllability in the target application of compensating grid or load variations in non-isolated HESSs, with a significant mismatch in the storage device voltage ratings.

After that, **Chapter 5** presents a fault ride-through control scheme for a non-isolated power topology used in a HESS designed for DC microgrids and nanogrids. The power topology under consideration is based on the buck-boost bidirectional converter, and it is controlled through a bespoke modulation scheme in order to obtain low losses at nominal operating conditions. The modulation scheme is based on two triangular carriers: one for the boost mode operation and the other for the buck operation mode. In addition, the operation of the proposed control scheme during a DC bus short-circuit failure is also shown, as well as a modification to the standard control in order to achieve fault ride-through capability once the fault is over.

Chapter 6 is devoted to establish the design procedure for implementing the different solutions proposed in the previous chapters. It includes the design of the HESS, the power converters, and the control strategies.

The feasibility and validity of the topologies and the control schemes during both islanding mode and grid-connected mode are validated in **Chapter 7**, through simulations using MATLAB/SIMULINK® and PLECS®.

At **Chapter 8**, the theoretical and simulation results are compared against experimental validations carried out on a 10 kW laboratory prototype, in order to assess the validity of the results and to demonstrate the feasibility of all the proposed topologies and control schemes during the design conditions.

Finally, **Chapter 9**, carries out a critical analysis of the performance of the proposed solutions, stating its benefits as well as its main limitations. Finally, the main contributions of the work are summarized, establishing future developments in the research.

As a consequence of the research carried out for the PhD thesis, several publications in indexed international journals and prestigious international conferences have been published. These publications are listed and included in the work as annexes.

Capítulo 1

Esquema de la investigación, Objetivos, Metodología y Estructura

Contents

1.1 Resumen de la Tesis Doctoral

Esta tesis doctoral se enmarca dentro del ámbito de la ingeniería eléctrica, específicamente en las disciplinas de sistemas eléctricos de potencia, electrónica de potencia y sistemas de control. Los desarrollos más recientes en nuevas tecnologías de convertidores y dispositivos de almacenamiento de energía, junto con los avances en estrategias y sistemas de control, están liderando una revolución tecnológica para impulsar el crecimiento del paradigma de la Generación Distribuida (DG, por sus siglas en inglés) en redes de potencia eléctrica. Este paradigma se basa en la integración de recursos distribuidos en los sistemas

eléctricos de transmisión y distribución, con el fin de maximizar la eficiencia energética de toda la red eléctrica.

El esquema convencional de generación centralizada de sistemas de potencia asume la operación de líneas de transmisión y distribución de corriente alterna (AC, por sus siglas en inglés), para enviar la energía eléctrica desde grandes centrales de generación hacia las instalaciones de red de CA a los usuarios y consumidores finales. Además, suele implicar que estos usuarios son siempre consumidores de energía. Sin embargo, a medida que aumenta la penetración de los sistemas de energía renovable en la red, que las cargas electrónicas en las instalaciones de los usuarios resultan cada vez más relevantes, y que el almacenamiento de energía comienza a ser une opción técnicamente viable, los requisitos de coordinación y la complejidad del sistema eléctrico completo aumentan significativamente. Las microrredes y las nanorredes surgen como una solución que facilita la gestión de la energía a nivel local, permitiendo una integración sin fisuras de los recursos renovables y distribuidos. En particular, las microrredes o nanorredes de corriente continua (DC, por sus siglas en inglés) y las híbridas (AC/DC) se están convirtiendo en una opción viable para aumentar la eficiencia general de las redes eléctricas modernas.

Como ya se ha mencionado, los sistemas de almacenamiento de energía (ESSs, por sus siglas en inglés) se están convirtiendo en una de las tecnologías clave en las disciplinas relacionadas con la electrónica de potencia. De hecho, mediante el uso de estos sistemas, se ha reportado una mejora en el rendimiento de aplicaciones tales como la integración en la red de distribución de generadores eléctricos estocásticos, la estabilidad de la red y el apoyo a la calidad de la energía en contingencias en línea, la gestión de cargas de alta potencia de dinámica rápida en el tren de potencia de vehículos eléctricos híbridos, entro otras. En general, se trata de un amplio abanico de aplicaciones industriales con un perfil de carga de grandes características transitorias.

Un caso particular de estos sistemas son los Sistemas Híbridos de Almacenamiento de Energía (HESS, por sus siglas en inglés). En términos generales, estos HESS interconectan un dispositivo de almacenamiento de alta potencia de dinámica rápida, además de una unidad de almacenamiento de energía a granel más lenta, con el sistema de alimentación original. El diseño del sistema híbrido completo implica la definición de las

especificaciones de potencia y energía adecuadas en sus elementos y dispositivos, así como el diseño de un esquema de control que gestione adecuadamente los flujos de potencia involucrados. El diseño final debe asegurar que el HESS resultante muestre un rendimiento global mejorado, proporcionando las especificaciones de energía del dispositivo de almacenamiento de energía principal, pero manteniendo simultáneamente las especificaciones de energía del dispositivo de dinámica rápida. La gestión de los flujos de potencia en el sistema se realiza generalmente a través de convertidores de potencia que permiten el control y funcionamiento sincronizado de las unidades de almacenamiento implicadas.

El objetivo principal de la investigación realizada a lo largo de este trabajo es proponer, analizar, comparar y probar diferentes soluciones para proporcionar un rendimiento adecuado del sistema durante los modos de operación más relevantes. Cada solución considera conjuntamente el diseño de la topología de potencia del convertidor electrónico y la estrategia de control implementada para asegurar los flujos de potencia deseados, lo que también depende de los modos de operación del sistema. Las condiciones de funcionamiento consideradas para la microrred incluyen tanto un modo de funcionamiento conectado a la red como un modo de funcionamiento en isla. También se ha considerado el comportamiento del sistema en caso de fallo, ya que la capacidad de robustez ante este tipo de fallos es uno de los requisitos clave del sistema. El objetivo principal de las etapas de control es simultáneamente disminuir las variaciones de tensión del bus de CC y realizar una rápida recuperación del bus de CC ante variaciones de carga rápidas y relativamente grandes. Además, la estrategia de control tiene como objetivo aumentar la fiabilidad y robustez del sistema.

Para lograr este objetivo principal, se han establecido una serie de objetivos en la siguiente sección. A continuación, se discute sobre la metodología para el cumplimiento de estos objetivos y, finalmente, se esboza la estructura de la tesis doctoral.

1.2 Objetivos de la Investigación

Para alcanzar estas metas principales, se han identificado una serie de objetivos. El cumplimiento de estos objetivos se desarrollará a lo largo de los siguientes capítulos, y se

evaluará en las etapas finales del documento. Los objetivos pueden expresarse como:

- Definición del sistema estudiado, de sus limitaciones en términos de aplicaciones, niveles de potencia, valores nominales de tensión y de sus prestaciones y comportamiento esperados.
- Caracterización del estado del arte de HESS para microrredes y nanorredes de CC.
- Definición de las topologías de electrónica de potencia adecuadas para HESS en microrredes de CC y selección de la topología de un caso base.
- Análisis de las principales condiciones de operación sin fallo del HESS. Definición de los modos de operación: operación en isla y operación conectada a la red.
- Estudio de los esquemas de control del HESS en el caso base, para cada modo de operación. Definición de las estrategias de control: estrategia de control en isla, estrategia de control independiente y estrategia de control total.
- Análisis de los límites de funcionamiento del caso base en función de los márgenes de las tensiones nominales.
- Propuesta de contribuciones para solventar las limitaciones relacionados con las restricciones de la tensión nominal.
- Análisis y problemas de funcionamiento del HESS en caso de fallo por cortocircuito en el bus de CC.
- Propuesta de aportaciones para el funcionamiento del sistema en caso de fallo.
- Establecimiento de una metodología de diseño para la validación e implementación de las soluciones propuestas.
- Validación de las soluciones propuestas a través de simulaciones y ensayos experimentales en prototipos de laboratorio.
- Análisis crítico de las conclusiones y establecimiento de futuros desarrollos.

1.3 Metodología de la Investigación

La metodología emprendida se inicia con una revisión del estado del arte, focalizada en las soluciones de última generación para la implementación de HESS en microredes de CC. Se consideran, entre otros aspectos, las tecnologías de almacenamiento, los problemas de topologías de potencia, los métodos y estrategias de control, y la operación en condiciones en condiciones normales y ante fallos en la microrred. A continuación, se realiza una comparación de las principales tecnologías, topologías y estrategias de control, con el fin de establecer un caso de base que será la base de la investigación llevada a cabo. El desempeño de este caso base será evaluado en todos los modos de operación, condiciones y estrategias de control. Asimismo, se analizarán en profundidad las limitaciones de este caso base y se identificarán los aspectos críticos de funcionamiento.

A continuación se presentan propuestas alternativas viables para superar las limitaciones identificadas en el caso de línea de base, y estas propuestas serán analizadas teóricamente para todos los modos de operación y estrategias requeridas. Esta metodología permite realizar una comparación crítica del desempeño de las soluciones propuestas con el caso base.

Para evaluar la viabilidad de la propuesta, estas soluciones deben ser probadas y validadas adecuadamente. Para ello, se llevará a cabo un procedimiento de diseño, para un conjunto dado de condiciones y limitaciones, tanto para el caso de referencia como para las soluciones propuestas. Este método de diseño se refinará mediante la evaluación del rendimiento del sistema mediante simulaciones, que incluirán modelos complejos de los elementos y dispositivos del sistema. Y finalmente, estos resultados serán comparados con los resultados experimentales en un prototipo de laboratorio del sistema HESS, con las mismas condiciones y restricciones de los resultados de diseño y simulación.

Posteriormente, se realizará un análisis crítico de las conclusiones derivadas de la investigación. El grado de cumplimiento de los objetivos fijados anteriormente también se discutirá en el capítulo final del documento.

1.4 Estructura de la Tesis Doctoral

A continuación se muestra la estructura de la tesis doctoral, destinada al cumplimiento de los objetivos establecidos mediante la implementación de la metodología discutida.

El capítulo 2 introduce y define claramente el alcance y el marco de la investigación realizada en este trabajo. Se discute el paradigma de la generación distribuida y se presenta brevemente el concepto de microrred y nanorred. También detalla el uso de sistemas de almacenamiento de energía en los sistemas de potencia, clasificando las diferentes tecnologías en función de los principales parámetros técnicos relevantes. Mediante el estudio de la diferencia de estos parámetros para varios dispositivos, se introduce y justifica el concepto de HESS. Finalmente, este capítulo realiza un estudio y comparación de las estructuras HESS para la interconexión de las unidades de almacenamiento con el bus de CC en microrredes y nanorredes de CC. El sistema de almacenamiento híbrido final está formado por una batería electroquímica de iones de litio (Li-Ion, por sus siglas en inglés) y un módulo de Supercondensadores.

A continuación, en textbfel capítulo 3 se estudian las topologías más relevantes para los convertidores electrónicos de potencia aplicados a los HESS. Se evalúan varias opciones para circuitos de tres puertos, necesarios para interconectar un bus de CC con dos unidades de almacenamiento de energía eléctrica distintas. En primer lugar, se seleccionan las opciones más significativas para configuraciones de topología de electrónica de potencia no aislada en microgrids y aplicaciones de nanogrid. A partir de este estudio, se establece una solución base para un convertidor bidireccional de tres puertos para la implementación de HESS en microrredes de CC. Esta topología, basada en el convertidor bidireccional CC/CC reductor, se analiza en profundidad. En este capítulo también se definen los modos de funcionamiento del HESS, es decir, el modo aislado y el modo conectado a la red. Finalmente, en este capítulo también se describe la implementación de dos estrategias de control distintas para el HESS. Estas estrategias de control son la estrategia de control en isla (que mantiene constante la tensión del bus de CC), la estrategia de control independiente (que, a su vez, considera el subsistema de almacenamiento como un esquema de control autónomo) y la estrategia de control completo (que tiene en cuenta también las

referencias para el convertidor de interconexión a la red de la microrred).

Los principales inconvenientes de la solución base se describen en **el Capítulo 4**. Para hacer frente a las limitaciones debidas a la gran diferencia de tensión nominal en los dispositivos de almacenamiento, se propone un nuevo esquema para implementar una solución no aislada para interconectar los dispositivos ESS con el bus de CC. A continuación, se realiza una comparación crítica entre las dos posibilidades principales: la primera basada en la Conexión Paralela (PC, por sus siglas en inglés) de convertidores bidireccionales independientes para cada dispositivo, y la segunda basada en la Conexión Serie-Paralelo (SPC, por sus siglas en inglés) de las unidades de almacenamiento. El SPC propuesto es particularmente útil en caso de un gran diferencia de tensión nominal entre una de las unidades ESS y el bus de CC.

A continuación, se discuten las estrategias de control básicas (control en isla, control independiente y control total) en ambos modos de funcionamiento de la microrred (modo isla y modo de conexión a la red). Esto permite comparar el rendimiento de la solución propuesta con la opción base, considerando aspectos estáticos, tales como limitaciones de ganancia, eficiencia o densidad de potencia, pero también con respecto al comportamiento dinámico. La estructura resultante se compara minuciosamente con las alternativas directas más significativas. El análisis de las pérdidas en conmutación y en conducción en los interruptores de potencia de la solución de destino indica las limitaciones de diseño en las que esta solución muestra una mejora del rendimiento. Este trabajo demuestra cómo la estructura propuesta, denominada SPC, funciona como una alternativa simple, compacta y fiable, basada en una modificación de la configuración de puente en H. La principal ventaja de esta solución es que se consigue una ganancia de tensión suficientemente grande, hasta cierto punto, en uno de los puertos mediante una simple topología, evitando el uso de etapas de potencia multinivel o aisladas galvánicamente. Como conclusión, el SPC muestra un mejor rendimiento en términos de fiabilidad y controlabilidad en la aplicación objetivo de las variaciones de la red de compensación o de la carga en los HESS no aislados, cuando existe gran diferencia en los parámetros de tensión nominales de los dispositivos de almacenamiento.

Después de eso, **el Capítulo 5** presenta un esquema de control de fallo para una topología

de potencia no aislada usada en un HESS diseñado para microrredes y nanorredes de CC. La topología de potencia considerada se basa en el convertidor bidireccional reductor-elevador, y se controla mediante un esquema de modulación a medida para obtener bajas pérdidas en condiciones nominales de funcionamiento. El esquema de modulación se basa en dos portadoras triangulares: una para el modo de operación elevador y otra para el modo de operación reductor. Además, también se muestra el funcionamiento del esquema de control propuesto durante una fallo por cortocircuito en el bus de CC, así como una modificación del control estándar para lograr la capacidad de rearme del sistema una vez finalizado el fallo.

El capítulo 6 está dedicado a establecer el procedimiento de diseño para implementar las diferentes soluciones propuestas en los capítulos anteriores. Incluye el diseño del HESS, los convertidores de potencia y las estrategias de control.

La viabilidad y validez de las topologías y los esquemas de control durante el modo en island y el modo conectado a la red se validan en textbfel Capítulo7, mediante simulaciones utilizando MATLAB/SIMULINK® y PLECS®.

En **el Capítulo 8** se comparan los resultados teóricos y de simulación con las validaciones experimentales realizadas en un prototipo de laboratorio de 10 kW, con el fin de evaluar la validez de los resultados y demostrar la viabilidad de todas las topologías y esquemas de control propuestos durante las condiciones de diseño.

Finalmente, en **el Capítulo 9**, se realiza un análisis crítico del desempeño de las soluciones propuestas, exponiendo sus beneficios, así como sus principales limitaciones. Finalmente, se resumen las principales aportaciones del trabajo, estableciendo los desarrollos futuros de la investigación.

Como consecuencia de la investigación realizada para la tesis doctoral, se han publicado varias publicaciones en revistas internacionales indexadas y prestigiosas conferencias internacionales. Estas publicaciones se enumeran y se incluyen en el trabajo como anexos.

Chapter 2

A Review of Energy Storage Systems for DC Microgrids

Contents

2.1 Introduction

This chapter explains and defines the different types of microgrids that can be found in the DG paradigm, attending to the nature of the electrical characteristics, i.e., pure AC microgrids, pure DC microgrids, and hybrid AC/DC microgrids. Also, it illustrates the different types of ESS for this kind of microgrids. Finally, it is focused on the review of state-of-the-art for the HESSs in microgrids.

2.2 The Concept of Microgrid

A microgrid is a power grid subsystem with DG capabilities which can operate detached from the main distribution grid, in an isolated mode. However, in most cases these subsystems operate in a grid-tied mode, enabling net power flows with the distribution network. The essential elements within a microgrid are the loads and the generation systems, either dispatchable generators or Renewable Energy Sources (RESs). The most significant share of RES in microgrids are based on solar Photovoltaic (PV) or Wind Turbines (WTs)

generation. Both sources rely on natural phenomena such as solar irradiance or wind speed. With the increasing penetration of the RESs, the stability and the reliability of the microgrid are affected [1, 2]. However, the continuous development of ESSs [3, 4], balances the stochastic behavior of both the RESs and the power demanded at the microgrid, ensuring an uninterrupted and stable power flow to the loads [5–7]. The microgrid is connected to the grid through the Point of Common Coupling (PCC) by means of Power Electronic Converters (PECs) [8–10]. The microgrid could be an AC microgrid, a DC microgrid or even a hybrid AC/DC microgrid [6, 10–18]. In an AC microgrid (Figure 2-1), the AC loads or generators are connected directly to the AC bus, or through AC/AC converters (e.g., speed drives for AC machines), while the DC units (either sources or loads) are interfaced to the AC bus through DC/AC converters. On the other hand, in DC microgrids (Figure 2-2), these AC units are connected to the DC bus through AC/DC converters, while the units with DC power are connected directly to the DC bus or, more generally, through DC/DC converters. Finally, in a hybrid microgrid (Figure 2-3), there are two buses for AC and DC for units with AC power and DC power, respectively. The power exchange is ensured through a given number of bidirectional AC/DC converters.

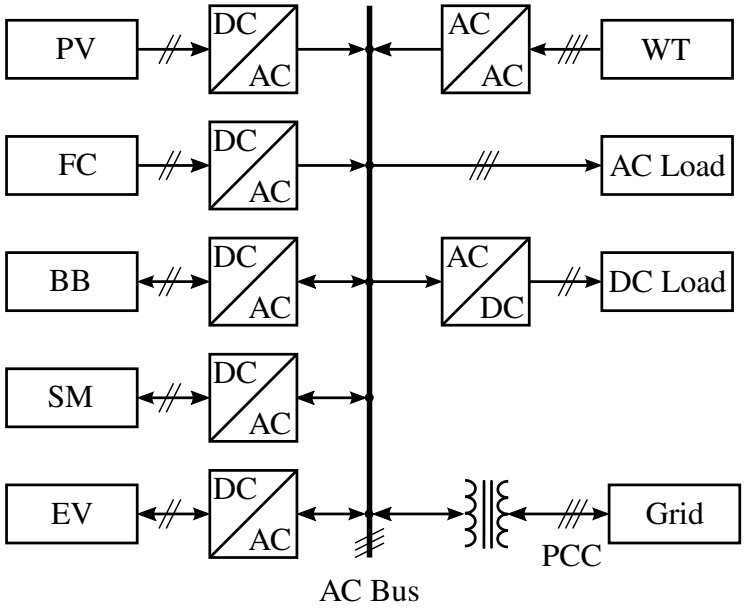


Figure 2-1: An AC microgrid.

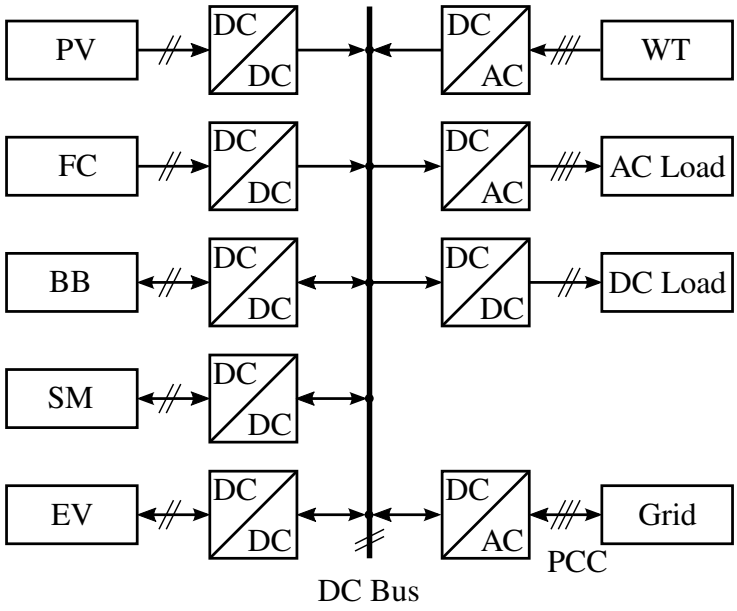


Figure 2-2: A DC microgrid.

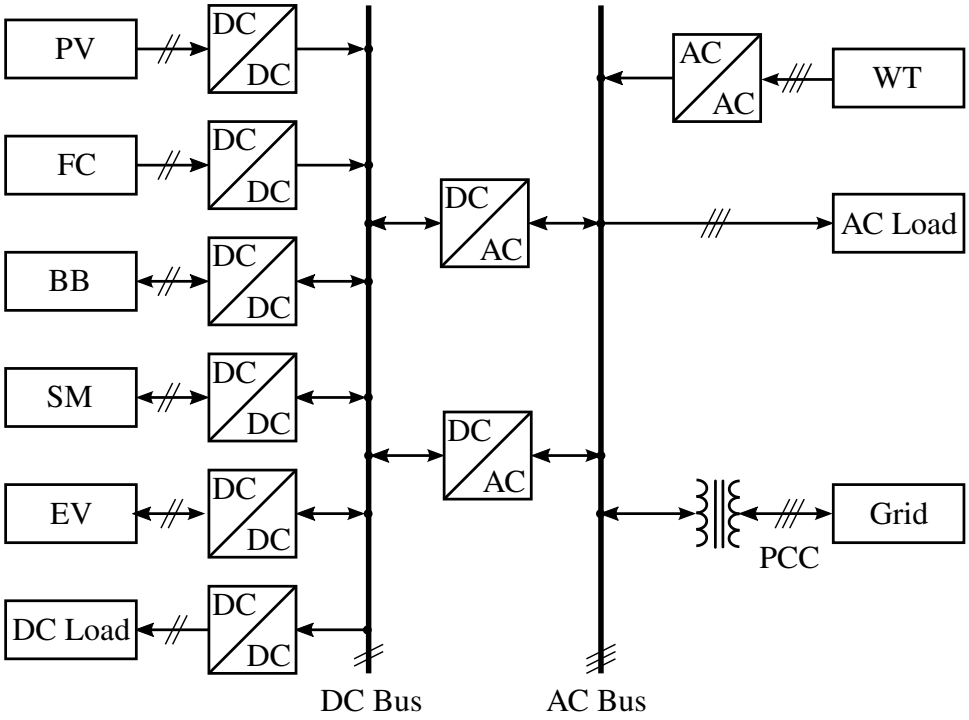


Figure 2-3: A hybrid microgrid.

Given the increasing number of DC units in power systems, there is a general perception in the technical literature that assumes the development of DC microgrids as a vital tool for increasing the efficiency, stability, and reliability of microgrids[1, 2, 15, 19]. This perception is based on several facts to be considered simultaneously. Currently, an increasing number of the AC loads (and generators) are formed by some multi-stage electronic converter structure. This structure generally is based on a cascaded connection of an AC/DC rectification stage and a DC/AC inverter. In DC microgrids, one of these stages may be removed, or at least substituted by a DC/DC converter, which usually has better efficiency than the original stage. DC units, analogously, require an AC/DC stage for interfacing with AC grids, that can be removed (or simplified by a DC/DC stage) in the case of DC microgrids. In any case, the grid frequency synchronization concerns at AC grids are not present in the case of DC microgrids; this issue also simplifies in a significant manner the control stages of the interfacing converters in DC grids [15, 19].

2.3 Benefits and Applications of Energy Storage Systems

The following deals with the benefits of integrating ESS in electrical power systems. This discussion aims to demonstrate how these ESS play a key supporting role in the performance of electric systems. Even though these benefits are valid from large-scale generation down to the end-user applications, in particular, the benefits of ESS in microgrids are targeted here [20–22]:

- From the point of view of the generation, ESS allow for:
  - Maintaining uninterrupted and stable power flow to the loads [5–7, 23]: Due to the penetration of renewable generation sources, ESS is needed to provide power when the renewable sources are not able to supply energy to the system.
  - Providing peak shaving/load leveling [1, 22, 24–27]: The ESSs enables the system to store the surplus energy during the light load and low price of energy periods and to provide the required energy at heavy load intervals and high price periods.

  - Giving support for black-start and reduce the risk of blackouts [1, 2, 22]: The black-start occurs when the system needs to be restarted after a blackout (collapse of failure or large power outage). It has been reported how some specific technologies (e.g., electrochemical batteries and supercapacitors) have the capability of achieving such restoring feature [28].
  - Enabling the use of mobile/remote applications [28]: It provides power for remote areas or stand-alone systems such as electric vehicles and portable devices.

- At transmission level, ESS provides for:

  - Possibility if postponement of infrastructure upgrades and congestion relief [20]: The usage of ESS reduces the need for new investments in order to have a suitable transmission capacity.
  - Voltage Regulation [21]: ESS allows for stabilizing the voltage levels between each end of the power lines in the system.

- Finally, at the distribution level and end-user services, the implementation of ESS yields to:

  - Improving the power quality [1, 20, 23–25, 29–31]: In order to effectively minimize the effects of power quality issues (instantaneous voltage drop, transients and flicker, sag, swell and harmonics), it is required a fast response of the ESS. Supercapacitors, superconducting magnetic storage system and flywheel have a very fast response, within the range of milliseconds. These dynamics are followed by the performance of batteries, with characteristic responses in the order of seconds [28].
  - Increasing reliability [20, 24, 25]: ESSs support customer loads in the case of the loss of the total power.
  - Providing voltage support [25]: Maintain the voltage within an acceptable range.

- Postponement of infrastructure upgrades [20]: Utilizing ESS reduce the need for new investments in order to have suitable distribution capacity to meet load demands.
- Ride-through support [25]: ESS can provide energy to ride-through operation after disconnection due to a fault in the system and fault clearance.

In order to determine the optimal ESS technology for a given application, the requirements in terms of minimum response time and minimum discharge time need to be characterized. Table 2.1 shows the minimum response time needed and the minimum discharge duration of for key applications of the ESSs [20, 29]:

Table 2.1: The minimum response time and discharge time of the applications of the ESS

Applications of ESS	Minimum Response Time	Minimum Discharge Duration
Generation		
Uninterrupted and stable power flow	sec.	10 min. - 2 hr.
Peak shaving	min. - hr.	sec. - 10 hr.
Black-start	sec. - min.	1 h - 6 hr.
Mobile applications	ms - sec.	sec. - hr.
Transmission		
Postponement of infrastructure upgrades	min.	1 hr. - 6 hr.
Voltage regulation	ms - sec.	6 min. - 1 hr.
Distribution and end-user services		
Power quality	< 5 ms	ms - 1.2 min.
Reliability	5 ms - sec.	5 min. - 5 hr.
Voltage support	< 5 ms	15 min.
Postponement of infrastructure upgrades	min.	2 hr. - 8 hr.
Ride-through support	< 5 ms	10 sec. - 15 min.

2.4 Energy Storage Systems Technologies

In this section, a summarized review of the different ESS technologies suitable for electrical system applications is carried out. Depending on the physical form in which the energy is stored, a first classification can be established [20, 29, 32–34]:

1. Mechanical Energy Storage System: The energy is stored in the form of kinetic or potential energy.
   (a) Kinetic Energy Storage System:
      i. Flywheel Energy Storage System (FESS) [1, 2, 17, 30, 31, 35–38].
   (b) Potential Energy Storage System:
      i. Compressed Air Energy Storage System (CAESS) [1, 2, 17, 30, 31, 35–38].
      ii. Pumped Hydro Energy Storage System (PHESS) [1, 2, 17, 30, 31, 35, 37, 38].
2. Electrical Energy Storage System: The energy is stored in the form of electrostatic or magnetic fields.
   (a) Electrostatic Energy Storage System:
      i. Conventional capacitors [2, 35].
      ii. Supercapacitors [1, 2, 17, 30, 31, 37, 38].
   (b) Magnetic Energy Storage System:
      i. Superconducting Magnetic Energy Storage System (SMESS) [1, 2, 17, 30, 31, 36, 37].
3. Chemical Energy Storage System: Energy can be stored and recovered when some chemical substances are subjected to a transformation through a chemical reaction. The main chemical technologies for energy storage are:
   (a) Fuel Cells (FCs) [36, 37].
   (b) Hydrogen Energy Storage System (H_2ESS) [1, 30, 38].
   (c) Synthetic Natural Gas (SNG) [1, 37, 39].
4. Electrochemical Energy Storage System: This can be defined as a particular case of chemical energy storage, in which reversible chemical reactions in a combination of cells are used to store electrical energy. This combination of cells in batteries can be classified into:
   (a) Conventional rechargeable batteries [1, 2, 30, 35, 36, 38].
   (b) Liquid-metal and molten-salt batteries [40].
   (c) Metal-air batteries [40].
   (d) Flow batteries [2, 30, 37, 38].
5. Thermal Energy Storage System [1, 2, 30]: Heat is also a form of energy that can be used for electrical systems storage applications. Depending on the range of temperatures involved, two different sets of technologies can be identified:
   (a) Low-Temperature Thermal Energy Storage System (LTTESS) [31]:

   i. Aquiferous Low-Temperature Energy Storage System (ALTESS) [20, 21, 29].
   ii. Cryogenic Energy Storage System (CESS) [20, 21, 29].
(b) High-Temperature Thermal Energy Storage System (HTTESS) [31]:
   i. Molten Salt Storage (MSS) and Room Temperature Ionic Liquids (RTIL) [20, 21].
   ii. Concrete storage [21].
   iii. Phase Change Materials (PSMs) [21, 29].

Notice how some of these technologies are classified into different forms of energy depending on the technical literature references. The criterion followed in this classifications aims to simplify the definitions of the technologies involved.

On the other hand, these technologies can also be classified based on their storage characteristic duration into short-term ESS used for power quality, medium-term ESS used for grid congestion management and frequency response and long-term ESS used for supply and demand matching. [1, 2, 17, 20–22, 24, 29, 39, 41]. The following classification is thus carried out as a function of this characteristic time:

1. Short-term Energy Storage System (from seconds to minutes): The energy to power ratio is less than 1 (e.g., capacity of less than 1 kWh with a power of 1 kW system).
   (a) FESS.
   (b) Conventional capacitors.
   (c) Supercapacitors.
   (d) SMESS.
2. Medium-term Energy Storage System (from minutes to hours): The energy to power ratio is between 1 and 10 (e.g., a capacity between 1 kWh and 10 kWh for a 1 kW system).
   (a) Conventional Rechargeable batteries.
   (b) Liquid-Metal and Molten-Salt Batteries.
   (c) ALTESS.
   (d) CESS.
   (e) SNG.
3. Long-term Energy Storage System (from hours to days to months): The energy to power ratio is greater than 10 (e.g., capacity of greater than 10 kWh for a 1 kW system).

(a) CAESS.

(b) PHESS.

(c) Metal-air batteries.

(d) Flow batteries.

(e) FCs.

(f) H_2ESS.

(g) MSS and RTIL.

(h) Concrete storage.

(i) PSMs.

Figure 2-4 shows the rated energy capacity versus duration of storage of the different technologies of ESS [17, 22, 24, 29]. Again, this division into short, medium and large term scales depends mainly on the specific application, on the power and energy ratings involved, an also on the given criteria followed in the analysis carried out at the specific technical literature references. The categorization shown here aims to match the most general classifications studied.

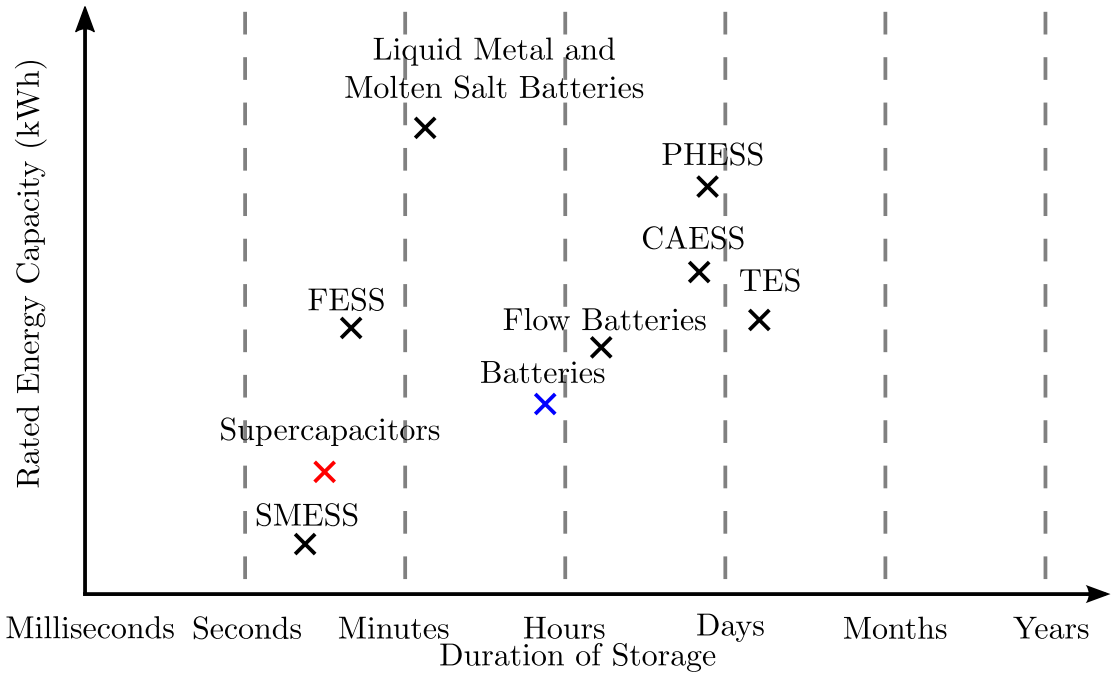


Figure 2-4: Rated energy capacity versus duration of storage.

2.4.1 Electrochemical Batteries

Electrochemical batteries stand out as one of the most commonly used storage technologies both in industrial and residential applications of power systems, microgrids and nanogrids [21, 29]. The energy and the power ratings of the electrochemical battery need to be sized to fulfill the peak power demands, as well as any backup requirements under islanding mode operation of the target application.

Given the inherent modular approach of the battery system, that indeed is formed by an assembly of cells and modules, the only limitation for finding a device with enough power ratings come from the cost or size/weight sides. In fact, increasing the size of the Battery Bank (BB) will solve the power rating requirements, apparently raising the cost as well.

The fundamental characteristic parameters used to define a battery are summarized ahead [42]:

- Nominal Voltage, V_{BB_nom}: Reference voltage of the BB, as per the conditions specified by the manufacturer. It is measured in Volts.

- Nominal Capacity, C_{BB_nom}: coulometric capacity, measured in Amperes-hour, available when the device is discharged at a given discharge current (generally specified as C-rate), from 100% state-of-charge to the cut-off voltage. The capacity generally decreases with increasing discharge currents.

- State of Charge, SOC_{BB}: The State of Charge (SoC) is a measure of the amount of electrical energy stored in BB [43]. The units of SoC are percentage points (0% = empty; 100% = full). An alternate form of the same measure is the Depth of Discharge (DoD), the inverse of SoC (100% = empty; 0% = full). SoC is normally used when discussing the current state of a BB in use, while DoD is most often seen when discussing the lifetime of the BB after repeated use.

- Discharge Current, C_{BB_rate}: A measure of the rate at which a BB is discharged, relative to its maximum capacity. A C-rate of 1C means that the discharge current will discharge the entire battery in 1 hour.

- State of Health, SOH_{BB}: The State of Health (SoH) of the BB is a figure of merit of the condition of a battery or a cell, compared to its ideal conditions. Typically, a battery's SOH_{BB} will be 100% at the time of manufacture and will decrease over time and use [44].

- Cycle Life: The number of discharge-charge cycles that the BB can suffer, before failing to meet specific performance criteria. This number of cycles is affected by the charge/discharge conditions, temperature, humidity, etc. Generally speaking, the higher the DoD, the lower the cycle life.

- Maximum Continuous Charge(Discharge) Current: Maximum current at which the BB can be charged (discharged) continuously. It is given by the manufacturer to limit dangerous charging/discharging rates.

- Maximum Voltage, V_{BB_max}: Also known as charge voltage, it is the voltage at which the device is charged to the full capacity.

- Float Voltage, V_{BB_fl}: The voltage at which the BB must be kept once charged to 100% SoC as to compensate for self-discharge.

- Internal Impedance, Z_{BB}: The impedance of the BB, generally different for charge and discharge, that accounts for internal losses and dynamic performance. This impedance is a function of parameters that state the BB condition, such as the SoH and the SoC.

- Specific Power and Specific Energy: The specific power, measured in W/kg, is the maximum available power per unit mass of the device. In turn, the specific energy (Wh/kg) is the nominal energy stored in the battery, at 100% SoC, per unit mass of the device.

- Power Density and Energy Density: The power density, measured in W/m^3, states the maximum available power per unit volume of the device, whereas the energy density defines the amount of energy stored per unit volume, in Wh/m^3.

The main limitation in the lifetime of the battery comes from the voltage mismatch at cell level within a given battery module. Passive or active cell balancing techniques are required for ensuring an even distribution of the voltages that maximizes the battery lifetime and SoH [45]. These devices are suffering from frequent charge and discharge cycles, in order to supply the instantaneous power requirements [46, 47]. Also, if the charge/discharge levels are greater than the rated ones, the lifetime of the battery is significantly jeopardized [48].

The thermal management of the batteries is a significant challenge to operate safely in high power demands. In fact, the batteries need to be adequately refrigerated in high-temperature environments, but in turn, they require warming-up in low-temperature environments, in order to provide the desired power in optimal conditions [49]. Generally speaking, the batteries have a limitation in the transient response (di/dt) [50] as large transient fluctuations might affect the device performance.

2.4.2 Classification of Electrochemical Battery Technologies

The batteries are widely used in power systems applications, being a quite mature, well-known technology ESS [23, 40]. The different implementations of such a BB can be classified attending to their general structure and operation principle.

1. Conventional Rechargeable Batteries: These batteries consists of: positive cathode, negative cathode, electrolyte and the separator. They are a mature technology and widely used in a lot of applications.

   (a) Li-Ion Battery [1, 2, 30, 31, 36, 49, 51, 52].

   (b) Lithium-Polymer (Li-Poly) Battery [49].

   (c) Lithium-Iron Phosphate ($LiFePO_4$) Battery [49].

   (d) Lead-Acid (Ph-Acid) Battery [1, 2, 31, 36, 49, 51, 52].

   (e) Nickel-Cadmium (NiCd) Battery [1, 2, 30, 31, 36, 52].

   (f) Nickel-Metal Hydride (NiMH) Battery [1, 2, 30, 36, 49, 51, 52].

   (g) Nickel–Zinc (NiZn) Battery [52].

(h) Nickel-Hydrogen (NiH_2) Battery.

(i) Nickel-Iron (NiFe) Battery [40].

(j) Zinc Silver Oxide (ZnAg) Battery [40].

(k) Alkaline Zinc-Manganese Dioxide (ZnMn) Battery [40].

2. Liquid-Metal and Molten-Salt Batteries: These batteries utilize liquid metal/molten salts as electrolytes which plays the part of electrodes. The electrodes are separated by a solid membrane separator. They are still not widely implemented in commercial applications.

   (a) Sodium-Sulfur (NaS) Battery [1, 2, 30, 31, 36].

   (b) Sodium Nickel Chloride (NaNiCl) also is known as (ZEBRA) Battery [1, 2, 21, 30, 31].

3. Metal-Air Batteries: These batteries replace the second electrode with an air electrode. At present, the technology is not mature enough for practical implementation in grid applications.

   (a) Zinc-air (Zn-Air) [21, 40].

   (b) Iron-Air (Fe-Air) [40].

4. Flow Batteries: The electrolytes in the battery contain dissolved active materials, that flow through the cell to generate electricity.

   (a) Vanadium Redox Flow Battery (VRFB) [1, 2, 30, 31].

   (b) Polysulfide-Bromide (PSB) Battery[1, 2, 20, 30, 31].

   (c) Zinc-Bromine (ZnBr) Redox Flow Battery [1, 2, 30, 31].

   (d) Zinc-Cerium (ZnCe) Redox Flow battery [40].

2.4.3 Characteristic Parameters of Batteries

The characteristics of the main battery technologies, regarding energy density, power density, specific energy, specific power, rated power and rated energy capacity are presented

in Table [20, 21, 29, 31–33, 36, 40, 40, 49, 53].

Table 2.2: Characteristics of batteries and supercapacitors.

Technology	Energy Density (Wh/L)	Power Density (W/L)	Specific Energy (Wh/Kg)	Specific Power (W/Kg)	Rated Power (MW)	Rated Energy Capacity (MWh)
Li-Ion	94-500	1300-10,000	30-300	8-2000	1-100	0.0004-25
Li-Poly	200	250-1000	130-200	1000 -2800	-	-
Pb-Acid	25-90	10-700	10-50	25-415	0-50	0.001-48
Ni-Cd	15-150	75-700	10-80	50-300	0-50	6.75
Ni-MH	38.9-350	7.8-588	30-120	6.02-1200	0.01	3
Ni-Zn	80-400	121.38	15-110	50-900	0.001-0.05	-
Ni-Fe	25-80	12.68-35.18	27-60	20.57-110	0-0.05	-
Zn-Ag	4.2-957	3.6-610	81-276	0.09-330	0.25	-
Zn-Mn	360-400	12.35-101.7	80-175	4.35-35	0-0.001	-
NaS	150-345	50-180	100-250	14.29-260	0.01-80	0.4-244.8
NaNiCl	108-200	54.2-300	85-140	10-260	0-53	0.12-5
Zn-Air	22-1673	10-208	10-470	60-225	0-1	5.4
Fe-Air	100-1000	250	8-109	18.86-146	0-0.01	-
VRB	10-70	0.5-33.42	10-75	31.3-166	0.03-50	2-60
PSB	10.8-60	1-4.16	10-50	-	0.001-100	0.06-120
ZnBr	5.17-70	1-25	11-90	5.5-150	0.001-20	0.05-50
Supercapacitor	1-35	40,000-120,000	0.05-85.6	5.44-100,000	0-5	0.0005

It can be seen from Table 2.2 that Li-Ion battery has better characteristics compared to other technologies of batteries [29]. Li-Ion batteries are increasing in the market due to they have a long cycle life, a high cell voltage, good low-temperature performance, good charge retention, high depth of charge [40].

Table 2.3 shows the response time and discharge time of the main ESS [1, 20, 21, 21, 22, 29, 39]in order to easily select the proper technology of ESS for the suitable application. Discharge time is the maximum power discharge duration. It depends on the depth of charge and operating conditions [37].

Table 2.3: The response time and discharge time of the ESS technologies.

ESS	Response Time	Discharge Time	Suitable Storage Duration
Mechanical Energy Storage System			
FESS	< 4 ms - min.	ms - 15 min.	s - min. (short-term)
CAESS	1 min. - 15 min.	30 sec. - days	hr. - months (long-term)
PHESS	sec. - min.	1 hr. - days	hr. - months (long-term)
Chemical Energy Storage System			
Li-Ion	ms	15 min. -8 hr.	min. - days (medium-term)
Ph-acid	< 5 ms	sec. - 10 hr.	min. - days (medium-term)
NiCd	ms	sec. - 8 hr.	min. - days (medium-term)
NiMH	ms	18 min. - 8 hr.	min. - days (medium-term)
NiZn	ms	18 min. - 8 hr.	min. - days (medium-term)
NaS	ms	sec. - 7 hr.	sec. - hr. (medium-term)
NaNiCl	ms	min. - 4 hr.	sec. - hr. (medium-term)
Zn-Air	ms	sec. - days	hr. - months (long-term)
VRFB	< 1 ms	sec. - ds	hr. - months (long-term)
PSB	20 ms	sec. - 10 hr.	hr. - months (long-term)
ZnBr	< 1 ms	sec. -10 hr.	hr. - months (long-term)
FC	ms - sec.	sec. - days	hr. - months (long-term)
hydrogen	ms - min.	sec. - days	hr. - months (long-term)
SNG	min.	hr. - days	Medium-term
Electrical Energy Storage System			
Conventional capacitors	< 5 ms	ms - 1 hr.	sec. - hr. (short-term)
Supercapacitors	< 5 ms	10 sec. - 1.2 hr.	sec. - hr. (short-term)
SMESS	17 ms	ms - 30 min.	min. - hr. (short-term)
Thermal Energy Storage System			
ALTESS	min.	1 hr. - 8 hr.	min. - days (medium-term)
CESS	sec.	1 hr. - 8 hr.	min. - days (medium-term)
HTTESS	sec.	1 hr. - days	min. - months (long-term)

2.4.4 Applications of the Lithium-Ion battery

From the technical literature and Tables 2.2 and 2.3, it can be said that the Li-Ion technology presents a great potential for many applications:

- At generation level:
  - Renewable energy smoothing and stable power flow to the loads[22].
  - Provide peak shaving [39].

  - Emergency supply [39].
  - Used in mobile applications such as electric vehicles [39].

- At transmission level:
  - Voltage regulation [22]

- At distribution level and end-user services and end user:
  - Improving the power quality [22, 39].
  - Increasing the service reliability (Customer backup) [22].
  - Distribution upgrade deferral [22].

2.4.5 Hybrid Energy Storage Systems

A battery system design means, basically, the selection of the final number of modules required, as well as their serial and/or parallel interconnection to ensure compliance with the storage specifications of the target application. However, because of the above discussion, a design that ensures the ability to provide the given power with the dynamics necessary for the application may be substantially greater than that required to ensure only the energy ratings. In this case, if the final design is taken as the one that guarantees the power levels of the application, the storage system will have a larger size, weight, and cost than in the case of the system that strictly guarantees the energy support [54]. On the other hand, if the design assures only the available energy required by the system, when surpassing the charge and discharge ratings and the current derivative values, the SoH of the storage device will be penalized, and thus the lifetime of the battery, and therefore of the full energy system, will be shortened. Summarizing, if the BB is sized only by energies, then the SoH might decrease rapidly, preventing lifespan. On the other hand, if the size of the BB is selected by power yields to extra costs and size in the storage system.

One of the options to solve this paradox is to propose an energy system consisting of two different device technologies, with complementary power and energy characteristics. Thus, the combined energy system, called HESS, presents the energy characteristics of one of the

devices, but the dynamic and power characteristics of the other one. In the case under study, the option chosen is to design the Li-Ion battery according to the energy specifications for the application, while an additional device is added to provide the necessary power, with the required dynamics [49]. Provided that the additional storage device meets some economic and volumetric constraints, this scheme would, in addition, decrease the cost and size of the resulting storage system. However, in any case, a correct design of the HESS will increase the SoH of the battery, therefore extending the lifespan of the storage system [3, 55].

In order to select the complementary technologies within a HESS, their performance must be compared according to their specific power and specific energy ratings, as well as according to the power and energy densities [29, 50, 56]. In general, the weight is not an issue in stationary grid utility applications; however, it is critical in transportation and aerospace applications. The volume, though, could be an issue in some grid utility applications. Figure 2-5 shows the characteristics behavior of the main ESSs technologies, with respect to the power and energy densities [29, 39, 57]. The higher the power and energy densities, the lower the volume.

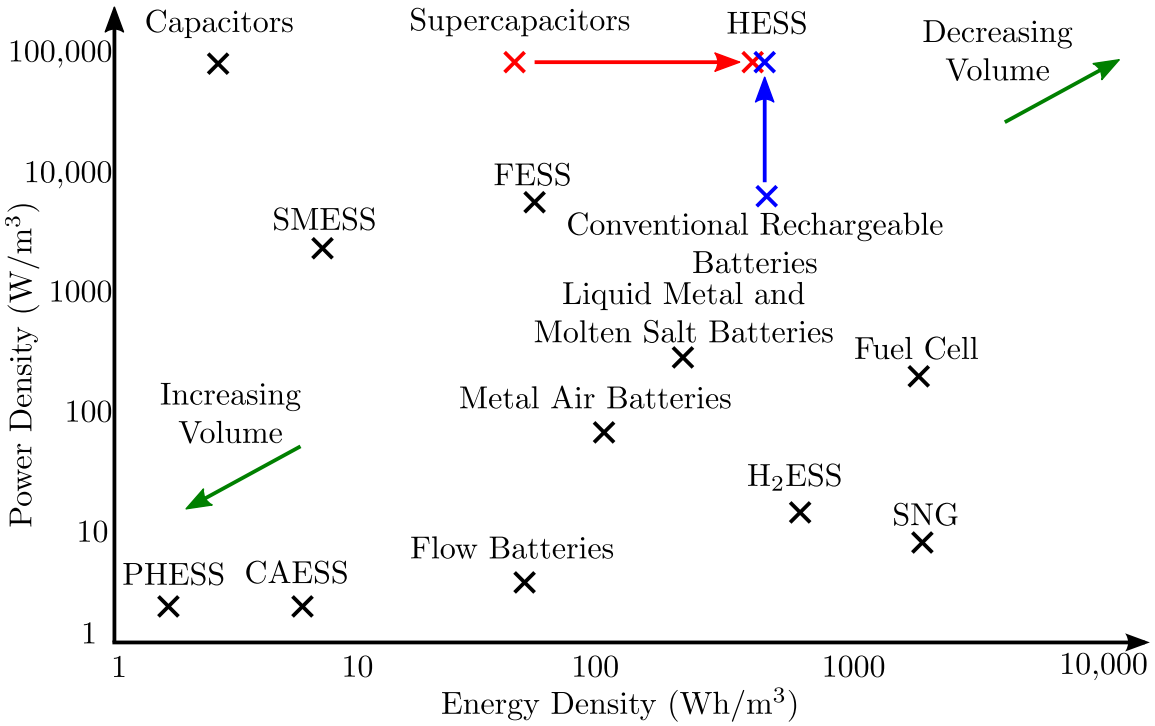


Figure 2-5: A comparison between the energy density and the power density for ESSs.

From figure 2-5, it can be seen how one of the technologies that may be hybridized with electrochemical batteries is the one based on supercapacitors (also known as ultracapacitors). The resulting HESS combines a main electrochemical battery ESS for high energy density with a characteristic relatively slow dynamics, while the auxiliary supercapacitor based ESS provides high power density and fast dynamics [36, 49, 51, 58, 59]. This combination improves the overall performance, increases the lifetime of the battery [49, 55, 60] and can achieve better efficiencies [51]. BB and Supercapacitor Module (SM) are one of the most widely used pairs of technologies in hybrid systems, given that the latter provide complementary characteristic ratings to the former in terms of power and energy densities [52, 61–64].

Transient fluctuations in the DC bus will occur upon changes in the operating conditions at the microgrid. These changes might be due to variations in the power flows, either due to variable load profiles or injection of power from DGs. Also, these changes might happen because of voltage variations in the distribution grid. Usually, the ESS used for energy supply in microgrids present limited dynamics, and large transient power spikes reduce their operating lifetime as in the case of BB [3]. In these cases, a fast, high-power capability storage system such as SM can be included, thus forming a HESS [3, 49, 51]. With an adequate coordinated control, these hybrid systems ensure a stiff behavior of the DC bus, decoupling the grid and the microgrid sides. But also, they enhance the system reliability by preventing the low-dynamic storage systems to provide large current spikes, increasing of the BB lifetime [65]. These HESS are gaining more and more research interest due to their potential benefits in power and energy support in grid applications [66]. The following subsection defines the main characteristics of supercapacitive technologies.

2.4.6 Supercapacitors

A supercapacitor, also is known as an ultracapacitor or Electric Double-Layer Capacitor (EDLC), is an electrical device able to store energy in an electric field, in a similar manner than standard capacitors [31, 67–69]. However, the level of capacitances reached by these devices is several orders of magnitude higher than in conventional capacitors [6, 36, 66, 70–73]. In general terms, these devices present faster dynamics, higher power density, high

charge and discharge ratings, and higher life cycling parameters (over 100,000 cycles) when compared to batteries [32, 73]. The energy stored in one SM is defined as:

$$E_{SM} = \frac{1}{2} C_{SM} \cdot V_{SM}^2 \tag{2.1}$$

where:

- E_{SM} is the SM energy storage in Joules or Watt-secs,
- C_{SM} is the SM capacitance in Farads,
- V_{SM} is the SM voltage in Volts.

This quadratic dependence of the energy versus the voltage in SM imposes some key design parameters. In order to deliver 75% of the stored energy in the SM, the SM is needed to discharge to half of its initial value [49].

The main characteristics of these devices are also included in Tables 2.2 and 2.3, for reference. In order to be able clearly to define the hybrid system, the following sections deal with a review of the main aspects of both the electrochemical batteries and the supercapacitors technologies.

2.4.7 Applications of the Supercapacitor

Following a review of the technical literature, a number of applications have been identified that uses the technology of supercapacitors in storage systems. These applications include:

- At generation level:
  - Centralized renewable energy integration (smoothing) [1].
  - Renewable generation grid integration [1].
  - Mobile applications such as transportation [1].
- At transmission level:

  - Voltage regulation [1].

- At distribution level and end-user services:

  - Improving power quality [1, 39].
  - Increasing reliability [1].
  - voltage regulation [1].
  - Transit and end ride-through capability (Bridging power). [1].

2.5 Configurations of the Hybrid Energy Storage Systems

As already mentioned, the technologies to be hybridized in the HESS under consideration are an electrochemical BB plus a SM, and both interfaced to a DC microgrid or nanogrid through PECs. There are many possible configurations in order to connect the main ESS (BB) and the auxiliary ESS (SM) to the DC microgrid/nanogrid. Usually, the hybrid system is connected to a DC bus that manages the power flow of the microgrid. These configurations depend on the voltage ratings and limit values of the BB (V_{BB}), the SM (V_{SM}), and the DC bus (V_{DC}). All the cases will be studied in order to give generality to the analysis; however, it will be assumed, for the establishment of the baseline case under consideration, that the SM voltage ratings are going to be significantly smaller than the BB voltage ratings.

2.5.1 The Basic Passive Parallel Configuration ($V_{BB} = V_{SM} = V_{DC}$)

In the most straightforward configuration, the BB and the SM are connected directly to the DC bus [49, 74] as depicted in Figure 2-6. Due to the behavior of the devices, the SM acts as a Low Pass Filter (LPF) [49]. The advantages of this configuration include no requirements of PECs, thus being very easy to implement [49]. The high transient current of the BB is avoided because of using the parallel scheme to connect the SM [61]. A drawback of this configuration is that it cannot effectively utilize the SM stored energy as

the working range of the SM is very small[49]. Besides, usually, a number of SM need to be connected in series in order to increase the operating voltage, thus yielding to a cost increase. Also, voltage balance mismatch effects might appear in the series connection of SM. However, the most significant drawback is that the power-sharing between the two ESS cannot be controlled [61].

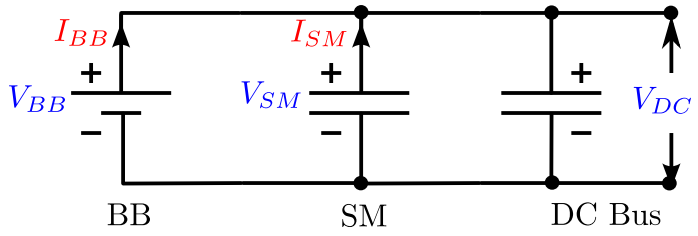


Figure 2-6: The BB and the SM are connected directly to DC bus.

2.5.2 The Passive Cascaded Configurations

This scheme, partly derived from the Basic Passive Parallel Configuration, includes a single bidirectional DC/DC converter. Depending on the relative voltage ratings of the BB, the SM and the DC bus, three different variants can be identified.

2.5.2.1 $V_{BB} = V_{SM}, (V_{BB}, V_{SM}) < V_{DC}$

In the case that the voltage ratings of the BB and the SM are similar and the ones at the DC are significantly different, the former devices can be connected directly in parallel, and, by means of a bidirectional DC/DC converter, they are also interfaced to the DC bus[36, 52, 62, 75]. As in the previous case, the advantage of this configuration is that high transient currents through the BB are prevented, as they flow through the SM. This ensures smooth current variations in the BB during charge and discharge, thus increasing the reliability of the system [61, 62]. An apparent drawback is that the power-sharing between the two ESS cannot be controlled, as the power contribution of each ESS depends on their respective internal resistances [49, 62]. Also, a bulk bidirectional DC/DC converter is needed to handle the total power of the full ESS, yielding to a cost investment increase, as compared to a direct connection. Also, it must be taken into account that the power flowing

from the ESSs has to flow through the bidirectional DC/DC converter, thus yielding to losses [61].

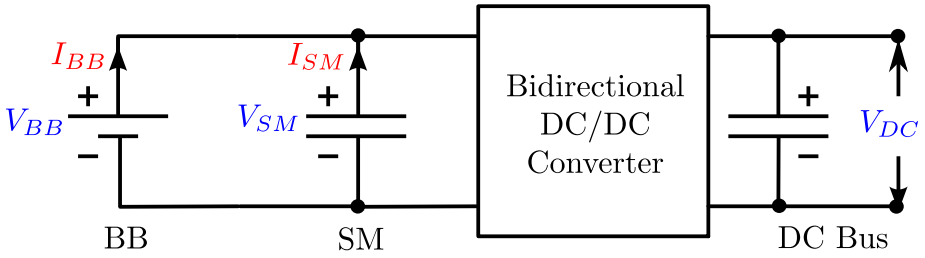


Figure 2-7: The BB and the SM are connected to a bidirectional DC/DC converter and then to the DC bus.

2.5.2.2 $V_{SM} < V_{BB}, V_{BB} = V_{DC}$

Assuming BB voltage ratings close to those at the DC, and also assuming that the SM ratings are significantly different. Then, a bidirectional DC/DC converter can be used to interface the SM and the DC bus, connecting the BB directly to the DC bus [36, 63, 64, 71, 74]. Figure 2-8 shows this configuration. The advantages of this scheme are the voltage of the SM can be utilized in a wide range, so the SM is efficiently used [49, 50]. The nominal voltage of the SM can be lower, and thus this might yield to a decrease the cost of the overall system. [49]. An additional advantage is that the voltage of the DC bus is relatively more stable [49]. The drawbacks of this configuration are that the BB still suffers from frequent charge and discharge operations and that the DC bus voltage cannot be controlled independently [49].

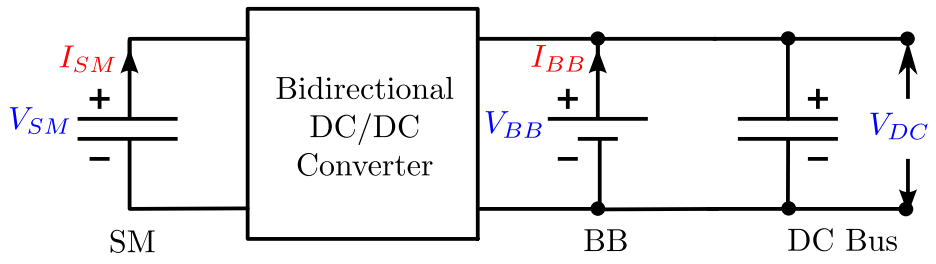


Figure 2-8: A bidirectional DC/DC converter is connected between the SM and the DC Bus, and the BB is connected directly to DC bus.

2.5.2.3 $V_{BB} < V_{SM}, V_{SM} = V_{DC}$

Finally, a bidirectional DC/DC converter can be connected between the BB and the DC bus. By designing an assembly of SM to present similar voltage ratings to the DC, the SM can be connected directly to the DC bus [36]. In this configuration, shown in Figure 2-9, the SM acts as a LPF. Thus, the main advantage of this configuration is that the BB current can be controlled, and therefore dangerous current and current derivative values are prevented, thus increasing the reliability of the device [49]. In addition, if the DC bus can be varied within a given range, the SM can be effectively used up to some extent [49, 61]. However, in general terms, this is also a drawback for this configuration, as usually the voltage of the DC bus cannot be varied over a large range [61]. In addition, it is generally required a series connection of a number of SM to match the DC bus voltage, often yielding to a non-optimal solution from the point of view of the cost.

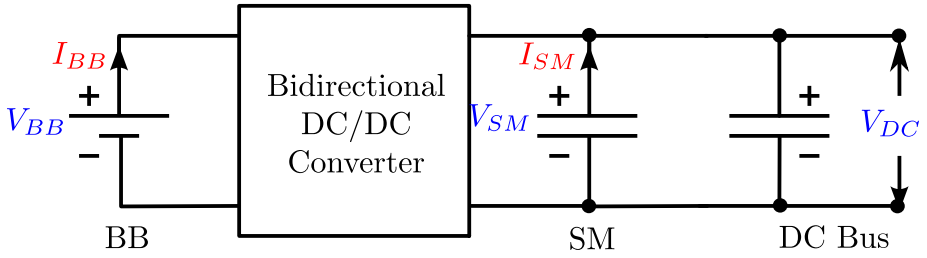


Figure 2-9: A bidirectional DC/DC converter is connected between the BB and the DC bus, and the SM is connected directly to the DC bus.

2.5.3 The Active Cascaded Configurations

In this configuration, there are two different possible structures, which in turn depend on the voltage ratings of the BB, the SM and the DC bus. For all these configurations, two bidirectional DC/DC converters are needed.

2.5.3.1 $V_{SM} < V_{BB} < V_{DC}$

A bidirectional DC/DC converter is connected between the SM and the BB and another bidirectional DC/DC converter is connected between the BB and the DC bus as shown in

Figure 2-10. The advantage of this configuration are that the voltage of the SM and the BB are varied in a vast range. The main drawback is that a bulk bidirectional DC/DC converter is needed to handle the total power of the ESSs, yields to increase the cost. All the energy storage has to flow through the bidirectional DC/DC converter connected to the DC bus, and this generates high losses [61].

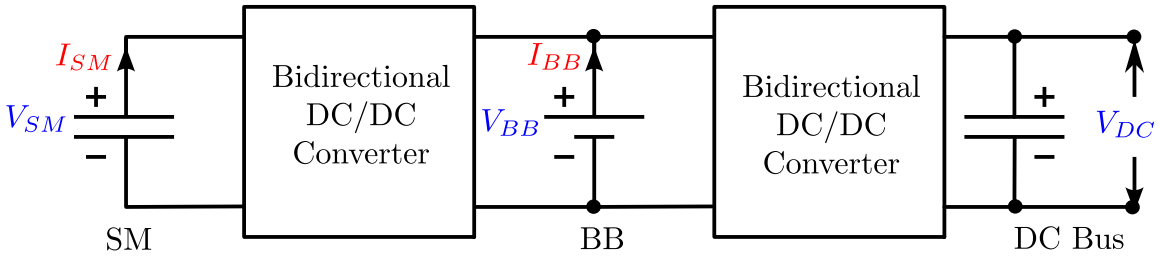


Figure 2-10: A bidirectional DC/DC converter is connected between the SM and the BB and another bidirectional DC/DC converter is connected between the BB and the DC bus.

2.5.3.2 $V_{BB} < V_{SM} < V_{DC}$

Also, a bidirectional DC/DC converter is connected between the BB and the SM and another bidirectional DC/DC converter is connected between the SM and the DC bus [49, 52, 75] as depicted in Figure 2-11. Again, the main advantage of this configuration is that the voltage of the SM and the BB are varied in an extensive range. The BB could have a small voltage, implying a specific cost reduction [52]. The drawback is that there are two bidirectional DC/DC converters, and therefore the cost, the size and the control complexity increases. The DC/DC converter connected between the BB and the DC bus should able to handle all the ESS power. This configuration yields to a subsequent rise in the system losses.

2.5.4 The Multiple Input Converter Configuration or the Multiport Converter Configuration ($V_{SM} \neq V_{BB}, (V_{SM}, V_{BB}) < V_{DC}$)

In this structure, a multiple input bidirectional DC/DC converter interfaces the BB, the SM and the DC bus [49, 50, 76, 76, 77], as depicted in Figure 2-12. The main advantages of this configuration are a decrease in the cost of the converters [49], and the possibility

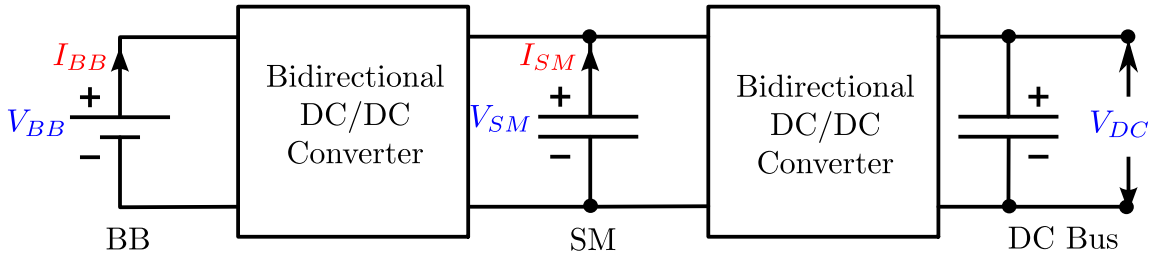


Figure 2-11: A bidirectional DC/DC converter is connected between the BB and the SM and another bidirectional DC/DC converter is connected between the SM and the DC bus.

of centralized control of the power flows involved in the system [77]. As main drawbacks, it can be said that together with a size increase, the control strategies and the power flow management are much more complicated [52, 61].

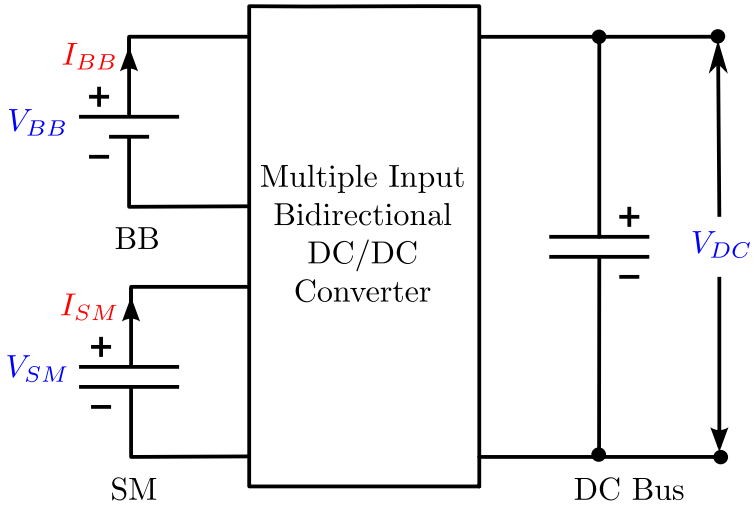


Figure 2-12: A multiple input bidirectional DC/DC converter is connected between the BB, the SM and the DC bus.

2.5.5 The Multiple Converter Configuration or the Active Parallel Configuration ($V_{SM} \neq V_{BB}, (V_{SM}, V_{BB}) < V_{DC}$)

The most common scheme used in HESS is finally introduced in this section. A first bidirectional DC/DC converter is connected between the SM and the DC bus, while another bidirectional DC/DC converter connects the BB and the DC bus [36, 49, 62, 74, 78, 78–82]. The basic diagram of the structure is depicted in Figure 2-13. The advantages of this

configuration is that the voltages of the BB and the SM can be varied in a wide range, and thus most of the SM available energy is effectively used [49, 62]. The power contribution of the two ESS can be managed independently. This yields to a set of interesting features for this structure, that include more flexibility for power management, overall system efficiency with an adequate design, and better general performance [52, 62, 83]. The drawbacks of this configuration are that two bidirectional DC/DC converters are needed [49, 50, 62], thus increasing the cost, size, and complexity of the design. But for all the advantages as mentioned earlier, this is the structure that has been selected for the application under consideration as it is the most suitable solution for the HESS. Therefore, this structure is used in the next sections of the discussion.

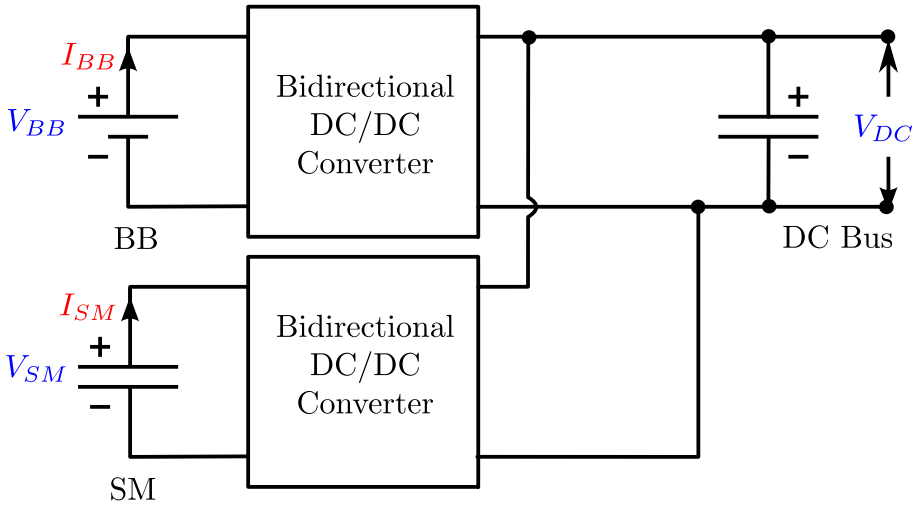


Figure 2-13: Two independent bidirectional DC/DC converter are used for interfacing the SM and the BB with the DC bus.

2.6 Conclusions

In this Chapter, the main ESS device technologies suitable for power systems have been presented, and their benefits, drawbacks, and applications have been discussed. Then, the state-of-the-art of the HESS for the DC microgrid and nanogrids have been characterized. The technologies of Li-Ion electrochemical BB and SM have been targeted as the most typical for the selected application, and therefore chosen as the two technologies to hybridize

in this research.

Finally, the power topology configurations suitable for the HESS are defined showing their merits and drawbacks. The active parallel configuration has been selected as the baseline structure for this kind of HESS. Next Chapter introduces the PC of two bidirectional buck converters as the base case for the selected configuration. Also, the control schemes during islanding mode and grid-connected mode are proposed, studied and discussed.

Chapter 3

Structure of Hybrid Storage Systems in DC Microgrids and Nanogrids

Contents

3.1 Introduction

This chapter focuses on the discussion of power electronic topologies at the multiple converter configuration, also known as active parallel configuration, applied in for HESS applications in DC microgrids and nanogrids. This configuration is the preferred one in HESSs when full control of all the power flows between the energy storage devices, and the DC bus is required. Later, the control strategies for these converter configurations are deeply analyzed, considering the system main operation constraints, i.e., both in the islanding mode and in the grid-connected mode. Finally, some contributions on this control strategies are proposed, in order to state a baseline case that can be used as a reference in the research in forthcoming Chapters.

3.2 Topologies of the Multiple Converter Configuration

In the application under study, i.e., HESSs for DC microgrids, different options can be chosen to implement the interfacing converters. The DC/DC bidirectional converters are generally divided into isolated and non-isolated types [5, 7, 84, 85]. If galvanic isolation is not a requirement for the HESS, then PC of two bidirectional buck converters, as shown in Figure 3-1 is the most prevalent for low to medium power applications. The variable current source (I_N) and the variable resistance (R_N) at the DC bus in Figure 3-1 are intended to model the behavior of the rest of the DC microgrid. The DC bus consists of two capacitors

connected in series, with equal capacitance values, so as to have access to the middle point of the DC bus, point m in figure 3-1. This scheme can also be defined as a H-bridge configuration [4, 36, 74, 78, 79, 86–90]. Given that the topology is a bidirectional circuit, the consideration of the topology as a buck or as a boost is a matter of defining adequately the references and the switch which has the main control action (i.e., duty cycle) in the corresponding leg, leaving the remaining switch commuting in a complementary scheme. For simplicity in the equations, the upper switch is considered to have the duty cycle that defined the control action in each leg; therefore, the topology will be called buck converter stage along this research.

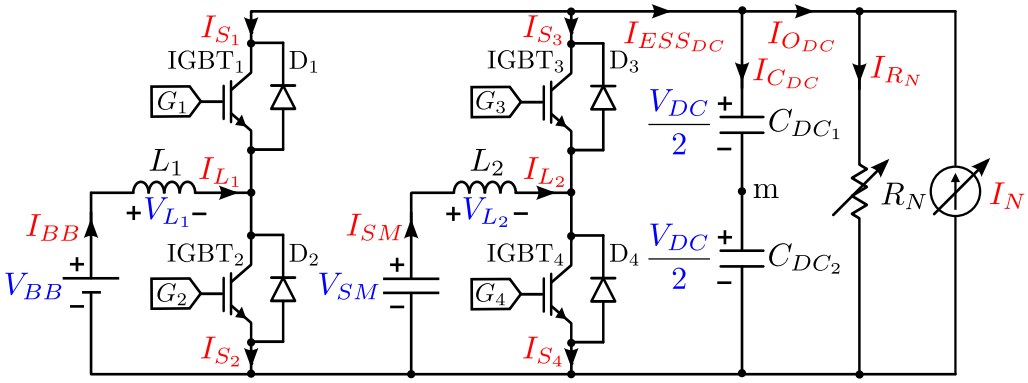


Figure 3-1: PC of two bidirectional buck converters interfacing the energy storage devices (BB and SM) and the DC bus.

For higher rated power levels in the ESS, still, without the isolation requirement, other options for the storage power converters, such as interleaved bidirectional converters [7, 85, 91] (Figure 3-2) or multilevel converters [92, 93] can be used.

However, if the galvanic isolation is a requirement in the design, a number of isolated DC/DC converter topologies might be considered. Among them, Dual Active Bridge (DAB) (Figure 3-3), stands as one of the most suitable for this application [36, 57, 58, 81, 94–96]. However, it yields an increase in the cost and the hardware complexity, as the number of switches also increases. For ah hybrid storage structure, the DAB is transformed into the Triple Port Active Bridge (TAB), depicted in Figure 3-4 [97–100]. This scheme results in a smaller number of switches compared to the two parallel DAB converters.

In general terms, isolation might be required to isolate the distribution grid from the

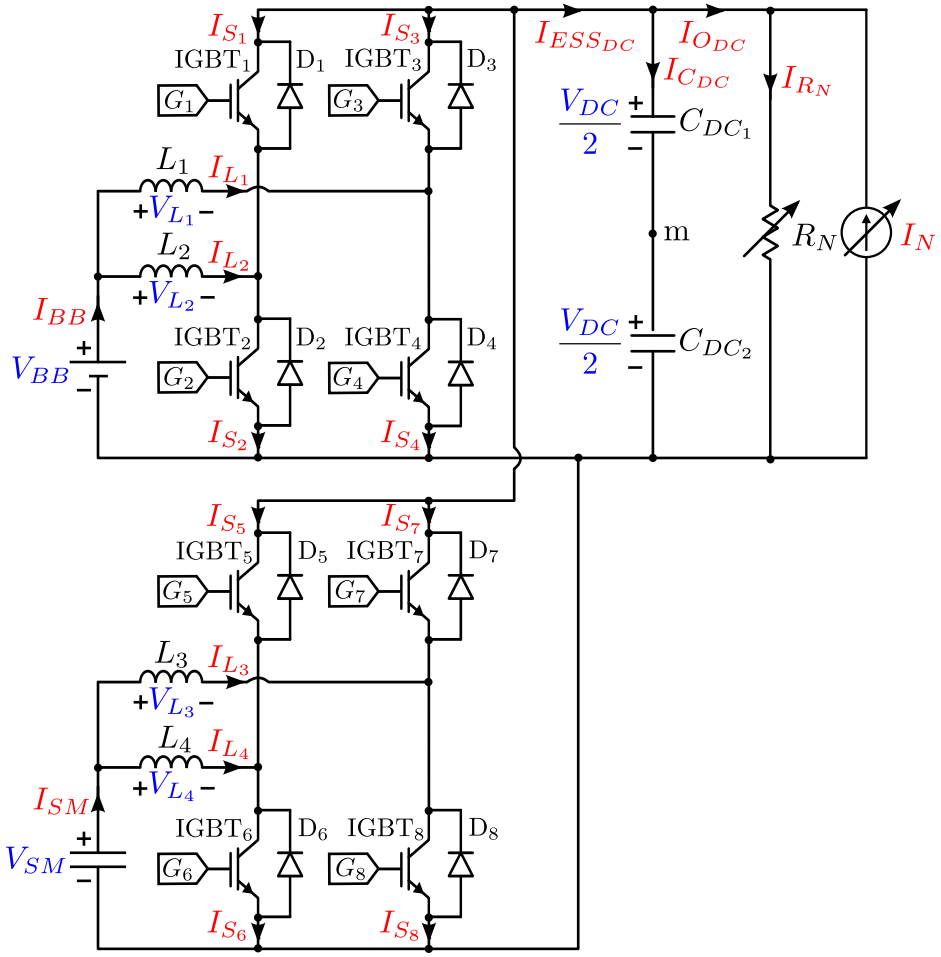


Figure 3-2: PC of two bidirectional interleaved buck converters interfacing the energy storage devices (BB and SM) and the DC bus.

microgrid galvanically. In this case, this is usually achieved by a line transformer or by a specific isolated conversion stage, usually at the PCC. However, in any case, if the isolation is not a requirement in the HESS, then the basic non-isolated converters are preferred because of smaller size, weight, and cost. Additionally, for a set of operating conditions that depend on the solutions implemented, it might yield to an improvement in the efficiency [4, 7]. For this reason, the case under study considers a system where isolation is not a requirement for the HESS. In addition, a power range below 100 kW is targeted. Therefore, the direct PC of bidirectional buck converters is selected as the baseline case in the coming discussion. The power topology will be reviewed, and the main advantages and limitations will be stated. Later, along with the coming chapters, some contributions will be proposed to overcome the identified limitations in the system.

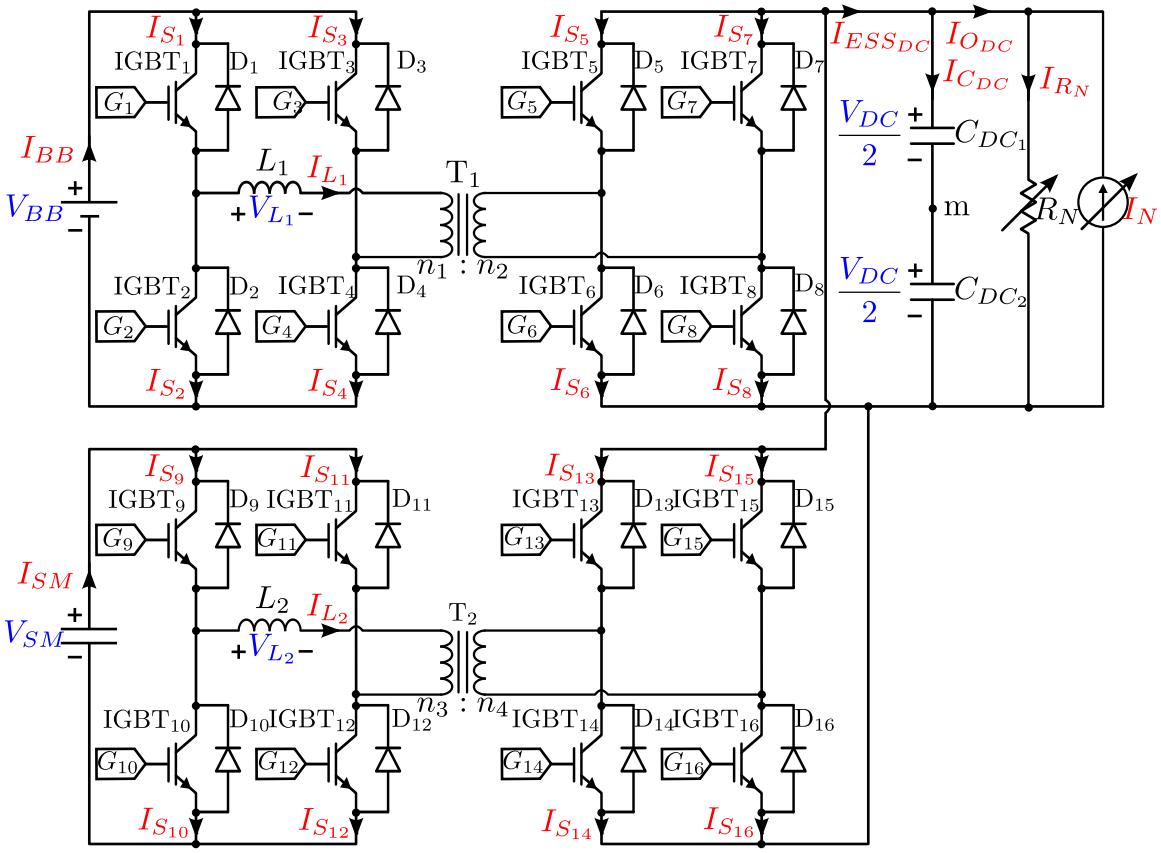


Figure 3-3: Two DAB converters connected in parallel interfacing the energy storage devices (BB and SM) and the DC bus.

3.3 Switching States of the Parallel Connection of Two Bidirectional Buck Converters

In the most straightforward arrangement, each interfacing stage connects a storage unit and the DC bus by means of two switches that are connected following a bidirectional buck converter scheme. This is the connection that is going to be referred to as PC. The switches in this arrangement can be implemented in the real application by means of several technologies. Nowadays, the leading technologies for implementing switches include Insulated Gate Bipolar Transistor (IGBT), Metal Oxide Silicon Field Effect Transistor (MOSFET) (based on Silicon (Si) or Silicon Carbide (SiC)) or Field Effect Transistor (FET) Gallium Nitride (GaN) [101, 102] devices. For this research, IGBT power modules are going to be considered, however, a similar analysis can be done with any other power device technol-

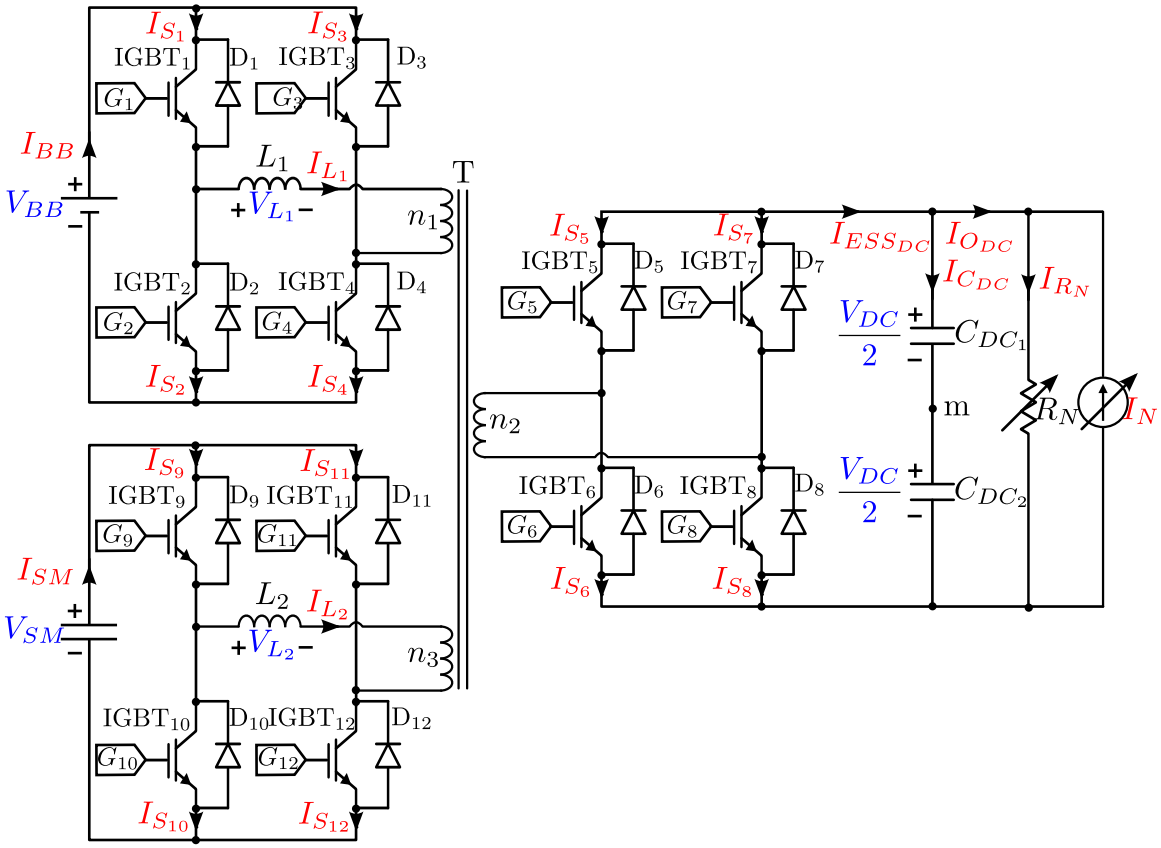


Figure 3-4: TAB is interfacing the energy storage devices (BB and SM) and the DC bus.

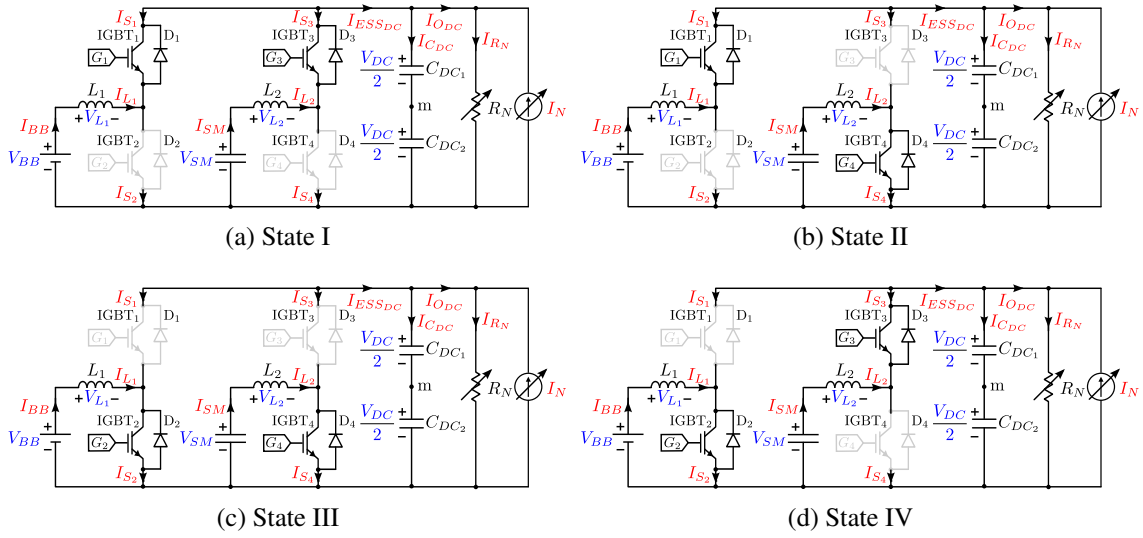
ogy. Each switch is formed by a Switch (S), that is formed by an IGBT and an anti-parallel Diode (D). The converter interfacing the BB is formed by S_1 ($IGBT_1$ and D_1) and S_2 ($IGBT_2$ and D_2), whereas the converter that interconnects the SM is formed by S_3 ($IGBT_3$ and D_3) and S_4 ($IGBT_4$ and D_4), as it is depicted in Figure 3-1. For each of the converters, the duty cycle is defined as the one for the upper switch, i.e., S_1 for the BB converter and S_3 for the SM converter. In any case, at each of the converters, the lower switch is commutating in a complementary scheme with respect to the upper switch. For this arrangement of switches, it is evident that dead time is needed in order to avoid cross-conduction of switches in a leg that yield to short circuit. For simplicity, this dead time is assumed to be much smaller (at least two orders of magnitude) than the switching period, and therefore it is neglected in this discussion. However, it will be considered in simulations and implemented in the experimental setup.

With this switching pattern, four possible switching states for the bidirectional buck

converters can be found. These states are shown in Table 3.1 and Figure 3-5.

Table 3.1: Switching states of the PC of two bidirectional buck converters.

States	BB Converter		SM Converter		Figure
	On	Off	On	Off	
State I	S_1	S_2	S_3	S_4	3-5a
State II	S_1	S_2	S_4	S_3	3-5b
State III	S_2	S_1	S_4	S_3	3-5c
State IV	S_2	S_1	S_3	S_4	3-5d



(a) State I (b) State II

(c) State III (d) State IV

Figure 3-5: Switching states of the PC of two bidirectional buck converters.

At each switch, the anti-parallel diode allows for bidirectional current flow capability in the converter. Table 3.2 shows all the possible combinations of which is the actual device driving the current at each switch (i.e., IGBT or Diode), for either the intervals of charging or discharging of the storage devices.

There are three possible conditions, regarding the relative values of the duty cycles of the upper switches:

$$d_1 > d_3 \tag{3.1}$$

$$d_1 = d_3 \tag{3.2}$$

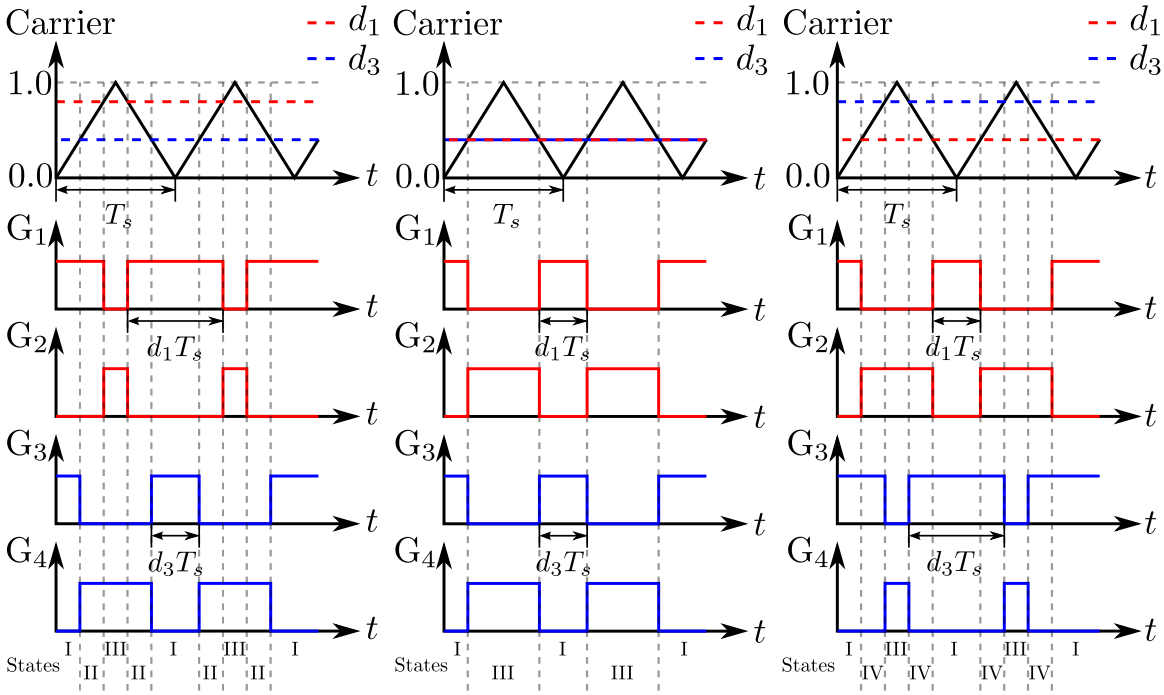
$$d_1 < d_3 \tag{3.3}$$

Table 3.2: Switching states of two bidirectional buck converters for the On switches.

States	BB Converter (On Switches)		SM Converter (On Switches)	
	BB Discharging	BB Charging	SM Discharging	SM Charging
State I	D_1	$IGBT_1$	D_3	$IGBT_3$
State II	D_1	$IGBT_1$	$IGBT_4$	D_4
State III	$IGBT_2$	D_2	$IGBT_4$	D_4
State IV	$IGBT_2$	D_2	D_3	$IGBT_3$

where d_1 and d_3 are the duty cycles of the $IGBT_1$ and $IGBT_3$, respectively.

Depending on these conditions, and considering a sine-triangle Pulse Width Modulation (PWM) scheme synchronized with a triangular waveform [84], the switching states will change as in Figure 3-6.



(a) $d_1 > d_3$ (b) $d_1 = d_3$ (c) $d_1 < d_3$

Figure 3-6: Switching states of the PC of two bidirectional buck converters, as a function of the relative values of the duty cycles.

The on and off times can be defined for every switch in the system. In particular, for the upper switches of each storage device converter, S_1 and S_3, this definition is carried

out in Equations (3.4)-(3.7). Among the four possible states, only three switching states appear in conditions (3.1) and (3.3), whereas only two states appear in condition (Equation (3.2)). In the case under study, the SM voltage is always smaller than the BB voltage ($V_{SM} < V_{BB}$). Therefore, at steady state and according to the rated voltage values of the ESS devices, the condition stated at Equation (3.1) will occur.

$$T_{on\_S1} = d_1 \cdot T_s \tag{3.4}$$

$$T_{off\_S1} = (1 - d_1)T_s \tag{3.5}$$

$$T_{on\_S3} = d_3 \cdot T_s \tag{3.6}$$

$$T_{off\_S3} = (1 - d_3)T_s \tag{3.7}$$

where:

- T_{on_S1} and T_{off_S1} are the on and off times of the upper switch (S_1) for the BB converter, respectively, in Secs,
- T_{on_S3} and T_{off_S3} are the on and off times of the upper switch (S_3) for the SM converter, respectively, in Secs,
- T_s is the switching time in Secs.

3.4 Operating Modes of the DC Microgrid

Figure 3-7 depicts a generic structure of a DC microgrid, where the PCC is interfaced to the microgrid by means of a DC/AC inverter. Upon grid-connected mode, the microgrid is effectively tied to the distribution grid through the PCC, and power can flow to/from the grid [5, 6, 103, 104]. On the other hand, in the islanding mode, also known as a stand-alone mode, the PCC is disconnected from the grid, and therefore an internal power balance must be ensured, as the power cannot flow to/from the grid side anymore [3, 14, 15, 18, 19, 77, 105–107].

The islanding mode might take place in several conditions. In some cases, a stand-alone operation is the only possible operation mode. This is the case of remote areas, where the connection costs to the distributions/transmission facilities are prohibitive [3, 15, 86, 108].

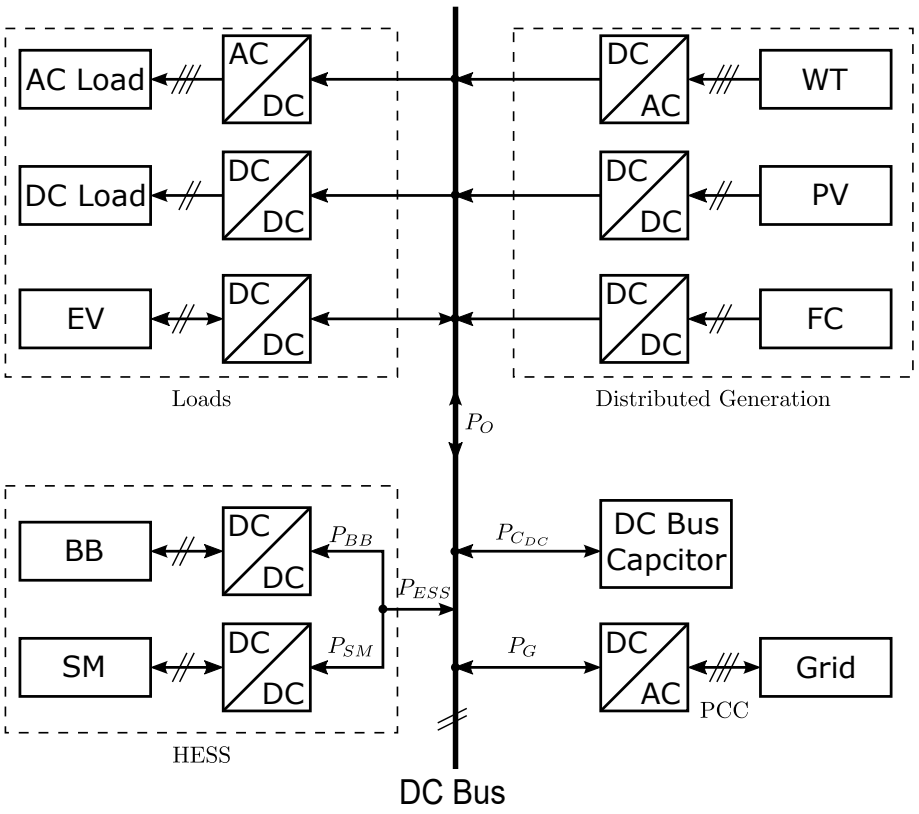


Figure 3-7: The power balance in a DC microgrid.

Even when the regular operation of the system is the grid-tied operation, the microgrid might enter in islanding mode upon given circumstances:

- Due to the appearance of the faults in the distribution system that triggers protections, in particular at the PCC [5].

- Reception of hierarchical commands from the Distribution Network Operator (DNO) forcing the disconnection of the microgrid, as in the case of the interruptibility service. This service is a demand management tool that provides flexibility and rapid response to system operation in situations of imbalance between generation and demand [109].

- The Existence of internal strategies that envisage potential benefits in the disconnection for the grid and stand-alone operation (tariff/economic constraints, etc.).

In any case, the microgrid must have the ability to supply the loads defined in each

circumstance. In particular and in order to optimize the cost of energy, several strategies can be implemented:

- Power shifting: Loads are programmed to work at off-peak hours and low price energy rate [110].

- Load shedding: When load power is high, non-critical and low-priority loads can be temporarily shut down for given periods of time. Usually, load shedding is used to prevent blackout and instability of the systems [111]. This is implemented in the stand-alone mode when the sum of the generated power plus the available power at the HESS is less than the power demanded.

- Peak shaving: During the off-peak hours and low-price energy rates, the battery is charged to a high SoC condition [112]. However, during the peak hours and high price energy rate, the power drained from the grid is limited to a given maximum value, and the remaining voltage is provided by the storage system [112]. In peak shaving, there is no need to shut down the loads or change the hours the load operation. Therefore, it has clear advantages over the alternative schemes. The peak shaving is implemented in the supervisory control.

A notation convention will be applied in the following discussion. Given that both the BB and SM devices are bidirectional power elements, it is evident that both can deliver or absorb power. As they are unipolar in voltage, therefore the current can be positive or negative, respectively. For establishing a consistent, unambiguous formulation in the following discussion, it will be considered that the positive current is the discharging current of the storage devices, while the negative current is the charging current of the storage devices. Therefore, the maximum current of each ESS will be the maximum discharging current, whereas the minimum current will be the maximum charging current, in order to be consistent with the signs of the currents. The same criteria are applied to the signs of the instant power at each device. The maximum power is the maximum power delivered; however, the minimum power is the maximum power absorbed by the device.

3.4.1 Control Scheme during the Islanding Mode

During the stand-alone operation, one of the internal converters at the microgrid must ensure the DC bus control that keeps system proper operation and stability [60]. One option is that the interfacing converter of the BB takes over the DC bus voltage control, thus regulating the power balance in the DC bus [99, 113]. In order to achieve the hybrid behavior of the storage system, the SM converter's control aims to provide or absorb the transient peak power during load variations or stochastic variations in the distributed generators within the microgrid [79, 114]. This control strategy is generally implemented through three control loops: one outer DC bus voltage control loop plus two inner current control loops, so as to control the current flowing through the inductors at both the BB and the SM converters [79, 86, 87, 89, 115]. This scheme is shown in Figure 3-8.

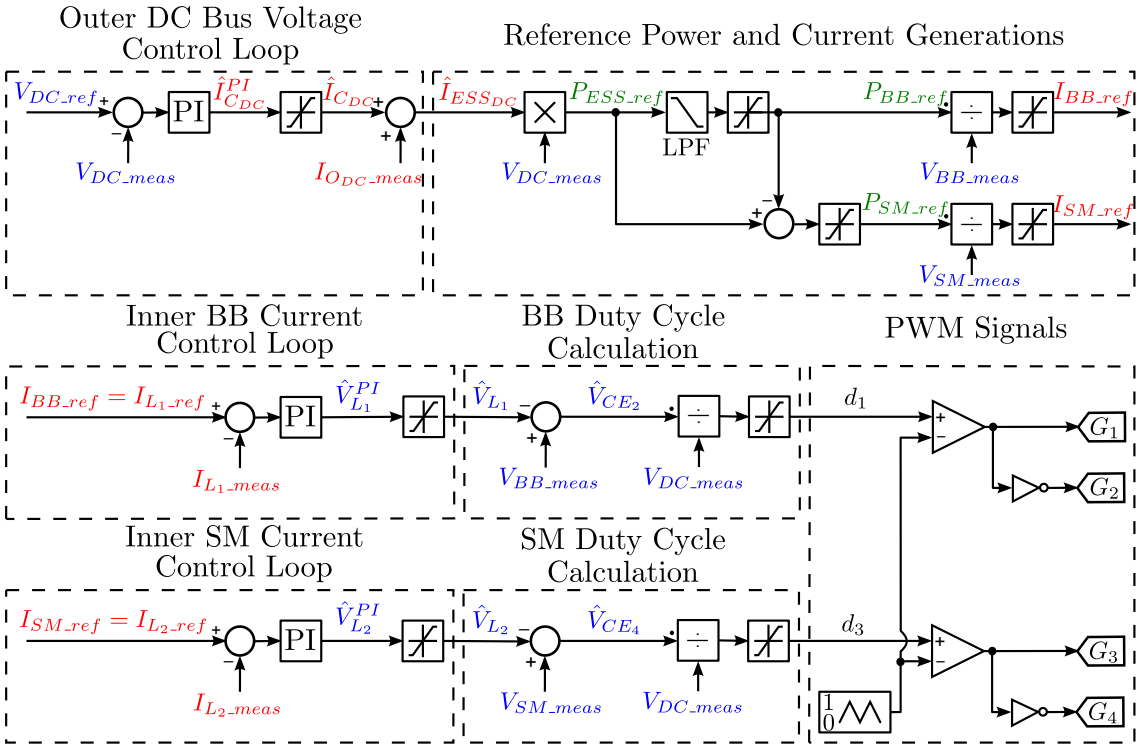


Figure 3-8: Control of the PC of the two bidirectional buck converters for islanding mode operation of the microgrid.

In order to implement the control strategy, several operating parameters need to be measured and computed. These set of parameters include the voltage and current values

of both the BB and SM, V_{BB}, I_{BB} and V_{SM}, I_{SM}, respectively. Also, the DC bus voltage (V_{DC}) is going to be acquired. The HESS output current ($I_{O_{DC}}$) also needs to be measured; however, for future developments, this parameter could be estimated if there is difficulty in measuring it. But for this research, the value of this parameter is always measured. In this scheme, the reference values are compared to the measured values and then are applied to a Proportional Integral (PI) controller. However, the estimated values are used to generate the reference values for the next stages.

3.4.1.1 Outer DC Bus Voltage Control Loop

The DC bus voltage is controlled by a typical PI controller as shown in Figure 3-9. The outer DC bus voltage control loop is considering that the transfer function of the two inner current control loops are equal to unity. In order to assume such condition, the inner current loops are designed to be much faster, with a bandwidth at least ten times faster than the bandwidth of the outer loop.

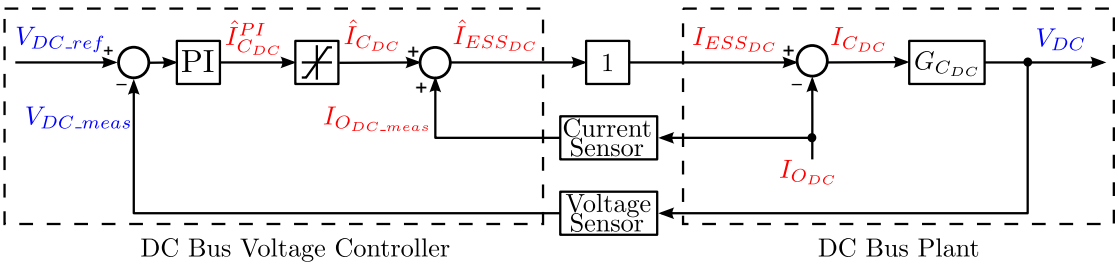


Figure 3-9: The DC bus voltage control closed loop.

Considering the standard form (ideal form) of the PI controller shown in Figure 3-10, the transfer function in Laplace transform is given by:

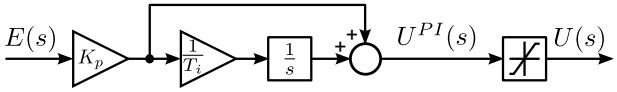


Figure 3-10: The PI controller in the standard form.

$$R(s) = \frac{U^{PI}(s)}{E(s)} = K_p\left(1 + \frac{1}{T_i s}\right) \tag{3.8}$$

$$R(s) = K_p\left(\frac{s + \frac{1}{T_i}}{s}\right) \tag{3.9}$$

where:

- R is the transfer function of the PI controller,
- U^{PI} is the output of the PI controller before the limiter,
- U is the output of the PI controller after the limiter,
- E is the error of the PI controller,
- K_p is the proportional gain of the PI controller,
- s is the Laplace complex variable $s = \sigma + j\omega_d$,
- T_i is the integral time constant of the PI controller in Secs.

As it can be seen from Figure 3-10, the output of the controller is limited according to the upper and lower limits as in Equation (3.10). It must be noticed that in case the output of the controller exceeds these values, an anti-windup mechanism is needed in order to avoid the saturation of the regulator.

$$U = \begin{cases} U_{min} & U^{PI} < U_{min} \\ U^{PI} & U_{min} \leq U^{PI} \leq U_{max} \\ U_{max} & U^{PI} < U_{max} \end{cases} \tag{3.10}$$

where U_{min} and U_{min} are the minimum and maximum value of the PI controller output.

As mentioned before, the DC bus is divided into two capacitors which have the same capacitance values as depicted in 3-1. The control parameters will be designed for the total DC capacitance, that can be expressed as in Equation (3.12). Therefore, the transfer function of the DC bus capacitor in Laplace transform is as in Equation (3.13).

$$\frac{1}{C_{DC}} = \frac{1}{C_{DC_1}} + \frac{1}{C_{DC_2}} = \frac{C_{DC_1} + C_{DC_2}}{C_{DC_1} \cdot C_{DC_2}} \tag{3.11}$$

$$C_{DC} = \frac{C_{DC_1} \cdot C_{DC_2}}{C_{DC_1} + C_{DC_2}} = \frac{C_{DC_1}}{2} = \frac{C_{DC_2}}{2} \tag{3.12}$$

$$G_{C_{DC}}(s) = \frac{V_{DC}(s)}{I_{C_{DC}}(s)} = \frac{1}{C_{DC} \cdot s} \tag{3.13}$$

where:

- C_{DC} is the DC bus capacitor's capacitance in Farads,
- C_{DC_1} and C_{DC_2} are the capacitance of the upper and lower half of the DC bus's capacitor, respectively in Farads,
- $G_{C_{DC}}$ is the transfer function of the DC bus capacitor,
- $I_{C_{DC}}$ is the DC bus capacitor's current in Amps.

The tuning of the parameters of the PI regulator for the DC bus voltage controller will be discussed in Chapter 6. However, the limits of the control action are obtained in the following discussion. With these limits, an anti-windup scheme can be implemented in order to prevent the saturation of the controller.

Figure 3-1 depicts how the rest of the microgrid is represented by a variable current source with a parallel variable resistance according to Norton's theorem. The parallel variable resistance represents the resistive loads, and the variable current source represents the other loads and the RES (e.g., constant current and constant power loads). Using Kirchhoff's Current Law (KCL) in Figure 3-1, it yields to:

$$I_{ESS_{DC}} = I_{O_{DC}} + I_{C_{DC}} \tag{3.14}$$

$$d_1 \cdot I_{BB} + d_3 \cdot I_{SM} = I_{R_N} - I_N + I_{C_{DC}} \tag{3.15}$$

$$I_{C_{DC}} = d_1 \cdot I_{BB} + d_3 \cdot I_{SM} + I_N - \frac{P_{R_N}}{V_{DC}} \tag{3.16}$$

where:

- $I_{ESS_{DC}}$ is the sum of the currents of the ESS converters at the DC bus side in Amps,
- $I_{O_{DC}}$ is the output current at the DC bus side drawn by the rest of the microgrid in Amps,
- I_{BB} and I_{SM} are the BB and SM currents, respectively, in Amps,
- I_{R_N} is the current drawn by the load resistance (R_N) in Amps,
- I_N is the Norton current modeling the behavior of the rest of the microgrid in Amps,
- R_N is the load resistance in Ohms,
- P_{R_N} is the load power in Watts.

The lower limit of the operation of the PI controller is obtained for both $d_1 = 1$ and $d_3 = 1$ (i.e., State I) which the storage converters remain with the upper switch turned on, and therefore:

$$I_{C_{DC}\_min} = I_{BB\_min} + I_{SM\_min} + I_{N\_min} - \frac{P_{R_N\_max}}{V_{DC\_ref}} \tag{3.17}$$

where:

- $I_{C_{DC}\_min}$ is the minimum DC bus capacitor current in Amps,
- I_{BB_min} and I_{SM_min} are the minimum BB and SM currents (the maximum BB and SM charging currents) in Amps,
- I_{N_min} is the minimum current delivered by the rest of the microgrid in Amps,
- V_{DC_ref} is the DC bus voltage reference in Volts,
- $P_{R_N\_max}$ is the maximum load power in Watts.

On the other hand, in order to obtain the upper limit for the PI controller, both upper switches are continuously turned on in the state I (i.e., $d_1 = 1$ and $d_3 = 1$) as well, the following equations apply:

$$I_{C_{DC}\_max} = I_{BB\_max} + I_{SM\_max} + I_{N\_max} - \frac{P_{R_N\_min}}{V_{DC\_ref}} \tag{3.18}$$

where:

- $I_{C_{DC}\_max}$ is the maximum DC bus capacitor current in Amps,
- I_{BB_max} and I_{SM_max} are the maximum BB and SM currents (the maximum BB and SM discharging currents) in Amps,
- I_{N_max} is the maximum current delivered by the rest of the microgrid in Amps,
- $P_{R_N\_min}$ is the minimum load power in Watts.

The limits of the DC bus PI voltage controller is obtained as follows:

$$\hat{I}_{C_{DC}} = \begin{cases} I_{C_{DC}\_min} & \hat{I}^{PI}_{C_{DC}} < I_{C_{DC}\_min} \\ \hat{I}^{PI}_{C_{DC}} & I_{C_{DC}\_min} \leq \hat{I}^{PI}_{C_{DC}} \leq I_{C_{DC}\_max} \\ I_{C_{DC}\_max} & \hat{I}^{PI}_{C_{DC}} > I_{C_{DC}\_max} \end{cases} \tag{3.19}$$

where $\hat{I}_{C_{DC}}$ and $\hat{I}^{PI}_{C_{DC}}$ are the estimated DC bus capacitor current after and before the limiter, respectively, in Amps.

After the limits for the control action ($\hat{I}^{PI}_{C_{DC}}$) are established, the feed-forward term ($I_{O_{DC}\_meas}$) is added in order to improve the dynamics and the recovery of the DC bus upon load variations [79]. The resulting variable after adding such feed-forward term is the ESS estimated current at the DC side ($\hat{I}_{ESS_{DC}}$) as depicted in Figure 3-8.

3.4.1.2 Generation of the Power References

From $\hat{I}_{ESS_{DC}}$, the references for the inner BB and SM current loops can be obtained. In order to do so, a scheme must be defined that can coordinate the evolution of the power delivered/absorbed by each storage device. Therefore, a power balance as a function of time must be defined during the transient stage [116]. Assuming that there are no losses in the converters, from the schematics at Figure 3-7, the following expressions are obtained:

$$P_{C_{DC}} = I_{C_{DC}} \cdot V_{DC} \tag{3.20}$$

$$P_{ESS} = I_{ESS_{DC}} \cdot V_{DC} \tag{3.21}$$

$$P_O = I_{O_{DC}} \cdot V_{DC} \tag{3.22}$$

$$P_{C_{DC}} = P_{ESS} - P_O \tag{3.23}$$

$$P_{ESS} = P_{C_{DC}} + P_O = (I_{C_{DC}} + I_{O_{DC}})V_{DC} \tag{3.24}$$

where:

- $P_{C_{DC}}$ is the power of the DC bus capacitor in Watts,
- P_{ESS} is the power of the ESS in Watts,
- P_O is the active power delivered to the rest of the microgrid in Watts.

As stated before, the voltage at the DC bus capacitor is controlled to maintain the power balance within the system. Therefore, the DC bus capacitor average power is null in steady state. Assuming a transient power positive step in the active power delivered to the rest of the microgrid (P_O), indicating that the rest of the microgrid suddenly demands more power. Initially, this power is provided by the DC bus capacitor. Thus, the DC bus voltage will

decrease. Given that voltage control is implemented, this voltage is being measured and compared against a reference. The sudden error in the DC bus voltage is the signal that is used to force the ESS to supply the required power to the system, and therefore the DC bus voltage will evolve towards its reference value, again charging the DC bus capacitor up to the steady-state value. Analogously, in case the microgrid suddenly delivers a transient power towards the DC bus, the system will evolve in a similar manner, but with the DC bus voltage initially increasing above the reference value. Finally, the DC bus voltage will reach the steady state again, in this case after the ESS absorbs the excessing amount of power.

The ESS power reference (P_{ESS_ref}) is calculated from the control action of the voltage control loop ($\hat{I}_{C_{DC}}$) and the feed-forward term ($I_{O_{DC}\_meas}$):

$$P_{ESS\_ref} = (\hat{I}_{C_{DC}} + I_{O_{DC}\_meas})V_{DC\_meas} \tag{3.25}$$

where:

- P_{ESS_ref} is the power reference of the ESS in Watts,
- $I_{O_{DC}\_meas}$ is the measured output current at the acrshordc bus side drawn by the rest of the microgrid in Amps,
- V_{DC_meas} is the measured DC bus voltage in Volts.

Several strategies can be used to split the power share among the BB and the SM. As mentioned in previous sections, the target is to define the SM power reference to support the peak current demands, while the BB is used to support the energy storage requirements. The most straightforward strategy is to obtain the BB power reference (P_{BB_ref}) by applying a LPF to the global ESS power reference (P_{ESS_ref}) [99, 117–119]. In this manner, provided that the adequate the LPF characteristics be selected, then the values of both the peak current and the di/dt through the BB can be effectively kept between the defined operational limits. In order to ensure that the SM storage system provides the additional power required by the load, the power reference for the SM (P_{SM_ref}) is calculated precisely as the subtraction between the reference of the overall power of the complete system (P_{ESS_ref}) and that delivered by the battery (P_{BB_ref}). This way, it is ensured that the SM storage

system is providing or absorbing the transient peak power during load variations:

$$P_{BB\_ref}(s) = \underbrace{\frac{1}{1 + T_{BB_{LPF}} \cdot s}}_{\text{LPF}} P_{ESS\_ref}(s) \tag{3.26}$$

$$T_{BB_{LPF}} = \frac{1}{2\pi \cdot f_{BB_{LPF}}} \tag{3.27}$$

where:

- P_{BB_ref} is the power reference of the BB in Watts,
- $T_{BB_{LPF}}$ is the time constant of the LPF of the BB power in Secs,
- $f_{BB_{LPF}}$ is the cutoff frequency of the LPF of the BB power in Hz.

A limiter for the BB power reference (P_{BB_ref}) is used here in order to force the SM to provide/absorb the excess power that BB cannot provide/absorb during the transient and steady state.

$$P_{BB\_ref} = \begin{cases} P_{BB\_min} & \frac{P_{ESS\_ref}}{1 + T_{BB_{LPF}} \cdot s} < P_{BB\_min} \\ \frac{P_{ESS\_ref}}{1 + T_{BB_{LPF}} s} & P_{BB\_min} \leq \frac{P_{ESS\_ref}}{1 + T_{BB_{LPF}} \cdot s} \leq P_{BB\_max} \\ P_{BB\_max} & \frac{P_{ESS\_ref}}{1 + T_{BB_{LPF}} \cdot s} > P_{BB\_max} \end{cases} \tag{3.28}$$

However, the SM power reference is calculated as the difference between the power references of the ESS and BB values as follows:

$$P_{SM\_ref} = P_{ESS\_ref} - P_{BB\_ref} \tag{3.29}$$

where P_{SM_ref} is the power reference of the SM in Watts.

It must be noticed how another limiter for the SM power reference (P_{SM_ref}) is used,

in this case, to ensure that SM power converter limits are not exceeded as follows:

$$P_{SM\_ref} = \begin{cases} P_{SM\_min} & (P_{ESS\_ref} - P_{BB\_ref}) < P_{SM\_min} \\ P_{ESS\_ref} - P_{BB\_ref} & P_{SM\_min} \leq (P_{ESS\_ref} - P_{BB\_ref}) \leq P_{SM\_max} \\ P_{SM\_max} & (P_{ESS\_ref} - P_{BB\_ref}) > P_{SM\_max} \end{cases} \quad (3.30)$$

3.4.1.3 Calculating the Operational Limits for the Power References

The following discussion deals with the control process depending on the SoC of each ESS as depicted in Figure 3-11. This control will be implemented as a state machine in the control of the HESS, as is a simple way to control the system and to change the power limits depending on the status of the ESS (charge/discharge). This control is a high-hierarchy level control, aiming to protect the ESS of a dangerous complete discharge or an excess overcharge. Given that the system must always operate within limits imposed by the absolute maximum ratings of the energy storage devices, the overall control algorithm must consider these limits.

The algorithm starts by reading the SoC of the BB and then comparing it with the stated SoC operating limits. In order to keep the system between safe operating margins, the limits of the BB power reference (P_{BB_ref}) will change depending on the SoC of the BB [120] as follows:

1. $SOC_{BB} < SOC_{BB\_min}$: In this case, only power flowing towards the battery is allowed, and therefore the discharging capability of the BB will be blocked. Considering the signs convention, then the following limits must be applied:

$$P_{BB\_min} = I_{BB\_min} \cdot V_{BB\_meas} \quad (3.31)$$

$$P_{BB\_max} = 0 \quad (3.32)$$

2. $SOC_{BB\_min} \leq SOC_{BB} \leq SOC_{BB\_max}$: This is the most general case [121]. The BB can either be charged and discharged, depending on the system operating condi-

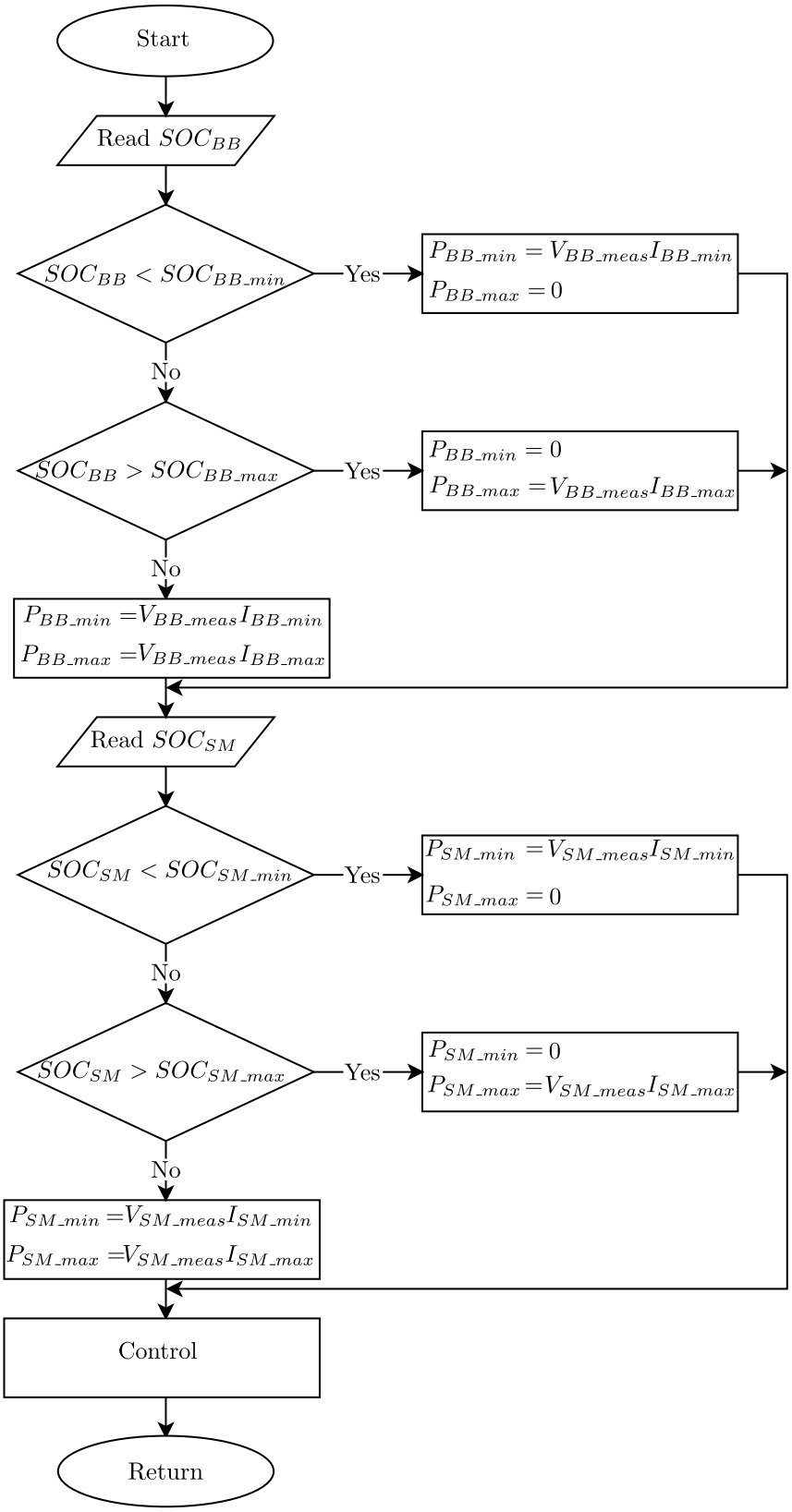


Figure 3-11: Flowchart of the control process depending on the SoC.

tions. The following limits apply:

$$P_{BB\_min} = I_{BB\_min} \cdot V_{BB\_meas} \tag{3.33}$$

$$P_{BB\_max} = I_{BB\_max} \cdot V_{BB\_meas} \tag{3.34}$$

3. $SOC_{BB} > SOC_{BB\_max}$: In this last case, the BB is fully charged; no more power can flow towards the battery, and only the discharge is allowed. The limits then evolve to:

$$P_{BB\_min} = 0 \tag{3.35}$$

$$P_{BB\_max} = I_{BB\_max} \cdot V_{BB\_meas} \tag{3.36}$$

From Equations (3.31) to (3.36), the following notation is used:

- SOC_{BB_min} and SOC_{BB_max} are the minimum and maximum SoC of the BB, respectively.
- P_{BB_min} is the minimum power of the BB (the maximum BB charging power) in Watts,
- P_{BB_max} is the maximum power of the BB (the maximum BB discharging power) in Watts,
- V_{BB_meas} is the measured BB voltage in Volts.

In a similar manner, the SoC of the SM is read and compared to the desired SoC operating limits. The operating limits for the SM power reference (P_{SM_ref}) values will change depending on the SoC of the device:

1. $SOC_{SM} < SOC_{SM\_min}$: The SM is at its minimum amount of stored energy, and therefore the operating limits for the SM power reference are:

$$P_{SM\_min} = I_{SM\_min} \cdot V_{SM\_meas} \tag{3.37}$$

$$P_{SM\_max} = 0 \tag{3.38}$$

2. $SOC_{SM\_min} \leq SOC_{SM} \leq SOC_{SM\_max}$: Again the base case and the SM can either charge and discharge. The most general limits for the SM power reference are:

$$P_{SM\_min} = I_{SM\_min} \cdot V_{SM\_meas} \tag{3.39}$$

$$P_{SM\_max} = I_{SM\_max} \cdot V_{SM\_meas} \tag{3.40}$$

3. $SOC_{SM} > SOC_{SM\_max}$: Finally, the SM is fully charged, and the control must allow only the discharge mode:

$$P_{SM\_min} = 0 \tag{3.41}$$

$$P_{SM\_max} = I_{SM\_max} \cdot V_{SM\_meas} \tag{3.42}$$

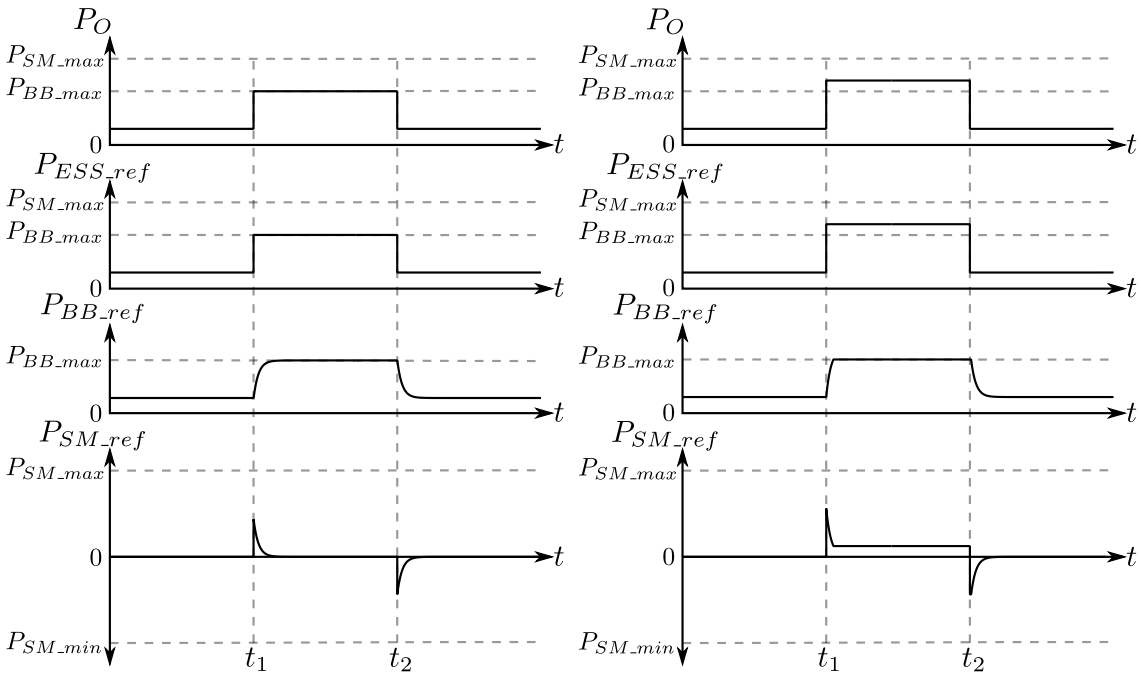
Analogously, from Equations (3.37) to (3.42), the following notation is used:

- SOC_{SM} is the SoC of the SM,
- SOC_{SM_min} and SOC_{SM_max} are the minimum and maximum SoC of the SM, respectively,
- P_{SM_min} is the minimum power of the SM (the maximum SM charging power) in Watts,
- P_{SM_max} is the maximum power of the SM (the maximum SM discharging power) in Watts,
- V_{SM_meas} is the measured SM voltage in Volts.

3.4.1.4 Implementation of the Control Algorithm

The operation of the energy management system at Figure 3-8 with the control algorithm defined above will be discussed in the following paragraphs. Firstly, the derivation of the power reference values for the storage subsystems will be discussed, considering a series of specific load power steps at the microgrid. Figure 3-12 shows the main references for the distinct power flows involved in the system, upon a sequence of two steps that provide a symmetric profile in the demanded power (P_O).

In this example, the demanded power (P_O) first increases at t_1 and then decreases back to the original level at t_2. As it can be seen, the islanding mode operation is assumed since



(a) $P_{BB\_max} \geq P_O$ (b) $P_{BB\_max} < P_O$

Figure 3-12: The power references generation during the islanding mode while the BB is discharging.

the ESS power reference (P_{ESS_ref}) is equal to the power demanded by the microgrid (P_O). In the most general case, if the maximum power demanded (P_{O_max}) is less or equal to the BB maximum power ratings (P_{BB_max}), then the SM will deliver or absorb the transient peak power, and the BB will deliver the rest of power needed. This situation is depicted in Figure 3-12a. Nevertheless, the demanded power might be greater than this BB maximum power ratings, and thus this would imply that the SM would deliver or absorb both the transient peak power, but also the remaining power that the BB is not able to provide for a short period. This alternative situation is shown in Figure 3-12b. This is implicitly assuming that power demanded to the SM storage system, (P_{SM_ref}) is not reaching the maximum power ratings of the SM (P_{SM_max}), but also that the amount of energy stored in the SM is enough to satisfy the (P_{SM_ref}) requirements during the required time. It will be assumed that the power ratings at the SM are in all cases large enough, and well above the maximum ratings at the demands. However, in case that the amount of remaining energy at the SM is not enough for ensuring the sustained power for a given time interval, i.e., the

SM presents a small initial SoC, the SM will provide the required amount of power only until the minimum SoC is reached, as depicted in Figure 3-13.

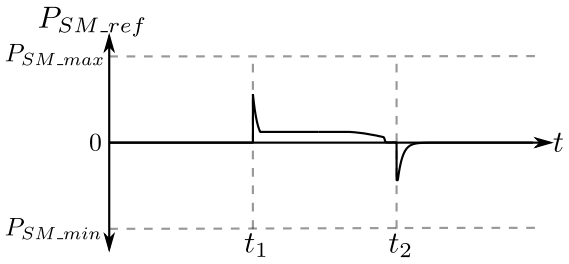
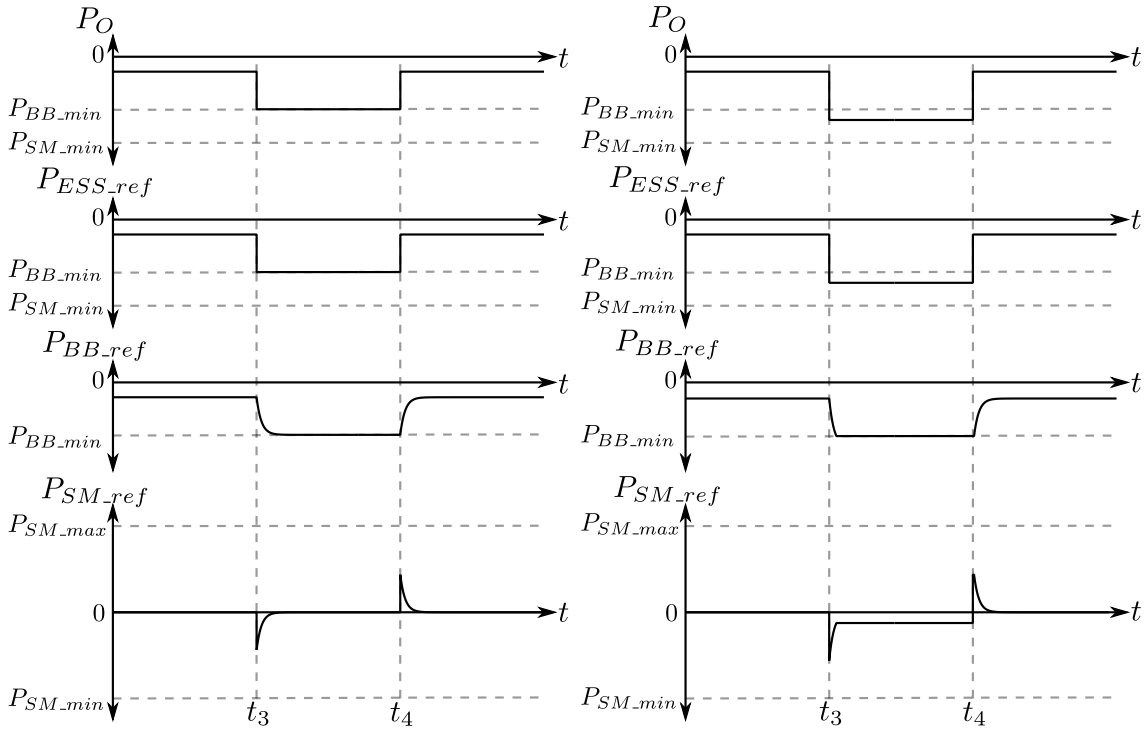


Figure 3-13: The SM power reference.

After this interval, the HESS is not able to support the required power anymore. To prevent this situation, the system might react by a set of predefined modes, such as detaching the non-critical loads, or treating this condition as a kind of saturation in the actuators (then redefining the commands by means of realizable references), etc. In any case, these operation modes are out of the scope of this work. In order to ensure that the control system will always be able to provide the required power, it is assumed that the power rating definition of the storage system is designed to be able to support the characteristic power demands. An anti-windup system will be implemented in every regulator considering the limiters mentioned in previous discussions.

The other characteristic example is sketched in Figure 3-14. It can be seen how the demanded power steps are interchanged. At the first step, the power decreases at t_3, while at the second one it increases again to the original value at t_4. For simplicity, it is assumed now that the initial demanded power is negative (power being delivered by the microgrid to the ESS). Again, the ESS power reference (P_{ESS_ref}) is equal to the power demanded (P_O). Similarly to the previous example, provided that (P_O) is greater or equal to the BB minimum power (P_{BB_min}), the SM will absorb/deliver the transient peak power and the BB will absorb the rest of power needed. This situation is depicted in Figure 3-14a. Alternatively, Figure 3-14b shows the case in which the power demanded (P_O) is smaller than the minimum BB power (P_{BB_min}). In this case, the SM will absorb/deliver the transient peak power as well as the rest of the power that BB cannot absorb for a short period as in Figure 3-14b. The same consideration about the limitations in the SoC at the SM can

be discussed, and similar premises about the limitations on the available energy and the anti-windup at the regulators are assumed.



(a) $P_{BB\_min} \leq P_O$ (b) $P_{BB\_min} > P_O$

Figure 3-14: The power references generation during the islanding mode while the BB is charging.

3.4.1.5 Generation of the Current References for the Inner Current Loops

Once the power references are obtained, the current references can be calculated by dividing the power reference for each storage device by its corresponding voltage [91].

$$I_{BB\_ref} = \frac{P_{BB\_ref}}{V_{BB\_meas}} \tag{3.43}$$

$$I_{SM\_ref} = \frac{P_{SM\_ref}}{V_{SM\_meas}} \tag{3.44}$$

where I_{BB_ref} and I_{SM_ref} are the current references for the BB and SM, respectively, in Amps.

The limits for these current references also need to be computed in real time. This is

because the voltages of BB and SM are changing as the SoC of both devices is evolving during the system operation. Therefore, dividing the power reference coming from the above algorithm by the voltage measured from the storage devices, then the current references for the BB and SM can be defined, respectively, as:

$$I_{BB\_ref} = \begin{cases} I_{BB\_min} & \frac{P_{BB\_ref}}{V_{BB\_meas}} < I_{BB\_min} \\ \frac{P_{BB\_ref}}{V_{BB\_meas}} & I_{BB\_min} \leq \frac{P_{BB\_ref}}{V_{BB\_meas}} \leq I_{BB\_max} \\ I_{BB\_max} & \frac{P_{BB\_ref}}{V_{BB\_meas}} > I_{BB\_max} \end{cases} \tag{3.45}$$

$$I_{SM\_ref} = \begin{cases} I_{SM\_min} & \frac{P_{SM\_ref}}{V_{SM\_meas}} < I_{SM\_min} \\ \frac{P_{SM\_ref}}{V_{SM\_meas}} & I_{SM\_min} \leq \frac{P_{SM\_ref}}{V_{SM\_meas}} \leq I_{SM\_max} \\ I_{SM\_max} & \frac{P_{SM\_ref}}{V_{SM\_meas}} > I_{SM\_max} \end{cases} \tag{3.46}$$

From Figure 3-1, it is clear that the current flowing through the inductors connected to both the BB and the SM are the same as the currents of the BB and the SM, respectively:

$$I_{L_1\_ref} = I_{BB\_ref} \tag{3.47}$$

$$I_{L_2\_ref} = I_{SM\_ref} \tag{3.48}$$

where $I_{L_1\_ref}$ and $I_{L_2\_ref}$ are the current references through the inductors connected to the BB (L_1) and SM (L_2), respectively, in Amps.

3.4.1.6 Design of the Inner Current Control Loops

At this point, it is necessary to select and tune the regulators for the inner current control loops. For tuning these controllers, it must be noticed that the expected dynamic behavior of both storage systems in a closed loop can be made very different. For instance, the dynamics of the regulator for the current control through the inductor at the SM converter (L_2) must be faster than the corresponding dynamics of the controller for the inductor in

the BB one (L_1). This condition will ensure that the SM inductor tracks adequately the SM current reference, which can be derived from the SM power reference (Equation (3.44)) [86].

As a consequence, this constraint in the SM current loop ensures that the SM can deliver or absorb the required transient power during fast load variations. This is because the SM voltage (V_{SM}) is relatively small, while the SM current reference (I_{SM_ref}) is quite large, as it is noticed from Equation (3.44). Given the relationship between the power references for both storage devices, it can easily be understood that the final di/dt of the battery results limited, thus protecting the device and extending the SoH.

In this case, two PI controllers in the standard form are implemented. The structure of these controllers is shown in Figure 3-15. For both control loops, the input variable of the plant under consideration is the respective inductor currents, V_{L_1} and V_{L_2}, whereas the outputs are the variables to control, i.e., I_{L_1} and I_{L_2}. Thus, the transfer functions of the plants are equal to the impedance of the converter inductors, that can be modeled by the first-order system, formed by series connection of an inductor and a resistor. Therefore, the output of the regulators will be, in both cases, the reference for the inductor voltages through the inductors. The transfer functions of the inductors connected to the ESS in Laplace transform are as follows:

$$G_{L_1}(s) = \frac{I_{L_1}(s)}{V_{L_1}(s)} = \frac{1}{L_1 \cdot s + R_1} \tag{3.49}$$

$$G_{L_2}(s) = \frac{I_{L_2}(s)}{V_{L_2}(s)} = \frac{1}{L_2 \cdot s + R_2} \tag{3.50}$$

where:

- G_{L_1} and G_{L_2} are the transfer function of the inductors connected to the BB and SM, respectively,
- I_{L_1} and I_{L_2} are the currents in the inductors connected to the BB and SM, respectively in Amps,
- V_{L_1} and V_{L_2} are the voltages across the inductors connected to the BB and SM, respectively in Volts,
- R_1 and R_2 are the parasitic resistances of the inductors connected to the BB and SM, respectively in Ohms.

Both current control loops assume that the transfer function of the switching functions in the converter are instantaneous and equal to unity. This can be guaranteed in practical setups for a switching frequency operating at least one order of magnitude above than the dynamics (bandwidth) of the current control loops. This structure allows for simple tuning of the controller, given that the target plant is a first order system that can be easily measured and characterized. The tuning of the PI inner current controllers' parameters will be explained in Chapter 6. In turn, the obtained control action from the PI regulators, in these case the inductor voltages, must be converted somehow into the real actions that will be implemented, i.e., the duty cycles of the switches at the converters.

The following paragraphs discuss this conversion, and it will be demonstrated how eventually it is going to result in a feed-forward action to compute the final duty ratio values. The estimated inductor voltages, $\hat{V}_{L_1}$ and $\hat{V}_{L_2}$ are the control actions at the output

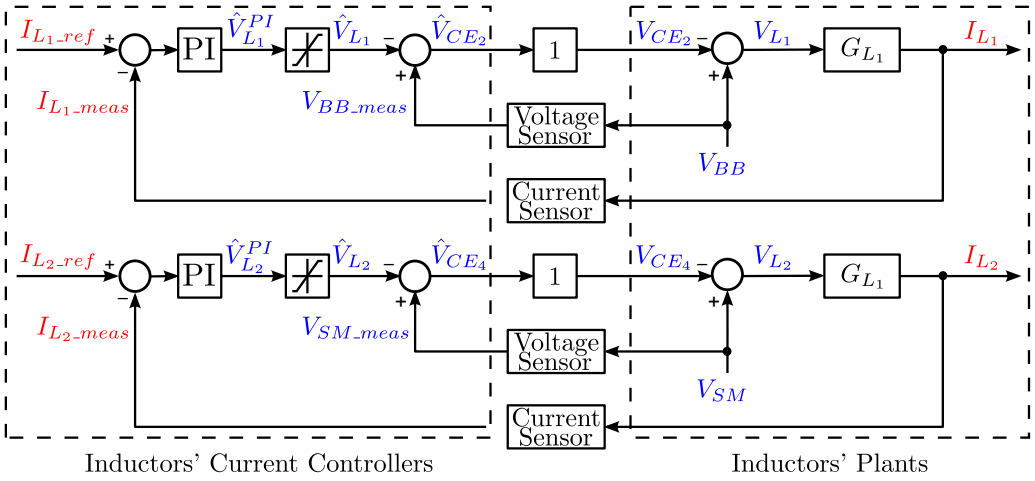


Figure 3-15: The inner current control closed loops.

of the current regulators. The limits for the inductor voltages are developed in the following discussion. Anti-windup scheme is used here to prevent the saturation of the control outputs (voltages at the inductors). By considering the transient state condition in Figure 3-1, Kirchhoff's Voltage Law (KVL) yields to the following expressions for the limit values of the inductor voltages:

$$V_{BB} - V_{L_1} - V_{CE_2} = 0 \tag{3.51}$$

$$V_{L_1} = V_{BB} - d_1 \cdot V_{DC} \tag{3.52}$$

where V_{CE_2} is the collector-emitter voltage of the IGBT$_2$ in Volts.

For the maximum duty cycle of the leg connected to the BB being equal to unity (e.g., $d_1 = 1$) (State I or State II), the following expression is found:

$$V_{L_1\_min} = V_{BB\_meas} - V_{DC\_ref} \tag{3.53}$$

where $V_{L_1\_min}$ is the minimum voltage across the inductor connected with the BB in Volts.

Conversely, when the minimum duty cycle for such leg connected to the BB is reached, and thus it equals to null (e.g., $d_1 = 0$) (State III or State IV), then:

$$V_{L_1\_max} = V_{BB\_meas} \tag{3.54}$$

where $V_{L_1\_max}$ is the maximum voltage across the inductor connected with the BB in Volts.

Now focusing at the SM branch at Figure 3-1, then:

$$V_{SM} - V_{L_2} - V_{CE_4} = 0 \tag{3.55}$$

$$V_{L_2} = V_{SM} - d_3 \cdot V_{DC} \tag{3.56}$$

where V_{CE_4} is the collector-emitter voltage of the IGBT$_4$ in Volts.

At a duty cycle of the leg connected to the SM being equal to unity (e.g., $d_3 = 1$) (State I or State IV) then it can be found that:

$$V_{L_2\_min} = V_{SM\_meas} - V_{DC\_ref} \tag{3.57}$$

where: $V_{L_2\_min}$ is the minimum voltage across the inductor connected with the SM in Volts.

Lastly, a duty cycle of the leg connected to the SM equals to null (e.g., $d_3 = 0$) (State II or State III) yields to:

$$V_{L_2\_max} = V_{SM\_meas} \tag{3.58}$$

where $V_{L_2\_max}$ is the maximum voltage across the inductor connected with the SM in Volts.

The limits for the control actions of the two PI current controllers can now be explicitly computed as:

$$\hat{V}_{L_1} = \begin{cases} V_{L_1\_min} & \hat{V}_{L_1}^{PI} < V_{L_1\_min} \\ \hat{V}_{L_1}^{PI} & V_{L_1\_min} \leq \hat{V}_{L_1}^{PI} \leq V_{L_1\_max} \\ V_{L_1\_max} & \hat{V}_{L_1}^{PI} > V_{L_1\_max} \end{cases} \tag{3.59}$$

$$\hat{V}_{L_2} = \begin{cases} V_{L_2\_min} & \hat{V}_{L_2}^{PI} < V_{L_2\_min} \\ \hat{V}_{L_2}^{PI} & V_{L_2\_min} \leq \hat{V}_{L_2}^{PI} \leq V_{L_2\_max} \\ V_{L_2\_max} & \hat{V}_{L_2}^{PI} > V_{L_2\_max} \end{cases} \tag{3.60}$$

where:

- $\hat{V}_{L_1}$ and $\hat{V}_{L_2}$ are the estimated voltage across the inductors connected to the BB and the SM after the limiter, respectively, in Volts,

- $\hat{V}_{L_1}^{PI}$ and $\hat{V}_{L_2}^{PI}$ are the estimated voltage across the inductors connected to the BB and the SM before the limiter, respectively, in Volts.

Finally, a needed adaptation between these control actions and the applied duty cycles in both converters, d_1 and d_3, is implemented in control, though the *Duty Cycle Calculation Blocks* in Figure 3-8. These blocks implement the following equations:

$$d_1 = \frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{DC\_meas}} \tag{3.61}$$

$$d_3 = \frac{V_{SM\_meas} - \hat{V}_{L_2}}{V_{DC\_meas}} \tag{3.62}$$

This results in applying a given feed-forward term for each block, which corresponds to the measured BB and SM voltages, V_{BB_meas} and V_{SM_meas} respectively. These feed-forward terms are improving the performance of the current control loops [79]. The limits

for the duty cycles are defined as follows:

$$d_1 = \begin{cases} 0 & \frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{DC\_meas}} < 0 \\ \frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{DC\_meas}} & 0 \leq \frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{DC\_meas}} \leq 1 \\ 1 & \frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{DC\_meas}} > 1 \end{cases} \tag{3.63}$$

$$d_3 = \begin{cases} 0 & \frac{V_{SM\_meas} - \hat{V}_{L_2}}{V_{DC\_meas}} < 0 \\ \frac{V_{SM\_meas} - \hat{V}_{L_2}}{V_{DC\_meas}} & 0 \leq \frac{V_{SM\_meas} - \hat{V}_{L_2}}{V_{DC\_meas}} \leq 1 \\ 1 & \frac{V_{SM\_meas} - \hat{V}_{L_2}}{V_{DC\_meas}} > 1 \end{cases} \tag{3.64}$$

These values of duty cycles are modulated through a triangular carrier waveform, in order to obtain the PWM signals. The upper switches (S_1 and S_3) are commuting with the values of the duty cycles of the BB and the SM, respectively. However, the lower switches (S_2 and S_4) are complementary:

$$d_2 = 1 - d_1 \tag{3.65}$$

$$d_4 = 1 - d_3 \tag{3.66}$$

where d_2 and d_4 are the duty cycles of the $IGBT_2$ and $IGBT_4$, respectively.

At the steady state, the voltages across the inductors are null, and therefore the duty cycles of the legs connected to the BB and SM are given by:

$$d_1 = \frac{V_{BB}}{V_{DC}} \tag{3.67}$$

$$d_3 = \frac{V_{SM}}{V_{DC}} \tag{3.68}$$

There is no need for any additional control to achieve peak shaving as during the off-peak hours, the BB charges if the generated power from the microgrid is higher than the load power. However, during the peak hours, the BB discharges in order to provide the demanded power to the loads. Given that the HESS is controlling the DC bus voltage, any surplus or lack of power will absorb/provide by the HESS.

3.4.2 Control Scheme during the Grid-Connected Mode

As stated previously, the condition for grid-tied mode operation is that the microgrid is able to interchange a net power flow with the distribution grid. In case this flow exists, it occurs through the PCC. For the case under study, the DC bus is connected to the grid by a three-phase Voltage Source Inverter (VSI) [36, 122] as shown in Figure 3-16. While other topologies might be considered for the grid interfacing, the assumption of the VSI topology does not imply any constraint in the design of the control strategies for the power interchanged with the grid. But in addition, it also ensures simplicity in the implementation of these control strategies. For instance, the scheme that manages the power flows for the HESS operation at the microgrid might include or not the control of this PCC converter. As a result, two different control strategies can be implemented. In the case that the VSI control is included in the system management, referred to as *full control strategy*, it will be shown how the performance and the dynamic behavior of the microgrid can be improved, as compared to the alternative scheme. However, this full control strategy needs a real-time communication scheme between the converters of the HESS and the grid, in order to generate the power references. This yields to a cost and complexity increase, and also to a concern for reliability aspects in the design.

On the other hand, the alternate scheme, named *independent storage control*, does not need any communication between the HESS converters and the PCC converter, resulting on a HESS control that is independent of the grid control. This increases the reliability and robustness of the system, and can easily be extended to be implemented in a manifold of distributed storage subsystems all along the microgrid resources. In fact, with this strategy, the full HESS can be attached to an existing microgrid, without modifying the operating control schemes.

In any case, the following is a basic analysis of the power flows involved in the converters depicted in Figure 3-7. Assuming that there are no losses in these converters, then:

$$P_G = I_{G_{DC}} \cdot V_{DC} \tag{3.69}$$

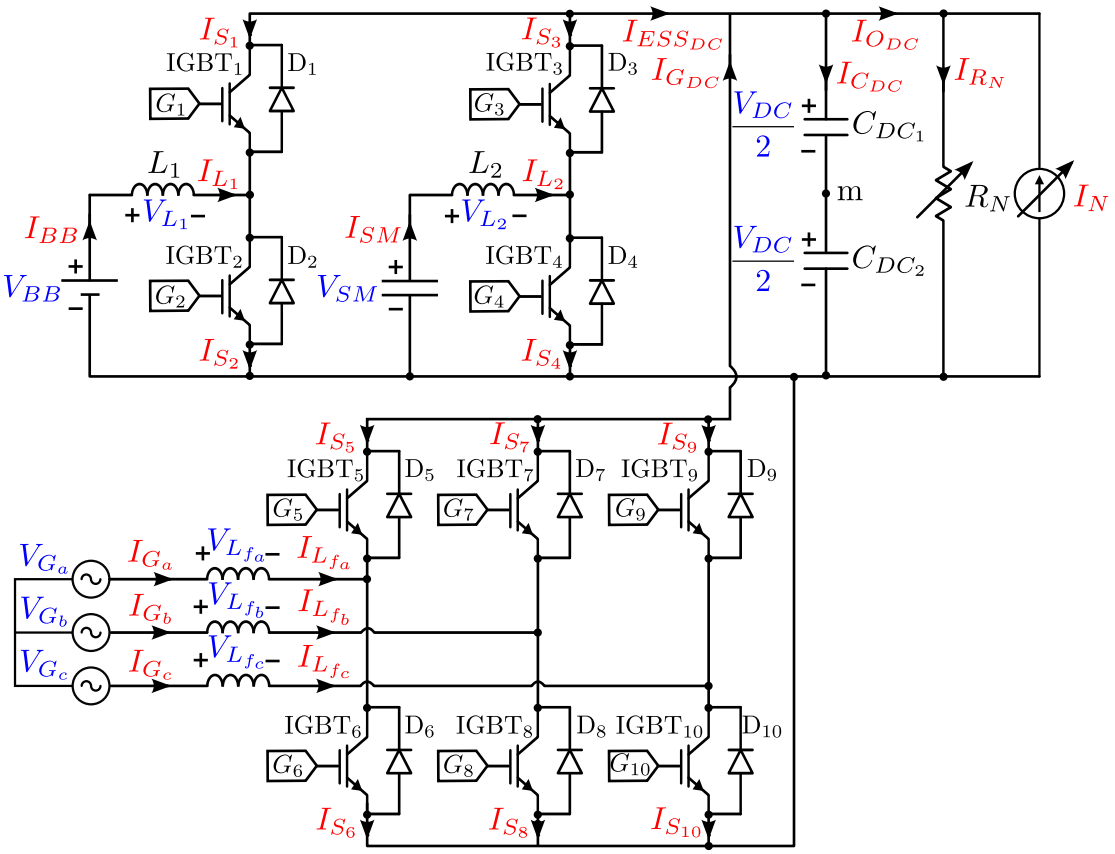


Figure 3-16: Two bidirectional buck converters connected in parallel to interface a BB and a SM, under grid-tied operation mode (connected to the grid through a VSI).

$$P_{C_{DC}} = P_{ESS} + P_G - P_O \tag{3.70}$$

$$P_{ESS} + P_G = P_{C_{DC}} + P_O = (I_{C_{DC}} + I_{O_{DC}})V_{DC} \tag{3.71}$$

where:

- P_G is the active grid power in Watts,
- $I_{G_{DC}}$ is the grid current delivered/absorbed to/from the DC microgrid in the DC side in Amps.

In steady-state conditions, the power drained from the DC bus (i.e., power extracted from the capacitor (C_{DC})) is null, and the DC bus voltage remains stable at the rated value. Upon sudden load variations, the DC bus intends to provide/absorb the corresponding power variations, yielding to a decrease/increase in the DC bus voltage. One of the main goals of the control scheme is to stabilize the system and to provide a fast recovery

in the DC bus to the desired reference value. For the case of the peak shaving strategy during the grid-connected mode, the general remarks stated previously about the share of the power at off-peak hours and peak hours can easily be implemented [112].

3.4.2.1 Independent Storage Control Strategy

As mentioned before, this strategy considers that the DC bus voltage is controlled by the three-phase VSI independently from the HESS control. The main purpose of the HESS control is to aid the VSI control in improving the recovery of the DC bus due to load variations. Therefore, the HESS is more focused on power quality aspects of the microgrid. This HESS control scheme is depicted in Figure 3-17. As in the general approach followed in this research, the SM is intended to provide/absorb the transient peak power, whereas the BB is in charge of providing/absorbing the remaining power of the storage system [99]. The general approach of this control scheme is that the reference steady-state power for the energy storage system is null, and then all the power is eventually being provided/absorbed by the grid. Nonetheless, in case that the grid power level is limited by any physical or economic constraints, the BB may also provide/absorb the excess power demand, providing some peak shaving feature up to some extent [123]. However, this approach needs some modifications to the control scheme, as it will be discussed in coming paragraphs. In any case, the control scheme is composed of two current control loops for the inductors at the storage device converters, given that the DC bus voltage control loop is out of the scope of the HESS control design.

3.4.2.1.1 Generation of the Power and Current References

The following discussion addresses the main case for the independent control, in which the peak shaving feature is not considered. The total ESS power reference ($P_{ESS\_tr\_ref}$) is generated by measuring the output power (P_{O_meas}) and filtering through a High Pass Filter (HPF) [115, 124, 125]:

$$P_{O\_meas} = I_{O_{DC}\_meas} \cdot V_{DC\_meas} \tag{3.72}$$

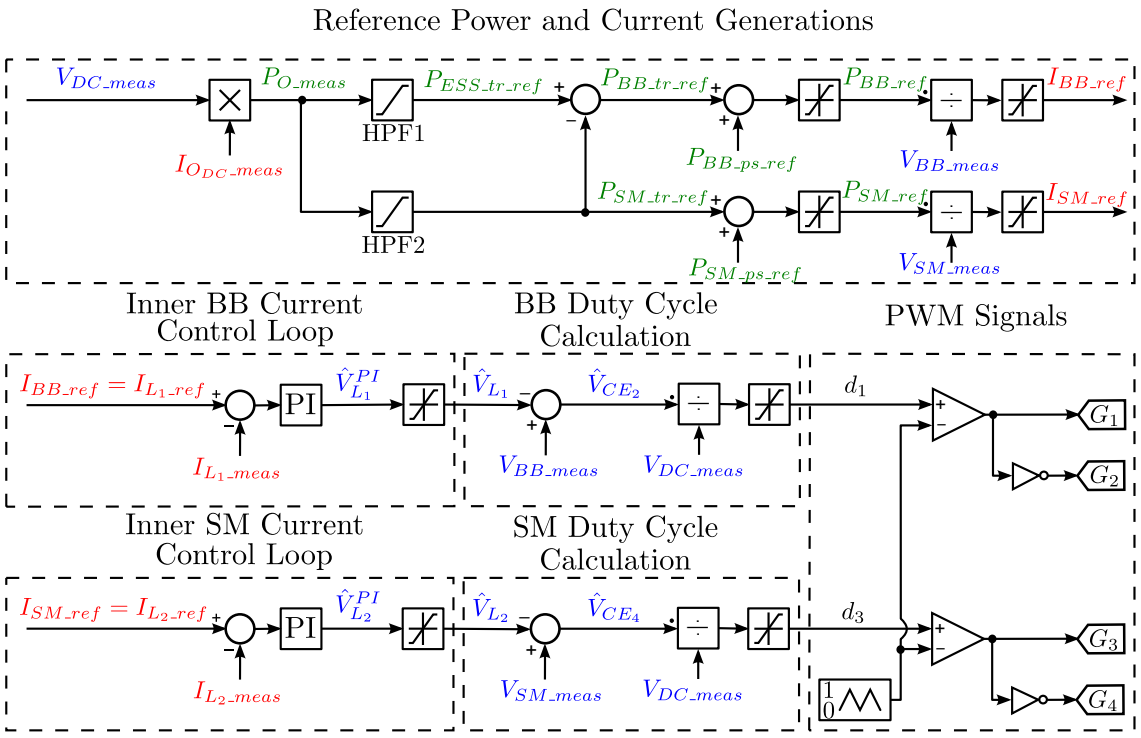


Figure 3-17: The control of the PC for the two bidirectional buck converters in order to provide or absorb transient power in case of grid-tied operation (focus on power quality).

$$P_{ESS\_tr\_ref}(s) = \underbrace{\frac{T_{ESS_{HPF}} \cdot s}{1 + T_{ESS_{HPF}} \cdot s}}_{\text{HPF}} P_{O\_meas}(s) \tag{3.73}$$

$$T_{ESS_{HPF}} = \frac{1}{2\pi \cdot f_{ESS_{HPF}}} \tag{3.74}$$

where:

- P_{O_meas} is the measured active power of the load in Watts,
- $P_{ESS\_tr\_ref}$ is the ESS transient power reference in Watts,
- $T_{ESS_{HPF}}$ is the time constant of the HPF of the ESS power in Secs,
- $f_{ESS_{HPF}}$ is the cutoff frequency of the HPF of the ESS power in Hz.

The total ESS transient power reference ($P_{ESS\_tr\_ref}$) is not directly applied to the system. Instead, the final transient SM power reference ($P_{SM\_tr\_ref}$) is generated by using a different HPF with a higher cut-off frequency, so to allow the SM to provide/absorb the

peak power reference:

$$P_{SM\_tr\_ref}(s) = \underbrace{\frac{T_{SM_{HPF}} \cdot s}{1 + T_{SM_{HPF}} \cdot s}}_{\text{HPF}} P_{O\_meas}(s) \tag{3.75}$$

$$T_{SM_{HPF}} = \frac{1}{2\pi \cdot f_{SM_{HPF}}} \tag{3.76}$$

where:

- $T_{SM_{HPF}}$ is the time constant of the HPF of the SM power in Secs,
- $f_{SM_{HPF}}$ is the cutoff frequency of the HPF of the SM power in Hz.

Then, the power transient for the BB ($P_{BB\_tr\_ref}$) is obtained as a difference between the total ESS transient power reference ($P_{ESS\_tr\_ref}$) and the SM transient power ($P_{SM\_tr\_ref}$) [89, 90]:

$$P_{BB\_tr\_ref} = P_{ESS\_tr\_ref} - P_{SM\_tr\_ref} \tag{3.77}$$

After that, the power reference for the battery control loop (P_{BB_ref}) is obtained from the transient power reference ($P_{BB\_tr\_ref}$) and the power reference from the peak shaving ($P_{BB\_ps\_ref}$) as follows:

$$P_{BB\_ref} = P_{BB\_tr\_ref} + P_{BB\_ps\_ref} \tag{3.78}$$

A limiter is used to ensure that the BB power limits are not exceeded:

$$P_{BB\_ref} = \begin{cases} P_{BB\_min} & P_{BB\_tr\_ref} + P_{BB\_ps\_ref} \\ P_{BB\_tr\_ref} + P_{BB\_ps\_ref} & P_{BB\_min} \leq P_{BB\_tr\_ref} + P_{BB\_ps\_ref} \leq P_{BB\_max} \\ P_{BB\_max} & P_{BB\_tr\_ref} + P_{BB\_ps\_ref} > P_{BB\_max} \end{cases} \tag{3.79}$$

The SM power reference (P_{SM_ref}) is calculated from the sum of the SM transient power reference ($P_{SM\_tr\_ref}$) and the power reference from the peak shaving ($P_{SM\_ps\_ref}$)

as follows:

$$P_{SM\_ref} = P_{SM\_tr\_ref} + P_{SM\_ps\_ref} \tag{3.80}$$

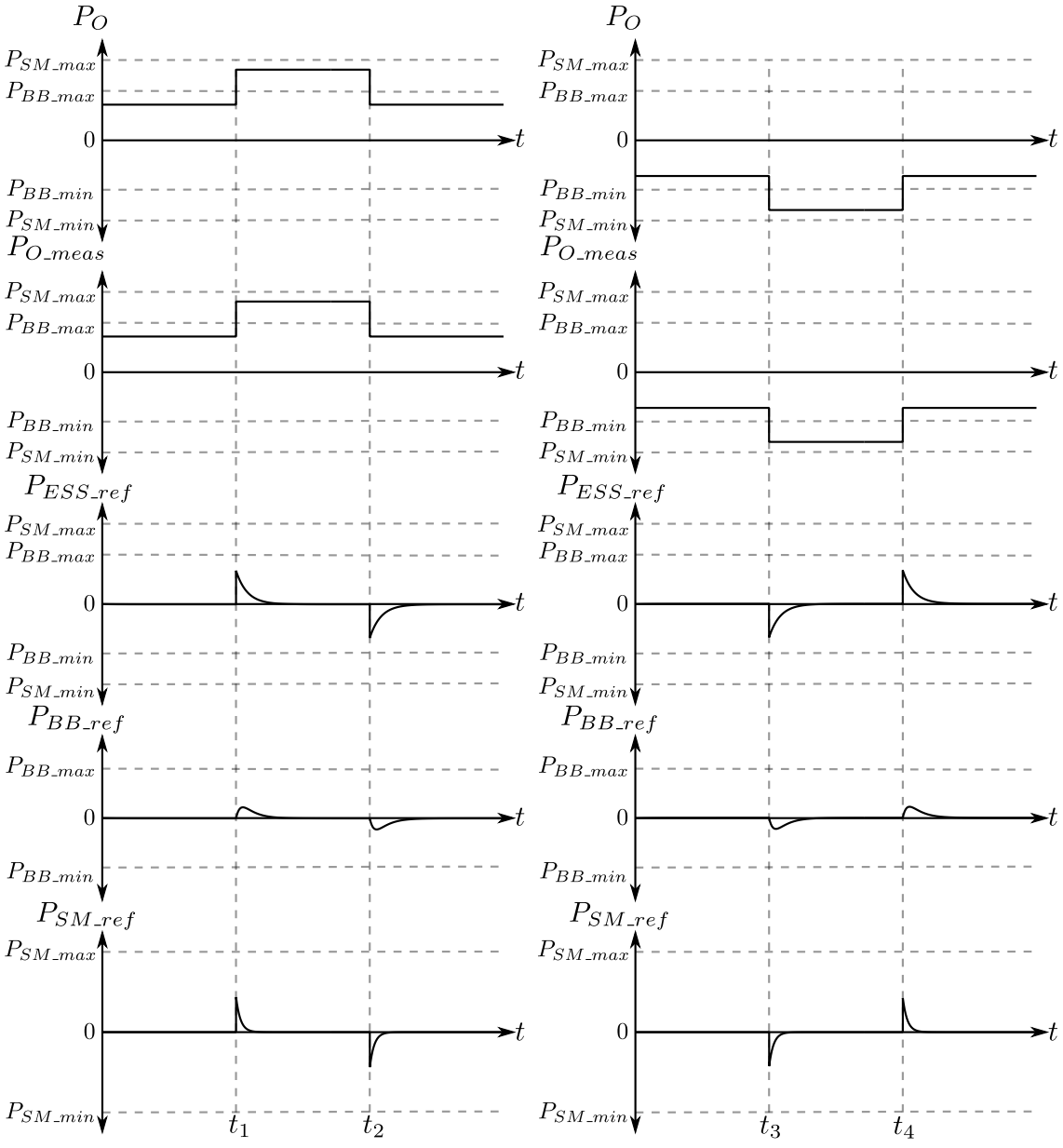
But again, a limiter must be included here to ensure that the SM power limits are not exceeded:

$$P_{SM\_ref} = \begin{cases} P_{SM\_min} & P_{SM\_tr\_ref} + P_{SM\_ps\_ref} < P_{SM\_min} \\ P_{SM\_tr\_ref} + P_{SM\_ps\_ref} & P_{SM\_min} \leq P_{SM\_tr\_ref} + P_{SM\_ps\_ref} \leq P_{SM\_max} \\ P_{SM\_max} & P_{SM\_tr\_ref} + P_{SM\_ps\_ref} > P_{SM\_max} \end{cases} \tag{3.81}$$

Once the power reference values are obtained, the current references of the BB and SM loops are calculated by dividing there power references by respective BB and SM measured voltages as in Equations (3.43) and (3.44). The rest of the control scheme is the same as in the case of the islanding mode control design. Then two PI current controllers are implemented. The bandwidth for SM current controller is faster than the BB current controller. The limits for the control action are defined as in Equations (3.59) and (3.60). Finally, the duty cycles of the upper switches of each ESS converter are calculated as in Equations (3.61) and (3.62). The limits for the duty cycles are defined as in Equations (3.63) and (3.64).

Figure 3-18a shows the evolution of the instantaneous power values along the HESS elements when the discussed control is applied. Again the performance of the control scheme is illustrated considering a characteristic sequence of two symmetric power steps in the demanded power (P_O) from the microgrid. It is assumed that the power references for the ESS are null ($P_{BB\_ps\_ref} = P_{SM\_ps\_ref} = 0$). As it can be seen, initially the demanded power step is positive, then increased at t_1 and then decreased back to the original level at t_2. The measured demanded power (P_{O_meas}) is also represented, and it is assumed to be equal to the demanded power (P_O). The ESS power reference (P_{ESS_ref}) will deliver/absorb the generated transient power, as sketched in Figure 3-18a. This ESS power reference (P_{ESS_ref}) is shared between the BB and the SM. As stated previously, the SM

delivers/absorbs transient peak power, while the BB provides/absorbs the rest of the transient power.



(a) $P_O > 0$ (b) $P_O < 0$

Figure 3-18: The power references generation during the grid-connected mode (Independent Storage Control).

Also, the opposite initial condition might be considered. The main power waveforms for an initial situation in which the starting power is delivered from the microgrid are depicted in Figure 3-18b. Now, the most adverse condition is that the demanded power (P_O)

initially decreases at t_3, and increasing back again to the original level after a given time at t_4. Still, the measured demanded power (P_{O_meas}) is the same as the demanded power (P_O). The rest of the power waveforms, for the ESS, the BB and the BB are defined in the same manner than in the previous case. In any case, as seen from Figure 3-18 the limit constraints in the BBand SM power values must be ensured at all times.

3.4.2.1.2 Control of the Voltage Source Inverter

A basic scheme of the VSI control connected to the grid at the PCC is shown in Figure 3-19. Besides effectively controlling the shape of the instant currents at the grid side, it is assumed that this VSI also maintains the DC bus of the microgrid constant [86, 113, 126, 127]. The overall control scheme consists of the outer DC bus voltage control loop and two inner current control loops in d-q coordinates.

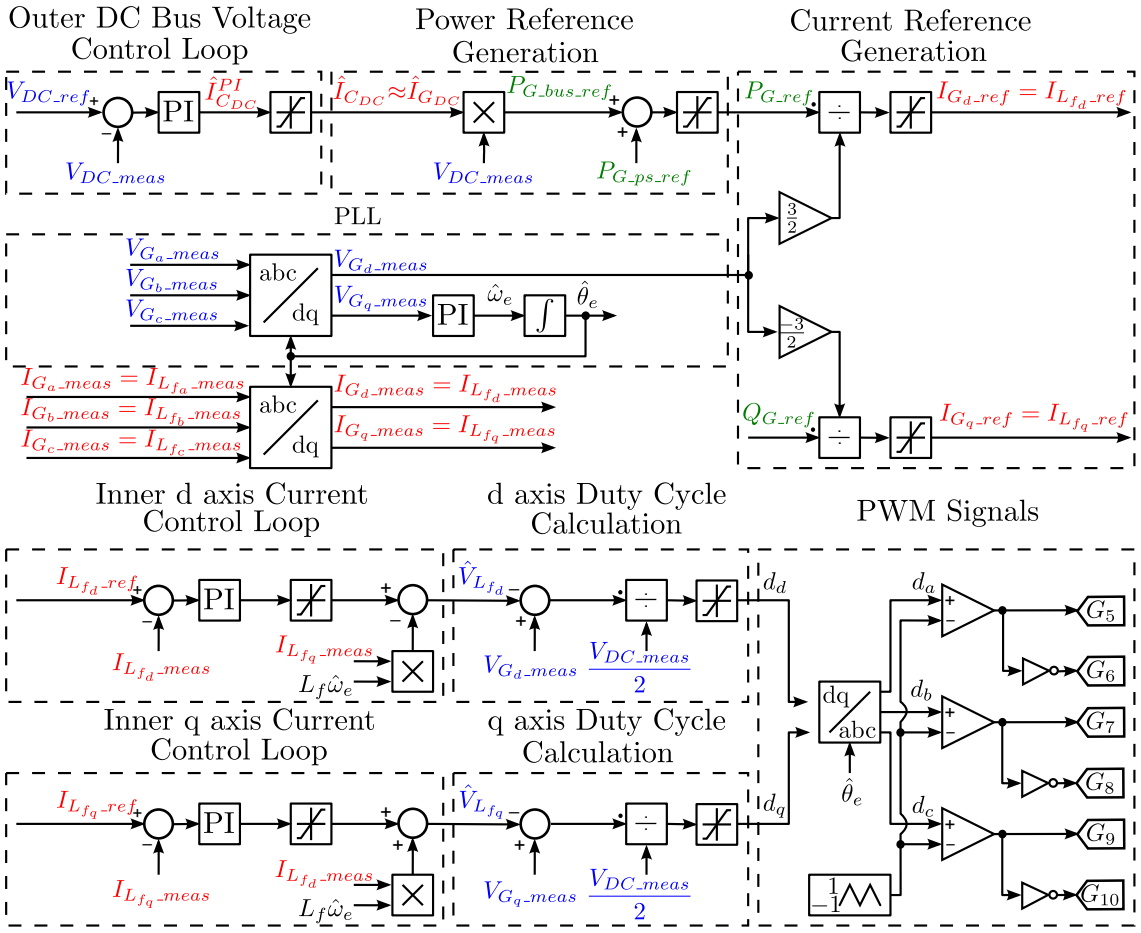


Figure 3-19: The control of the VSI in order to maintain the DC bus voltage fixed.

The outer DC bus voltage control loop performs similarly than in the case of the islanding mode. However, the limits for the control action ($\hat{I}_{C_{DC}}$) are in this case different. In order to calculate these limits, a KCL in Figure 3-16 is applied:

$$I_{ESS_{DC}} + I_{G_{DC}} = I_{O_{DC}} + I_{C_{DC}} \tag{3.82}$$

Unlike the full control strategy, now the feed-forward term coming from load variations cannot be directly applied. This would imply the use of this information as control variables at the VSI control stage, or at least a high-speed communications link that is not generally available. Therefore, the transient load and the performance of the ESS are considered as perturbations in control, and will not be considered in the control design. In turn, the control system is designed considering the parameters at the DC bus and the VSI converter, assuming that:

$$I_{C_{DC}} \approx I_{G_{DC}} = \frac{P_G}{V_{DC}} \tag{3.83}$$

The lower limit for this current is calculated as follows:

$$I_{C_{DC\_min}} = \frac{P_{G\_min}}{V_{DC\_ref}} \tag{3.84}$$

where P_{G_min} is the minimum grid active power (the maximum power absorbed from the grid) in Watts.

On the other side, the upper limit can be expressed as:

$$I_{C_{DC\_max}} = \frac{P_{G\_max}}{V_{DC\_ref}} \tag{3.85}$$

where P_{G_max} is the maximum active grid power (the maximum power delivered from the grid) in Watts.

Then, the active grid power reference from the DC bus voltage control ($P_{G\_bus\_ref}$) is

calculated from the control action term ($\hat{I}_{C_{DC}}$) as given by:

$$P_{G\_bus\_ref} = \hat{I}_{C_{DC}} \cdot V_{DC\_meas} \tag{3.86}$$

The grid active power reference (P_{G_ref}) is obtained from the sum of the grid active power reference from the DC bus control ($P_{G\_bus\_ref}$) and the power reference from peak shaving as follows:

$$P_{G\_ref} = P_{G\_bus\_ref} + P_{G\_ps\_ref} \tag{3.87}$$

Notice that there is a limiter for the active grid power as follows:

$$P_{G\_ref} = \begin{cases} P_{G\_min} & P_{G\_bus\_ref} + P_{G\_ps\_ref} < P_{G\_min} \\ P_{G\_bus\_ref} + P_{G\_ps\_ref} & P_{G\_min} \leq P_{G\_bus\_ref} + P_{G\_ps\_ref} \leq P_{G\_max} \\ P_{G\_max} & P_{G\_bus\_ref} + P_{G\_ps\_ref} > P_{G\_max} \end{cases} \tag{3.88}$$

The reactive grid power (Q_{G_ref}) is controlled as to improve the power quality in a relatively weak microgrid. A rigorous, detailed derivation for calculating the active and reactive power in the system [6] is explained in Appendix A. The grid active power and reactive power for the three-phase balanced system is obtained as follows:

$$P_{G\_ref} = \frac{3}{2}(V_{G_{d}\_meas} \cdot I_{G_{d}\_ref} + V_{G_{q}\_meas} \cdot I_{G_{q}\_ref}) \tag{3.89}$$

$$Q_{G\_ref} = \frac{3}{2}(V_{G_{q}\_meas} \cdot I_{G_{d}\_ref} - V_{G_{d}\_meas} \cdot I_{G_{q}\_ref}) \tag{3.90}$$

where:

- Q_{G_ref} is the reactive grid power reference in Volt-Amps-Reactive,
- $V_{G_{d}\_meas}$ and $V_{G_{q}\_meas}$ are the measured grid voltage in d and q axes, receptively, in Volts,
- $I_{G_{d}\_ref}$ and $I_{G_{q}\_ref}$ are the grid current references in d and q axes, respectively, in Amps.

In order to synchronize with the grid, a vector control scheme using the d-q synchronous

reference frame is going to be used. The phase angle of the grid voltages is extracted utilizing a Phase Locked Loop (PLL) block [128–131]. The d-axis of the synchronous reference frame is aligned with the grid voltage, ($V_{G_d} = V_G$); and the q-axis component is equal to zero: ($V_{G_q} = 0$) [6, 66, 132]. Therefore, the power equations reduce to:

$$P_{G\_ref} = \frac{3}{2} V_{G_d\_meas} I_{G_d\_ref} \tag{3.91}$$

$$Q_{G\_ref} = -\frac{3}{2} V_{G_d\_meas} I_{G_q\_ref} \tag{3.92}$$

The current references of the grid in d and q axes are calculated as follows:

$$I_{G_d\_ref} = \frac{P_{G\_ref}}{\frac{3}{2} V_{G_d\_meas}} \tag{3.93}$$

$$I_{G_q\_ref} = \frac{-Q_{G\_ref}}{\frac{3}{2} V_{G_d\_meas}} \tag{3.94}$$

The limits of the current references are as given by:

$$I_{G_d\_ref} = \begin{cases} I_{G_d\_min} & \frac{P_{G\_ref}}{\frac{3}{2} V_{G_d\_meas}} < I_{G_d\_min} \\ \frac{P_{G\_ref}}{\frac{3}{2} V_{G_d\_meas}} & I_{G_d\_min} \leq \frac{P_{G\_ref}}{\frac{3}{2} V_{G_d\_meas}} \leq I_{G_d\_max} \\ I_{G_d\_max} & \frac{P_{G\_ref}}{\frac{3}{2} V_{G_d\_meas}} > I_{G_d\_max} \end{cases} \tag{3.95}$$

$$I_{G_q\_ref} = \begin{cases} I_{G_q\_min} & \frac{-Q_{G\_ref}}{\frac{3}{2} V_{G_d\_meas}} < I_{G_q\_min} \\ \frac{-Q_{G\_ref}}{\frac{3}{2} V_{G_d\_meas}} & I_{G_q\_min} \leq \frac{-Q_{G\_ref}}{\frac{3}{2} V_{G_d\_meas}} \leq I_{G_q\_max} \\ I_{G_q\_max} & \frac{-Q_{G\_ref}}{\frac{3}{2} V_{G_d\_meas}} > I_{G_q\_max} \end{cases} \tag{3.96}$$

where:

- $I_{G_d\_min}$ and $I_{G_d\_max}$ are the minimum and maximum grid current in d axis, respectively, in Amps,
- $I_{G_q\_min}$ and $I_{G_q\_max}$ are the minimum and maximum grid current in q axis, respectively, in Amps.

Hence, the current references of the filter inductors in d and q axes are the same as the

current references of the grid:

$$I_{L_{f_d}\_ref} = I_{G_d\_ref} \tag{3.97}$$

$$I_{L_{f_q}\_ref} = I_{G_q\_ref} \tag{3.98}$$

where $I_{L_{f_d}\_ref}$ and $I_{L_{f_q}\_ref}$ are the current references in the filter inductors in d and q axes, respectively, in Amps.

Finally, the vector control implemented can be seen in Figure 3-20. Two current control loops are used for d and q axes in the ideal form [128]. A detailed derivation of the voltage across the filter in d-q axes is explained in Appendix A. In order to improve the disturbance rejection, the decoupling term is added [133]. The decoupling term in Laplace transform can be calculated as follows [6, 115]:

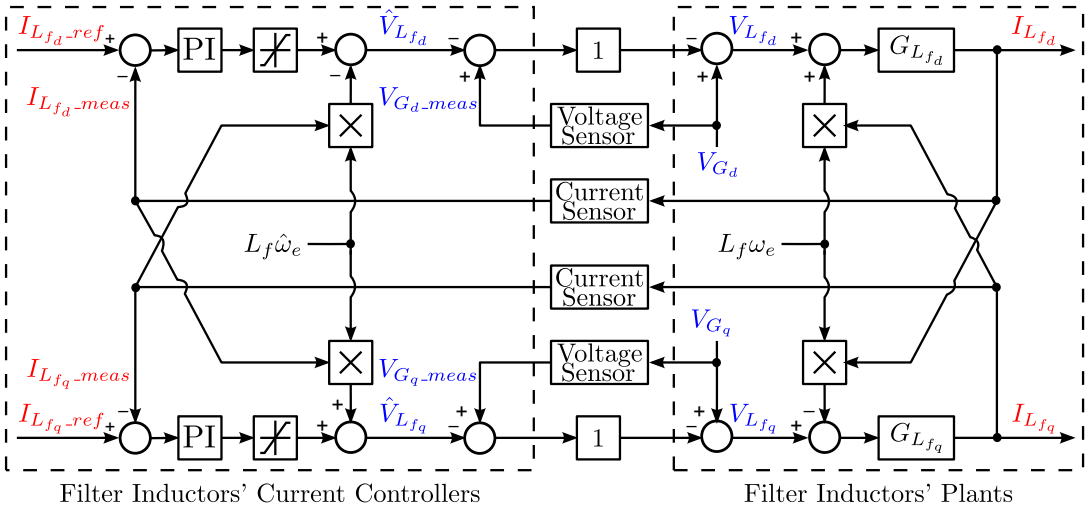


Figure 3-20: The inner current control closed loops in d and q axes.

$$V_{L_{f_d}}(s) = I_{L_{f_d}}(s)(R_f + L_f \cdot s) - \underbrace{I_{L_{f_q}}(s) \cdot L_f \cdot \omega_e}_{\text{Decoupling Term}} \tag{3.99}$$

$$V_{L_{f_q}}(s) = I_{L_{f_q}}(s)(R_f + L_f \cdot s) + \underbrace{I_{L_{f_d}}(s) \cdot L_f \cdot \omega_e}_{\text{Decoupling Term}} \tag{3.100}$$

where:

- $V_{L_{f_d}}$ and $V_{L_{f_q}}$ are the voltages across the filter inductors in d and q axes, respectively, in Volts,

- $I_{L_{f_d}}$ and $I_{L_{f_q}}$ are the currents in the filter inductors in d and q axes, respectively, in Amps,
- R_f is the resistance of the filter in Ohms,
- L_f is the inductance of the filter in Henries,
- ω_e is the grid frequency in rads/sec.

The transfer functions of the filter inductors in Laplace transform are as follows:

$$G_{L_{f_d}}(s) = \frac{I_{L_{f_d}}(s)}{V_{L_{f_d}}(s) + I_{L_{f_q}}(s) \cdot L_f \cdot \omega_e} = \frac{1}{L_f \cdot s + R_f} \tag{3.101}$$

$$G_{L_{f_q}}(s) = \frac{I_{L_{f_q}}(s)}{V_{L_{f_q}}(s) - I_{L_{f_d}}(s) \cdot L_f \cdot \omega_e} = \frac{1}{L_f \cdot s + R_f} \tag{3.102}$$

where $G_{L_{f_d}}$ and $G_{L_{f_q}}$ are the transfer function of the filter inductors in d and q axes, respectively.

As the core of the control design, the tuning of the parameters of the PI current vector controllers will be explained in Chapter 6.

The detailed derivation of the inductor voltage of the filter in d-q axes, as a function of the grid voltage and the DC bus voltage, can be found in Appendix A. The expressions for these inductor voltage values can then be expressed as:

$$V_{L_{f_d}} = V_{G_d} - d_{G_d}\frac{V_{DC}}{2} \tag{3.103}$$

$$V_{L_{f_q}} = V_{G_q} - d_{G_d}\frac{V_{DC}}{2} \tag{3.104}$$

where:

- V_{G_d} and V_{G_q} are the grid voltage in d and q axes in Volts,
- d_{G_d} and d_{G_q} are the grid duty cycles in d and q axes.

In order to obtain the minimum operating limits for the control action (inductor voltage of the filter) in d and in q axes, the duty ratios at both axes are made equal to one:

$$V_{L_{f_d}\_min} = V_{G_d\_meas} - \frac{V_{DC\_ref}}{2} \tag{3.105}$$

$$V_{L_{f_q}\_min} = V_{G_q\_meas} - \frac{V_{DC\_ref}}{2} \tag{3.106}$$

where $V_{L_{f_d}\_min}$ and $V_{L_{f_q}\_min}$ are the minimum voltages across the filter inductors in d and q axes, respectively, in Volts.

On the other hand, aiming to obtain the maximum limits for the control action (inductor voltage of the filter) in d and q axes, then these duty ratios are made equal to minus one:

$$V_{L_{f_d}\_max} = V_{G_d\_meas} + \frac{V_{DC\_ref}}{2} \tag{3.107}$$

$$V_{L_{f_q}\_max} = V_{G_q\_meas} + \frac{V_{DC\_ref}}{2} \tag{3.108}$$

where $V_{L_{f_d}\_max}$ and $V_{L_{f_q}\_max}$ are the maximum voltages across the filter inductors in d and q axes, respectively, in Volts.

From the above sets of equations, the limits for the control actions of the current controllers (the voltage across the inductors) in d and q axes is given by:

$$\hat{V}_{L_{f_d}} = \begin{cases} V_{L_{f_d}\_min} & \hat{V}^{PI}_{L_{f_d}} < V_{L_{f_d}\_min} \\ \hat{V}^{PI}_{L_{f_d}} & V_{L_{f_d}\_min} \leq \hat{V}^{PI}_{L_{f_d}} \leq V_{L_{f_d}\_max} \\ V_{L_{f_d}\_max} & \hat{V}^{PI}_{L_{f_d}} > V_{L_{f_d}\_max} \end{cases} \tag{3.109}$$

$$\hat{V}_{L_{f_q}} = \begin{cases} V_{L_{f_q}\_min} & \hat{V}^{PI}_{L_{f_q}} < V_{L_{f_q}\_min} \\ \hat{V}^{PI}_{L_{f_q}} & V_{L_{f_q}\_min} \leq \hat{V}^{PI}_{L_{f_q}} \leq V_{L_{f_q}\_max} \\ V_{L_{f_q}\_max} & \hat{V}^{PI}_{L_{f_q}} > V_{L_{f_q}\_max} \end{cases} \tag{3.110}$$

where:

- $\hat{V}_{L_{f_d}}$ and $\hat{V}_{L_{f_q}}$ are the estimated voltages across the filter inductors in d and q axes after the limiter, respectively, in Volts,
- $\hat{V}^{PI}_{L_{f_d}}$ and $\hat{V}^{PI}_{L_{f_q}}$ are the estimated voltage across the filter inductors in d and q axes before the limiter, respectively, in Volts.

The values of the duty cycles in both d and q axes, derived in detail in Appendix A, can be expressed as:

$$d_{G_d} = \frac{V_{G_d\_meas} - \hat{V}_{L_{f_d}}}{\frac{V_{DC\_meas}}{2}} \tag{3.111}$$

$$d_{G_q} = \frac{V_{G_{q\_meas}} - \hat{V}_{L_{f_q}}}{\frac{V_{DC\_meas}}{2}} \tag{3.112}$$

The limits for the grid duty cycles in d and q axes are defined as follows:

$$d_{G_d} = \begin{cases} -1 & \frac{V_{G_{d\_meas}} - \hat{V}_{L_{f_d}}}{\frac{V_{DC\_meas}}{2}} < -1 \\ \frac{V_{G_{d\_meas}} - \hat{V}_{L_{f_d}}}{\frac{V_{DC\_meas}}{2}} & -1 \leq \frac{V_{G_{d\_meas}} - \hat{V}_{L_{f_d}}}{\frac{V_{DC\_meas}}{2}} \leq 1 \\ 1 & \frac{V_{G_{d\_meas}} - \hat{V}_{L_{f_d}}}{\frac{V_{DC\_meas}}{2}} > 1 \end{cases} \tag{3.113}$$

$$d_{G_q} = \begin{cases} -1 & \frac{V_{G_{q\_meas}} - \hat{V}_{L_{f_q}}}{\frac{V_{DC\_meas}}{2}} < -1 \\ \frac{V_{G_{q\_meas}} - \hat{V}_{L_{f_q}}}{\frac{V_{DC\_meas}}{2}} & -1 \leq \frac{V_{G_{q\_meas}} - \hat{V}_{L_{f_q}}}{\frac{V_{DC\_meas}}{2}} \leq 1 \\ 1 & \frac{V_{G_{q\_meas}} - \hat{V}_{L_{f_q}}}{\frac{V_{DC\_meas}}{2}} > 1 \end{cases} \tag{3.114}$$

Finally, the duty cycles for the switches at the three-phases of the VSI, d_{G_a}, d_{G_b} and d_{G_c}, can be obtained from the duty cycles in d and q coordinates, d_{G_d} and d_{G_q}, respectively, through the dq-abc standard transformation. The upper switches (S_5, S_7 and S_9) are commuting with the values of the duty cycles of the three-phases a, b and c, respectively. However, the lower Ss (S_6, S_8 and S_{10}) follow a complementary pattern with respect to their respective upper switches:

$$d_5 = d_{G_a} \tag{3.115}$$

$$d_6 = 1 - d_{G_a} \tag{3.116}$$

$$d_7 = d_{G_b} \tag{3.117}$$

$$d_8 = 1 - d_{G_b} \tag{3.118}$$

$$d_9 = d_{G_c} \tag{3.119}$$

$$d_{10} = 1 - d_{G_c} \tag{3.120}$$

where:

- d_5, d_6, d_7, d_8, d_9 and d_{10} are the duty cycles of the $IGBT_5$, $IGBT_6$,$IGBT_7$, $IGBT_8$, $IGBT_9$ and $IGBT_{10}$, respectively,
- d_{G_a}, d_{G_b} and d_{G_c} are the duty cycles of the three-phase, respectively.

3.4.2.2 Full Control Strategy

The other approach considered for the control strategy is, as stated in the previous paragraphs, the full control scheme. Figure 3-21 shows this approach, being the DC bus controlled by a coordinated scheme of the grid converter and the HESS converters controls.

As in the previous case, the grid is providing/absorbing the steady-state power; the transient peak power is delivered/absorbed by the SM, and finally, the rest of the transient power is delivered/absorbed by the BB. The coordination of the strategies is effectively achieved through the implementation of a control scheme that consists of one outer loop for the DC bus voltage and four inner loops for the inductor's current. It must be noticed that this strategy assumes ideal information flows between the different control stages involved. This ultimately implies the need for implementing a real-time communications subsystem between the grid converter and the HESS converters. This ensures the generation of the required synchronized and coordinated power references for every control loop in the system.

The keystone of the system management is the control of the DC bus capacitor voltage. This voltage control is inherently providing a power flow balance between all the agents in the system, i.e., the grid (through the PCC VSI converter), the HESS system (through the BB and SM converters) and the rest of the microgrid resources (loads and generation elements). In steady state, the DC bus capacitor power is null. However, upon any variation in this capacitor voltage, due to any change in the load/generation scheme, will force the control loops to react as to oppose to this change. The following discussion details the role of the distinct control loops in the overall control system. First, the DC bus is controlled by an outer PI controller in the ideal form as discussed before. However, the limits for the control action ($\hat{I}_{C_{DC}}$) are, again, different. Starting from Equation (3.82), the limits are

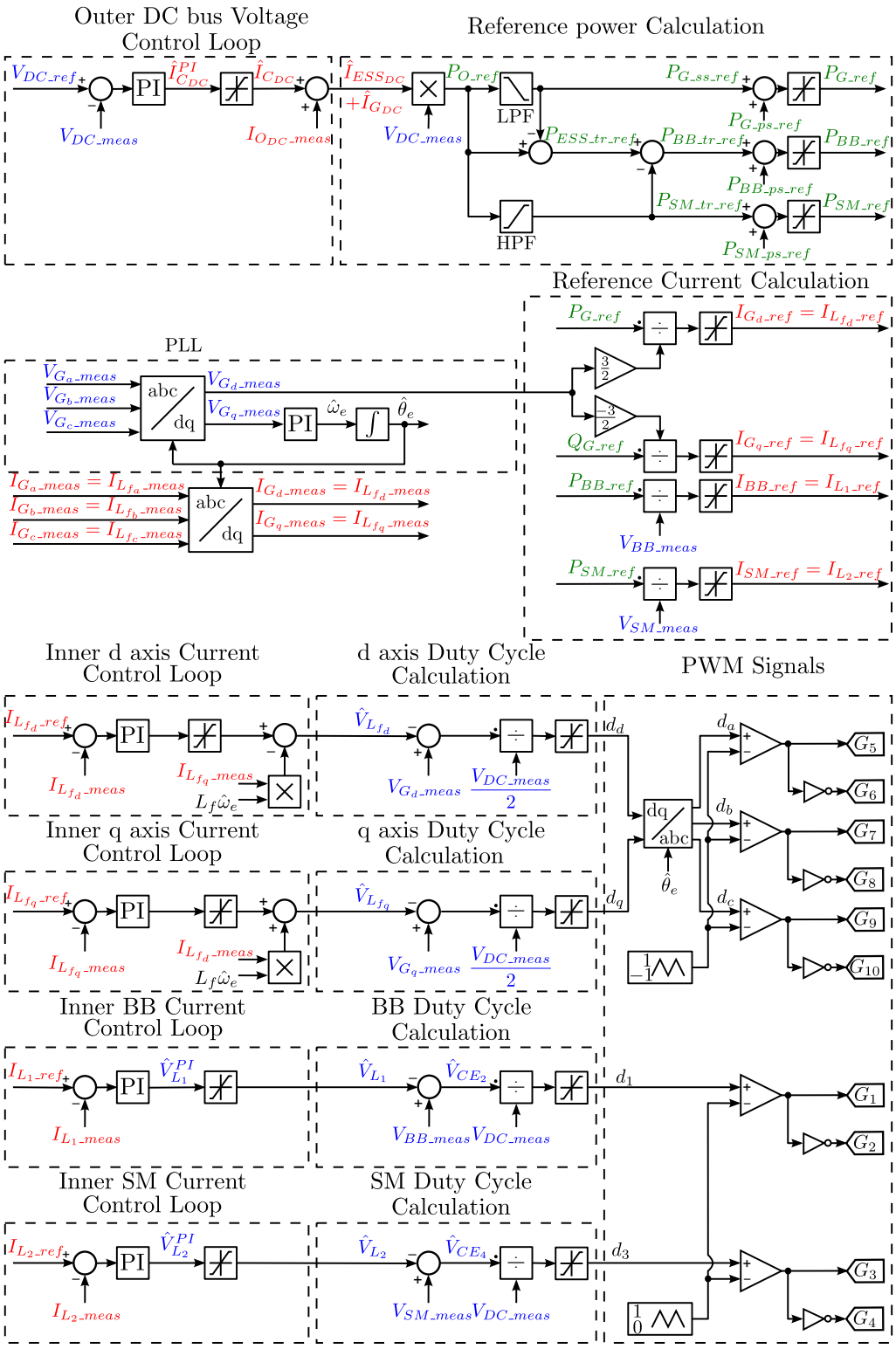


Figure 3-21: The control of the PC of the two bidirectional buck converters and the VSI in case grid-connected (Full Control).

calculated as follows:

$$d_1 \cdot I_{BB} + d_3 \cdot I_{SM} + \frac{P_G}{V_{DC}} = I_{R_N} - I_N + I_{C_{DC}} \tag{3.121}$$

$$I_{C_{DC}} = d_1 \cdot I_{BB} + d_3 \cdot I_{SM} + \frac{P_G}{V_{DC}} + I_N - \frac{P_{R_N}}{V_{DC}} \tag{3.122}$$

In order to obtain the lower limit, the duty cycles of the BB and the SM are made equal to unity (state I):

$$I_{C_{DC}\_min} = I_{BB\_min} + I_{SM\_min} + \frac{P_{G\_min}}{V_{DC\_ref}} + I_{N\_min} - \frac{P_{R_N\_max}}{V_{DC\_ref}} \tag{3.123}$$

Besides that, to obtain the upper limit, the duty cycles of the BB and SM should be made equal to zero (state III):

$$I_{C_{DC}\_max} = I_{BB\_max} + I_{SM\_max} + \frac{P_{G\_max}}{V_{DC\_ref}} + I_{N\_max} - \frac{P_{R_N\_min}}{V_{DC\_ref}} \tag{3.124}$$

On the other hand, the output power reference (P_{O_ref}) is calculated from the control action of the voltage controller ($\hat{I}_{C_{DC}}$) and the feed-forward term (I_{O_meas}):

$$P_{O\_ref} = V_{DC\_meas}(\hat{I}_{C_{DC}} + I_{O\_meas}) \tag{3.125}$$

This allows for the calculation of the steady-state active grid power reference ($P_{G\_ss\_ref}$), by applying a LPF to the output power reference (P_{O_ref}):

$$P_{G\_ss\_ref} = \underbrace{\frac{1}{1 + T_{G_{LPF}} \cdot s}}_{\text{LPF}} P_{O\_ref} \tag{3.126}$$

$$T_{G_{LPF}} = \frac{1}{2\pi \cdot f_{G_{LPF}}} \tag{3.127}$$

where:

- $P_{G\_ss\_ref}$ is the steady-state active grid power reference in Watts,
- $T_{G_{LPF}}$ is the time constant of the LPF of the active grid power in Secs,
- $f_{G_{LPF}}$ is the cutoff frequency of the LPF of the active grid power in Hz.

Then, the active grid power reference (P_{G_ref}) is calculated as the sum of the steady-state active grid power reference ($P_{G\_ss\_ref}$) and the power reference from peak shaving ($P_{G\_ps\_ref}$) as follows:

$$P_{G\_ref} = P_{G\_ss\_ref} + P_{G\_ps\_ref} \tag{3.128}$$

A limiter for the active grid power is obtained, given that:

$$P_{G\_ref} = \begin{cases} P_{G\_min} & P_{G\_ss\_ref} + P_{G\_ps\_ref} < P_{G\_min} \\ P_{G\_ss\_ref} + P_{G\_ps\_ref} & P_{G\_min} \leq P_{G\_ss\_ref} + P_{G\_ps\_ref} \leq P_{G\_max} \\ P_{G\_max} & P_{G\_ss\_ref} + P_{G\_ps\_ref} > P_{G\_max} \end{cases} \tag{3.129}$$

The transient ESS power reference ($P_{ESS\_ss\_ref}$) can be obtained from the difference between the output power reference (P_{O_ref}) and the steady-state grid active power reference ($P_{G\_ss\_ref}$):

$$P_{ESS\_tr\_ref} = P_{O\_ref} - P_{G\_ss\_ref} \tag{3.130}$$

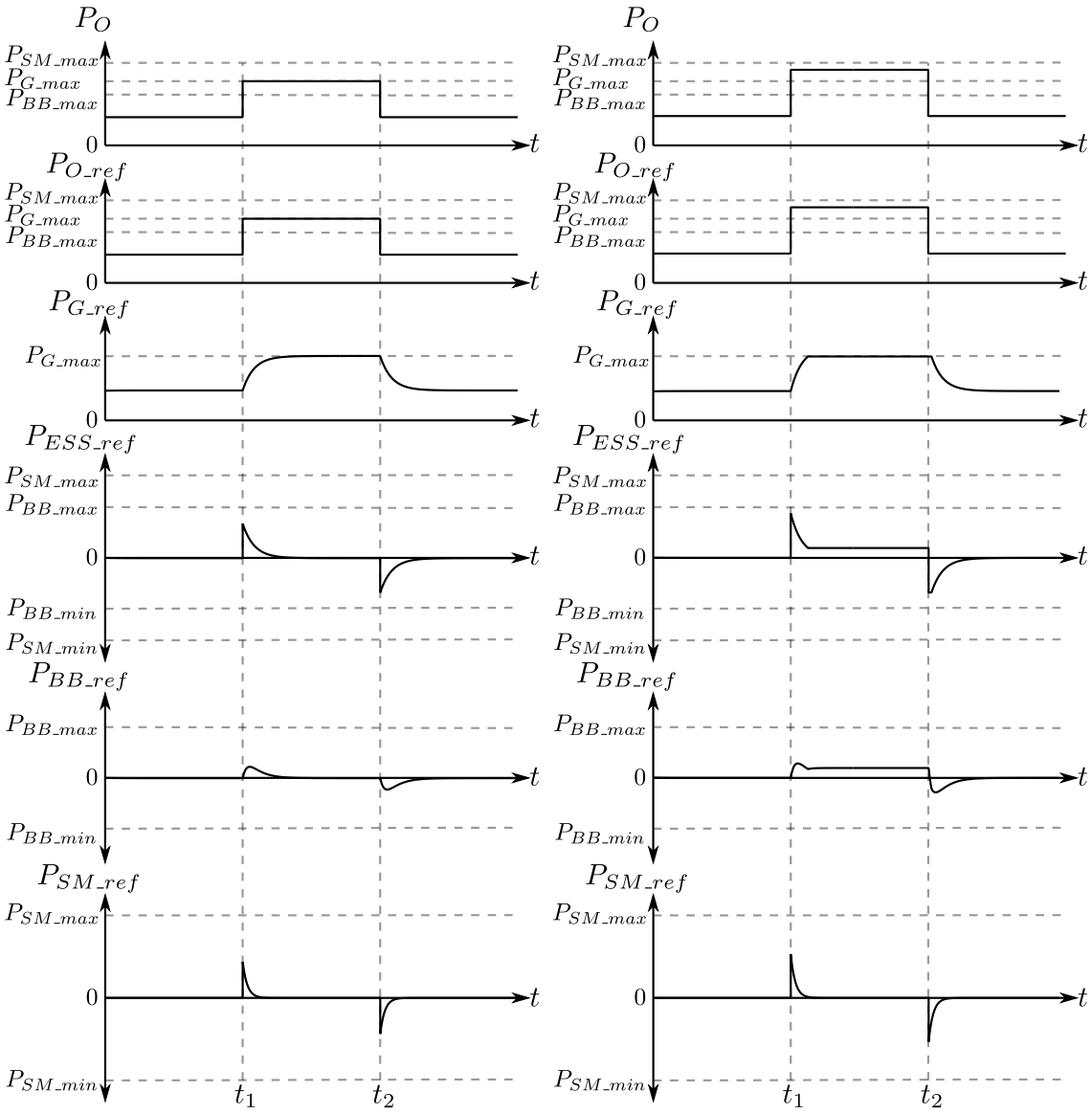
Once the global transient ESS power reference ($P_{ESS\_tr\_ref}$) is known, it can be split into the individual storage device power references. Firstly, the SM power reference ($P_{SM\_tr\_ref}$) can be expressed, again by applying a HPF to the output power reference (P_{O_ref}):

$$P_{SM\_tr\_ref} = \underbrace{\frac{T_{SM\_HPF} \cdot s}{1 + T_{SM\_HPF} \cdot s}}_{\text{HPF}} P_{O\_ref} \tag{3.131}$$

Secondly, the BB transient power reference ($P_{BB\_tr\_ref}$) is obtained from the difference between the ESS transient power reference ($P_{ESS\_tr\_ref}$) and the SM power reference ($P_{SM\_tr\_ref}$). This is given exactly as in Equation (3.77) and the BB power reference (P_{BB_ref}) is obtained as the sum of the BB transient power reference ($P_{BB\_tr\_ref}$) and the BB power reference from the peak shaving as in Equation (3.78). Also, the corresponding limits for P_{BB_ref} are also the ones defined in Equation (3.79). The SM power reference

(P_{SM_ref}) is calculated from the sum of the SM transient power reference ($P_{SM\_tr\_ref}$) and the SM power reference from the peak shaving ($P_{SM\_ps\_ref}$) as in Equation (3.80). As in the previous cases, a limiter is used to ensure that the SM power limits are not exceeded as in Equation (3.81).

In order to explain the power sharing among all the agents involved in the system, Figure 3-22 and Figure 3-23 show the evolution of the main power flows references involved.



(a) $P_{G\_max} \geq P_O$ (b) $P_{G\_max} < P_O$

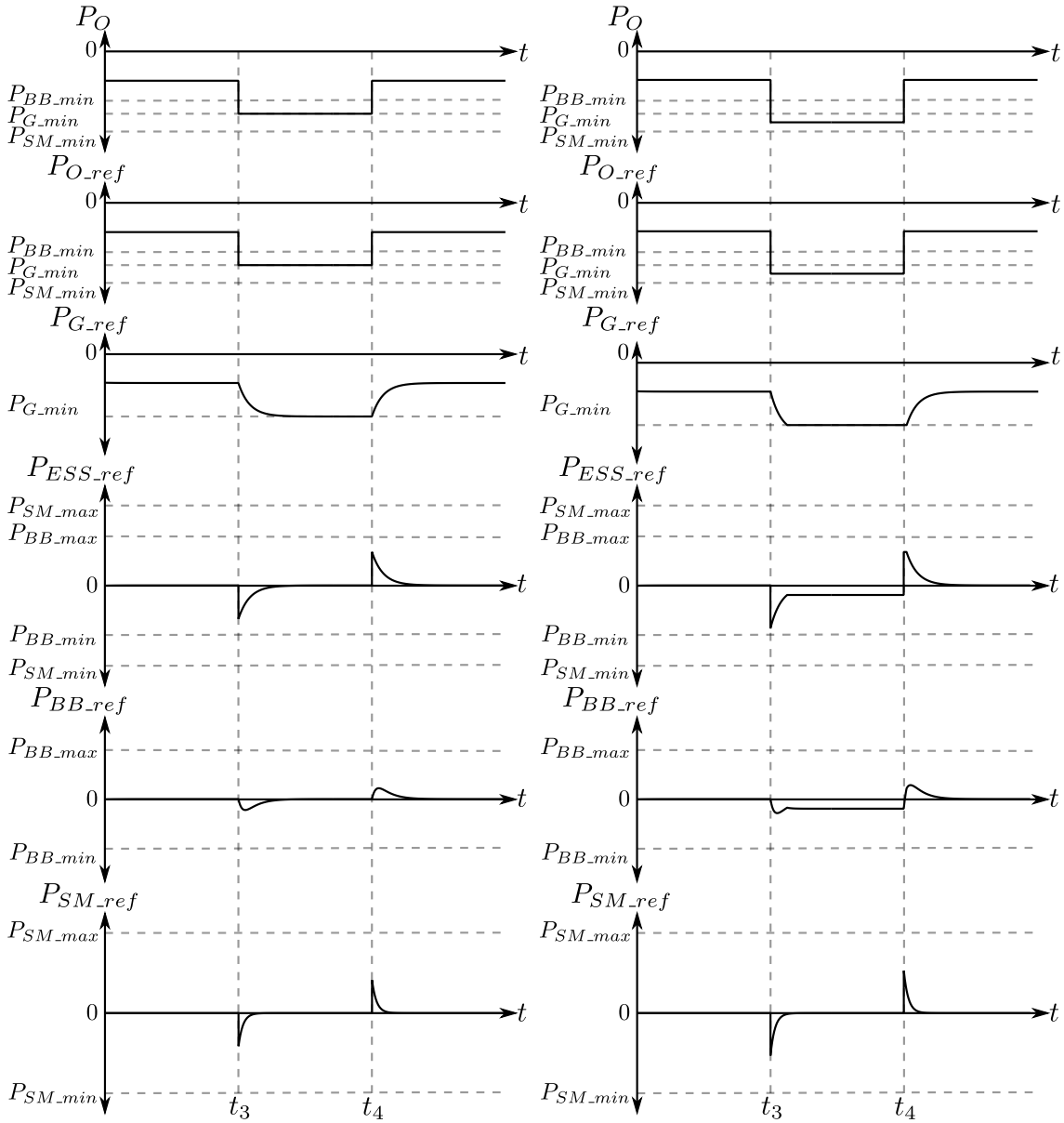
Figure 3-22: The power references generation upon positive steps during the grid-connected mode (Full Control).

Once more, the two-step profile in the demanded power (P_O) is assumed, considering an initial positive value for the demanded power. Upon this condition, Figure 3-22 shows an initial positive step in the demanded power (P_O) at t_1. After a given time (t_2), the demanded power decreases back to the original level. Considering the power references from the peak shaving are equal to zeros ($P_{G\_ps\_ref} = P_{BB\_ps\_ref} = P_{SM\_ps\_ref} = 0$). As it can be seen, the load power reference (P_{O_ref}) is equal to the power demanded by the microgrid (P_O).

If the maximum power reference delivered is less or equal to the maximum limit for the grid power (P_{G_max}) (i.e., HESS not used for peak-shaving), then the grid will deliver or absorb all the required power, and the ESS will only deliver the transient power, eventually reaching zero. This ESS transient power is shared between the BB and the SM, as in the previous cases; the SM provides/absorbs the transient peak power, while the BB provides/absorbs the remaining ESS power. This situation is depicted in Figure 3-22a. However, now, the peak-shaving scheme can easily be included in the casuistic of the control system, without the need for additional requirements. In this case, if the demanded power is greater than the limit for the maximum grid power, the BB will deliver or absorb both the transient power, but also the remaining steady-state power that the grid is not able to provide anymore. The SM, on its side, will provide only the transient peak power (as in the former case). This situation is shown in Figure 3-22b.

Figure 3-23 shows both situations but for initial negative value for the demanded power. In fact, the sequence of power steps is also interchanged, i.e., the power decreases at t_3 and then it increases again to the original value at t_4, to account for the worst possible situation. A completely similar discussion can then be carried out, but changing the signs of the power references involved. The power demanded reference (P_{O_ref}) is equal to the power demanded (P_O). Provided now that (P_O) is greater or equal to the minimum grid power (P_{G_min}), the grid will absorb/deliver the power necessary. The SM will absorb/deliver the transient peak power, while the BB will absorb the rest of the transient power. This situation is depicted in Figure 3-23a. Alternatively, Figure 3-23b shows the case in which the power demanded (P_O) is smaller than the minimum BB power (P_{G_min}). In this case, the grid will absorb/deliver some of the power needed. However, SM will absorb/deliver

the transient peak power, and the BB will absorb/deliver the rest of the power that grid cannot absorb and the rest of the transient power as in Figure 3-23b.



(a) $P_{G\_min} \leq P_O$ (b) $P_{G\_min} > P_O$

Figure 3-23: The power references generation upon negative steps during the grid-connected mode (Full Control).

After the calculation of the power references, the current references are calculated by dividing the power references by their corresponding voltage as in Equations (3.43), (3.44), (3.93) and (3.94). PLL is needed in order to synchronize with the grid voltage [134]. The

limits of the current references are defined as in Equations (3.45), (3.46), (3.95) and (3.96). Then, four current control loops are required: two current control loops for the d and q axes to control the grid current in the filters and another two current control loops for the BB and SM converters. The limits of the control actions are defined as in Equations (3.59), (3.60), (3.109) and (3.110). The bandwidth of the current control of the SM is faster than the bandwidth of the current control of the BB and the current control in d and q axes. Finally, the duty cycles are calculated as in Equations (3.61), (3.62), (3.111) and (3.112). The limits for the duty cycles are defined as in Equations (3.63), (3.64), (3.113) and (3.114). In Chapter 6, all these conditions, for every operation mode and every control strategy discussed here, will be applied to obtain a detailed design of all the parameters required to provide a full scheme of a HESS in a DC microgrid.

3.5 Conclusions

In this Chapter, the PC of two bidirectional buck converters is targeted as the base case for the research in this work. Then, the control schemes for this topology during islanding mode and grid-connected mode have been defined, studied, analyzed and discussed in detail. The general theoretical performance of these control schemes has been outlined. Next steps in the design consist of studying the limitations of these topologies in HESS applications. These limitations are studied in Chapters 4 and 5, and these chapters also propose topologies and control solutions to overcome these limitations. After providing a detailed design of every solution in Chapter 6, the performance of all these control schemes is validated, through simulations and experimental results in Chapters 7 and 8.

Next Chapter 4 studies the operating limits in the baseline solution when there is a large mismatch in the voltage ratings of the storage systems, and proposes a topology, named SPC of two bidirectional buck converters, as a feasible alternative to solve these operating limitations.

Chapter 4

Contributions for the Solution of the Voltage Mismatch Problem in Hybrid Energy Storage Systems

Contents

4.1 Introduction

This chapter discusses in detail the operation limits of the PC scheme in HESS, mainly coming from high voltage rating mismatch between the storage devices. Once these constraints are studied, different alternative solutions are explored. Finally, a novel connection structure is proposed, aiming to overcome the problems that arise in the original PC of two bidirectional buck converters. This gives pace to the introduction of the SPC of two bidirectional buck converters. This scheme is defined and analyzed in detail, and finally, the control schemes already discussed for the PC during the islanding and grid-tied modes are adapted for the new configuration.

4.2 Limitations of the Parallel Connection

As discussed in the previous section, the most straightforward scheme for a three-port bidirectional converter interface in a HESS able to attach these devices to a controlled DC bus is the PC of two bidirectional buck converters. The following is a discussion of how the main limitations of the multiple converter configuration, i.e., the active parallel configuration, come from the ratio between the storage devices voltage ratings and the DC bus voltage [80, 135].

For the sake of clarity, a nominal DC bus voltage (V_{DC}) of 500 V is going to be considered in the next discussion. In the same manner, the operating voltage ratings for the BB (V_{BB}) is considered to be in the range of 200–300 V (e.g., a Li-Ion BB intended for grid applications). For a BB operating voltage of 250 V, with these constraints, then the duty cycle of the S_1 (d_1) according to Equation (4.1) will be around 50%, thus optimizing the performance of such converter, regarding stresses balancing, design complexity and control

capability.

$$d_1 = \frac{V_{BB}}{V_{DC}} = \frac{250}{500} = 50\% \tag{4.1}$$

However, in some applications, the extra storage unit presents significant lower voltage ratings than the ones in the BB, and thus the voltage ratios between the DC bus voltage and the additional storage unit voltage will change correspondingly. For instance, some SM voltage ratings (V_{SM}) are ranged from 20V to 80V. This implies that at some operating conditions, e.g., the SM discharged to a voltage of 30 V, and for the stated DC bus voltage ratings, the required gains for the dedicated interfacing converter will reach values up to 17 or even higher (Equation (4.2)).

For the conditions mentioned above for the DC bus voltage of 500 V and the SM operating voltage of 30 V, the performance in the steady state can be assessed, yielding to the following duty cycle for the S_3 (d_3):

$$d_3 = \frac{V_{SM}}{V_{DC}} = \frac{30}{500} = 6\% \tag{4.2}$$

This mismatch in the operating voltage ratings would yield to the operation of the converters at the PC topology at duty cycle around 6%, well beyond the optimal 20–80% range [136]. As a large gain is required, the efficiency and the cost-effectiveness of the buck converter-based design are compromised [137, 138].

For the discussed conditions, S_3 is turned on 6 % of the switching time, while the S_4 is turned on 94 % of the switching time. These extreme duty ratio values yield low efficiency in the buck-based configuration [139]. Besides, the parasitic series resistor of the inductor together with the non-ideal components at the switches implies a limit in the achievable voltage gain of the buck converter [140]. Such a high voltage ratio can be attained only by using optimal, high-performance magnetic devices. For this discussion, it is assumed that the inductors present a relatively small parasitic resistance.

As the switches must be designed for the high DC bus voltage, high voltage ratings must be used. However, these devices present relatively large on-resistance values, and therefore conduction losses increase [141]. Moreover, in IGBT based topologies, this im-

plies large currents at the anti-parallel diodes, yielding to operation drawbacks derived from the reverse recovery phenomenon [142]. Moreover, the high duty cycles limit the switching frequency, as the minimum off-time of the switch must be ensured [143].

In addition, the dynamic performance of the converter is also affected, since the small duty cycles yield to non-symmetric bandwidths limitation in charge and discharge operation [137]. The instant value of the duty cycles in the converters states the capability of providing a given transient voltage to the inductors in the converters, therefore yielding to a given current by those inductors. On top of an unbalance of the stresses in the switches and poor performance due to extreme duty cycles, the main problem in PC comes from the fact that the starting value of the duty cycle in the SM leg is quite small (6%).

Considering an abrupt negative step in the SM current demand, then the control stage must generate a control action in the duty cycles that provide the actual SM current, equal to the reference value. However, the available control actions range from the 6% value down to 0%, which ultimately implies S_3 and S_4 continuously turned off and on, respectively. This condition implies that the SM inductance (L_2) is discharged with the relatively small voltage at the SM (V_{sm}) thus implying a limitation in the rate of decrease of the SM current. This aspect penalizes the discharging dynamics enormously, also introducing a non-symmetric behavior in the system performance. Indeed, for the opposite case (charging current), the extreme operation in the control action would imply a charging voltage of V_{DC}, and the rate of charge results dramatically increased.

Finally, the small duty cycle of the S_3 leg (d_3) yields to thermal and electrical stresses mismatch on the switches at this leg. The reliability of the design is a function of the relative value and distribution scheme of the thermal efforts associated with the electrical parameters [144]. The following discusses the effect of the shape of the waveforms in the distribution of the electrical stresses of a leg at the converter. The concept of Form Factor (FF) will be used, understood as the ratio if the Root Mean Square (RMS) value of a waveform to its average value. Assuming small current ripples, then the FF of the current waveform for a given switch in the converter follows the general expression for a square

waveform:

$$K_f = \frac{I_{rms}}{I_{avg}} \tag{4.3}$$

$$I_{rms} = I_{pk}\sqrt{\frac{T_{on}}{T_s}} \tag{4.4}$$

$$I_{avg} = I_{pk}(\frac{T_{on}}{T_s}) \tag{4.5}$$

$$K_f = \frac{I_{pk}\sqrt{\frac{T_{on}}{T_s}}}{I_{pk}\frac{T_{on}}{T_s}} = \frac{1}{\sqrt{\frac{T_{on}}{T_s}}} \tag{4.6}$$

where:

- K_f is the FF of the current in the switch,
- I_{rms}, I_{avg} and I_{pk} are the RMS, average and peak currents of a periodic square waveform of switching period, respectively, in Amps,
- T_{on} is the interval of the waveform that the current value equals peak value in Secs.

Figure 4-1 shows a scheme of the switch current waveform approximations in case of low ripple, with the graphical definition of the parameters used for the definition of the FF.

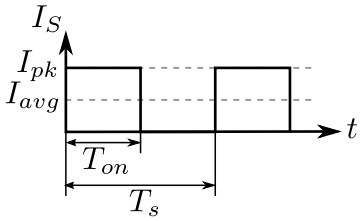


Figure 4-1: Current waveform of a switch considering small ripple.

In the PC topology, for a large mismatch between the ratings at the SM and at the DC bus, the duty cycle at the upper switch of the SM leg (d_3) is close to 0%, around 6% in the case under study. From Equation 3.6, the duty cycle at the (d_3) can be expressed as:

$$d_3 = \frac{T_{on\_S3}}{T_s} \tag{4.7}$$

and therefore the FF of the current for the S_3 (K_{f_3}) is obtained as follows:

$$K_{f_3} = \frac{1}{\sqrt{\frac{T_{on\_S3}}{T_s}}} = \frac{1}{\sqrt{d_3}} \tag{4.8}$$

Analogously, the FF of the current for the S_4 (K_{f_4}) is calculated as follows:

$$K_{f_4} = \frac{1}{\sqrt{\frac{T_{on\_S4}}{T_s}}} = \frac{1}{\sqrt{1-d_3}} \tag{4.9}$$

Therefore, for a duty ratio close to 6%:

$$K_{f_3} = \frac{1}{\sqrt{0.06}} = 4.08 \tag{4.10}$$

$$K_{f_4} = \frac{1}{\sqrt{1-0.06}} = 1.03 \tag{4.11}$$

This difference between the FFs at the switches of the leg of the SM converter implies that the thermal efforts at both switches are very different. Ideally, to evenly distribute these thermal efforts among the upper and lower switches of a leg, the duty cycles should be around 50%, yielding to FF values close to:

$$K_f = \frac{1}{\sqrt{1-0.5}} = 1.41 \tag{4.12}$$

Such requirements cannot be accomplished by the parallel buck arrangement, nor for the rest of the commonly used single-stage non-isolated converter topologies [80, 136]. More complex alternatives can be used to solve the problem of voltage mismatch, including cascaded stages, multilevel or even isolated approaches. Some of these options are the parallel configuration of two DAB [36, 58, 81, 95], the use of triple active bridge [97, 98], as well as systems based in resonant converters [145] or multilevel converters [92]. However, it could yield to higher costs and system complexity due to the increase in the number of switches and passive elements [136].

4.3 The Full-Bridge Connection

In order to solve these issues, the most straightforward solution among non-isolated topologies is to use a Full Bridge Connection (FBC) [146], as depicted in Figure 4-2. The negative terminal of the SM is connected to the middle point of a third leg, formed by S_5 and S_6. It is assumed that the duty cycles of S_4 and S_6, are complementary to the ones at S_3 and S_5, respectively, as in the following scheme:

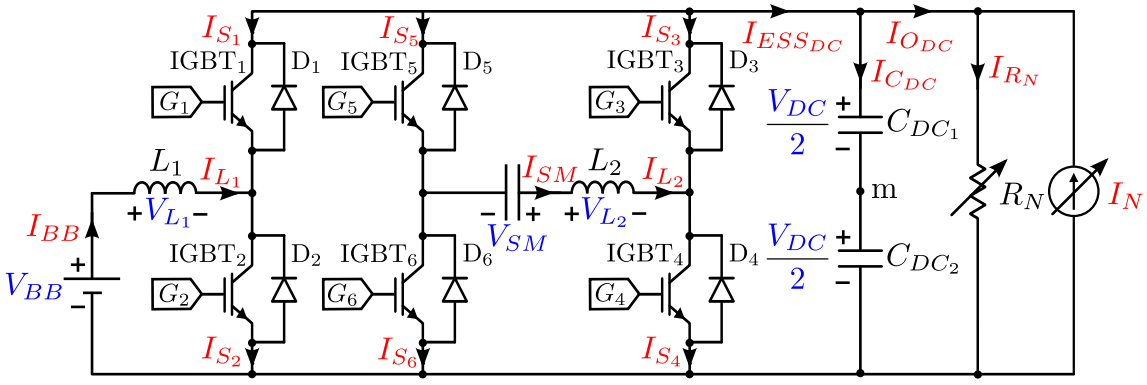


Figure 4-2: The FBC of the two bidirectional buck converters connected to BB and SM and sharing the DC bus.

$$d_4 = 1 - d_3 \tag{4.13}$$

$$d_6 = 1 - d_5 \tag{4.14}$$

Considering the transient state an by applying KVL in Figure4-2, it yields to:

$$V_{CE_6} + V_{SM} - V_{L_2} - V_{CE_4} = 0 \tag{4.15}$$

$$d_5 \cdot V_{DC} + V_{SM} - V_{L_2} - d_3 \cdot V_{DC} = 0 \tag{4.16}$$

$$d_3 = \frac{d_5 \cdot V_{DC} + V_{SM} - V_{L_2}}{V_{DC}} \tag{4.17}$$

$$d_3 = d_5 + \frac{V_{SM} - V_{L_2}}{V_{DC}} \tag{4.18}$$

At steady state, the duty cycle of the S_3 is given by:

$$d_3 = d_5 + \frac{V_{SM}}{V_{DC}} \tag{4.19}$$

In fact, this effect comes as there is a new degree of freedom, that can be selected to have one of the duty cycles, e.g. d_5, fixed at a given value, for instance, equal to 50%. This ensures effective duty cycles at each leg out away from the extreme values, i.e., within the 20% - 80% areas, therefore achieving better general performance [137, 138, 141].

In addition, the dynamic range is greater, given that the asymmetric modulation constraint of the PC solution is not present anymore. The payback, in this case, is the use of two additional switches in a second leg. This issue increases the size and weight of the converter, as well as the switching and conduction losses. However, with this solution, the dynamics are not limited to the low duty cycles in the converter [137]. Still, all the four switches need to cope with the large V_{DC} voltages at the DC bus, even though the device to interface presents significantly small ratings, yielding again to large conduction and switching losses [141].

4.4 The Series Connection

To overcome the drawbacks of the PC and the FBC, a solution that prevents from moving to more complex schemes is the Series Connection (SC) of the storage systems depicted in Figure 4-3 [70, 137]. This solution aims to avoid the low duty cycles at the SM branch. The negative terminal of the SM is connected to the positive terminal of the BB.

By applying KVL to the voltage mesh that includes the BB, the SM, inductor L_2 and S_4 in Figure4-3, then:

$$V_{BB} + V_{SM} - V_{L_2} - V_{CE_4} = 0 \tag{4.20}$$

$$V_{BB} + V_{SM} - V_{L_2} - d_3 \cdot V_{DC} = 0 \tag{4.21}$$

$$d_3 = \frac{V_{BB} + V_{SM} - V_{L_2}}{V_{DC}} \tag{4.22}$$

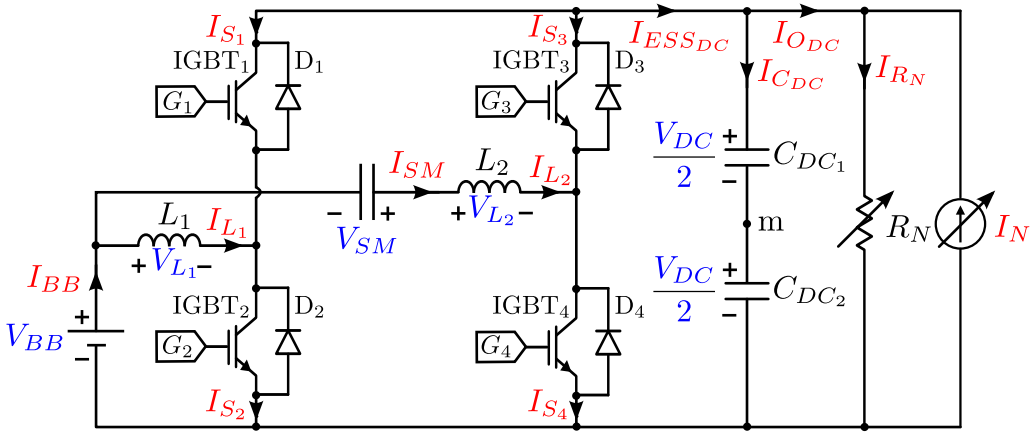


Figure 4-3: The SC of the two bidirectional buck converters connected to BB and SM and sharing the DC bus.

Upon steady-state condition, the average voltages at the inductors are null, and therefore the value of the duty cycle at the S_3 (d_3) is given by:

$$d_3 = \frac{V_{BB} + V_{SM}}{V_{DC}} \tag{4.23}$$

$$d_3 = d_1 + \frac{V_{SM}}{V_{DC}} = 56\% \tag{4.24}$$

The value of the duty cycle at the BB leg is given by Equation (4.1). The duty cycle of the S_3 (d_3) is always bigger than the duty cycle of the S_1 (d_1). With the same voltage values than in the PC case, S_3 is turned on 56%, and S_4 is turned on 44 % of the switching time in the SC scheme. This yields to a balance in the thermal stress on the switches for the SM leg. In the aforementioned connection, the duty cycle of the S_3 is a function of the SM voltage and BB voltage, not only of the SM voltage as in case of PC. Therefore, the stresses in the switches of the SM leg are much more balanced than in the previous case, thus avoiding the decrease in the reliability aspects mentioned before.

The gain required for the SM leg of the converter results in a much more reasonable value than before. Indeed, the drawback of the voltage mismatch at the PC is solved as the average voltage at the midpoint of the SM leg results in the addition of the SM plus the BB voltages. Assuming that the SM ratings are much smaller than the BB ones, this leg operates with a duty cycle similar to the BB leg. However, the main drawbacks of this connection are that at the end the BB needs to provide also the SM peak current, decreasing

the lifespan of the BB. This is deduced from applying the KCL at the node that connects the BB, the SM and inductor L_1:

$$I_{BB} = I_{L_1} + I_{SM} \tag{4.25}$$

$$I_{SM} = I_{L_2} \tag{4.26}$$

This results in the impossibility of implementing a practical decoupled current control scheme in both the storage systems (BB and SM). In fact, if both inductor currents are independently controlled, then the evolution of the battery inductor current is forced by Equation (4.25), yielding either to dangerous voltages in the system due to the inductive behavior, or to a limited dynamic performance if these overvoltages are prevented at the control level.

Another point of the analysis comes by looking at Figure 4-3. From the inductors connection scheme, it might seem that a certain beneficial interleaving effect is possible in the BB current (I_{BB}). Nevertheless, this effect would only be valid for small operating conditions ranges, as it depends on the values of the duty cycles and in the synchronization of the pulses in the switches. This enhanced interleaving effect will not occur for all possible conditions, particularly for SM currents much higher than BB currents.

Finally, also derived from Equation (4.25), the peak current flowing through the BB inductor is calculated as a function of the SM and BB currents. Thus, inductor L_1 must be designed considering values in the order of magnitude of the SM current, that is significantly larger than the BB current. This results in a much larger inductor device, which compromises the efficiency and the cost of the full HESS.

Given all these constraints, the SC scheme is disregarded as a feasible option. Therefore it will not be included in the validation stages, by simulation or experimental tests.

4.5 The Series-Parallel Connection

All these drawbacks of the previous schemes can be effectively solved by considering the SPC of both storage units [125, 147, 148]. This scheme, shown in Figure 4-4, keeps

the original H-bridge configuration of the switches. As shown in Figure 4-4, the negative terminal of the SM is connected to the middle point of the leg connected to the BB. This configuration can be seen as an integration of the FBC from three to two legs, removing the degree of freedom that existed in the latter.

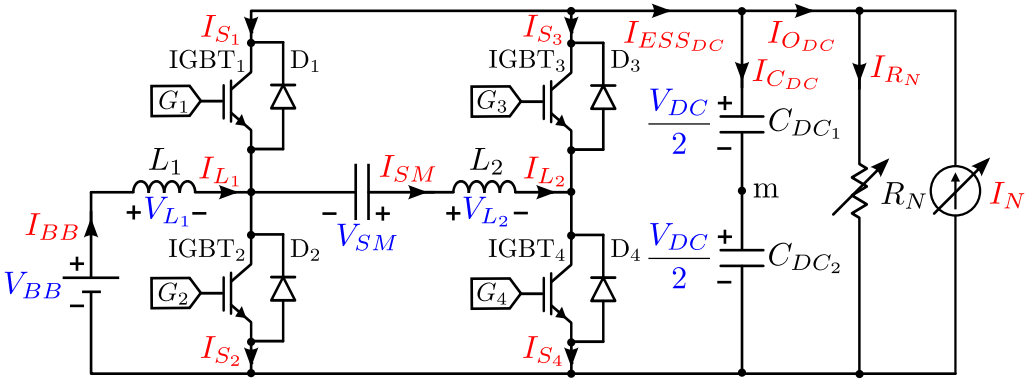


Figure 4-4: The SPC of the two bidirectional buck converters connected to BB and SM and sharing the DC bus.

For the references at Figure 4-4, the mesh equation that includes the voltage at the SM can be expressed as:

$$V_{CE_2} + V_{SM} - V_{L_2} - V_{CE_4} = 0 \tag{4.27}$$

$$V_{BB} - V_{L_1} + V_{SM} - V_{L_2} - d_3 \cdot V_{DC} = 0 \tag{4.28}$$

$$d_3 = \frac{V_{BB} - V_{L_1} + V_{SM} - V_{L_2}}{V_{DC}} \tag{4.29}$$

$$d_3 = d_1 + \frac{V_{SM} - V_{L_2}}{V_{DC}} \tag{4.30}$$

Again, upon steady-state conditions, the average inductor voltages are null, and therefore the value of the duty cycle at the S_3 (d_3) is given by:

$$d_3 = \frac{V_{BB} + V_{SM}}{V_{DC}} = d_1 + \frac{V_{SM}}{V_{DC}} \tag{4.31}$$

In SPC, the duty cycle of the S_3 (d_3) is a function also of the voltage at the inductor connected to the battery. This ultimately yields to an extension on the values that the SM

inductor might take, and therefore extending the range of symmetrical behavior. Again, it presents a similar expression than in the SC case; thus all the statements concluded for the new duty cycle values are still valid.

In order to quantify the stresses distribution, the values of the FF can be calculated for the switches at the SM branch at the SPC configuration:

$$K_{f_3} = \frac{1}{\sqrt{0.56}} = 1.34 \tag{4.32}$$

$$K_{f_4} = \frac{1}{\sqrt{1-0.56}} = 1.51 \tag{4.33}$$

These values are close to the optimal value for an even distribution of the current efforts stated in Equation (4.12), therefore increasing the reliability of the system. This effect is obtained for any application in which one of the legs at the converter interfaces a device with voltage ratings significantly smaller than the other one, this latter being around half (e.g., practical values of 40–60%) the DC bus value.

In addition to that, it must be noticed how, in the SPC scheme, the following expression can be calculated for the BB current:

$$I_{BB} = I_{L_1} \tag{4.34}$$

Therefore, and unlike in the SC case, decoupling both BB and SM current control is quite simple in the SPC scheme. This results in the possibility of implementing an independent current control (and hence power flow) for both storage devices. This allows for an effective hybridization of the energy devices, without the drawbacks of extreme duty rations in the system. The following discussion deals with an in-depth analysis of the operation of the SPC converter, aiming to provide the foundations for an adequate design of the HESS.

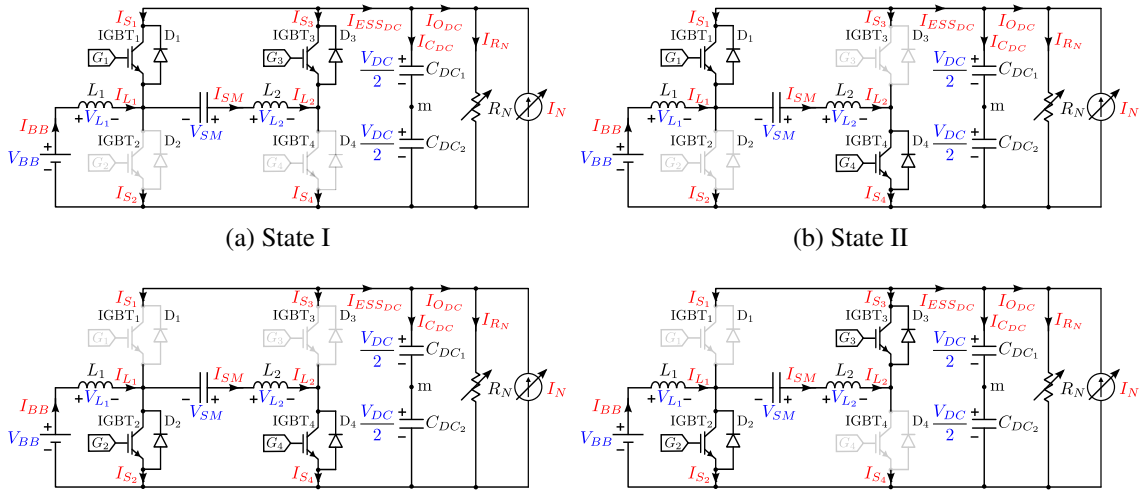
4.5.1 Switching States

Similar to the PC of the two bidirectional buck converters, the SPC also has four switching states as in Table 4.1 and Figure 4-5. The S_1 and the S_3 are commutating with the value

of the duty cycle for the BB and SM converters, respectively, while the S_2 and the S_4 are complementary.

Table 4.1: The switching states of the SPC of the two bidirectional buck converters.

States	BB Converter		SM Converter		Figures
	On	Off	On	Off	
State I	S_1	S_2	S_3	S_4	4-5a
State II	S_1	S_2	S_4	S_3	4-5b
State III	S_2	S_1	S_4	S_3	4-5c
State IV	S_2	S_1	S_3	S_4	4-5d



(a) State I (b) State II

(c) State III (d) State IV

Figure 4-5: The switching states of the SPC of the two bidirectional buck converters.

The equivalent switching states depicted in Figure 4-5 are described in detail in the following subsections.

4.5.1.1 State I. S_1 and S_3 Turned On

Figure 4-5a shows both S_1 and S_3 turned on. The resulting current expressions in the switches for this interval are:

$$\begin{aligned} I_{S_1}(State\ I) &= -I_{BB} + I_{SM}; & I_{S_3}(State\ I) &= -I_{SM}; \\ I_{S_2}(State\ I) &= 0; & I_{S_4}(State\ I) &= 0; \end{aligned} \tag{4.35}$$

where I_{S_1}, I_{S_2}, I_{S_3} and I_{S_4} are the currents of S_1, S_2, S_3 and S_4, respectively, in Amps.

4.5.1.2 State II. S_1 and S_4 Turned On

In the next switching interval, depicted in Figure 4-5b, S_3 turns off, and S_4 turns on, whereas the BB leg remains unchanged as in state I. The resulting current expressions in the switches are as follows:

$$\begin{aligned} I_{S_1}(State\ II) &= -I_{BB} + I_{SM}; & I_{S_3}(State\ II) &= 0; \\ I_{S_2}(State\ II) &= 0; & I_{S_4}(State\ II) &= I_{SM}; \end{aligned} \tag{4.36}$$

4.5.1.3 State III. S_2 and S_4 Turned On

State III keeps the SM leg as in state II, but now S_2 is turned on as S_1 turns off (Figure 6c). The inductor connected to the BB charges through S_2 ($I_{BB} > 0$). Assuming also $I_{SM} > 0$, then L_2 charges through S_2 and S_4:

$$\begin{aligned} I_{S_1}(State\ III) &= 0; & I_{S_3}(State\ III) &= 0; \\ I_{S_2}(State\ III) &= I_{BB} - I_{SM}; & I_{S_4}(State\ III) &= I_{SM}; \end{aligned} \tag{4.37}$$

4.5.1.4 State IV. S_2 and S_3 Turned On

Finally, S_4 turns off, and S_3 turns on, while the BB leg is kept the same as in state III. The SM current flows towards the DC bus through S_3, and therefore:

$$\begin{aligned} I_{S_1}(State\ IV) &= 0; & I_{S_3}(State\ IV) &= -I_{SM}; \\ I_{S_2}(State\ IV) &= I_{BB} - I_{SM}; & I_{S_4}(State\ IV) &= 0; \end{aligned} \tag{4.38}$$

Depending on its direction, the current may flow in the switch either through the IGBT or the anti-parallel diode in the SM leg, as stated in Table 4.2. However, for the case of the BB leg, the final device that carries the current in the switch is given by the sign of the combination of the BB current and the SM, as shown in Table 4.3.

Table 4.2: The switching states of the SPC of the two bidirectional buck converters.

States	BB Converter (On Switches)		SM Converter (On Switches)	
	BB Discharging	BB Charging	SM Discharging	SM Charging
State I	D_1 / $IGBT_1$	$IGBT_1$ / D_1	D_3	$IGBT_3$
State II	D_1 / $IGBT_1$	$IGBT_1$ / D_1	$IGBT_4$	D_4
State III	$IGBT_2$ / D_2	D_2 / $IGBT_2$	$IGBT_4$	D_4
State IV	$IGBT_2$ / D_2	D_2 / $IGBT_2$	D_3	$IGBT_3$

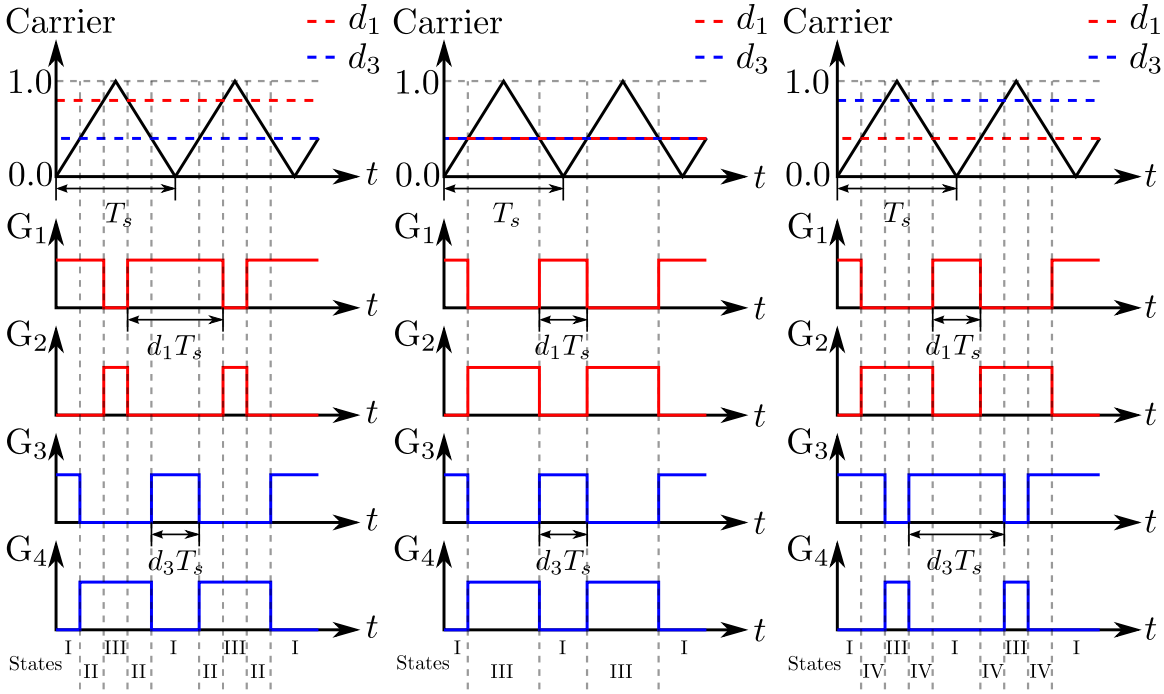
Table 4.3: The switching states of the SPC of the two bidirectional buck converters for the On switches.

States	BB Converter (On Switches)			
	BB Discharging		BB Charging	
	$I_{BB} > I_{SM}$	$I_{BB} < I_{SM}$	$I_{BB} < I_{SM}$	$I_{BB} > I_{SM}$
State I	D_1	$IGBT_1$	$IGBT_1$	D_1
State II	D_1	$IGBT_1$	$IGBT_1$	D_1
State III	$IGBT_2$	D_2	D_2	$IGBT_2$
State IV	$IGBT_2$	D_2	D_2	$IGBT_2$

Similar to PC, there also are three possibilities for the duty cycles of both ESS: ($d_1 > d_3$) or ($d_1 = d_3$) or ($d_1 < d_3$). Depending on the duty cycles, the switching states will change as in Figure 4-6.

4.5.2 Steady-State Analysis

Once the switching states are defined, the steady-state analysis of the SPC scheme can be carried out. It must be noticed that both converters are bidirectional in the current, and



(a) $d_1 > d_3$ (b) $d_1 = d_3$ (c) $d_1 < d_3$

Figure 4-6: The switching states of the SPC of the two bidirectional buck converters depending on the values of the duty cycles.

thus, if a general analysis is desired, all possible combinations must be assessed. Considering a system that operates with DC bus voltage control, and provided that both storage device legs be controlled in current mode, the operating conditions that need to be taken into account are stated in Table 4.4.

Table 4.4: Operating conditions of storage systems, considering reference notations in Figure 4-4

BB	SM	Operating Conditions
Discharging I_{BB}>0	Charging I_{SM}<0	Opposite sign in currents
Discharging I_{BB}>0	Discharging I_{SM}>0	Same sign in currents
Charging I_{BB}<0	Charging I_{SM}<0	Opposite sign in currents
Charging I_{BB}<0	Discharging I_{SM}>0	Same sign in currents

From Equations (4.35)-(4.38), it can be concluded that the current flowing through the switches at the BB leg is a subtraction of the BB and SM inductor currents. Therefore,

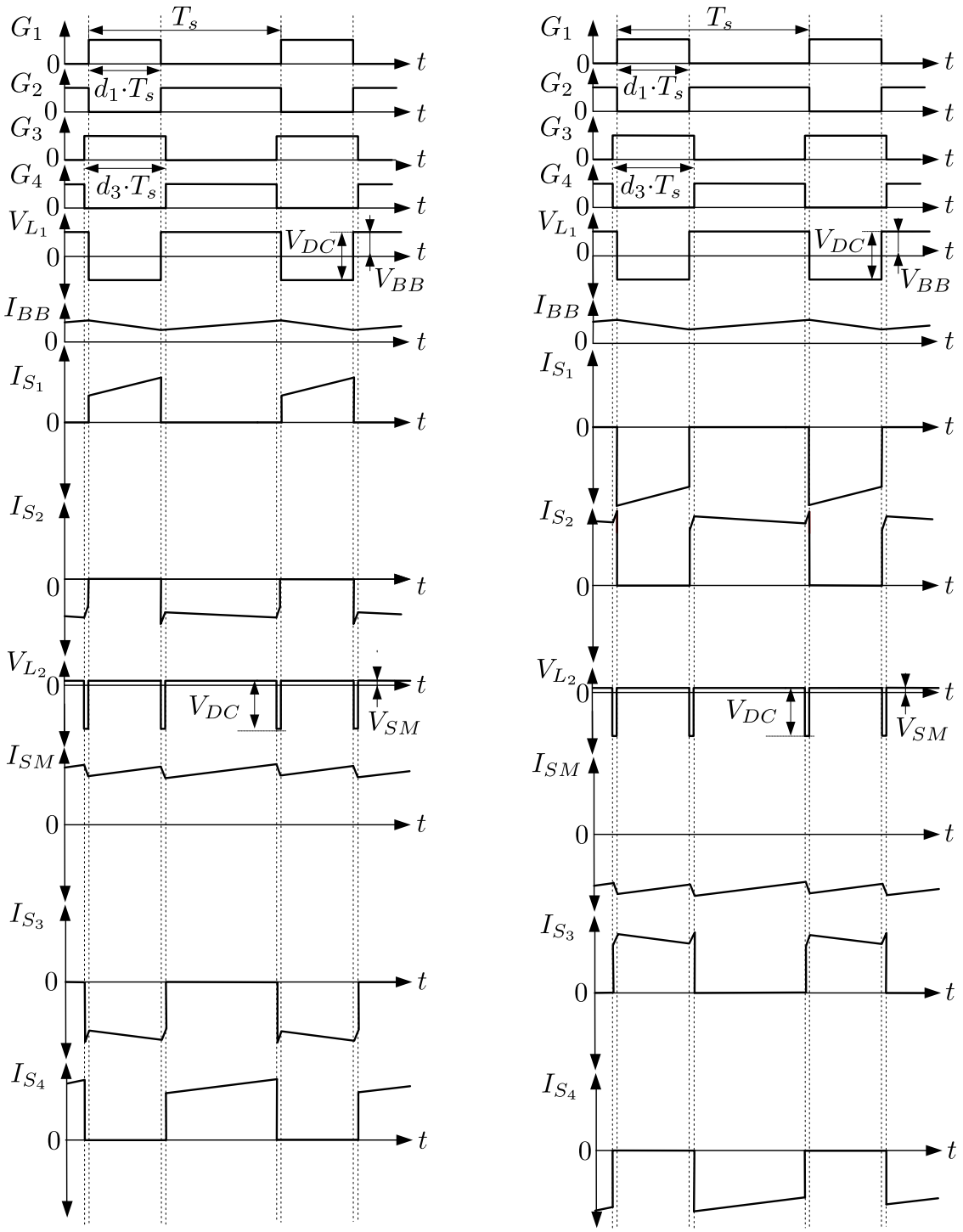
the net result of these switch currents depends on whether these currents are added or subtracted in absolute value. Thus, this study can be simplified to the cases in which SM and BB currents have either the same or opposite signs. The theoretical waveforms for these two key cases can be seen in Figure 4-7a (BB and SM discharging, I_{BB} and I_{SM} have same signs) and Figure 4-7b (BB discharging, SM charging, I_{BB} and I_{SM} present opposite signs). Even if the resulting current values at the switches result in significant change, the claimed balancing effect in the current stresses at the SM leg switches can still be noticed, as all the involved duty ratios are relatively close to the 50% optimal value.

Another consequence of this switching pattern is that the current waveforms through the SM inductor present a ripple at twice the switching frequency. This allows for a certain degree of optimization in the inductor design, as current ripple will decrease for the same target inductor value, or, conversely, the inductor can be made smaller for the same target current ripple.

In any case, the most significant consequence of this connection comes from the relationship between the duty cycle at S_3 at both PC and SPC configurations. Considering the steady-state operation, then from Equation (4.31), d_3 is always greater than d_1 ($d_1 < d_3$) as in Figure 4-6c for SPC scheme. However, in transient operation (Equation (4.31)), the inductor voltage at the SM might be substantially large, depending on the transient current demanded. This might yield d_3 to reach values smaller than d_1 ($d_1 > d_3$) as in Figure 4-6a. However, as in the FBC case, now the control action at the SM is not clamped as in PC, and therefore a better dynamic performance is found. Moreover, this behavior is now symmetric. Given that the control action can reach negative values naturally, the modulation is never interrupted in the SPC operation. These issues will be validated experimentally in Chapter 8, devoted to the validation of the topologies.

4.5.3 Circulating Currents and Efficiency

From the above discussion, the SPC can be initially considered as an alternative solution for a non-isolated interface in a HESS, in the case that one of the storage devices is rated at very low voltage. As can be seen, the proposed scheme overcomes the main drawbacks of the PC, FBC and SC schemes. However, significant concerns in the performance of



(a) BB and SM both are discharging.

(b) BB is discharging, but SM is charging.

Figure 4-7: Theoretical waveforms of the SPC scheme.

the solution arise from the fact that the SM current will also flow through the switches of the BB leg. It means that both switching and conduction losses through these switches

will be affected. In the event that the final losses at these switches increase with respect to the original scheme, the overall efficiency loss might make infeasible the use of this solution. Thus, a thorough, objective analysis of the time evolution of losses in the system as a function of the state of operation must be carried out. As it will be demonstrated, the final balance depends on the operation point of the HESS.

The main issue to consider is that, at the switching states (I or II) and (III or IV) depicted in figure 4-5, respectively, when both the current through the BB and SM have the same sign (both charging or discharging, as per Table 4.4), then the current through the switches at the BB leg are effectively subtracted. Indeed, considering KCL at the node that connects inductor L_1, Switches S_1 and S_2, and the SM in Figure 4-5a or Figure 4-5b for the state I or the state II, respectively, then:

$$I_{S_1} = I_{L_2} - I_{L_1} = I_{SM} - I_{BB} \tag{4.39}$$

However, from Table 4.4, if both devices are charging or discharging, then this arithmetic subtraction is a subtraction of the moduli of the currents, and therefore the current I_{S_1} is smaller than any of the device currents. The same conclusion for the current of S_2 can be derived from state III or state IV, looking at the same node in Figure 4-5c or Figure 4-5d:

$$I_{S_2} = I_{L_1} - I_{L_2} = I_{BB} - I_{SM} \tag{4.40}$$

Thus, depending on the relative current values flowing through the storage devices, the final current stresses at the BB leg of the converter might result smaller than the ones in the PC connection. On the other hand, when the current through the storage devices present different signs, these current arithmetic subtractions at S_1 and S_2 will result in an addition of the moduli of the currents, thus increasing the current stresses.

To assess this comparison quantitatively, the losses at every switch of converter have been expressed following a simplified theoretical approach. The general equations of both the switching and conduction losses, for inductive switching of the converter, have been calculated, to compute the converter power losses, P_{Loss} as a function of the BB and SM

current values [137, 146]. However, to extract conclusions on the comparison of performances, the figure of merit that is considered is the difference between the losses at both the PC and SPC configurations, ΔP_{Loss}, rather than the losses at each of the schemes on their own. Figure 4-8 shows the power losses, P_{Loss_PC} in steady-state, for the operating characteristics discussed previously, as a function of different BB and SM. Analogously, Figure 4-9 shows the same P_{Loss_SPC} parameter for the SPC configuration. Finally, Figure 4-10 shows the difference in the power loss, as expressed by:

$$\Delta P_{Loss} = P_{Loss\_SPC} - P_{Loss\_PC} \tag{4.41}$$

where:

- ΔP_{Loss} is the difference in power loss between PC and SPC in Watts,
- P_{Loss_PC} and P_{Loss_SPC} are the power losses of the PC and the SPC, respectively, in Watts.

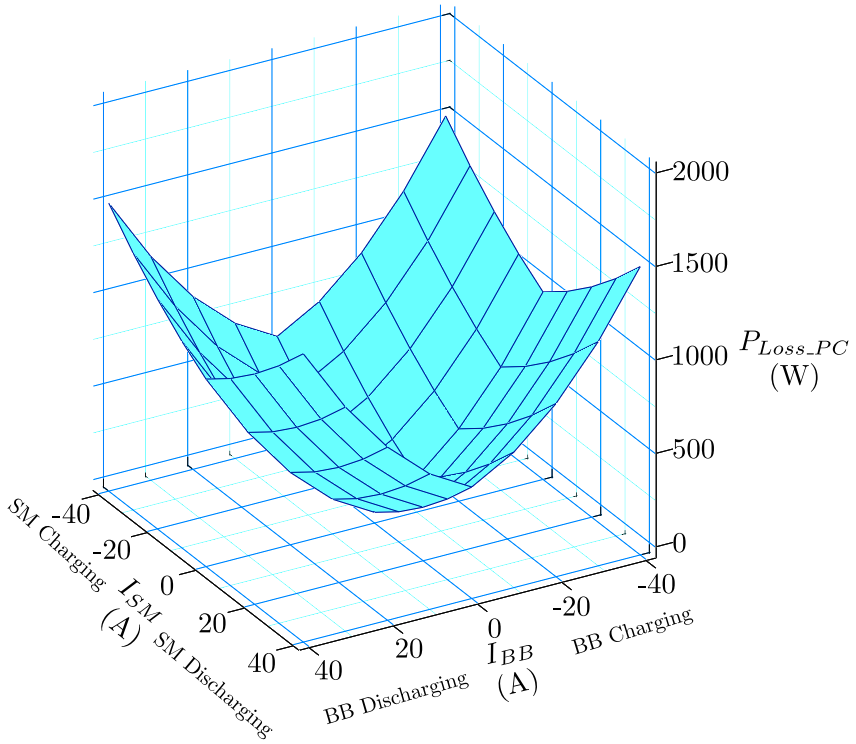


Figure 4-8: Power Losses of the PC in steady state.

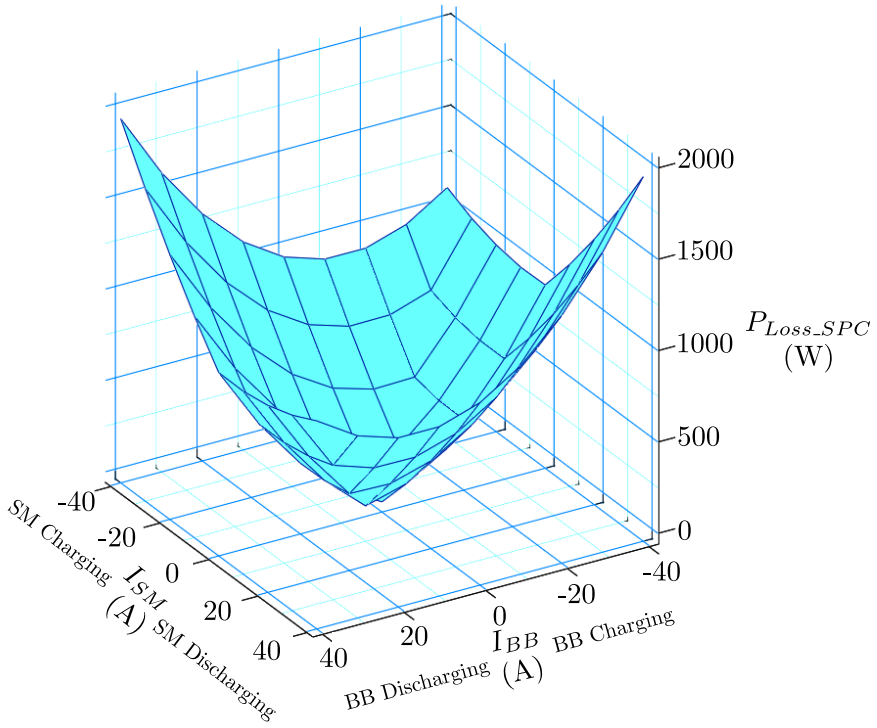


Figure 4-9: Power Losses of the SPC in steady state.

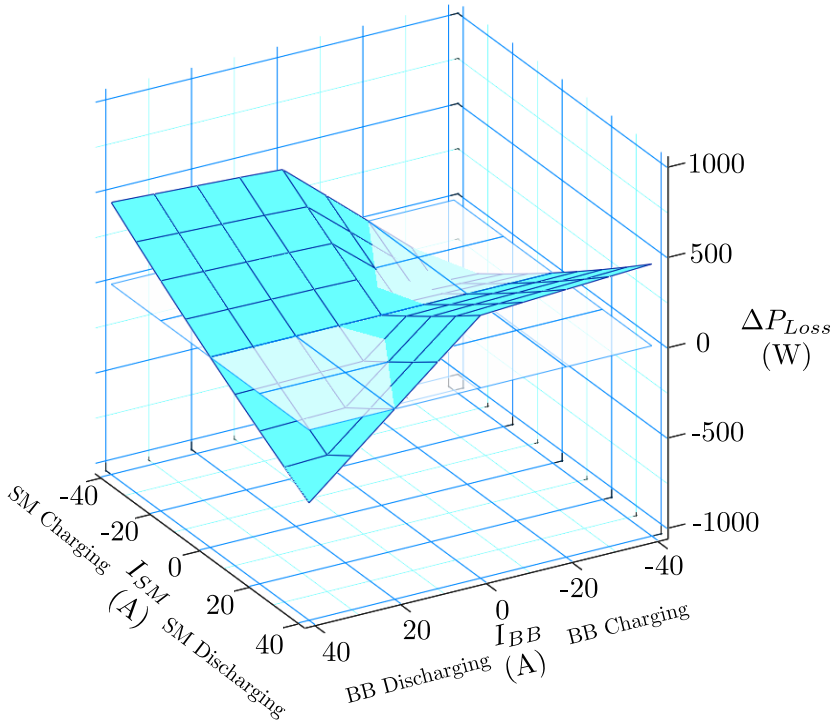


Figure 4-10: The difference in the power loss between PC and SPC.

From Figure 4-10, some conclusions can be derived. At those pairs of $(I_{BB} - I_{SM})$ coordinates for which the values of ΔP_{Loss} are negative, the losses at SPC configuration are smaller than the losses at PC scheme. This means that for these operating conditions, the circulating currents at the SPC configuration have an overall positive impact on the efficiency of the converter. However, for another set of coordinates, at which ΔP_{Loss} is positive, losses at the SPC configuration are higher. These theoretical conclusions, along with the applicability to HESS systems will be corroborated and validated by experimental results in Chapter 8 after a detailed design procedure is defined in Chapter 6.

4.5.4 Control Schemes

Finally, the implications on the control schemes discussed previously of the SPC topology will be analyzed. As mentioned in the previous chapter, there are three control schemes depending on the two modes of operation: islanding mode and grid-connected mode. The difference between the control schemes of the SPC and the control schemes of the PC is the limits of the control action (SM inductor voltage) of the SM current controller and the calculating of the duty cycle of the SM in each connection as depicted in Figure 4-11.

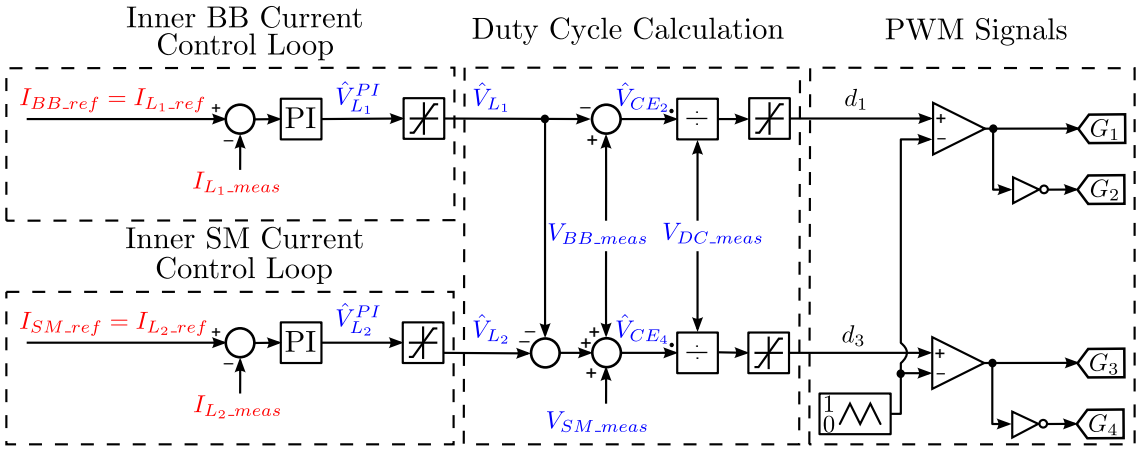


Figure 4-11: Inner current controllers scheme for the SPC of the two bidirectional buck converters.

The limits of the control actions of the inner BB current controller are the same as in the PC case (Equations (3.53) and (3.54)). However, the limits of control action of the inner SM are different from PC case [148]. In order to calculate the limits of the inductor voltage

connected to the SM, from Equation (4.28) yielding to:

$$V_{L_2} = V_{BB} - V_{L_1} + V_{SM} - d_3 \cdot V_{DC} = 0 \tag{4.42}$$

At a duty cycle of the leg connected to the BB equals to zero and a duty cycle of the leg connected to the SM equals to unity (i.e., $d_1 = 0$ and $d_3 = 1$) (State IV) yielding to:

$$V_{L_1} = V_{BB} \tag{4.43}$$

$$V_{L_2} = V_{BB} - V_{BB} + V_{SM} - V_{DC} \tag{4.44}$$

$$V_{L_2\_min} = V_{SM\_meas} - V_{DC\_ref} \tag{4.45}$$

As it can be noticed that the minimum inductor voltage limit is the same as in Equation (3.57); however, the maximum voltage of the inductor connected to the SM is calculated as follows. At a duty cycle of the leg connected to the BB equal to unity and duty cycle of the leg connected to the SM equals to zero (i.e., $d_1 = 1$ and $d_3 = 0$) (State II) yielding to:

$$V_{L_1} = V_{BB} - V_{DC} \tag{4.46}$$

$$V_{L_2} = V_{BB} - (V_{BB} - V_{DC}) + V_{SM} \tag{4.47}$$

$$V_{L_2\_max} = V_{SM\_meas} + V_{DC\_ref} \tag{4.48}$$

The duty cycle of the S_3 is calculated as follows:

$$d_3 = \frac{V_{BB\_meas} - \hat{V}_{L_1} + V_{SM\_meas} - \hat{V}_{L_2}}{V_{DC\_meas}} \tag{4.49}$$

$$d_3 = \begin{cases} 0 & \frac{V_{BB\_meas} - \hat{V}_{L_1} + V_{SM\_meas} - \hat{V}_{L_2}}{V_{DC\_meas}} < 0 \\ \frac{V_{BB\_meas} - \hat{V}_{L_1} + V_{SM\_meas} - \hat{V}_{L_2}}{V_{DC\_meas}} & 0 \leq \frac{V_{BB\_meas} - \hat{V}_{L_1} + V_{SM\_meas} - \hat{V}_{L_2}}{V_{DC\_meas}} \leq 1 \\ 1 & \frac{V_{BB\_meas} - \hat{V}_{L_1} + V_{SM\_meas} - \hat{V}_{L_2}}{V_{DC\_meas}} > 1 \end{cases} \tag{4.50}$$

After all this discussion, the current control loops for the inductors, adapted to the SPC

scheme, are finally shown in Figure 4-12. As it can be seen, the average value of the collector-emitter voltage of the IGBT$_4$ (V_{CE4}), required for the control implementation, is obtained from the control actions of both control actions ($\hat{V}_{L_1}$ and $\hat{V}_{L_2}$) of both control loops, and also from the feed-forward terms (V_{BB_meas} and V_{SM_meas}). This is the control scheme that will be implemented in the SPC scheme for validation.

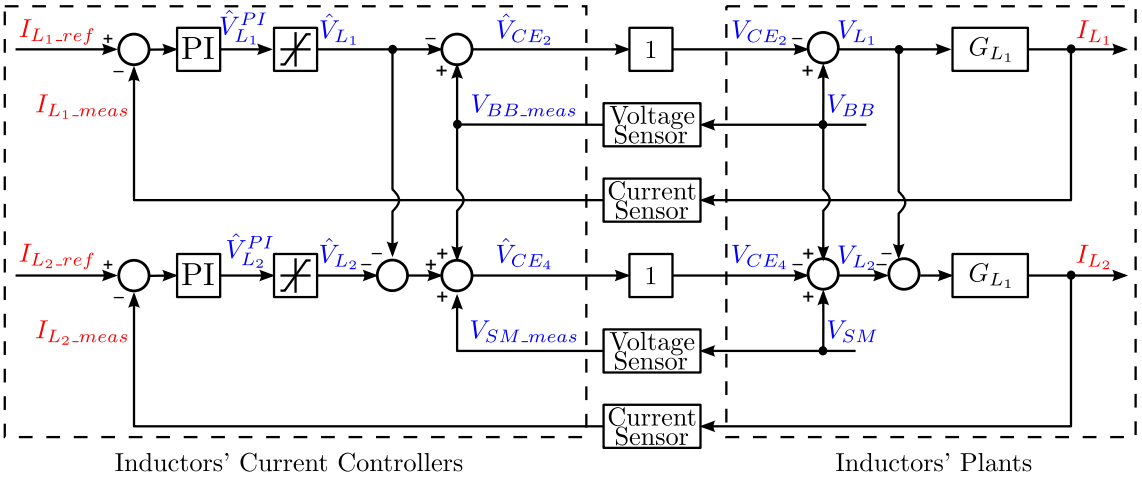


Figure 4-12: The inner current control closed loops.

4.6 Conclusions

It has been discussed how the proposed SPC scheme solves the problem of voltage mismatch between SM voltage and the DC bus voltage, showing a better balance of the thermal and electrical stress on the switches, overcoming the limitation of the duty cycles involved and providing a dynamic symmetric behavior in the charge and discharge operation of the storage devices. The effect on the overall losses has also been quantified, and the adaptations needed in order to apply the already defined control strategies have been stated. In Chapters 7 and 8, the SPC is validated through simulation and experimental results. But prior to that, in the following chapter, a fault ride-through capability for the HESS is going to be studied.

Chapter 5

Contributions for Fault Ride-Through Hybrid Energy Storage Systems

Contents

5.1 Introduction

This chapter describes a new strategy for the design and implementation of a non-isolated fault-tolerant converter solution to integrate HESS in microgrid applications. Firstly, the sensitivity to short-circuits of the PC scheme, considered as the baseline case for implementing the HESS in DC microgrids will be analyzed. After that, the derivation of a Fault-Tolerant Parallel Connection (FTPC) scheme for HESS will be introduced. This solution covers both the power topology and the control scheme required to protect and manage the HESS operation during the DC side short-circuit faults. It also presents a fault ride-through control scheme for the discussed solution. The power topology under consideration is based on the buck-boost bidirectional converter, and it is controlled through a bespoke modulation scheme in order to obtain low losses at normal healthy operation. The operation of the proposed control scheme during a DC bus short-circuit failure is shown, as well as a modification to the standard control in order to achieve the fault ride-through capability, after clearing the fault.

5.2 Fault-Tolerant Topologies

Power quality is a major concern in modern power systems, particularly in weak microgrids. The interest for the economic importance of power quality issues has led the development of standards and regulations that define the requirements for equipment and utilities in grid applications [149, 150]. Faults in power systems are one of the major causes of power quality issues. Therefore, continuous research is being done in turning electric system and its components to Fault-Tolerant (FT) systems, in order to boost and develop a more resilient electric grid [18].

In particular, the effects of voltage issues in microgrids have attracted a lot of attention from the research community. In particular, for the case under consideration in this research, the PCC is implemented through a PEC that interfaces the AC grid with a DC bus.

As seen in previous chapters, the control of the DC bus voltage at the DC side of the grid interfacing converter is critical to ensure adequate operation of the system [66]. In an increasing number of applications, HESS is connected to this DC bus through dedicated PEC, aiming to primarily provide the needed energy in case the microgrid operates in islanding mode. Additionally, the HESS balances the energy flows of the microgrid, accounting for the stochastic behavior of distributed generation and loads; therefore, decreasing this random factor in the power consumed from the grid [66].

The FT HESS are intended to be able to deal with fault conditions in the grid. Depending on the magnitude and the distance to the fault location, the induced variations on the DC bus might vary substantially [10]. For faults far away from the PCC, at distribution or even at transmission levels, the effects within the microgrid are generally limited to voltage sags that can be solved by the regular operation of the HESS. However, for faults at the distribution level closer to the PCC or even at the DC bus inside the microgrid, more severe voltage variations, and also short-circuit currents might appear through the storage subsystem [10]. FT topologies prevent these dangerous short-circuit currents to circulate across the storage subsystem [151, 152]. Also, fault-ride through capability is also expected in this case, and therefore once the fault is removed, the system is can automatically operate properly again in a reasonable amount of time, in accordance to the standards/regulations and the expected behavior of the microgrid [10].

In addition to the lack of galvanic isolation and the operating limits due high voltage rating mismatch of the PC of the bidirectional buck converter, a major disadvantage of this system is its sensitivity to short-circuit faults at the DC bus. If a short-circuit occurs at the DC bus, the current drawn from both the BB and the SM will increase without control, as the anti-parallel diodes of the upper switches in the legs of the converters will allow large short-circuit currents as depicted in Figure 5-1. These short-circuit currents will cause damage to the inductors, the storage devices (BB and SM) and the switches themselves [10, 18].

In order to avoid this behavior of the original topology upon DC faults, a specific device which can interrupt, or at least limit the fault currents flowing through the storage units must be included [10]. One option is to connect switches in series with the storage units and the

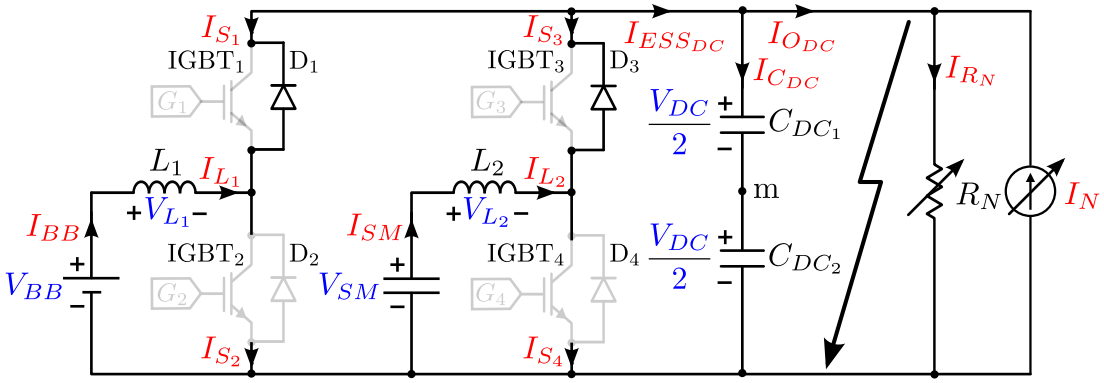


Figure 5-1: Short-circuit fault at the DC bus of the PC of the two bidirectional buck converters.

inductors of the converters, as it can be seen in Figure 5-2. These switches can be opened during fault conditions to prevent the BB and SM short-circuit currents [117].

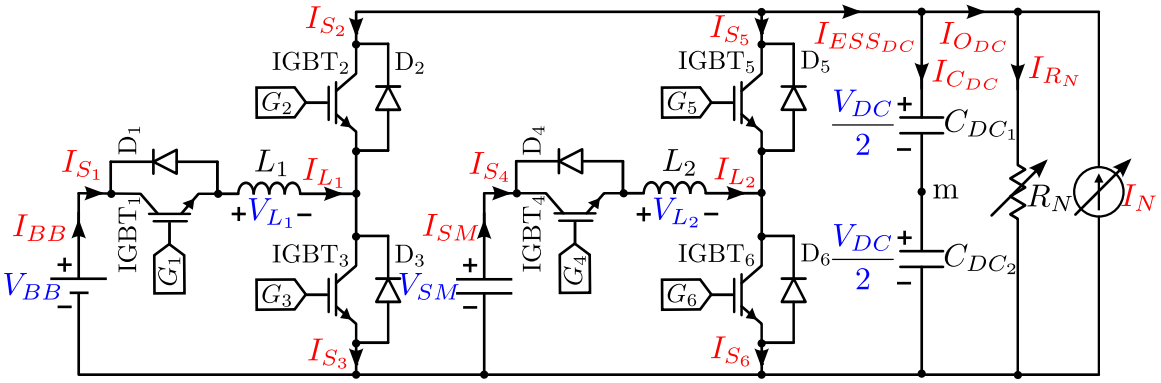


Figure 5-2: The PC of the two bidirectional buck converters with a switch in series between the storage devices and inductors.

But, in order to allow a discharge path for any current flowing through the inductors once the series switches are open, additional free-wheeling switches for each leg are required. Otherwise, a voltage spike will occur, causing an arcing or even destruction of the switches. This eventually yields to a final configuration of two parallel bidirectional non-inverting buck-boost converters [4, 7], as shown in Figure 5-3. This topology can be used for implementing fault tolerance in non-isolated PC of storage devices to a DC bus. This solution, denoted as FTPC, has not been analyzed for this particular challenge.

This buck-boost scheme can operate either as a step-up or a step-down voltage interface. As the buck-boost converter is inherently symmetric, a choice must be made at this

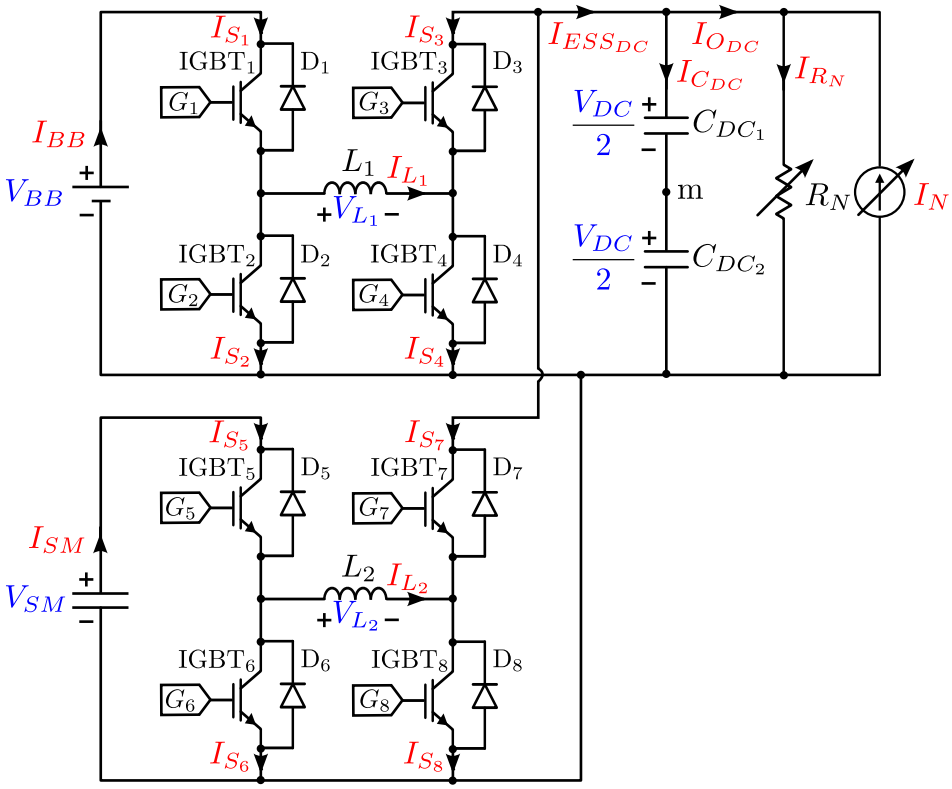


Figure 5-3: The FTPC of the two bidirectional buck-boost converters connected to BB and SM and sharing the DC bus.

stage as to settle a common reference for both converters, and to identify the variables to control. The convention that will be followed along the present work is that upon these conditions, i.e., the storage voltage is smaller than the DC bus voltage, the buck-boost converter operates as a buck converter. This is important to ensure that the control definition of the duty cycles involved is made consistently. Therefore, in the system under consideration, configured as in Figure 5-3, the BB voltage (V_{BB}) and the SM voltage (V_{SM}) ratings are less than the DC bus voltage (V_{DC}) in healthy conditions, the buck-boost converters will always operate as a buck converter. On the other hand, it is assumed that the positive sign of the current is obtained when the storage device is being discharged.

The main feature of this scheme is the operation under fault condition of the HESS, by effectively limiting the current drained from the storage devices if the DC bus is shorted. Provided that a suitable control strategy is implemented, the proposed solution enables a swift system reset once the fault is cleared. It must be noticed that during the fault conditions and immediately after the fault is cleared, the DC voltage will be relatively

small, and then the operation as a boost converter is also required. A proposal for such a fault ride-through feature will also be demonstrated in the following sections.

It is evident that the inclusion of the short-circuit FT features in the converter adds four more switches compared to the original topology (Figure 3-1), therefore resulting in higher cost and size than in the initial case. However, as it will be demonstrated in the following sections, by using a proper control, even though the number of switches has increased, the losses of the two topologies can be made very similar.

5.3 Fault-Tolerant Parallel Connection Converter Operating Modes

Each non-inverting buck-boost converter is implemented by means of two legs, and therefore the HESS converter is now formed by a total amount of eight switches. It is initially assumed that all switches are commutating at High Frequency (HF), as in the PC case. In addition, the complementary switching scheme for a leg is also assumed. But on top of that, both legs in a converter are synchronized. The diagonal switches (S_2-S_3) and (S_6-S_7) are commutating with the values of the duty cycle for the BB and SM converters respectively, while the other diagonal switches (S_1-S_4) and (S_5-S_8) are commutating in a complementary scheme in order to be compared easily with the previous topologies:

$$d_2 = d_3 \tag{5.1}$$

$$d_1 = d_4 = 1 - d_2 = 1 - d_3 \tag{5.2}$$

$$d_6 = d_7 \tag{5.3}$$

$$d_5 = d_8 = 1 - d_6 = 1 - d_7 \tag{5.4}$$

As a result, the only degrees of freedom in the switching pattern are d_2 and d_6, being the duty cycle of the buck-boost converters for the BB and SM, respectively, used in the

well-known steady-state static gain relationships of a buck-boost converter:

$$\frac{V_{BB}}{V_{DC}} = \frac{d_2}{1-d_2} = \frac{d_3}{1-d_3} \tag{5.5}$$

$$\frac{V_{SM}}{V_{DC}} = \frac{d_6}{1-d_6} = \frac{d_7}{1-d_7} \tag{5.6}$$

With these switching patterns, there are four possible switching states as shown in Table 5.1 and Figure 5-4.

Table 5.1: Switching states of the FTPC of the two bidirectional buck-boost converters.

States	BB Converter		SM Converter		Figures
	On	Off	On	Off	
State I	S_1 , S_4	S_2 , S_3	S_5 , S_8	S_6 , S_7	5-4a
State II	S_1 , S_4	S_2 , S_3	S_6 , S_7	S_5 , S_8	5-4b
State III	S_2 , S_3	S_1 , S_4	S_6 , S_7	S_5 , S_8	5-4c
State IV	S_2 , S_3	S_1 , S_4	S_5 , S_8	S_6 , S_7	5-4d

At each switch at the converter, the current can flow either through the IGBT or the anti-parallel diode, depending on whether the ESSs device is charging or discharging. This particular issue is shown in Table 5.2.

Table 5.2: Switching states of the PC of the two bidirectional buck-boost converters of the On switches.

States	BB Converter (On Switches)		SM Converter (On Switches)	
	BB Discharging	BB Charging	SM Discharging	SM Charging
State I	$IGBT_1$, $IGBT_4$	D_1 , D_4	$IGBT_5$, $IGBT_8$	D_5 , D_8
State II	$IGBT_1$, $IGBT_4$	D_1 , D_4	D_6 , D_7	$IGBT_6$, $IGBT_7$
State III	D_2 , D_3	$IGBT_2$, $IGBT_3$	D_6 , D_7	$IGBT_6$, $IGBT_7$
State IV	D_2 , D_3	$IGBT_2$, $IGBT_3$	$IGBT_5$, $IGBT_8$	D_5 , D_8

Still ensuring that the voltage across both ESSs (V_{BB} and V_{SM}) are smaller than the DC bus voltage (V_{DC}), but depending on the relative values of the storage device voltages, there are three possible conditions in the operation of the converters:

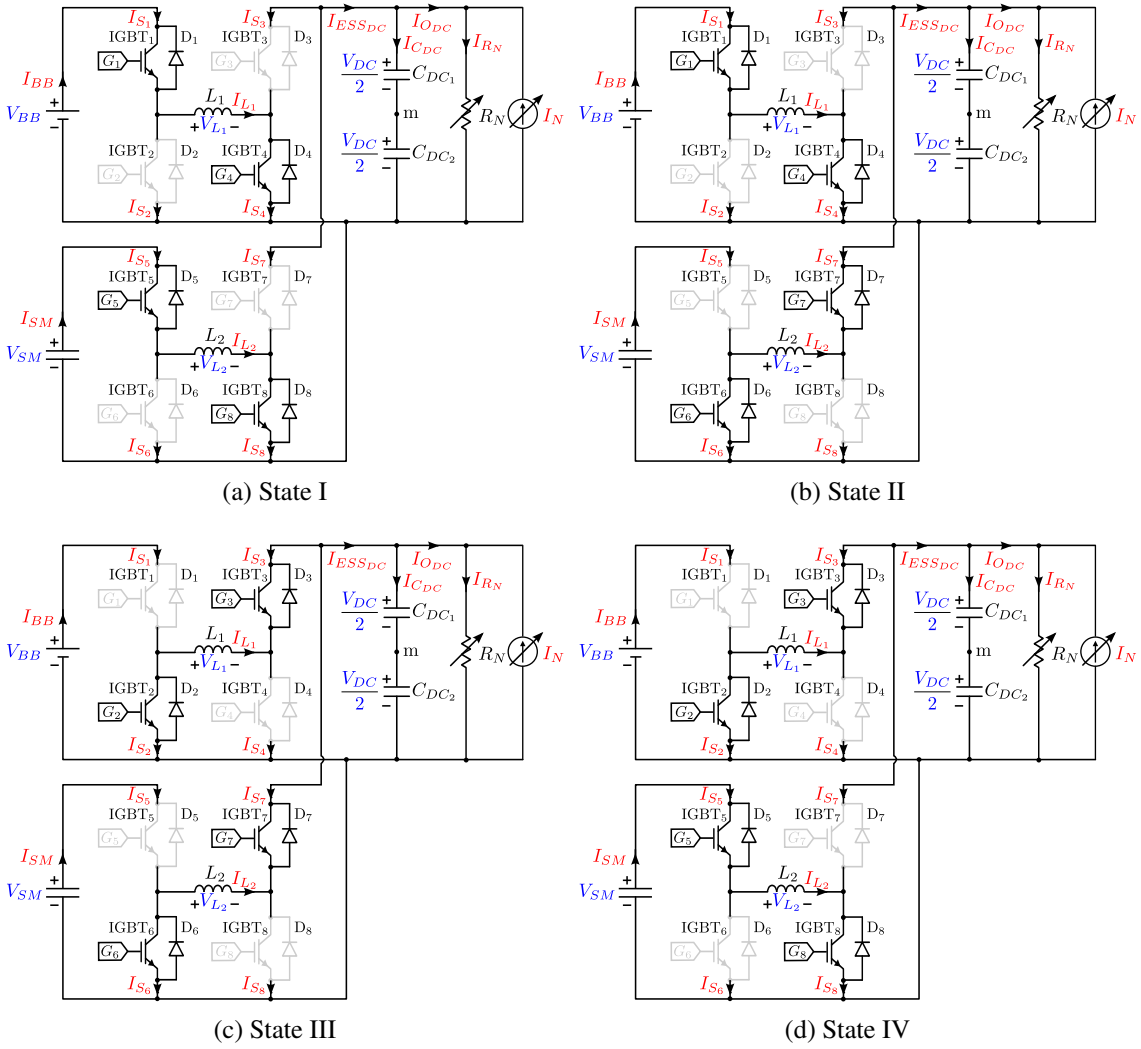


Figure 5-4: Switching states of the FTPC of the two bidirectional buck-boost converters.

- If $V_{BB} < V_{SM}$, then from Equations (5.5) and (5.6), then:

$$d_2 < d_6 \tag{5.7}$$

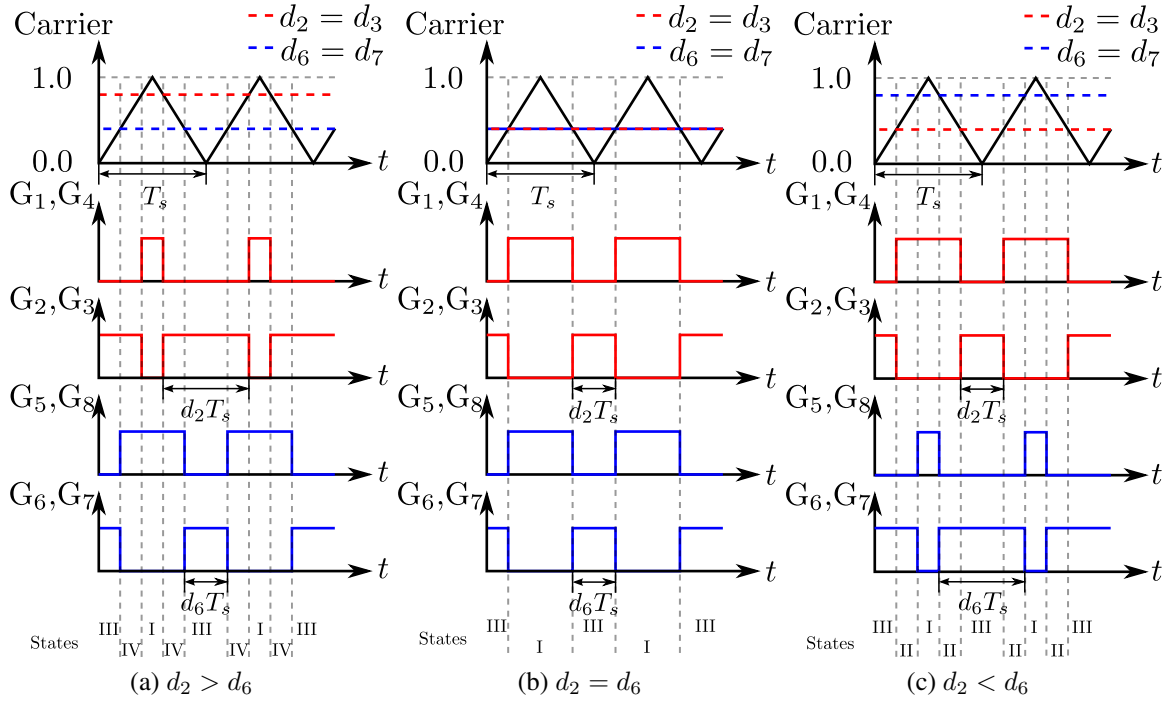
- If $V_{BB} = V_{SM}$, again from Equations (5.5) and (5.6):

$$d_2 = d_6 \tag{5.8}$$

- And, finally, if $V_{BB} > V_{SM}$, analogously,

$$d_2 > d_6 \tag{5.9}$$

Depending on these three possibilities, the switching states will change as derived from Figure 5-5. In this Figure, the *on* and *off* times are defined as those of the diagonal switches (S_2-S_3) and (S_6-S_7) of each converter.



(a) $d_2 > d_6$ (b) $d_2 = d_6$ (c) $d_2 < d_6$

Figure 5-5: The switching states of the FTPC of the two bidirectional buck-boost converters depending on the values of the duty cycles.

5.4 Control Scheme during Healthy Condition

The same control schemes depicted in Chapter 3, for the islanding and the grid-tied modes can be implemented in the FTPC scheme. At each mode, the performance of both the independent and full designs of the control schemes are thus ensured. However, in order to achieve a perfectly matched behavior of these control system with respect to the standard PC scheme, some modifications are required. Given that the expressions that relate

the voltages ratio and the duty cycles in the topology are different, the control blocks that compute the duty cycle from the output of the regulator (*Duty Cycle Calculation Blocks* at Figures 3-8, 3-17 and 3-21), need to be adapted.

Again, and considering transient state, the inductor voltage connected to the BB (V_{L_1}) can be calculated by using KVL in Figure 5-3:

$$V_{BB} - V_{CE_1} - V_{L_1} - V_{CE_4} = 0 \tag{5.10}$$

$$V_{BB} - d_2 \cdot V_{BB} - V_{L_1} - d_3 \cdot V_{DC} = 0 \tag{5.11}$$

By substituting d_3 from Equations (5.3) into (5.11) yields to:

$$V_{BB} - d_2 \cdot V_{BB} - V_{L_1} - d_2 \cdot V_{DC} = 0 \tag{5.12}$$

$$V_{BB} - V_{L_1} - d_2(V_{BB} + V_{DC}) = 0 \tag{5.13}$$

$$V_{L_1} = V_{BB} - d_2(V_{BB} + V_{DC}) \tag{5.14}$$

In order to calculate the limits for the control action of the PI current controller (inductor voltage), the maximum and minimum values for the duty cycles involved need to be computed. The lower limit is obtained at a duty cycle of switches S_2 and S_3 equal to unity (i.e., $d_2 = d_3 = 1$) (State III or IV):

$$V_{L_1} = V_{BB} - (V_{BB} + V_{DC}) \tag{5.15}$$

$$V_{L_1\_min} = -V_{DC\_ref} \tag{5.16}$$

On the other hand, the upper limit is obtained at the duty cycle of switches S_2 and S_3 equal to zero (i.e., $d_2 = d_3 = 0$) (State I or II) yielding to:

$$V_{L_1} = V_{BB} \tag{5.17}$$

$$V_{L_1\_max} = V_{BB\_meas} \tag{5.18}$$

With the same mathematical manipulation and using KVL to calculate the inductor

voltage connected to the SM (V_{L_2}), the following relations obtained:

$$V_{SM} - V_{CE_5} - V_{L_2} - V_{CE_8} = 0 \tag{5.19}$$

$$V_{SM} - d_6 \cdot V_{SM} - V_{L_2} - d_7 \cdot V_{DC} = 0 \tag{5.20}$$

Again, by substituting d_7 from Equations (5.1) into (5.20) yields to:

$$V_{SM} - d_6 \cdot V_{SM} - V_{L_2} - d_6 \cdot V_{DC} = 0 \tag{5.21}$$

$$V_{SM} - V_{L_2} - d_6(V_{SM} + V_{DC}) = 0 \tag{5.22}$$

$$V_{L_2} = V_{SM} - d_6(V_{SM} + V_{DC}) \tag{5.23}$$

The lower limit is calculated at duty cycles of switches S_6 and S_7 equal to unity (i.e., $d_6 = d_7 = 1$) (State II or III) yielding to:

$$V_{L_2} = V_{SM} - (V_{SM} + V_{DC}) \tag{5.24}$$

$$V_{L_2\_min} = -V_{DC\_ref} \tag{5.25}$$

Finally, the upper limit is calculated at duty cycle of switches S_6 and S_7 equal to zero (i.e., $d_6 = d_7 = 0$) (State I or IV) yielding to:

$$V_{L_2} = V_{SM} \tag{5.26}$$

$$V_{L_2\_max} = V_{SM\_meas} \tag{5.27}$$

From Equation (5.13), the duty cycle of switches S_2 and S_3 is obtained as follows:

$$d_2(V_{BB} + V_{DC}) = V_{BB} - V_{L_1} \tag{5.28}$$

$$d_2 = \frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{BB\_meas} + V_{DC\_meas}} \tag{5.29}$$

The limits of the duty cycle of switches S_2 and S_3 are given by:

$$d_2 = d_3 = \begin{cases} 0 & \frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{BB\_meas} + V_{DC\_meas}} < 0 \\ \frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{BB\_meas} + V_{DC\_meas}} & 0 \leq \frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{BB\_meas} + V_{DC\_meas}} \leq 1 \\ 1 & \frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{BB\_meas} + V_{DC\_meas}} > 1 \end{cases} \tag{5.30}$$

The same manipulation for Equation (5.22) is done for the duty cycle of switches S_6 and S_7:

$$d_6(V_{SM} + V_{DC}) = V_{SM} - V_{L_2} \tag{5.31}$$

$$d_6 = \frac{V_{SM\_meas} - \hat{V}_{L_2}}{V_{SM\_meas} + V_{DC\_meas}} \tag{5.32}$$

The limits of the duty cycle of switches S_6 and S_7 are thus:

$$d_6 = d_7 = \begin{cases} 0 & \frac{V_{SM\_meas} - \hat{V}_{L_2}}{V_{SM\_meas} + V_{DC\_meas}} < 0 \\ \frac{V_{SM\_meas} - \hat{V}_{L_2}}{V_{SM\_meas} + V_{DC\_meas}} & 0 \leq \frac{V_{SM\_meas} - \hat{V}_{L_2}}{V_{SM\_meas} + V_{DC\_meas}} \leq 1 \\ 1 & \frac{V_{SM\_meas} - \hat{V}_{L_2}}{V_{SM\_meas} + V_{DC\_meas}} > 1 \end{cases} \tag{5.33}$$

Given that, at steady state, the voltages across the inductors are null, the duty cycles are calculated from:

$$d_2 = \frac{V_{BB\_meas}}{V_{BB\_meas} + V_{DC\_meas}} \tag{5.34}$$

$$d_6 = \frac{V_{SM\_meas}}{V_{SM\_meas} + V_{DC\_meas}} \tag{5.35}$$

Finally, from Equations (5.29) and (5.32), the control scheme for this scheme can be now depicted and is represented in Figure 5-6. Notice how the BB and SM *Duty Cycle Calculation Blocks* now consider the specific case of the FTPC scheme topology.

At this point, the theoretical derivations for making compatible the healthy operation of the buck-boost converter with the standard PC scheme have been shown. The next section deals with the operation of the buck-boost topology under faulty conditions. Neverthe-

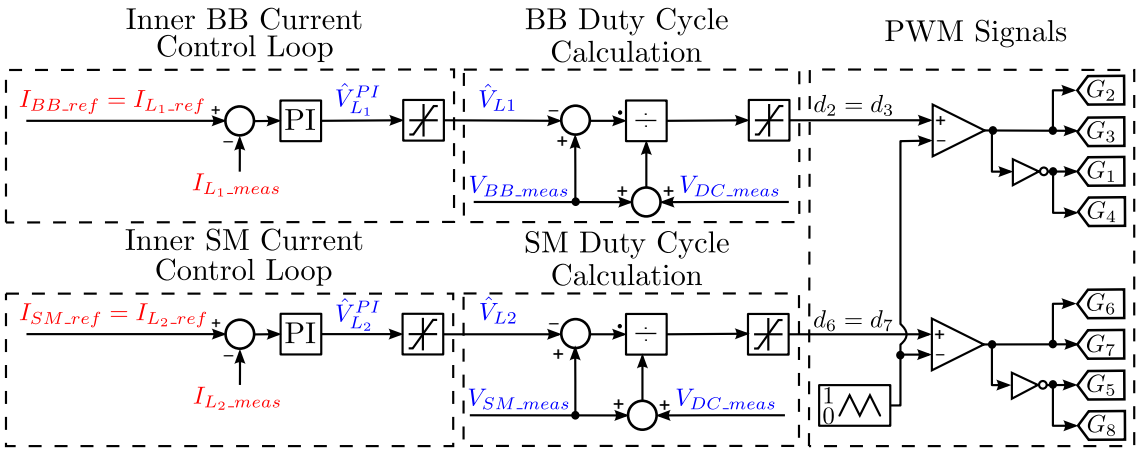


Figure 5-6: Inner current controllers scheme for the two bidirectional buck-boost converters.

less, it must be remarked that in this initial approach all the switches are commutating at HF. This yields to high losses in the switches, roughly twice the switching and conduction losses than in the PC case, and therefore the total efficiency of the system will drop, as compared to the mentioned original PC scheme. This point will be quantitatively demonstrated in Chapter 7.

An alternate switching scheme, aiming to fix this efficiency issue, is proposed in forthcoming sections after the fault operation of the original buck-boost scheme operation is studied.

5.5 Proposed Control Scheme during Faulty Condition

The most critical short-circuit faults types in DC microgrids, with the split DC bus scheme of Figure 5-3, are either a short-circuit between positive and negative bus bars or a short-circuit between any bus bar and ground [18, 153]. In the first approach of the proposed control scheme, once a DC bus short-circuit fault is detected (for instance by detecting a DC bus voltage below a threshold level), all the switches of the storage converters will be turned off [117]. Therefore the storage devices are instantly disconnected from the DC bus while allowing a discharge path for the inductors at the converters through the anti-parallel diodes of the switches. After the inductances are discharged, no more energy is

interchanged between the HESS and the DC bus. However, this first control scheme does not have a ride-through capability, and therefore even if the fault is removed, the system by itself has no ability for returning to the initial operation mode, unless the control is reset manually and the DC bus is charged externally. After the DC bus is back at rated values, the control scheme works again, and the HESS will remain to support the microgrid normal operation. This scheme is shown in Figure 5-7.

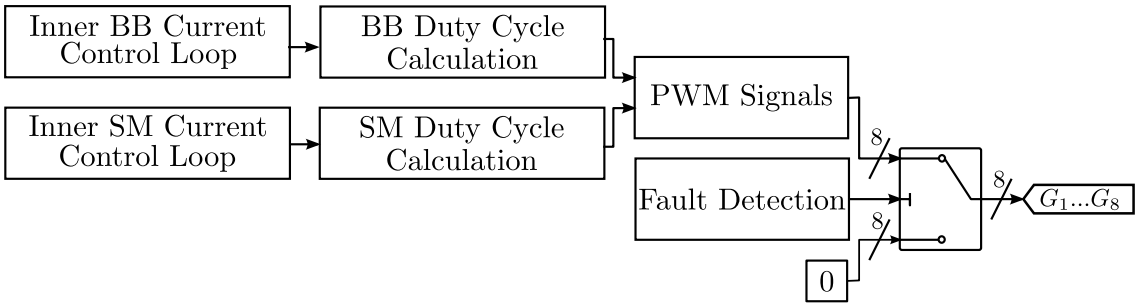


Figure 5-7: Control scheme including the fault detection block and the pulse disabling.

However, by making a relatively simple modification to the control scheme, the converter can still operate in a controlled manner under fault conditions and can resume normal healthy operation once the fault is over. This modification is introduced in Figure 5-8,

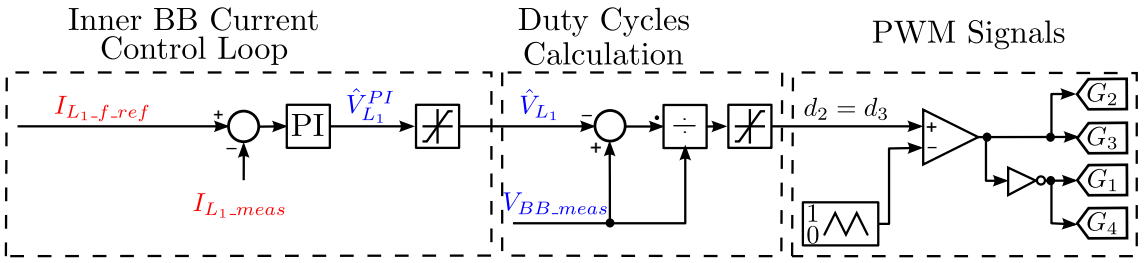


Figure 5-8: The proposed control of the FTPC of the two bidirectional buck-boost converters during the DC bus fault.

The fault sequence operation of this control scheme is outlined in Figure 5-9. The DC bus fault occurs at t_f. Then, the fault ride-through capability of the proposed strategy is achieved by providing a small safe current reference ($I_{L_1\_f\_ref}$) value for the BB converter only under DC bus short-circuit. While the DC bus fault is still present, the DC bus voltage remains nearly zero. However, this small current enables the DC bus capacitance to charge linearly once the fault is cleared ar t_c. Once a threshold value is reached at t_n, the system

gets back to the normal operation scheme, and the standard control takes the system back to the steady state at t_{ss}. This current reference value must be low enough as not to discharge the BB in a reasonable time frame. On the other side, this value must be large enough as to allow a fast detection of the fault clearance condition. Ultimately, this reference value is a function of the DC bus voltage rating and the DC bus capacitance.

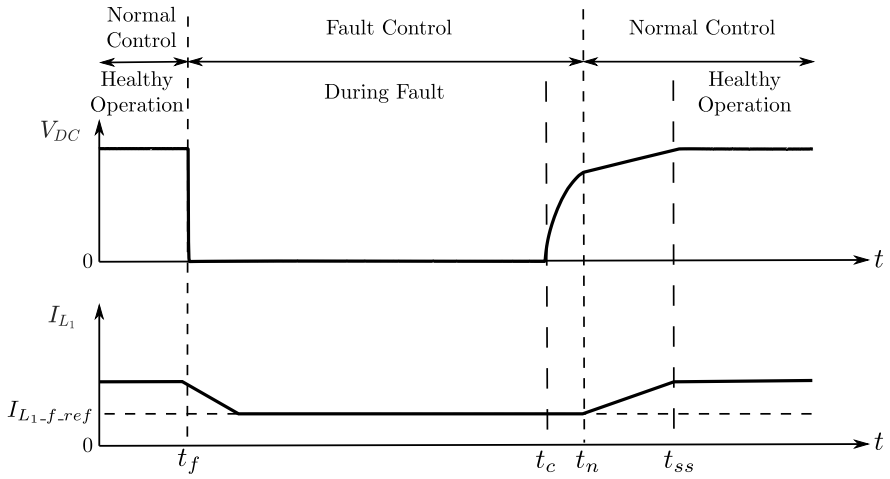
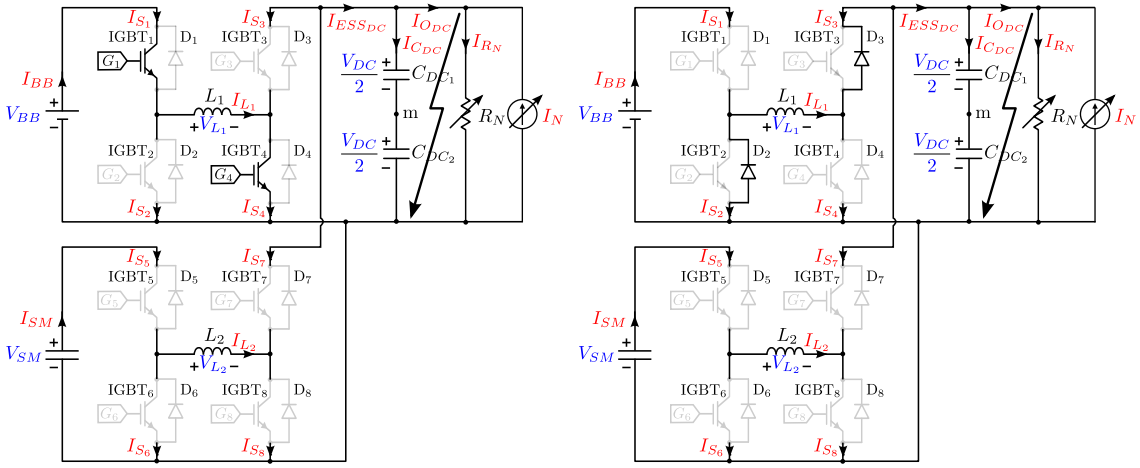


Figure 5-9: Performance of the fault ride-through control sequence.

In any case, the switches of the SM converter will be turned off continuously from the fault detection until the fault ride-through stage is over. Thus, there are only two switching states as in Table 5.3 and Figure 5-10. The current flows in the switch through IGBT during state I and the anti-parallel D during state II as in Table 5.4 because the BB is only discharging. The $IGBT_1$ and $IGBT_4$ are commutating with the value of the duty cycle of the BB as shown in Figure 5-11.

Table 5.3: The switching states of the PC of the two bidirectional buck-boost converters during the fault.

States	BB Converter		SM Converter		Figures
	On	Off	On	Off	
State I	S_1 , S_4	S_2 , S_3	-	S_5 , S_6 , S_7 , S_8	5-10a
State II	S_2 , S_3	S_1 , S_4	-	S_5 , S_6 , S_7 , S_8	5-10b



(a) State I (b) State II

Figure 5-10: The switching states of the PC of the two bidirectional buck-boost converters during short-circuit fault at the DC bus.

Table 5.4: The switching states of the PC of the two bidirectional buck-boost converters of the On switches during the fault.

States	BB Converter (On Switches)
	Discharging
State I	$IGBT_1$, $IGBT_4$
State II	D_2 , D_3

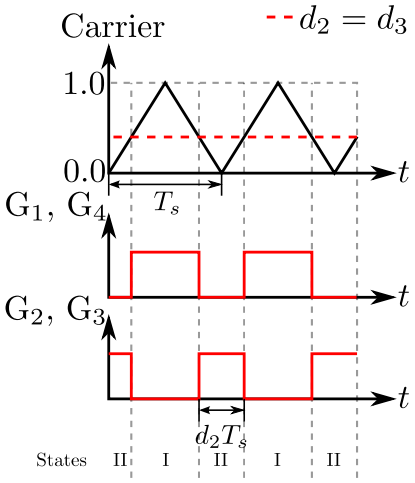


Figure 5-11: The switching states of the PC of the two bidirectional buck-boost converters.

At the DC bus short-circuit fault, the voltage of the DC bus is almost null ($V_{DC} \simeq 0$). Substituting in Equation (5.14), yielding to:

$$V_{L_1} = V_{BB} - d_2 \cdot V_{BB} \tag{5.36}$$

$$V_{L_1} = (1 - d_2)V_{BB} \tag{5.37}$$

By putting the minimum and maximum values of the duty cycle, the limits of the voltage of the inductor are calculated as follows:

$$V_{L_1\_min} = 0 \tag{5.38}$$

$$V_{L_1\_max} = V_{BB\_meas} \tag{5.39}$$

Therefore, the duty cycle for switches S_2 and S_3 is given by:

$$1 - d_2 = \frac{V_{L_1}}{V_{BB}} \tag{5.40}$$

$$d_2 = 1 - \frac{V_{L_1}}{V_{BB}} \tag{5.41}$$

$$d_2 = \frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{BB\_meas}} \tag{5.42}$$

The limits of the duty cycle for switches S_2 and S_3 as follows:

$$d_2 = d_3 = \begin{cases} 0 & \frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{BB\_meas}} < 0 \\ \frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{BB\_meas}} & 0 \leq \frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{BB\_meas}} \leq 1 \\ 1 & \frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{BB\_meas}} > 1 \end{cases} \tag{5.43}$$

However, in this control scheme (Figure 5-8), the carrier is using values from 0.0 to 1.0. During fault and fault ride-through intervals, the switches of the SM converter are turned off, and SM current is null. It also must be noticed that if the fault is permanent, the control is designed to operate for a specific time and then the switches of the BB converters will be turned off in order to decrease the power dissipated from the BB. Another advantage is

that this control can be used to charge the DC bus at system start-up.

Simulated and experimental demonstrations of the fault and fault ride-through performance of the FTPC topology, with the outlined control scheme, are included in Chapters 7 and 8.

5.6 Double Modulation Switching Scheme of the Fault-Tolerant Parallel Connection

As it has been discussed before, the FTPC solution (all the switches in the converters are commuting at HF) presents increased losses compared to the PC scheme, i.e., the standard non-inverting buck-boost approach. In order to decrease these switching losses, only one leg at each converter will switch at HF, thus obtaining the behavior of a simple buck (or boost) DC/DC converter.

For instance, looking at Figure 5-3, S_1 and S_5 could be forced to turn on all time in healthy conditions, while S_2 and S_6 could be turned off. This scheme implies that the switching losses at the storage-side legs of the converters (S_1-S_2 and S_5-S_6) will be null, thus decreasing the overall switching losses. In this case, the resulting converters operate as standard buck converters, for all the duty cycle possible values at the upper switches S_3 and S_7 (d_3 and d_7, respectively). This is consistent with the definition of the static gain of the converters already stated at Equations (3.67) and (3.68) in Chapter 3 for the PC. These expressions are modified now for this topology considering the switch labels to be:

$$d_3 = \frac{V_{BB}}{V_{DC}} \tag{5.44}$$

$$d_7 = \frac{V_{SM}}{V_{DC}} \tag{5.45}$$

This buck converter mode of the setup is also consistent with the healthy operation of the system, as it is implicitly considered that both storage devices present voltage ratings smaller than the DC bus voltage rated values. Therefore, all the control schemes used in the PC of the two bidirectional converters depicted in Chapter 3 can be directly used.

Nevertheless, this approach prevents the use of the FTPC approach in boost operating mode, i.e., when any of the storage device voltages is greater than the DC bus voltage. As a general discussion, this situation would increase the applicability of the FTPC to situations in which in steady state the storage ratings is greater than the DC bus ratings, such as low-voltage DC bus applications (house-hold safe DC values, automotive, etc.). It will increase also the applicability to extend the voltage ratings of the storage subsystems, for instance in case the electrochemical battery presents higher voltage ratings (e.g., in order to increase the storage capability, etc.). But the real, specific reason to use this boost mode in every application is that it would allow controlling the power flows when the DC bus voltage is very low (for instance, after start-up, during DC bus faults).

For the boost operation mode, the strategy is to keep S_3 and S_7 continuously turned on, whereas S_4 and S_8 are turned off permanently. This means that the leg of the converters adjacent to the DC bus is not switching at HF; instead, the control signals at the converters are going to be the HF duty cycles of the lower switches S_2 and S_6 (d_2 and d_6), respectively. As usual, the upper switches are governed by means of the complementary scheme. This provides the following relationships in steady state in this case:

$$\frac{1}{1-d_2} = \frac{V_{BB}}{V_{DC}} \Rightarrow d_2 = \frac{V_{BB} - V_{DC}}{V_{BB}} \tag{5.46}$$

$$\frac{1}{1-d_6} = \frac{V_{SM}}{V_{DC}} \Rightarrow d_6 = \frac{V_{SM} - V_{DC}}{V_{SM}} \tag{5.47}$$

In all the cases, i.e., buck-boost, buck and boost modes, the equations for the inductor voltage values, when the converter is in transient, can also be derived. Both the steady-state and the transient stage equations for the BB converter can be summarized as it is expressed in Table 5.5.

Apparently, the buck-boost case inherently covers all the possible cases (buck and boost modes) for the system operation, but at the cost of an increase in the switching losses, as previously mentioned.

However, to take advantage of both the buck and boost modes of the FTPC solution in a unified control scheme, and at the same time decrease the switching losses, the use of a hybrid modulation scheme that implements two carriers is proposed. The idea of

Table 5.5: Duty cycles of the BB and SM converters in case of buck-boost mode, buck mode, and boost mode.

	Buck-boost mode	Buck mode	Boost mode
BB Converter	$(d_{bb\_BB} = d_2 = d_3)\epsilon(0,1)$	$(d_{bu\_BB} = d_3)\epsilon(0,1)$	$(d_{bo\_BB} = d_2)\epsilon(0,1)$
Steady State	$\frac{V_{BB}}{V_{BB}+V_{DC}}$	$\frac{V_{BB}}{V_{DC}}$	$\frac{V_{BB}-V_{DC}}{V_{BB}}$
Transient stage	$\frac{V_{BB}-V_{L_1}}{V_{BB}+V_{DC}}$	$\frac{V_{BB}-V_{L_1}}{V_{DC}}$	$\frac{V_{BB}-V_{DC}-V_{L_1}}{V_{BB}}$
SM Converter	$(d_{bb\_SM} = d_5 = d_6)\epsilon(0,1)$	$(d_{bu\_SM} = d_6)\epsilon(0,1)$	$(d_{bo\_SM} = d_5)\epsilon(0,1)$
Steady State	$\frac{V_{SM}}{V_{SM}+V_{DC}}$	$\frac{V_{SM}}{V_{DC}}$	$\frac{V_{SM}-V_{DC}}{V_{SM}}$
Transient stage	$\frac{V_{SM}-V_{L_2}}{V_{SM}+V_{DC}}$	$\frac{V_{SM}-V_{L_2}}{V_{DC}}$	$\frac{V_{SM}-V_{DC}-V_{L_2}}{V_{SM}}$

the proposed control strategy deals with using two independent modes of operation for each converter in steady state. These modes are the already commented buck mode for healthy conditions, and the boost mode in low DC bus conditions (transient stages after the fault takes place or at system start-up). This scheme aims to decrease the number of commutating switches in each converter, in order to consequently minimize the switching losses [84, 94, 154–157], but at the same time, simplifying the control scheme.

For the implementation of the unified dual boost or buck options, once the driving scheme has provided the control action coming from the regulators, and depending on the existing operation mode, the *Duty Cycle Calculation Blocks* in the control system need to be defined according to Equations (5.29) and (5.32). But this operation mode, in turn, depends on the relative values of the storage and DC bus voltage values, and thus this selection must be made in real time. The change in control schemes needs to be swift, fast and automatic, in order to fully achieve the desired behavior. The first idea is to use the existing buck-boost control scheme derived in the previous sections, using the same *Duty Cycle Calculation Blocks* as defined in Figure 5-6. The operating mode can be obtained

naturally from the value of the duty cycle, given that:

- For the BB converter:

$$d_{bb\_BB} < 0.5 \Rightarrow V_{BB} < V_{DC} \Rightarrow \text{buck mode} \Rightarrow \text{DC bus leg at HF} \quad (5.48)$$

$$d_{bb\_BB} > 0.5 \Rightarrow V_{BB} > V_{DC} \Rightarrow \text{boost mode} \Rightarrow \text{BB leg at HF} \quad (5.49)$$

- For the SM converter:

$$d_{bb\_SM} < 0.5 \Rightarrow V_{SM} < V_{DC} \Rightarrow \text{buck mode} \Rightarrow \text{DC bus leg at HF} \quad (5.50)$$

$$d_{bb\_SM} > 0.5 \Rightarrow V_{SM} > V_{DC} \Rightarrow \text{boost mode} \Rightarrow \text{SM leg at HF} \quad (5.51)$$

Thus, a simple manner to naturally obtain the dual behavior is to use two different triangular carrier signals to generate the pulses for the converter branches, parting from the *Duty Cycle Calculation Blocks* defined at the buck-boost control scheme. One carrier is intended for the buck mode only (using values of the triangular modulating waveform from 0.0 to 0.5), and the output of the comparison will provide the duty ratios d_3 and d_7 to drive only the DC side leg switches at HF, S_3-S_4 and S_7-S_8 for the BB and SM converters, respectively. In this situation, the rest of the switches will remain in a static condition as to allow the buck mode operation.

On the other hand, another carrier will be implemented for the boost mode (using values from 0.5 to 1.0). Analogously, it will generate the HF driving signals for switches S_1-S_2 and S_5-S_6, keeping the rest of the switches in a constant state to allow for the boost mode. This scheme is outlined in Figure 5-12.

According to this proposed switching pattern, there are nine possible switching states as it is detailed in Table 5.6 and Figure 5-13. As in the previous analysis, depending on the sign of the current through the switch, it can flow either through the IGBT or through the anti-parallel diode. This is shown in Table 5.7, taking as reference the charging or discharging of the respective ESS device.

In any case, for every possible operating condition, the converters can operate in boost or buck mode independently. This implies four combinations, that account for both con-

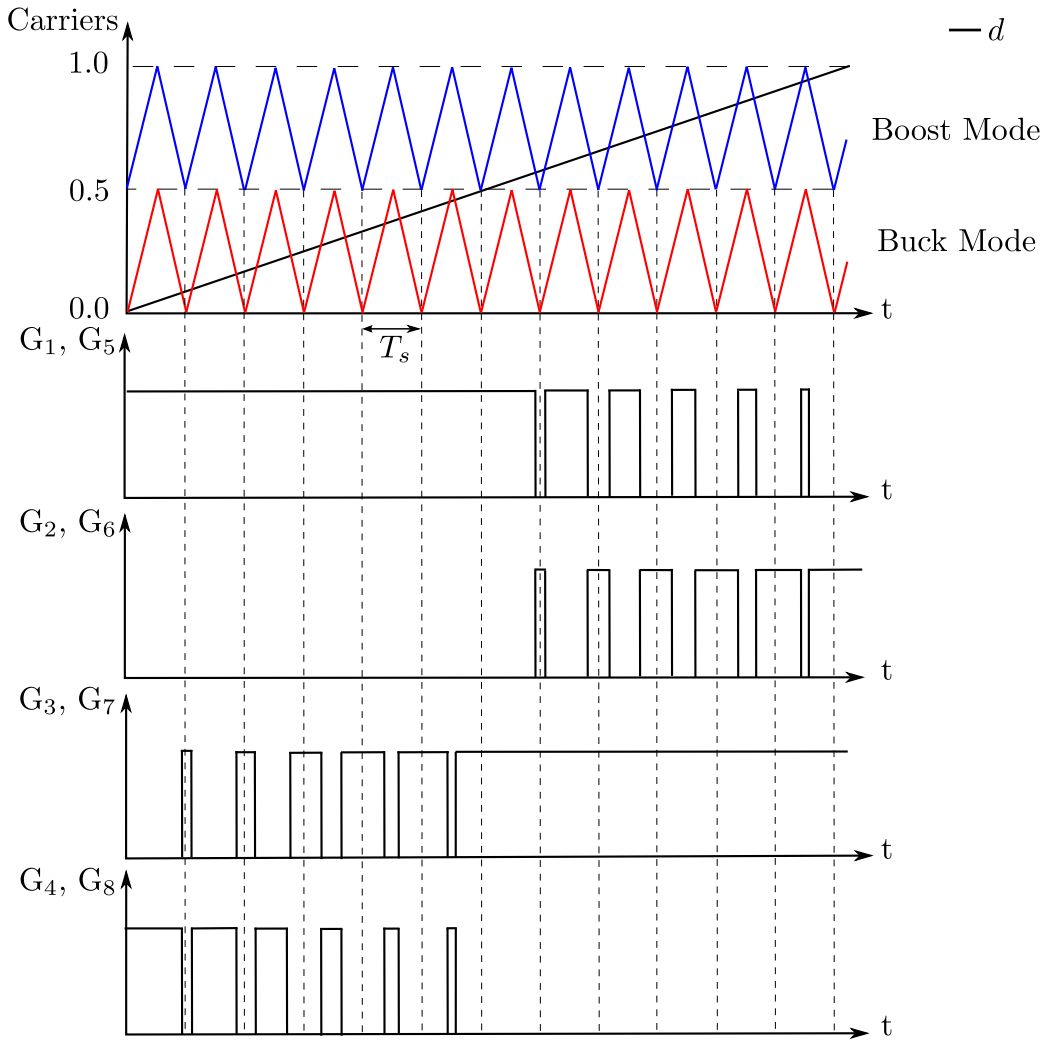


Figure 5-12: The proposed PWM modulation of the FTPC of the two bidirectional buck-boost converters based on two different carriers.

verters operating in buck mode, both in boost mode or one in buck mode and the other in boost mode. Thus, the four cases stated in Table 5.8 will be considered. For each of these cases, a set of switching states appear. Additionally, the relative value of the duty cycles of the converters, for each case, is also taken into account in order to define all the possible switching states. In cases 1 and 2 (both converters in buck mode or both in boost mode, respectively), three possibilities for the relative values of the duty cycles of both ESS are going to be considered. These three conditions, ($d_2 > d_6$, $d_2 = d_6$ and $d_2 < d_6$), are described in Figure 5-14 for case 1 and Figure 5-15 for case 2. In case 3, though, only two possibilities are considered: ($d_2 > d_6 - 0.5$ or $d_2 < d_6 - 0.5$), as it is shown in Figure

Table 5.6: The switching states of the FTPC of the two bidirectional buck-boost converters.

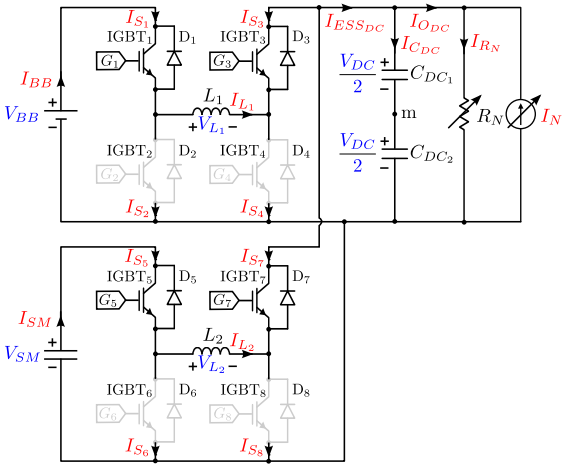
States	BB Converter		SM Converter		Figures
	On	Off	On	Off	
State I	S_1 , S_3	S_2 , S_4	S_5 , S_7	S_6 , S_8	5-13a
State II	S_1 , S_3	S_2 , S_4	S_5 , S_8	S_6 , S_7	5-13b
State III	S_1 , S_3	S_2 , S_4	S_6 , S_7	S_5 , S_8	5-13c
State IV	S_1 , S_4	S_2 , S_3	S_5 , S_7	S_6 , S_8	5-13d
State V	S_1 , S_4	S_2 , S_3	S_5 , S_8	S_6 , S_7	5-13e
State VI	S_1 , S_4	S_2 , S_3	S_6 , S_7	S_5 , S_8	5-13f
State VII	S_2 , S_3	S_1 , S_4	S_5 , S_7	S_6 , S_8	5-13g
State VIII	S_2 , S_3	S_1 , S_4	S_5 , S_8	S_6 , S_7	5-13h
State IX	S_2 , S_3	S_1 , S_4	S_6 , S_7	S_5 , S_8	5-13i

Table 5.7: The switching states of the FTPC of the two bidirectional buck-boost converters of the On switches.

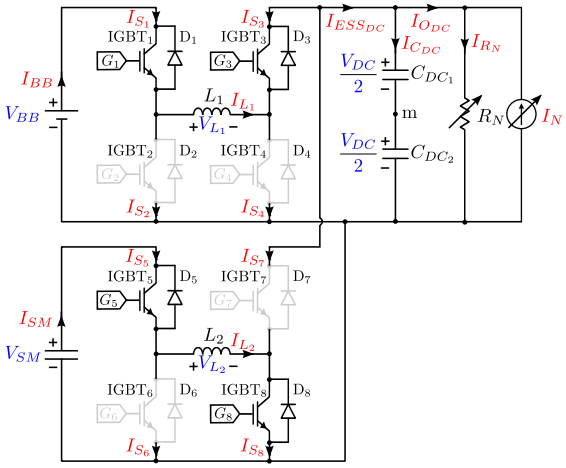
States	BB Converter (On Switches)		SM Converter (On Switches)	
	BB Discharging	BB Charging	SM Discharging	SM Charging
State I	$IGBT_1$, D_3	D_1 , $IGBT_3$	$IGBT_5$, D_7	D_5 , $IGBT_7$
State II	$IGBT_1$, D_3	D_1 , $IGBT_3$	$IGBT_5$, $IGBT_8$	D_5 , D_8
State III	$IGBT_1$, D_3	D_1 , $IGBT_3$	D_6 , D_7	$IGBT_6$, $IGBT_7$
State IV	$IGBT_1$, $IGBT_4$	D_1 , D_4	$IGBT_5$, D_7	D_5 , $IGBT_7$
State V	$IGBT_1$, $IGBT_4$	D_1 , D_4	$IGBT_5$, $IGBT_8$	D_5 , D_8
State VI	$IGBT_1$, $IGBT_4$	D_1 , D_4	D_6 , D_7	$IGBT_6$, $IGBT_7$
State VII	D_2 , D_3	$IGBT_2$, $IGBT_3$	$IGBT_5$, D_7	D_5 , $IGBT_7$
State VIII	D_2 , D_3	$IGBT_2$, $IGBT_3$	$IGBT_5$, $IGBT_8$	D_5 , D_8
State IX	D_2 , D_3	$IGBT_2$, $IGBT_3$	D_6 , D_7	$IGBT_6$, $IGBT_7$

5-16. Finally, case 4 has also two possibilities ($d_2 - 0.5 > d_6$ or $d_2 - 0.5 < d_6$) that are expressed in Figure 5-17. It must be remarked that for cases 3 and 4, the value of 0.5 needs to be subtracted from the duty cycle in order to compare both duty cycles at the BB and SM converters.

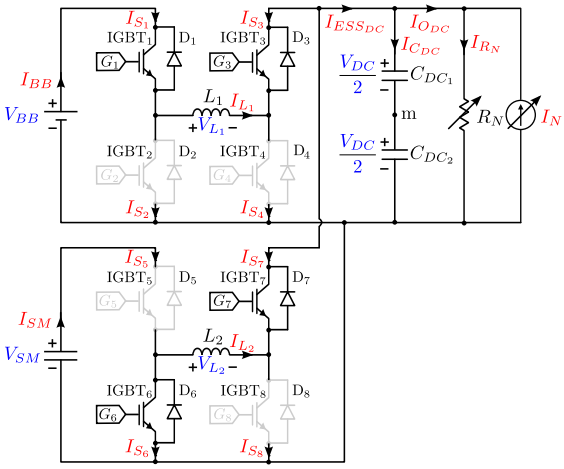
As mentioned, it is assumed that in healthy conditions, the voltage values at the BB and the SM are smaller than the DC bus voltage value, and both ESS converters are operating in buck mode. Thus, case 1 from Table 5.8 is considered. Upon this case 1 operation,



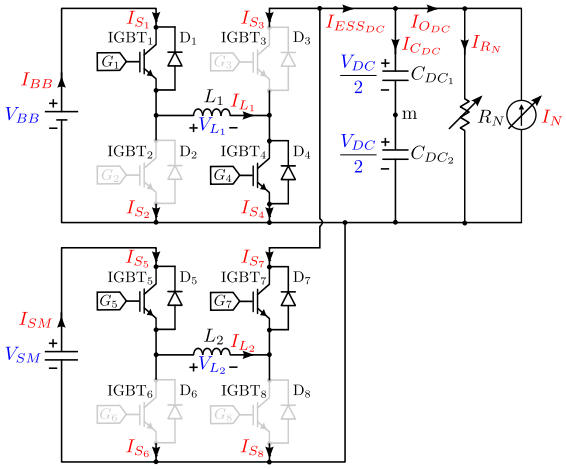
(a) State I



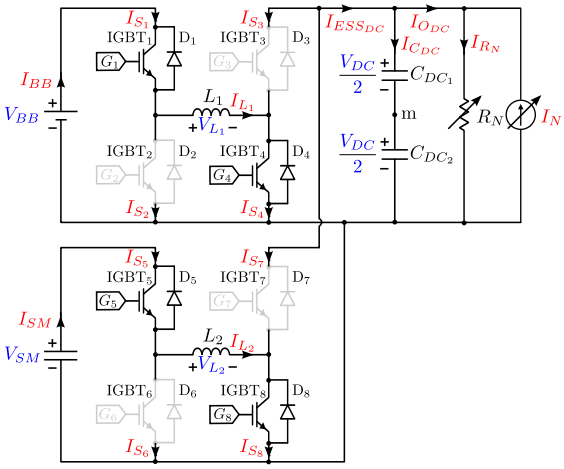
(b) State II



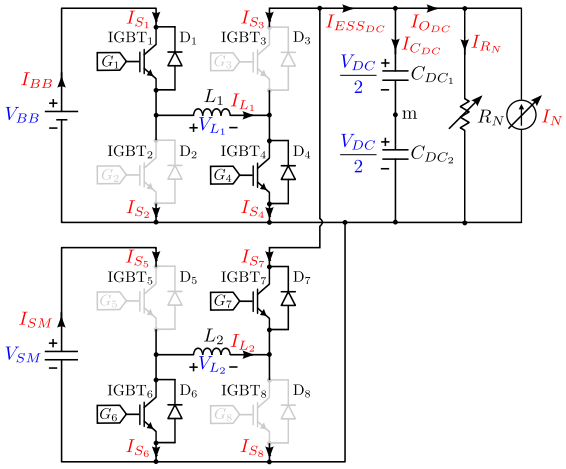
(c) State III



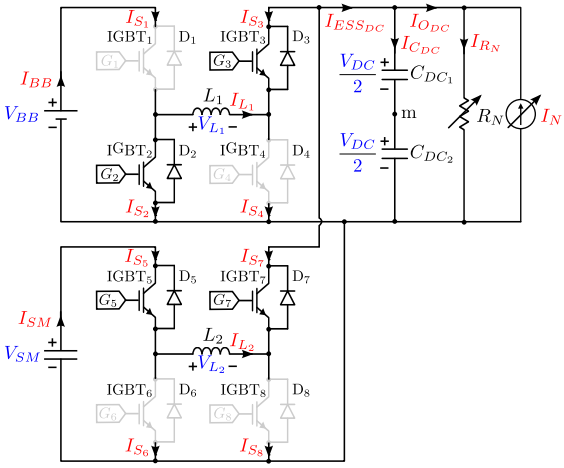
(d) State IV



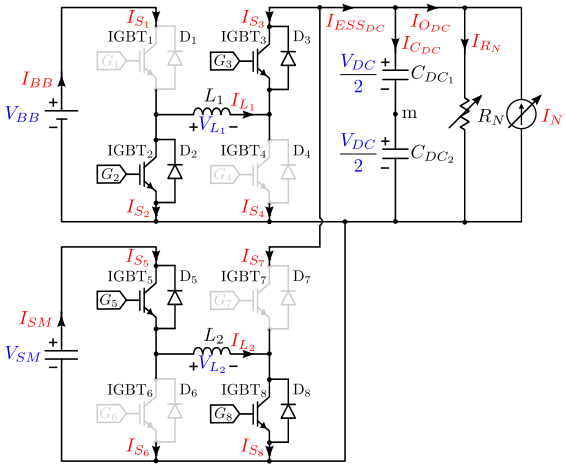
(e) State V



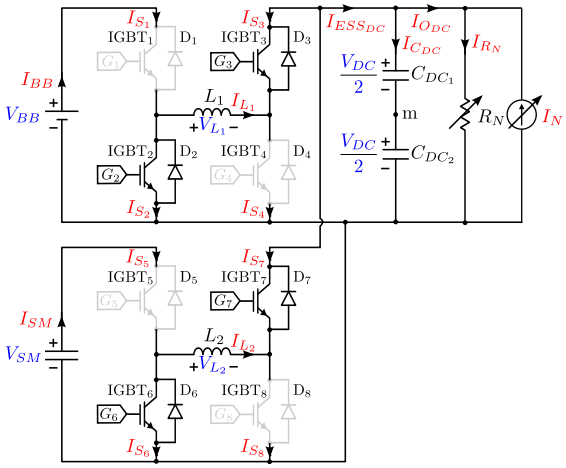
(f) State VI



(g) State VII



(h) State VIII

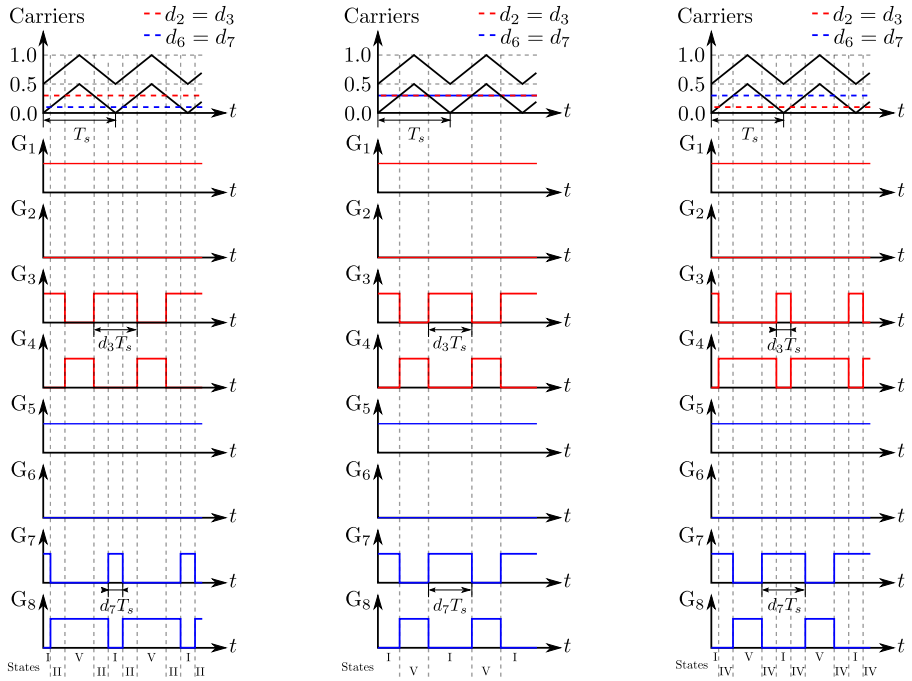


(i) State IX

Figure 5-13: The switching states of the FTPC of the two bidirectional buck-boost converters.

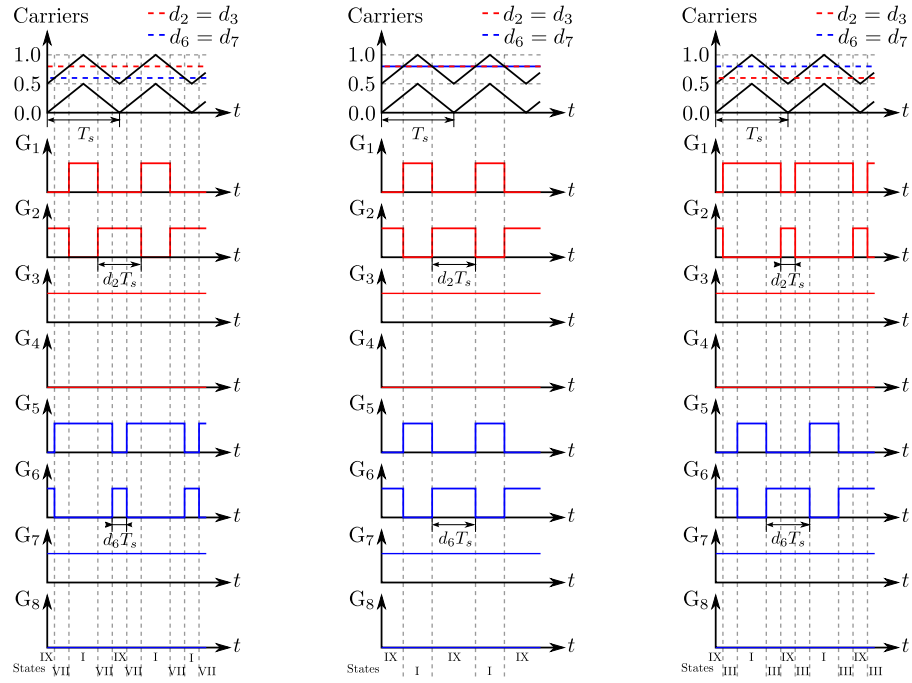
Table 5.8: The switching states of the PC of the two bidirectional buck-boost converters of the On switches during the buck and boost modes.

Cases	BB Converter	SM Converter	States	Figures
Case 1	Buck Mode ($d_2 < 0.5$)	Buck Mode ($d_6 < 0.5$)	I,II,IV,V	5-14
Case 2	Boost Mode ($d_2 > 0.5$)	Boost Mode ($d_6 > 0.5$)	I,III,VII,IX	5-15
Case 3	Buck Mode ($d_2 < 0.5$)	Boost Mode ($d_6 > 0.5$)	I,III,IV,VI	5-16
Case 4	Boost Mode ($d_2 > 0.5$)	Buck Mode ($d_6 < 0.5$)	I,II,VII,VIII	5-17



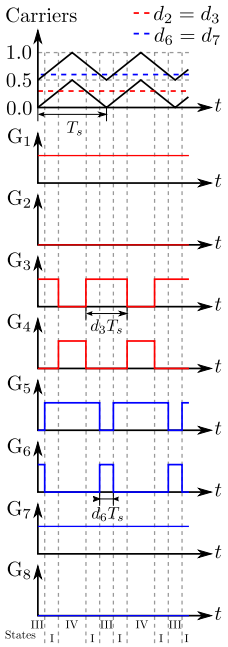
(a) $d_2 > d_6$ (b) $d_2 = d_6$ (c) $d_2 < d_6$

Figure 5-14: Both the BB and the SM converters are operating in the buck mode.

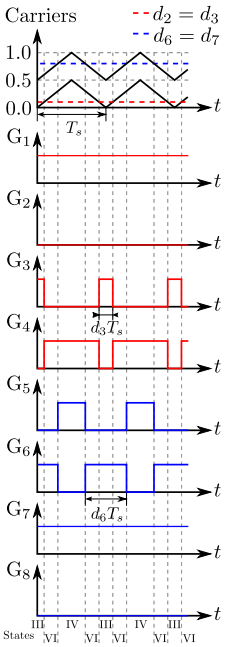


(a) $d_2 > d_6$ (b) $d_2 = d_6$ (c) $d_2 < d_6$

Figure 5-15: Both the BB and the SM converters are operating in the boost mode.

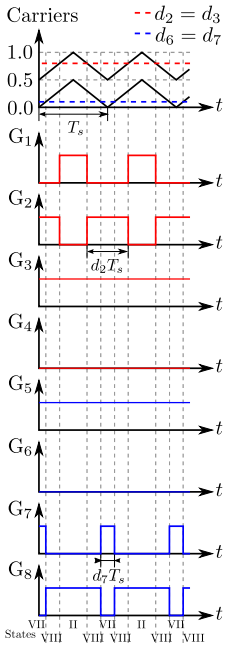


(a) $d_2 > d_6 - 0.5$

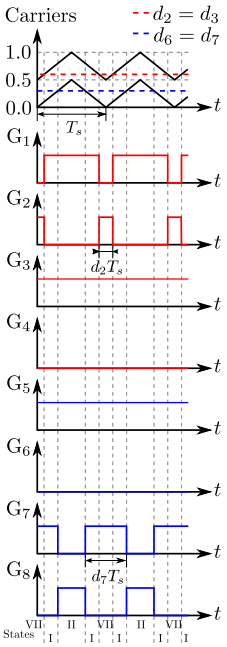


(b) $d_2 < d_6 - 0.5$

Figure 5-16: The BB converter is operating in the buck mode, and the SM is operating in the boost mode ($d_2 < d_6$).



(a) $d_2 - 0.5 > d_6$



(b) $d_2 - 0.5 < d_6$

Figure 5-17: The BB converter is operating in the boost mode, and the SM converter is operating in the buck mode ($d_2 > d_6$).

the current flowing through the inductors equal the storage device currents for both ESS currents. Also, following the assumptions made in previous chapters, in which the SM ratings are smaller than the BB ratings, it can be calculated that the duty ratio of the BB converter (d_2) is greater than the duty cycle of the SM converter (d_6) in steady state. This condition is expressed as ($d_2 > d_6$).

However, this approach has an important drawback, derived from the fact that the control actions obtained considering the buck-boost scheme do change when applied to the dual-carrier scheme, for both buck and boost operation modes. As shown in Figure 5-18, if the duty cycle (d) derived from the buck-boost, single-carrier scheme is applied directly in the dual-carrier scheme for the buck mode, the switching pattern diverges sensibly. In fact, this target duty cycle (d) should be decreased to achieve the same control action and switching pattern as in the original one-carrier scheme. Therefore, in order to correct this error, an additional block is implemented. This block modifies duty cycle (d_m) to be applied in the buck mode.

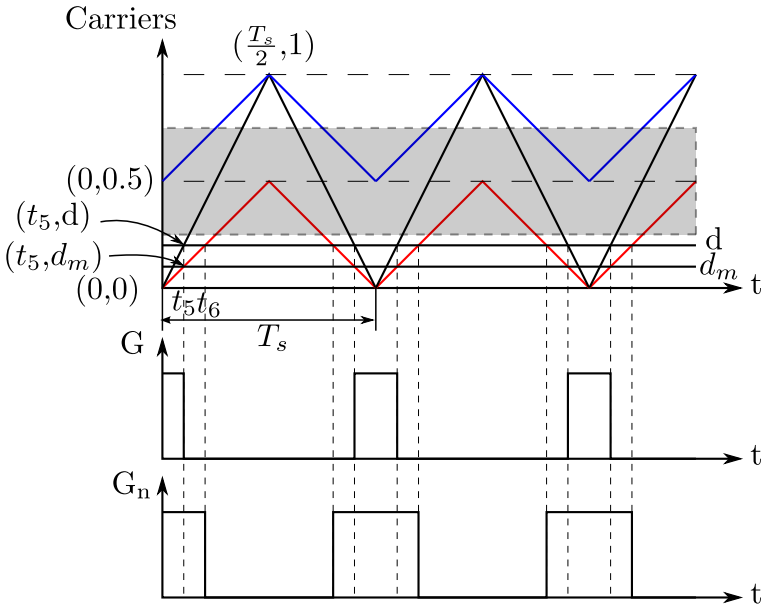


Figure 5-18: Switching scheme of the buck mode for one carrier and dual carriers.

The basis of this modification is discussed in the following lines. The initial buck-boost scheme presents the original carrier changing from 0.0 to 1.0. Looking at Figure 5-18, the instant at which the control waveform, G, toggles from *turn-on* state to *turn-off* state, (t_5),

can be calculated as a function of the duty cycle, (d), as follows:

$$\frac{d-0}{t_5-0} = \frac{1-0}{\frac{T_s}{2}-0} \tag{5.52}$$

$$\frac{d}{t_5} = \frac{2}{T_s} \tag{5.53}$$

$$t_5 = \frac{d \cdot T_s}{2} \tag{5.54}$$

In the dual-carrier buck mode, a similar calculation would yield to a different instant t_6. In order to maintain t_5 as the instant at which the control waveform, G, toggles from the *turn-on* state to the *turn-off* state, a new value of the duty cycle, d_m, will be established as:

$$\frac{d_m-0}{t_5-0} = \frac{0.5-0}{\frac{T_s}{2}-0} \tag{5.55}$$

$$\frac{d_m}{t_1} = \frac{1}{T_s} \tag{5.56}$$

$$t_5 = d_m \cdot T_s \tag{5.57}$$

where d_m is the modified duty cycle for a given switch.

From Equations (5.54) and (5.57), then the modified duty cycle (d_m) can be obtained as follows:

$$d_m \cdot T_s = \frac{d \cdot T_s}{2} \tag{5.58}$$

$$d_m = 0.5d \tag{5.59}$$

This last equation shows the conversion required to directly apply the buck-boost duty cycle in the dual-carrier scheme, for the buck operation mode. Analogously, Figure 5-19 shows the similar error obtained when considering the dual-carrier boost mode. In this case, the duty cycle (d) needs to be increased, in order to provide the same control action applied to the converter.

The new modified duty cycle (d_m) for the boost mode can be calculated by using the

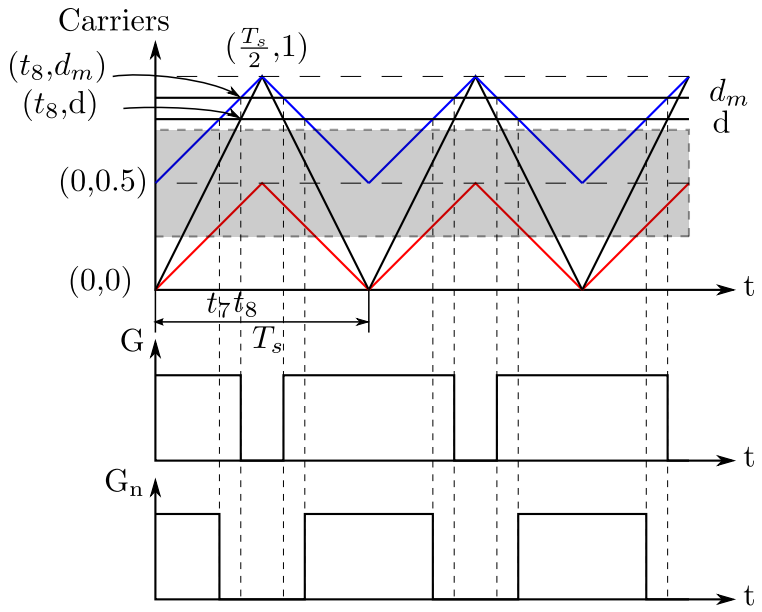


Figure 5-19: Switching scheme of the boost mode for one carrier and dual carriers.

same technique as in the previous case. But now, the target instant is t_8 in Figure 5-19:

$$t_8 = \frac{dT_s}{2} \tag{5.60}$$

Thus, t_8 can be obtained for this boost mode, considering the carrier waveform is taking values from 0.5 to 1.0:

$$\frac{d_m - 0.5}{t_8 - 0} = \frac{1 - 0.5}{\frac{T_s}{2} - 0} \tag{5.61}$$

$$\frac{d_m - 0.5}{t_8} = \frac{1}{T_s} \tag{5.62}$$

$$t_8 = (d_m - 0.5)T_s \tag{5.63}$$

And, from Equations (5.60) and (5.63), the following relationship is found:

$$(d_m - 0.5)T_s = \frac{dT_s}{2} \tag{5.64}$$

$$d_m = 0.5 + 0.5d \tag{5.65}$$

Finally, considering Equations (5.59) and (5.65), a final expression for the modified

duty cycle can be expressed as:

$$d_m = \begin{cases} 0.5d & 0 \leq d \leq 0.5 \quad \text{(buck mode)} \\ 0.5 + 0.5d & 0.5 < d \leq 1 \quad \text{(boost Mode)} \end{cases} \tag{5.66}$$

One drawback of this approach is that the operating range of the modified duty is not continuously defined:

$$\begin{cases} 0 \leq d_m \leq 0.25 & \text{buck mode} \\ 0.75 < d_m \leq 1 & \text{boost Mode} \end{cases} \tag{5.67}$$

This means that the range of values from 0.25 to 0.75 is not used. These margins are marked in Figures 5-18 and 5-19 as grey areas. Therefore the resolution of the duty is smaller than in the previous case (in particular there is 1-bit resolution lost, as the final available range is half of the original). In order to solve this problem, and in order to increase the resulting operating range (decreasing the grey areas), the original maximum and minimum values of the carriers can be varied.

5.6.0.1 Changing the Carrier Range

The idea is to establish the maximum and minimum values of the triangular waveforms at the dual-carrier scheme. From the original values (i.e., the triangular carrier ranging from 0 to 0.5 at buck mode and from 0.5 to 1.0 at boost mode), the carriers' range can be changed as in Figure 5-20. The final situation is that the triangular carrier for buck mode ranges from 0.0 to A_{c_max}, while at boost mode, the triangular carrier evolves from A_{c_min} to 1.0, where:

- A_{c_max} is the maximum limit for buck carrier,
- A_{c_min} is the minimum limit for boost carrier.

Now, for the buck mode, the instant t_5 is calculated as a function of the maximum

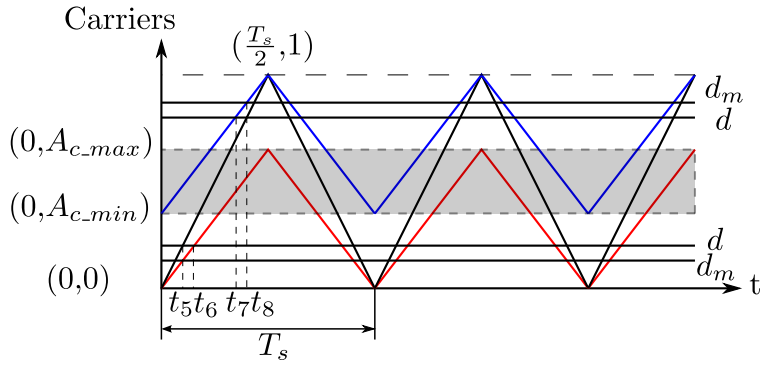


Figure 5-20: Switching scheme for one carrier and dual carriers.

carrier limit as follow:

$$\frac{d_m - 0}{t_5 - 0} = \frac{A_{c\_max} - 0}{\frac{T_s}{2} - 0} \tag{5.68}$$

$$\frac{d_m}{t_5} = \frac{2A_{c\_max}}{T_s} \tag{5.69}$$

$$t_5 = \frac{d_m \cdot T_s}{2A_{c\_max}} \tag{5.70}$$

Recalculating again the expression that relates both d and d_m, from Equations (5.54) and (5.70), then:

$$\frac{d \cdot T_s}{2} = \frac{d_m \cdot T_s}{2A_{c\_max}} \tag{5.71}$$

$$d_m = d \cdot A_{c\_max} \tag{5.72}$$

The maximum possible value for d in the original buck-boost converter that results in buck operation in the dual-carrier scheme, is, by definition:

$$d = 0.5 \tag{5.73}$$

On the other hand, the maximum possible value for the modified duty ratio, d_m, has an operational limit at the minimum of the carrier for the boost mode.

$$d_m = A_{c\_min} \tag{5.74}$$

Notice that if d_m has a greater value, the resulting pattern will present spurious triggering of the switches. Therefore, a condition that relates both limit values, for the buck case operation, can be obtained from Equations (5.72), (5.73) and (5.74):

$$A_{c\_min} = 0.5A_{c\_max} \tag{5.75}$$

A similar approach will be followed to calculate the limit operation values in the case of the boost carrier:

$$\frac{d_m - A_{c\_min}}{t_8 - 0} = \frac{1 - A_{c\_min}}{\frac{T_s}{2} - 0} \tag{5.76}$$

$$\frac{d_m - A_{c\_min}}{t_8} = \frac{2 - 2A_{c\_min}}{T_s} \tag{5.77}$$

$$t_8 = \frac{T_s(d_m - A_{c\_min})}{2 - 2A_{c\_min}} \tag{5.78}$$

From Equations (5.60) and (5.78), the modified duty cycle is obtained as follows:

$$\frac{dT_s}{2} = \frac{T_s(d_m - A_{c\_min})}{2 - 2A_{c\_min}} \tag{5.79}$$

$$d = \frac{d_m - A_{c\_min}}{1 - A_{c\_min}} \tag{5.80}$$

$$d_m = A_{c\_min} + d(1 - A_{c\_min}) \tag{5.81}$$

Again, the minimum possible value for d for the boost mode is as Equation (5.73). The limit for d_m can be calculated:

$$d_m = A_{c\_max} \tag{5.82}$$

From the previous relationships, substituting in Equation (5.81), yields to:

$$A_{c\_max} = A_{c\_min} + 0.5(1 - A_{c\_min}) \tag{5.83}$$

$$A_{c\_max} = 0.5A_{c\_min} + 0.5 \tag{5.84}$$

Substituting for A_{c_min} from Equations (5.75) in (5.84), yields to:

$$A_{c\_max} = 0.5 \times 0.5A_{c\_max} + 0.5 \tag{5.85}$$

$$0.75A_{c\_max} = 0.5 \tag{5.86}$$

$$A_{c\_max} = \frac{2}{3} \tag{5.87}$$

Then, from equation (5.75), the minimum limit for the buck carrier is obtained as:

$$A_{c\_min} = \frac{1}{3} \tag{5.88}$$

Finally, from Equations (5.72), (5.81), (5.87) and (5.88), the modified duty cycle (d_m) is found to be:

$$d_m = \begin{cases} \frac{2}{3}d & 0 \leq d \leq 0.5 \quad \text{buck mode} \\ \frac{1}{3} + \frac{2}{3}d & 0.5 < d \leq 1 \quad \text{boost mode} \end{cases} \tag{5.89}$$

The new operating range of the modified duty is given by:

$$\begin{cases} 0 \leq d_m \leq \frac{1}{3} & \text{buck mode} \\ \frac{2}{3} < d_m \leq 1 & \text{boost mode} \end{cases} \tag{5.90}$$

The final implementation of the modified duty cycle scheme, considering the two carriers calculated with this approach are depicted in Figure 5-21.

Figure 5-21 shows how the duty cycle modification depends on the buck-boost duty cycle in steady state, as taken from Table 5.5:

$$d_{BB\_ss} = \frac{V_{BB\_meas}}{V_{BB\_meas} + V_{DC_meas}} \tag{5.91}$$

$$d_{SM\_ss} = \frac{V_{SM\_meas}}{V_{SM\_meas} + V_{DC_meas}} \tag{5.92}$$

As it can be seen, the inductor current reference of the BB converter ($I_{L_{1\_ref}}$) changes depending on the mode of operation (buck or boost). In buck mode, the inductor current

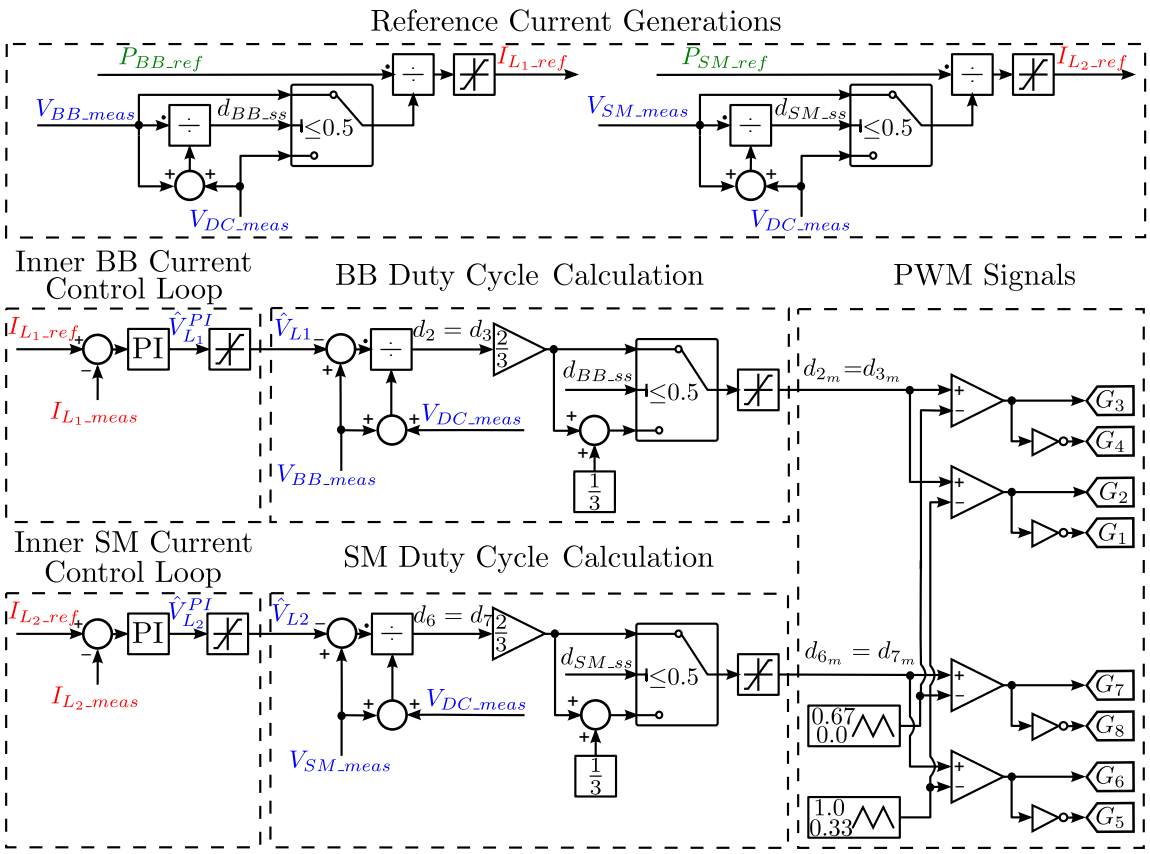


Figure 5-21: Inner current controllers scheme for the two bidirectional buck-boost converters with modified carrier range technique.

reference is equal to the BB device current reference. However, for boost operation mode, this inductor current reference equals the output current of the BB converter at the DC side. This can be summarized as:

$$I_{L_1\_ref} = \begin{cases} \dfrac{P_{BB\_ref}}{V_{BB\_meas}} & d_{BB\_ss} \leq 0.5 \quad \text{(Buck mode)} \\ \dfrac{P_{BB\_ref}}{V_{DC\_meas}} & d_{BB\_ss} > 0.5 \quad \text{(Boost mode} \end{cases} \tag{5.93}$$

In a similar manner, the inductor current reference in the SM converter ($I_{L_{2\_ref}}$) can be expressed as:

$$I_{L_2\_ref} = \begin{cases} \dfrac{P_{SM\_ref}}{V_{SM\_meas}} & d_{SM\_ss} \leq 0.5 \quad \text{(Buck mode)} \\ \dfrac{P_{SM\_ref}}{V_{DC\_meas}} & d_{SM\_ss} > 0.5 \quad \text{(Boost mode)} \end{cases} \tag{5.94}$$

The modification of the ranges of the carriers results in some increase of the resolution against the original implementation. However, there is still a loss in the achievable accuracy. Figure 5-22 shows the static voltage gain ($\frac{V_{BB}}{V_{DC}}$) as a function of the duty cycle, in the buck-boost converter, for every operation scheme. It is noticed from Figure 5-22 that the gain for the buck operation (green line) reaches 1.0 at a duty ratio of 0.33; however, the gain for the boost scheme (magenta line) surpasses 1.0 from the duty ratio of 0.66. This yields to a discontinuity in the duty cycle if using the two-carrier scheme, compared to the original modulation scheme with one carrier only. In order to keep the original PWM resolution, and avoiding this discontinuity, another approach is followed, that consists of using a different *Duty Cycle Calculation Block* for either the buck and the boost modes. This analysis is valid for the other buck-boost converter connected to the SM.

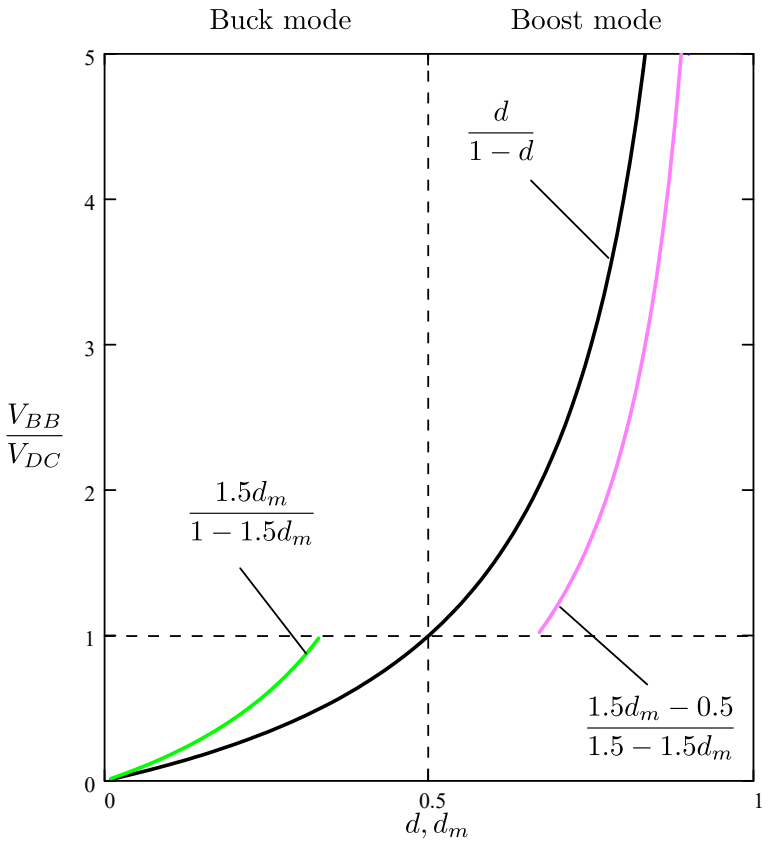


Figure 5-22: The gain ($\frac{V_{BB}}{V_{DC}}$) as a function of the duty.

5.6.0.2 Changing the Duty Cycle Calculation

Again, this approach consists of using two triangular carriers for boost mode and buck mode, as in the previous case. However, in this strategy, the control action is going to be tailored for the operation case, and therefore no additional adjustment on the duty cycle needs to be undertaken. The duty cycles d_2 and d_6, as defined in Table 5.5, are going to be applied for the buck mode;

$$d_3 = \frac{V_{BB\_meas} - \hat{V_{L_1}}}{V_{DC\_meas}} \tag{5.95}$$

$$d_7 = \frac{V_{SM\_meas} - \hat{V_{L_2}}}{V_{DC\_meas}} \tag{5.96}$$

and for the boost mode, the following relationships can be found:

$$d_2 = \frac{V_{BB\_meas} - V_{DC\_meas} - \hat{V_{L_1}}}{V_{BB\_meas}} \tag{5.97}$$

$$d_6 = \frac{V_{SM\_meas} - V_{DC\_meas} - \hat{V_{L_2}}}{V_{SM\_meas}} \tag{5.98}$$

And from this expression, the value that actually is going to be compared to the dual-carrier scheme, defined in Equation (5.66), needs to be calculated. Notice how in this case, this transformation does not imply a loss in the resolution as the available duty ratio margin is again the full 0.0-1.0 region:

$$d_{2_m} = d_{3_m} \begin{cases} 0.5\big(\frac{V_{BB\_meas} - \hat{V}_{L_1}}{V_{DC\_meas}}\big) & 0 \leq \frac{V_{BB\_meas}}{V_{BB\_meas}+V_{DC\_meas}} \leq 0.5 \\ 0.5 + 0.5\big(\frac{V_{BB\_meas} - \hat{V}_{L_1} - V_{DC\_meas}}{V_{DC\_meas}}\big) & 0.5 < \frac{V_{BB\_meas}}{V_{BB\_meas}+V_{DC\_meas}} \leq 1 \end{cases} \tag{5.99}$$

$$d_{6_m} = d_{7_m} \begin{cases} 0.5\frac{V_{SM\_meas} - \hat{V}_{L_1}}{V_{DC\_meas}} & 0 \leq \frac{V_{SM\_meas}}{V_{SM\_meas}+V_{DC\_meas}} \leq 0.5 \\ 0.5 + 0.5\frac{V_{SM\_meas} - \hat{V}_{L_2} - V_{DC\_meas}}{V_{DC\_meas}} & 0.5 < \frac{V_{SM\_meas}}{V_{SM\_meas}+V_{DC\_meas}} \leq 1 \end{cases} \tag{5.100}$$

This yields to a final modification in the *Duty Cycle Calculation Blocks*, as it is depicted in figure 5-23.

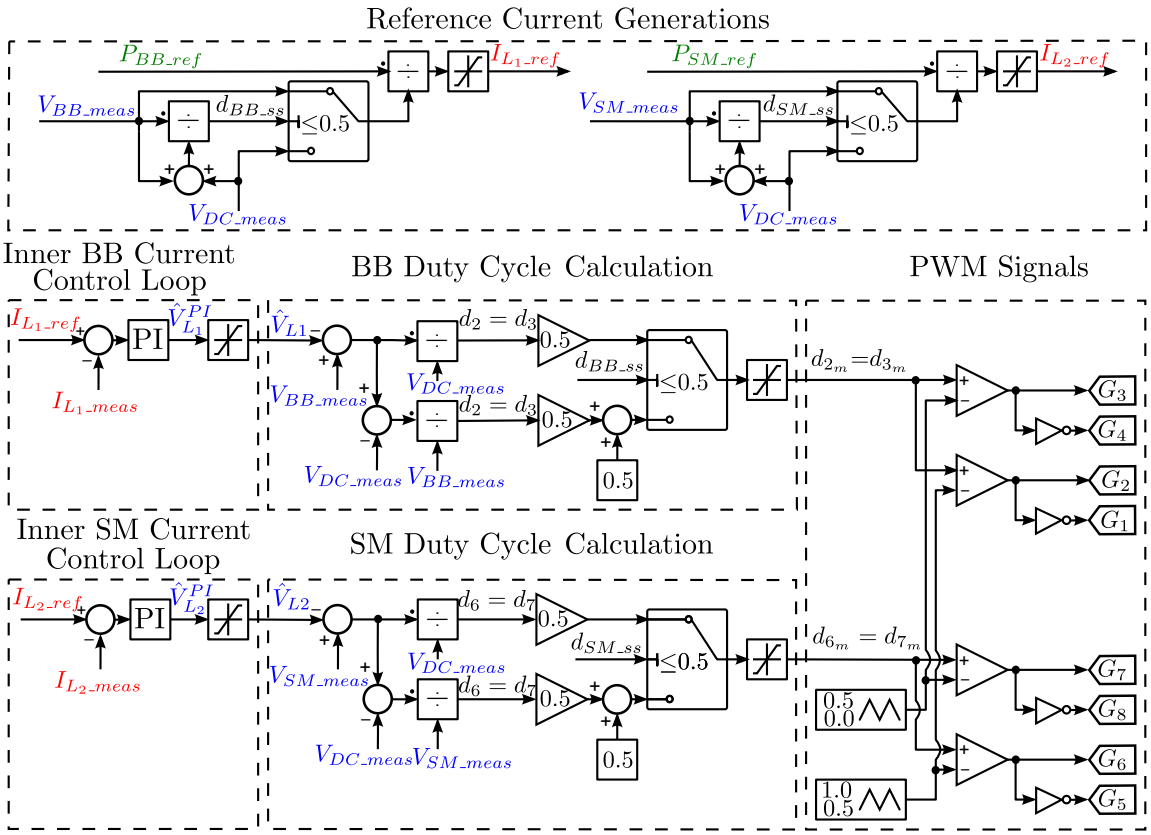


Figure 5-23: Inner current controllers scheme for the two bidirectional buck-boost converters with changing duty calculation technique.

This is the final control scheme that is going to be implemented in the control of the converter. Figure 5-24 shows the continuity of the duty cycle by using this proposed approach. The gain in buck mode (red line) reaches unity at 0.5, and the gain in buck mode (red line) surpasses unity exactly at 0.5.

5.7 Conclusions

In this chapter, a FTPC of two bidirectional buck-boost converters, with a proposal for a dual-carrier switching pattern and for a specific control scheme (by changing the *Duty Cycle Calculation Blocks*) has been carried out. This scheme provides a fault ride-through capability once the fault is over, for the whole HESS, operating at any condition. In Chapters 7 and 8, simulated and experimental demonstrations of the control schemes of this topology are presented to demonstrate the performance. Before this demonstrations,

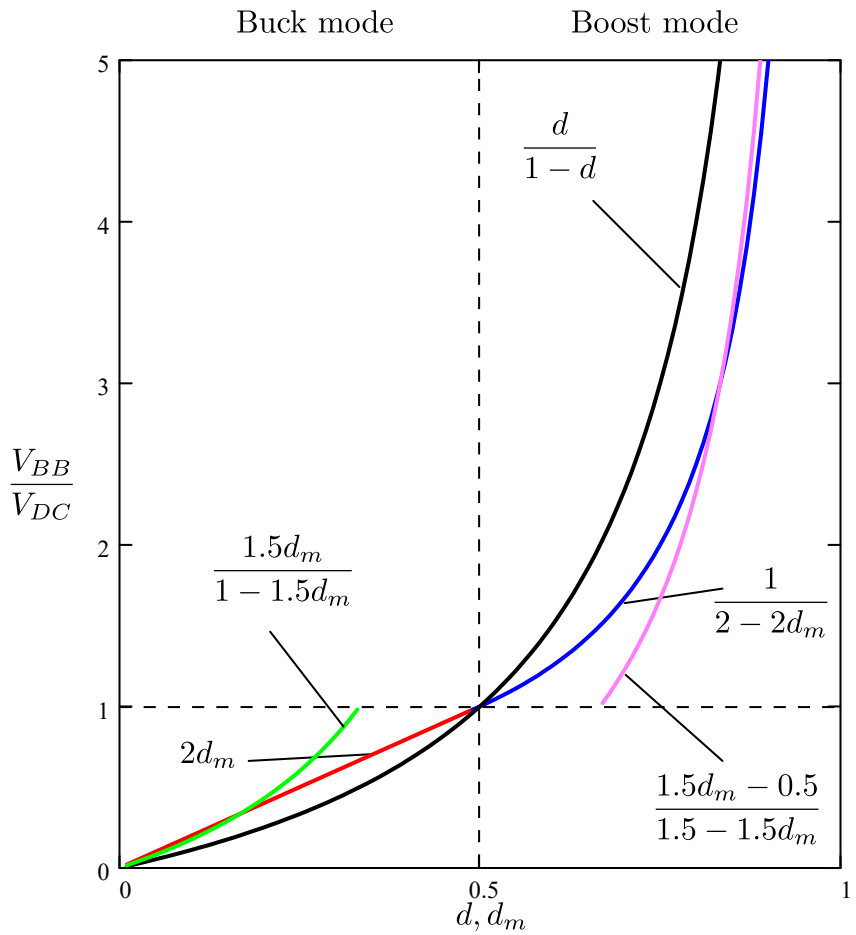


Figure 5-24: Static voltage gain of the BB converter as a function of the duty, for all the control strategies evaluated.

the following Chapter 6 presents the derivation of the detailed design parameters of the HESS converter topologies, for every proposed control schemes studied so far.

Chapter 6

Design Procedure

Contents

6.1 Introduction

This chapter considers a design procedure for the baseline case of the study. It covers the sizing and definition of all the characteristic parameters and magnitudes of the physical system, such as voltage, current, power and energy ratings, impedances of inductors and capacitors, switching frequencies, etc. It also defines a procedure for designing the control parameters in the management strategy, such as the signal conditioning blocks, the bandwidth of the control systems, coordination strategies, etc. This definition is done for the operation modes and constraints considered in the previous chapters. These parameters will be used in the forthcoming simulation and experimental chapters in order to compare the different proposed topologies and control schemes.

6.2 Definition of the System

Firstly, the main power and voltage ratings of the DC microgrid are going to be defined. Generally speaking, the power range in microgrids might change from some megawatts down to few kilowatts. In this case, the target nominal power level of the system is balanced towards the lower range of the scale, as justified in the previous chapters for microgrid and nanogrid applications. It also allows for a reasonable size of the laboratory prototypes, suitable for being efficiently managed. Considering typical figures for small users, a target level of the nanogrid of 10 kW is thus selected.

The power values that the HESS can provide are going to be different to this rated value for the whole microgrid. This fact adds generality to the system performance, enabling the study of additional features such as peak-shaving, the detachment of non-critical loads strategies, etc. In this sense, the transient peak power capability to the system is limited to 75% of the total rated load power, aimed to dimension the power-support device of the ESS. The long-term, steady-state islanding power capability of the system is, though, dimensioned to be 50% of the rated load power. About the energy sizing, it is assumed that the system must be able to provide an energy equivalent to that of the rated power during one hour, thus providing a rated energy value of 10 kWh.

Finally, the DC bus voltage ratings need to be considered as to include most of the possible grid interfaces that might be found in real applications. Considering both single-phase and three-phase voltage ratings at the PCC for European grid levels (230 V_{rms}/50 Hz for single-phase, and 400 V_{rms}/50 Hz line-to-line for three-phase systems), then the range of the DC bus voltage must cover from 400 V to 700 V. The following table summarizes the basic requirements of the system.

Table 6.1: Base parameters of the HESS design.

Parameter	Symbol	Value	Unit
Rated microgrid power	P_{MG}	10	kW
Transient peak power supported by the HESS	P_{ESS_max}	7.5	kW
Sustained power supported by the HESS (islanding mode)	P_{ESS_sus}	5	kW
Energy stored at the ESS	E_{ESS}	10	kWh
Minimum Output power	P_{O_min}	-10	kW
Maximum Output power	P_{O_max}	10	kW
Minimum DC bus voltage	V_{DC_min}	400	V
Maximum DC bus voltage	V_{DC_max}	700	V

Parting from the information in the previous table, the individual blocks of the system can now be sized and designed.

6.3 Energy Storage System

The first block to be defined is the ESS subsystem. As discussed in the previous chapters, there are two individual ESSs devices, arranged in a complementary scheme. The ESS used in the designed DC microgrid is BB and SM.

6.3.1 Battery Bank

The target electrochemical BB is going to be an assembly of a number of specific commercial modules. In this case, the base module is the 48 V module from CEGASA PORTABLE ENERGY. The parameters of this module are shown in Table 6.2. This module is based on the Li-Ion technology. In order to optimize the battery lifetime, it is recommended to operate between 20% and 90% of the SoC. It is noted from the Table 6.2 that the discharging current is greater than charging current due to the chemical processes involved. This means that in practice the power delivered is greater than the power absorbed.

Table 6.2: Parameters of the BB.

Parameter	Symbol	Value	Unit
Nominal voltage	V_{BB}	48	V
Minimum voltage at SOC 0%	V_{BB_min}	37.5	V
Maximum voltage at SOC 100%	V_{BB_max}	54.75	V
Minimum current (Maximum charging current) (1C)	I_{BB_min}	-48	A
Maximum current (Maximum discharging current) (3C)	I_{BB_max}	144	A
Rated continuous charging current (0.5C)	I_{BB}	-24	A
Rated continuous discharging current (1C)	I_{BB}	48	A
Minimum power (Maximum charging power)	P_{BB_min}	-2.628	kW
Maximum power (Maximum discharging power)	P_{BB_max}	6.912	kW
Nominal energy storage	E_{BB}	2.3	kWh
Nominal capacity	Q_{BB}	42	Ah
Minimum SoC	SOC_{BB_min}	20	%
Maximum SoC	SOC_{BB_max}	90	%

By carefully looking at the parameters in the previous table, some considerations are

taken into account:

- In order to attain the energy requirements of the BB as expressed in Table 6.1, a number of 5 modules must be used. Thus, a commercial assembly 5 modules (ROOK 48×5 battery) will be used. This yields to an increase of the voltage levels of the BB, avoiding the problem of the voltage mismatch between the DC bus and the BB.
- This initial assumption implicitly considers that the contribution of the energy support of the alternate storage system in the hybrid setup, i.e., the SM, will be neglected.
- SoC around 50% will be considered which give a margin for the BB to provide or absorb power.
- As the SM will provide the peak transient requirements, the continuous current of the BB will be considered.
- The maximum battery current is the maximum discharging current. Also, a symmetric performance is required, and therefore the maximum discharge current is considered the same as the maximum charging current. For the convention stated in previous chapters, then this maximum charge current it is going to be noted as the minimum battery current.

Table 6.3 shows the new parameters of the BB taking into account all the previous consideration and these parameters will be considered for the control and the protection devices.

As it can be seen from Tables 6.3 and 6.1, this setup also fulfills the power requirements for the long-term energy system; therefore, there is no need to parallel additional battery setups to increase the current of the storage element.

6.3.2 Supercapacitor Module

Similarly, the basic building block for the SM device is firstly defined. The SM selected for this design is the BMOD0165 P048 C01 from Maxwell Technologies. The main parameters are given in Table 6.4. The SM can operate theoretically between 0% and 100%

Table 6.3: Parameters of the designed BB.

Parameter	Symbol	Value	Unit
Nominal voltage	V_{BB}	240	V
Minimum voltage at SOC 0%	V_{BB_min}	187.5	V
Maximum voltage at SOC 100%	V_{BB_max}	273.75	V
Initial voltage at SoC 50%	V_{BB}	260	V
Minimum continuous current (Maximum charging current) (0.5C)	I_{BB_min}	-24	A
Maximum continuous current (Maximum discharging current) (1C)	I_{BB_max}	24	A
Minimum power (Maximum charging power)	P_{BB_min}	-6.57	kW
Maximum power (Maximum charging power)	P_{BB_max}	6.57	kW
Nominal energy storage	E_{BB}	11.5	kWh
Nominal capacity	Q_{BB}	42	Ah
Minimum SoC	SOC_{BB_min}	20	%
Maximum SoC	SOC_{BB_max}	90	%

of the SoC. This means an operation range from rated voltage to zero volts. However, From (2.1), it is possible to utilize 75% of the available energy if the SM voltage reaches half the rated value (approximately 50% of the SoC).

Table 6.4: Parameters of the SM.

Parameter	Symbol	Value	Unit
Rated voltage	V_{SM}	48	V
Minimum voltage	V_{SM_min}	0	V
Maximum voltage	V_{SM_max}	51	V
Minimum current (Maximum charging current)	I_{SM_min}	-1900	A
Maximum current (Maximum discharging current)	I_{SM_max}	1900	A
Minimum power (Maximum charging power)	P_{SM_min}	-96.9	kW
Maximum power (Maximum discharging power)	P_{SM_max}	96.9	kW
Energy storage	E_{SM}	53	Wh
Rated capacitance	C_{SM}	165	F
Maximum DC ESR	ESR_{DC}	6	mΩ
Minimum SoC	SOC_{SM_min}	0	%
Maximum SoC	SOC_{SM_max}	100	%
Number of cells	N_{SM}	18	-

At the HESS, the SM is designed in terms of the power requirements, rather than regarding the stored energy. On the other hand, the discharge and charge of the SM can occur at the same rate because of the energy storage mechanism of the SM is not a chemical reaction. This yields to an equal theoretical discharging and charging power levels. Also, as expected, the rated power of the SM is greater than the power of the BB, as the SM is providing or absorbing the transient peak power.

However, the final output current extracted from the SM is going to be limited, in this particular case, by the absolute maximum ratings of the selected IGBT. This value is equal to 75 A, as it is justified in the Subsection 6.4.1. This results in a significantly smaller current than the one depicted in the previous table. This consideration has been made due only by practical implementation reasons, as these are the available switches and SM parts at the laboratory premises where the validations have been carried out. This situation causes that the effective values for the current and power values in the SM are equal to these values in Table 6.5.

Table 6.5: Effective current and power parameters of the SM.

Parameter	Symbol	Value	Unit
Minimum effective current (Maximum effective charging current)	I_{SM_min}	-75	A
Maximum effective current (Maximum effective discharging current)	I_{SM_max}	75	A
Minimum effective power (Maximum effective charging power)	P_{SM_min}	-3.825	kW
Maximum effective power (Maximum effective discharging power)	P_{SM_max}	3.825	kW

With these effective values for the SM storage device, and analogously to the case of the BB device, the following consideration need to be carried out:

- In order to guarantee the power requirements specified for the HESS system in Table 6.1, an assembly of 2 modules is required.
- The modules will be connected in series, thus increasing the device voltage.

- As mentioned, the current of the SM assembly during charging and discharging will be limited to the current that flows through the IGBT and the anti-parallel diode. However, the power delivered or absorbed from the SM is still greater than the power supplied or absorbed from the BB.
- The minimum voltage will be above 10V for each SM in order to not fully discharge the SM.
- SoC around 75% is considered as nominal voltage, in order to maximize the symmetric energy availability.

With these considerations, the final design parameters for the SM device are presented in Table 6.6.

Table 6.6: Parameters of the designed SM.

Parameter	Symbol	Value	Unit
Rated voltage	V_{SM}	96	V
Minimum voltage	V_{SM_min}	19.2	V
Maximum voltage	V_{SM_max}	102	V
Initial voltage at SoC 75%	V_{SM}	80	V
Minimum current (Maximum charging current)	I_{SM_min}	-75	A
Maximum current (Maximum discharging current)	I_{SM_max}	75	A
Minimum power (Maximum charging power)	P_{SM_min}	-7.65	kW
Maximum power (Maximum discharging power)	P_{SM_max}	7.65	kW
Energy storage	E_{SM}	106	Wh
Rated capacitance	C_{SM}	82.5	F
Maximum DC ESR	ESR_{DC}	12	mΩ
Minimum SoC	SOC_{SM_min}	20	%
Maximum SoC	SOC_{SM_max}	100	%
Number of cells	N_{SM}	36	-

6.4 DC/DC Converters and AC/DC Converter

For simplicity in the design, the same parameters for all the switches in the power topologies are going to be selected. This allows for a common design of the PC and the

SPC of the two bidirectional buck converters, the FTPC of the two bidirectional buck-boost converters and the three-phase VSI. The main reason for this scheme is that commercial H-bridge / three-phase VSI modules of converters can be used for the considered topologies, thus simplifying the implementation and the construction stages. In addition, for simplicity, but also for economic constraints, the inductors and the DC bus capacitors used in the converters are also going to be the same, for all the converter topologies implemented.

6.4.1 Switches

The switch module is 2MBI200HH-120-50 from Fuji Electric, and its parameters are in Table 6.7. This module has two IGBTs, with an anti-parallel diode with each IGBT, representing one leg of the converter. The emitter of the first IGBT is connected to the collector of the second IGBT. One IGBT module can form a bidirectional buck converter. Two IGBT modules can form a bidirectional buck-boost converter, while three IGBT modules can form a three-phase VSI. The SPC converter is also easily implemented with this modular device. It is noticed from Table 6.7 that the current flowing through the anti-parallel diode is less than the current flowing the IGBT. As the currents from the ESS will flow through the IGBT and the diode, the current will be limited to the current values of the diode.

Table 6.7: Parameters of the IGBT module.

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CE}	1200	V
Gate-emitter voltage	V_{GE}	$\pm$20	V
Collector continuous current (Current through IGBT)	I_c (25°C)	300	A
	I_c (80°C)	200	A
Maximum collector pulse current (Current through IGBT)	I_{c_max} (25°C)	600	A
	I_{c_max} (80°C)	400	A
Collector continuous current (Current through diode)	I_c (25°C)	-75	A
Minimum collector pulse current (Current through diode)	I_{c_max} (25°C)	-150	A

6.4.2 The Inductors and the DC Bus Capacitors

This section shows the basic design procedure of the inductors and the DC bus capacitor for the baseline case, i.e., the PC scheme. It aims at defining the main parameters of the power topology. The BB converter is designed in a first stage. The design must ensure that the converters can operate within a given range for the operational voltage values at every port of the converter. These design limits for the voltages of BB (V_{BB}) and SM (V_{SM}) are expressed in Table 6.3 and Table 6.6. However, the limits for the DC bus voltage (V_{DC}) and the output power (P_O) is shown in Table 6.1.

6.4.2.1 Calculation of the Inductance

The inductance of the inductor is calculated as follows [141]:

$$V_L = L\frac{dI_L}{dt} \tag{6.1}$$

$$V_L = L\frac{\Delta I_L}{\Delta T} \tag{6.2}$$

$$L = \frac{V_L \cdot \Delta T}{\Delta I_L} \tag{6.3}$$

where:

- V_L is the inductor's voltage in Volts,
- L is the inductance of the inductor in Henries,
- $\frac{dI_L}{dt}$ is the rate of inductor current change in Amps/Sec,
- ΔI_L is the current ripple of the inductor in Amps,
- ΔT is the time duration in Secs.

The inductance of the inductor can be calculated during the *turn-on* or *turn-off* of the switches. At steady state, the duty of S_1 is greater than the duty cycle of S_3, then the states I, II and III will occur (Figure 6-1).

From Equation (3.51), the inductor voltage is as follows:

$$V_{L_1} = V_{BB} - V_{CE_2} \tag{6.4}$$

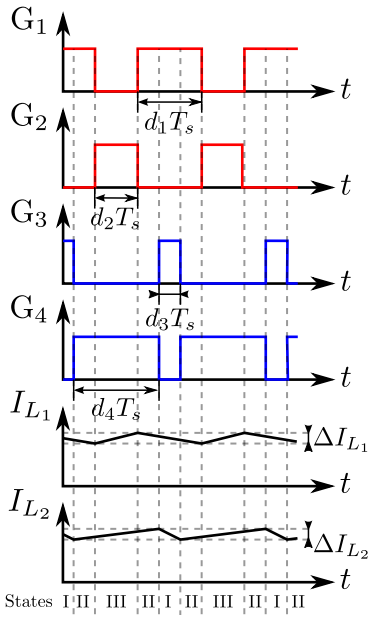


Figure 6-1: Switching states and the inductors' currents of the PC of two bidirectional buck converters.

During T_{on_2}, considering state III (Figure 3-5c), the switch S_2 is closed so the $V_{CE_2} = 0$ and $\Delta T = T_{on\_2} = d_2 \cdot T_s = \dfrac{(1 - d_1)}{f_s}$.

The value of the inductance of the buck converter, given from the general Equations of this topology in the continuous operation mode, is provided by [141]:

$$L_1 = \frac{V_{BB}\left(1 - \dfrac{V_{BB}}{V_{DC}}\right)}{f_s \cdot \Delta I_{L_1}} \tag{6.5}$$

where ΔI_{L_1} is the current ripple of the inductor connected with the BB (L_1) in Amps.

Thus, the value of the inductor depends on the target current ripple for each application, as well as on the voltage levels at both the BB and the DC bus. About this HF current ripple, it must be noticed that this inductor is directly connected in series with the BB. Therefore, the inductor ripple is the HF current ripple through the BB. Given that the existing literature states that the HF current ripple might affect the SoH of the battery in the long term [158, 159], this parameter is kept relatively low to ensure both a reliable design and proper operation of the converter. This implies a relatively large inductance value [93]; however, this is not an understood as a concern in the design, given that no major weight

or size constraints are envisaged for the static application of power support in microgrids. The target value for this parameter is:

$$\delta I_{L_1} < 0.02 \tag{6.6}$$

$$\Delta I_{L_1} = \delta I_{L_1} \cdot I_{L_{1\_avg}} = \delta I_{L_1} \left(\frac{P_{O\_max}}{V_{BB}} \right) \tag{6.7}$$

where:

- δI_{L_1} is the p.u. value of the peak to peak current ripple at the inductor connected with the BB L_1,
- $I_{L_{1\_avg}}$ is the average value of the current through inductor connected with the BB (L_1) in Amps,
- P_{O_max} is the maximum active output power delivered to the rest of the microgrid in Watts.

Combining this parameter with the worst-case scenario for the input voltage magnitudes involved (i.e., maximum values for the DC bus voltage V_{DC_max} and BB voltage V_{BB_max}), the value for inductor L_1 can be calculated:

$$L_1 = \frac{V_{BB\_max} \left(1 - \frac{V_{BB\_max}}{V_{DC\_max}} \right)}{f_s \cdot \delta I_{L_1} \left(\frac{P_{O\_max}}{V_{BB\_max}} \right)} \tag{6.8}$$

$$L_1 = \frac{273.75 \left(1 - \frac{273.75}{700} \right)}{20000 \times 0.02 \times \frac{10000}{273.75}} \tag{6.9}$$

$$L_1 > 11.408 mH \tag{6.10}$$

In order to ensure some safety margin, a slightly large value has been selected for L_1. The final value chosen is shown in Table 6.8

The inductor connected to SM should be less than the inductor connected to the BB to charge and discharge quickly in order to can provide or absorb the peak transient current.

From Equation (3.51), the inductor voltage is as follows:

$$V_{L_2} = V_{SM} - V_{CE_4} \tag{6.11}$$

Table 6.8: Parameters of the inductors.

Parameter	Symbol	Value	Unit
Inductance of the inductor connected with the BB	L_1	14.36	mH
Parasitic resistance of the inductor connected with the BB	R_1	0.34	Ω
Inductance of the inductor connected with the SM	L_2	3.59	mH
Parasitic resistance of the inductor connected with the SM	R_2	0.085	Ω
Inductance of the filter connected to the grid	L_f	7.18	mH
Parasitic resistance of the filter connected to the grid	R_f	0.17	Ω

During T_{on_4}, considering state II (Figure 3-5b) and state III (Figure 3-5c), the switch S_4 is closed so the $V_{CE_4} = 0$ and $\Delta T = T_{on\_4} = T_s \cdot d_4 = \dfrac{1 - d_3}{f_s}$. For inductor connected with the SM (L_2), the same formulation is used:

$$L_2 = \frac{V_{SM}\left(1 - \dfrac{V_{SM}}{V_{DC}}\right)}{f_s \cdot \Delta I_{L_2}} \tag{6.12}$$

where ΔI_{L_2} is the current ripple of the inductor connected with the SM (L_2) in Amps.

However, for the SM case, it must be noticed how the voltage values at the storage device are significantly smaller than in the BB case, yielding too much higher current levels. The target per-unit current ripple level is kept the same as follows:

$$\delta I_{L_2} < 0.02 \tag{6.13}$$

$$\Delta I_{L_2} = \delta I_{L_2} \cdot I_{L_2\_avg} = \delta I_{L_2}\left(\frac{P_{O\_max}}{V_{SM}}\right) \tag{6.14}$$

where

- δI_{L_2} is the p.u. value of the peak to peak current ripple at the inductor connected with the SM L_2,
- $I_{L_2\_avg}$ is the average value of the current through inductor connected with the SM (L_2) in Amps.

The HF losses in the magnetic device are a function of the square of the RMS value of the HF current harmonics, being the fundamental one of the switching frequency. Hence,

given that the average current flowing through the SM is high, relatively large HF current ripples imply high magnetic losses. For the worst-case scenario (i.e., maximum values for the DC bus voltage (V_{DC_max}) and SM voltage (V_{SM_max}), the obtained value for the capacitance can be calculated:

$$L_2 = \frac{V_{SM\_max}\left(1 - \frac{V_{SM\_max}}{V_{DC\_max}}\right)}{f_s \cdot \delta I_{L_2}\left(\frac{P_{O\_max}}{V_{SM\_max}}\right)} \tag{6.15}$$

$$L_2 = \frac{102\left(1 - \frac{102}{700}\right)}{20000 \times 0.02 \times \frac{10000}{102}} \tag{6.16}$$

$$L_2 > 2.2222mH \tag{6.17}$$

As a final remark, a slightly larger value has been selected, to ensure a safety margin in the design. The value at Table 6.8 is finally selected. The inductors of the filter connected to the grid are commercial inductors, and their parameters are presented in Table 6.8.

6.4.2.2 Calculation of the DC Bus Capacitor

The capacitance of the DC bus is calculated considering the following equation [141]:

$$I_{DC} = C_{DC}\frac{dV_{DC}}{dt} \tag{6.18}$$

$$I_{DC} = C_{DC}\frac{\Delta V_{DC}}{\Delta T} \tag{6.19}$$

$$C_{DC} = I_{DC}\frac{\Delta T}{\Delta V_{DC}} \tag{6.20}$$

where:

- $\frac{dV_{DC}}{dt}$ is the rate of DC bus voltage change in Volts/Sec,
- ΔV_{DC} is the DC bus voltage ripple in Volts.

Considering state II (Figure 3-5b) for the PC of two bidirectional, S_2 and S_4 are turned

on, $I_{dc} = \dfrac{P_{O\_max}}{V_{DC}}$ and $\Delta T = T_{on\_2} = d_2 \cdot T_s = \dfrac{1 - d_1}{f_s}$

$$C_{DC} = \frac{\dfrac{P_{O\_max}}{V_{DC}}\left(1 - \dfrac{V_{BB}}{V_{DC}}\right)}{f_s \cdot \Delta V_{DC}} \tag{6.21}$$

In a first approach, the effect of the capacitor Equivalent Series Resistance (ESR) is neglected. The target voltage ripple at the DC bus voltage is chosen to be:

$$\delta V_{DC} < 0.005 \tag{6.22}$$

$$\Delta V_{DC} = \delta V_{DC} \cdot V_{DC} \tag{6.23}$$

where δV_{DC} is the p.u. value of the peak to peak voltage ripple at the DC bus capacitor C_{DC}.

Then, once again considering the worst-case condition (i.e., minimum BB voltage (V_{BB_min}) and minimum DC bus voltage (V_{DC_min})), the required value for the DC bus capacitance results:

$$C_{DC} = \frac{\dfrac{P_{O\_max}}{V_{DC\_min}}\left(1 - \dfrac{V_{BB\_min}}{V_{DC\_min}}\right)}{f_s \cdot \delta V_{DC} \cdot V_{DC\_min}} \tag{6.24}$$

$$C_{DC} = \frac{\dfrac{10000}{400}\left(1 - \dfrac{187.5}{400}\right)}{20000 \times 0.005 \times 400} \tag{6.25}$$

$$C_{DC} > 332.03\mu F \tag{6.26}$$

As in the case of the inductance value, a certain safety margin has been ensured, and thus the value of Table 6.9 is finally implemented. The DC bus has two capacitors in series in order to increase the voltage of the DC bus and have access to the middle point of the DC bus.

These design parameters for the reactive elements are kept unchanged for the SPC of the two bidirectional buck converters and the FTPC of the two bidirectional buck-boost converters, in order to compare the variations due solely to the performance of the topology.

Table 6.9: Parameters of the DC bus.

Parameter	Symbol	Value	Unit
Capacitance of the both half of the DC bus	C_{DC_1}, C_{DC_2}	940	μF
Maximum voltage of both half of the DC bus	$V_{DC_1\_max}$, $V_{DC_2\_max}$	450	V
Capacitance of the DC bus	C_{DC}	470	μF
Maximum voltage of the DC bus	V_{DC_max}	900	V

6.5 Electrical Grid and Grid Transformer

For the baseline case in the considered application, the DC microgrid is connected to the distribution line through a three-phase line transformer at the PCC. This transformer is implemented primarily in order to provide galvanic isolation between the distribution grid and the microgrid. If no extra constraints are imposed in the system, the turns ratio of this transformer can be 1:1, yielding to a minimum DC bus value that is typically 700V for nominal European three-phase grid voltage of 400 V_{LL_rms}/50 Hz. Besides, and in the event that it is required, the use of the transformer also allows for an adaptation and matching of the voltage values that might be necessary for proper operation of the VSI PEC grid converter. In the case under study, practical constraints in the implementation of the laboratory setup, such as limitations in the ratings of the protections, static switches, contactors, etc., prevent the DC bus voltage ratings from reaching more than 500 V. Therefore, the line transformer will have a turns ratio of 3/4, that ensures a proper control margin in the grid converter for a European three-phase grid voltage of 400 V_{LL_rms}/50 Hz. Notice that this constraint does not affect the validity of the results obtained. The parameters of the grid are presented in Table 6.10.

6.6 Rest of the DC Microgrid

The rest of the DC microgrid including the RES (PV panels and wind turbines, ...) and the loads are represented by the variable current source in parallel with the variable resistance. Their parameters are presented in Table 6.11.

Table 6.10: Parameters of the grid.

Parameter	Symbol	Value	Unit
Line to Line voltage	V_{LL_rms}	400	V
Voltage ratio of the line transformer	rt_{line}	3/4	-
Frequency	f_e	50	Hz
Phase current	I_{ph_rms}	25	A
Minimum current	I_{G_min}	-35	A
Maximum current	I_{G_max}	35	A
Minimum active power	P_{G_min}	-10	kW
Maximum active power	P_{G_max}	10	kW
Minimum reactive power	Q_{G_max}	-10	kVAR
Maximum reactive power	Q_{G_max}	10	kVAR

Table 6.11: Parameters of the rest of the DC microgrid.

Parameter	Symbol	Value	Unit
Minimum current drawn by the rest of the microgrid	I_{N_min}	-20	A
Maximum current drawn by the rest of the microgrid	I_{N_max}	20	A
Minimum power drawn by the rest of the microgrid	P_{N_min}	-10	kW
Maximum power drawn by the rest of the microgrid	P_{N_max}	10	kW
Nominal DC bus voltage	V_{DC}	500	V

6.7 Control Schemes

Due to the current and the power will flow from the ESS through the inductors and the IGBTs to the DC bus and vice versa. As well from the grid to the DC bus through the filter inductor and vice-versa. The limits of the control schemes should consider all the elements in the system and the lifetime of the ESS.

Some of the control parameters will change depending on the operation mode of the DC microgrid, either islanding mode or grid-connected mode. General consideration for the control are taken into account:

- The bandwidth of the outer DC bus voltage control loop should be ten times less than the inner current control loops in order to appear as instantaneous to the outer loop

($10Bw_v \leq Bw_i$) [86, 160, 161].

- The bandwidth of the SM current control should be faster than the bandwidth of the BB current control loop due to that the SM provides/absorbs the transient power ($Bw_{i\_SM} > Bw_{i\_BB}$) [86].

- The bandwidths of both current control loop should be ten times less than or equal the cutoff frequency of the anti-aliasing filter in order to avoid filtering the dynamics by the anti-aliasing filter ($10Bw_i \leq f_a$).

- The cutoff frequency of the anti-aliasing filter should be less than or equal the half of the sampling frequency by Nyquist–Shannon sampling theorem to avoid aliasing ($2f_a \leq f_{sa}$).

- The sampling frequency should be less than or equal the switching frequency ($f_{sa} \leq f_s$). In particular, a synchronous switching scheme is going to be implemented in the real prototypes.

- The switching frequency is selected depending on the technology of the switch.

6.7.1 Control Parameters during the Islanding Mode

The control schemes (Figure 3-8) consists of outer DC bus control loop and two inner current control loops. Tuning of the PI controller will be discussed in the following Sections:

6.7.1.1 DC Bus Voltage Controller

The open loop transfer function is presented as follows:

$$R_{C_{DC}}(s)G_{C_{DC}}(s) = \frac{K_{p_v}\left(s + \frac{1}{T_{i_v}}\right)}{C_{DC} \cdot s^2} \tag{6.27}$$

where:

- $R_{C_{DC}}$ is the transfer function of the PI controller for the DC voltage control,

- K_{p_v} is the proportional gain of the PI controller of the DC bus voltage control,

- T_{i_v} is the integral time constant of the PI controller of the DC bus voltage control in Secs.

Then, the closed loop transfer function is obtained as follows:

$$\frac{V_{DC}(s)}{V_{DC\_ref}(s)} = \frac{R_{C_{DC}}(s)G_{C_{DC}}(s)}{1 + R_{C_{DC}}(s)G_{C_{DC}}(s)} = \frac{\frac{K_{p_v}\left(s+\frac{1}{T_{i_v}}\right)}{C_{DC}\cdot s^2}}{1 + \frac{K_{p_v}\left(s+\frac{1}{T_{i_v}}\right)}{C_{DC}\cdot s^2}} \tag{6.28}$$

$$= \frac{\frac{K_{p_v}}{C_{DC}}s + \frac{K_{p_v}}{C_{DC}\cdot T_{i_v}}}{s^2 + \frac{K_{p_v}}{C_{DC}}s + \frac{K_{p_v}}{C_{DC}\cdot T_{i_v}}} \tag{6.29}$$

Therefore, the characteristic Equation is calculated as follows:

$$s^2 + 2\zeta\omega_n s + \omega_n^2 = s^2 + \frac{K_{p_v}}{C_{DC}}s + \frac{K_{p_v}}{C_{DC}\cdot T_{i_v}} \tag{6.30}$$

where:

- ω_n is the undamped natural frequency in rads/sec,

- ζ is the damping ratio.

Be equaling the terms, then the proportional gain of the is calculated as:

$$K_{p_v} = 2\zeta\omega_n C_{DC} = 4\zeta\pi Bw_v C_{DC} \tag{6.31}$$

And the integral gain is obtained as follows:

$$T_{i_v} = \frac{K_{p_v}}{\omega_n^2 \cdot C_{DC}} = \frac{4\zeta\pi Bw_v C_{DC}}{4\pi^2 Bw_v^2 \cdot C_{DC}} = \frac{\zeta}{\pi Bw_v} \tag{6.32}$$

ζ is selected to be equal to 0.707 in order to have a maximum peak overshoot of 4.32% [160].

6.7.1.2 BB and SM Currents Controller

In Figure 3-15, assuming the measured and estimated values of the voltage and current are equal to their real values; therefore, the open loop transfer functions are :

$$R_{L_1}(s)G_{L_1}(s) = \frac{K_{p_{i\_BB}}}{L_1 \cdot s}\left(\frac{s + \frac{1}{T_{i_{i\_BB}}}}{s + \frac{R_1}{L_1}}\right) \tag{6.33}$$

$$R_{L_2}(s)G_{L_2}(s) = \frac{K_{p_{i\_SM}}}{L_1 \cdot s}\left(\frac{s + \frac{1}{T_{i_{i\_SM}}}}{s + \frac{R_1}{L_1}}\right) \tag{6.34}$$

where:

- R_{L_1} and R_{L_2} are the transfer function of the PI controller for the BB and SM current controls, respectively,
- $K_{p_{i\_BB}}$ and $K_{p\_i\_SM}$ are the proportional gain of the PI controller of the BB and SM current control, respectively,
- $T_{i_{i\_BB}}$ and $T_{i_{i\_SM}}$ are the internal time of the PI controller of the BB and SM current control, respectively, in S.

From Equations (3.49) and (3.50), the open loop transfer functions of the BB and SM inductors have a pole at $(-\frac{R_1}{L_1})$ and $(-\frac{R_2}{L_2})$, respectively. Typically, these poles are fairly close to the origin and corresponds to a slow natural response. To improve the open-loop frequency response, the pole can be canceled by the zero of the PI controller [162]:

$$T_{i_{i\_BB}} = \frac{L_1}{R_1} \tag{6.35}$$

$$T_{i_{i\_SM}} = \frac{L_2}{R_2} \tag{6.36}$$

Considering the pole is canceling the zero, then the closed loop transfer functions are:

$$\frac{I_{L_1}(s)}{I_{L_{1\_ref}}(s)} = \frac{\frac{K_{p_{i\_BB}}}{L_1 \cdot s}}{1 + \frac{K_{p_{i\_BB}}}{L_1 \cdot s}} = \frac{\frac{K_{p_{i\_BB}}}{L_1}}{s + \frac{K_{p_{i\_BB}}}{L_1}} \tag{6.37}$$

$$\frac{I_{L_2}(s)}{I_{L_{2\_ref}}(s)} = \frac{\frac{K_{p_{i\_SM}}}{L_2 \cdot s}}{1 + \frac{K_{p_{i\_SM}}}{L_2 \cdot s}} = \frac{\frac{K_{p_{i\_SM}}}{L_2}}{s + \frac{K_{p_{i\_SM}}}{L_2}} \tag{6.38}$$

Equations (6.37) and (6.38) are first order with unity gain; therefore, $\frac{K_{p_{i\_BB}}}{L_1}$ and $\frac{K_{p_{i\_SM}}}{L_2}$ are the bandwidth of the closed loop transfer functions. The larger the bandwidth gives the faster the current control response.

$$K_{p_{i\_BB}} = 2\pi Bw_{i\_BB} L_1 \tag{6.39}$$

$$K_{p_{i\_SM}} = 2\pi Bw_{i\_SM} L_2 \tag{6.40}$$

where Bw_{i_BB} and Bw_{i_SM} are the bandwidth of the PI controller of the BB and the SM current control in Hz.

The method used for the tuning the PI current controller is the pole-zero cancellation method. The parameters of the PI DC bus voltage controller and the current controller are tested by Control System Designer tool (sisotool) from MATLAB®.

Table 6.12 includes the parameters of the control schemes during the islanding mode. These parameters are valid in case of the PC and the SPC of the two bidirectional buck converters and the FTPC of the bidirectional buck-boost converters as the inductors connected with the ESS and the DC bus capacitor are kept the same.

The LPF frequency is selected in order to reduce the stress on the BB [55]. The smaller filter frequency, the more significant the amount of power drawn from the SM and smoother the power of the BB. The LPF filter frequency can be obtained from the power profile of the microgrid/nanogrid in islanding mode.

Table 6.13 shows the parameters of the control during the short circuit fault in the DC bus. When the DC bus voltage is less than the minimum voltage threshold, this means that there is a fault and the control during the fault will be activated. However, when the DC bus voltage reaches the maximum threshold voltage, the fault is cleared, and the control during the healthy condition is enabled. The tuning of the PI for BB current control during fault conditions is the same as the previous case (during the islanding mode).

6.7.2 Control Parameters during the Grid-Connected Mode

Upon grid-tied operation mode, two different control strategies can be implemented: independent storage control scheme (Figure 3-17) and full control scheme (Figure 3-21).

Table 6.12: Parameters of the control during islanding mode.

Parameter	Symbol	Value	Units
Outer DC Bus Voltage Control Loop			
DC bus voltage reference	V_{DC_ref}	500	V
Bandwidth	Bw_v	30	Hz
Proportional gain	K_{p_v}	0.124	-
Integral time	T_{i_v}	0.0075	s
LPF of the BB			
Cutoff frequency	$f_{BB_{LPF}}$	0.7	Hz
Inner BB Current Control Loop			
Bandwidth	Bw_{i_BB}	300	Hz
Proportional gain	$K_{p_{i\_BB}}$	27.068	-
Integral time	$T_{i_{i\_BB}}$	0.0422	s
Inner SM Current Control Loop			
Bandwidth	Bw_{i_SM}	500	Hz
Proportional gain	$K_{p_{i\_SM}}$	11.2783	-
Integral time	$T_{i_{i\_SM}}$	0.0422	s
PWM Signals			
Switching frequency	f_s	20	kHz
Dead time	t_D	1	μHz

Table 6.13: Parameters of the control during the fault.

Parameter	Symbol	Value	Units
Minimum DC bus voltage threshold	$V_{DC\_f\_min}$	100	V
Maximum DC bus voltage threshold	$V_{DC\_f\_max}$	400	V
Inner BB Current Control Loop			
Fault current reference	$I_{L_1\_f\_ref}$	5	A
Bandwidth	Bw_{i_BB}	300	Hz
Proportional gain	$K_{p_{i\_BB}}$	27.068	-
Integral time	$T_{i_{i\_BB}}$	0.0422	s

6.7.2.1 Independent Storage Control Strategy

Regarding the independent storage control scheme, two PI current control loops are used. The parameters of these controllers are the same as in the islanding mode. Table 6.14 includes these parameters. The cut-off frequency of the HPF of the SM is kept the same

as the cut-off frequency of the LPF for the BB, as in the case of islanding mode, in order to have the same transient power. However, the cut-off frequency of the HPF of the ESS power is selected smaller than the one of the SM. Again, the values of the HPF frequency can be obtained from the power profile of the DC microgrid or nanogrid.

Table 6.14: Parameters of the control during the grid-connected mode.

Parameter	Symbol	Value	Units
HPF of the ESS power			
Cutoff frequency	$f_{HPF_{ESS}}$	0.4	Hz
HPF of the SM power			
Cutoff frequency	$f_{HPF_{SM}}$	0.7	Hz
Inner BB Current Control Loop			
Bandwidth	Bw_{i_BB}	300	Hz
Proportional gain	$K_{p_{i\_BB}}$	27.068	-
Integral time	$T_{i_{i\_BB}}$	0.0422	s
Inner SM Current Control Loop			
Bandwidth	Bw_{i_SM}	500	Hz
Proportional gain	$K_{p_{i\_SM}}$	11.2783	-
Integral time	$T_{i_{i\_SM}}$	0.0422	s
PWM Signals			
Switching frequency	f_s	20	kHz
Dead time	t_D	1	μHz

6.7.2.2 Voltage Source Inverter Control

The DC bus voltage control loop parameters are the same as the one of the islanding mode. The parameters of the PI current controllers in d and q axes are tuned by pole-zero cancellation method as follows:

$$K_{p_{i\_G\_d}} = 2\pi Bw_{i\_G\_d} L_f \tag{6.41}$$

$$T_{i_{i\_G\_d}} = \frac{L_f}{R_f} \tag{6.42}$$

$$K_{p_{i\_G\_q}} = 2\pi Bw_{i\_G\_q} L_f \tag{6.43}$$

$$T_{i_{i\_G\_q}} = \frac{L_f}{R_f} \tag{6.44}$$

where:

- $K_{p\_i\_G\_d}$ and $K_{p\_i\_G\_q}$ are the proportional gain of the PI controller of the d and q axes grid current control, respectively,
- $Bw_{i\_G\_d}$ and $Bw_{i\_G\_q}$ are the bandwidth of the PI controller of the d and q axes grid current control, respectively, in Hz,
- $T_{i_{i\_G\_d}}$ and $T_{i_{i\_G\_q}}$ are the integral time constant of the PI controller of the d and q axes grid current control, respectively, in Secs.

Table 6.15 includes the main design parameters of the VSI for the DC bus voltage control and the current control in dq axes.

Table 6.15: Parameters of the control for the inverter during grid-connected Mode.

Parameter	Symbol	Value	Units
Outer DC Bus Voltage Control Loop			
DC bus voltage reference	V_{DC_ref}	500	V
Bandwidth	Bw_v	30	Hz
Proportional gain	K_{p_v}	0.124	-
Integral time	K_{i_v}	0.0075	s
Inner d and q Axes Current Control Loop			
Bandwidth	Bw_{i_d}, Bw_{i_q}	300	Hz
Proportional gain	$K_{p_{i\_G\_d}}$, $K_{p_{i\_G\_q}}$	13.534	-
Integral time	$T_{i_{i\_G\_d}}$, $T_{i_{i\_G\_q}}$	0.0422	s
PWM Signals			
Switching frequency	f_s	20	kHz
Dead time	t_D	1	μHz

6.7.2.3 Full Control Strategy

As in this strategy, the control of the HESS and the VSI is included; therefore, there are outer DC bus control loop and four inner current control loops. Table 6.16 includes the parameters of the full control. As it is seen, that the parameters are the same as in the case of independent storage control and the VSI control.

Table 6.16: Parameters of the full control during the grid-connected mode.

Parameter	Symbol	Value	Units
Outer DC Bus Voltage Control Loop			
DC bus voltage reference	V_{DC_ref}	500	V
Bandwidth	Bw_v	30	Hz
Proportional gain	K_{p_v}	0.124	-
Integral time	T_{i_v}	0.0075	s
LPF of the grid			
Cut off frequency	f_{LPF_G}	0.4	Hz
HPF of the SM power			
Cut off frequency	$f_{HPF_{SM}}$	0.7	Hz
Inner d and q Axes Current Control Loop			
Bandwidth	Bw_{i_d}, Bw_{i_q}	300	Hz
Proportional gain	$K_{p_{i\_G\_d}}$, $K_{p_{i\_G\_q}}$	13.534	-
Integral time	$T_{i_{i\_G\_d}}$, $T_{i_{i\_G\_q}}$	0.0422	s
Inner BB Current Control Loop			
Bandwidth	Bw_{i_BB}	300	Hz
Proportional gain	$K_{p_{i\_BB}}$	27.068	-
Integral time	$T_{i_{i\_BB}}$	0.0422	s
Inner SM Current Control Loop			
Bandwidth	Bw_{i_SM}	500	Hz
Proportional gain	$K_{p_{i\_SM}}$	11.2783	-
Integral time	$T_{i_{i\_SM}}$	0.0422	s
PWM Signals			
Switching frequency	f_s	20	kHz
Dead time	t_D	1	μHz

6.8 Conclusions

In this chapter, a complete design of the power stage parts and components, as well as of the control systems of the converters in the HESS has been obtained. These parameters are going to be used in the coming validation chapters. The simulation results will be compared with the experimental results in Chapter 8.

Chapter 7

Simulation Results

Contents

7.1 Introduction

This chapter presents all the simulations intended to verify and assess the performance of the proposed topologies and control strategies shown in the previous chapters. It also targets the validation of the design procedure defined previously for the PC scheme of the two bidirectional buck converters. The performance of this scheme in the specified operating conditions of grid-tied mode and islanding mode is verified for the corresponding control strategies. For the islanding operation mode, the control strategy assumes that the HESS system is taking over both the power flow command and the DC bus control. On the other hand, in the grid-tied scheme, the control strategies assumed are both the full control and the independent control strategies defined in Chapter 3.

Once the performance of the PC baseline case is validated, it is compared against the SPC of the two bidirectional buck converters, in order to assess its behavior upon large mismatch in storage device voltage ratings defined in Chapter 4. Next, the fault-tolerant topology proposed in Chapter 5, based on the parallelization of two buck-boost converters, is compared as well with the PC. Firstly, the performance in healthy conditions is assessed. Finally, the behavior against short-circuit fault of this PC of the two bidirectional buck-boost converters is validated, including the fault ride-through control scheme

outlined. Again, the simulations of each topology will be done in case of the islanding mode and the grid-connected mode. The simulations are carried out with the environment MATLAB/ SIMULINK/ PLECS®.

7.2 Simulation Considerations

In the previous chapters, the main contributions of the research work have been presented, including a theoretical justification and a preliminary evaluation of their validity. These contributions are summarized as the discussion of the operation of the HESS system in islanding and grid-connected operation modes, for the control strategies already discussed; the study of alternate non-isolated topologies and control strategies for solving the voltage mismatch problems; and a discussion on the performance of the HESS upon short-circuit faults at the DC bus, as well as a proposal of a fault ride-though solution. In any case, the verification of these contributions must be carried out rigorously in order to assess the feasibility, the robustness and the limitations in the validity of the solutions that define the constraints of applicability.

The demonstration will start by the islanding operation mode, considering the DC bus control scheme outlined in Chapter 3. Then, the grid-connected operation mode of the microgrid will be resembled, taking into account both the full and the independent control strategies. In this work, the performance of all the proposals will be carried out in a two-step approach; initially, a set of simulations to check and refine the parameters of operation of the proposals will be undertaken. In this simulations, complex, detailed models of all the subsystems involved will be implemented. Later, in Chapter 8, experimental results obtained from a working laboratory prototype of the HESS will be discussed and analyzed.

As a first stage, some general considerations are taken into account, in order to obtain valid results that can be compared against the experimental results that are going to be presented in the next chapter.

- The solver in MATLAB® is discrete, and its type is fixed-step (Sample time = 1 μs). This value is selected given that the switching period equals 50 μs, and thus it is ensured a reasonable resolution, beyond the minimum recommended value of 20

samples per period.

- In order to simulate the electrochemical storage unit, the built-in model of MATLAB /SIMULINK® for a Li-Ion BB is going to be selected. The parameters have been fixed from the available information from the real device from the manufacturer (Table 6.3). In order to establish a baseline reference operation point, the SoC of the BB is considered as 50% ($V_{BB} = 260\ V$).

- In the same manner, an initial SoC of the SM is stated as to allow a symmetrical power capability in case positive or negative power steps occur [46]. Considering the maximum and minimum values indicated in Table 6.6, then this value corresponds to a SM voltage of:

$$V_{SM} = \sqrt{\frac{V_{SM\_max}^2 + V_{SM\_min}^2}{2}} = \sqrt{\frac{(19.2)^2 + (102)^2}{2}} = 73.4\ V \qquad (7.1)$$

- About the integration method selected for the PI controllers, the option chosen is trapezoidal. The PI implementation of the controller is selected in the ideal form.

- Anti-Windup method has been selected to avoid saturation of the controllers. In particular, the methodology used is back-calculation mode.

- The measured magnitudes of voltages and currents in the circuit are filtered by a LPF with a cutoff frequency of 3.5 kHz. This is consistent with the existing signal conditioning available at the laboratory setup.

- A dead-time of 1 μs in the switching of the converters is considered.

- As a reference, the evolution of the systems upon a load step on the 10 kW converter, will be simulated. Two symmetric load steps where the load is changed from 1 kW to 2 kW at 0.5 s and then back to 1 kW again at 2.5 s, is going to be considered in order to compare against the achievable operation values at the experimental results carried out at the coming chapter.

- For the fault analysis, a short circuit fault sequence has been defined. The DC bus is shorted at $t = 0.5\ s$ and cleared after two seconds (at $t = 2.5\ s$).

- The colors of the simulation Figures are defined according to Table 7.1, and the same colors will be kept in the following Chapter in order to easily compare with the experimental results.

Table 7.1: Colors of the simulation figures.

Parameter	Color
References of the controllers	Magenta
Using only single ESS (BB only)	Green
Utilizing inverter only without ESS	Black
Using PC of two bidirectional buck converters	Blue
Utilizing SPC of two bidirectional buck converters	Red
Utilizing FTPC of two bidirectional buck-boost converters	Yellow

7.3 Baseline Case: Parallel Connection of the Two Bidirectional Buck Converters

The benefits of using the HESS in power systems, compared to the ones if a simple ESS, are to optimize the size and cost of the storage system, and to simultaneously increase the lifetime of the BB while improving the dynamic performance of the system. Initially, it will be assessed how the use of a HESS performs in these main aspects, against a regular ESS with a unique storage system. In order to guarantee the energy storage requirements, the single storage unit will be the BB based storage system. Then, the islanding operation mode will be targeted. It is assumed that there is no connection to the distribution grid through the grid PEC at the PCC, and therefore the HESS is controlling the DC bus voltage. After the grid-connected mode with the two schemes is verified, the steady-state operation of the converter is analyzed.

7.3.1 Islanding Operation Mode

In this operating mode, a voltage control loop is applied to the converters of the ESS, in order to keep the DC bus voltage at a reference value of 500 V. The DC bus voltage control is implemented at the HESS control stage. The BB is providing or absorbing the steady-state power, and the SM is suppling or absorbing the transient power. But in a first step, Figure 7-1 compares the performance between using the defined HESS, formed by the coordinated assembly of the BB and the SM storage units, versus a single storage unit ESS, formed by the BB only.

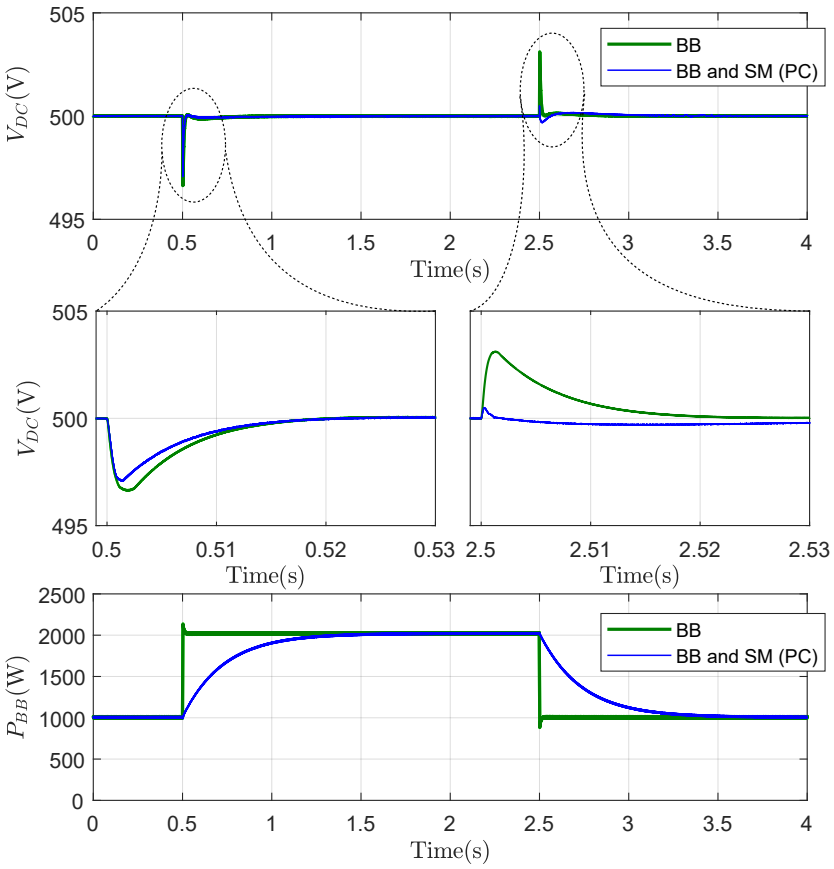


Figure 7-1: Simulation results in islanding mode for two storage systems: the HESS vs. the single ESS (BB only).

The sequence of the power steps applied to the system is the one depicted in the general consideration of this Chapter. It can be seen how the DC bus voltage varies less in magnitude, in the case of the HESS, rather than in the case of the BB only. This is due to the

fact that the SM has the ability to provide power with higher dynamics than in the case of the BB when required to track the DC bus voltage reference. Also, it is noticed how in the HESS, the BB does not suffer a quick change in di/dt, as compared to the single storage ESS. This yields to an increase in the SoH of the device, and hence on the lifetime of the BB, as expected.

In order to validate the control scheme (Figure 3-8), the output power demand (P_O) is changed using the defined power step sequence (Figure 7-2). The performance of the HESS in this control scheme can be seen in Figures 7-2 and 7-3.

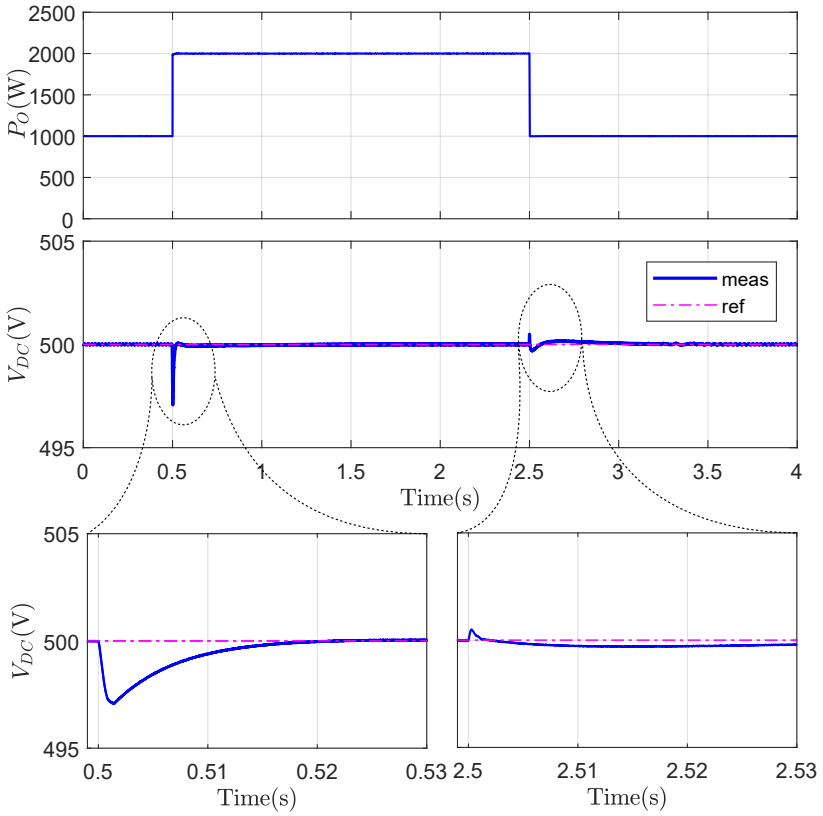


Figure 7-2: Simulation results for the PC of the two bidirectional buck converters during the islanding mode showing the performance of the outer DC bus voltage loop control.

The references (magenta lines) of the DC bus voltage and the powers of the BB and the SM are compared with their measured (blue lines) to validate the control scheme. The DC bus voltage (V_{DC}) reference is 500 V; when the output power (P_O) changes at 0.5 s, V_{DC} decreases down to 497 V; on the other hand, when power demand (P_O) varies back at 2.5 s, V_{DC} increases slightly up to 500.5 V. The behavior of the DC bus voltage at 0.5

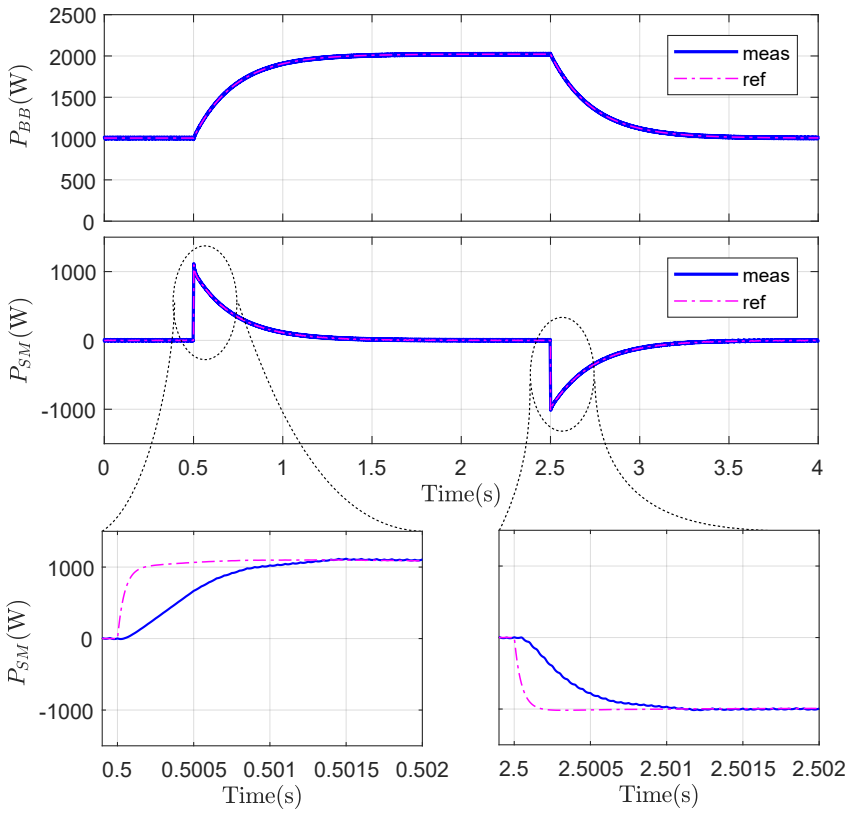


Figure 7-3: Simulation results for the PC of the two bidirectional buck converters during the islanding mode showing the performance of the two inner control loops.

s is different from its behavior at 2.5 s and not symmetrical. This effect is due to that it is relatively easy for the SM to absorb the current from the DC bus voltage.

About the hybrid performance of the control system, it can be seen in Figure 7-3 how the BB is providing and absorbing the steady-state power. However, the SM is providing and absorbing the transient power, as the control is designed to limit the transient power delivered by the BB, thus increasing its lifespan. It is noticed that the peak transient SM power (P_{SM}) is 1.099 kW and not 1 kW at 0.5 s. This effect is due to the fact that the SM needs to provide the transient power for the load and also to the DC bus, in order to recover the original DC bus voltage to 500 V. The measured values (blue lines) are tracking their references (magenta lines), within the limitations of the control system. It must be noticed that given that the voltages at the BB and the SM present a relatively small variation within the simulation interval, then the power references variations are representing the current references variations. Thus, this power evolution can be used to validate the two

inner current control loops. The power distribution between the BB and SM at Figure 7-3 matches the power distribution from the theoretical analysis in Figure 3-12a.

7.3.2 Grid-Connected Operation Mode

Once the islanding mode has been validated through simulations, the grid-tied operation can be targeted. In this case, there is an effective capability of interchanging power between the microgrid and the distribution network, through the grid PEC at the PCC. It is assumed that the DC bus control is carried out by this grid PEC. As mentioned before, two different control strategies can be implemented, the independent and the full control strategies.

In the independent control, there is no communication between the grid inverter control and the proposed HESS control. Therefore the full HESS can be conceived in the manner of a "plug and play" autonomous system that can be attached to any existing DC microgrid. On the other hand, in the full control strategy, the inverter and the ESS control is designed in a coordinated manner, and both converters are jointly controlled. In both control strategies, the control scheme for the PC of the two bidirectional buck converters is firstly validated in this section. Later, the control schemes of the SPC of the two bidirectional buck converters and the FTPC of the buck-boost based solution are compared with the baseline case.

In any case, it will be considered that the reactive power is equal to zero ($Q_{G\_ref} = 0$). Also, it will be assumed that the power references that would provide the peak-shaving feature in the performance of the HESS are equal to zero ($P_{BB\_ps\_ref} = P_{SM\_ps\_ref} = 0$).

7.3.2.1 Independent Control Strategy

In this strategy, the DC bus voltage is controlled by a VSI connected to the grid, in order to maintain the DC bus voltage around the reference value of 500 V. The SM is providing or absorbing the transient peak power and the BB is providing or absorbing the rest of the transient power. Figure 7-4 shows the effect of adding the HESS. It can be seen how the DC bus voltage varies much more if the HESS is not connected (black lines), compared to the variations when the HESS is attached and controlled adequately (blue lines). However, it is also noticeable that the DC bus voltage evolution is slower in the case of the HESS

connection than in the case of the inverter only.

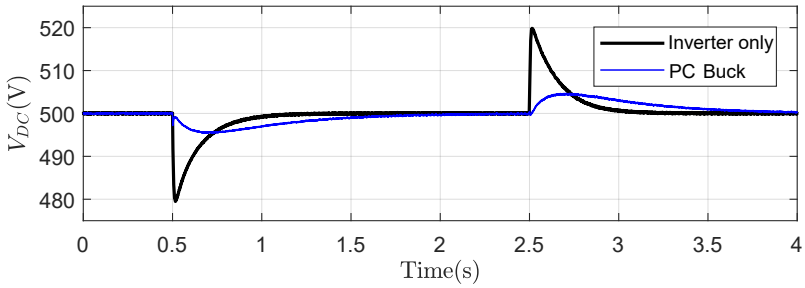


Figure 7-4: Simulation results for the inverter only and the PC of the two bidirectional buck converters during the grid-connected mode (Independent control strategy).

The following Figures 7-5 and 7-6 are validating the control scheme for the independent control outlined in Figure 3-17. The measured (blue lines) of the DC bus voltage and the power of the full ESS (the BB and the SM) are tracking their references (magenta lines).

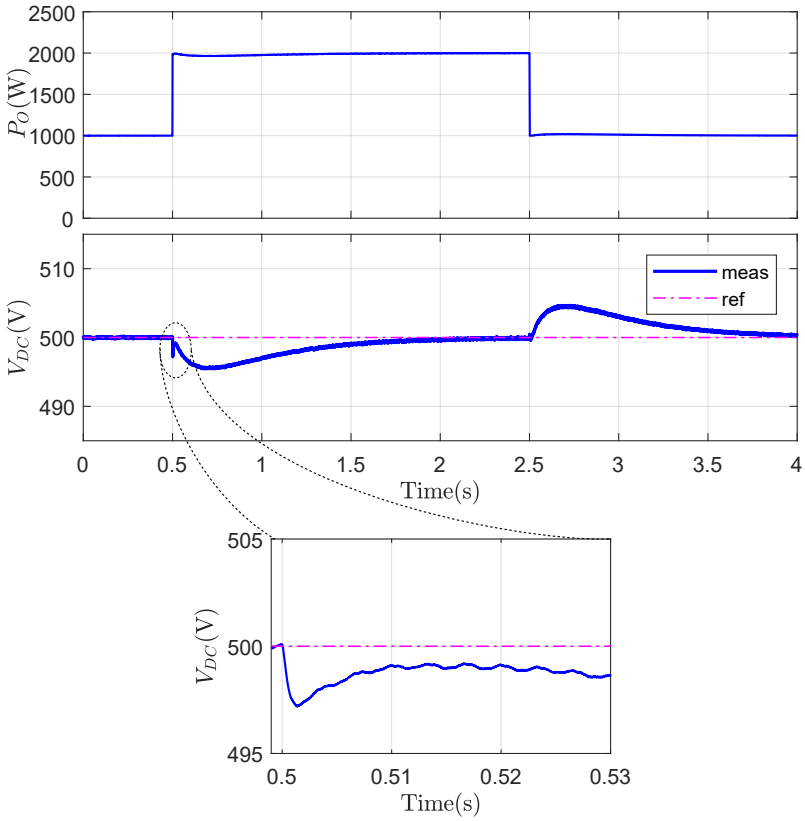


Figure 7-5: Simulation results for the PC of the two bidirectional buck converters during the grid-connected mode (Independent control strategy) showing the performance of the outer DC bus voltage control loop.

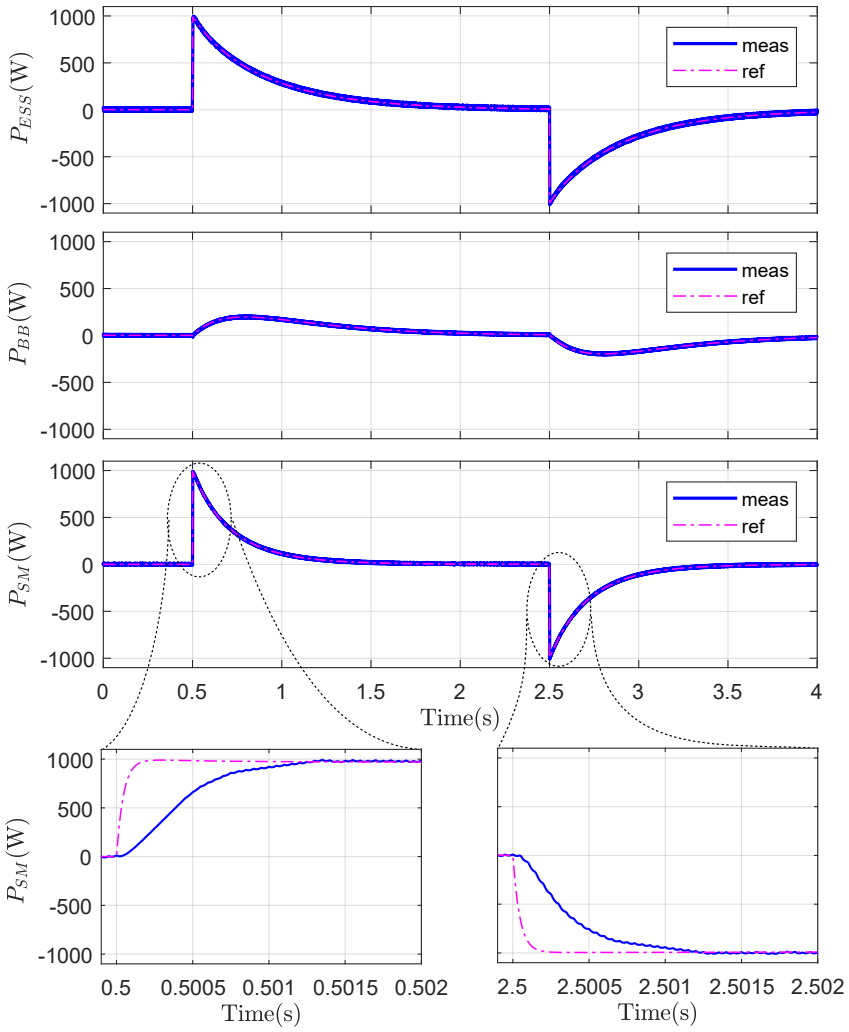


Figure 7-6: Simulation results for the PC of the two bidirectional buck converters during the grid-connected mode (Independent control strategy) showing the performance of the two inner control loops.

It must be noticed in Figure 7-5 how the DC bus voltage evolves initially (see a zoomed area of the DC bus voltage) by decreasing, then slightly increases, to finally decrease again. This situation, when the output power changes at 0.5 s, is due to the fact that there is no communication between the control stages, the one of the grid inverter and the one of the HESS. In fact, both are trying to recover the DC bus simultaneously, yielding to this effect.

As the control has been designed in Figure 3-17 to split the power contribution of the storage devices, it can be seen how effectively the ESS power is divided between the SM power (provides/absorbs the transient peak power) and the BB power (delivers/absorbs the rest of the transient power). This power share is depicted in Figure 7-6, and it matches with

the theoretical power distribution at Figure 3-18a.

7.3.2.2 Full Control Strategy

In this control, there is a typical, coordinated design of the full system control, including the VSI, the BB and the SM converters. The primary purpose of this control is again to maintain the DC bus voltage close to the reference of 500 V, for any power profile demanded by the load. The VSI is designed to provide/absorb the steady-state power; the SM, in turn, is targeted to provide/absorb the transient peak power; whereas the BB will take over the remaining transient power.

Figure 7-7 shows that by using this full control scheme, the recovery of the DC bus voltage (blue lines) is much faster when compared against the two previous cases, i.e., without ESS (black lines) and with the independent control scheme (cyan lines).

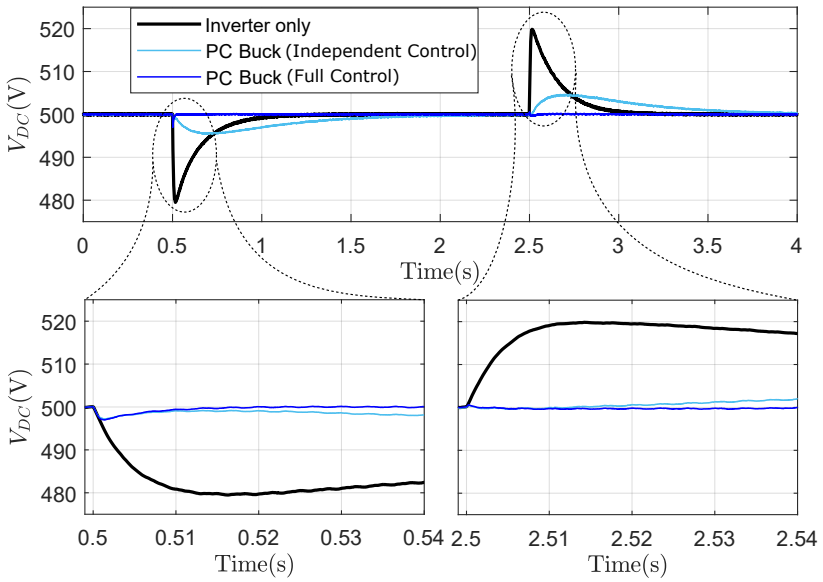


Figure 7-7: Simulation results for the inverter only and with HESS (Independent control and full control strategies) during the grid-connected mode.

The control scheme defined in Figure 3-19 is now validated in Figure 7-8 and Figure 7-9. As it can be noticed in Figure 7-8, the measured (blue line) DC bus voltage is tracking its reference (magenta line). On the other hand, Figure 7-9 shows the power share among the different subsystems; the grid provides/absorbs the steady-state power, and the ESS provides/absorbs the transient power. The ESS power is divided between the SM

(provides/absorbs the transient peak power) and the BB (provides/absorbs the rest of the transient power). Figure 7-9 matches the theoretical power share at Figure 3-22a.

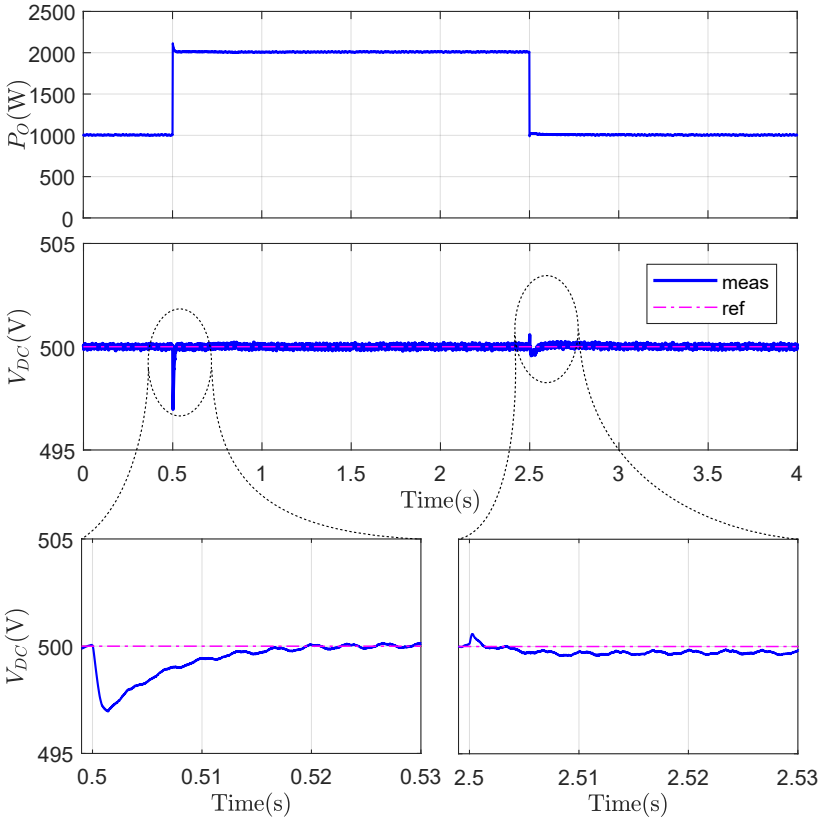


Figure 7-8: Simulation results for the PC of the two bidirectional buck converter during the grid-connected mode (Full control strategy) showing the performance of the outer DC bus voltage control loop.

7.3.3 Steady-State Operation

At this point, one aspect still pending is to verify that the design conditions, such a the current ripple in the inductor at the steady-state operation of the baseline case, match the specifications stated in Chapter 6. The inductors current ripples will be calculated theoretically for the operating parameters under consideration, and then they will be compared with the simulation results. From Equation (6.5), the current ripple of the inductor connected to the BB is as follows:

$$\Delta I_{L_1} = \frac{V_{BB}(1 - \frac{V_{BB}}{V_{DC}})}{f_s L_1} \tag{7.2}$$

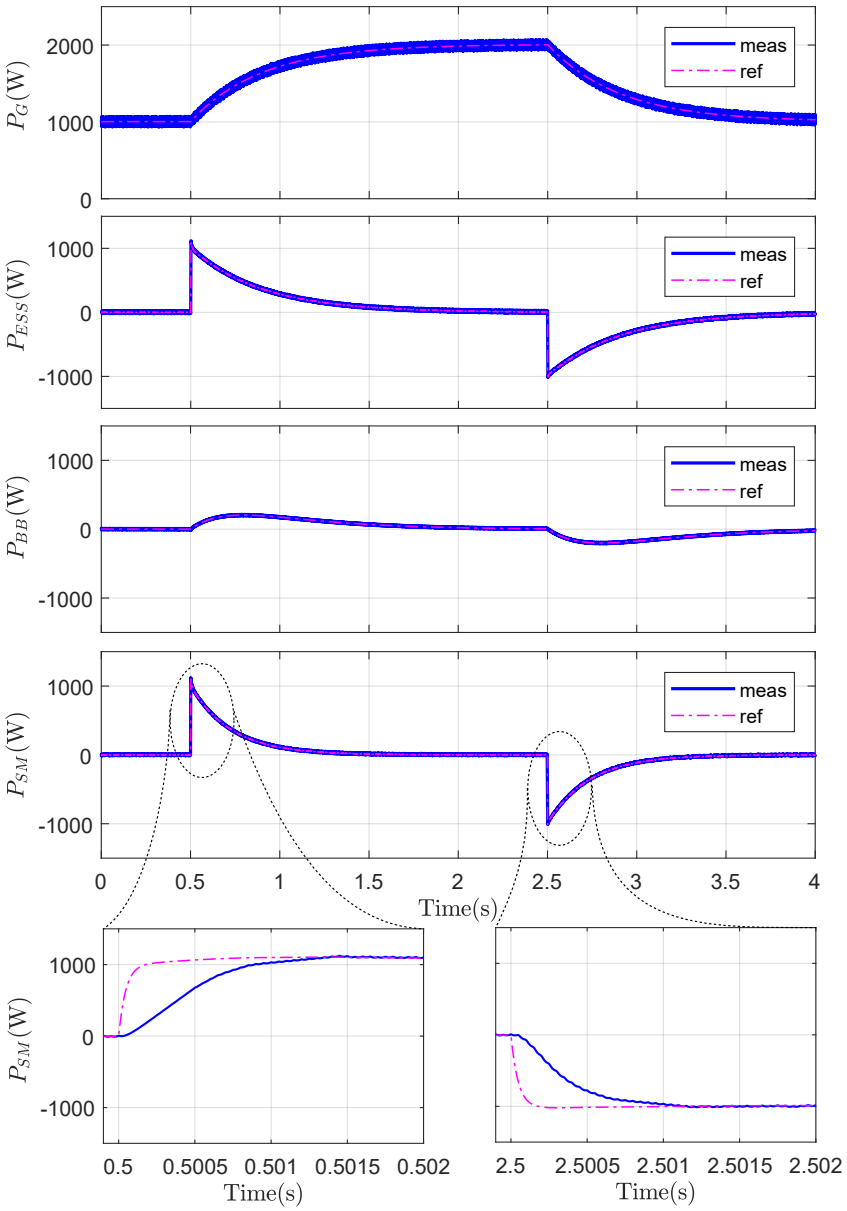


Figure 7-9: Simulation results for the PC of the two bidirectional buck converters during the grid-connected mode (Full control strategy) showing the performance of the four inner control loops.

$$\Delta I_{L_1} = \frac{260(1 - \frac{260}{500})}{20000 \times 14.36 \times 10^{-3}} = 0.4345\ A \tag{7.3}$$

Another way to calculate the current ripple during T_{off_2}, considering state I (Figure 3-5a) and state II (Figure 3-5b), the lower switch S_2 is opened so the $V_{CE_2} = V_{DC}$ and $\Delta T = T_{off\_2} = T_{on\_1} = d_1 \cdot T_s = \frac{d_1}{f_s}$. The ripple current of the inductor connected to the

BB is as follows:

$$\Delta I_{L_1} = \frac{(V_{BB} - V_{DC})d_1}{f_s \cdot L_1} = \frac{(V_{BB} - V_{DC})\dfrac{V_{BB}}{V_{DC}}}{f_s \cdot L_1} \tag{7.4}$$

$$\Delta I_{L_1} = \frac{(260 - 500)\dfrac{260}{500}}{20000 \times 14.36 \times 10^{-3}} = -0.4345\ A \tag{7.5}$$

The negative sign means the slop is negative. It is noticed that the current ripple in turn off of the S_2 has the same value in turn on.

Now, the current ripple of the inductor connected to the SM (ΔI_L) is calculated with the same technique. From Equation (6.12), yields to:

$$\Delta I_{L_2} = \frac{V_{SM}(1 - \dfrac{V_{SM}}{V_{DC}})}{f_s \cdot L_2} \tag{7.6}$$

$$\Delta I_{L_2} = \frac{73.4(1 - \dfrac{73.4}{500})}{20000 \times 3.59 \times 10^{-3}} = 0.8722\ A \tag{7.7}$$

Again, during T_{off_4}, considering state I (Figure 3-5a), the switch S_4 is turned-off so the $V_{CE_4} = V_{DC}$ and $\Delta T = T_{off\_4} = T_{on\_3} = d_3 \cdot T_s = \dfrac{d_3}{f_s}$. The ripple current of the inductor connected to the SM is as follows:

$$\Delta I_{L_2} = \frac{(V_{SM} - V_{DC})d_3}{f_s L_2} = \frac{(V_{SM} - V_{DC})\dfrac{V_{SM}}{V_{DC}}}{f_s L_2} \tag{7.8}$$

$$\Delta I_{L_2} = \frac{(73.4 - 500)\dfrac{73.4}{500}}{20000 \times 3.59 \times 10^{-3}} = -0.8722\ A \tag{7.9}$$

The current ripple value in turn off of S_4 is the same as during turn on. However, this is different from the SPC case, as it will be discussed later in the following sections.

In order to compare with the simulation results, the DC bus is regulated by the VSI to a constant value of 500V, and the BB and SM current references are set at 5 A and 10 A, respectively. Figure 7-10 shows the currents at the inductors of both storage devices at the ESS, plus the collector-emitter voltages of the switches S_2 and S_4. As it is noticed from

Figure 7-10, the peak to peak current ripple of the inductor connected to the BB is 0.4291 A and the peak to peak current ripple of the inductor connected to the SM is 0.8257 A. The main operating waveforms are tracking the expected theoretical values outlined. Therefore, it can be concluded that the design of the converter has been carried out satisfactorily.

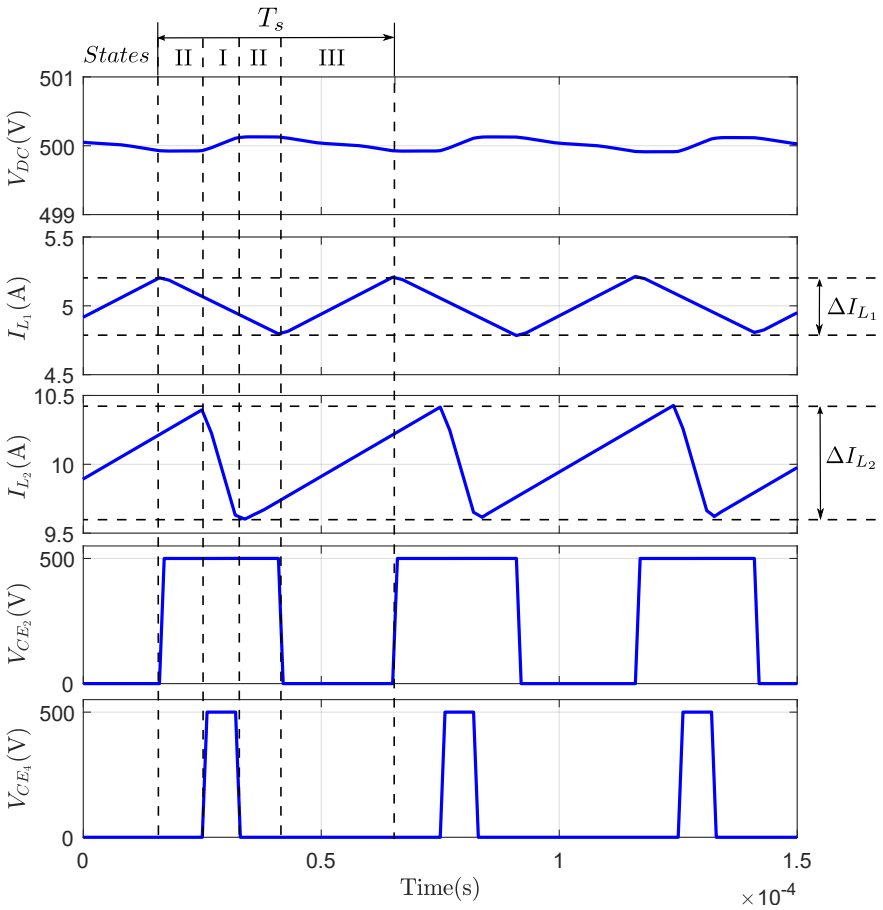


Figure 7-10: Simulation results for the PC of two bidirectional buck converters where 5 A BB current reference and 10 A SM current reference are applied and the grid VSI controls the DC bus.

The collector-emitter voltage of $IGBT_2$ and $IGBT_4$ in Figure 7-10 can represent the duty cycles of the BB and SM converters, respectively. As it can be noticed from Figure 7-10 that the SM converter has a small duty cycle compared to the duty cycle of the BB converter. This yields to thermal and electrical stress on the switches.

7.4 Series-Parallel Connection of Bidirectional Buck Converters

Once the baseline case has been studied for every healthy operating condition, the operation of the SPC scheme is now going to be verified by simulations. The main conditions of the simulation will be maintained, in order to obtain results that can be easily compared. In a first stage, the situation in islanding mode will be validated; later, the grid-tied operation mode will be tackled, for both the independent and the full control strategies. Then, the steady-state operation will be verified.

7.4.1 Islanding Operation Mode

At this section, the simulations already were done for PC of the two bidirectional buck converters will be compared with the performance of the SPC. Again, the power step sequence will follow the already defined evolution. This load power, (P_O) is changed from 1 kW to 2 kW at 0.5 s and back to 1 kW at 2.5 s. Figure 7-11 shows the evolution of the SPC scheme against the PC scheme and also against the non-hybrid ESS (BB only).

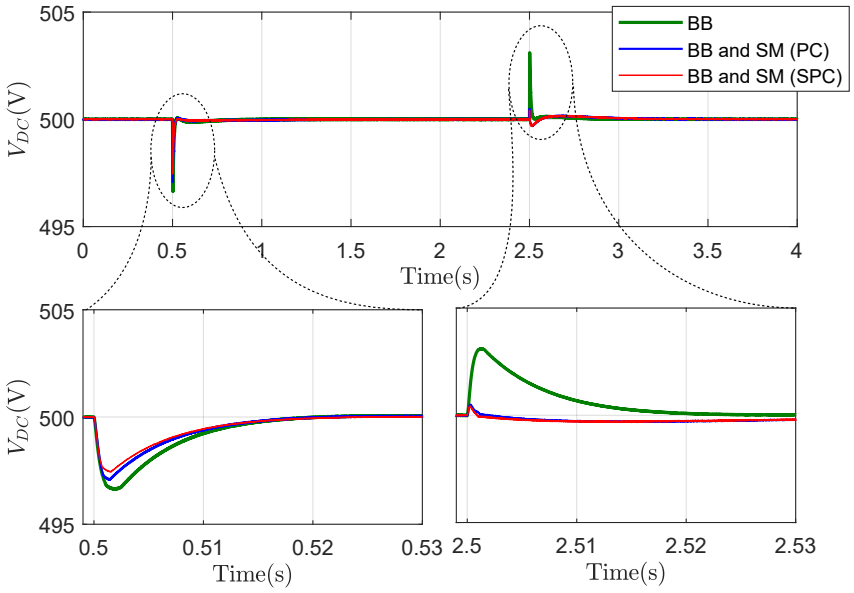


Figure 7-11: Simulation results for the SPC of the two bidirectional buck converters compared to the PC one and the BB only during the islanding mode.

It can be seen from Figure 7-11 how the SPC has a better performance than the non-hybrid solution, but also a slightly better performance than the PC scheme. Again, the improvement is much more significant in recovering the DC bus voltage (V_{DC}) when the load power increases or the SM has a small voltage compared with the SM voltage in the PC as it will be seen in the following discussion. This is because, in the SPC scheme, the SM is providing the transient power (P_{SM}) slightly faster than in case PC as shown in Figure 7-12. The power provided by the BB (P_{BB}) is the same in both cases.

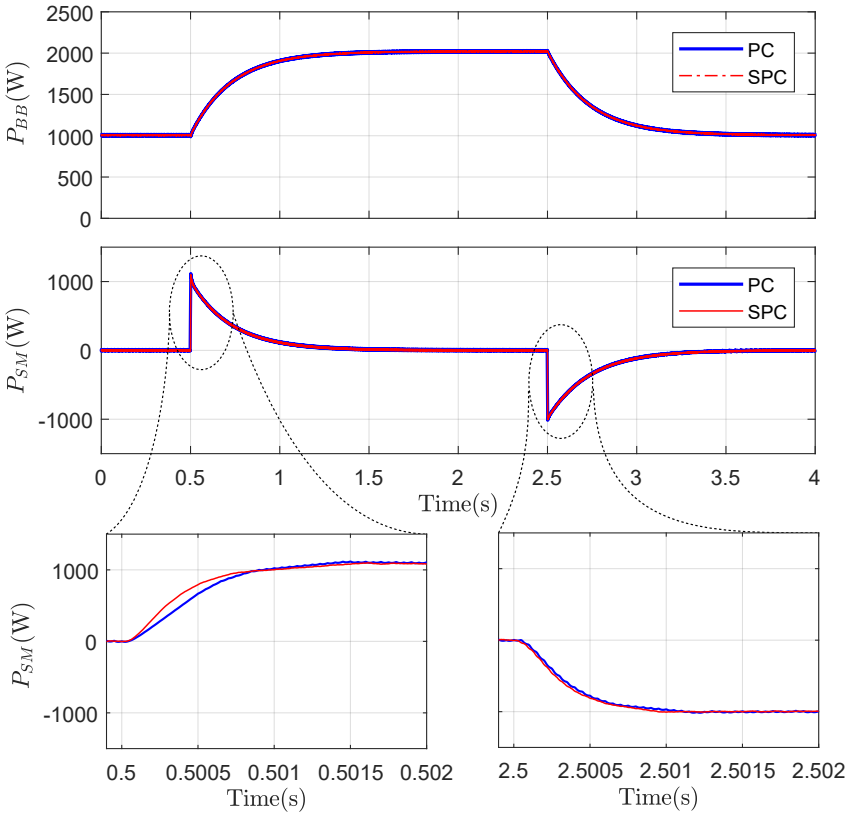


Figure 7-12: Simulation results for the SPC of the two bidirectional buck converters compared to the PC one during the islanding mode showing the power distribution between ESSs.

The critical aspect at the SPC scheme is that the SM can provide a faster power dynamics, given that the margin of possible variations of the duty cycle of switch S_3 (d_3) is much more significant than the case of PC (see Figure 7-13). In case of the PC, the duty cycle of the SM (blue line) is saturated to zero. On top of allowing a faster variation of the current levels involved, this situation also affects that, for the case of the SPC, the thermal

and electrical stresses on the IGBTs are balanced. This last aspect yields to increase the lifetime of the IGBTs, also contributing to solving, up to some extent, the problem of the voltage mismatch.

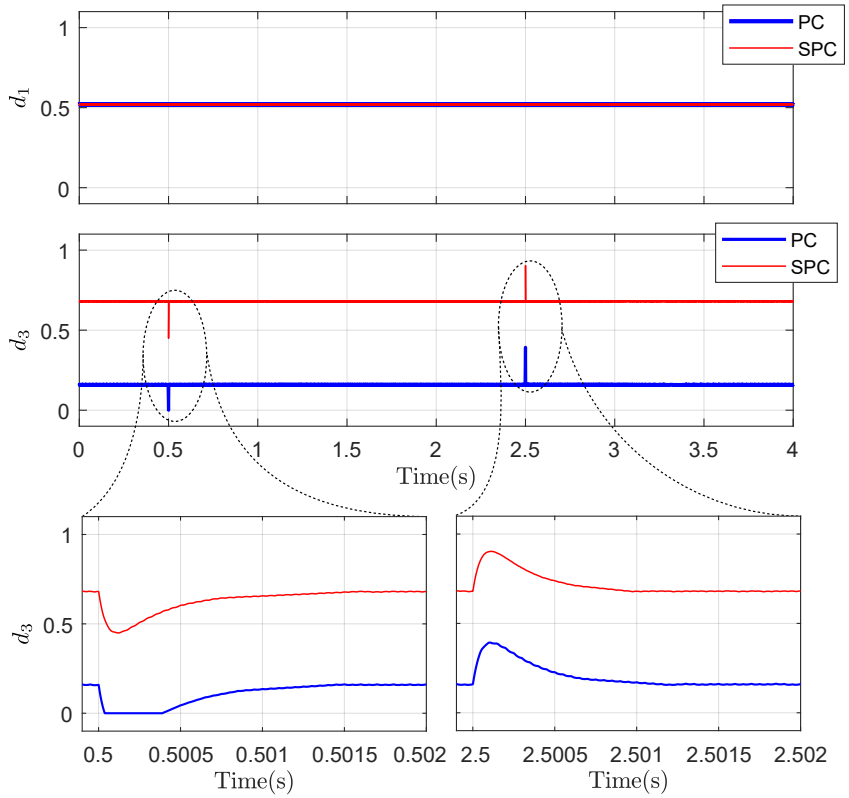


Figure 7-13: Simulation results for the SPC of the two bidirectional buck converters compared to the PC one during the islanding mode showing the duty cycles of BB and SM.

All the aforementioned problems of the too narrow duty ratio range obtained for PC scheme are therefore solved in the SPC configuration. On the other side, the duty cycle of the S_1 (d_1), which defines the behavior of the BB subsystem, is the same in both the PC and the SPC cases (0.5) and does not suffer any change in its contribution to the load power.

Figure 7-14 shows the DC bus voltage when the SM voltage decreases down 40 V. This is an extreme situation, but realistic, since the SM might be discharged during regular operation. It is noticed that the DC bus decreases significantly upon an increasing load step, for the PC (blue line), whereas this decrease is much smaller for the SPC (red line). This is because, unlike in the case of SPC, the duty cycle reaches saturation in PC scheme.

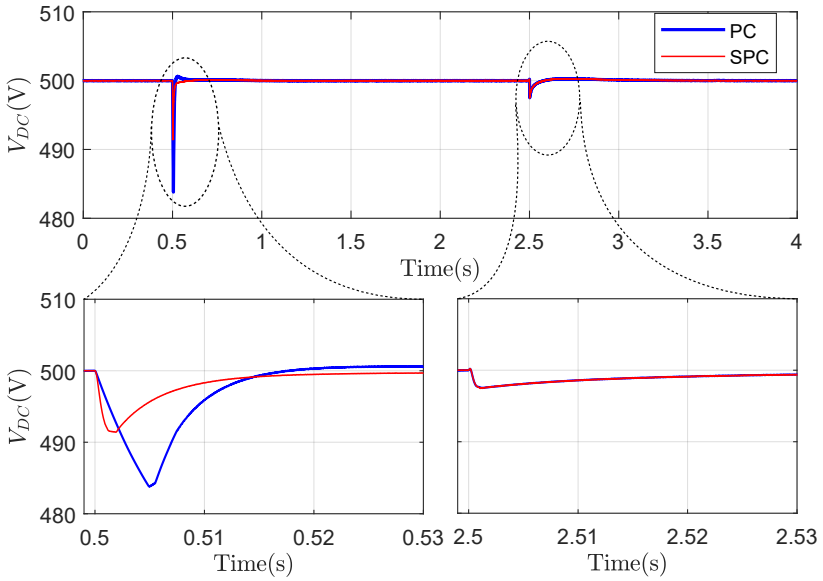


Figure 7-14: Simulation results for the SPC of the two bidirectional buck converters compared to the PC one during the islanding mode, showing the behavior of the DC bus ($V_{SM} = 40V$).

7.4.2 Grid-Connected Operation Mode

Once the performance of the SPC in islanding mode is calculated, the effect of connecting to the grid will now be assessed. The same sequence of simulations will be carried out. Initially, the independent control will be targeted, and later the full control strategy will be performed.

7.4.2.1 Independent Control Strategy

The simulations results of the SPC of the two bidirectional buck converters will be compared to the PC. Figure 7-15 shows the DC bus voltage in case the grid inverter has not any storage unit (black line), compared to the effect of the two possible HESS systems (i.e., PC (blue line) and SPC (red line) schemes, for grid-tied independent control scheme). It can be seen how the SPC scheme has slightly better performance compared to the PC scheme in the recovery of the DC bus.

As noticed from Figure 7-16, the SM in SPC provides power a little bit faster than the PC one at 0.5 s. This is due to duty of the $IGBT_3$ in the SPC scheme is not saturated when the output power increases at 0.5 s as depicted in Figure 7-17. The power of the ESS and

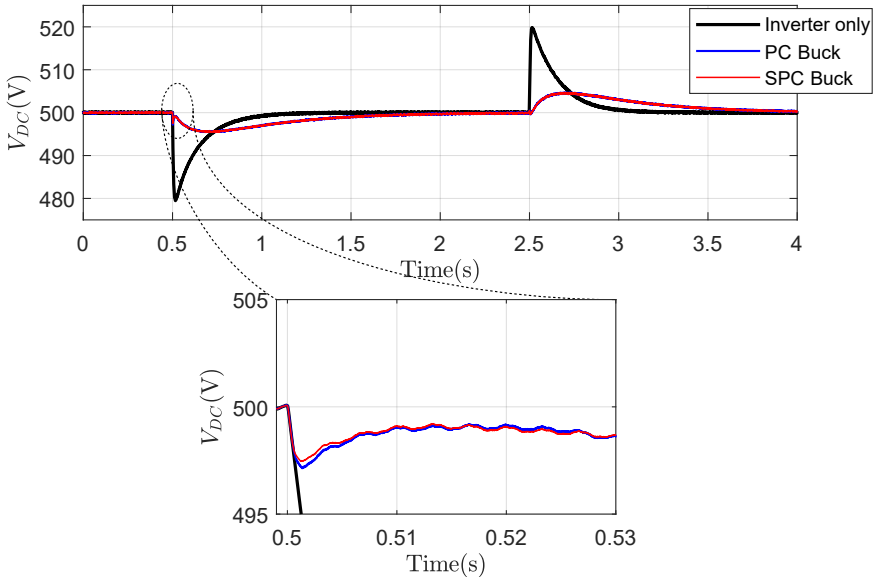


Figure 7-15: Simulation results for the SPC of the two bidirectional buck converters compared to the PC one during the grid-connected mode (Independent control strategy) and the inverter only.

the BB are the same in both cases (PC (blue line) and SPC (red line) as shown in Figure 7-16.

7.4.2.2 Full Control Strategy

The results of the SPC scheme are now compared to the PC, again in the grid-tied operation mode, but for the full control strategy. Figure 7-18 shows how a better dynamics is obtained in the recovery of the DC bus voltage for the SPC (red line) compared to the system without storage (black line) and the PC (blue line). Again the performance of the SPC scheme (red line) is slightly better than in the case of the PC scheme (blue line).

The power of the grid (P_G) and the BB (P_{BB}) in SPC (red line) are fully matched with the PC case (blue line). However, the power of the SM (P_{SM}) in SPC evolves faster than in PC as depicted in Figure 7-19. This is due to the duty cycle of the S_3 (d_3) in SPC does not saturate, as shown in Figure 7-20.

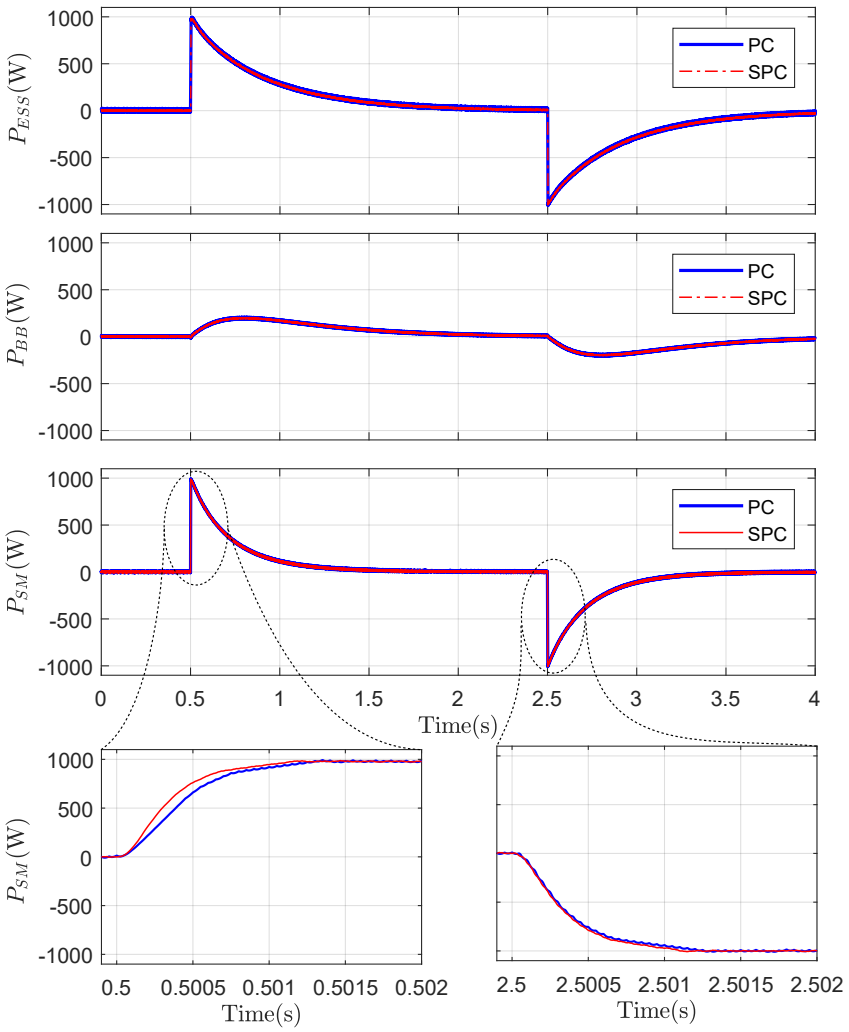


Figure 7-16: Simulation results for the SPC of the two bidirectional buck converters compared to the PC one during the grid-connected mode (Independent control strategy) showing the power distribution between ESSs.

7.4.3 Steady-State Operation

The validity of the design of the SPC will be demonstrated by assessing the current ripple value in steady-state operation, as in the case of the PC scheme. At steady-state, the duty of S_3 is greater than the duty cycle of S_1, then the states I, III and IV will occur (Figure 7-21).

During T_{on_2}, considering the state III (Figure 4-5c) and state IV (Figure 4-5d), the ripple current of the inductor connected to the BB is precisely the same as in the case of the PC of the two bidirectional buck converter (Equation (7.3)). However, if the state I

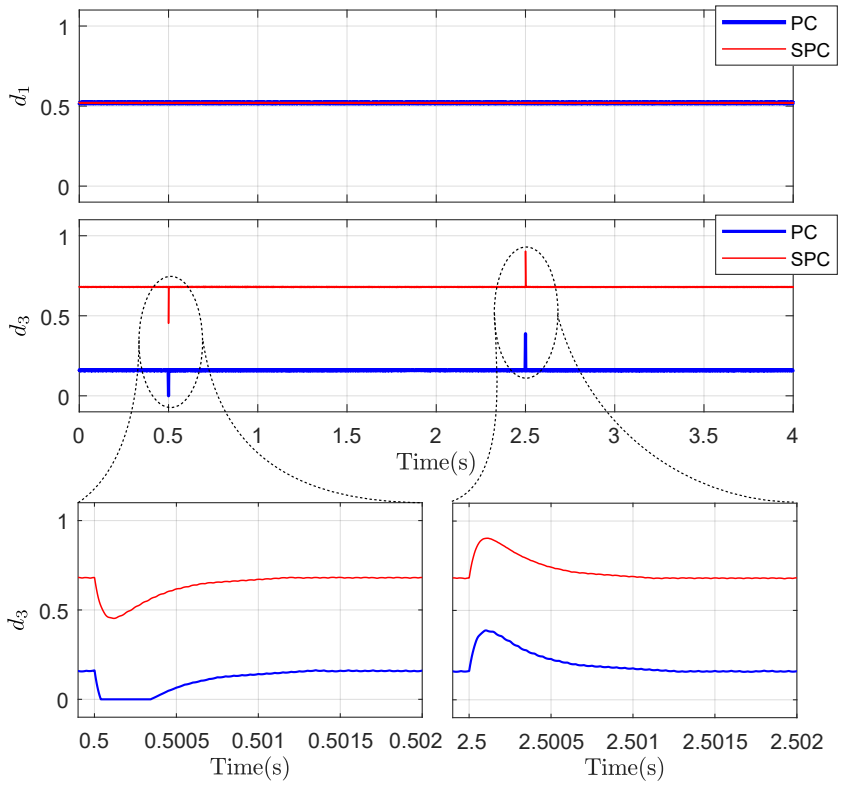


Figure 7-17: Simulation results for the SPC of the two bidirectional buck converters compared to the PC one during the grid-connected mode (Independent control strategy) showing the duty cycles of the BB and the SM.

(Figure 4-5a) and state II (Figure 4-5b) is considered during T_{off_2}, the ripple current of the inductor connected to the BB matches the one stated at Equation (7.5).

From Equation (4.27), the voltage of the inductor connected to the SM is calculated as follows:

$$V_{L_2} = V_{CE_2} + V_{SM} - V_{CE_4} \tag{7.10}$$

During T_{on_4}, considering the state III (Figure 4-5c), $V_{CE_2} = 0$ and $V_{CE_4} = 0$ and $\Delta T = T_{on\_4} = (1 - d_3)T_s = \dfrac{1 - d_3}{f_s}$. Therefore, the ripple current of the inductor connected to the SM as follows:

$$\Delta I_{L_2} = \frac{V_{SM}(1 - d_3)}{f_s \cdot L_2} = \frac{V_{SM}(1 - \dfrac{V_{BB} + V_{SM}}{V_{DC}})}{f_s \cdot L_2} \tag{7.11}$$

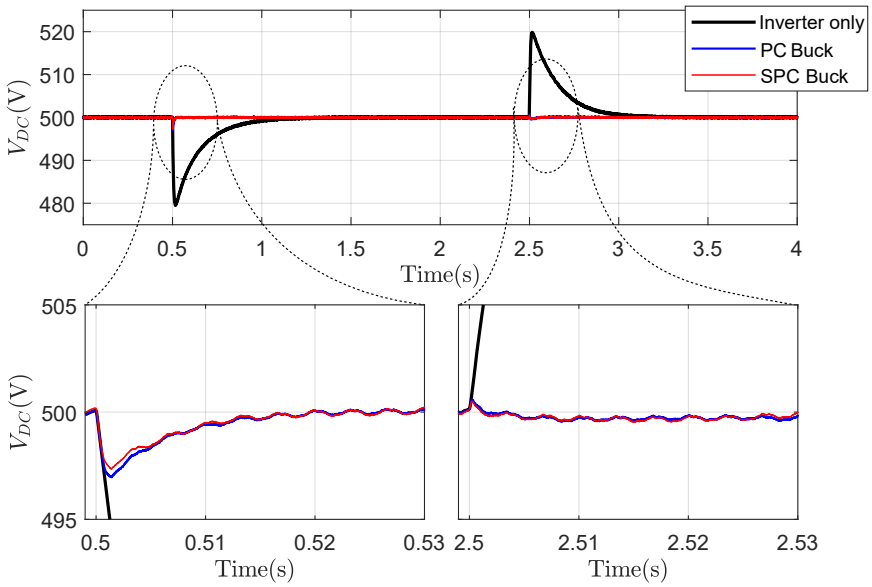


Figure 7-18: Simulation results for the SPC of the two bidirectional buck converters compared to the PC one during the grid-connected mode (Full control strategy) and inverter only.

$$\Delta I_{L_2} = \frac{73.4(1 - \frac{260 + 73.4}{500})}{20000 \times 3.59 \times 10^{-3}} = 0.3388\ A \tag{7.12}$$

During T_{off_4}, there are two different cases: Considering State I (Figure 4-5a), $V_{CE_2} = V_{DC}$ and $V_{CE_4} = V_{DC}$ and $\Delta T = T_{off\_2} = T_{on\_1} = d_1 \cdot T_s = \frac{d_1}{f_s}$. Then, the current ripple of the inductor connected to SM is obtained as follows:

$$\Delta I_{L_2} = \frac{(V_{DC} + V_{SM} - V_{DC})(d_1)}{f_s \cdot L_2} = \frac{(V_{SM})(\frac{V_{BB}}{V_{DC}})}{f_s \cdot L_2} \tag{7.13}$$

$$\Delta I_{L_2} = \frac{73.4(\frac{260}{500})}{20000 \times 3.59 \times 10^{-3}} = 0.5316\ A \tag{7.14}$$

Now, considering state IV (Figure 4-5d), $V_{CE_2} = 0$ and $V_{CE_4} = V_{DC}$ and $\Delta T = \frac{T_{off\_4} - T_{off\_2}}{2} = \frac{T_{on\_3} - T_{on\_1}}{2} = d_3 \cdot T_s - d_1 \cdot T_s = \frac{(d_3 - d_1)T_s}{2}$. Therefore, the current ripple of the inductor connected to SM is calculated as follows:

$$\Delta I_{L_2} = \frac{(V_{SM} - V_{DC})\left(\frac{d_3 - d_1}{2}\right)}{f_s \cdot L_2} = \frac{(V_{SM} - V_{DC})\left(\frac{(\frac{V_{BB}+V_{SM}}{V_{DC}}) - \frac{V_{BB}}{V_{DC}}}{2}\right)}{f_s \cdot L_2} \tag{7.15}$$

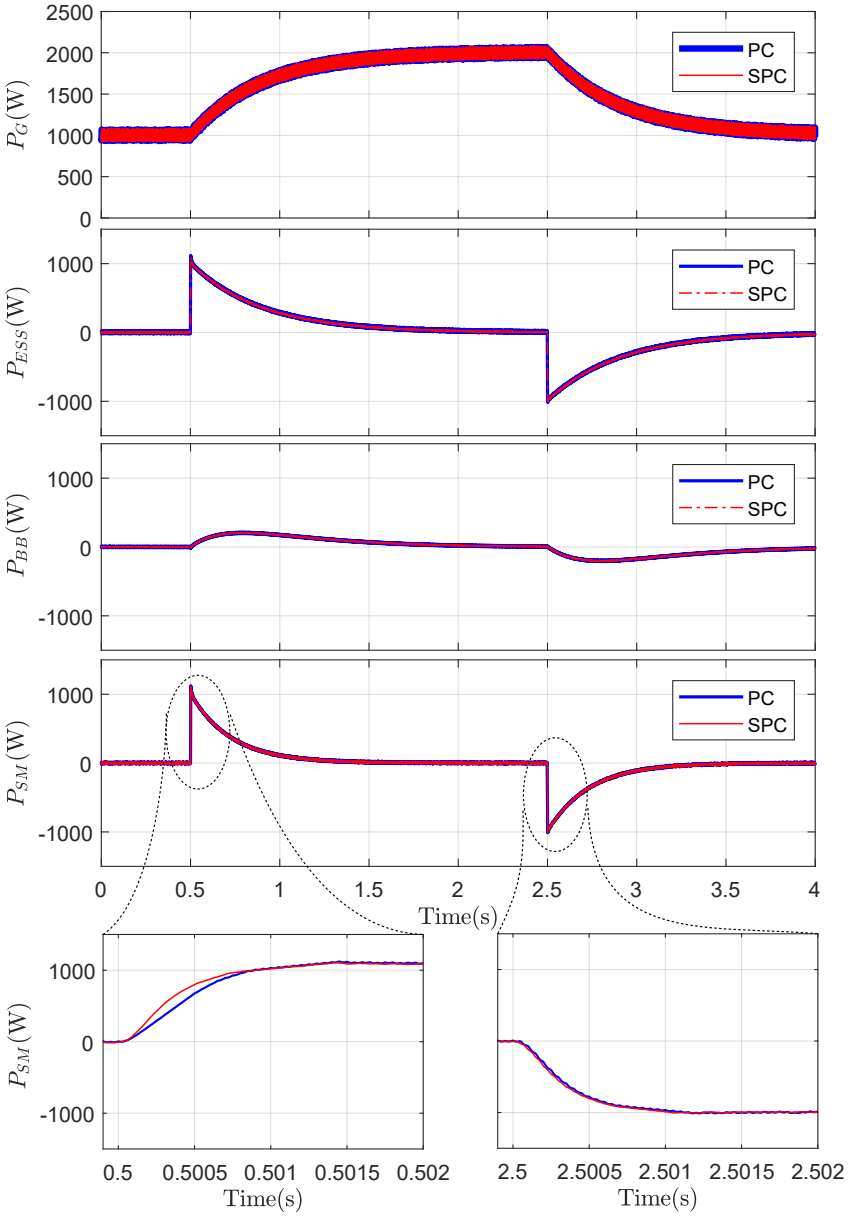


Figure 7-19: Simulation results for the SPC of the two bidirectional buck converters compared to the PC one during the grid-connected mode (Full control strategy) showing the power distribution between the ESSs.

$$\Delta I_{L_2} = \frac{(73.4 - 500)\left(\frac{(\frac{260 + 73.4}{500}) - \frac{260}{500}}{2}\right)}{20000 \times 3.59 \times 10^{-3}} = -0.4361\ A \tag{7.16}$$

By using SPC scheme, a smaller ripple is obtained for the same inductance value at the SM converter. For the SPC scheme, the principal operating waveforms can be seen at

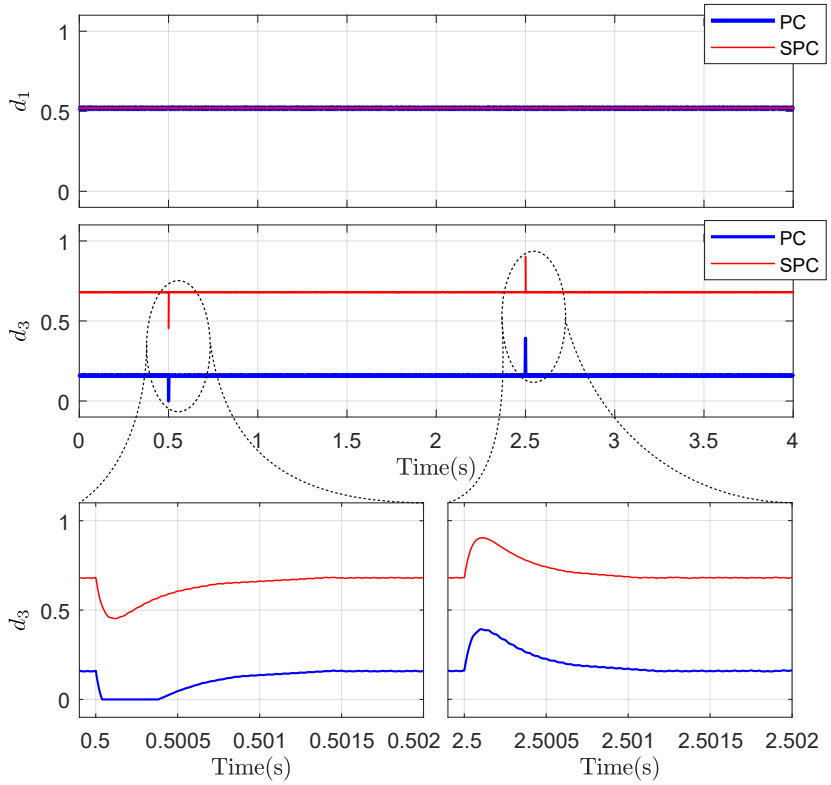


Figure 7-20: Simulation results for the SPC of the two bidirectional buck converters compared to the PC one during the grid-connected mode (Full control strategy) showing the duty cycles of the BB and the SM.

Figure 7-22. As it can be noticed from Figure 7-22 that the peak to peak current ripple of the inductor connected to the BB is 0.4291 A. However, the peak to peak current ripple of the inductor connected to the SM is 0.3021 A for state III, 0.4834 A for the state I and -0.4364 A for state IV. The simulation results match the expected theoretical values. Again, the operation of the steady-state converter is thus demonstrated.

Figure 7-22 shows that the SM converter has a duty cycle very near to the duty cycle of the BB converter. This yields to solve the problem of voltage mismatch and balance the thermal and electrical stresses in the switches.

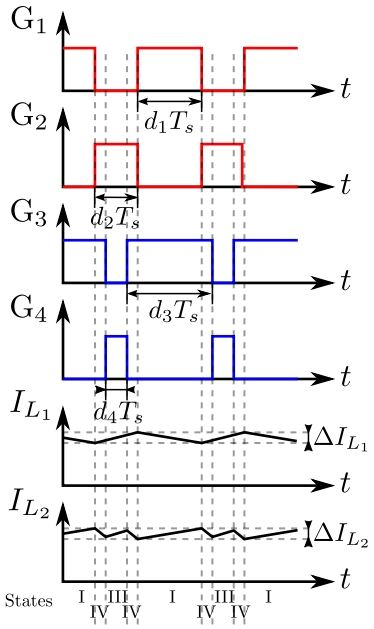


Figure 7-21: Switching states and the inductors' currents of the SPC of two bidirectional buck converters.

7.5 Fault-Tolerant Parallel Connection of the two Bidirectional Buck-Boost Converters

So far, the performance of the SPC scheme has proven to be better than the baseline case for solving issues due to voltage mismatch in the storage ratings. The main limitation of this topology, though, is the behavior during DC bus short-circuit fault. From the discussion carried out in Chapter 5, the buck-boost topology, i.e., the FTPC scheme, stands out as a suitable solution to cope with DC bus short-circuit faults. This section will demonstrate the performance of the FTPC in the healthy operating conditions that were characterized for the cases of PC and SPC. Then, the performance in faulty conditions and the fault ride-through sequence will also be simulated. In any case, the modulation scheme is the two-triangular modulation pattern (Figure 5-23) defined in Chapter 5 for healthy conditions, while the standard operation will be used for fault operation. Finally, the steady-state operation will be analyzed.

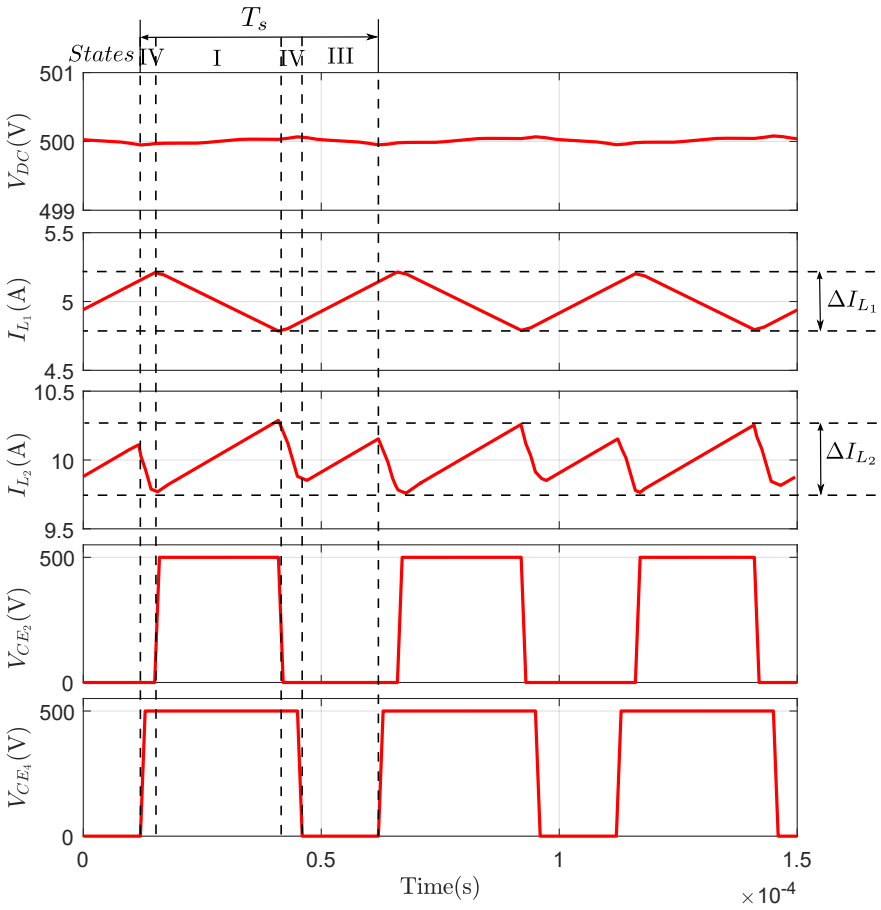


Figure 7-22: Simulation results for the SPC of two bidirectional buck converters where 5 A BB current reference and 10 A SM current reference are applied and the grid VSI controls the DC bus.

7.5.1 Islanding Operation Mode (Healthy Condition)

Figure 7-23 shows that the FTPC of the buck-boost converter presents a perfectly matched performance as the PC of two bidirectional buck converters, as expected.

Again, following the power distribution profiles outlined in the discussion, the SM will take over the fast, transient share of the required load power. It can be noticed in Figure 7-24 that the SM provides/absorbs the same power for the FTPC as well in the case of the PC of two bidirectional buck converter. Also, the BB power (P_{BB}) is the same in any case.

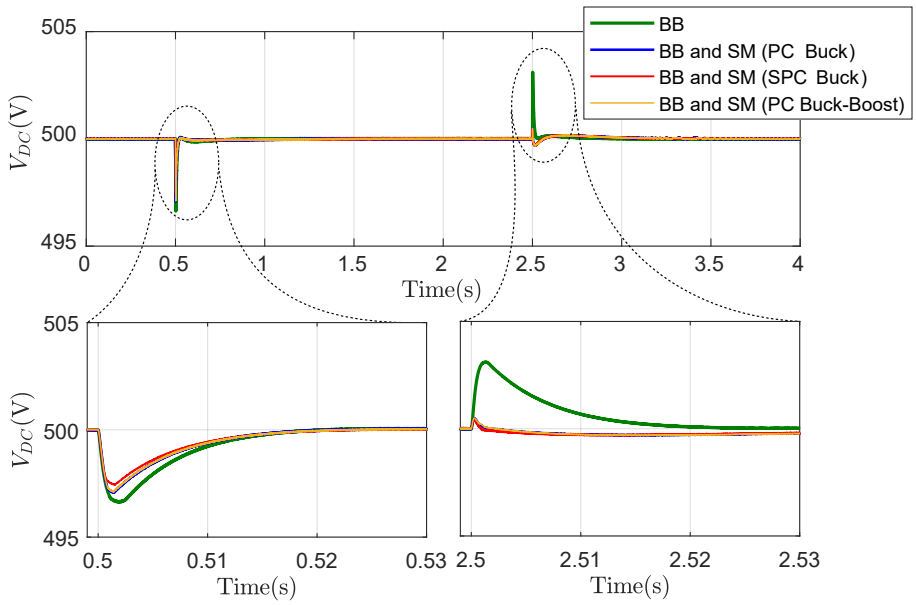


Figure 7-23: Simulation results for the FTPC of the two bidirectional buck-boost converters compared to the PC and SPC of the two bidirectional buck converters and the BB only during the islanding mode in the healthy conditions.

7.5.2 Grid-Connected Operation Mode (Healthy Condition)

Once the islanding condition has been demonstrated, the grid-tied connection is now assessed. Again, both control strategies (the independent control strategy and the full control scheme) are verified. The results of the FTPC of the two bidirectional buck-boost converters are compared with the PC and the SPC of the two bidirectional buck converters in healthy conditions. It must be recalled that in the event of a short-circuit fault at the DC bus is detected, the control changes to islanding mode until the fault is cleared and the DC bus charged again to a safe value. If the fault is permanent, all the PWM will turn off. This will be discussed thoroughly in the dedicated subsection.

7.5.2.1 Independent Control Strategy

The same power step sequence is applied to the FTPC system, in order to obtain comparable results. As it is noticed from Figure 7-25, the DC bus voltage in the PC of two bidirectional buck-boost converters has a similar behavior as the PC of two bidirectional buck converters considering the variation on the DC bus voltage. The power share for this

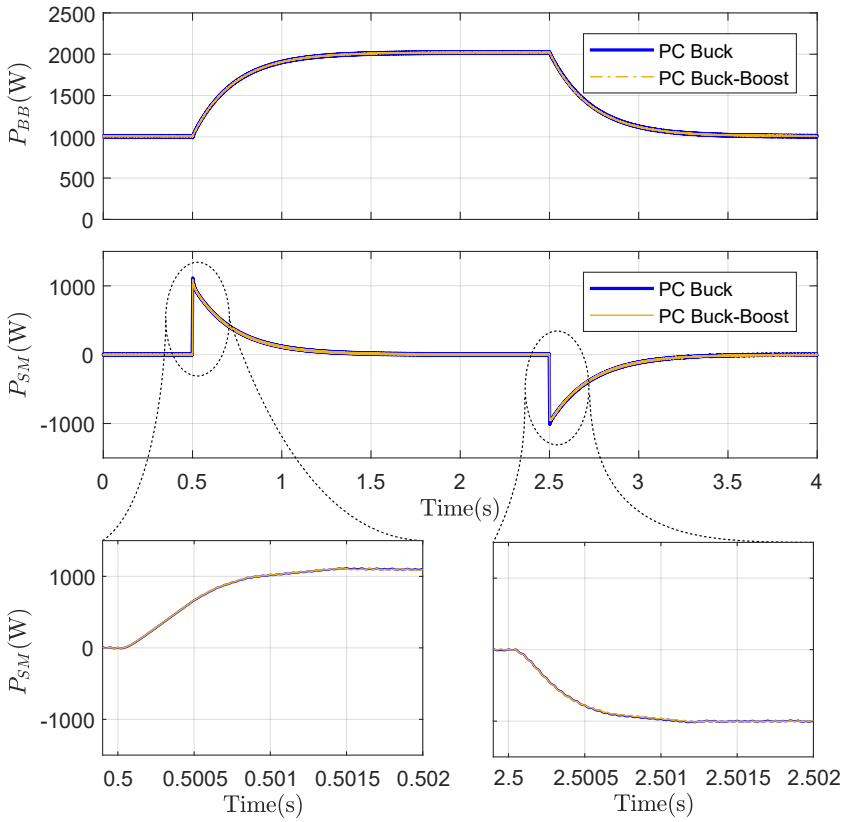


Figure 7-24: Simulation results for the FTPC of the two bidirectional buck-boost converters compared to the PC one during the islanding mode showing the power distribution between the ESSs.

case is depicted in Figure 7-26, where the SM power has the same behavior as the PC of two bidirectional buck converters.

7.5.2.2 Full Control Strategy

In the case of the full control strategy, where the grid VSI control is considered as part of the coordinated control design, the FTPC of the two bidirectional buck-boost converters is compared with the performance of VSI only, the PC and the SPC schemes. The PC of the two bidirectional buck-boost converters has the same performance in the recovery of the DC bus voltage as the PC scheme as depicted in Figure 7-27.

Figure 7-28 shows the power share in the FTPC case. As it can be seen, the power of the grid (P_G) and the BB (P_{BB}) in the FTPC are adequately matched with their corresponding values for the PC and the SPC cases. However, the power of the SM in the FTPC

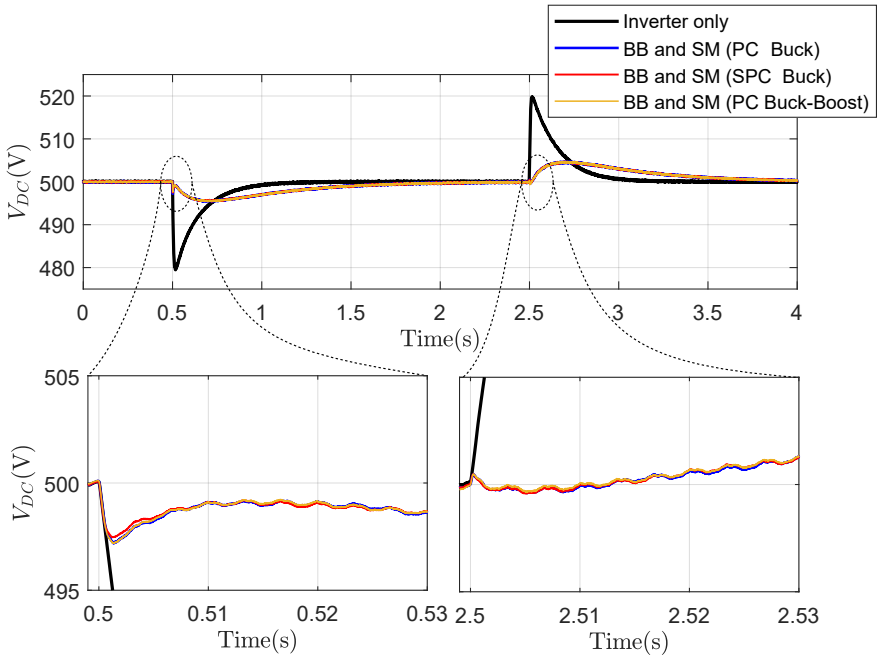


Figure 7-25: Simulation results for the FTPC of the two bidirectional buck-boost converters compared to the PC and SPC of the two bidirectional converters during the grid-connected mode (Independent control strategy) and inverter only.

provides/absorbs power with same dynamics as in the corresponding in the PC as expected.

7.5.3 Steady-State Operation

Again, the performance of the converter in steady-state operation will be checked, by comparing the theoretical and simulated values o the current switching ripples at the inductors of the converter. Because of the BB voltage (V_{BB}) and the SM voltage (V_{SM}) are less than the DC bus voltage, then states I, II, IV, V will occur from Table 5.8 ($V_{CE_1} = V_{CE5} = 0$). At steady-state, the duty of S_2 is greater than the duty cycle of S_6, then the states I, II and V will occur (Figure 7-29).

From Equation (5.10), the inductor voltage of the BB converter is obtained as follows:

$$V_{L_1} = V_{BB} - V_{CE_1} - V_{CE_4} \tag{7.17}$$

$$V_{L_1} = V_{BB} - V_{CE_4} \tag{7.18}$$

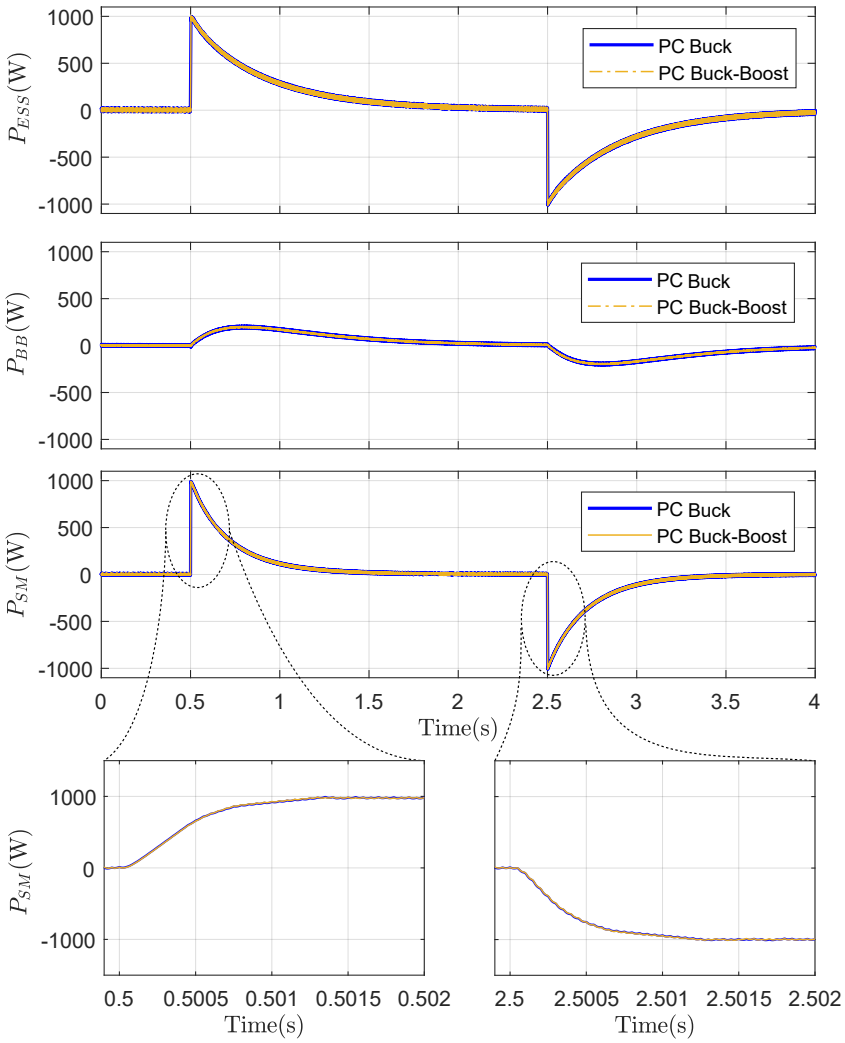


Figure 7-26: Simulation results for the FTPC of the two bidirectional buck converter compared to the PC one during the grid-connected mode (Independent control strategy) showing the power distribution between ESSs.

During T_{on_4}, considering state V (Figure 5-13f), $V_{CE_4} = 0$ and $\Delta T = T_{on\_4} = T_s \cdot d_4 = \frac{1 - d_3}{f_s}$. The current ripple of the inductor connected to the BB is as follows:

$$\Delta I_{L_1} = \frac{V_{BB}(1 - d_3)}{f_s \cdot L_1} = \frac{V_{BB}(1 - \frac{V_{BB}}{V_{DC}})}{f_s \cdot L_1} \tag{7.19}$$

$$\Delta I_{L_1} = \frac{260(1 - \frac{260}{500})}{20000 \times 14.36 \times 10^{-3}} = 0.4345\ A \tag{7.20}$$

During T_{off_4}, considering state I (Figure 5-13a) and state II (Figure 5-13b), $V_{CE_4} =$

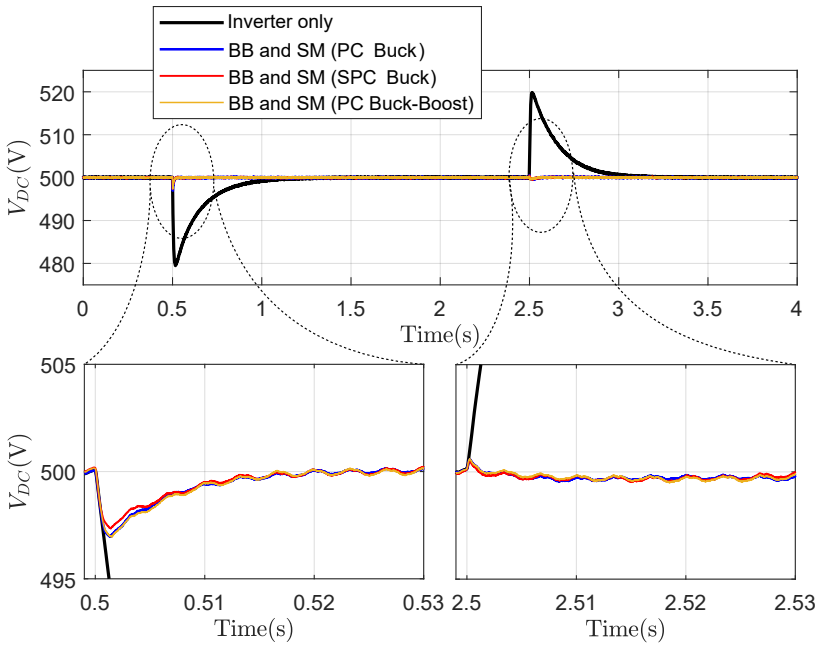


Figure 7-27: Simulation results for the FTPC of the two bidirectional buck-boost converters compared to the PC and SPC of the two bidirectional buck converters during the grid-connected mode (full control strategy) and inverter only.

V_{DC} and $\Delta T = T_{off\_4} = T_{on\_3} = d_3 T_s = \dfrac{d_3}{f_s}$. The current ripple of the inductor connected to the BB is as follows:

$$\Delta I_{L_1} = \frac{(V_{BB} - V_{DC})(d_3)}{f_s \cdot L_1} = \frac{(V_{BB} - V_{DC})(\frac{V_{BB}}{V_{DC}})}{f_s \cdot L_1} \tag{7.21}$$

$$\Delta I_{L_1} = \frac{(260 - 500)(\frac{260}{500})}{20000 \times 14.36 \times 10^{-3}} = -0.4345\ A \tag{7.22}$$

From Equation (5.19), the inductor voltage of the SM converter is obtained as follows:

$$V_{L_2} = V_{SM} - V_{CE_5} - V_{CE_8} \tag{7.23}$$

$$V_{L_2} = V_{SM} - V_{CE_8} \tag{7.24}$$

During T_{on_8}, considering state II Figure 5-13b) and state V (Figure 5-13e), the switch S_8 is closed so the $V_{CE_8} = 0$ and $\Delta T = T_{on\_8} = T_s \cdot d_8 = \dfrac{1 - d_7}{f_s}$. The current ripple of

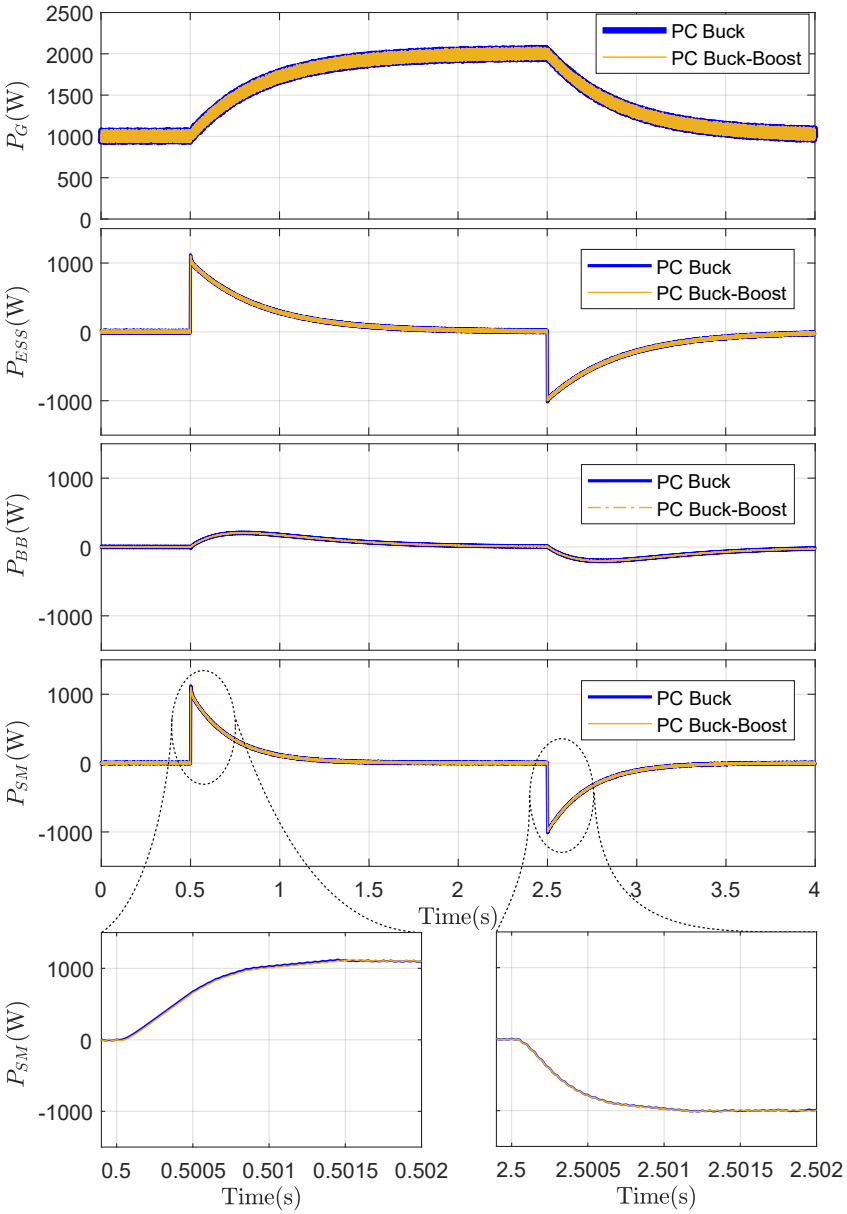


Figure 7-28: Simulation results for the FTPC of the two bidirectional buck-boost converters compared to the PC one during the grid-connected mode (full control strategy) showing the power distribution between the ESSs and the grid.

the inductor connected to the SM is calculated as follows:

$$\Delta I_{L_2} = \frac{V_{SM}(1-d_7)}{f_s \cdot L_2} = \frac{V_{SM}(1-\frac{V_{SM}}{V_{DC}})}{f_s \cdot L_2} \tag{7.25}$$

$$\Delta I_{L_2} = \frac{73.4(1-\frac{73.4}{500})}{20000 \times 3.59 \times 10^{-3}} = 0.8722\ A \tag{7.26}$$

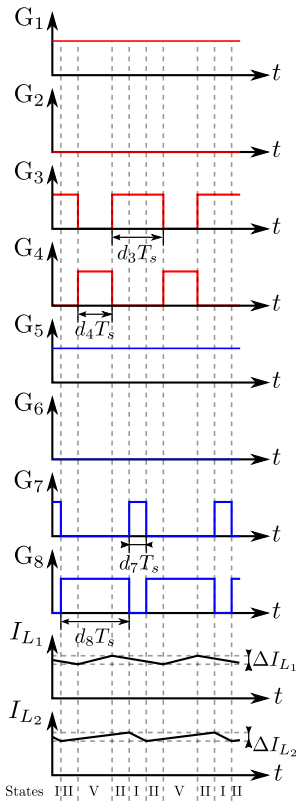


Figure 7-29: Switching states and the inductors' currents of the FTPC of two bidirectional buck-boost converters.

During T_{off_8}, considering state I (Figure 5-13a), the switch S_8 is opened so the $V_{CE_8} = V_{DC}$ and $\Delta T = T_{off\_8} = T_{on\_7} = d_7 \cdot T_s = \frac{d_7}{f_s}$. The ripple current of the inductor connected to the SM is as follows:

$$\Delta I_{L_2} = \frac{(V_{SM} - V_{DC})d_7}{f_s \cdot L_2} = \frac{(V_{SM} - V_{DC})\frac{V_{SM}}{V_{DC}}}{f_s \cdot L_2} \tag{7.27}$$

$$\Delta I_{L_2} = \frac{(73.4 - 500)(\frac{73.4}{500})}{20000 \times 3.59 \times 10^{-3}} = -0.8722\ A \tag{7.28}$$

The current ripples of the inductor connected to the BB and SM in case the FTPC are the same as the ones found for the PC scheme. This is consistent with the expected results, given that the buck-boost converters operate, in steady-state, in buck operation mode. The dual carrier scheme does not affect the current ripples as the duty cycles are correspondingly modified. For the FTPC scheme, the steady-state operation is shown in

Figure 7-30. As it can be seen, the peak to peak ripple current of the inductor connected to BB is 0.4361 A, while the ripple for the inductor connected to the SM is 0.8258 A. The results for the current ripples obtained from the simulation matches the expected theoretical values.

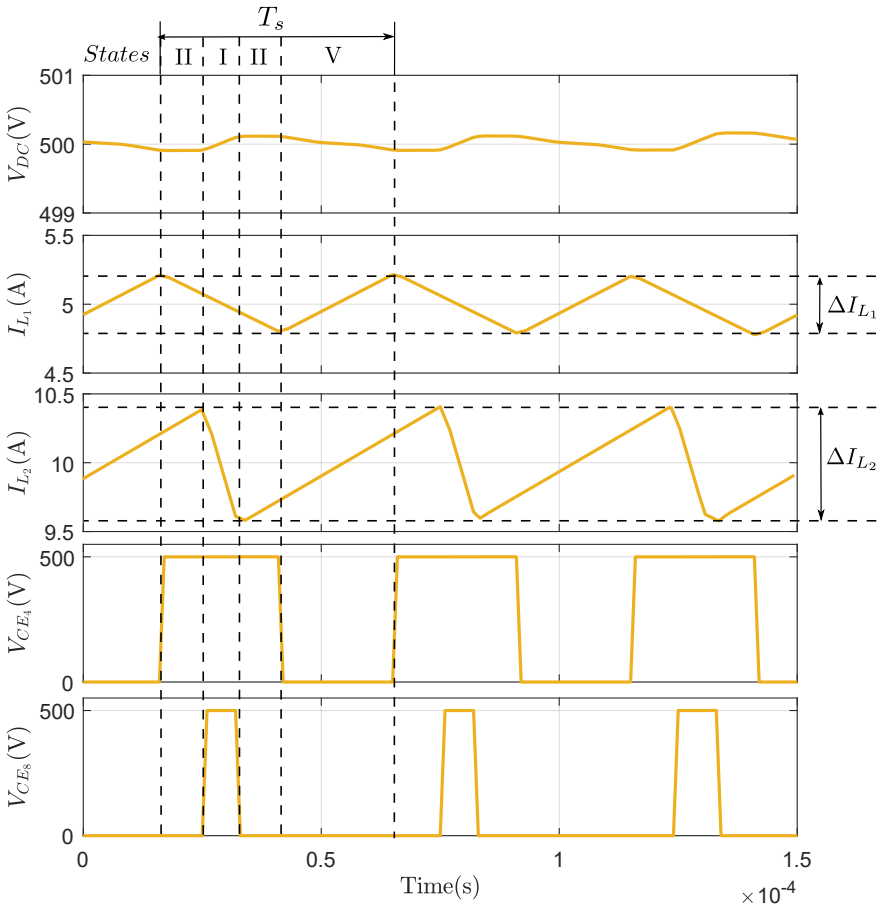


Figure 7-30: Simulation results for the FTPC of the two bidirectional buck-boost converters where 5 A BB current reference and 10 A SM current reference are applied, and the DC bus is controlled by the grid VSI.

7.5.4 Power Losses Calculation of the Switches

Another aspect that was still pending to validate in the FTPC scheme is the comparison of power semiconductor device losses depending on the switching pattern utilized. Special attention has been put on the calculation of the losses in the switches (both conduction and switching losses) during the healthy operation of the converters. The simulations are done

in PLECS® in order to calculate the switching and conduction losses. The parameters and the curves of the IGBT are taken from the datasheet of the 2MBI200HH-120-50 IGBT module from Fuji Electric. The switches losses are divided into conduction losses and switching losses. The conduction and the switching losses of the switches are calculated according to Equations (7.29) and (7.32) as these equations are implemented in PLECS®. For the conduction losses, the following expressions are considered:

$$P_{avg\_cond} = P_{avg\_cond\_IGBT} + P_{avg\_cond\_Diode} \tag{7.29}$$

$$P_{avg\_cond\_IGBT} = \frac{1}{T_s}\int_0^{T_s}(V_{ce}(t)\cdot I_c(t))dt \tag{7.30}$$

$$P_{avg\_cond\_D} = \frac{1}{T_s}\int_0^{T_s}(V_D(t)\cdot I_c(t))dt \tag{7.31}$$

where:

- P_{avg_cond} is the average conduction losses of the switch in Watts,
- $P_{avg\_cond\_IGBT}$ is the average conduction losses of the IGBT in Watts,
- $P_{avg\_cond\_D}$ is the average conduction losses of the anti-parallel diode in Watts,
- V_{ce} is the on-state collector-emitter voltage of the IGBT in Volts,
- Integrated Circuit (IC) Integrated Circuit,
- V_D is the on-state forward voltage of the anti-parallel diode in Volts.

On the other hand, regarding the switching losses, these equations are used:

$$P_{sw} = P_{sw\_IGBT} + P_{rec\_D} \tag{7.32}$$

$$P_{sw\_IGBT} = (E_{on} + E_{off})f_s \tag{7.33}$$

$$P_{rec\_D} = E_{rec}\cdot f_s \tag{7.34}$$

where:

- P_{sw} is the switching losses of the switch in Watts,
- P_{sw_IGBT} is the switching losses of the IGBT in Watts,
- P_{rec_D} is the reverse recovery losses of the anti-parallel diode in Watts,

- E_{on} is the energy loss at IGBT turn on in Joules or Watt-Secs,
- E_{off} is the energy loss at IGBT turn off in Joules Watt-Secs,
- f_s is the switching frequency in Hz,
- E_{rec} is the energy loss of the reverse recovery of the anti-parallel diode in Joules or Watt-Secs.

The calculation of the losses is done for a given set of operating conditions. The converter is working in the steady-state case. The microgrid is operating in grid-connected mode, where the DC is controlled by the grid VSI to a reference voltage of 500 V. The current references for the storage devices are 5 A for the BB and 10 A for the SM are applied. With these conditions, a comparison between the losses in the original PC scheme and the new FTPC topology, both with the standard control (one carrier) and with the proposed control (dual carries), has been carried out.

The results of this comparison are summarized in Table 7.2. It can be seen how the value of the losses (switching and conduction) using the original switching mode in the FTPC are high compared to the original PC scheme. However, the switching losses using the proposed dual carrier control scheme are almost equal compared to the original buck converters, while the conduction losses are higher as S_1 and S_5 are turned on during buck mode. In general, the total losses with the dual carrier scheme are a little bit higher than the original buck converter case.

Table 7.2: The losses in the topologies.

Topology	Conduction Losses (W)	Switching Losses (W)	Total losses (W)
PC Buck	14.68	53.8	68.48
FTPC Buck-Boost (One carrier)	29.7	85.7	115.4
FTPC Buck-Boost (two carriers)	30.09	52.08	82.17

7.5.5 Fault Condition and Performance, and Fault Ride-Through Scheme

A simulation of the fault ride-through capability of the buck-boost converter sketched in Chapter 5 is shown in Figure 7-31. The converters are initially operating under normal control (either grid-tied or islanding control). During the healthy condition, the islanding mode is considered, and the load power is equal to 1 kW.

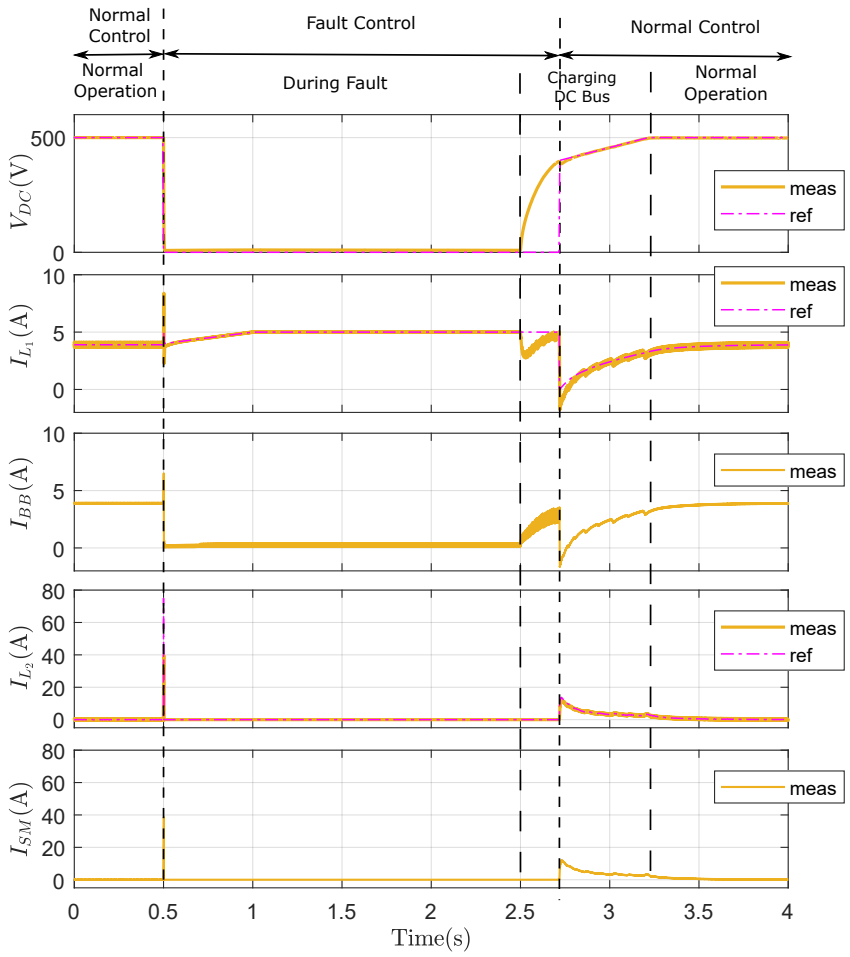


Figure 7-31: Simulation results during fault and normal operation with the proposed control for the FTPC of the two bidirectional buck-boost converters where the fault occurred at 0.5 s and cleared at 2.5 s.

However, when a DC bus fault is detected at 0.5 s (being the fault condition of the DC bus voltage below a 100 V threshold), the converters enter to operate under fault control. In this fault control mode, a given current reference is applied to the BB, while the SM

leg is disconnected. The choice of this current reference is selected employing a trade-off considering the amount of power dissipated and the ability to provide a quick change in the DC bus voltage once the fault is cleared. For convenience, in this case, a reference of 5 A has been selected.

When the fault is removed at 2.5 s, this reference will charge the DC bus to a specific value (400 V threshold in this case). Then, the system is automatically reset to the normal control. The DC bus will continue charging with a ramp until the DC bus reference voltage value and the converter operates in normal mode.

7.6 Conclusions

As a conclusion, it can be demonstrated that the SPC of two bidirectional buck converters solves the problem of the voltage mismatch, balances the thermal and electrical stresses on the switches and provides a symmetric behavior in supplying and absorbing power. However, the FTPC of the two bidirectional buck-boost converters has a fault ride-through capability against DC short circuit faults. The results obtained from simulation will be compared to experimental results from the physical prototype in the following Chapter.

Chapter 8

Experimental Results

Contents

8.1 Introduction

This chapter covers all the experimental verification of the contributions outlined, defined, analyzed and validated through simulations in previous chapters. It starts by defining the power experimental setup characteristics of the laboratory prototypes. Then, it explains the different Printed Circuit Boards (PCBs) designed for i) signal conditioning (measuring the voltages and the currents and scaling and filtering these measurements); ii) sending and receiving the PWM and error (trip-zone) signals through fiber optics wiring between the converter and the controller; as well as iii) adapting these signals to control the IGBT switches. Finally, this chapter shows the results of experiments carried out in the same con-

ditions that in the previous simulations, in order to easily compare the results, to validate the proposed power topologies and control schemes presented in the earlier chapters.

8.2 Experimental Considerations

The following describes the main parameters of the laboratory setup required to provide a platform that allows the experimental verification of the proposals. It also considers requirements from the point of view of the safety.

- The power stage will be implemented with a configurable assembly of switch modules. The switch module is the 2MBI200HH-120-50 from Fuji Electric, as defined in Chapter 6. The main parameters of the switches can be seen in Table 6.7. This module has two IGBTs and two anti-parallel D with each IGBT module representing one leg.

- Figure 8-1 shows the schematics of the power arrangement of the switches. With this scheme, the configuration of the power topology can be easily modified, in order to act as any of the topologies described in this work.

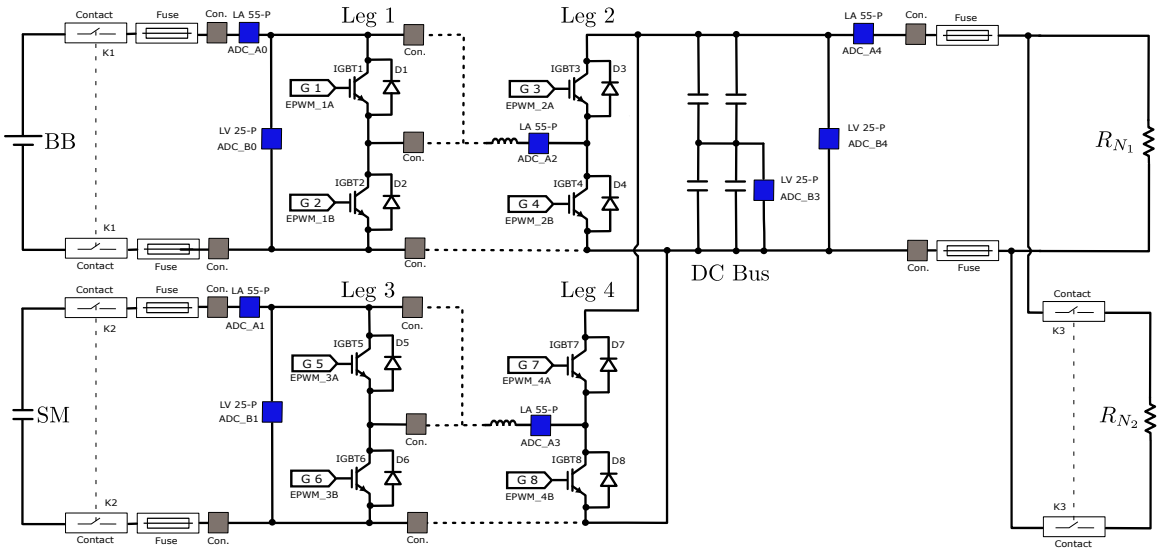


Figure 8-1: Schematic of the experimental setup implemented.

- The inductors and DC bus capacitors implemented have the values specified in Chapter 6.

- Surge arrestors are used to protect the DC bus from overvoltage conditions. In addition, fuses are used to protect from overcurrent.

- A synchronous sampling scheme has been selected for the digital control of the converter. The sampling frequency could be less than or equal the switching frequency ($f_{sa} \leq f_s$). So, it is selected to be equal to the switching frequency which is the maximum allowable sampling frequency.

- The reactive power reference is set to zero ($Q_{G\_ref} = 0$).

- The power ratings of the converters in are 10 kW.

- A sudden load step of $\pm 50\%$, from the storage power reference of 2 kW has been implemented. The step sequence implemented is a change in the power reference from 1 kW to 2 kW at 1 s and then back to 1 kW again at 5 s.

- Again, the same colors defined for the simulation results in Table 7.1 in the previous chapter are kept the same for the experimental results.

8.3 Digital Control and Discretization

The control schemes are implemented in a Digital Signal Processor (DSP), in particular in the TMS320F28335 control card, from Texas Instruments. Therefore, the regulators of the control loops designed in previous chapters, and implemented as continuous PI controllers are transformed to discrete form by using bilinear transformation (Tustin) (Equation (8.1)). The same thing applies to the LPF and HPF filters in the generation of power references for the HESS control scheme.

$$s = \frac{2}{T_s} \frac{z-1}{z+1} \tag{8.1}$$

In order to get the difference equation of PI controller, Tustin transform as discretization

method is applied. By substituting Equation (8.1) into Equation (3.9), it yields to:

$$C(z) = \frac{U^{PI}(z)}{E(z)} = K_p(\frac{\frac{2}{T_s}\frac{z-1}{z+1} + \frac{1}{T_i}}{\frac{2}{T_s}\frac{z-1}{z+1}}) \tag{8.2}$$

All the transfer functions are defined in Chapter 3. A detailed analysis can be found in Appendix B. Then, the difference equation obtained is thus as follows:

$$U[k] = K_p(\frac{T_s}{2}\frac{1}{T_i} + 1)E[k] + K_p(\frac{T_s}{2}\frac{1}{T_i} - 1)E[k-1] + U[k-1] \tag{8.3}$$

where:

- $U[k]$ and $E[k]$ are the present values of the controller and error, respectively,
- $U[k-1]$ and $E[k-1]$ are the values of the controller and error, respectively, obtained in the previous sample.

An anti-windup strategy has been implemented in order to avoid saturation of the controllers. The implemented anti-windup technique is based on a back-calculation scheme. The error is calculated, according to the operating limits, as follow:

$$E[k] = \frac{1}{K_p(\frac{T_s}{2}\frac{1}{T_i} + 1)}U[k] - \frac{K_p(\frac{T_s}{2}\frac{1}{T_i} - 1)}{K_p(\frac{T_s}{2}\frac{1}{T_i} + 1)}E[k-1] - \frac{1}{K_p(\frac{T_s}{2}\frac{1}{T_i} + 1)}U[k-1] \tag{8.4}$$

The same manipulation will be done for the LPF (Equation (3.26) and (3.126)) and for the HPF (Equations (3.73) and (3.75)) that are used for calculating the power references in the HESS control. Thus, by substituting Equation (8.1) into Equations (3.26) and (3.126), the following expressions are calculated:

$$P_{BB\_ref}(z) = \frac{1}{1 + T_{BB\_LPF}(\frac{2}{T_s}\frac{z-1}{z+1})}P_{ESS\_ref}(z) \tag{8.5}$$

$$P_{G\_ss_{ref}}(z) = \frac{1}{1 + T_{G\_LPF}(\frac{2}{T_s}\frac{z-1}{z+1})}P_{O\_ref}(z) \tag{8.6}$$

A detailed analysis of this calculations is given in Appendix B. The difference equations

of the LPF is obtained as follows:

$$\begin{aligned} P_{BB\_ref}[k] = & \frac{\frac{T_s}{2}}{(\frac{T_s}{2}+T_{BB\_LPF})}P_{ESS\_ref}[k] + \frac{\frac{T_s}{2}}{(\frac{T_s}{2}+T_{BB\_LPF})}P_{ESS\_ref}[k-1] \\ & - \frac{(\frac{T_s}{2}-T_{BB\_LPF})}{(\frac{T_s}{2}+T_{BB\_LPF})}P_{BB\_ref}[k-1] \end{aligned} \tag{8.7}$$

$$\begin{aligned} P_{G\_ss\_ref}[k] = & \frac{\frac{T_s}{2}}{(\frac{T_s}{2}+T_{G\_LPF})}P_{O\_ref}[k] + \frac{\frac{T_s}{2}}{(\frac{T_s}{2}+T_{G\_LPF})}P_{O\_ref}[k-1] \\ & - \frac{(\frac{T_s}{2}-T_{G\_LPF})}{(\frac{T_s}{2}+T_{G\_LPF})}P_{G\_ss\_ref}[k-1] \end{aligned} \tag{8.8}$$

where:

- $P_{BB\_ref}[k]$, $P_{ESS\_ref}[k]$, $P_{G\_ss\_ref}[k]$ and $P_{O\_ref}[k]$ are the present values of the BB, the ESS, the steady-state active grid and output power references, respectively, in Watts,

- $P_{BB\_ref}[k-1]$, $P_{ESS\_ref}[k-1]$, $P_{G\_ss\_ref}[k-1]$ and $P_{O\_ref}[k-1]$ are the values of the BB, the ESS, the steady-state active grid and output power references, respectively, obtained in the previous sample in Watts.

Analogously, The difference equation of the HPF of the ESS and the SM is calculated by substituting Equation (8.1) into Equations (3.73) and (3.75):

$$P_{ESS\_tr\_ref}(z) = \frac{T_{ESS\_HPF}(\frac{2}{T_s}\frac{z-1}{z+1})}{1+T_{ESS\_HPF}(\frac{2}{T_s}\frac{z-1}{z+1})}P_{O\_meas}(z) \tag{8.9}$$

$$P_{SM\_tr\_ref}(z) = \frac{T_{SM\_HPF}(\frac{2}{T_s}\frac{z-1}{z+1})}{1+T_{SM\_HPF}(\frac{2}{T_s}\frac{z-1}{z+1})}P_{O\_meas}(z) \tag{8.10}$$

A detailed analysis of this calculations can be found in Appendix B. Finally,the expression of the ESS and SM transient power references, as difference Equations, is obtained as follows:

$$\begin{aligned} P_{ESS\_tr\_ref}[k] = & \frac{T_{ESS\_HPF}}{(\frac{T_s}{2}+T_{ESS\_HPF})}P_{O\_meas}[k] - \frac{T_{ESS\_HPF}}{(\frac{T_s}{2}+T_{ESS\_HPF})}P_{O\_meas}[k-1] \\ & - \frac{\frac{T_s}{2}-T_{ESS\_HPF}}{(\frac{T_s}{2}+T_{ESS\_HPF})}P_{ESS\_tr\_ref}[k-1] \end{aligned} \tag{8.11}$$

$$P_{SM\_tr\_ref}[k] = \frac{T_{SM\_HPF}}{(\frac{T_s}{2} + T_{SM\_HPF})} P_{O\_meas}[k] - \frac{T_{SM\_HPF}}{(\frac{T_s}{2} + T_{SM\_HPF})} P_{O\_meas}[k-1] - \frac{\frac{T_s}{2} - T_{SM\_HPF}}{(\frac{T_s}{2} + T_{SM\_HPF})} P_{SM\_tr\_ref}[k-1] \tag{8.12}$$

where:

- $P_{BB\_ref}[k]$, $P_{BB_ref}[k]$and $P_{ESS\_ref}[k]$ are the present values of the ESS and the SM transient power references and measured power of the load, respectively, in Watts,
- $P_{BB\_ref}[k-1]$, $P_{BB_ref}[k-1]$and $P_{ESS\_ref}[k-1]$ are the values of the ESS and the SM transient power references and measured power of the load, respectively, obtained in the previous sample in Watts.

8.4 Experimental Setup

This section defines the experimental power setup and explains the PCBs designed and used in order to obtain the experimental results.

8.4.1 Power Stage of the Laboratory Setup

The experimental results are done in a 10 kW demonstrator setup shown in Figure 8-2. It shows the two ESSs used: BB and SM, the control cards, the driver boards, the inductors, the DC bus, transducers, contactors and fuses.

8.4.2 Signal Conditioning

For simplicity, all the voltage signals in the physical setup are measured with equal sensors, in particular with LV 25-P voltage transducers from LEM. In the same manner, all the currents are measured using current transducers LA 55-P, also from LEM. Then, the signals coming from the transducers are processed, firstly by a scaling stage that fits the values in the Analog-to-Digital Converter (ADC) range of the controllers, and then by filtering the signal with an anti-aliasing scheme, as shown in Figure 8-3 and Figure 8-4. It must be noticed how the output of both the voltage and current transducers is a current signal.

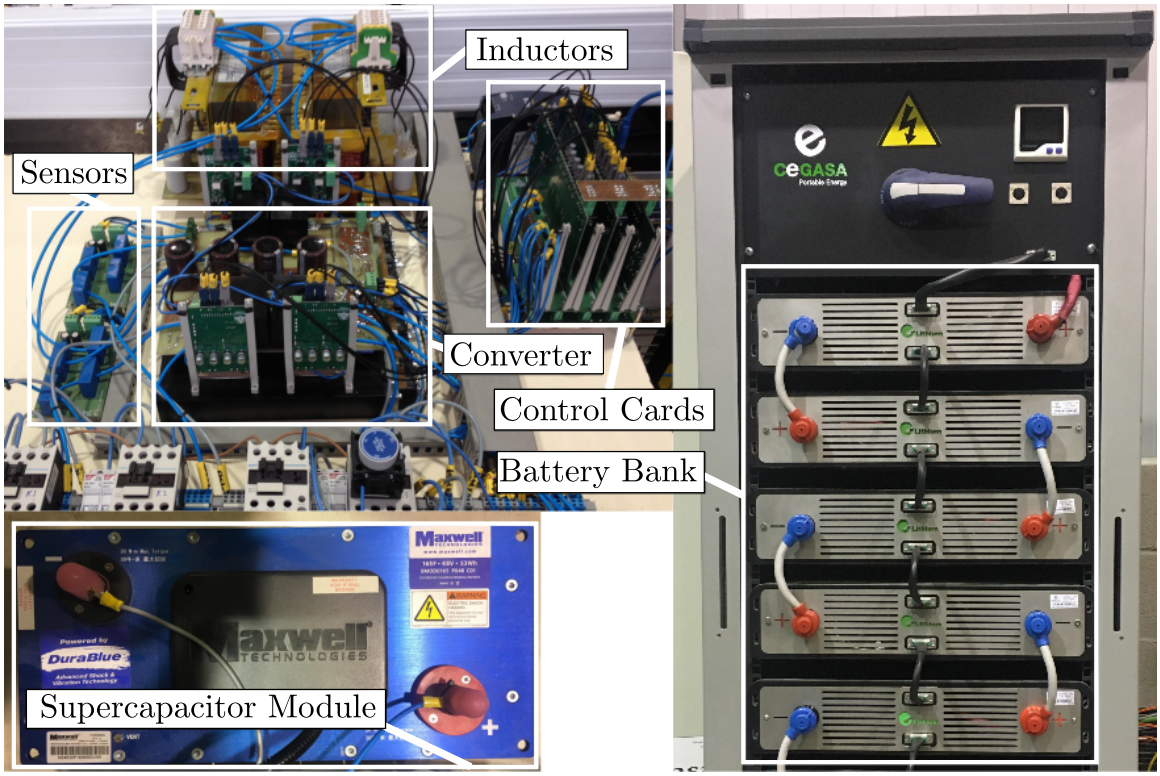


Figure 8-2: Experimental setup of four legs of IGBT modules that can be connected in several configurations (buck, boost, buck-boost converter, etc.).

In the case of the voltage transducer, the primary current of the voltage sensor (I_p^{LV25-P}) shown in Figure 8-3 is calculated as follows:

$$I_p^{LV25-P} = \frac{V_{meas}}{R_1 + R_2} = \frac{(V_{meas}+) - (V_{meas}-)}{R_1 + R_2} \tag{8.13}$$

On the other hand, the primary current of the current transducer (I_p^{LA55-P}) is the same magnitude as the desired measured current, as shown in Figure 8-4:

$$I_p^{LA55-P} = I_{meas} \tag{8.14}$$

These primary currents pass through the ferromagnetic core in the sensor and create a magnetic flux, which is balanced by the magnetic flux created by the secondary current [163]. The output currents of both the voltage or current transducers are the secondary current of the sensors (I_s). These currents depend on the conversion ratio at each transducer

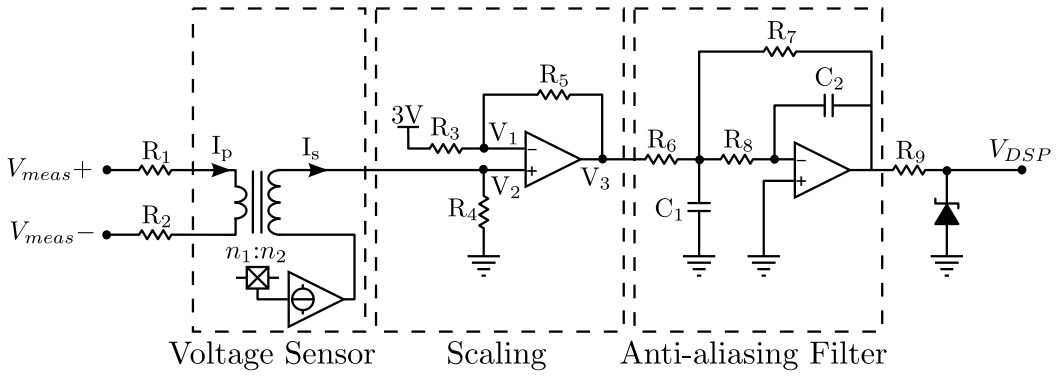


Figure 8-3: Voltage transducer and signal conditioning stages (scaling and filtering).

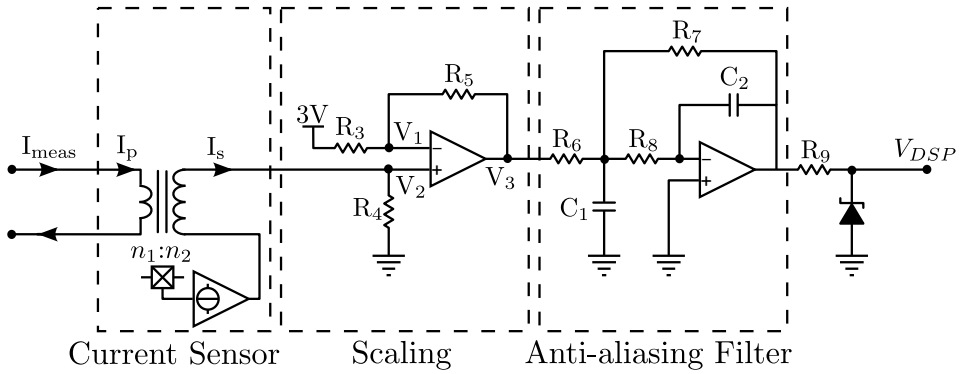


Figure 8-4: Current transducer and signal conditioning stages (scaling and filtering).

as follows:

$$I_s = I_p \frac{n_1}{n_2} \tag{8.15}$$

The parameters of the voltage transducer (LV 25-P) and the current transducer (LA 55-P) are shown in Table 8.1.

The output current (I_s) is converted to a voltage, through Ohm's law, by multiplying by R_4. The value of R_4 depends on the characteristics and type of the measured signals and might be different in case of the voltage and current sensors.

$$V_2 = I_s R_4 \tag{8.16}$$

This V_2 must be scaled to the input values range imposed by ADC at the DSP, which in this case are varied from 0 V to 3 V. This scaling is implemented by using an operational

Table 8.1: Parameters of the voltage and current transducers.

Parameter	Symbol	Value	Unit
Voltage Transducer			
Measured Voltage range	V_{meas}	$\pm$924	V
Primary current range	I_p	$\pm$14	mA
Conversion ratio	$n_1 : n_2$	2500:1000	
Sensor output current range	I_s	$\pm$35	mA
Current Transducer			
Measured current range	I_{meas}	$\pm$70	A
Conversion ratio	$n_1 : n_2$	1:1000	
Sensor output current range	I_s	$\pm$70	mA

amplifier to implement the following linear relationship:

$$V_3 = V_2 \frac{R_3 + R_5}{R_3} - 3\frac{R_5}{R_3} \tag{8.17}$$

Considering that $R_3 = R_5$, then:

$$V_3 = 2V_2 - 3 \tag{8.18}$$

After this scaling scheme, voltage V_3 is filtered. The anti-aliasing filter implemented is a second-order active LPF. The filter response that has been selected is a second order Butterworth LPF, with unity gain. The electronic circuit topology for implementing this filter is Multiple Feedback topology. The input ADC voltage at the DSP (V_{DSP}) is obtained as follows:

$$V_{DSP} = -V_3 \frac{R_7}{R_6} \tag{8.19}$$

R_9 is used to limit the current to the ADC input at the DSP. In addition, the zener diode is used to limit the voltage above 3 V. The parameters of the resistors and capacitors used for the scaling stage and the anti-aliasing filter can be seen in Table 8.2.

Given that the characteristic values of the measured voltages at the BB, the SM and

Table 8.2: Scaling stage and anti-aliasing filter parameters.

R_3	R_5	R_6	R_7	R_8	R_9	C_1	C_2
2 KΩ	2 KΩ	2 KΩ	1 KΩ	1.74 KΩ	47 Ω	27 nF	10 nF

the DC have different ratings, the values of resistors R_1, R_2 and R_4 vary depending on the case, as to ensure an optimal matching between the measuring margins for each device and the resolution of the measurements. These values are shown in Table 8.3:

Table 8.3: Measured voltages ranges.

V_{SM_meas} $R_1 + R_2 = 16.5$ KΩ $R_4 = 100$ Ω	V_{BB_meas} $R_1 + R_2 = 66$ KΩ $R_4 = 100$ Ω	V_{DC_meas} $R_1 + R_2 = 66$ KΩ $R_4 = 50$ Ω	V_2	V_3	V_{DSP}	Bits
99	396 V	792 V	1.5 V	0 V	0 V	0
0	0 V	0 V	0 V	-3 V	1.5 V	2048
-99	-396 V	-792 V	-1.5 V	-6 V	3.0 V	4095

By changing R_4, the measured current range of the BB and the SM changes to increase the resolution as in Table 8.4.

Table 8.4: Measured currents ranges.

I_{BB_meas} $R_4 = 47$ Ω	I_{SM_meas} $R_4 = 22$ Ω	V_2	V_3	V_{DSP}	Bits
31.9 A	68.2 A	1.5 V	0 V	0 V	0
0 A	0 A	0 V	-3 V	1.5 V	2048
-31.9 A	-68.2 A	-1.5 V	-6 V	3.0 V	4095

For a generic design, the cutoff frequency of the anti-aliasing filter (f_{sa}) could be less than or equal the half of the sampling frequency (f_a) ($2f_a \leq f_{sa}$). The parameters of the frequencies are in Table 8.5.

Table 8.5: Parameters of the frequencies.

Parameter	Symbol	Value	Unit
Sampling frequency	f_{sa}	20	kHz
Cutoff frequency of the anti-aliasing filter	f_a	3.5	kHz

8.4.3 Gate Driver Board

The gate driver is another interfacing board between the controller and the power stage. The PWM signals are sent from the DSP dedicated module to the gate driver board, whereas the fault signals, i.e., trip-zone signals, are sent from the driver board to the DSP. This connection is made through fiber optic wires, in order to minimize noise in the connections. The PWM signals of the DSP are from 0 V to 3.3 V. Then, the driver board receives the PWM signals, after the opto-couping stage, ranging from 0 V to 5 V. The IGBTs switches are turned on and off with a gate-to-source voltage (V_{GE}) values of 15 V and -15 V, respectively. Therefore, the driver board adapts these signals and also isolates the gating references between the upper IGBT and the lower one. On the other hand, the driver board sends the trip zone signals to the DSP back through the fiber optic cables. The driver I_c used is the ACPL-333J from AvaGO Technologies. The driver board schematic is shown in Figure 8-5.

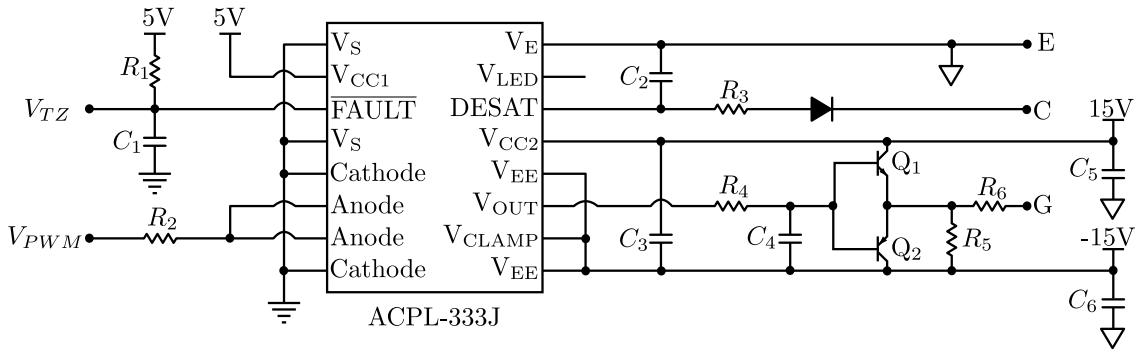


Figure 8-5: Driver Board Scheme.

The anode of the optocoupler is connected to the PWM signals. R_2 is limiting the current which is passing from the anode to the cathode of the optocoupler input LED. The

fault signal is sent to the trip zone input of the DSP. This fault output at the driver is an open collector; therefore, it is connected to a pull-up resistance R_1. The fault pin changes from a high impedance to a logic low output when the voltage on the DESAT pin exceeds an internal reference voltage of 6.5 V while the IGBT is on. C_1 is used to maintain the voltage fixed against noise spikes. In order to increase the gate current, two NPN (Q_1) and PNP (Q_2) transistors are added in a complementary stage. R_5 is a pull-down resistance to maintain the IGBT turned off in case there is no output from V_{OUT}. R_6 is the gate resistance which depends on the IGBTs used. R_4 limits the current to the bases of the transistors. C_2, C_3, C_4, C_5 and C_6 are used to maintain the voltage level fixed and provide the peak current. The parameters of the resistors and capacitors of the driver board are in Table 8.6.

Table 8.6: Driver parameters.

R_1	R_2	R_3	R_4	R_5	R_6
2 KΩ	430 Ω	100 Ω	10 Ω	47 KΩ	2 Ω
C_1	C_2	C_3	C_4	C_5	C_6
330 pF	100 pF	100 nF	10 nF	100 nF	100 nF

The implemented dead time between the upper and lower switches, programmed in the PWM module of the DSP, must ensure that the short circuit between the upper and lower switches, and hence cross-conduction in the IGBT leg is prevented.

8.5 Outline of the Experimental Results

With the experimental setup shown in the previous section, a set of experiments has been carried out, in order to validate the simulations carried out in Chapter 7. The experiments are done for the three main topologies involved; the baseline case (PC of the bidirectional buck converters), the SPC scheme, and the FTPC based in the buck-boost bidirectional converter. Initially, the behavior at islanding mode is evaluated. Then, the performance in grid-connected operation mode is assessed, for both the independent storage and full control strategies, for the three mentioned topologies. Finally, the operation of

the FTPC upon a DC bus fault is experimentally validated.

8.6 Baseline Case: Parallel Connection of the two Bidirectional Buck Converters

This section covers the experiments carried out to verify the operation of the PC scheme of the bidirectional buck converters. The PC is the baseline case to be compared with the other cases.

8.6.1 Islanding Operation Mode

The results obtained by simulation will be repeated to validate the proposed topology and the defined control schemes. In this mode, the DC bus is controlled to track a reference of 500 V. The SM provides/absorbs the peak transient power and the BB provides/absorbs the steady-state power. The load is changed at 1 s from 1 kW to 2 kW and at 5 s is changed again to 1 kW. Figure 8-6 shows the performance by using BB only (green line) and the by using BB and SM in the PC scheme (blue line). It is fully matched with Figures 7-2 and 7-3 from simulations. It is noticed that the BB is providing/absorbing the steady-state power while the SM is providing/absorbing the peak power as expected for the implemented control design.

8.6.2 Grid-Connected Operation Mode

After the islanding mode is validated, the grid-connected mode is targeted. As it has been discussed earlier, two control schemes are implemented, i.e., the independent storage control strategy and the full control strategy.

8.6.2.1 Independent Control Strategy

In this control, the DC bus voltage is controlled by a VSI connected to the grid in order to maintain the DC bus voltage tracking the 500 V reference. In turn, the SM is providing or absorbing the transient peak power, while the BB takes over the rest of the transient

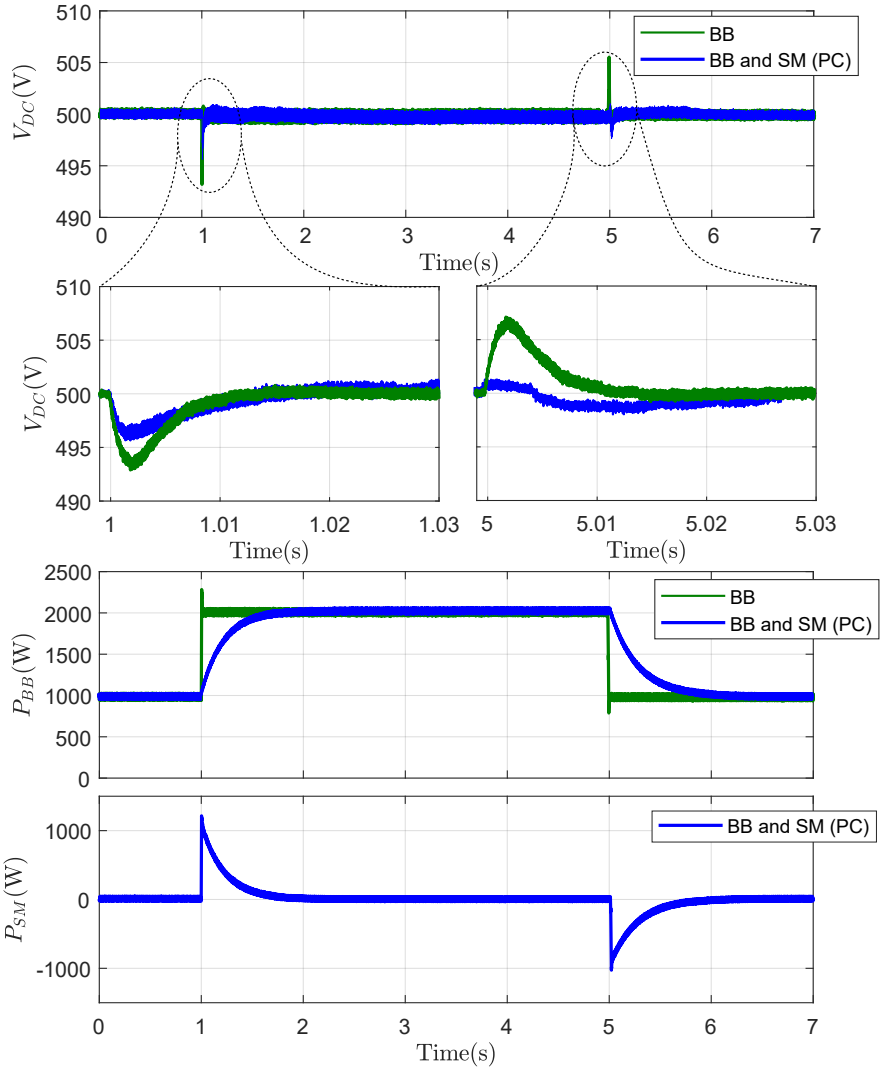


Figure 8-6: Experimental results for the BB only and the HESS (BB+SM) during the islanding mode.

power. Figure 8-7 shows that the DC bus is recovered very fast with using ESS (blue line) compared to the inverter only (black line). Figure 8-7 matches the simulation results at Figures 7-4 and 7-6.

8.6.2.2 Full Control Strategy

This control keeps the same DC bus voltage control reference of 500V. But in this case, the control scheme includes this outer loop within a full control design scheme. Again, the grid is providing/absorbing the steady-state power, the SM is providing/absorbing the peak transient power and the BB is providing/absorbing the transient power. Figure 8-8 shows

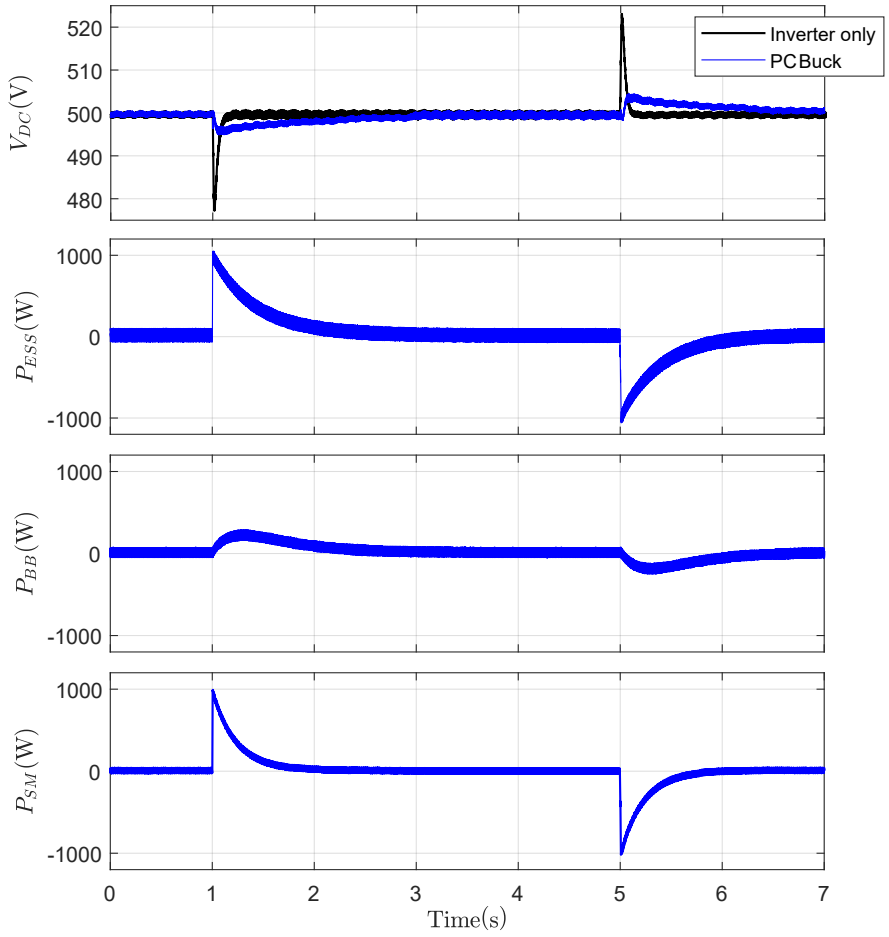


Figure 8-7: Experimental results for the inverter only and the PC of the two bidirectional buck converters during the grid-connected mode (Independent control strategy).

the DC bus has a fast recovery by using the ESS (blue line) compared to the inverter only (black line). Figure 8-8 matches the simulation results at Figures 7-7 and 7-9.

8.6.3 Steady-State Operation

Considering the DC bus voltage is controlled by the grid VSI to maintain the DC bus voltage around 500 V. A 5 A BB current reference and 10 A SM current reference are applied. As shown in Figure 8-9, the collector-emitter voltage of IGBT$_2$ (V_{CE_2}) and the collector-emitter voltage of IGBT$_4$ (V_{CE_4}) are representing the duty cycles of the BB and SM, respectively. The duty cycle of SM in PC is a very small value compared to the duty cycle of the BB as in Figure 8-9. It can be appreciated how the duty cycle of the switches reaches extreme values. This yields to the aforementioned operational and design

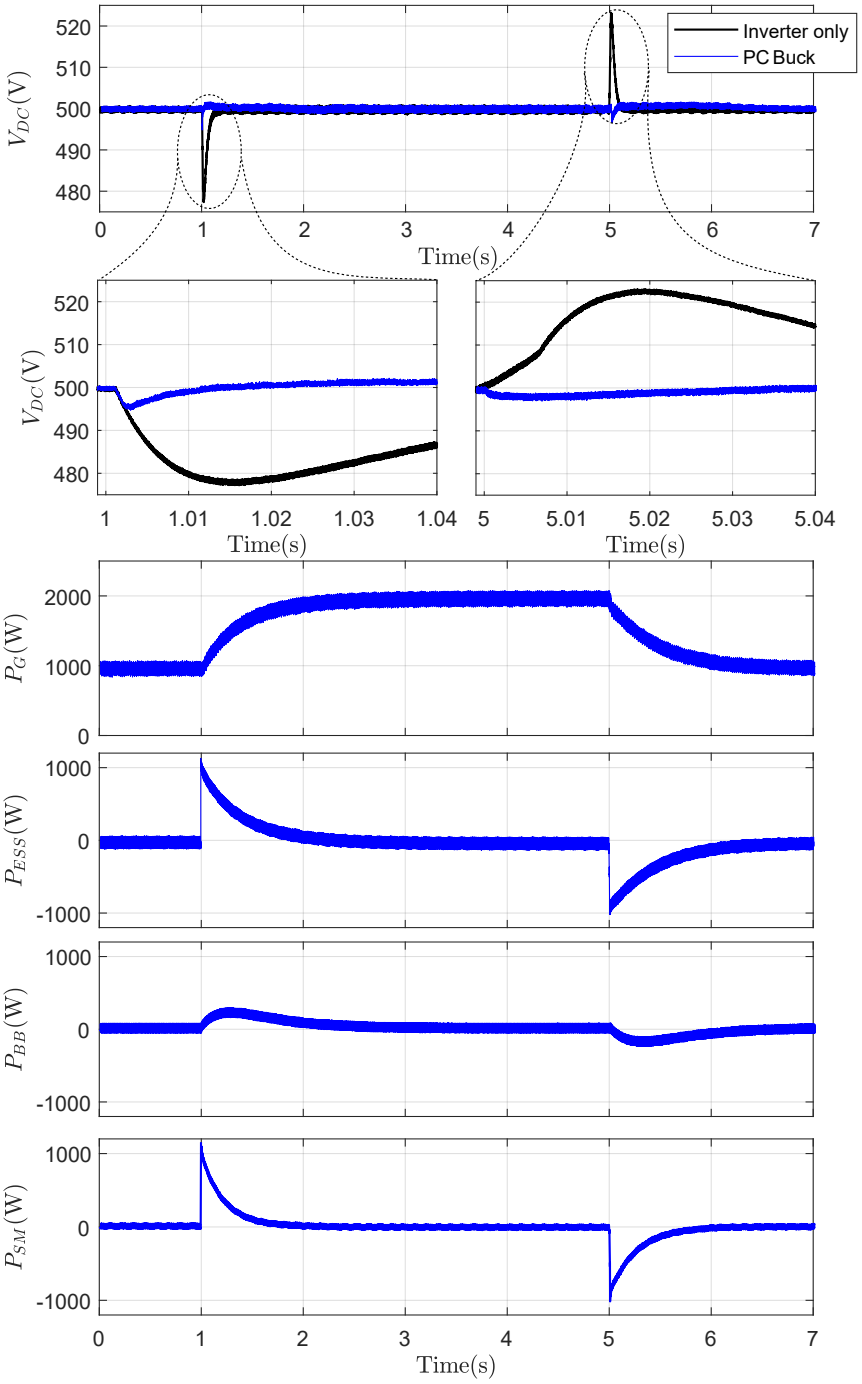


Figure 8-8: Experimental results for the inverter only and with HESS for the PC of two bidirectional buck converters during the grid-connected mode (Full control strategy).

limitations.

As it can be noticed from Figure 8-9, the peak to peak ripple current is 0.407 A for the inductor connected to the BB and 0.757 A for the inductor connected to the SM. These

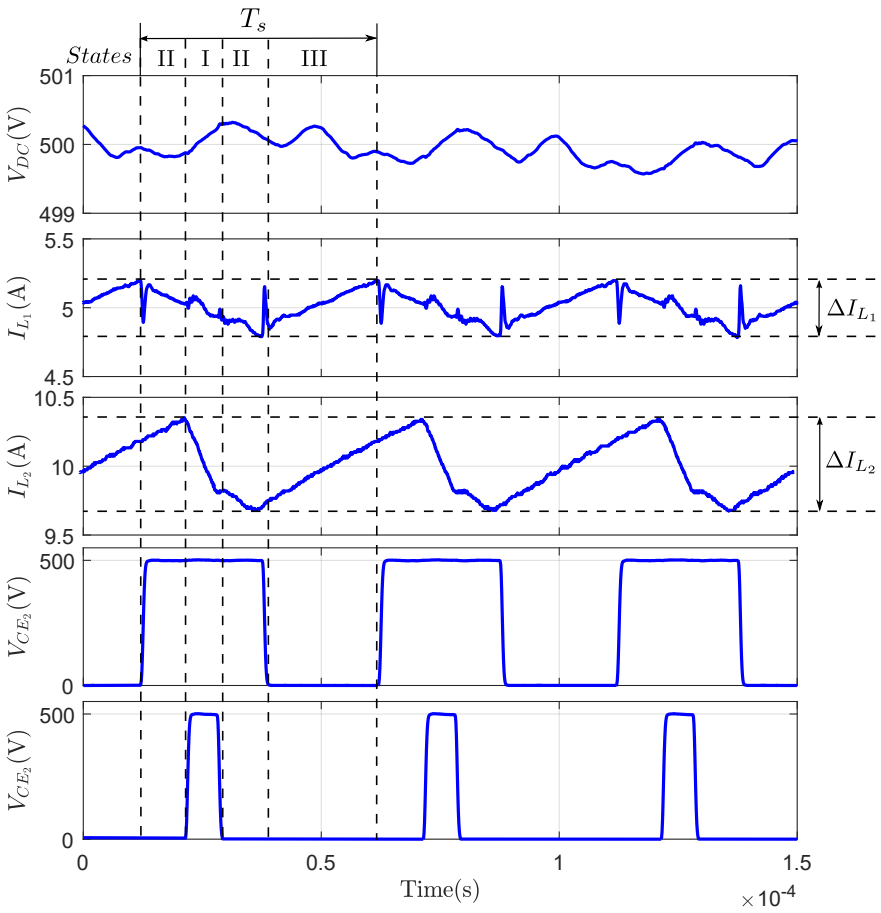


Figure 8-9: Experimental results for the PC where 5 A BB current reference and 10 A SM current reference are applied, and the DC bus is controlled by the grid VSI.

results match with the theoretical results and the simulation derived in Chapter 7.

As mentioned, the dynamic performance is also significantly affected by the extreme duty cycle values in the SM leg, which are very close to the 0–100% physical limits. Considering an abrupt negative step in the SM current demand (I_{SM_ref}), then the control stage must generate a control action in the duty cycles that provide the actual SM current equal to the reference value. However, the available control actions range from $d_3 = 14\%$ to $d_3 = 0\%$, which ultimately implies S_3 and S_4 continuously turned off and on, respectively. This condition implies that the SM inductance (L_2) is discharged with the relatively small voltage at the SM (V_{SM}) thus implying a limitation in the rate of decrease of the SM current. This aspect penalizes the discharging dynamics enormously, also introducing a non-symmetric behavior in the system performance. Indeed, for the opposite case (charging current), the

extreme operation in the control action would imply a charging voltage of the DC bus (V_{DC}), and the rate of charge results dramatically increased.

This situation is illustrated in Figure 8-10, where a series of alternate steps in the SM current reference, from 10 A to -10 A and vice-versa, are provided to the system. It can be seen how, at the beginning of the charging step (i.e., SM current changing from -10 A to 10 A), the modulation temporarily stops, as (d_3) results clamped to 0%. Therefore, the demanded control action would drop to negative values, yielding to an impossible operating constraint. On the other hand, for the discharging step (-10 A to 10 A), the control action can be provided by the system without constraints. Thus, the non-symmetrical performance of the system is demonstrated. Notice that this effect would take place even if the switches are considered ideal. In the following subsection, it will be demonstrated that by using the SPC scheme yields to a symmetric behavior in charging and discharging.

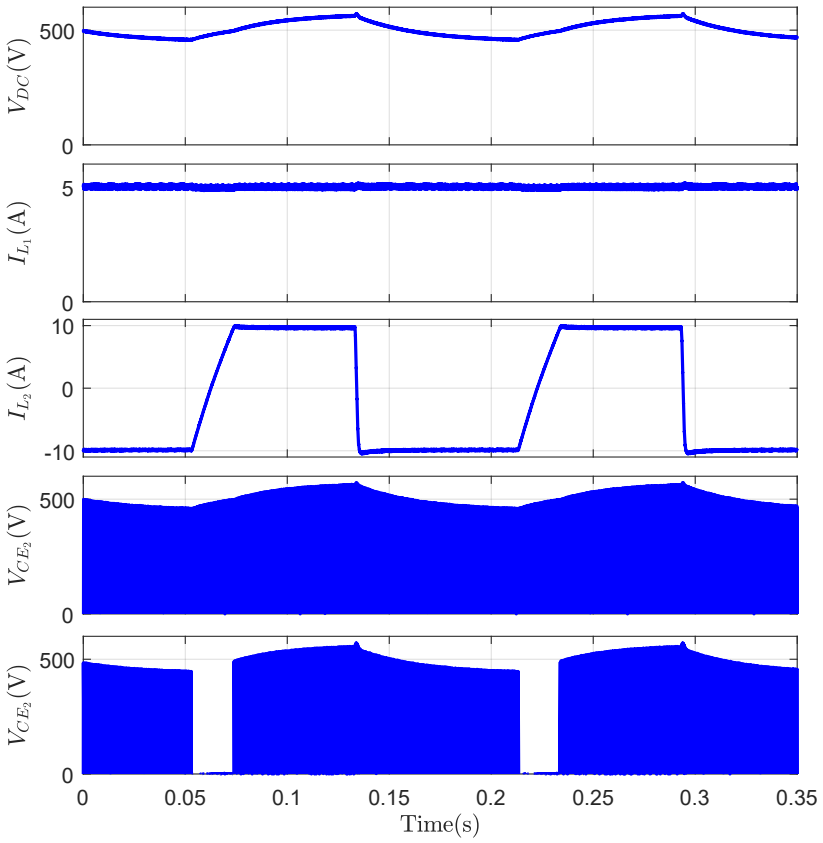


Figure 8-10: Experimental results of the PC scheme, for I_{SM} steps from 10 A to -10 A, and the DC bus is controlled by the grid VSI.

8.7 Series-Parallel Connection of the two Bidirectional Buck Converters

After the baseline case has been validated, the SPC scheme will be assessed. This scheme aims to cope with the functional problems identified by a large mismatch between storage unit voltage ratings and the DC bus voltage. Initially, the dynamic behavior of the system will be tested. After that, the switching waveforms at the converter will be assessed, in order to validate the claims on the variations of the resulting duty cycles in the converters.

8.7.1 Islanding Operation Mode

Again, the DC bus voltage is controlled to target the 500 V reference, in this case utilizing an external controller. As it can be seen from Figure 8-11, the experimental results match pretty well the simulations in Figures 7-11 and 7-12 as well as the expected behavior. The voltage drop with the proposed control scheme for the SPC configuration is smaller than for the standard PC case as shown in Figure 8-11. The BB provides/absorbs the steady-state power while the SM delivers/absorbs the transient power in order to increase the lifetime of the BB.

Therefore, the implemented control system has been experimentally validated for the system under consideration. It must be noticed how the proposed SPC configuration and control scheme does not imply any extra component than the base PC scheme, and therefore the enhancement in the performance is obtained at no cost.

8.7.2 Grid-Connected Operation Mode

In the same manner, the following conditions to test are the ones the resemble the grid-tied operating conditions. In order to do this, a VSI converter has been attached to the DC bus voltage to provide the ability to implement the PCC grid converter.

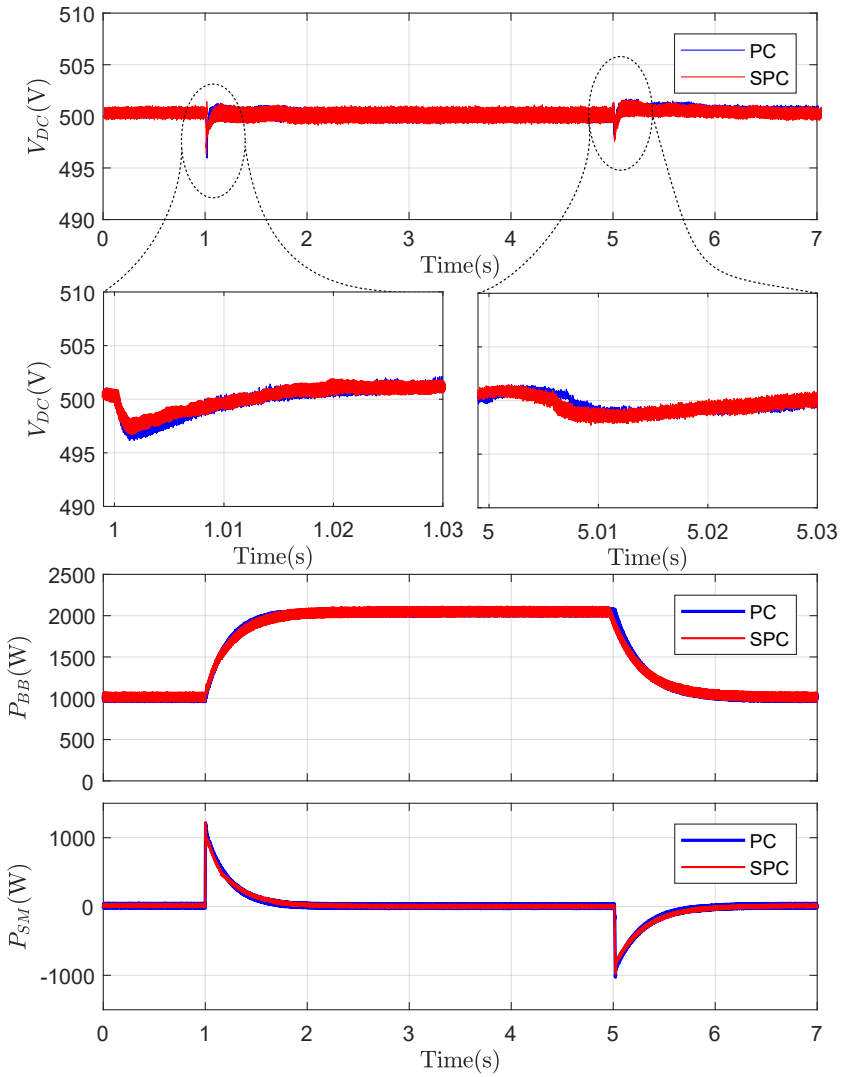


Figure 8-11: Experimental results for the SPC of the two bidirectional buck converter compared to the PC one during the islanding mode.

8.7.2.1 Independent Control Strategy

A comparison of the performance of both the SPC and the baseline case (PC), for the independent control strategy in the grid-tied operation mode, is depicted in Figure 8-12. It matches the simulation results at Figures 7-15 and 7-26. The SM provides/absorbs the transient peak power and the BB supplies/absorbs the rest of the transient power.

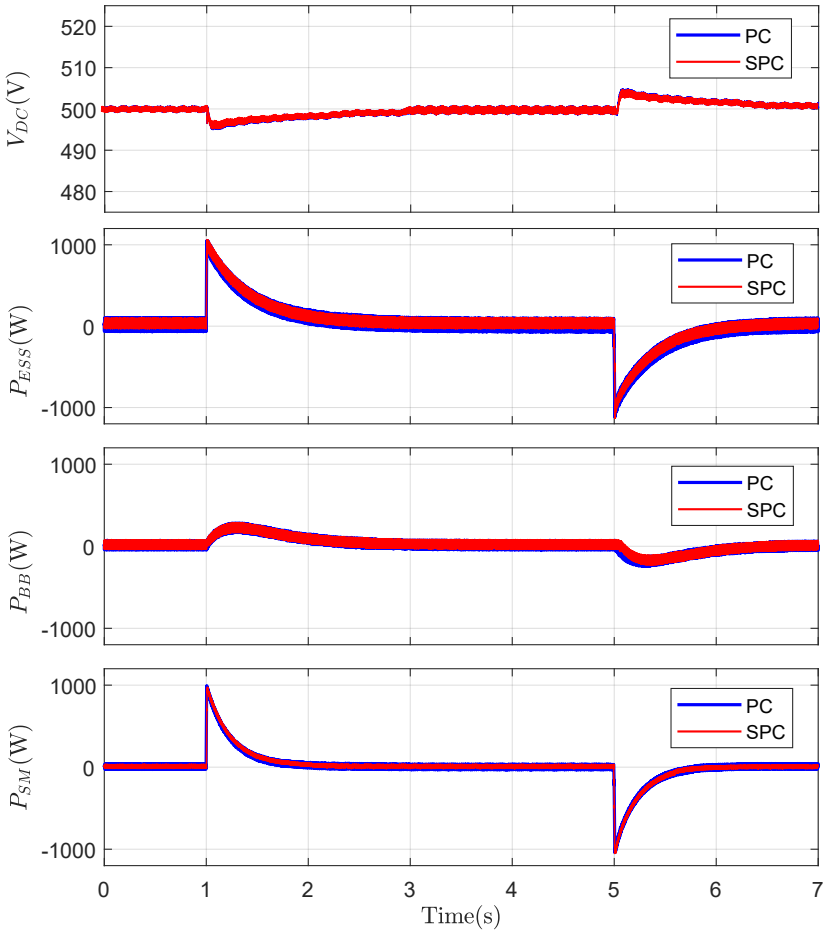


Figure 8-12: Experimental results for the SPC of the two bidirectional buck converter compared with the PC one during the grid-connected mode (Independent control strategy).

8.7.2.2 Full Control Strategy

The SPC of the two bidirectional buck converters is compared with the base case PC of the two buck converters as depicted in Figure 8-13. Again, it can be seen how Figure 8-13 matches the simulation results at Figures 7-18 and 7-19. The grid provides/absorbs the steady-state power while the SM delivers/absorbs the transient peak power, and the BB supplies/absorbs the rest of the transient power.

8.7.3 Steady-State Operation

In order to demonstrate the merits and the feasibility of the SPC, the steady-state operation will be validated, considering the current ripples involved. In Figure 8-14, the duty

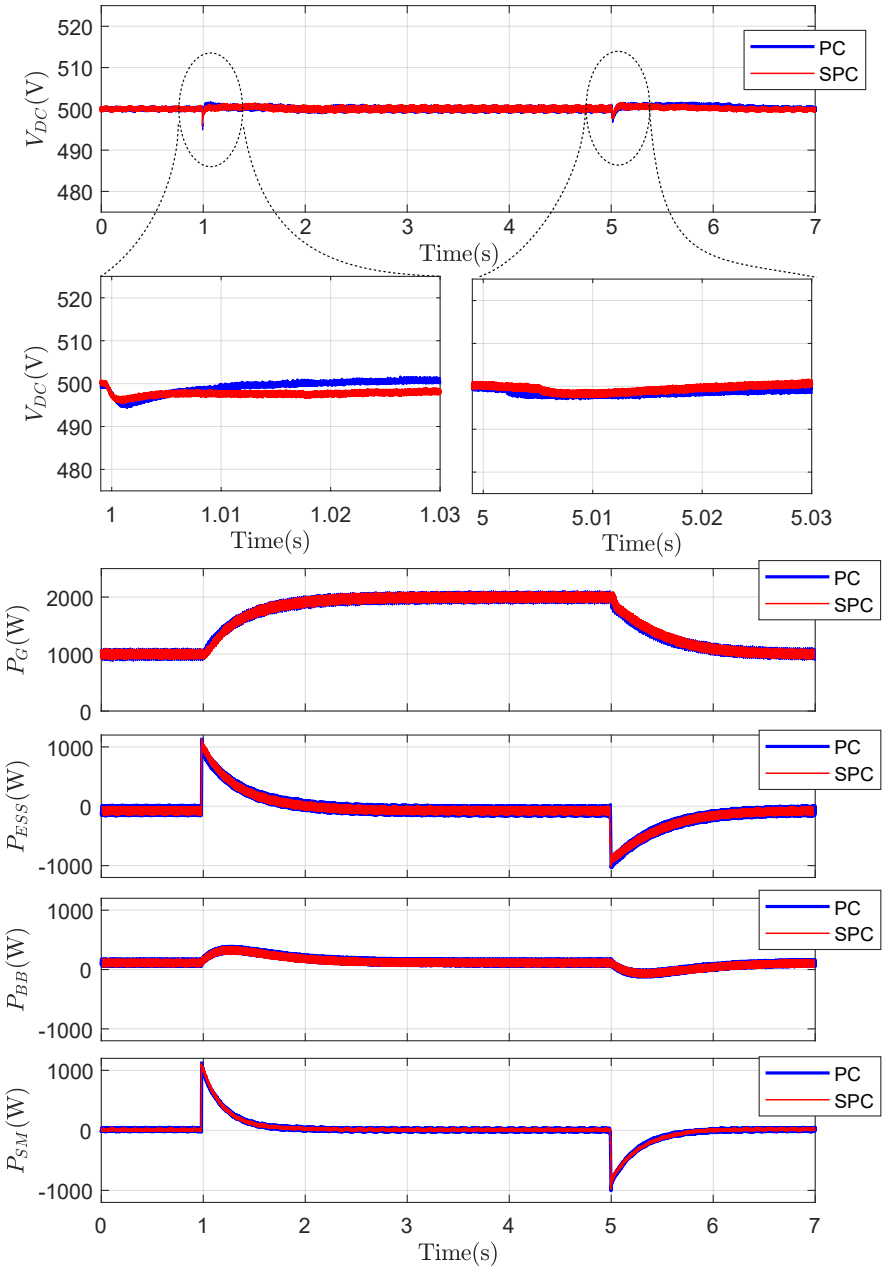


Figure 8-13: Experimental results of the SPC of the two bidirectional buck converter compared with the PC one during the grid-connected mode (Full control strategy).

cycle of the SM converter is slightly higher than the duty cycle of BB converter. This yields to decrease the thermal and electrical stresses and increasing the lifetime of the IGBTs, thus contributing to solve the problems derived from the voltage mismatch. From Figure 8-14, the peak to peak current ripple is 0.358 A for the inductor connected to the BB. However, the peak to peak ripple current is 0.212 A (state III), 0.382 A (state I) and -0.3194 A (state

IV). It can be thus verified how these results match the theoretical and simulation results for this scheme presented in Chapter 7.

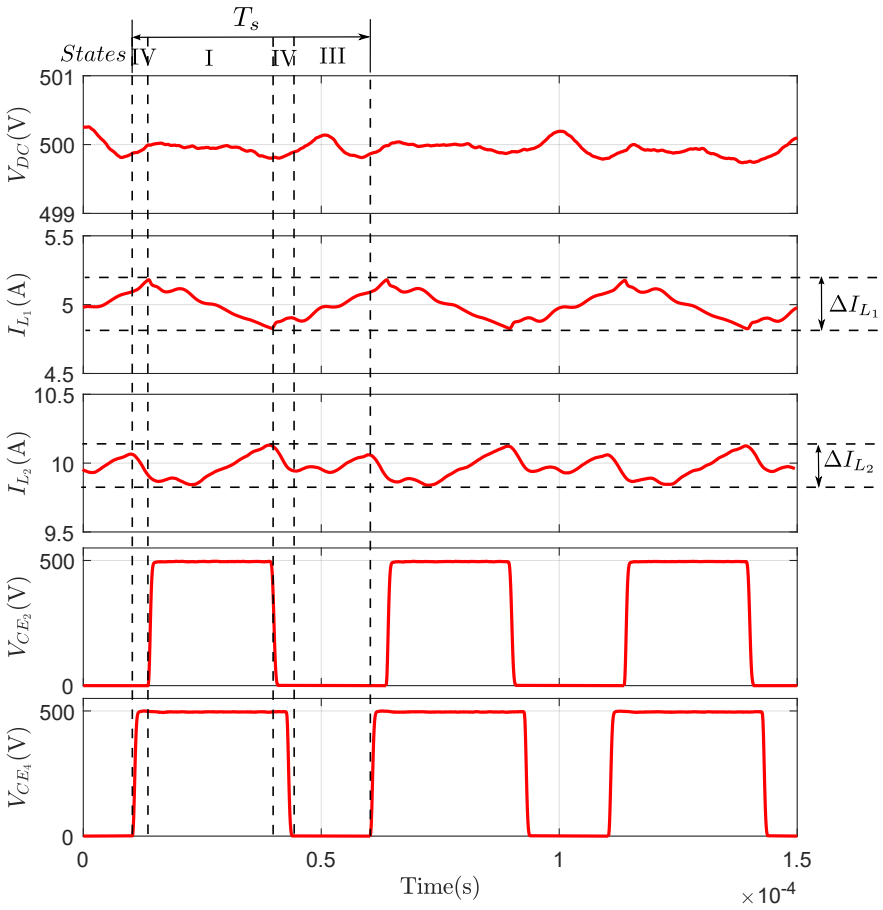


Figure 8-14: Experimental results for the SPC where 5 A BB current reference and 10 A SM current reference are applied, and the DC bus is controlled by the grid VSI.

But the key aspect of the SPC scheme is that now, the control action at the SM is not clamped in such a dramatic manner as in PC, and therefore a better dynamic performance is expected. Moreover, the behavior is also expected to be symmetric, as discussed in previous chapters. To illustrate these last assertions, Figure 8-15 shows a series of symmetric $\pm$10 A consecutive bidirectional current steps for the SPC connection. As it can be seen, and given that the control action can reach negative values in a natural manner, the modulation is never interrupted in the SPC operation, unlike the case of the PC.

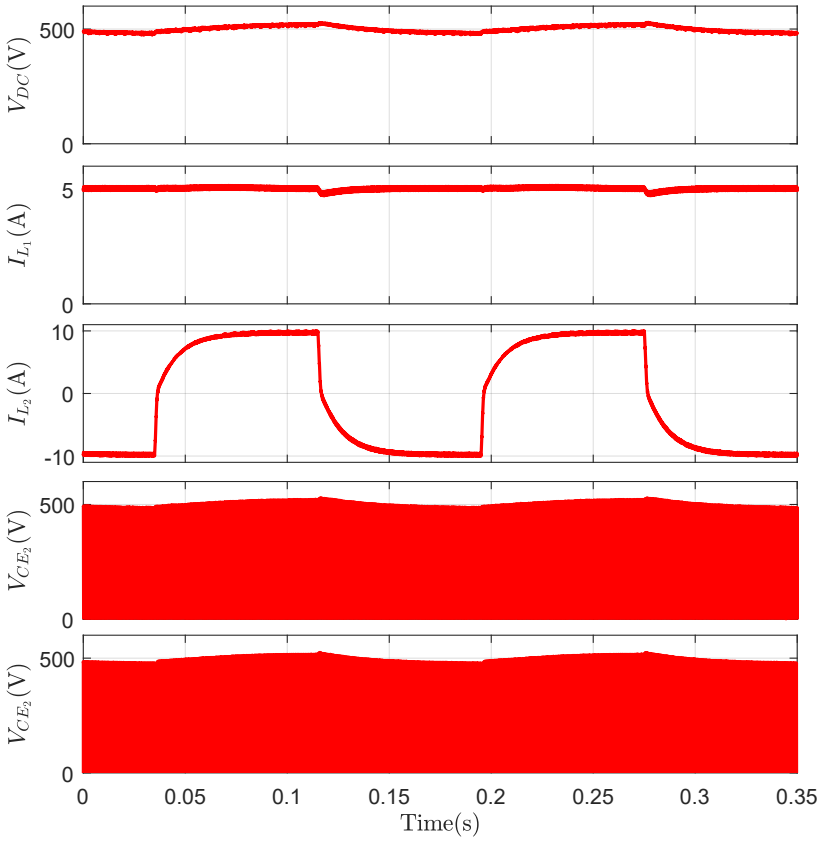


Figure 8-15: Experimental results of the SPC scheme, for I_{SM} steps from 10 A to -10 A, and the DC bus is controlled by the grid VSI.

8.7.4 Power Losses Comparison and Effects in the Efficiency

Still, the overall efficiency performance of the SPC scheme must be assessed. In Chapter 4, particularly in Subsection 4.5.3, it was discussed how, in principle, the SPC scheme would yield different losses in the switches, depending on the mode of operation. The theoretical calculation of these losses, and a comparison with the expected losses at the PC scheme were calculated an presented graphically in Figures 4-8, 4-9 and 4-10. The conclusions to this analysis were that, upon given operating conditions, the losses at SPC were smaller than those at the PC, as the circulating currents in the BB branch resulted in lower net current flowing through the BB switches.

This analysis has been validated through a series of experiments on the built setup, for different power stage configurations. Table 8.7 shows efficiencies and losses obtained in

steady state, of both the PC and SPC configurations, for the known given voltage conditions of V_{DC} = 500 V, V_{BB} = 260 V and V_{SM} = 73 V. The recorded current reference values considered were I_{BB} = 0 A, +5 A, +10 A and I_{SM} = -10 A, -5 A, 0 A, +5 A and +10 A.

Table 8.7: Experimental losses and efficiency performance of PC and SPC configurations.

I_{BB_ref} (A)	I_{SM_ref} (A)	$P_{Loss}(PC)$ (W)	$P_{Loss}(SPC)$ (W)	ΔP_{Loss} (W)	η_{PC} (%)	η_{SPC} (%)
0	10	142.0	248.6	106.6	-	-
0	5	82.0	147.9	65.9	-	-
0	0	20.3	15.1	-5.3	-	-
0	-5	99.8	55.3	-44.5	-	-
0	-10	206.0	250.8	44.8	-	-
5	10	240.1	224.4	-15.7	87.0%	87.4%
5	5	177.8	139.0	-38.8	89.5%	91.6%
5	0	146.0	138.3	-7.7	90.5%	91.0%
5	-5	166.0	191.8	25.9	89.1%	87.4%
5	-10	188.1	277.5	89.4	87.5%	81.9%
10	10	308.6	257.2	-51.5	90.6%	92.1%
10	5	251.8	218.7	-33.1	92.0%	93.1%
10	0	222.7	215.9	-6.9	92.6%	92.9%
10	-5	247.5	293.9	46.4	91.7%	90.3%
10	-10	286.4	363.9	77.5	90.4%	88.0%

From these results, it can be verified that the switches losses are lower in SPC provided that the BB and SM currents are both large and of the same sign. On the other hand, if the signs of both currents are opposite, SPC presents more losses than PC. Thus, Table 8.7 corroborate the theoretical results depicted in Figure 4-10. The results in Table 8.7 are graphically represented in Figure 8-16. As can be seen, the SPC presents fewer losses when the BB and SM currents have the same sign and larger values. As a conclusion, it must be noticed that, even though at some operating points the losses will be higher with the proposed SPC scheme than in the original PC scheme, the full performance concerning the efficiency of the proposed topology must be assessed only after considering the application and the control scheme used.

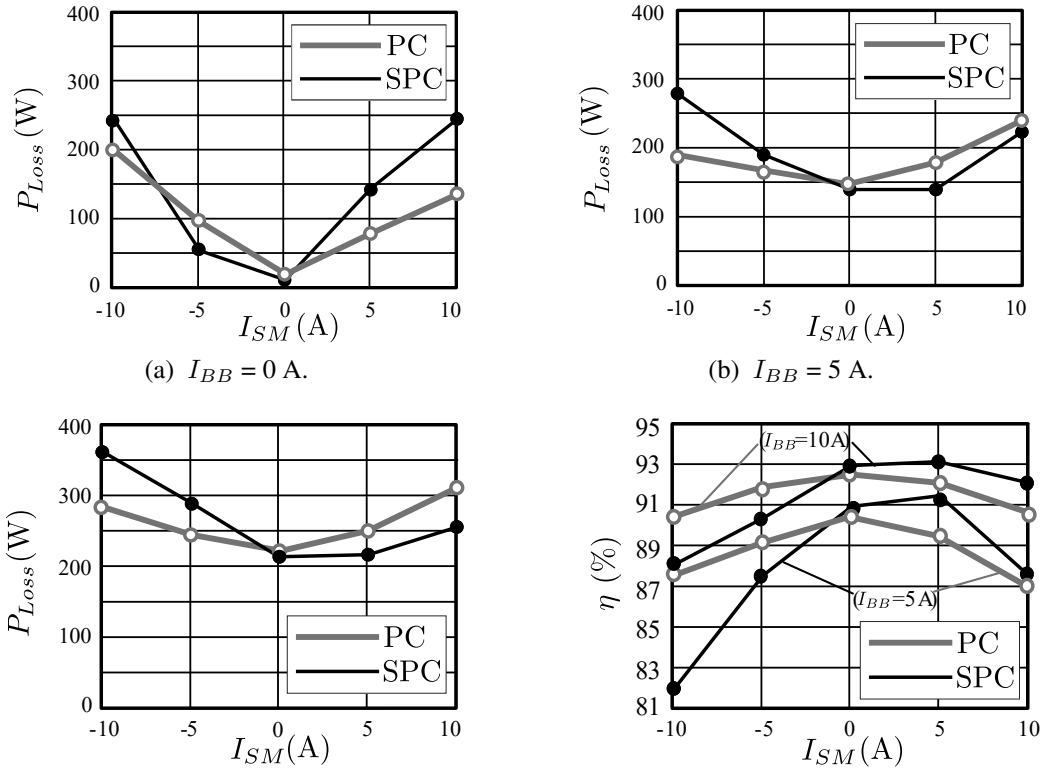


Figure 8-16: Steady-state losses comparison between PC and SPC configurations.

8.8 Fault-Tolerant Parallel Connection of the two Bidirectional Buck-Boost Converters

The next set of experiments dealing with the operation of the FTPC scheme. These experiments are done for both healthy and faulty conditions.

8.8.1 Islanding Operation Mode (Healthy Condition)

Figure 8-17 shows the healthy operation of the PC of two bidirectional buck converters (baseline case), together with the FTPC of two bidirectional buck-boost converters, in the same conditions as outlined in Section 7.5 of the previous Chapter. As it can seen from Figure 8-17, the BB delivers/absorbs the steady state power while the SM provides/absorbs the transient peak power. The behavior of the FTPC of two bidirectional buck-boost con-

verters is the same as the PC of the two bidirectional buck converters. Figure 8-17 fully matches with the simulation results in Figures 7-23 and 7-24.

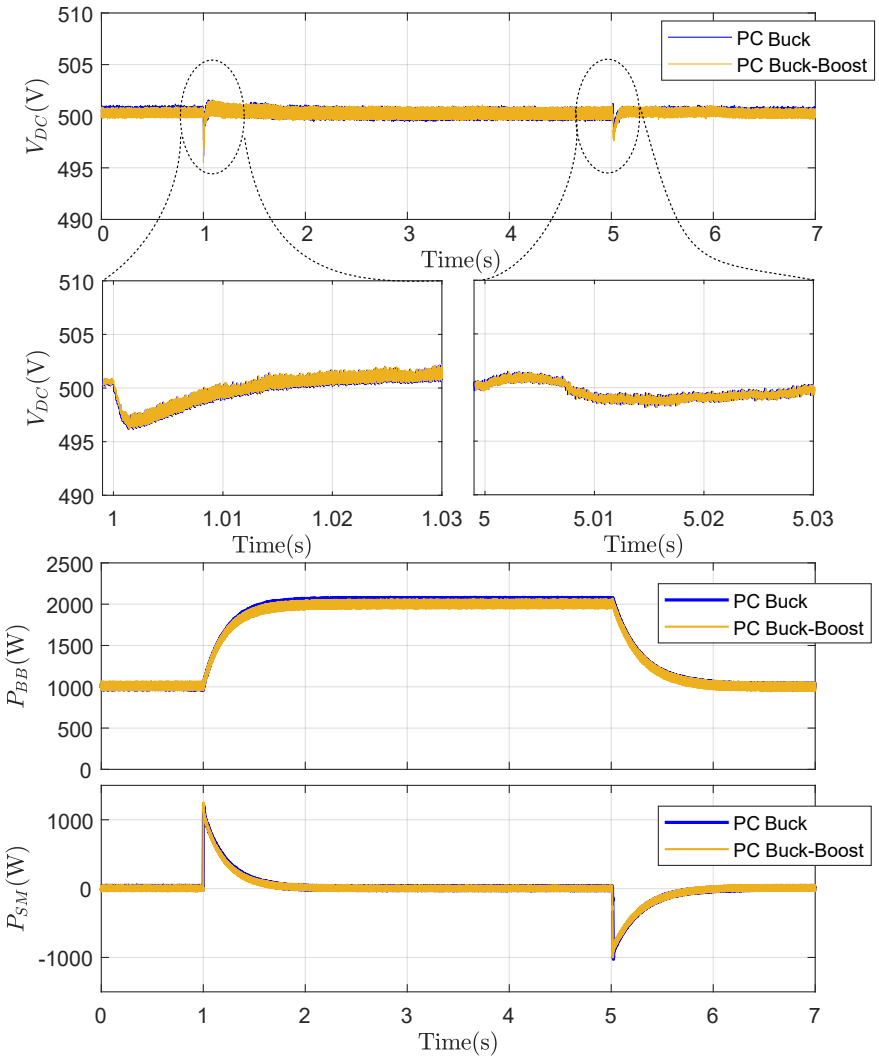


Figure 8-17: Experimental results for the FTPC of the two bidirectional buck-boost converters compared to the PC one during the islanding mode in the healthy condition.

These experiments validate the conclusions obtained in the simulations for these operating conditions.

8.8.2 Grid-Connected Operation Mode (Healthy Condition)

Once the islanding operation is validated, the system is now assessed upon the grid-tied operating mode (Independent and full control strategies).

8.8.2.1 Independent Control Strategy

The experimental results are done during healthy operation of the system (no fault at the DC bus). The DC bus is controlled by the VSI. The FTPC (yellow line) is compared with the PC baseline case (blue line) as depicted in Figure 8-18. The SM delivers/absorbs the transient peak power while the BB delivers/absorbs the rest of the transient power. From Figure 8-18, The FTPC of two bidirectional buck-boost converters (yellow line) has the same behavior as the PC of two bidirectional buck converters (blue line) as expected from simulation results. Figure 8-18 matches Figures 7-25 and 7-26, again validating the conclusions of the simulated tests.

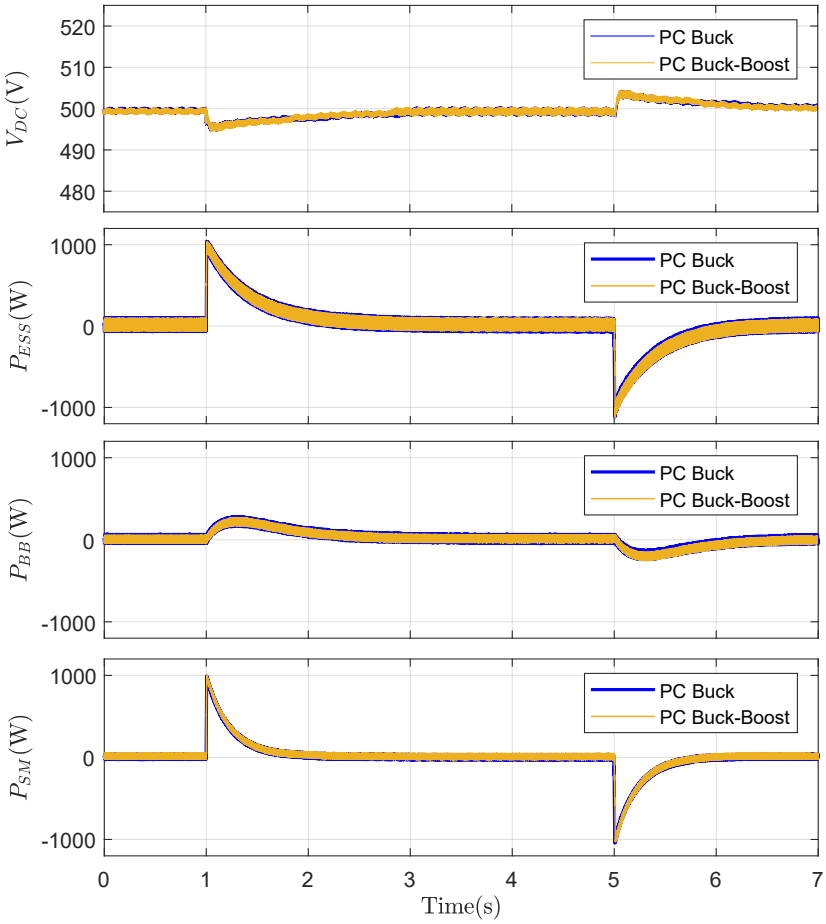


Figure 8-18: Experimental results for the FTPC of the two bidirectional buck-boost converters compared to the PC one during the grid-connected mode (Independent control strategy) in healthy condition.

8.8.2.2 Full Control Strategy

The FTPC of the two buck-boost converters is compared with the base case PC of the two buck converters in healthy conditions, but now for the case of the full control strategy. The performance in these conditions is shown in Figure 8-13. Again, the grid delivers the steady-state power; however, the SM delivers/absorbs the transient peak power, and the BB delivers/absorbs the rest of transient power. Figure 8-19 shows that the FTPC of two bidirectional buck-boost converters (yellow line) has the same behavior as the PC of two bidirectional buck converters (blue line). As it can be seen, Figure 8-19 matches the simulation results at Figures 7-27 and 7-28.

8.8.3 Steady-State Operation

Again, the steady-state operation is validated by measuring the current ripple at the inductors. The DC bus is kept constant by a VSI, and two current controllers are applied for the BB and SM. As it is shown from Figure 8-20, the peak to peak current ripple for the inductor connected to the BB is 0.41 A; however, for the inductor connected to the SM is 0.743 A. These results match the theoretical and simulation results in Chapter 7.

8.8.4 Fault Condition and Fault Ride-Through Scheme

As the performance at healthy conditions of the FTPC scheme of the HESS has been demonstrated, the next step is to assess the behavior of the setup upon a short-circuit fault at the DC bus. Figure 8-21 shows the operation of the buck-boost converter with the proposed control during the fault sequence outlined in the previous chapter. First, the system is operating at healthy conditions; suddenly a short-circuit fault is imposed at $t = 0.5$ s, and the fault is cleared only at $t = 2.75$ s. From this instant, the system recovery is finally obtained at around $t = 3.2$ s. It must be noticed how the fault operation and fault ride-through performance of the system again fully matches with Figure 7-31 from simulations.

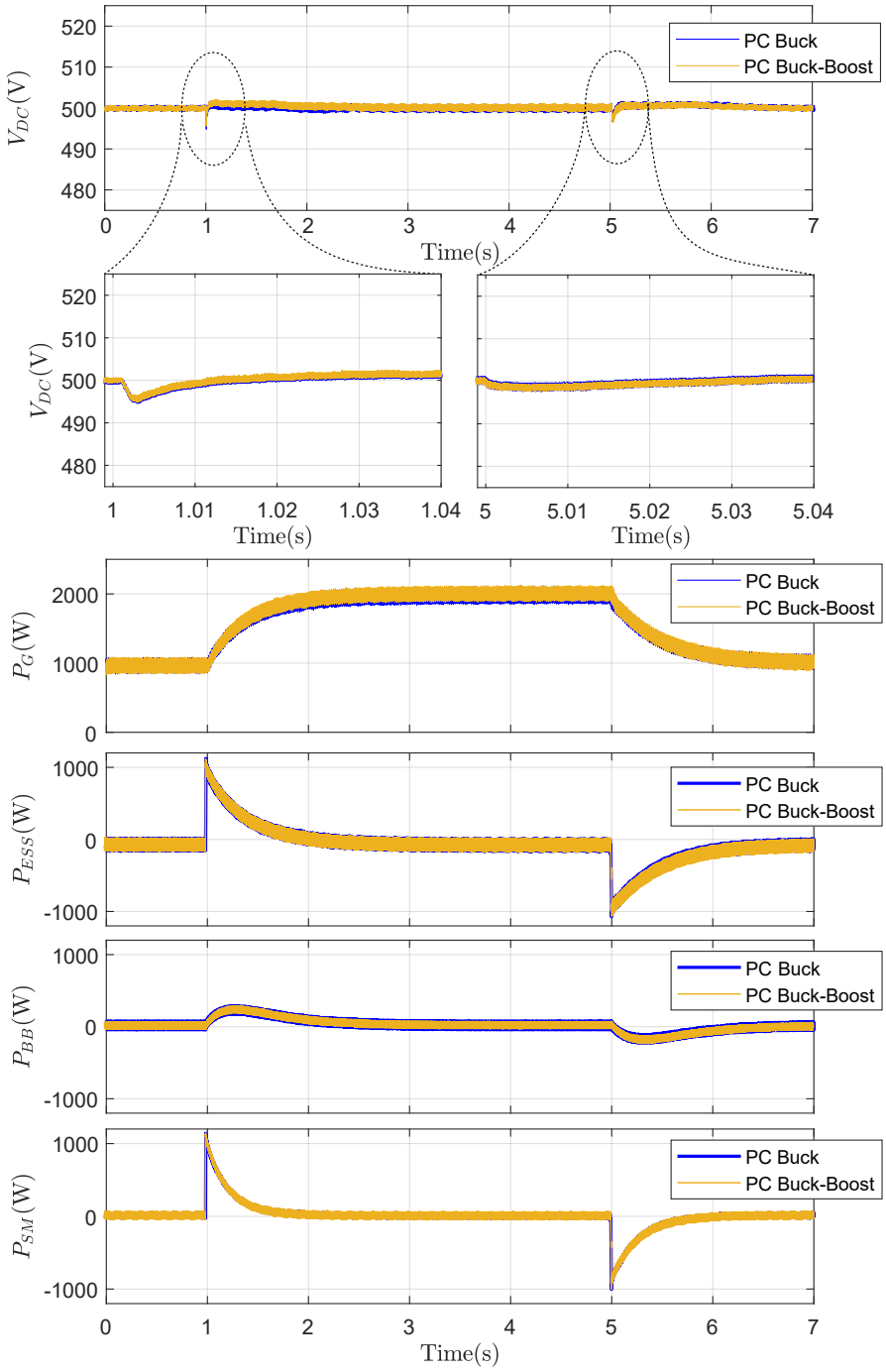


Figure 8-19: Experimental results for the FTPC of the two bidirectional buck-boost converters compared to the PC one during the grid-connected mode (Full control strategy) in healthy condition.

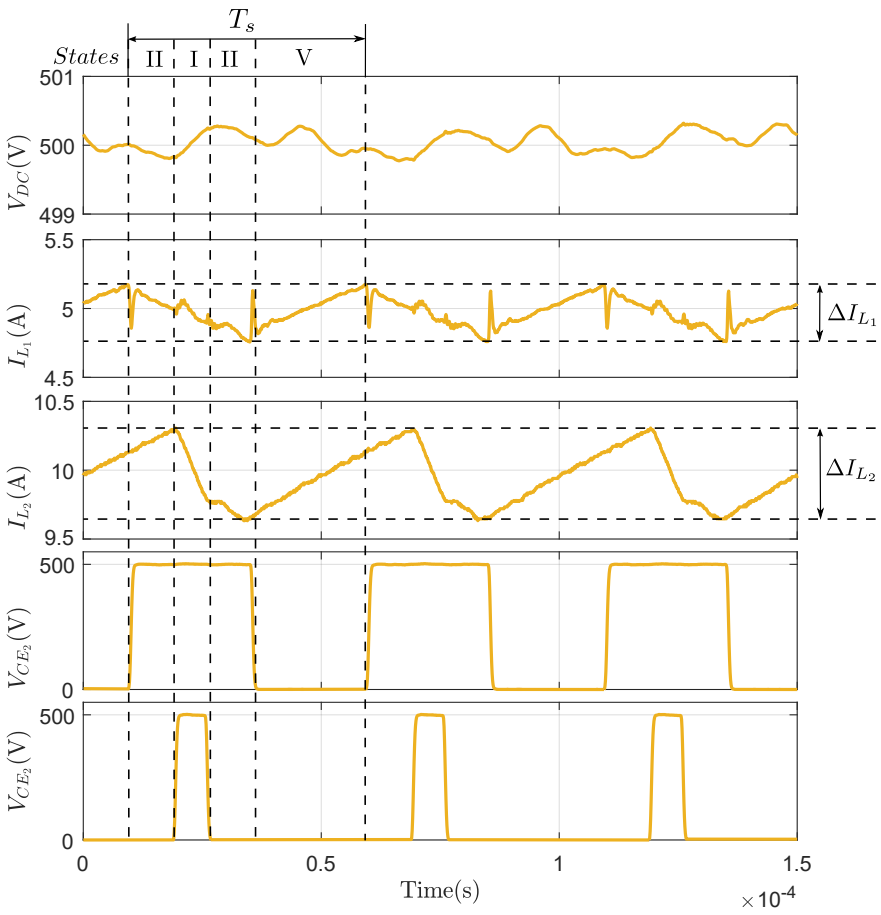


Figure 8-20: Experimental results for the FTPC where 5 A BB current reference and 10 A SM current reference are applied, and the DC bus is controlled by the grid VSI.

8.9 Conclusions

This chapter has validated, through experimental tests carried out in a laboratory setup, all the operation modes and control strategies defined in the earlier Chapters 3 to 6 and simulated in previous Chapter 7. As it will be discussed in detail in the next chapter, this proves the feasibility and validity of the solutions proposed in this PhD thesis as contributions to the implementation of non-isolated, bidirectional PEC to interface storage devices in a HESS to DC microgrids and nanogrids.

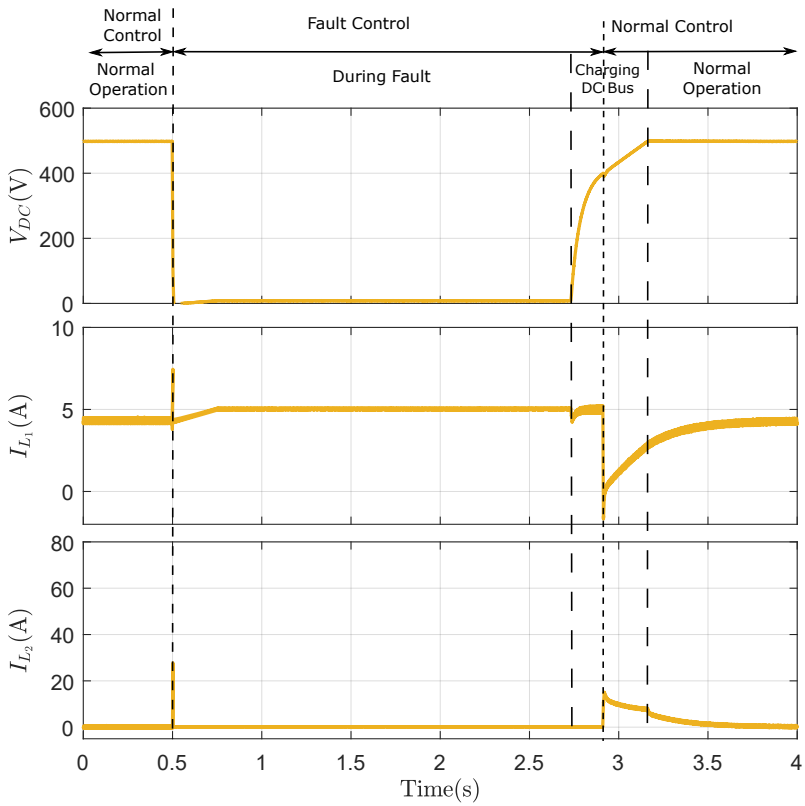


Figure 8-21: Experimental results during fault and normal operation with the proposed control, the fault occurred at 0.5 s and cleared at 2.75 s.

Chapter 9

Conclusion and Future Development

Contents

9.1 Conclusions

The following summarizes the research conducted through the realization of this PhD thesis.

Firstly, the target problem to tackle, including the definition of the application, the operating constraints, and the design limits, is defined in detail. The basic structure of the HESS attached to DC microgrids is initially studied. Then, a comparison among the basic power converter topologies for these HESS in DC nanogrids and microgrids is performed.

From the results of the comparison, the PC of two bidirectional converters was selected as the baseline case. After that, a control scheme for islanding mode and two control schemes for grid-connected mode (independent storage control and full control) for ESSs in DC microgrids were analyzed, compared and validated (both by simulation and through experiments). The results show that the full control scheme has a better and faster DC bus recovery that the independent storage control scheme, for the grid-connected mode. However, the full control needs a genuinely real-time communication between the grid converter and the ESS converters in order to generate the power reference. This decreases the robustness and reliability of the control system, as malfunction or delays in the communication link affect the control performance significantly. On the other hand, in case the HESS control is independent of the grid converter control, there is no need for real-time communication. This increases the robustness and reliability of the independent storage control scheme, yet at the cost of a slower DC bus recovery. In any case, both control schemes provide better performance in grid-connected mode compared to the operation of the grid converter without HESS. Therefore, the final decision relies on the constraints of the target application.

Secondly, the limitations of the base case were identified, mainly arising from the operational limits of the converters upon high voltage mismatch ratings, and from the behavior of the system upon DC bus fault conditions.

In the case of the operational limitations due to a large mismatch in the voltage ratings of the ESS devices, a novel topology for this configuration, the SPC, has been proposed. This constraint considers low/medium power levels where galvanic isolation is not a requirement. The topologies studied are the base PC of two bidirectional converters, the FBC configuration for the SM leg, the SC of the storage devices, and the proposed SPC of the storage units. All these options can be implemented by connecting the power switches in the standard single-leg configuration with complementary control pulses switching. This constraint facilitates the final implementation using ready-to-market, cheap components. The control schemes for islanding mode and grid-connected mode are adapted for the SPC. The control scheme implemented in the analysis manages the storage power flows to compensate the system DC bus voltage due to load steps or grid perturbations.

The results of the theoretical study, which included aspects such as losses, efficiency, loss balance between switches, and margins in the control stage design have been validated utilizing simulations and experimental tests on a built laboratory prototype with a rated power level of 10 kW. All throughout the analysis, and to find comparable results, the main parameters in the design, i.e., power, voltage and current levels of the devices were kept constant. For the same reason, also the values of the reactive elements were held constant. From the comparison, it can be seen how SPC presents a better efficiency (fewer losses) and also a better distribution of the electric and thermal stresses in the switches of the legs of the converter than the PC case. Given that the SM inductor presents half the inductance value than in the PC case for the same target current ripple, higher power density might also be achieved. SPC also allows for extended control margin. On the other hand, as mentioned, SC does not allow for independent current control of the storage devices, therefore preventing its use as a hybrid storage solution. For SC and FBC cases, the thermal and stresses balance is similar to the SPC; however, FBC presents increased power losses than SPC.

The comparative efficiency results show how the performance comparison between PC and SPC depend on the signs of the currents; therefore, the control scheme determines the overall efficiency of the system. From the above discussion, the proposed SPC scheme is considered as a feasible option for non-isolated interfacing of highly mismatched voltage rating storage systems in multiport configurations, for low to medium power rated HESSs applications. The critical issue demonstrated in this work is that, regardless of the efficiency of the base-case (PC), an increase in the efficiency, in the dynamic performance, and in the stresses distribution in the converter switches achieved by the SPC connection scheme will be obtained, provided that a set of operating constraints be met. In the performed comparison, the hardware setup has been kept constant, and therefore this gain does not yield to modification in the components count or the basic control implementation requirements. The performance of the SPC solution is better than the standard PC option, and this enhancement is obtained without any extra component.

To address the second critical limitation of the base-case solution, a DC bus short-circuit fault-tolerant, fault ride-through control scheme for a non-isolated topology for HESSs has

been presented, analyzed and verified through simulations and validated by experiments. The proposed strategy includes automatic fault ride-through once the DC bus short-circuit is cleared. This configuration has a higher component count than the bidirectional buck version which is the simplest topology able to achieve the required dynamic performance. However, provided that the proposed control scheme with a dual carrier be used, it has been stated that the inclusion of the fault-tolerant, fault-ride through feature does not significantly increase the overall power losses. The proposed configuration, based on the two carrier signals can operate in buck or boost mode, making this scheme also useful for different applications.

The Degree of fulfillment of the objectives defined in the introductory sections of this research is now discussed:

- **Objective**: Definition of the system under study, its constraints in terms of applications, power levels, voltage ratings and its expected performance and behavior. **Degree of the fulfillment**: This objective has been completely achieved, particularly in Chapter 2.

- **Objective**: Characterization of the state-of-the-art of the HESS for DC microgrids and nanogrids. **Degree of the fulfillment**: This objective has been completely achieved, particularly in Chapter 2.

- **Objective**: Definition of the power electronic topologies suitable for HESS in DC microgrids and nanogrids, and selection of the base case topology. **Degree of the fulfillment**: This objective has been completely achieved, particularly in Chapter 3.

- **Objective**: Analysis of the main healthy operating conditions of the HESS. Definition of the operation modes: islanding operation and grid-connected operation. **Degree of the fulfillment**: This objective has been completely achieved, particularly in Chapter 3.

- **Objective**: Study of the control schemes for the HESS in the baseline case, for every operation mode. Definition of the control strategies: islanding control strategy, inde-

pendent control strategy, and full control strategy. **Degree of the fulfillment**: This objective has been completely achieved, particularly in Chapter 3.

- **Objective**: Analysis of the operating limitations of the base case for the voltage rating constraints. **Degree of the fulfillment**: This objective has been completely achieved, particularly in Chapter 4.

- **Objective**: Proposal of contributions for dealing with issues related to voltage rating constraints. **Degree of the fulfillment**: This objective has been completely achieved, particularly in Chapter 4.

- **Objective**: Analysis and operating issues of the HESS upon DC bus short-circuit fault conditions. **Degree of the fulfillment**: This objective has been completely achieved, particularly in Chapter 5.

- **Objective**: Proposal of fault ride-through operation of the system. **Degree of the fulfillment**: This objective has been completely achieved, particularly in Chapter 5.

- **Objective**: Establishment of a design methodology for validation and implementation of the proposed solutions. **Degree of the fulfillment**: This objective has been completely achieved, particularly in Chapter 6.

- **Objective**: Validation of the proposed solutions through simulations and experimental test in laboratory prototypes. **Degree of the fulfillment**: This objective has been completely achieved, particularly in Chapters 7 and 8.

- **Objective**: Critical analysis of the conclusions and establishment of future developments. **Degree of the fulfillment**: This objective has been completely achieved, particularly in this Chapter.

9.2 Publications

The following lists the publications in prestigious international conferences and indexed international journals directly derived from this PhD thesis:

9.2.1 Journal Publications (First Author)

- **R. Georgious**, J. García, Á. Navarro-Rodríguez and P. García, "A Study on the Control Design of Non-Isolated Converter Configurations for Hybrid Energy Storage Systems", in IEEE Transactions on Industry Applications [125].

- **Ramy Georgious**, Jorge Garcia, Pablo Garcia, and Angel Navarro-Rodriguez. A comparison of non-isolated high-gain three-port converters for hybrid energy storage system. Energies, 11(3), 2018 [146].

9.2.2 Conference Publications (First Author)

- **R. Georgious**, J. García, P. García and M. Sumner, "Analysis of hybrid energy storage systems with DC link fault ride-through capability," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8 [117].

- **R. Georgious**, J. García, Á. Navarro-Rodríguez and P. García, "A study on the control loop design of non-isolated configurations for hybrid storage systems," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-6 [148].

- **R. Georgious**, J. Garcia, A. Navarro, S. Saeed and P. Garcia, "Series-Parallel Connection of Low-Voltage sources for integration of galvanically isolated Energy Storage Systems," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 3508-3513 [147].

- **R. Georgious** and J. García, "Hybridization of Energy Storage Systems for electric transportation by means of bidirectional Power Electronic Converters," 2015 6th International Conference on Power Electronics Systems and Applications (PESA), Hong Kong, 2015, pp. 1-6 [119].

A complete copy of all the previous publications is included in the Appendix C. Additionally, the PhD candidate, as a member of the LEMUR research group at the University of

Oviedo, Spain, has also collaborated in the following publications, related to the research in microgrids and nanogrids for grid support applications:

9.2.3 Journal Publications (Coauthor)

- Á. Navarro-Rodríguez, P. García, **R. Georgious**, J. García and S. Saeed, "Observer-based Transient Frequency Drift Compensation in AC Microgrids," in IEEE Transactions on Smart Grid [129].

9.2.4 Conference Publications (Coauthor)

- Á. Navarro-Rodríguez, P. García, **R. Georgious** and J. García, "Adaptive active power sharing techniques for DC and AC voltage control in a hybrid DC/AC microgrid," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017, pp. 30-36 [133].

- J. Garcia, **R. Georgious**, P. Garcia and A. Navarro-Rodriguez, "Non-isolated high-gain three-port converter for hybrid storage systems," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8 [137].

- A. Navarro-Rodriguez, P. Garcia, **R. Georgious** and J. Garcia, "A communication-less solution for transient frequency drift compensation on weak microgrids using a D-statcom with an energy storage system," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 6904-6911 [130].

- T. U. Okeke and **R. G. Zaher**, "Flexible AC Transmission Systems (FACTS)," 2013 International Conference on New Concepts in Smart Cities: Fostering Public and Private Alliances (SmartMILE), Gijon, 2013, pp. 1-4.

- T. U. Okeke and **R. G. Zaher**, "Reactive power management for distributed generation: Motivation and solutions," 2013 International Conference on New Concepts in Smart Cities: Fostering Public and Private Alliances (SmartMILE), Gijon, 2013, pp. 1-4.

9.3 Future Development

After the work carried out in this PhD research, a series of future developments have been identified. These topics extend the validity and applicability of the obtained conclusions beyond the constraints of the studied application. These developments include:

- Implementing the experimental prototype on a high scale with high ratings of IGBTs modules and loads.
- Including photovoltaic panels in the microgrid and the design of the control scheme to obtain the Maximum Power Point Tracking (MPPT) during the islanding mode and grid-connected mode.
- Using other technologies of ESS with different dynamics such as fuel cells and compared with the HESS implemented in this research.
- Extending the methodology for other possible power topologies and different strategies for the control schemes.
- Optimizing the system for increasing the efficiency and power density assuming SPC scheme as the target topology.
- Including the extension of the study to other fault types, for instance at the storage units; optimization of the control parameters to minimize the energy lost during fault mode or the extension of this scheme to a different type of applications apart from HESS.
- Including the energy storage devices modeling as to refine the control algorithms performance; or extension of the proposed solution in another kind of applications apart from HESS.

Capítulo 9

Conclusión y Desarrollos Futuros

Contents

9.1 Conclusiones

En este capítulo final se resumen las investigaciones realizadas a través de la realización de esta tesis doctoral.

En primer lugar, se define detalladamente el problema objetivo a abordar, incluida la definición de la aplicación, las restricciones de explotación y los límites de diseño. Inicialmente se estudia la estructura básica del HESS acoplado a microrredes de CC. A continuación, se realiza una comparación entre las topologías básicas de convertidores de poten-

cia para estos HESS en nanorredes y microrredes de CC. De los resultados de la comparación, se seleccionó un caso base de topología de convertidor para interconectar el HESS al bus CC, denominada PC. A continuación, se analizaron, compararon y validaron un esquema de control para el modo aislado y dos esquemas de control para el modo conectado a la red (control independiente del almacenamiento y control total) para la aplicación objetivo. Esta validación se llevó a cabo tanto por simulación como a través de experimentos en prototipos de laboratorio. Los resultados muestran que el esquema de control completo tiene una recuperación de bus de CC mejor y más rápida que el esquema de control de almacenamiento independiente, para el modo conectado a la red. Sin embargo, el control total necesita una comunicación en tiempo real entre el convertidor de red y los convertidores ESS para generar la referencia de potencia. Esto implica aspectos que limitan la robustez y fiabilidad del sistema de control, ya que el mal funcionamiento o los retrasos en el enlace de comunicación afectan significativamente al comportamiento del control. Por otro lado, en caso de que el control HESS sea independiente del control del convertidor de red, no hay necesidad de comunicación en tiempo real. Esto aumenta la robustez y fiabilidad del esquema de control de almacenamiento independiente, pero a costa de una recuperación de bus de CC más lenta. En cualquier caso, ambos esquemas de control proporcionan un mejor rendimiento en el modo conectado a la red en comparación con el funcionamiento del convertidor de red sin HESS. Por lo tanto, la decisión final se basa en las limitaciones de la aplicación del objetivo.

En segundo lugar, se identificaron las limitaciones del caso base, principalmente derivadas de los límites operativos de los convertidores en las clasificaciones de desajuste de alto voltaje, y del comportamiento del sistema en condiciones de fallo del bus de CC.

En el caso de las limitaciones de funcionamiento debidas a una gran diferencia en las especificaciones de tensión nominal de los dispositivos ESS, se ha propuesto una nueva topología para esta configuración, denominada esquema SPC. La aplicabilidad de esta solución se restringe en principio a niveles de potencia bajos/medios donde el aislamiento galvánico no es un requisito. Las topologías estudiadas son la solución base (PC de dos convertidores bidireccionales), la configuración en puente completo (FBC, por sus siglas en inglés), la conexión serie (SC, por sus siglas en inglés) de los dispositivos de almace-

namiento, y el SPC propuesto de las unidades de almacenamiento. Todas estas opciones se pueden implementar conectando los interruptores de potencia en la configuración estándar de una sola etapa con conmutación de pulsos de control complementarios. Esta restricción facilita la implementación final utilizando componentes baratos y simples, fácilmente disponibles en el mercado. Además, los esquemas de control para el modo aislado y el modo conectado a la red se han adaptado para poder ser aplicados al SPC. El esquema de control implementado en el análisis gestiona los flujos de energía de almacenamiento para compensar la tensión del bus de CC del sistema debido a transitorios de carga o a las perturbaciones de la red.

Los resultados del estudio teórico, que incluye aspectos tales como pérdidas, eficiencia, balance de pérdidas entre interruptores y márgenes en el diseño de la etapa de control, han sido validados utilizando simulaciones y pruebas experimentales en un prototipo de laboratorio construido con un nivel de potencia nominal de 10 kW. A lo largo de todo el análisis, y para encontrar resultados comparables, se mantuvieron constantes los principales parámetros del diseño, es decir, los niveles de potencia, tensión y corriente de los dispositivos. Por la misma razón, también los valores de los elementos reactivos se mantuvieron constantes. De la comparación se puede ver cómo SPC presenta una mejor eficiencia (menos pérdidas) y también una mejor distribución de los esfuerzos eléctricos y térmicos en los interruptores de las ramas del convertidor que en el caso base del esquema PC. Dado que la bobina del SM presenta la mitad del valor de inductancia que en el caso base para la mismo rizado de corriente, también podría lograrse una densidad de potencia más alta. El SPC también permite un margen de control ampliado. Por otro lado, como ya se ha mencionado, la estructura SC no permite un control independiente de la corriente de los dispositivos de almacenamiento, lo que impide su uso como solución híbrida de almacenamiento. En los casos de SC y FBC, el balance térmico y de tensiones es similar al SPC; sin embargo, el FBC presenta mayores pérdidas de potencia que el SPC.

Los resultados muestran cómo la comparación de rendimiento entre PC y SPC depende de los signos relativos de las corrientes; por lo tanto, el esquema de control determina la eficiencia global del sistema. A partir del análisis anterior, el esquema SPC propuesto se considera una opción viable para la interconexión no aislada de sistemas de almace-

namiento de valores nominales de tensión muy dispares en configuraciones multipuerto, para aplicaciones HESS de baja a media potencia. La cuestión crítica demostrada en este trabajo es que, al utilizar la estructura SPC, se obtendrá un aumento en la eficiencia, una mejora en el comportamiento dinámico y en la distribución de los esfuerzos de tensiones en los interruptores del convertidor frente al caso base, siempre que se cumpla un conjunto de restricciones de funcionamiento. En la comparación realizada, la configuración de hardware se ha mantenido constante, y por lo tanto esta ganancia no implica modificaciones en el número ni características de los componentes o en los requisitos básicos de implementación de control. El rendimiento de la solución SPC es mejor que el de la opción estándar de PC, y esta mejora se obtiene sin ningún componente adicional.

Para abordar la segunda limitación crítica de la solución del caso base, se ha presentado, analizado y verificado mediante simulaciones un esquema de control de cortocircuito de bus de CC tolerante a fallo, para una topología no aislada para integración de HESS en microrredes, y se ha validado también de forma experimental. La estrategia propuesta incluye el rearme automático del sistema una vez que se haya eliminado el cortocircuito del bus de CC. Esta configuración tiene un mayor número de componentes que la versión bidireccional base, que es la topología más simple capaz de alcanzar el rendimiento dinámico requerido. Sin embargo, siempre que se utilice el esquema de control propuesto con una portadora doble, se ha demostrado que la inclusión de las modificaciones necesarias para conseguir un sistema robusto a fallos no aumente significativamente las pérdidas totales de potencia. La configuración propuesta, basada en dos señales portadoras triangulares, puede operar en modo reductor o elevador, lo que hace que este esquema también sea útil para diferentes aplicaciones.

Se discute a continuación el grado de cumplimiento de los objetivos definidos en las secciones introductorias de esta investigación:

- **Objetivo**: Definición del sistema en estudio, sus limitaciones en términos de aplicación, niveles de potencia, valores nominales de tensión y su rendimiento y comportamiento esperados. Grado de cumplimiento: Este objetivo se ha alcanzado plenamente, en particular en el capítulo 2.

- **Objetivo**: Caracterización del estado del arte del HESS para microrredes y nanorredes de CC. Grado de cumplimiento: Este objetivo se ha alcanzado plenamente, en particular en el capítulo 2.

- **Objetivo**: Definición de las topologías de electrónica de potencia adecuadas para HESS en microrredes y nanorredes de CC, y selección de la topología del caso base. Grado de cumplimiento: Este objetivo se ha alcanzado plenamente, en particular en el capítulo 3.

- **Objetivo**: Análisis de las principales condiciones operativas nominales (sin fallo) del HESS. Definición de los modos de operación: operación en isla y operación conectada a la red. Grado de cumplimiento: Este objetivo se ha alcanzado plenamente, en particular en el capítulo 3.

- **Objetivo**: Estudio de los esquemas de control del HESS en el caso base, para cada modo de operación. Definición de las estrategias de control: estrategia de control en modo isla, estrategia de control independiente y estrategia de control total. Grado de cumplimiento: Este objetivo se ha alcanzado plenamente, en particular en el capítulo 3.

- **Objetivo**: Análisis de los límites de funcionamiento de la hipótesis de base para las restricciones de tensión nominal. Grado de cumplimiento: Este objetivo se ha alcanzado plenamente, en particular en el capítulo 4.

- **Objetivo**: Propuesta de contribuciones para solucionar problemas relacionados con las restricciones de tensión nominal. Grado de cumplimiento: Este objetivo se ha alcanzado plenamente, en particular en el capítulo 4.

- **Objective**: Análisis de las limitaciones de funcionamiento del HESS en condiciones de fallo por cortocircuito en el bus de CC. Grado de cumplimiento: Este objetivo se ha alcanzado plenamente, en particular en el capítulo 5.

- **Objetivo**: Propuesta de funcionamiento del sistema en caso de fallo. Grado de

cumplimiento: Este objetivo se ha alcanzado plenamente, en particular en el capítulo 5.

- **Objetivo**: Establecimiento de una metodología de diseño para la validación e implementación de las soluciones propuestas. Grado de cumplimiento: Este objetivo se ha alcanzado plenamente, en particular en el capítulo 6.

- **Objetivo**: Validación de las soluciones propuestas mediante simulaciones y ensayos experimentales en prototipos de laboratorio. Grado de cumplimiento: Este objetivo se ha alcanzado plenamente, en particular en los capítulos 7 y 8.

- **Objetivo**: Análisis crítico de las conclusiones y establecimiento de futuros desarrollos. Grado de cumplimiento: Este objetivo se ha alcanzado plenamente, en particular en este capítulo.

9.2 Publications

A continuación, se enumeran las publicaciones en prestigiosas conferencias internacionales y revistas internacionales indexadas derivadas directamente de esta tesis doctoral:

9.2.1 Publicaciones en Revistas (Primer Autor)

- **R. Georgious**, J. García, Á. Navarro-Rodríguez and P. García, "A Study on the Control Design of Non-Isolated Converter Configurations for Hybrid Energy Storage Systems", in IEEE Transactions on Industry Applications [125].

- **Ramy Georgious**, Jorge Garcia, Pablo Garcia, and Angel Navarro-Rodriguez. A comparison of non-isolated high-gain three-port converters for hybrid energy storage system. Energies, 11(3), 2018 [146].

9.2.2 Publicaciones en Conferencias (Primer Autor)

- **R. Georgious**, J. García, P. García and M. Sumner, "Analysis of hybrid energy storage systems with DC link fault ride-through capability," 2016 IEEE Energy Conver-

sion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8 [117].

- **R. Georgious**, J. García, Á. Navarro-Rodríguez and P. García, "A study on the control loop design of non-isolated configurations for hybrid storage systems," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-6 [148].

- **R. Georgious**, J. Garcia, A. Navarro, S. Saeed and P. Garcia, "Series-Parallel Connection of Low-Voltage sources for integration of galvanically isolated Energy Storage Systems," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 3508-3513 [147].

- **R. Georgious** and J. García, "Hybridization of Energy Storage Systems for electric transportation by means of bidirectional Power Electronic Converters," 2015 6th International Conference on Power Electronics Systems and Applications (PESA), Hong Kong, 2015, pp. 1-6 [119].

Se incluye una copia completa de todas las publicaciones anteriores en el Apéndice C. Además, el candidato a doctorado, como miembro del grupo de investigación LEMUR de la Universidad de Oviedo, España, también ha colaborado en las siguientes publicaciones, relacionadas con la investigación en microrredes y nanorredes para aplicaciones de soporte de red:

9.2.3 Publicaciones en Revistas (Coautor)

- Á. Navarro-Rodríguez, P. García, **R. Georgious**, J. García and S. Saeed, "Observer-based Transient Frequency Drift Compensation in AC Microgrids," in IEEE Transactions on Smart Grid [129].

9.2.4 Publicaciones en Conferencias (Coautor)

- Á. Navarro-Rodríguez, P. García, **R. Georgious** and J. García, "Adaptive active power sharing techniques for DC and AC voltage control in a hybrid DC/AC micro-

grid," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017, pp. 30-36 [133].

- J. Garcia, **R. Georgious**, P. Garcia and A. Navarro-Rodriguez, "Non-isolated high-gain three-port converter for hybrid storage systems," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8 [137].

- A. Navarro-Rodriguez, P. Garcia, **R. Georgious** and J. Garcia, "A communication-less solution for transient frequency drift compensation on weak microgrids using a D-statcom with an energy storage system," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 6904-6911 [130].

- T. U. Okeke and **R. G. Zaher**, "Flexible AC Transmission Systems (FACTS)," 2013 International Conference on New Concepts in Smart Cities: Fostering Public and Private Alliances (SmartMILE), Gijon, 2013, pp. 1-4.

- T. U. Okeke and **R. G. Zaher**, "Reactive power management for distributed generation: Motivation and solutions," 2013 International Conference on New Concepts in Smart Cities: Fostering Public and Private Alliances (SmartMILE), Gijon, 2013, pp. 1-4.

9.3 Desarrollos Futuros

Tras el trabajo realizado en esta investigación de doctorado, se han identificado una serie de desarrollos futuros. Estos temas extienden la validez y aplicabilidad de las conclusiones obtenidas más allá de las limitaciones de la aplicación estudiada. Estos desarrollos incluyen:

- Implementación del prototipo experimental a mayor escala de potencias, adaptando las especificaciones de los interruptores, elementos reactivos y cargas del a microrred.

- Inclusión de generación distribuida (como por ejemplo paneles fotovoltaicos) en la microrred, así como el diseño del esquema de control para obtener el Seguimiento

del Punto de Máxima Potencia (MPPT) durante el modo de funcionamiento en isla y el modo de conexión a red.

- Uso de otras tecnologías de ESS con diferentes dinámicas tales como celdas de combustible, y combinación de estos equipos con el HESS implementado en esta investigación.

- Ampliación de la metodología para otras posibles topologías de potencia y diferentes estrategias para los esquemas de control.

- Optimizar el sistema para aumentar la eficiencia y la densidad de potencia asumiendo el esquema SPC como topología objetivo.

- Extensión del estudio a otros tipos de fallo, por ejemplo en las unidades de almacenamiento; la optimización de los parámetros de control para minimizar la pérdida de energía durante el modo de falla o la extensión de este esquema a un tipo diferente de aplicaciones aparte del HESS.

- Inclusión del modelado detallado de los dispositivos de almacenamiento de energía para refinar el rendimiento de los algoritmos de control. Extensión de la solución propuesta en otro tipo de aplicaciones además del HESS.

Appendix A

DQ Transformation

Contents

A.1 Transformation from abc Stationary Reference Frame to dq Rotating Reference Frame

Considering a three-phase balanced system has an anti-clockwise positive phase sequence (abc) (i.e., $f_a(t)$ leads $f_b(t)$ by 120 electrical degrees and $f_b(t)$ leads $f_c(t)$ by 120

electrical degrees) as depicted in Figure A-1.

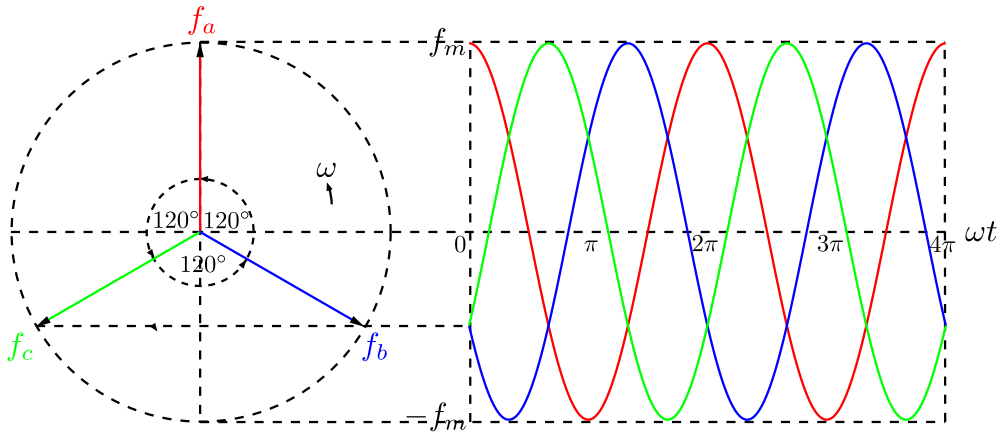


Figure A-1: Three phase balanced system as a function of cosine.

Therefore, the three-phase time-varying quantities are represented as a function of cosine as follows:

$$f_a(t) = f_m \cos(\omega \cdot t) \tag{A.1}$$

$$f_b(t) = f_m \cos(\omega \cdot t - \tfrac{2\Pi}{3}) \tag{A.2}$$

$$f_c(t) = f_m \cos(\omega \cdot t + \tfrac{2\Pi}{3}) \tag{A.3}$$

where:

- f is any of the electrical variables, and it could be voltage or current,
- f_m is the amplitude of f,
- ω is the angular frequency of f in rads/sec.

A.1.1 Transformation from abc Stationary Reference Frame to $\alpha\beta\gamma$ Stationary Reference Frame

In order to convert these quantities from abc stationary reference frame into $\alpha\beta$ stationary reference frame, taking the projections of the three-phase quantities on orthogonal $\alpha\beta$ axes where α axis is aligned with a-axis as shown in Figure A-2. The $\alpha\beta\gamma$ transformation is also known as the Clarke transformation [164].

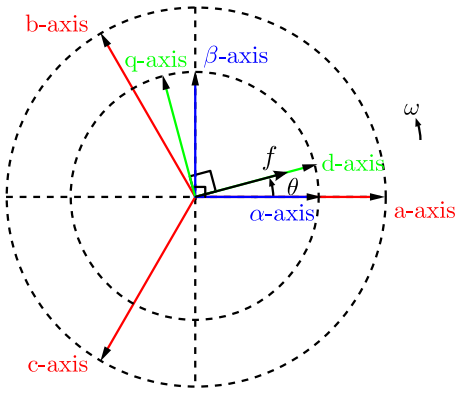


Figure A-2: The relationship between the abc stationary reference frame, the $\alpha\beta$ stationary reference frame and the dq rotating reference frame.

$$\begin{bmatrix} f_\alpha \\ f_\beta \\ f_\gamma \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(0) & \cos(\frac{2\Pi}{3}) & \cos(-\frac{2\Pi}{3}) \\ \sin(0) & \sin(\frac{2\Pi}{3}) & \sin(-\frac{2\Pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{A.4}$$

$$\begin{bmatrix} f_\alpha \\ f_\beta \\ f_\gamma \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{A.5}$$

Therefore, the $\alpha\beta\gamma$ quantities are represented as follows:

$$f_\alpha = f_m \cos(\omega \cdot t) \tag{A.6}$$

$$f_\beta = f_m \sin(\omega \cdot t) \tag{A.7}$$

$$f_\gamma = 0 \tag{A.8}$$

In order to transform from $\alpha\beta$ stationary reference frame to abc stationary reference frame, the inverse transformation can be used as follows:

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} & 1 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} f_\alpha \\ f_\beta \\ f_\gamma \end{bmatrix} \tag{A.9}$$

A.1.2 Transformation from $\alpha\beta\gamma$ Stationary Reference Frame to dq Rotating Reference Frame

The net vector for the components of dq reference frame makes an angle (θ) with the orthogonal $\alpha\beta$ reference frame and rotates with angular frequency (w) as shown in Figure A-2. The system can be reduced to a DC by taking the projection of the $\alpha\beta$ stationary reference frame components on the dq rotating reference frame.

$$\theta = \omega \cdot t \tag{A.10}$$

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 \\ -\sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} f_\alpha \\ f_\beta \\ f_\gamma \end{bmatrix} \tag{A.11}$$

Therefore, the transformations from abc stationary reference frame to dq rotating reference frame are expressed as:

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 \\ -\sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{A.12}$$

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\Pi}{3}) & \cos(\theta + \frac{2\Pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\Pi}{3}) & -\sin(\theta + \frac{2\Pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{A.13}$$

Aligning the d-axis with the vector f (both rotating with the same angle (θ)), this yields to:

$$f_d = \tfrac{2}{3}(\cos(\theta) f_a + \cos(\theta - \tfrac{2\Pi}{3}) f_b + \cos(\theta + \tfrac{2\Pi}{3}) f_c) \tag{A.14}$$

$$f_q = 0 \tag{A.15}$$

The transformation from a three-phase abc reference frame to dq rotating reference frame is known as Park transformation [164]. However, in order to transform from dq

rotating reference frame to abc stationary reference frame, the inverse transformation is obtained as follows:

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 1 \\ \cos(\theta - \frac{2\Pi}{3}) & -\sin(\theta - \frac{2\Pi}{3}) & 1 \\ \cos(\theta + \frac{2\Pi}{3}) & -\sin(\theta + \frac{2\Pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} \tag{A.16}$$

$$f_{abc} = A f_{dq} \tag{A.17}$$

where:

$$f_{abc} = \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{A.18}$$

$$f_{dq} = \begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} \tag{A.19}$$

$$A = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 1 \\ \cos(\theta - \frac{2\Pi}{3}) & -sin(\theta - \frac{2\Pi}{3}) & 1 \\ \cos(\theta + \frac{2\Pi}{3}) & -sin(\theta + \frac{2\Pi}{3}) & 1 \end{bmatrix} \tag{A.20}$$

where A is the matrix to transform from abc axes to dq axes.

The space vector of f can be presented as follows:

$$f = f_a + a f_b + a^2 f_c \tag{A.21}$$

$$f = f_d + j f_q = (f_\alpha + j f_\beta) e^{(-j\omega t)} = \frac{2}{3}(f_a + f_b e^{(-\frac{2\Pi}{3})} + f_c e^{(\frac{2\Pi}{3})}) e^{(-j\omega t)} \tag{A.22}$$

A.1.3 Three-phase Components as a Function of Sine

Now, considering a three-phase balanced system abc has a clockwise phase sequence (abc) (i.e., $f_a(t)$ lags $f_b(t)$ by 120 electrical degrees) as depicted in Figure A-3.

Therefore, the three-phase time-varying components are represented as a function of

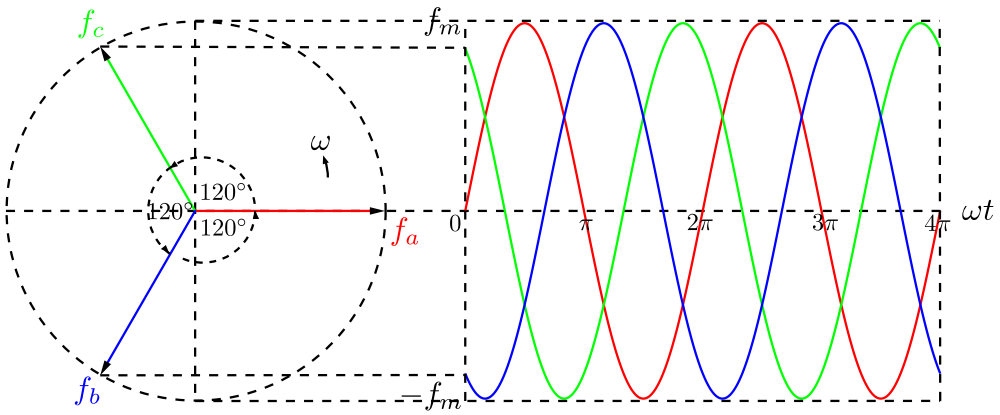


Figure A-3: Three phase balanced system as a function of sine.

sine as follows:

$$f_a(t) = f_m \sin(\omega \cdot t) \tag{A.23}$$

$$f_b(t) = f_m \sin(\omega \cdot t - \tfrac{2\Pi}{3}) \tag{A.24}$$

$$f_c(t) = f_m \sin(\omega \cdot t + \tfrac{2\Pi}{3}) \tag{A.25}$$

As it can seen from Figure A-4, the α-axis is aligned 90 degrees behind a-axis

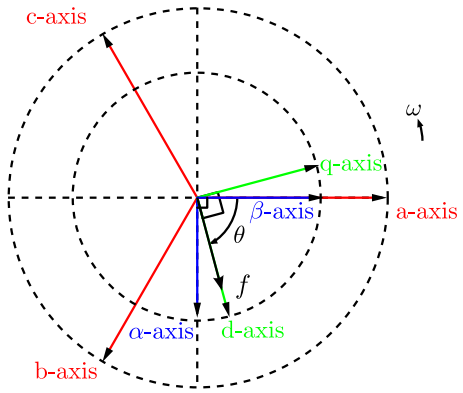


Figure A-4: The relationship between the abc stationary reference frame, the $\alpha\beta$ stationary reference frame and the dq rotating reference frame.

Therefore, the dq components will be as follows:

$$f_{d\_new} = -f_q \tag{A.26}$$

$$f_{q\_new} = f_d \tag{A.27}$$

A.2 Three-Phase Power in dq Axes

In order to obtain the instantaneous active and reactive power in terms of dq reference frame variables. Starting by the grid apparent power for three-phase balanced system is obtained as follows [6, 162]

$$S_G = V_{G_a} {I_{G_a}}^* + V_{G_b} I_{G_b}^* + V_{G_c} I_{G_c}^* \tag{A.28}$$

$$S_G = V_{G_{abc}}^T I_{G_{abc}}^* \tag{A.29}$$

$$S_G = V_{G_{dq}}^T A^T A^* I_{G_{dq}}^* \tag{A.30}$$

where:

- S_G is the apparent grid power in Volt-Amps,
- V_{G_a}, V_{G_b} and V_{G_c} are the grid voltages in a, b and c, respectively, in Volts,
- I_{G_a}, I_{G_b} and I_{G_c} are the grid currents in a, b and c, respectively, in Amps,
- $V_{G_{abc}}$ is the grid voltage in abc axes in Volts,
- $I_{G_{abc}}$ is the grid current in abc axes in Amps,
- $V_{G_{dq}}$ is the grid voltage in dq axes in Volts,
- $I_{G_{dq}}$ is the grid current in dq axes in Amps.

It is found that $A^T = \frac{3}{2} A^{-1}$ and $A^{-1} \cdot A = 1$. This yields to:

$$S_G = \frac{3}{2} V_{G_{dq}}^T A^{-1} A I_{G_{dq}}^* \tag{A.31}$$

$$S_G = \frac{3}{2} V_{G_{dq}}^T I_{G_{dq}}^* \tag{A.32}$$

$$S_G = \frac{3}{2} (V_{G_d} + jV_{G_q})(I_{G_d} - jI_{G_q}) \tag{A.33}$$

$$S_G = \frac{3}{2} (V_{G_d} I_{G_d} - jV_{G_d} I_{G_q} + jV_{G_q} I_{G_d} + V_{G_q} I_{G_q}) \tag{A.34}$$

$$S_G = \underbrace{\frac{3}{2} (V_{G_d} I_{G_d} + V_{G_q} I_{G_q})}_{P_{\mathrm{G}}} + j \underbrace{\frac{3}{2} (V_{G_q} I_{G_d} - V_{G_d} I_{G_q})}_{Q_G} \tag{A.35}$$

where:

- I_{G_d} is the grid current in d-axis in Amps,
- I_{G_q} is the grid current in q-axis in Amps,
- Q_G is the reactive grid power in Volt-Amps-Reactive.

Then, the instantaneous active and reactive power are obtained as follows:

$$P_G = \frac{3}{2}(V_{G_d} I_{G_d} + V_{G_q} I_{G_q}) \tag{A.36}$$

$$Q_G = \frac{3}{2}(V_{G_q} I_{G_d} - V_{G_d} I_{G_q}) \tag{A.37}$$

A.3 Three-Phase Inductor Voltage in dq Axes

In order to calculate the inductor voltage, the differential of the A is needed to be calculated:

$$\frac{dA}{dt} = \frac{d\theta}{dt}\begin{bmatrix} -\sin(\theta) & -\cos(\theta) & 0 \\ -\sin(\theta - \frac{2\Pi}{3}) & -\cos(\theta - \frac{2\Pi}{3}) & 0 \\ -\sin(\theta - \frac{4\Pi}{3}) & -\cos(\theta - \frac{4\Pi}{3}) & 0 \end{bmatrix} \tag{A.38}$$

$$\frac{dA}{dt} = j\frac{d\theta}{dt}\begin{bmatrix} \cos(\theta) & -\sin(\theta) & 1 \\ \cos(\theta - \frac{2\Pi}{3}) & -\sin(\theta - \frac{2\Pi}{3}) & 1 \\ \cos(\theta - \frac{4\Pi}{3}) & -\sin(\theta - \frac{4\Pi}{3}) & 1 \end{bmatrix} \tag{A.39}$$

$$\frac{dA}{dt} = j\omega A \tag{A.40}$$

The decoupling term is needed to be calculated [6]. Therefore, the three-phase inductor voltage is calculated as follows:

$$V_{L_{f_{abc}}}(t) = I_{L_{f_{abc}}}(t) R_f + L_f \frac{dI_{L_{f_{abc}}}(t)}{dt} \tag{A.41}$$

$$AV_{L_{f_{dq}}}(t) = AI_{L_{f_{dq}}}(t) R_f + L_f \frac{dAI_{L_{f_{dq}}}(t)}{dt} \tag{A.42}$$

$$AV_{L_{f_{dq}}}(t) = AI_{L_{f_{dq}}}(t) R_f + L_f A \frac{dI_{L_{f_{dq}}}(t)}{dt} + L_f I_{L_{f_{dq}}}(t) \frac{dA}{dt} \tag{A.43}$$

$$AV_{L_{f_{dq}}}(t) = AI_{L_{f_{dq}}(t)} R_f + L_f A \frac{dI_{L_{f_{dq}}}(t)}{dt} + L_f I_{L_{f_{dq}}}(t) j\omega A \tag{A.44}$$

where:

- $V_{L_{f_{abc}}}$ is the voltage across the inductor in abc axes in Volts,
- $I_{L_{f_{abc}}}$ is the current in the inductor in abc axes in Amps,
- $V_{L_{f_{dq}}}$ is the voltage across the inductor in dq axes in Volts,
- $I_{L_{f_{dq}}}$ is the current in the inductor in dq axes in Amps.

Then, multiplying both sides in Equation (A.44) by A^{-1} as follows:

$$A^{-1}AV_{L_{f_{dq}}}(t) = A^{-1}AI_{L_{f_{dq}}}(t)R_f + A^{-1}L_fA\frac{dI_{L_{f_{dq}}}(t)}{dt} + A^{-1}L_fI_{L_{f_{dq}}}(t)j\omega A \tag{A.45}$$

After that, $A^{-1} \cdot A = 1$, this yields to:

$$V_{L_{f_{dq}}}(t) = I_{L_{f_{dq}}}(t)R_f + L_f\frac{dI_{L_{f_{dq}}}(t)}{dt} + L_fI_{L_{f_{dq}}}(t)j\omega \tag{A.46}$$

Converting from the time domain into Laplace domain:

$$V_{L_{f_{dq}}}(s) = I_{L_{f_{dq}}}(s)R_f + L_fsI_{L_{f_{dq}}}(s) + L_fI_{L_{f_{dq}}}(s)j\omega \tag{A.47}$$

$$\begin{aligned} V_{L_{f_{dq}}}(s) = {} & (I_{L_{f_d}}(s) + jI_{L_{f_q}}(s))R_f + L_fs(I_{l_{f_d}}(s) + jI_{L_{f_q}}(s)) \\ & + [I_{L_{f_d}}(s) + jI_{L_{f_q}}(s)]j\omega L_f \end{aligned} \tag{A.48}$$

$$\begin{aligned} V_{L_{f_{dq}}}(s) = {} & I_{L_{f_d}}(s)R_f + L_fsI_{L_{f_d}}(s) - I_{L_{f_q}}(s)\omega L_f \\ & + j(I_{L_{f_q}}(s)R_f + L_fsI_{L_{f_q}}(s) + I_{L_{f_d}}(s)j\omega L_f) \end{aligned} \tag{A.49}$$

$$\begin{aligned} V_{L_{f_{dq}}}(s) = {} & \underbrace{I_{L_{f_d}}(s)(R_f + L_fs) - I_{L_{f_q}}(s)\omega L_f}_{V_{L_{f_d}}(s)} \\ & + j\underbrace{(I_{L_{f_q}}(s)(R_f + L_fs) + I_{L_{f_d}}(s)j\omega L_f)}_{V_{L_{f_q}}(s)} \end{aligned} \tag{A.50}$$

Finally, the inductor voltage in d and q axes including the decoupling term is obtained as follows:

$$V_{L_{f_d}}(s) = I_{L_{f_d}}(s)(R_f + L_fs) - \underbrace{I_{L_{f_q}}(s)L_f\omega}_{\text{Decoupling Term}} \tag{A.51}$$

$$V_{L_{fq}}(s) = I_{L_{fq}}(s)(R_f + L_f s) + \underbrace{I_{L_{fd}}(s)L_f\omega}_{\text{Decoupling Term}} \tag{A.52}$$

A.4 Three-Phase Duty Cycles in dq Axes

By using KVL for the VSI, the duty cycle in dq axes is obtained as follows:

$$V_{G_{abc}} - V_{L_{f_{abc}}} - V_{abcm} = 0 \tag{A.53}$$

$$V_{G_{abc}} - V_{L_{f_{abc}}} - d_{G_{abc}}\frac{V_{DC}}{2} = 0 \tag{A.54}$$

$$AV_{G_{dq}} - AV_{L_{f_{dq}}} - Ad_{G_{dq}}\frac{V_{DC}}{2} = 0 \tag{A.55}$$

$$A^{-1}AV_{G_{dq}} - A^{-1}AV_{L_{dq}} - A^{-1}Ad_{G_{dq}}\frac{V_{DC}}{2} = 0 \tag{A.56}$$

where:

- V_{abcm} is the three-phase voltage referred to the middle point of the DC bus in abc axes in Volts,
- d_{abc} is the duty cycle in abc axes,
- $d_{G_{dq}}$ is the duty cycle in dq axes.

Again, $A^{-1} \cdot A = 1$, this yields to:

$$V_{G_{dq}} - V_{L_{f_{dq}}} - d_{G_{dq}}\frac{V_{DC}}{2} = 0 \tag{A.57}$$

$$[V_{G_d} + jV_{G_q}] - [V_{L_{f_d}} + jV_{L_{f_q}}] - [d_{G_d} + jd_{G_q}]\frac{V_{DC}}{2} = 0 \tag{A.58}$$

Then, taking only the real part, this yields to

$$V_{G_d} - V_{L_d} - d_d\frac{V_{DC}}{2} = 0 \tag{A.59}$$

$$V_{G_d} - V_{L_d} = d_d\frac{V_{DC}}{2} \tag{A.60}$$

$$d_d = \frac{V_{G_d} - V_{L_d}}{\frac{V_{DC}}{2}} \tag{A.61}$$

Now, considering only the imaginary part:

$$V_{G_q} - V_{L_q} - d_q \frac{V_{DC}}{2} = 0 \tag{A.62}$$

$$V_{G_q} - V_{L_q} = d_q \frac{V_{DC}}{2} \tag{A.63}$$

$$d_q = \frac{V_{G_q} - V_{L_q}}{\frac{V_{DC}}{2}} \tag{A.64}$$

Appendix B

Difference Equation Calculation

Contents

The continuous PI controllers and LPF and HPF filters are transformed into discrete form by using bilinear transformation (Tustin) in order to be implemented in the DSP.

B.1 Difference Equation of PI Controller

In order to get the difference equation of PI controller, Tustin method is applied by substituting for s from (8.1) in (3.9) as follows:

$$R(z) = \frac{U^{PI}(z)}{E(z)} = K_p(\frac{\frac{2}{T_s}\frac{z-1}{z+1} + \frac{1}{T_i}}{\frac{2}{T_s}\frac{z-1}{z+1}}) \tag{B.1}$$

Then, multiplying the numerator and denominator by $\frac{T_s}{2}(z+1)$ as follows:

$$\frac{U^{PI}(z)}{E(z)} = K_p(\frac{z - 1 + \frac{T_s}{2}\frac{z+1}{T_i}}{z-1}) \tag{B.2}$$

$$U^{PI}(z)z - U^{PI}(z) = K_p(\frac{T_s}{2}\frac{1}{T_i} + 1)E(z)z + K_p(\frac{T_s}{2}\frac{1}{T_i} - 1)E(z) \tag{B.3}$$

$$U^{PI}(z) = K_p(\frac{T_s}{2}\frac{1}{T_i} + 1)E(z) + K_p(\frac{T_s}{2}\frac{1}{T_i} - 1)E(z)z^{-1} + U^{PI}(z)z^{-1} \tag{B.4}$$

Finally, the difference equation is obtained as follows:

$$U[k] = K_p(\frac{T_s}{2}\frac{1}{T_i} + 1)E[k] + K_p(\frac{T_s}{2}\frac{1}{T_i} - 1)E[k-1] + U[k-1] \tag{B.5}$$

B.2 Difference Equation of LPF

The same manipulation will be done for the LPF (3.26) by substituting for s from (8.1) in (3.26) as follows:

$$P_{BB\_ref}(z) = \frac{1}{1 + T_{BB\_LPF}(\frac{2}{T_s}\frac{z-1}{z+1})}P_{ESS\_ref}(z) \tag{B.6}$$

Then, multiplying the numerator and denominator by $\frac{T_s}{2}(z+1)$ as follows:

$$P_{BB\_ref}(z) = \frac{\frac{T_s}{2}(z+1)}{\frac{T_s}{2}(z+1) + T_{BB\_LPF}(z-1)}P_{ESS\_ref}(z) \tag{B.7}$$

$$\begin{aligned}(\frac{T_s}{2} + T_{BB\_LPF})P_{BB\_ref}(z)z + (\frac{T_s}{2} - T_{BB\_LPF})P_{BB\_ref} = \frac{T_s}{2}P_{ESS\_ref}(z)z \\ + \frac{T_s}{2}P_{ESS\_ref}(z)\end{aligned} \tag{B.8}$$

$$\begin{aligned}(\frac{T_s}{2} + T_{BB\_LPF})P_{BB\_ref}(z)z = \frac{T_s}{2}P_{ESS\_ref}(z)z + \frac{T_s}{2}P_{ESS\_ref}(z) \\ - (\frac{T_s}{2} - T_{BB\_LPF})P_{BB\_ref}\end{aligned} \tag{B.9}$$

After that, dividing both sides by $((\frac{T_s}{2} + T_{BB\_LPF})z)$, yields to:

$$\begin{aligned}P_{BB\_ref}(z) = \frac{\frac{T_s}{2}}{(\frac{T_s}{2} + T_{BB\_LPF})}P_{ESS\_ref}(z) + \frac{\frac{T_s}{2}}{(\frac{T_s}{2} + T_{BB\_LPF})}P_{ESS\_ref}(z)z^{-1} \\ - \frac{(\frac{T_s}{2} - T_{BB\_LPF})}{(\frac{T_s}{2} + T_{BB\_LPF})}P_{BB\_ref}\end{aligned} \tag{B.10}$$

Finally, the difference equation of the LPF is obtained as follows:

$$P_{BB\_ref}[k] = \frac{\frac{T_s}{2}}{(\frac{T_s}{2}+T_{BB\_LPF})}P_{ESS\_ref}[k] + \frac{\frac{T_s}{2}}{(\frac{T_s}{2}+T_{BB\_LPF})}P_{ESS\_ref}[k-1] - \frac{(\frac{T_s}{2}-T_{BB\_LPF})}{(\frac{T_s}{2}+T_{BB\_LPF})}P_{BB\_ref}[k-1] \tag{B.11}$$

B.3 Difference Equation of HPF

The same manipulation will be done for the HPF (3.73) by substituting for s from (8.1) in (3.73) as follows:

$$P_{ESS\_tr\_ref}(z) = \frac{T_{ESS\_HPF}(\frac{2}{T_s}\frac{z-1}{z+1})}{1+T_{ESS\_HPF}(\frac{2}{T_s}\frac{z-1}{z+1})}P_{O\_meas}(z) \tag{B.12}$$

Then, multiplying the numerator and denominator by $\frac{T_s}{2}(z+1)$ as follows:

$$P_{ESS\_tr\_ref}(z) = \frac{T_{ESS\_HPF}(z-1)}{\frac{T_s}{2}(z+1)+T_{ESS\_HPF}(z-1)}P_{O\_meas}(z) \tag{B.13}$$

$$(\frac{T_s}{2}+T_{ESS\_HPF})P_{ESS\_tr\_ref}(z)z + (\frac{T_s}{2}-T_{ESS\_HPF})P_{ESS\_tr\_ref}(z) = T_{ESS\_HPF}P_{O\_meas}(z)z - T_{ESS\_HPF}P_{O\_meas}(z) \tag{B.14}$$

$$(\frac{T_s}{2}+T_{ESS\_HPF})P_{ESS\_tr\_ref}(z)z = T_{ESS\_HPF}P_{O\_meas}(z)z - T_{ESS\_HPF}P_{O\_meas}(z) - (\frac{T_s}{2}-T_{ESS\_HPF})P_{ESS\_tr\_ref}(z) \tag{B.15}$$

After that, dividing both sides by $((\frac{T_s}{2}+T_{ESS\_HPF})z)$, yields to:

$$P_{ESS\_tr\_ref}(z) = \frac{T_{ESS\_HPF}}{(\frac{T_s}{2}+T_{ESS\_tr\_HPF})}P_{O\_meas}(z) - \frac{T_{ESS\_HPF}}{(\frac{T_s}{2}+T_{ESS\_HPF})}P_{O\_meas}(z)z^{-1} - \frac{\frac{T_s}{2}-T_{ESS\_HPF}}{(\frac{T_s}{2}+T_{ESS\_HPF})}P_{ESS\_ref}(z)z^{-1} \tag{B.16}$$

Finally, the difference equation of the HPF is obtained as follows:

$$P_{ESS\_tr\_ref}[k] = \frac{T_{ESS\_tr\_HPF}}{(\frac{T_s}{2} + T_{ESS\_HPF})} P_{O\_meas}[k] - \frac{T_{ESS\_HPF}}{(\frac{T_s}{2} + T_{ESS\_HPF})} P_{O\_meas}[k-1] - \frac{\frac{T_s}{2} - T_{ESS\_HPF}}{(\frac{T_s}{2} + T_{ESS\_HPF})} P_{ESS\_ref}[k-1] \tag{B.17}$$

Appendix C

Publications

Contents

C.1 Publication I

R. Georgious, J. García, Á. Navarro-Rodríguez and P. García, "A Study on the Control Design of Non-Isolated Converter Configurations for Hybrid Energy Storage Systems", in IEEE Transactions on Industry Applications.

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A Study on the Control Design of Non-Isolated Converter Configurations for Hybrid Energy Storage Systems

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***Abstract*—This paper is focused on the control strategies for non-isolated Hybrid Energy Storage Systems (HESSs) in power support applications for microgrids and nanogrids. The hybrid storage system under analysis consists of two storage units with significantly different ratings and characteristics. These units are interfaced to the main system through dedicated power converters with coordinated control schemes to manage the power flows according to the system requirements.**

Firstly, the most relevant candidate options for the power electronics topology configurations in nanogrid applications are selected. These target solutions are reduced to two possibilities: the first one based on independent bidirectional boost converters for each device, the second one based on the Series Parallel Connection (SPC) of the storage units.

Then, the basic control scheme is implemented at each of these topologies. This allows to compare the performance of each solution considering static aspects, such as gain limitations, efficiency or power density, but also considering the dynamic behavior.

Finally, a strategy to design the control loops of the resulting HESS is proposed, studied, simulated and experimentally implemented on a 2 kW demonstrator. The reported results show how the proposed control strategy applied to the SPC presents better performance in terms of dynamic behavior and steady state operation.

***Index Terms*—Hybrid Energy Storage System, Boost Converter, Non-Isolated Storage System, Nanogrid.**

I. Introduction

NOWADAYS, Energy Storage Systems (ESSs) are considered as a key tool in the development of power systems, and particularly in the field of microgrids and nanogrids design. These ESSs are able to mitigate the effects of the power fluctuations coming from the generation plants and the load demands, as well as to supply the power mismatch between generation and demand [1]–[4]. These ESSs can be applied to AC or DC microgrids and nanogrids [5]–[7]. This work will consider an ESS applied to one of such DC nanogrids.

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In general, DC microgrids and nanogrids present better efficiency, stability and reliability compared to AC ones. In fact, due to the reported trend to increase the amount of final DC loads in household and industry consumers [8], the use of DC microgrids prevents extra conversion steps from DC to AC and finally to DC again, but it also avoids the need for grid synchronization control algorithms [9]. On the other hand, AC microgrids and nanogrids have some key advantages, such as the implementation of protections, the fault management, etc. In addition, AC distribution relays on a more mature technology, hence there is a huge number of available electronic loads designed for a direct connection to the AC grid [8]. But in any case, for a DC microgrid or nanogrid like the one depicted in Fig. 1, the AC units need an AC/DC converter to connect to the main DC bus, while the units with DC power are connected either directly to the DC bus or through DC/DC converters [10], [11].

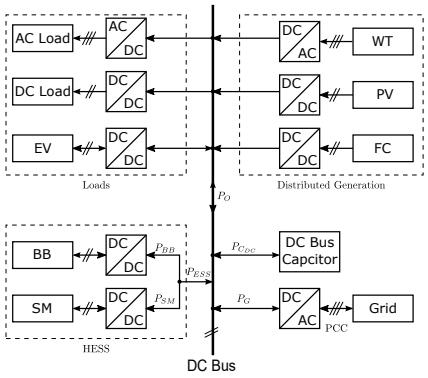

Fig. 1: The power balance in a DC microgrid.

Among all the possible options for implementing ESSs in DC microgrids, Hybrid ESSs (HESSs) become the most versatile in terms of performance and cost optimization [12]. These HESS combine a bulk energy storage device, usually presenting slow-dynamics, with a high-power fast-dynamics storage module [13]–[18]. For the bulky energy device, one suitable option for nanogrid applications is the selection of electrochemical Battery Banks (BBs). Among all the possible technologies, Lithium-Ion batteries are one of the preferred choices due their overall performance [19]. An interesting option for the fast, high-power counterpart to hybridize these

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batteries is the use of Supercapacitor Modules (SMs) [20], [21]. The philosophy underlying these HESS is to obtain a global system that combines the energy storage capabilities of the BB and the power ratings of the SM. This results in a decrease of the overall system costs (by reducing the battery size and increasing its operating lifespan [2], [12]) and an increase in the system reliability (by decreasing stresses at both the battery and the dedicated converter during transient stages) [3], [4], [22], [23].

The target ESS devices are interfaced to the DC bus through Power Electronics Converters (PECs), that adapt the electric parameters from both sides and also control and coordinate the power flows from the HESS to the nanogrid and vice-versa [14]. Among all the possibilities of the configuration of these HESS, the most simple connection able to fully control all the power flows is the Parallel Connection (PC) [1], [24]–[27], shown in Fig. 2. This scheme is based on two bidirectional boost converters connected to the DC bus. Yet being a simple, well-known and compact solution, its main limitations come in the event of a high voltage mismatch between one of the storage devices voltage ratings (usually the SM) and the DC bus voltage. In the nanogrid under study, the DC bus nominal voltage considered as reference value in the target application is 500 V. Considering a design BB voltage rating of around half the DC bus nominal voltage, then the duty ratio of the converter at the battery leg will be around 50%, thus optimizing the performance of such converter in terms of stresses balancing, design complexity and control capability. However, provided that in some applications the SM voltage rating is ranged from 20V to 40V, then, for this DC bus voltage rating, the required gains for the dedicated interfacing converter will reach values up to 25:1 or even higher.

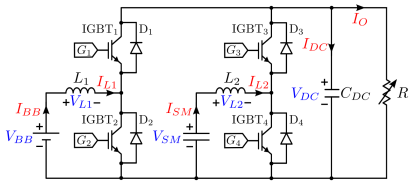

Fig. 2: PC of two bidirectional boost converters connected to a BB and to a SM.

Such requirements cannot be accomplished by the parallel boost arrangement, nor for the rest of the commonly used single-stage non-isolated converter topologies [28], [29]. But even for practical gain values (for instance 10:1), the bidirectional boost converter experiences an increase in the unbalance of the current stresses on the upper and lower switches, a decrease in the control margin of the converter, more sensitivity to parasitic elements, etc. [29]. More complex alternatives can be used to solve the problem of voltage mismatch, including cascaded stages, multilevel or even isolated approaches. Some of these options are the parallel configuration of two Dual Active Bridges (DABs) [30]–[34], the use of triple active bridge [35]–[37], as well as power stages based on resonant converters [38] or multilevel converters [39]. However, these solutions yield to higher costs, losses and system complexity due to the increase in the number of switches and passive elements [29].

To overcome these drawbacks, a solution that prevents from moving to more complex schemes is the Series Connection (SC) [40], [41] of the storage systems. This solution aims to avoid the low duty cycles ratios at the SM branch. However, the main drawbacks of this connection is that at the end the BB needs to provide also the SM peak current, disserving the lifespan of the BB. To cope with this issue, the Series-Parallel Connection (SPC) depicted in Fig. 3 has been introduced as an option for HESS in nanogrid applications [42], [43]. As shown in Fig. 3, the negative terminal of the SM is connected to the middle point of the leg connected to the BB.

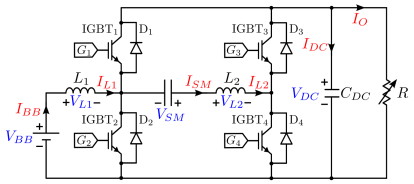

Fig. 3: SPC of two bidirectional boost converters connected to BB and SM and sharing the DC bus.

This work is thus focused on the study of the control of a Hybrid BB/SM ESS for nanogrid applications, interfaced by the SPC scheme, and its comparison vs. the standard parallel boost converter option. The paper is organized as follows: Section II compares in depth the SPC to the conventional PC. Section III briefly discusses the main design parameters of the converters. Next, section IV proposes the control scheme required for the control of both the PC and the SPC schemes. After that, section V shows the validation of the proposed system through simulations. Then, Section VI shows experimental results to demonstrate the performance of the proposed solution. Finally, Section VII summarizes the work done and discusses the future developments.

II. Comparison of Configurations

The system targeted in this research is defined ahead, considering the HESS shown in Fig. 1. This HESS has a rated power of 2kW, and includes two individual commercial storage systems. The first storage device, a Lithium-Ion BB (Rook 48×5 module from CEGASA PORTABLE ENERGY) is interfaced by a dedicated PEC. Analogously, the second device, a SM (BMOD0165 P048 C01 from Maxwell Technologies) is also attached to the DC bus by means of a PEC. The rated operating values of the system and the individual parts are given in Table I. The performance of the HESS will initially be assessed in steady state.

Upon the conventional PC scheme, the well-known boost converter equations under complementary switching pattern are fulfilled. Therefore the corresponding duty cycles at steady state for the $IGBT_1$ (at the leg connected to the battery) and $IGBT_3$ (at the leg connected to the SM), d_{BB} and d_{SM}, keep the following expressions:

$$d_{BB} = \frac{V_{BB}}{V_{DC}} = 50\% \tag{1}$$

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TABLE I: Rated Operating Parameters of the Target HESS.

Parameter	Symbol	Value	Units
Nominal BB voltage	V_{BB}	240	V
Rated continuous BB charging current (0.5C)	I_{BB}	-24	A
Rated continuous BB discharging current (1C)	I_{BB}	48	A
Rated SM voltage	V_{SM}	48	V
Capacitance of the SM	C_{SM}	165	F
DC bus voltage	V_{DC}	500	V

$$d_{SM} = \frac{V_{SM}}{V_{DC}} = 6\% \tag{2}$$

where V_{BB}, V_{SM} and V_{DC} are the BB, the SM and the DC bus voltage values in Volts, respectively.

Thus, for the parameters under consideration (250V BB, 30V SM, 500V DC bus), $IGBT_3$ is turned on 6% of the switching time, while $IGBT_4$ is turned on 94% of the switching time as shown in Fig. 4a. The small duty cycle of the SM leg yields to thermal and electrical stresses mismatch on the switches at this leg. These constraints of the duty cycle also limit the switching frequency. On the other hand, after a detailed analysis of the SPC scheme [41], it can be seen how the following equation applies to the leg formed by $IGBT_3$ and $IGBT_4$:

$$V_{BB} - V_{L_1} + V_{SM} - V_{L_2} = d_{SM} V_{DC} \tag{3}$$

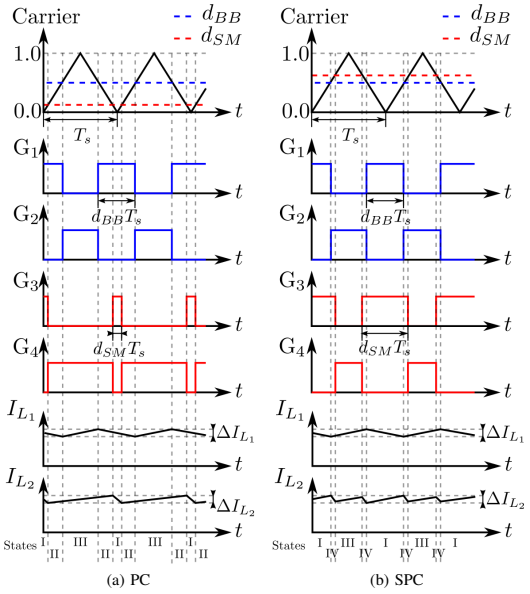
where V_{L_1} and V_{L_2} are the voltages in the inductors connected to the BB and to the SM in Volts, respectively.

Upon steady state condition, the inductor voltages are null; therefore, the value of the duty ratio at the SM leg is given by:

$$d_{SM} = \frac{V_{BB} + V_{SM}}{V_{DC}} = 56\% \tag{4}$$

The value of the duty ratio at the battery leg is given by (1). With the same voltage values than in the PC case, $IGBT_3$ is turned on 56% and $IGBT_4$ is turned on 44% of the switching time in the SPC scheme as shown in Fig. 4b. This yields to a balance on the thermal stress on the switches for the SM leg. In the aforementioned connection, the duty cycle of the $IGBT_3$ is a function of the supercapacitor and battery voltages, not only of the supercapacitor voltage as in case of PC. Therefore, the stresses in the switches of the SM leg are much more balanced than in the previous case, yielding to a better performance in terms of reliability and increased control margin.

The main drawback is the appearance of circulating extra currents through the switches of the battery leg in the SPC. However, as it was demonstrated in [41], in the case of using the SM subsystem for transient compensation of power demands, where most of the time the current reference for the SM will be null, this issue is not a concern. Thus, the SPC is an option for some applications of HESS with high voltage ratings mismatch. Nevertheless, in order to fully assess its performance, a deep analysis of the control system required to govern the power flows in the converter is still needed. This study is the focus of the present work.



(a) PC (b) SPC

Fig. 4: Switching states of the PC and SPC of two bidirectional boost converters, as a function of the relative values of the duty cycles.

III. Design of the Converters

This section shows the basic design procedure for the PC scheme, aiming to define the main parameters of the power topology. The BB converter is designed in a first stage. The nominal values for the voltage ratings for the converter design are given in Table I. However, the design must ensure that the converters can operate within a given range for the operational voltage values at every port of the converter. These design limits are expressed in Table II.

TABLE II: Limits of the Operating Parameters.

Parameter	Symbol	Value	Units
Minimum BB voltage (0% SOC)	V_{BB_min}	178.5	V
Maximum BB voltage (100% SOC)	V_{BB_max}	273.75	V
Minimum SM voltage	V_{SM_min}	20	V
Maximum SM voltage	V_{SM_max}	51	V
Minimum DC Bus voltage	V_{DC_min}	400	V
Maximum DC Bus voltage	V_{DC_max}	700	V
Minimum load power	P_{O_min}	-2	kW
Maximum load power	P_{O_max}	2	kW

The value of the inductance of the boost converter, given from the general equations of this topology in continuous operation mode, is given by [44]:

$$L_1 = \frac{V_{BB}(1 - \frac{V_{BB}}{V_{DC}})}{f_s \Delta I_{L_1}} \tag{5}$$

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where:

- f_s is the switching frequency of the converter, in Hz,
- ΔI_{L_1} is the current ripple of the BB inductor, in Amps.

Thus, the value of the inductor depends on the target current ripple for each application, as well as on the voltage levels at both the BB and the DC bus. About this High Frequency (HF) current ripple, it must be noticed that this inductor is directly connected in series with the battery. Therefore, the inductor ripple is the HF current ripple through the battery. Even though it is not clear from the existing literature that the HF current ripple affects the State of Health (SOH) of the battery in the long term [45], [46], this parameter is kept relatively low in order to ensure proper operation of the converter. This implies a relatively large inductance value; however, this is not a understood as a concern in the design, given that no major weight or size constraints are envisaged for the static application of power support in microgrids. The target value for this parameter is:

$$\delta I_{L_1} < 0.1 \tag{6}$$

$$\Delta I_{L_1} = \delta I_{L_1} \cdot I_{L_{1\_avg}} = \delta I_{L_1} \cdot \frac{P_{O\_max}}{V_{BB}} \tag{7}$$

where:

- δI_{L_1} is the per unit (p.u.) value of the peak to peak current ripple at the inductor L_1,
- $I_{L_{1\_avg}}$ is the average value of the current through L_1, in Amps.

Combining this parameter with the worst-case scenario for the input voltage magnitudes involved (i.e. maximum values for V_{DC} and V_{BB}), the value for inductor L_1 can be calculated:

$$L_1 > 11.4mH \tag{8}$$

In order to ensure some safety margin, a slightly large value has been selected for L_1. The final value selected is shown in Table III.

TABLE III: Design Values for the PC Configuration.

Parameter	Symbol	Value	Units
Inductance of the inductor connected with the BB	L_1	14	mH
Parasitic resistance of the inductor connected with the BB	R_1	0.2	Ω
Inductance of the inductor connected with the SM	L_2	7	mH
Parasitic Resistance of the inductor connected with the SM	R_2	0.1	Ω
Capacitance of the DC bus	C_{DC}	470	μF

For the SM converter inductor, the same formulation is used:

$$L_2 = \frac{V_{SM}(1 - \frac{V_{SM}}{V_{DC}})}{f_s \Delta I_{L_2}} \tag{9}$$

where ΔI_{L_2} is the current ripple of the SM inductor in Amps.

However, for the SM case, it must be noticed how the voltage values at the storage device are significantly smaller than in the battery case, yielding to much higher current levels. The target current level is decreased down to:

$$\delta I_{L_2} < 0.01 \tag{10}$$

$$\Delta I_{L_2} = \delta I_{L_2} \cdot I_{L_{2\_avg}} = \delta I_{L_2} \cdot \frac{P_{O\_max}}{V_{SM}} \tag{11}$$

where

- δI_{L_2} is the p.u. value of the peak to peak current ripple at the inductor L_2,
- $I_{L_{2\_avg}}$ is the average value of the current through L_2, in Amps.

This decrease in the target current ripple is justified from the losses perspective. The HF losses in the magnetic device are a function of the square of the RMS value of the HF current harmonics, being the fundamental one the switching frequency. Hence, given that the average current flowing through the SM is high, relatively large HF current ripples imply high magnetic losses. For the worst-case scenario, the obtained value for the inductor L_2 can be calculated:

$$L_2 > 6.03mH \tag{12}$$

As a final remark, a slightly larger value has been selected, to ensure a safety margin in the design. The value at Table III is finally selected.

The DC bus capacitor is calculated considering the following equation [44]:

$$C_{DC} = \frac{I_{DC}(1 - \frac{V_{BB}}{V_{DC}})}{f_s \Delta V_{DC}} = \frac{\frac{P_{O\_max}}{V_{DC}}(1 - \frac{V_{BB}}{V_{DC}})}{f_s \Delta V_{DC}} \tag{13}$$

where:

- I_{DC} is the capacitor current in Amps,
- ΔV_{DC} is the DC bus voltage ripple in Volts.

Neglecting the effect of the capacitor ESR, and for a voltage ripple of:

$$\delta V_{DC} < 0.001 \tag{14}$$

$$\Delta V_{DC} = \delta V_{DC} \cdot V_{DC} \tag{15}$$

where δV_{DC} is the p.u. value of the peak to peak voltage ripple at the DC bus capacitor C_{DC}.

Then, once again considering the worst-case condition (minimum battery voltage and minimum DC bus voltage), the required value for the DC bus capacitance results:

$$C_{DC} > 346.1\mu F \tag{16}$$

As in the case of the inductance value, a certain safety margin has been ensured, and thus value of Table III is finally implemented. These design parameters for the reactive elements are kept unchanged for the SPC connection, in order to compare the variations due solely to the performance of the topology.

IV. Proposed Control of the Series-Parallel Connection

The following paragraphs discuss the control strategy considered in this work, as well as the proposal for the implementation in the SPC scheme. The control strategy assumes

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grid-tied operation, and considers that the DC bus voltage is controlled externally to the HESS, like for instance, through the inverter connected to the grid at the Point of Common Coupling (PCC) depicted in Fig. 1. This structure, including the control block signals, is outlined in Fig. 5. It must be noticed how the intended control scheme will not consider any kind of real-time communications between the HESS and the rest of the system. In particular, the control of the HESS is assumed to be independent of the bus control that governs the Grid PEC. Once designed, implemented and operating, the HESS will act as an independent subsystem, using only internal variables, except for an external load current sensor to determine I_O at Fig. 2. Hence, the effects of the HESS on the Grid PEC control are treated as disturbances.

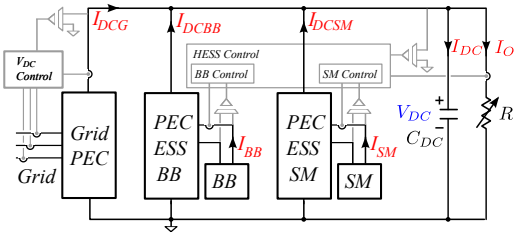

Fig. 5: Block diagram of the HESS, including the signals required for the control scheme.

The first aspect to clarify is the desired behavior of the ESS upon sudden changes in the power demand profile. This will be illustrated with the help of Fig. 6. As it can be seen, the system is initially in steady state. The grid power equals the load power, P_{O_meas} and; therefore, the power demanded from the HESS, P_{ESS_ref} is null. The P_{ESS_ref} is split into the BB and SM reference power values, P_{BB_ref} and P_{SM_ref} respectively. The measured load power is known, since:

$$P_{O\_meas} = I_{O\_meas} V_{DC\_meas} \tag{17}$$

where:

- P_{O_meas} is the measured power of the load in Watts,
- I_{O_meas} is the measured current through the load in Amps,
- V_{DC_meas} is the measured DC bus voltage in Volts.

In case an external event such as a fault or a Distribution Network Operator (DNO) triggering command forces the PCC to decouple from the grid, the system must enter into islanding mode. In this mode, the HESS takes over all the power generation during the duration of the external event. These specifications (ensured amount of power available, duration of events) can be used to design the energy capability of the battery. The SM is used to absorb the high frequency components of the power demand, while the battery reference is kept relatively constant. This prevents the battery to reach the maximum current levels given by the charge/discharge rate of the manufacturers.

However, in grid-tied operation, the main goal of the ESS is to compensate transient power variations, so as to keep constant the DC bus voltage, therefore ensuring system stability. In order to ensure the ESS ability to provide the required

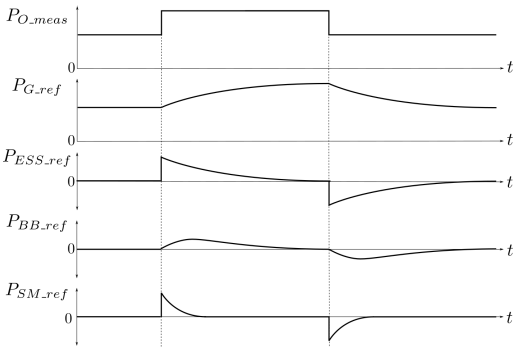

Fig. 6: Evolution of the instant power values involved in the HESS operation in grid tied operation.

energy in case of grid-tied operation, the ESS power reference will eventually be null again after the transient variations are compensated. Therefore, the power reference for the ESS is generated by passing the load power through a High Pass Filter (HPF) [47]–[49], thus obtaining similar waveforms to the ones depicted at Fig. 6. This can be defined as:

$$P_{ESS\_ref}(s) = \underbrace{\frac{T_{ESS}s}{1+T_{ESS}s}}_{\text{HPF}} P_{O\_meas}(s) \tag{18}$$

where:

- P_{ESS_ref} is the power reference for the total HESS in Watts,
- T_{ESS} is the time constant of the HPF of the ESS power in seconds,
- s is the Laplace complex variable; s = σ + j ω_d.

The Bandwidth of this HPF must be slow enough as to allow for the DC bus control. The effect of the ESS control will actually change the DC bus value. Given that there is no information interchanged between the HESS and the Grid PEC controller (except for the obvious measurement of the DC bus itself), this effect is seen as a disturbance from the point of view of the Grid PEC controller.

The bandwidth for the HPF is chosen well below the bandwidth of the DC bus voltage control loop. Thus, it is ensured that for any design of the HPF corner frequency, the components of any disturbance close to these frequencies are attenuated at the sensibility function of the voltage control loop. Assuming a bandwidth for this DC bus control of 20-30 Hz, then the bandwidth of the HPF will be chosen at least one order of magnitude smaller. For demonstration purposes, the bandwidth for this HPF is selected as:

$$f_{ESS} = 0.4Hz << BW_{DC} = 20Hz \tag{19}$$

where:

- f_{ESS} is the cut-off frequency of the HPF of the ESS power in Hz,
- BW_{DC} is the bandwidth of the DC bus voltage control loop in Hz.

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Once the power reference is defined for the full HESS, it must be noticed that the aim of the hybrid control is to force the SM to deliver or absorb the transient peaks in the demanded power profile, while ensuring that the BB delivers or absorbs the remaining ESS demanded power. Therefore, a second HPF must be implemented to generate the power reference for the SM subsystem, thus splitting the share of power between both storage subsystems:

$$P_{SM\_ref}(s) = \underbrace{\frac{T_{SM}s}{1+T_{SM}s}}_{\text{HPF}} P_{O\_meas}(s) \tag{20}$$

where:

- P_{SM_ref} is the power reference of the SM in Watts,
- T_{SM} is the time constant of the HPF of the SM power in seconds.

In this case, the bandwidth of this second HPF is calculated taking into account the limits in the power ratings of the battery (given by the charge/discharge capacity) and in the di/dt of the battery current. By keeping low the derivative of the battery current, aspects such as voltage unbalance between cells, thermal mismatch between cells/modules, or noise-triggering of battery protections are avoided, thus increasing the system reliability. Therefore, the limitation of these parameters contribute to optimize the SOH and the lifespan of the battery. Also for demonstration purposes, this value is settled as:

$$f_{SM} = 0.7Hz \tag{21}$$

where f_{SM} is the cut-off frequency of the HPF of the SM power in Hz.

Fig. 7 shows the block diagram of this control scheme, as designed for the conventional PC configuration. It must be remarked how two limiter blocks are used to ensure that the limits for both the SM and the BB power ratings are not exceeded.

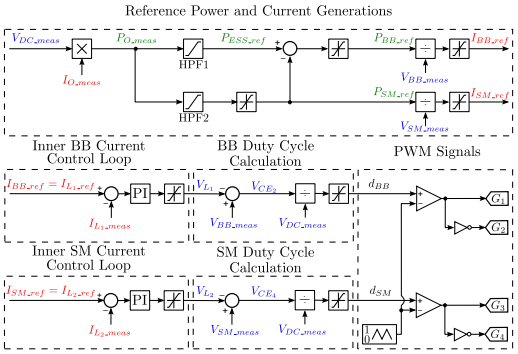

Fig. 7: Control of the PC in order to provide or absorb transient power demand as to improve the recovery of the DC bus.

Finally, the power reference for the battery control loop is obtained as a difference between the total ESS power and the SM power reference [50]–[52]. The battery power reference expression is thus defined as:

$$P_{BB\_ref} = P_{ESS\_ref} - P_{SM\_ref} \tag{22}$$

where P_{BB_ref} is the power reference of the BB in Watts. As a consequence of the structure implemented for HPF1 and HPF2, the resulting power references follow the general shapes depicted in Fig. 6. Once the power reference values for both the BB and the SM subsystems are obtained, the current references of the BB and SM loops are calculated by dividing these power magnitudes by the BB and SM measured voltages, respectively [53]. From Fig. 3, the current flowing through the BB (and SM) inductor is also the current flowing through the BB (and SM) itself. Thus, the BB (and SM) current control is indeed an inductor current control.

Through the V-I characteristic of these inductors, two independent current control loops can be implemented, one at each of the storage devices, simplifying the control design, and allowing for a different dynamic behavior of each of these subsystems. Therefore, typical ideal-form Proportional Integral (PI) current controllers are selected as regulators:

$$C(s) \quad = \quad K_p\left(1+\frac{1}{T_i s}\right) \tag{23}$$

where:

- C(s) is the transfer function of the PI controller,
- K_p is the proportional gain,
- K_i is the integral gain.

These PI controllers are tuned to ensure that the references are tracked adequately. In order to do so, these controllers will be made as fast as possible. Thus, the system will be taken to the operational limits, including saturation of the controller. However, an anti-windup method will be implemented to prevent the uncontrolled operation upon saturation of the PI regulator [1].

The output of these controllers are the respective inductor voltages (see Fig. 7). Therefore, these limits for the voltages at the inductors in the PC are calculated as follows:

$$V_{L_1\_min} = V_{BB\_min} - V_{DC\_ref} \tag{24}$$

$$V_{L_1\_max} = V_{BB\_max} \tag{25}$$

$$V_{L_2\_min} = V_{SM\_typ} - V_{DC\_ref} \tag{26}$$

$$V_{L_2\_max} = V_{SM\_typ} \tag{27}$$

where:

- V_{L1_min}, V_{L1_max}, V_{L2_min} and V_{L2_max}: are the minimum and maximum inductor voltages in Volts for the BB and SM boost converters, respectively,
- V_{BB_min} and V_{BB_max} are the minimum and maximum battery voltage values, respectively, defined by the manufacturer ratings, in Volts,
- V_{SM_typ} is the value, in Volts, of the SM voltage that ensures the same amount of energy available for charging and for discharging, obtained through the expression:

$$V_{SM\_typ} = \sqrt{\frac{V_{SM\_max}^2 + V_{SM\_min}^2}{2}} \tag{28}$$

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With these inductor values, the bandwidths of the PI controllers can be selected. The chosen value, for each of the current loops involved, is that of a typical second order system with a rising (and falling) time corresponding to saturation of the controller:

$$T_r \simeq 1.8 \cdot \frac{1}{\omega_n}, \omega_n = 2 \cdot \pi \cdot Bw \tag{29}$$

where:

- T_r is the rising (or falling) time, in this case of the inductor current, from 10% to 90% of steady state value, in seconds,
- ω_n is the natural frequency of the equivalent system, in rad/s,
- Bw is the bandwidth of the current loop, in Hz.

In the case of the battery for a positive current step, if the output of the controller is saturated, the voltage at the inductor is clamped at its maximum possible value, $V_{L1clamp}$:

$$V_{L1\_clamp} = V_{L_1\_max} \tag{30}$$

The step value of the inductor current from the steady state value, $I_{L_1\_max}$, corresponds to:

$$I_{L_1\_max} = \frac{P_{step}}{V_{L_1\_max}} \tag{31}$$

And thus, the rise time is given by:

$$T_r = (0.9 - 0.1) \cdot \frac{I_{L_1\_max} \cdot L_1}{V_{L_1\_clamp}} \tag{32}$$

From (29) and (32), the value of the bandwidth for the maximum battery voltage and positive current step can be calculated:

$$Bw_{I1_{VmaxImax}} \simeq \frac{1.8 \cdot V_{L1clamp}}{2\pi \cdot 0.8 \cdot L_1 \cdot I_{L_1\_max}} \tag{33}$$

In a similar manner, this parameter is calculated for the rest of the boundary conditions (minimum possible battery voltage, decreasing current step), in order to find the minimum bandwidth. This minimum value for the bandwidth ensures that the design will be adequate in all cases. The same procedure is carried out in the case of the SM, but in this case considering only the V_{SMtyp} value. This procedure finally allows to select the values of the bandwidths for both the battery and the SM current controllers.

Besides, some extra calculations are required to compute the control actions on the control loops, in this case the duty ratios of both legs, from the obtained values for the voltages at the inductors. For the PC in Fig. 2, and considering the transient state, the relationships for the duty cycles are found as follows:

$$d_{BB} = \frac{V_{BB} - V_{L1}}{V_{DC}} \tag{34}$$

$$d_{SM} = \frac{V_{SM} - V_{L2}}{V_{DC}} \tag{35}$$

These instant values of the duty ratios state the capability of the converter for providing a given transient voltage to the inductors in the converter legs; therefore, yielding to a given current by those inductors. As mentioned earlier, in addition to stresses unbalance in the switches and poor performance due to extreme duty ratios, the main problem in the PC comes from the fact that in the SM leg, the starting value of the duty ratio is quite small (6%). This is due to the fact that the discharging voltage for the SM inductor in the case of positive current step is limited to V_{SMtyp}.

If a high SM charging current is required, the control system acts providing a high duty ratio to this leg. For this reason, the resulting voltage in the SM inductor increases noticeably (up to 450-500V), and therefore, a very high SM charging current can be achieved. On the other hand, when a high discharging SM current is desired, the duty ratio of the SM leg cannot be smaller than zero (saturation of the controller), so consequently the discharging voltage in this inductor is limited to the SM voltage (for example 30V). Thus, the discharging current is significantly smaller than the charging one. This results in a non-symmetric behavior of the control, which is not admissible for a transient compensating scheme [41].

However, in the alternate SPC scheme at Fig. 3, it was stated from (3) that the duty cycle of $IGBT_3$ at the SM branch is also a function of the BB voltage. This ultimately yields to an extension on the values that the SM inductor might take during the transient, and therefore extending the range of symmetrical behavior. For this reason, in the case of implementing this control in the SPC scheme, the following relationships of the duty cycles are derived from (3):

$$d_{BB} = \frac{V_{BB} - V_{L_1}}{V_{DC}} \tag{36}$$

$$d_{SM} = \frac{V_{SM} - V_{L_2} + V_{BB} - V_{L_1}}{V_{DC}} \tag{37}$$

Fig. 8 shows the proposed control when implemented for the SPC scheme. The differences with the control schemes implemented in Fig. 7 for the PC configuration are the following:

- The calculation of the duty cycle of the SM branch parting from the output of the PI controller.
- The limit for the SM inductor maximum voltage values is now given as follows:

$$V_{L_2\_max} = V_{SM\_max} + V_{DC\_meas} \tag{38}$$

- As a result, the bandwidth at the SM branch, as calculated from (33), but for the new clamping values for the inductor voltage at the SM branch, is significantly increased. This yields not only to a symmetric behavior, but also to a faster dynamics in the SM subsystem performance.

V. Validation of the Proposed Control through Simulation

The next step in the procedure is the comparison through a simulation platform of the performance of the proposed control in both power topologies, PC and SPC. This step aims to validate the assumptions carried out during the analysis and design, and to assess the expected performance of the full HESS. The parameters used in the operating conditions of the validation procedure are listed in Table I and Table III, whereas the control design parameters implemented can be seen in Table IV. The validation has been carried out in the

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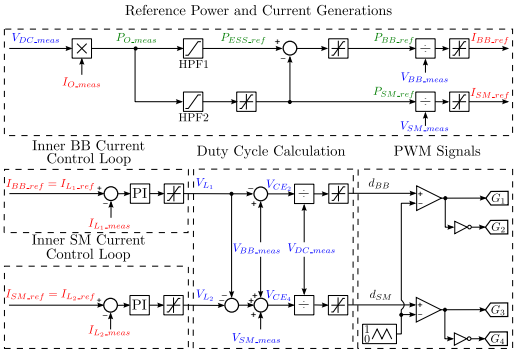

Fig. 8: Proposed control of the SPC in order to supply or absorb transient power during load variations providing the improvement of the recovery of the DC bus due to load variations.

environment MATLAB-Simulink®, considering the model of an existing prototype setup of a HESS of 2kW rated power. In this first approach, ideal components and devices have been considered.

TABLE IV: Parameters of the control of the converters.

Parameter	Symbol	Value	Units
HPF1 of the ESS power			
Cut off frequency	f_{ESS}	0.4	Hz
HPF2 of the SM power			
Cut off frequency	f_{SM}	0.7	Hz
Inner BB Current Control Loop			
Bandwidth	Bw_{BB}	500	Hz
Proportional gain	K_{pBB}	45.1133	
Integral time	$T_{i_{BB}}$	0.0422	Secs
Inner SM Current Control Loop in PC			
Bandwidth	Bw_{SM}	36	Hz
Proportional gain	K_{pSM}	1.6241	
Integral time	$T_{i_{SM}}$	0.0422	Secs
Inner SM Current Control Loop in SPC			
Bandwidth	Bw_{SM}	222	Hz
Proportional gain	K_{pSM}	10.0151	
Integral time	$T_{i_{SM}}$	0.0422	Secs
Switching frequency	f_s	20	kHz

In order to compare the results, an initial State of Charge (SOC) of the BB of 50% is considered in all cases. In the same way, the initial voltage value at the SM is kept constant during the test. The DC bus voltage is controlled by an inverter connected to the grid in order to maintain its value around 500 V. Initially, all the load power is being provided by the grid, and therefore the initial ESS power references are null. From the initial equilibrium operation point, two load steps of 1kW (from 833W to 1833W) and -1kW (from 1833W back to 833W) have been applied, at time instants 0.5 and 2.5 seconds, respectively.

Figure 9 shows the behavior of both topologies for an initial SM voltage of 40V. As it can be seen, both topologies are able to perform a voltage compensation for the DC bus faster than the system without the energy storage system as depicted in Fig. 10. In the first load step up transient, the initial peak power is provided by the SM, while the rest of the total transient power is delivered by the BB. After around 2 seconds, the steady state is reached again and the power is again fully delivered by the grid. A similar situation is seen for the step down transient. It is interesting to remark how, in the original PC situation, the power delivered by the SM. For the implemented design, the sudden increased power demand implies duty ratio values that are below 0%, and the controller is saturated. The SM branch stops switching for a while, the anti-windup mechanism implemented in the PI controller turns on, and only after some instants the system starts to operate again to track again the reference. Given that the steady state duty cycle for this branch is relatively small (typically a 5%), the resulting dynamics are relatively slow.

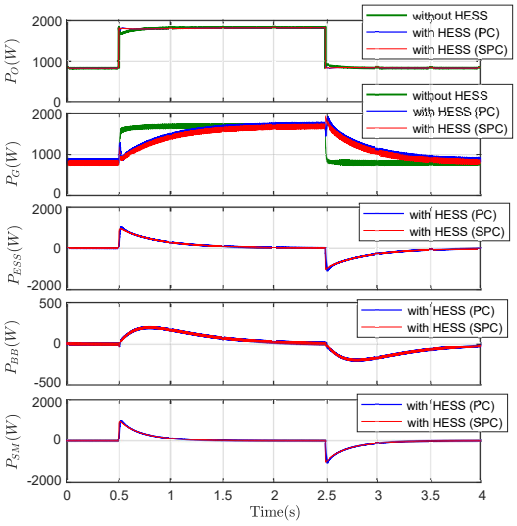

Fig. 9: Simulation results for the PC and the SPC where the load power is changed from 833.3 W to 1833.3 W at 0.5 seconds and then to 833.3 W again at 2.5 seconds.

For the mentioned design, also saturation is given in the SPC scheme, however for much faster dynamics. As the steady state initial duty ratio of this branch is closer to a 50%, well above the 5% typical values in the PC solution, the existing range for the control action, and hence the obtained bandwidth for the controller, are significantly higher. This results in the SM subsystem tracking the power reference much faster for

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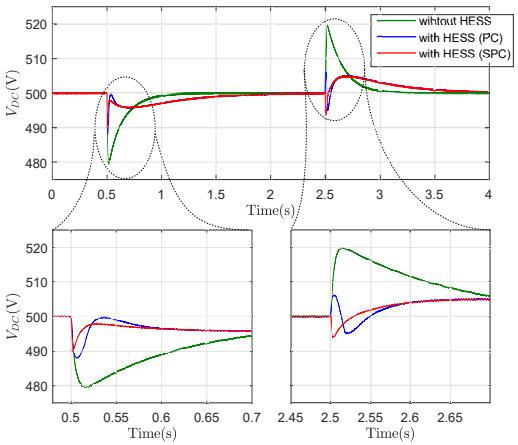

Fig. 10: Simulation results of the DC bus for the PC and the SPC where the load power is changed from 833.3 W to 1833.3 W at 0.5 seconds and then to 833.3 W again at 2.5 seconds.

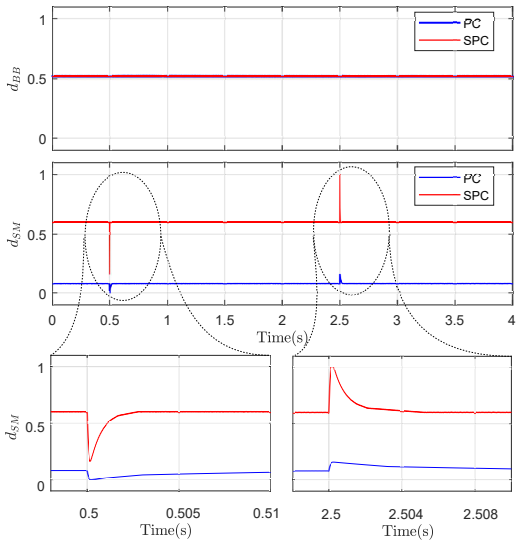

Fig. 11: Simulation results of the BB duty cycle (d_{BB}) and SM duty cycle (d_{SM}) for the PC and the SPC where the load power is changed from 833.3 W to 1833.3 W at 0.5 seconds and then to 833.3 W again at 2.5 seconds.

the proposed SPC scheme. Hence, all the aforementioned problems of the too small duty ratio obtained for the SM branch of the PC scheme are therefore solved in the SPC configuration. The evolution of the control actions (i.e. the duty ratios of both the BB and SM subsystems) as a function of time is depicted in Fig. 11. The saturation of the duty ratio for the SM in the PC scheme can be clearly seen.

VI. Experimental Validation

This control strategy for both topologies has been implemented in a laboratory demonstrator of the HESS setup defined in Table I and Table III. Figure 12 shows the 2kW laboratory prototype. The same initial operating conditions have been applied.

In a first step, the merits and feasibility of the SPC configuration for the steady state operation has been validated for the conditions of the system under study. The main waveforms at switching frequency have been represented in Fig. 13 and Fig. 14, for both the PC scheme and the SPC configuration, respectively. In both cases, the DC bus voltage is kept constant and equal to 500V, while the current references for the BB and SM subsystems are, respectively, I_{BB_ref} = 5A, I_{SM_ref} = 10A. Figures 13 and 14 show the collector-to-emitter voltages of IGBT$_2$ (V_{CE_2}) and of IGBT$_4$ (V_{CE_4}), in order to clearly demonstrate the duty cycles of the BB and SM subsystems, respectively. From Fig. 13, it can be seen how the duty cycle for the SM branch in the conventional parallel scheme presents a very small value compared to the duty cycle of the BB converter. On the other hand, Fig. 14 shows how under the SPC configuration, the duty cycle of this SM branch has a value slightly larger than the duty cycle of BB, but, in any case, within the 20%-80% optimal range [41]. As mentioned in the previous sections, these waveforms yield to decrease the thermal and electrical stresses mismatch, thus improving

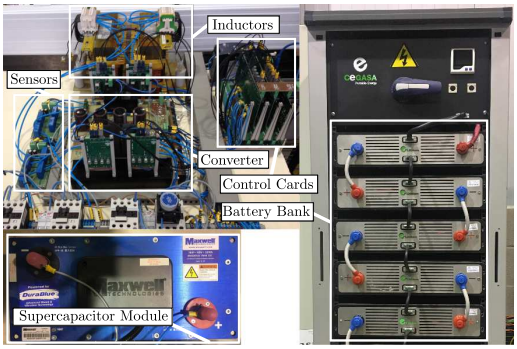

Fig. 12: Experimental setup that can be configured as PC or SPC.

the system reliability. But it also solves the voltage mismatch between the SM device and the DC bus, allowing an increase in the available margin for the evolution of the control action in the current control loop.

Once the steady state operation is experimentally validated, the behavior of the system upon load variations has also been verified in the prototype setup. Figure 15 shows the evolution of the system for the same +1kW and -1kW load step sequence that was applied through simulations in section V. Again, the DC bus was kept constant and equal to 500V, by means of an external controller. The main electric parameters have been recorded and analyzed, in order to verify the claims

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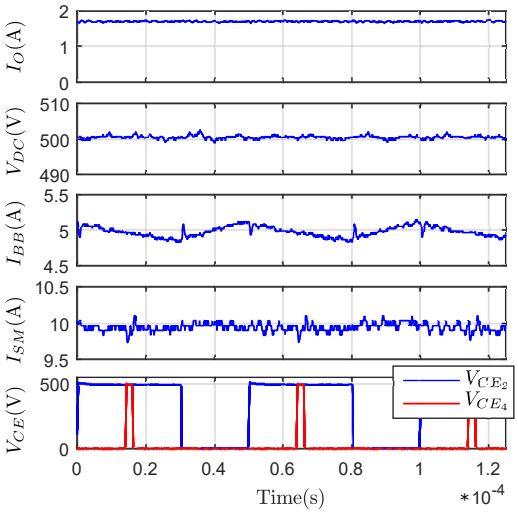

Fig. 13: Experimental results for the PC where 5 Amps BB current reference and 10 Amps SM current reference are applied and the DC bus is controlled by the grid inverter.

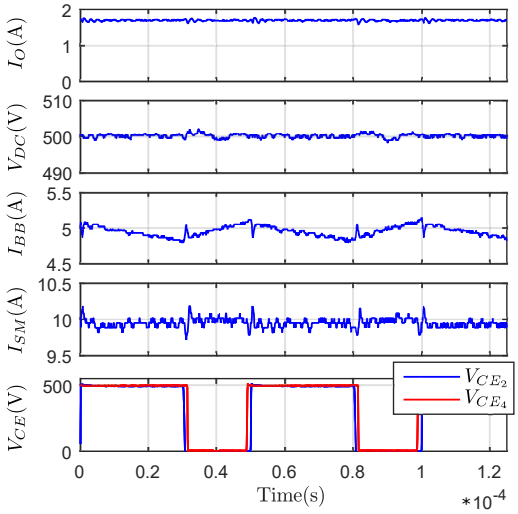

Fig. 14: Experimental results for the SPC where 5 Amps BB current reference and 10 Amps SM current reference are applied and the DC bus is controlled by the grid inverter.

of the research. As it can be seen, the experimental results match pretty well the simulations as well as the expected behavior. The voltage drop with the proposed control scheme for the SPC configuration is smaller than for the standard PC case as shown in Fig. 16. Therefore, the implemented control system has been experimentally validated for the system under consideration. It must be noticed how the proposed SPC configuration and control scheme does not imply any extra component than the base PC scheme, and therefore the enhancement in the performance is obtained at no cost.

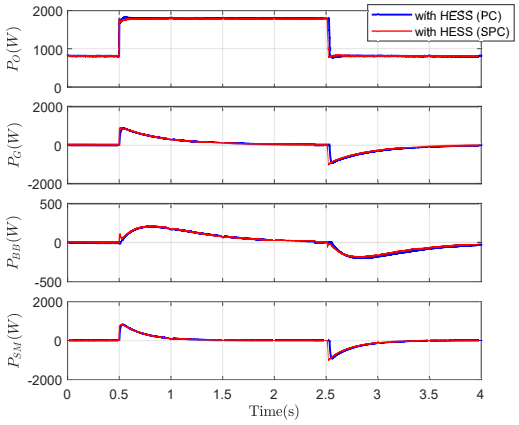

Fig. 15: Experimental results for the PC and the SPC where the load power is changed from 833.3 W to 1833.3 W at 0.5 seconds and then to 833.3 W again at 2.5 seconds.

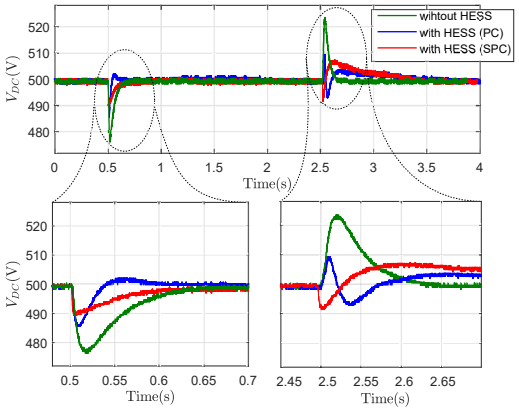

Fig. 16: Experimental results of the DC bus for the PC and the SPC where the load power is changed from 833.3 W to 1833.3 W at 0.5 seconds and then to 833.3 W again at 2.5 seconds.

VII. Conclusion and Future Developments

In this paper, a control loop design strategy for the implementation of the SPC of HESS in nanogrids is proposed, studied, simulated and experimentally validated. The design constraints have been established considering the ratings of an existing laboratory demonstrator. The performance of this strategy is compared to the original PC of the storage units proving that the dynamics of the SM aren't limited by the small voltage of the SM. The results show that the proposed

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control for the SPC scheme keeps the DC bus under control upon sudden load variations, with a non-isolated, transformerless simple solution. This solution decreases the thermal and electrical stress on the switches by balancing the voltage on the switches.

Therefore, the goal of the work has been accomplished satisfactorily. It has been demonstrated how the SPC configuration with the proposed control scheme is a suitable option for the implementation of HESS in nanogrid applications, when there is a large voltage mismatch in the ratings of one of the storage units and those of the DC bus. The performance of the SPC solution is better than the standard PC option, and this enhancement is obtained without any extra component.

Future developments include the optimization of the system for increasing the efficiency and power density, and even the extension of the analysis and validation in other kind of applications apart from HESS.

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C.2 Publication II

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A Comparison of Non-Isolated High-Gain Three-Port Converters for Hybrid Energy Storage Systems

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Abstract: This work carries out a comparison of non-isolated topologies for power electronic converters applied to Hybrid Energy Storage Systems. At the considered application, several options for three-port circuits are evaluated when interfacing a DC link with two distinct electrical energy storage units. This work demonstrates how the proposed structure, referred to as Series-Parallel Connection, performs as a simple, compact and reliable approach, based on a modification of the H-bridge configuration. The main advantage of this solution is that an effective large voltage gain at one of the ports is attained by means of a simple topology, preventing the use of multilevel or galvanic-isolated power stages. The resulting structure is thoroughly compared against the most significant direct alternatives. The analysis carried out on the switching and conduction losses in the power switches of the target solution states the design constraints at which this solution shows a performance improvement. The experimental validations carried out on a 10 kW prototype demonstrate the feasibility of the proposed scheme, stating its benefits as well as its main limitations. As a conclusion, the Series-Parallel Connection shows a better performance in terms of efficiency, reliability and controllability in the target application of compensating grid or load variations in Non-Isolated Hybrid Storage Systems, with large mismatch in the storage device voltage ratings.

Keywords: hybrid storage systems; power electronic converters; multiport; high gain converters; ultracapacitors

1. Introduction

At present, Hybrid Storage Systems (HSSs) are turning into one of the key technologies in power electronics related disciplines [1]. Indeed, by using these systems, there is a reported improvement in the performance at leading applications such as integration in the distribution network of stochastic power generators [2,3], grid stability and power quality support upon line contingencies [4], management of fast dynamics high power loads at the power-train in electric-hybrid vehicles [5,6], and a manifold of industrial applications with a load profile of large transient characteristics [7], among others. Generally speaking, these HSSs interface a fast-dynamics high-power storage device, e.g., a Ultracapacitor Module (UM), with a slower, bulk-energy storage unit, e.g., an Electrochemical Battery (EB) [8]. The design of the HSS involves the selection of adequate energy and power ratings in the elements of the system, as well as the design of a control scheme that manages properly the involved power flows [9]. The final design must ensure that the resulting HSS shows an overall enhanced performance, providing the energy ratings of the main energy storage device, but simultaneously maintaining the power ratings of the fast-dynamics one [1,10–12]. The management of the power flows in the system is generally implemented through Power Electronic Converters (PEC) that enable synchronized control and operation of the involved storage units [10–12].

Figure 1 depicts the power flow balance in a generic HSS. The primary energy source (in this case, it is the grid) supplies a given amount of power, P_{Grid}, to the front grid PEC (PECG). The aim of the system is to supply a power flow, P_{Load} towards another port that behaves either as a load or as a generator, for instance in the case of regenerative breaking applications. This port is interfaced through a Load/Generator PEC (PECL). At every instant, the difference between the load and grid power values, P_D, is managed by the control at the DC link. An adequate power balance into this DC link is essential for the correct operation of the system. A capacitor bank, DC link Cap in Figure 1, is usually employed as energy buffer for this difference power, being able to absorb or deliver the required P_{Cdc}. In some applications, for instance in islanded operation of microgrids, a very large energy storage capability is required at the DC link. The energy stored in the capacitor bank is normally not enough to ensure a stable operation at the DC link. Therefore, an extra energy storage system is interfaced to this DC link, ensuring also a fast recovery in case large power steps are demanded. Furthermore, in the case of hybrid systems, the total power of the HSS, P_{HSS}, is divided into two different storage units, ESS1 and ESS2, which are interfaced through two power converters, PEC ESS1 and PEC ESS2. The power through the EB and UM, P_{EB} and P_{UM}, respectively, is finally interfaced to the DC link.

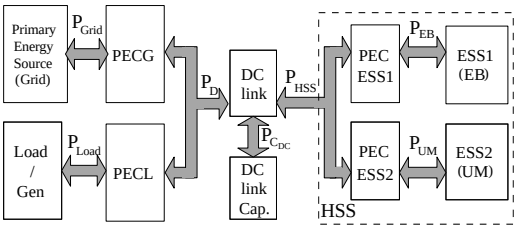

Figure 1. Scheme of the power flow balance in a general Hybrid Storage System (HSS).

To ensure a general case, all the power flows in the system must be considered as bidirectional. The conventional control scheme ensures that, upon normal conditions, i.e., power flowing from the grid to the load or from a generator back to the grid, the voltage at the DC link capacitor is kept constant. Then, in the event of sudden fluctuations at either load or line characteristics, the HSS control must compensate the resulting variation of operational parameters to ensure an adequate behavior of the system.

The simplest scheme for a three-port bidirectional converter interface in a HSS, able to attach these devices to a controlled DC link is the Direct Parallel Connection (DPC), can be seen in Figure 2a [13,14]. This scheme is formed by two independent bidirectional boost converters, each of them implemented by adding a filter inductor to a leg of a H-bridge converter. For the sake of clarity, a nominal DC link voltage of 600 V is defined in the coming discussion. In the same manner, the operating voltage ratings for the EB is considered to be in the range of 300–400 V (e.g., a Li-Ion EB intended for grid supporting applications). For these voltage ratios, a bidirectional boost converter can be selected as a feasible solution for interfacing both ports. Nevertheless, considering an extra storage unit with significant lower voltage ratings that requires to be interfaced, the voltage ratios between the DC link voltage and the storage unit voltage will change correspondingly. For instance, in the case of a UM as storage device of, e.g., 48 V voltage rating, and considering a steady-state reference value of 30 V, the direct interface through a boost topology would yield to the operation of the converter at duty ratios around 5%, well beyond the optimal 20–80% range [15]. On top of major concerns in the effect of parasitic elements, these extreme values for the duty ratio of the converter imply significantly high form factors in the voltage and current switch waveforms at the UM converter leg. In addition, it implies constraints in the practical control margins used in the regulation of the converter. All these issues, which are covered extensively in Section 2, make mandatory a search for simple, high-gain alternatives to interface low voltage ratings storage devices with the DC link [16–18].

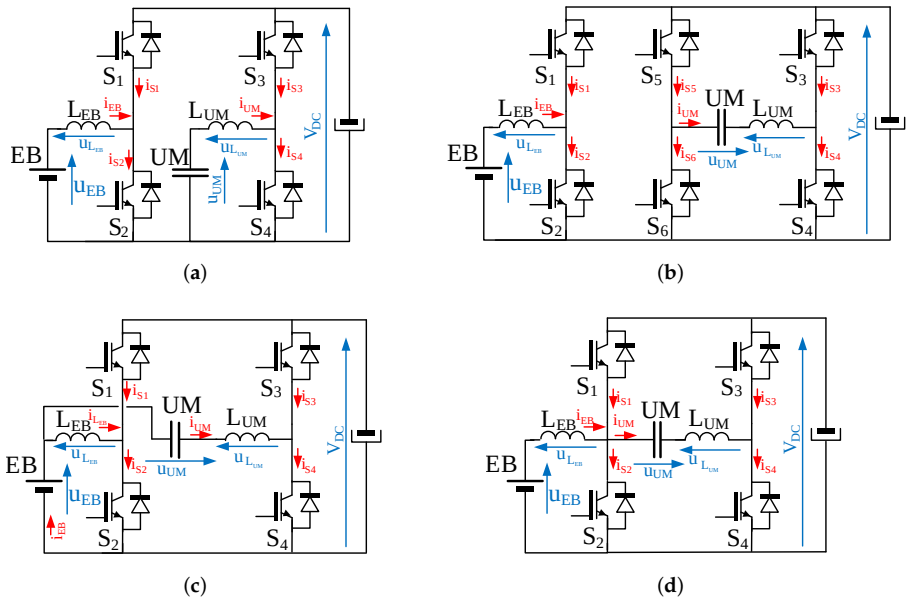

Figure 2. Non-isolated topologies considered for the HSS: (**a**) Direct Parallel Connection (DPC); (**b**) Full-Bridge Connection (FBC); (**c**) Series Connection (SC); and (**d**) Series-Parallel Connection (SPC).

The most used alternatives in high power applications include complex cascaded schemes (multistage solutions and tapped-inductor topologies), multilevel converters, or galvanically-isolated converters [19–25]. However, for small power levels, these solutions are not cost-competitive depending on the application. To solve these issues, the most straightforward solution in non-isolated converters is to use a Full Bridge Converter (FBC), as depicted in Figure 2b, for the UM storage system. As is justified in Section 3, this solution implies higher sizes and costs, as well as increased power losses. After that, Section 4 explores the non-isolated interfacing scheme proposed in [16], and depicted in Figure 2c, based on a Series Connection (SC) of the storage devices. After studying this scheme in detail, its advantages and drawbacks are highlighted. The most important drawback of this proposal is the series connection of both storage systems that eventually makes impossible an independent current control of both storage subsystems. This aspect will be discussed in Section 4. To overcome the mentioned drawbacks, an alternate solution is finally proposed for high voltage gain applications. The performance of the proposed Series-Parallel Connection (SPC) has been preliminarily explored on isolated applications [26]. However, this paper is focused on applying the SPC to the non-isolated scheme, as depicted in Figure 2d, and provides a deeper study than the one carried out in [27]. Therefore, this work aims to critically assess the performance of the SPC as a non-isolated alternative for HSS applications. This assessment is carried out through a detailed theoretical analysis, which is then validated by means of experimental performance demonstrations on a 10 kW rated laboratory setup. Section 5 covers the definition and detailed discussion of the switching modes in the converter, whereas Section 6 provides an analysis of the steady state operation of the topology. Section 7 evaluates the losses performance of the converter, and compares it to the DPC topology. From the conclusions derived of this study, Section 8 discusses the operation and suitability of this topology for HSS. A discussion on the control loop implemented for the validation is carried out in Section 9. Finally, Section 10 presents the final conclusions on the comparison carried out, and proposes some future work related with this topic.

2. Limitations of the Direct Parallel Connection

As mentioned, the DPC scheme in Figure 2a is suitable for the interconnection of DC sources when the voltage ratings at the storage systems are in the order of magnitude of half the DC link value. However, when a significantly small voltage ratings storage device is interfaced with a large DC link, i.e., with a ratio of 1:10 or higher, the bidirectional boost configuration is not the optimal option. As a large gain is required, the efficiency and the cost-effectiveness of the design are compromised [27,28]. Such a high gain requires a large duty ratio at the lower switch, over 90%. On the other hand, and considering a complementary pulses scheme, the remaining upper switch must be turned on with a very small duty ratio. These extreme duty ratio values yield to low efficiency [29]. As the switches must be designed for the high DC link voltage, high voltage ratings must be used. However, these devices present relatively large on-resistance values, and therefore conduction losses increase [30]. Moreover, in IGBT based topologies, this implies large currents at the antiparallel diodes, yielding to operation drawbacks derived from the reverse recovery phenomenon [31]. Moreover, the high duty cycles limit the switching frequency, as the minimum off-time of the switch must be ensured [32].

Finally, the dynamic performance of the converter is also affected, since the small duty ratios yield to non-symmetric bandwidths limitation in charge and discharge operation [27]. This last issue will be evidenced by considering an example of a HSS with the operating parameters of Table 2. In this case study, a 600 V DC link voltage is assumed, with a nominal operation voltages for the EB and the UM of 300 V and 30 V, respectively. All through this work, a particular notation will be used to clarify the discussion. Note that the subscript applied to the parameters for each of the studied topologies include a capital letter to distinguish the different configurations under consideration. In agreement with Figure 2, the magnitudes related to the DPC have a capital letter A in the subscript. In the same manner, the subscripts in the FBC include capital letter B. Letter C is used for subscripts in the SC, whereas subscripts for the SPC include capital letter D. For instance, the parameter D_1 (i.e., the duty ratio of Switch S_1) is represented as D_{1_A} for the DPC (Figure 2a), but is notated by D_{1_B} for the FBC (Figure 2b), and so on.

Initially, the steady state behavior is discussed. Upon these conditions, the corresponding duty ratios for the EB and UM legs are given by:

$$D_{1_A} = \frac{u_{EB}}{V_{DC}} = 50\% \tag{1}$$

$$D_{3_A} = \frac{u_{UM}}{V_{DC}} = 5\% \tag{2}$$

where D_{1_A} and D_{3_A} are the duty ratios of switches S_1 and S_3, respectively, for the DPC configuration. These relationships come directly from the gains of each leg of the bidirectional topology, which can be defined as:

$$M_{EB_A} = \frac{u_{EB}}{V_{DC}} \tag{3}$$

$$M_{UM_A} = \frac{u_{UM}}{V_{DC}} \tag{4}$$

where M_{EB_A} and M_{UM_A} are the static gain of the EB and the UM voltages to the DC link voltage, respectively, for the DPC configuration. In this case, the final capital letter A in the subscript indicates the DPC scheme.

Therefore, it is obvious to see that:

$$D_{1_A} = M_{EB_A} \tag{5}$$

$$D_{3_A} = M_{UM_A} \tag{6}$$

However, these expressions are a function of the topology, and will change for the rest of the topologies considered, as shown in the coming analysis.

2.1. Effects of the Waveform Shape in the Thermal Efforts

The final reliability of the design is a function of the relative value and distribution scheme of the thermal efforts associated to the electrical parameters [33]. The following paragraph discusses the effect of the shape of the waveforms in the distribution of the electrical stresses of a leg at the converter. Assuming small current ripples, then the form factor (K_f) of the current waveform for a given switch in the converter follows the general expression for a square waveform:

$$K_f = \frac{I_{rms}}{I_{avg}} \tag{7}$$

$$I_{rms} = I_{pk}\sqrt{\frac{T_{up}}{T_s}} \tag{8}$$

$$I_{avg} = I_{pk}\frac{T_{up}}{T_s} \tag{9}$$

$$K_f = \frac{1}{\sqrt{\frac{T_{up}}{T_s}}} \tag{10}$$

where I_{rms}, I_{avg} and I_{pk} are the rms, average and peak currents of a periodic square waveform of period T_s, respectively, being T_{up} the interval of the waveform that the current value equals I_{pk}.

In the DPC topology, for large mismatch between the ratings at the UM and at the DC link, the duty ratio at the UM leg (D_{3_A}) is close to 0%, around 5% in the case under study. This duty ratio at the upper leg can be expressed as:

$$D_{3_A} = \frac{T_{up}}{T_s} \tag{11}$$

and therefore:

$$K_{f_{3_A}} = \frac{1}{\sqrt{D_{3_A}}} \tag{12}$$

Analogously for the lower switch:

$$K_{f_{4_A}} = \frac{1}{\sqrt{1 - D_{4_A}}} \tag{13}$$

Therefore, for a duty ratio close to 5%:

$$K_{f_{3_A}} = 4.47 \tag{14}$$

$$K_{f_{4_A}} = 1.02 \tag{15}$$

This difference between the form factors at the switches of the leg of the UM converter implies that the thermal efforts at both switches are very different. Ideally, to evenly distribute these thermal efforts among the upper and lower switches of a leg, the duty ratios should be around 50%, yielding to K_f values close to:

$$K_{f_3} = K_{f_4} = 1.41 \tag{16}$$

2.2. Prototype and Experimental Setup

An experimental setup of the PC converter has been implemented in an existing laboratory prototype of 10 kW (Table 1). The prototype can be configured in all the configurations discussed in this work (Figure 3). The setup is built using a ROOK 48 × 6 module lithium-ion battery from CEGASA Portable Energy, a BMOD0165 P048 C01 Ultracapacitor Module from Maxwell Technologies and 2MB1200HH-120-50 IGBT modules from Fuji Electric, switching at a frequency of 20 kHz. The setup uses a TMS320F28335 from TI as control platform. The design uses standard reactive elements.

Table 1. Parameters of the 10 kW prototype.

Symbol	Parameter	Value
u_{EB}	Nominal Battery Voltage	288 V
u_{EB_min}	Minimum Battery Voltage (0% SOC)	225 V
u_{EB_max}	Maximum Battery Voltage (100% SOC)	328 V
i_{EB}	Battery Current	±30 A
u_{UM}	Rated UM Voltage	48 V
i_{UM}	UM Current	±200 A
C_{UM}	UM Capacitance	165 F

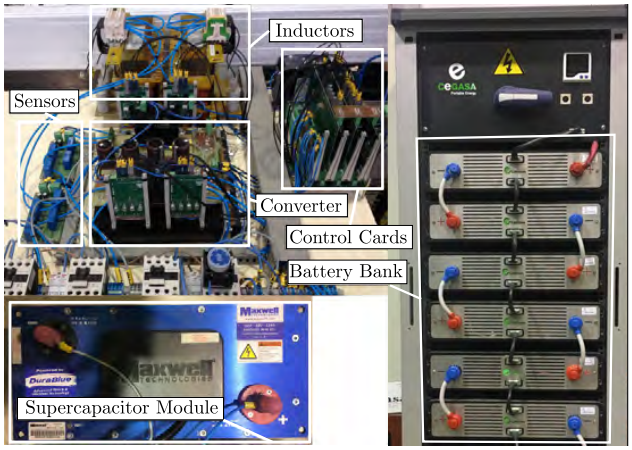

Figure 3. Experimental setup that can be configured as Parallel Connection (PC), Full Bridge Converter (FBC), Series Connection (SC) or Series-Parallel Connection (SPC).

For the conditions of the above description for the DPC scheme, with such a small D_{3_A}, the waveforms of the current through both switches S_3 and S_4 in Figure 2a present average values and K_f that are significantly different. This issue implies a high mismatch, both in the electrical and in the thermal stresses at each switch.

Figure 4a shows these waveforms at the switches, for the setup operating with the parameters in Table 2. As can be seen, the main currents and voltages measurements, consistent with the references in Figure 2a, are represented. It can be appreciated how the duty ratio of the switches reach extreme values. This yields to the aforementioned operational and design limitations, that eventually prevent the use of this topology.

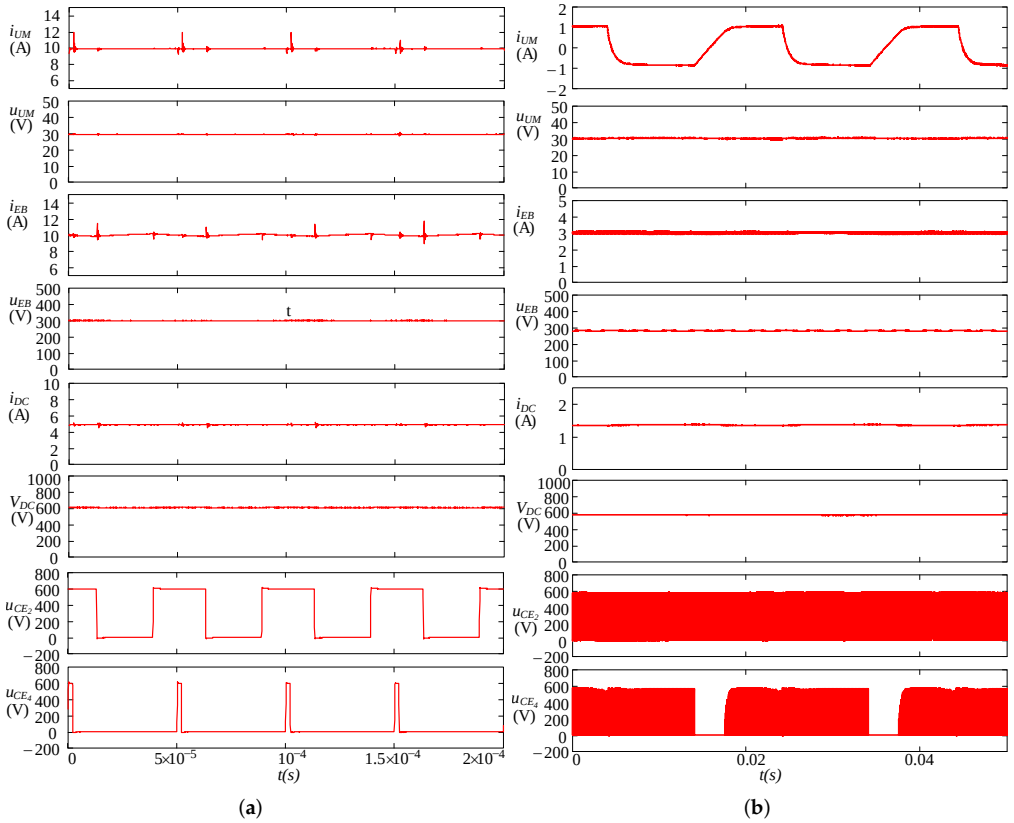

Figure 4. Experimental waveforms of the DPC scheme. Steady states: (**a**) i_{EB} = 10 A, i_{UM} = 10 A; and (**b**) i_{EB} = 10 A, i_{UM} steps from 1 A to −1 A.

Table 2. Operating parameters of the system under study.

Symbol	Parameter	Value
V_{DC}^*	DC link Voltage	600 V
R_{LOAD}	DC load resistor	300 Ω
u_{EB}	Battery Voltage	300 V
i_{EB}^*	Battery Current	10 A
u_{UM}	UM Voltage	30 V
i_{UM}^*	UM Current	10 A
f_s	Switching Frequency	20 kHz

As mentioned, the dynamic performance is also significantly affected by the extreme duty ratio values in the UM branch, which are very close to the 0–100% physical limits. Considering an abrupt negative step in the UM current demand, i_{UM}*, then the control stage must generate a control action in the duty ratios that provide the actual UM current, i_{UM}, equal to the reference value. However, the available control actions range from D_{3_A} = 5% to D_{3_A} = 0%, which ultimately implies S_3 and S_4 continuously turned off and on, respectively. This condition implies that the UM inductance, L_{UM}, is discharged with the relatively small voltage at the UM, u_{UM}, thus implying a limitation in the rate of decrease of the UM current. This aspect penalizes the discharging dynamics enormously, also introducing a non-symmetric behavior in the system performance. Indeed, for the opposite case

(charging current), the extreme operation in the control action would imply a charging voltage of V_{DC}, and the rate of charge results dramatically increased.

This situation is illustrated in Figure 4b, where a series of alternate steps in the UM current reference, from 1 A to −1 A and vice-versa, are provided to the system. Even though these current values are several orders of magnitude smaller than the expected operational range, it can be seen how, at the beginning of the charging step (i.e., current i_{UM} changing from −1 A to 1 A), the modulation temporarily stops, as D_{3_A} results clamped to 0%. Therefore, the demanded control action would drop to negative values, yielding to an impossible operating constraint. On the other hand, for the discharging step (−1 A to 1 A), the control action can be provided by the system without constraints. Thus, the non-symmetrical performance of the system is demonstrated. Notice that this effect would take place even if the switches are considered ideal.

3. The Full Bridge Converter

To solve these issues, the most straightforward solution among non-isolated topologies is to use a FBC, as depicted in Figure 2b. During the following discussion, the inductors at the converter are considered ideal and purely inductive, therefore neglecting any parasitic resistances. This simplification is generally accurate for a reasonably good design of the magnetic devices. For the references at this figure, and considering an ideal inductor, the static gain of the UM leg of the converter can be defined as:

$$M_{UM_B} = \frac{u_{UM}}{V_{DC}} = \frac{D_{3_B} \cdot V_{DC} - D_{5_B} \cdot V_{DC}}{V_{DC}} = D_{3_B} - D_{5_B} \tag{17}$$

where D_{3_B} and D_{5_B} are the duty ratios of switches S_3 and S_5, respectively, for the FBC solution.

As can be seen, the effective gain between the UM and the DC link is the difference between the duty ratios of both legs of the H bridge converter. The value of the duty ratio of the UM branch can be calculated then as:

$$D_{3_B} = D_{5_B} + \frac{u_{UM}}{V_{DC}} = D_{5_B} + M_{UM_B} \tag{18}$$

It is assumed that the duty ratios of S_3 and S_5 are complementary to the ones at S_4 and S_6, respectively, as in the following scheme:

$$D_{4_B} = 1 - D_{3_B} \tag{19}$$

$$D_{6_B} = 1 - D_{5_B} \tag{20}$$

In this case, the effective static gain of the UM leg, M_{UM_B}, is a subtraction of both converter legs duty ratio levels. In other words, the voltage constraints impose the difference in the values of D_{3_B} and D_{5_B}, but the value itself can be selected arbitrarily. This implies that these duty ratios can reach more adequate values than in the boost converter case, while the difference can be made very small to achieve a large resulting gain. In fact, this effect comes as there is a new degree of freedom that can be selected to have one of the duty ratios, e.g., D_{5_B}, fixed and equal to 50%. This ensures effective duty ratios at each leg out away from the extreme values, i.e., within the 20–80% areas, therefore achieving better general performance [27,28,30–32]. In addition, the dynamic range is greater, given that the asymmetric modulation constraint of the DPC solution is not present any more. The payback in this case is the use of two additional switches in a second leg. This issue increases the size and weight of the converter, as well as the switching and conduction losses. However, with this solution the dynamics are not limited to the low duty ratios in the converter [27]. However, all four switches need to cope with the large voltages at the DC-link, V_{DC}, even though the device to interface presents significantly small ratings, yielding again to large conduction and switching losses [30,31]. A set of experiments has been carried out, configuring the same converter used in Figure 4 as a FBC. The system operates at a DC link

voltage of 600 V, a UM voltage of 30 V, and different current values combinations flowing through both the EB and the UM. Table 3 shows experimental values of the losses and efficiency measurements of both DPC and FBC configurations, for the aforementioned voltage and current conditions, considering an extended set of UM current values (it must be noticed that the asterisks at any variable represent the references for the control systems). As can be seen, compared to the DPC operation, the FBC losses result increased, and therefore the efficiency of the FBC configuration is significantly smaller.

Table 3. Experimental losses and efficiency performance of DPC and FBC configurations.

i^*_{EB} (A)	i^*_{UM} (A)	$P_{Loss}(DPC)$ (W)	$P_{Loss}(FBC)$ (W)	η_{DPC} (%)	η_{FBC} (%)
10	10	308.6	434.3	90.6%	86.6%
10	5	251.8	339.4	92.0%	89.3%
10	0	222.7	250.4	92.6%	91.8%
10	−5	247.5	310.8	91.7%	89.4%
10	−10	286.4	374.7	90.4%	86.7%

4. Series Connection of the Storage Systems

Figure 2c shows the series configuration of the storage systems [10]. It must be noticed how the UM is connected in series to the EB. The analysis of the topology starts by looking at the mesh equation that relates the voltages at the switches S_2 and S_4, at both inductors and at the UM, with the references in Figure 2c:

$$u_{CE_2}(t) + u_{UM}(t) + u_{L_{EB}}(t) - u_{L_{UM}}(t) = u_{CE_4}(t) \tag{21}$$

where $u_{CE_2}(t)$ and $u_{CE_4}(t)$ are the collector to emitter voltages of switches S_2 and S_4, respectively, and $u_{L_{EB}}(t)$ and $u_{L_{UM}}(t)$ are the voltages at the inductors L_{EB} and L_{UM}, in the EB and UM legs, respectively. The average inductor voltages will be null at steady state, and thus Equation (21) can be expressed as:

$$u_{CE_2} + u_{UM} = u_{CE_4} \tag{22}$$

Given that each leg of the H-bridge operates as a bidirectional boost converter, the average values of $u_{CE_2}(t)$ and $u_{CE_4}(t)$ are again a function of the duty ratios at the upper switches of the H-bridge converter, D_{1_C}, for S_1 at the EB leg, and D_{3_C}, for S_3 at the UM leg, respectively. The expressions for the static gain in SC is analog to the ones derived in Equations (3) and (4), for FBC, but for consistency, they are expressed for this topology as:

$$M_{EB_C} = \frac{u_{EB}}{V_{DC}} \tag{23}$$

$$M_{UM_C} = \frac{u_{UM}}{V_{DC}} \tag{24}$$

Equations (23) and (24) yield to the expression for the duty ratios, D_{1_C} and D_{3_C}, and the static gains, M_{UM_C} and M_{EB_C}, in steady state:

$$D_{1_C} = \frac{u_{EB}}{V_{DC}} = M_{EB_C} \tag{25}$$

$$D_{3_C} = \frac{u_{UM} + u_{EB}}{V_{DC}} = M_{UM_C} + M_{EB_C} \tag{26}$$

From Equations (25) and (26), the expression that relates the duty ratio from both legs can be calculated as:

$$D_{3_C} = D_{1_C} + \frac{u_{UM}}{V_{DC}} = \frac{u_{UM} + u_{EB}}{V_{DC}} \tag{27}$$

Equation (27) is interesting, since the duty ratio of switch S_3 at the UM leg, i.e., D_{3_C}, is not a function of the UM and DC voltage values alone (which would yield to very small duty ratio values as in the DPC), but also a function of the battery voltage. This is has a similar effect to what was found for the FBC scheme. From Equation (27), for the operating conditions in Table 2, the duty ratio values at the UM leg of the converter for the DPC change from D_{3_A} = 5% for the DPC to D_{3_C} = 55% in the SC. Therefore, again, the resulting duty ratios at the SC scheme imply a significant improvement in the current stresses balancing versus the DPC case. In addition, the control margins for the control actions achievable in this topology result increased, and in principle this would allow for a symmetrical fast dynamics performance design, in line with the FBC case. The only constraint in the design for SPC scheme is that the voltage at the battery as well as the voltage at the UM cannot reach the DC link voltage. This means the duty ratio of the switch S_3 at the UM leg must be less than or equal 100% ($D_{3_C} \leq 100\%$). However, for practical values, a feasible system ensuring this condition can be designed without major issues.

However, the most significant drawback in this scheme comes from the expression of the battery current, which can be expressed by:

$$i_{EB} = i_{L_{EB}} + i_{UM} \tag{28}$$

where i_{EB}, $i_{L_{EB}}$ and i_{UM} are the currents of the EB, inductor L_{EB} and UM, respectively.

This results in the impossibility of implementing a practical decoupled current control scheme in both storage systems (EB and UM). In fact, if both inductor currents are independently controlled, then the evolution of the battery inductor current is forced by Equation (28), yielding either to dangerous voltages in the system due the inductive behaviour, or to a limited dynamic performance if these overvoltages are prevented at control level.

Another point of the analysis comes by looking in Figure 2c. From the inductors connection scheme, it might seem that a certain beneficial interleaving effect is possible in the EB current, i_{EB}. Nevertheless, this effect would only be true for small operating conditions ranges, as it depends on the values of the duty ratios and in the synchronization of the pulses in the switches. This enhanced interleaving effect will not occur for all possible conditions, particularly for UM currents much higher than EB currents.

Finally, also derived from Equation (28), the peak current flowing through the EB inductor is calculated as a function of the UM and EB currents. Thus, inductor L_{EB} must be designed considering values in the order of magnitude of the UM current, that is, significantly larger than the EB current. This results in a much larger inductor device, which compromises the efficiency, the power density and the cost of the full HSS.

Given all these constraints, the SC scheme is disregarded as a feasible option. Therefore, it will not be included for the validation stages, by simulations or experimental tests.

5. Analysis of the Series-Parallel Connection

All these drawbacks of the SC scheme can be effectively solved by considering the SPC of both storage units. This scheme, shown in Figure 2d, keeps the H-bridge configuration of the switches. However, in this case, the series assembly formed by the EB and inductor L_{EB}, is connected between both midpoints of the legs. This configuration can be seen as an integration of the FBC from three to two legs, removing the degree of freedom that existed in the latter. For the references in Figure 2d, the mesh equation that includes the voltage at the UM can be expressed as:

$$u_{CE_2}(t) + u_{UM}(t) - u_{L_{UM}}(t) = u_{CE_4}(t) \tag{29}$$

Analyzing Equation (29) analogously to the former FBC and SC cases, the expression for the duty ratio at the UM leg, results in:

$$D_{3_D} = M_{UM_D} + M_{EB_D} = \frac{u_{UM} + u_{EB}}{V_{DC}} = D_{1_D} + \frac{u_{UM}}{V_{DC}} \tag{30}$$

Again, it presents a similar expression to the SC case; thus, all statements concluded for the new duty ratio values are still valid.

Regarding the stresses distribution, the values of the K_f can be calculated for the switches at the SM branch at the SPC configuration, considering the values of Table 2:

$$K_{f_{3D}} = \frac{1}{\sqrt{0.55}} = 1.35 \tag{31}$$

$$K_{f_{4D}} = \frac{1}{\sqrt{0.45}} = 1.49 \tag{32}$$

These values are close to the optimal value for an even distribution of the current efforts stated in Equation (16), therefore increasing the reliability of the system. This effect is obtained for any application in which one of the legs at the converter interfaces a device with voltage ratings significantly smaller than the other one, this latter being around half (e.g., practical values of 40–60%) the DC link value.

However, in addition to that, it must be noticed how, in the SPC scheme, the following expression can be calculated for the EM current:

$$i_{EB} = i_{L_{EB}} \tag{33}$$

Therefore, and unlike in the SC case, decoupling both EB and UM current control is quite simple in the SPC scheme. This results in the possibility of implementing an independent current control (and hence power flow) for both storage devices. This allows for an effective hybridization of the energy devices, without the drawbacks of extreme duty rations in the system.

The following discussion deals with a deep analysis of the operation of the SPC converter, aiming to provide the foundations for an adequate design of the HSS. The previous step of the analysis is to settle the assumptions and limitations that are going to be considered to simplify and establish the limits of the study. These assumptions are the following:

- The UM is a unipolar DC device, and the terminal of negative polarity is attached to the center point of the battery leg. Thus, it can be deduced from (30) that D_{3_D} is greater than D_{1_D} in steady state.
- The switching pulses of all the switches are synchronized at the same frequency, f_S.
- The ripple values of the current through both inductors and of the voltage at the capacitor, are relatively smaller than the respective average values.
- Each leg at the converter operates in a complementary scheme, i.e., the pulse signals for the lower switches are the logical inverted pulses of the upper ones. It is also assumed that a dead time is implemented in the switching scheme, aiming to avoid cross-conduction, and that its effect in the overall performance can be neglected.
- The initial conditions assume a positive value for i_{EB}, i.e., the battery is being discharged towards the DC link.
- Finally, it is also considered a positive value for i_{UM}, i.e., the UM is also being discharged. However, to increase the generality of the analysis, in a later stage, the case of negative i_{UM} will also be considered.

Once the basic operating assumptions are settled, the instant waveforms at the converter must be analyzed. However, the shapes of these waveforms depend on the exact sequence of gating signals in the switches. Each leg operates in complementary mode, as stated previously; however, in the most general case, the phase shift between legs might take any value, resulting in different synchronization schemes. From the point of view of the implementation of the PWM scheme in a digital controller, the most straightforward manner to synchronize the pulses is to use a single triangular waveform at f_S, and compare this triangular shape with given reference values to generate the control pulses for every switch in the converter. For this single triangular waveform scheme, the pulses obtained are symmetrical from the central point of the on/off intervals, as depicted in Figure 5. In particular,

Figure 5a corresponds to the switching pattern in the steady state, i.e., for D_{3_D} being greater than D_{1_D}. This gives rise to a set of operating modes, as a function of the combination of on/off states of the switches in the converter. These equivalent switching modes are detailed in the following subsections, considering the chronograms in Figure 5.

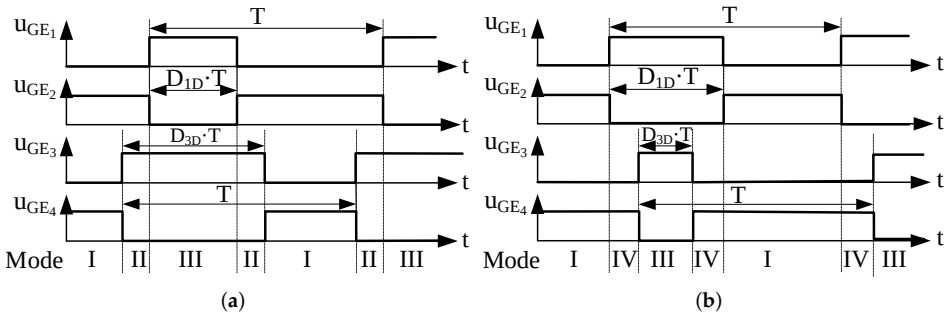

Figure 5. Switching modes in the SPC for the pulse scheme considered: (**a**) D_{3_D} is greater than D_{1_D}; and (**b**) D_{3_D} is smaller than D_{1_D} (only in transients).

5.1. Mode I. S_2 and S_4 Turned On

Figure 6a shows both S_2 and S_4 turned on. The battery inductor charges through S_2 ($i_{EB} > 0$). Assuming also $i_{UM} > 0$, then L_{UM} charges through S_2 and S_4:

$$\begin{array}{ll} i_{S1}(Mode\ I) = 0; & i_{S3}(Mode\ I) = 0; \\ i_{S2}(Mode\ I) = i_{EB} - i_{UM}; & i_{S4}(Mode\ I) = i_{UM}; \end{array} \tag{34}$$

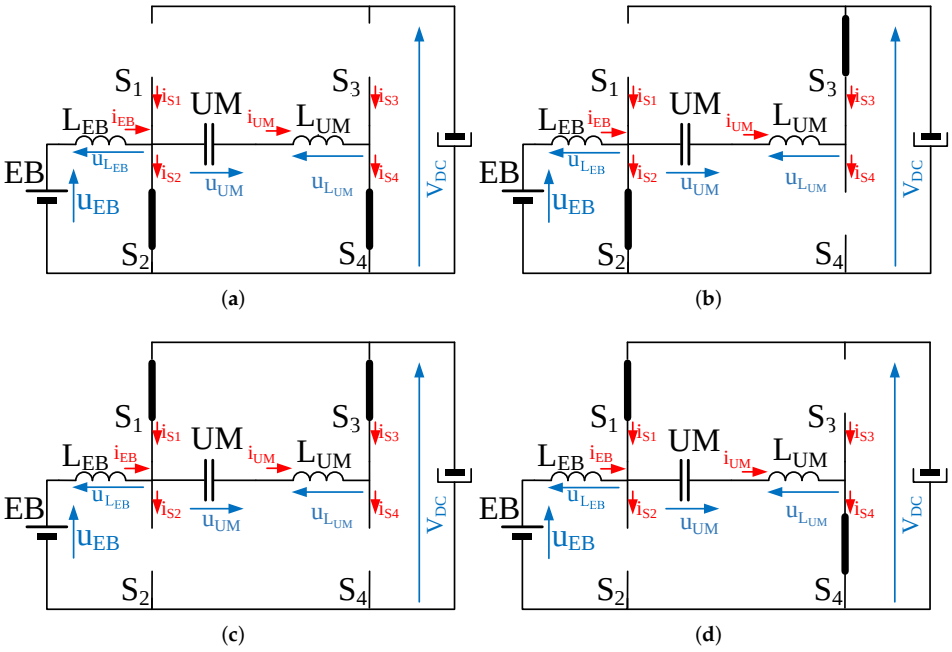

Figure 6. Switching modes in the SPC scheme: (**a**) Mode I; (**b**) Mode II; (**c**) Mode III; and (**d**) Mode IV.

5.2. Mode II. S_2 and S_3 Turned On

In the next switching interval, depicted in Figure 6b, S_4 turns off and S_3 turns on, whereas the battery leg remains unchanged. The UM current flows towards the DC link through S_3, and therefore:

$$\begin{array}{cc} i_{S1}(Mode\ II) = 0; & i_{S3}(Mode\ II) = -i_{UM}; \\ i_{S2}(Mode\ II) = i_{EB} - i_{UM}; & i_{S4}(Mode\ II) = 0; \end{array} \tag{35}$$

5.3. Mode III. S_1 and S_3 Turned On

Finally, mode III keeps the UM leg as in Mode II, but now S_1 is turned on as S_2 turns off (Figure 6c). The resulting current expressions in the switches for this interval are:

$$\begin{array}{cc} i_{S1}(Mode\ III) = -i_{EB} + i_{UM}; & i_{S3}(Mode\ III) = -i_{UM}; \\ i_{S2}(Mode\ III) = 0; & i_{S4}(Mode\ III) = 0; \end{array} \tag{36}$$

5.4. Mode IV. S_1 and S_4 Turned On

An additional switching mode has to be analyzed. During transients, D_{3_D} might get smaller than D_{1_D}, and therefore Mode IV would take place instead of Mode II (see Figure 6b) in the switching sequence. In this case, S_1 and S_4 will be turned on, whereas S_2 and S_3 will remain turned off (Figure 6d):

$$\begin{array}{cc} i_{S1}(Mode\ IV) = -i_{EB} + i_{UM}; & i_{S3}(Mode\ IV) = 0; \\ i_{S2}(Mode\ IV) = 0; & i_{S4}(Mode\ IV) = i_{UM}; \end{array} \tag{37}$$

6. SPC Steady State Analysis

Once the switching states are defined, the steady state analysis of the SPC scheme can be carried out. It must be noticed that both converters are bidirectional in current, and thus, if a general analysis is desired, all possible combinations must be assessed. Considering a system that operates with DC link voltage control, and provided that both storage device legs are controlled in current mode, the operating conditions that need to be taken into account are stated in Table 4.

Table 4. Operating conditions of storage systems, considering references in Figure 6.

EB	UM	Operating Condition
Discharging $i_{EB} > 0$	Charging $i_{UM} < 0$	Opposite sign in currents
Discharging $i_{EB} > 0$	Discharging $i_{UM} > 0$	Same sign in currents
Charging $i_{EB} < 0$	Charging $i_{UM} < 0$	Same sign in currents
Charging $i_{EB} < 0$	Discharging $i_{UM} > 0$	Opposite sign in currents

From Equations (34)–(37), the current that flows through the switches at the battery leg are a subtraction of the EB and UM inductor currents. Therefore, the net result of these switch currents depends on whether these currents are added or subtracted in absolute value. Thus, this study can be simplified to the cases in which UM and EB currents have either the same or opposite signs. The theoretical waveforms for these two key cases can be seen in Figure 7a (EB and UM discharging, i_{EB} and i_{UM} have same signs) and Figure 7b (EB discharging, UM charging, i_{EB} and i_{UM} present opposite signs). Even if the resulting current values at the switches result in significant change, the claimed balancing effect in the current stresses at the UM leg switches can still be noticed, as all the involved duty ratios are relatively close to the 50% optimal value.

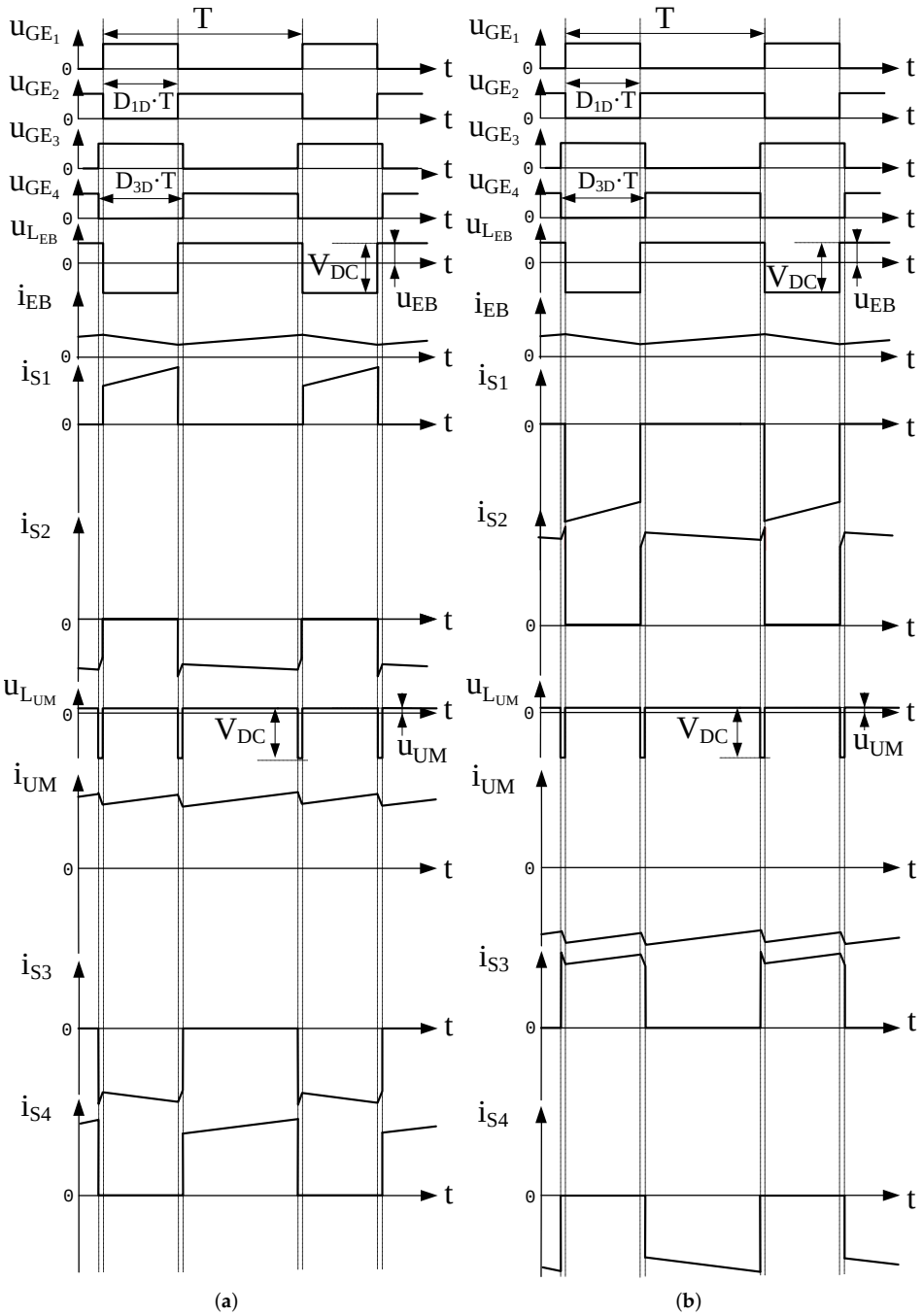

Figure 7. Theoretical waveforms of the SPC scheme: (**a**) EB and UM both are in discharge mode; and (**b**) EB is in discharge mode but UM is in charge mode.

Another consequence of this switching pattern is that the current waveforms through the UM inductor evolves at twice the switching frequency. This allows for a certain degree of optimization in the inductor design, as current ripple will decrease for the same target inductor value, or, conversely,

inductor can be made smaller for the same target current ripple. Figure 8a shows key experimental waveforms measured at steady state, for the SPC configuration of the prototype setup defined in Table 2.

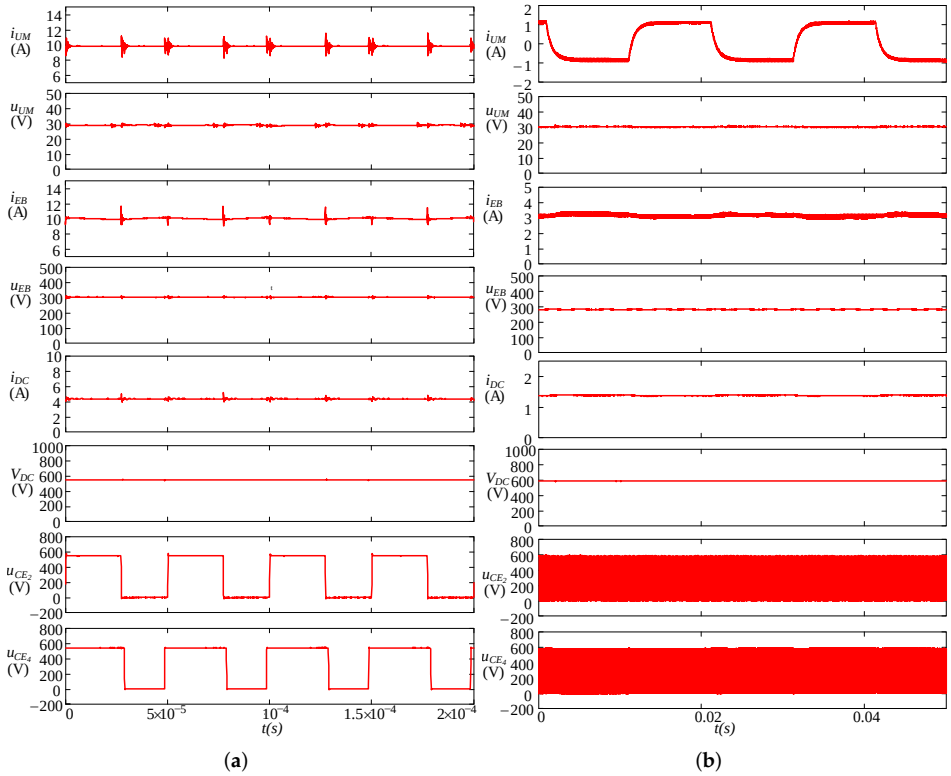

Figure 8. Experimental waveforms of the SPC scheme. Steady states: (**a**) i_{EB} = 10 A, i_{UM} = 10 A; and (**b**) i_{EB} = 3 A, i_{UM} steps from 1 A to −1 A.

However, the most significant consequence of this connection comes from the relationship between M_{EB_D} and M_{UM_D}, and therefore between D_{1_D} and D_{3_D}. As stated in the assumptions, and considering the steady state operation, then from Equation (30), D_{3_D} is always greater than D_{1_D}. However, in transient operation, the inductor voltage at the UM might be substantially large, depending on the transient current demanded. This might yield D_{3_D} to reach values smaller than D_{1_D}. However, as in the FBC case, now the control action at the UM is not clamped as in DPC, and therefore a better dynamic performance is found. Moreover, this behavior is now symmetric. To illustrate this last assertion, Figure 8b shows a series of symmetric ±1 A consecutive bidirectional current steps for the SPC connection, in order to keep the same values as in the DPC case (Figure 4b), as to be compared directly. As it can be seen, and given that the control action is able to reach negative values in a natural manner, the modulation is never interrupted in the SPC operation. Figure 9 shows the performance for an increased current steps than in Figure 8b, up to ±10 A current steps. As it can be seen in this figure, a large ripple an be appreciated in the DC link voltage. This is due the fact that for these experiments, the DC link is not regulated with optimal bandwidth. However, the aim of these plots is to show how this topology can supply large, fast current steps to the DC link voltage by the UM storage subsystem.

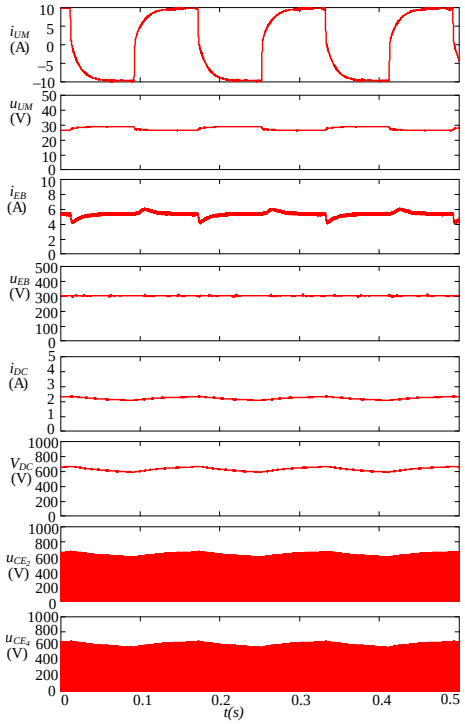

Figure 9. Experimental waveforms of the SPC scheme, for i_{UM} steps from 10 A to −10 A.

7. Losses Comparison and Effects in the Efficiency

From the above discussion, the SPC can be initially considered as an alternative solution for a non-isolated interface in a HSS, in the case that one of the storage devices is rated at very low voltage. As can be seen, the proposed scheme overcomes the main drawbacks of the DPC, FBC and SC schemes. However, major concerns in the performance of the solution arise from the fact that the UM current will flow also through the switches of the EB leg. It means that both switching and conduction losses through these switches will be affected. In the event that the final losses at these switches result in an increase with respect to the original scheme, the overall efficiency loss might make unfeasible the use of this solution. Moreover, as is demonstrated below, the final balance depends on the operation point of the HSS. Thus, a thorough, objective analysis of the time evolution of losses in the system as a function on the mode of operation must be carried out.

To assess this comparison quantitatively, the losses at every switch of converter have been expressed following a simplified theoretical approach. The generic equations of both the switching and conduction losses, for inductive switching of the converter, have been expressed as a function of the EB and UM current values [15]. However, to extract conclusions on the comparison of performances, the figure of merit that is considered is the difference between the losses at both the DPC and SPC configurations, ΔP_{Loss}, rather than the losses at each of the schemes on their own. Thus:

$$\Delta P_{Loss} = P_{Loss}(SPC) - P_{Loss}(DPC) \tag{38}$$

This parameter has been quantified theoretically for the operating parameters in Table 2, and the results are shown in Figure 10. This picture represents ΔP_{Loss} in a grey scale. The darker areas correspond to larger negative differences, i.e., the proposed SPC performs with fewer losses than the original DPC. Conversely, the clearer regions imply larger positive differences, i.e., SPC performs with more losses than DPC. As a conclusion, a better efficiency is obtained by using the proposed SPC

scheme if the system evolves within at the darker areas. This implies both UM and EB currents are large in amplitude and of the same sign, that is to say, both storage devices are simultaneously being either charged or discharged.

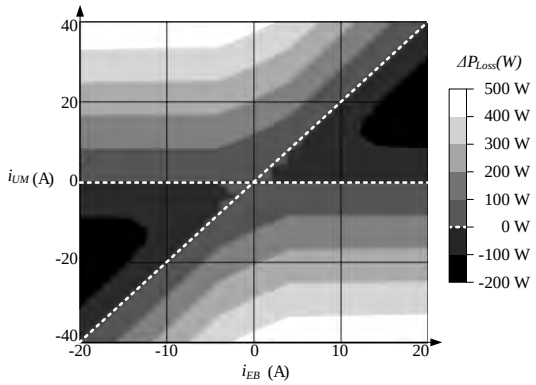

Figure 10. Difference between the losses in DPC and SPC configurations, as a function of the UM and EB currents. The darker areas correspond to SPC scheme operating with fewer losses than the original DPC scheme. For reference, it must be noted that P_{Loss} equals to zero if $i_{UM} = 0$ (i.e., horizontal axis).

The conclusions of this analysis have been validated through a series of experiments on the built setup. Table 5 shows efficiencies and losses obtained in steady state, of both the DPC and SPC configurations, for the known given voltage conditions of V_{DC} = 600 V, u_{EB} = 300 V and u_{UM} = 30 V. The recorded current reference values considered were $i_{UM} = -10$ A, -5 A, 0 A, +5 A and +10 A, and i_{EB} = 0 A, +5 A, +10 A. From these results, it can be verified that the switches losses are lower in SPC provided that the UM and EB currents are both large and of the same sign. On the other hand, if the signs of both currents are opposite, SPC presents more losses than DPC. Thus, Table 5 corroborate the theoretical results depicted in Figure 10. The results in Table 5 are graphically represented in Figure 11. As can be seen, the SPC presents fewer losses when the EB and UM currents have the same sign and larger values. As a conclusion, it must be noticed that, even though at some operating points the losses will be higher with the proposed SPC scheme than in the original DPC scheme, the full performance in terms of efficiency of the proposed topology must be assessed only after considering the application and the control scheme used.

Table 5. Experimental losses and efficiency performance of SPC and DPC configurations.

i^*_{EB} (A)	i^*_{UM} (A)	$P_{Loss}(DPC)$ (W)	$P_{Loss}(SPC)$ (W)	ΔP_{Loss} (W)	η_{DPC} (%)	η_{SPC} (%)
0	10	142.0	248.6	106.6	-	-
0	5	82.0	147.9	65.9	-	-
0	0	20.3	15.1	−5.3	-	-
0	−5	99.8	55.3	−44.5	-	-
0	−10	206.0	250.8	44.8	-	-
5	10	240.1	224.4	−15.7	87.0%	87.4%
5	5	177.8	139.0	−38.8	89.5%	91.6%
5	0	146.0	138.3	−7.7	90.5%	91.0%
5	−5	166.0	191.8	25.9	89.1%	87.4%
5	−10	188.1	277.5	89.4	87.5%	81.9%
10	10	308.6	257.2	−51.5	90.6%	92.1%
10	5	251.8	218.7	−33.1	92.0%	93.1%
10	0	222.7	215.9	−6.9	92.6%	92.9%
10	−5	247.5	293.9	46.4	91.7%	90.3%
10	−10	286.4	363.9	77.5	90.4%	88.0%

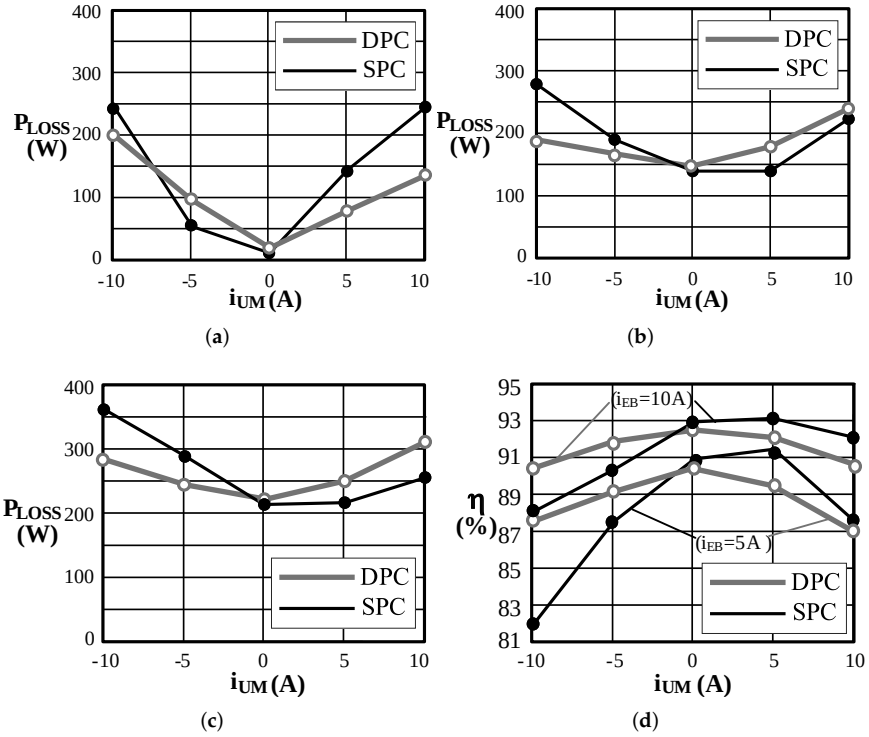

Figure 11. Steady state losses comparison between DPC and SPC configurations: (**a**) i_{EB} = 0 A; (**b**) i_{EB} = 5 A; and (**c**) i_{EB} = 10 A. (**d**) Efficiency measurements of the DPC and SPC schemes, for i_{EB} = 5 A and i_{EB} = 10 A.

8. SPC Scheme in Hybrid Storage Systems Applications

Thus far, the comparison of losses has been carried out considering steady state conditions. This section, instead, deals with the analysis of the SPC performance in HSS applications upon transient operation. For the power flows stated in Figure 1:

$$P_{C_{DC}} = P_{Grid} - P_{Load} + P_{EB} + P_{UM} \tag{39}$$

$$P_D = P_{Grid} - P_{Load} \tag{40}$$

$$P_{ESS} = P_{EB} + P_{UM} \tag{41}$$

where P_{Cdc} is the power absorbed by the DC link capacitor, P_{Grid} is the power coming from the grid, P_{Load} is the power consumed by the load, and P_{EB} and P_{UM} are the power flowing from both the EB and UM, respectively, towards the DC link. These power values are defined as a function of the voltage and current values at each subsystem [14]:

$$P_{Grid} = V_{DC} \cdot i_{Grid_{DC}} \tag{42}$$

$$P_{Load} = V_{DC} \cdot i_{DC} \tag{43}$$

$$P_{EB} = u_{EB} \cdot i_{EB} = V_{DC} \cdot i_{EB_{DC}} \tag{44}$$

$$P_{UM} = u_{UM} \cdot i_{UM} = V_{DC} \cdot i_{UM_{DC}} \tag{45}$$

$$P_{C_{DC}} = V_{DC} \cdot i_{C_{DC}} \tag{46}$$

where $i_{Grid_{DC}}$, i_{DC}, $i_{EB_{DC}}$, $i_{UM_{DC}}$ and $i_{C_{DC}}$ are the currents of the grid, the load, the EB, the UM and the DC link capacitor, respectively, all of them at the DC link side. In the system under consideration, the DC link voltage is regulated and fixed to a reference value. Therefore, in steady state P_{Cdc} is null. Assuming that all the load power is supplied by the grid converter, then the storage system remains idle in steady state, which means that also P_{EB} and P_{UM} are null. Thus, from Equation (39), the following equality applies in steady state:

$$P_{Grid} = P_{Load} \tag{47}$$

However, upon transient variations modeled by power steps in either the grid (line fluctuations) or in the load (random load/stochastic generator), the balance given by Equation (47) is lost. It yields to a transient change in the DC link steady voltage value, that must be compensated by the control scheme if a stable operation is desired [34]. For simplicity, it is assumed that, once the system is in steady state, a load instant power step takes place at a given moment (i.e., the grid power is kept constant). It is also assumed that the hybrid behavior is designed as to achieve UM dynamics (power support) much faster than the EB dynamics (energy support) [35].

Figure 12 sketches this evolution. Interval 1 shows the initial steady state situation, when no power is flowing from any of the storage systems to the DC link. The power that the load is consuming is fully delivered by the grid. The storage system is in idle mode, and thus the currents flowing through the storage devices are null. Interval 2 starts with a sudden load change, in this case a step increase in the load. The control stage reacts demanding more power from the HSS. Therefore, both storage devices start to supply energy to the system. Due the system constraints, the battery has limited safe dynamic response, and hence the power is initially supplied by the UM converter. In any case, P_{UM} and P_{EB}, and therefore i_{EB} and i_{UM}, present the same polarity. As per the aforementioned discussion, this results in smaller current stresses in the switches at the EB leg. Notice that an analogous situation is achieved in the case of decreasing step in the load power.

Once the energy supply is taken over by the EB, the UM must recharge to reach the initial reference value again in a reasonable amount of time. This ensures the HSS is ready to supply again any forthcoming power steps. However, this implies that the sign of the UM current changes, yielding to Interval 3. In this situation, EB and UM currents present opposite signs, resulting in an increase of the stresses at the switches of the EB leg. Nevertheless, this evolution back to idle mode might be done relatively slowly, allowing to minimize the effect of the addition of currents. Then, provided that the control dynamics are tuned adequately, SPC provides a better efficient performance than DPC.

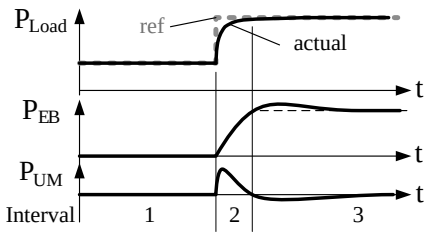

Figure 12. Control operation intervals upon sudden load variation.

9. Stability of the SPC Scheme

Figure 13a shows the scheme of the UM current mode control loop. Although the standard EB current mode and DC link voltage mode control schemes are not represented, it is assumed that these loops are operating properly. $H(s)$ is a signal conditioning block, in charge of measuring, adapting and filtering the current through the UM. The obtained measured value, $I_{UM_{Meas}}$, is compared to the reference, I_{UM}*, to obtain the UM current error, ϵ_I. This error is the input of the regulator $R(s)$. The output of this regulator is the control action that enters the transfer function of the system, $G(s)$.

As seen in Figure 2d, the UM storage device current equals the UM inductor current, and hence the UM control is indeed an inductor current control. Such a control scheme can be implemented considering the inductor voltage, $U_{L_{UM}}$, as the control action. This yields to a transfer function given by:

$$G(s) = \frac{I_{L_{UM}}}{U_{L_{UM}}} = \frac{1}{s \cdot L_{UM} + R_{L_{UM}}} \tag{48}$$

where $R_{L_{UM}}$ is the parasitic resistor of the real magnetic component. This approach results in a simple first order transfer function, and therefore the tuning of the controller can be made very easily. After tuning the regulator, the duty ratio at the UM leg of the converter, D_{3_D}, can be obtained from Equation (29). After linearizing:

$$D_{3_D} = D_{1_D} + \frac{u_{UM} - u_{L_{UM}}}{V_{DC}} \tag{49}$$

Figure 13b shows the block diagram of the control scheme, where the measured DC link and UM voltage values, $V_{DC_{Meas}}$ and $U_{UM_{Meas}}$, respectively, are used to compute D_{3_D}. The implemented filter $H(s)$ is a second order Butterworth filter, on a Sallen–Key configuration, with a cut-off frequency of 3.5 kHz. The chosen bandwidth of the PI regulator $R(s)$ is BW = 300 Hz. The UM inductor has an inductance value of L_{UM} = 21 mH and a series parasitic resistor of R_{UM} = 0.48 Ω. Figure 14 shows the open loop gain of $G(s) \cdot R(s) \cdot H(s)$, used to check the system stability. As can be seen, for this design, the Phase Margin (PM) is close to 90°, therefore the system is stable.

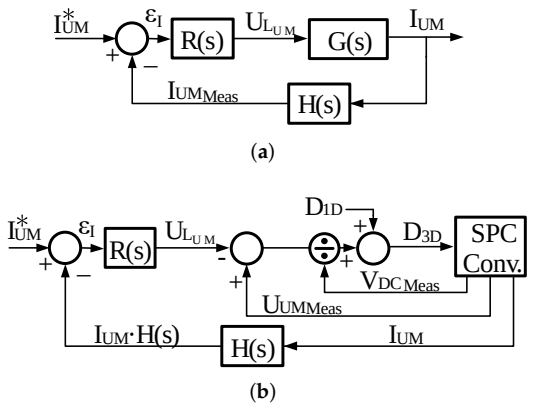

Figure 13. Control schemes: (**a**) Current control loop simplified scheme for tuning the regulator; and (**b**) implemented control scheme, obtaining D_{3_D} from the control action, $U_{L_{UM}}$.

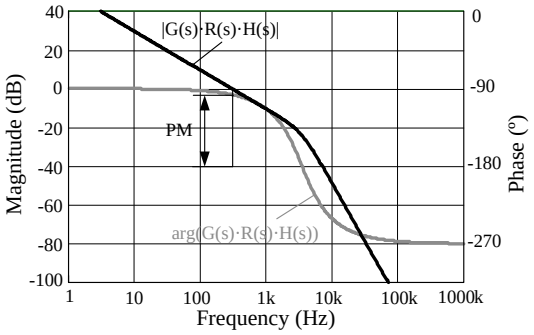

Figure 14. Bode plot with the Phase Margin (PM) of the system.

10. Conclusions and Future Developments

In this work, a comparison among basic power converter topologies for multiport Hybrid Storage Systems (HSSs) has been conducted. The conditions in which the results of the analysis are valid have been clearly defined. These particular constraints include the target application HSS, with a DC link interfaced with two storage units, one of them with significantly smaller voltage ratings. In addition, the constraints consider low/medium power levels where galvanic isolation is not a requirement. The control scheme implemented in the analysis manages the storage power flows to compensate the system DC link voltage due load steps or grid perturbations.

The topologies under study are the base Direct Parallel Connection (DPC) of two bidirectional converters, the Full-Bridge Converter (FBC) configuration for the UM leg, the Series Connection (SC) of the storage devices, and the proposed Series-Parallel Connection (SPC) of the storage units. All these options can be implemented by connecting the power switches in the standard single-leg configuration with complementary control pulses switching. This constraint facilitates the final implementation using ready-to-market, cheap components.

The results of the theoretical study, that included aspects such as losses, efficiency, loss balance between switches, and margins in the control stage design, have been validated by means of simulations and experimental tests on a built laboratory prototype with a rated power level of 10 kW. All throughout the analysis, and for the purpose of finding comparable results, the main parameters in the design, i.e., power, voltage and current levels of the devices were kept constant. For the same reason, also the values of the reactive elements were kept constant.

For HSS applications, SPC presents better efficiency (fewer losses) and also a better distribution of the electrical and thermal stresses in the switches of the legs of the converter. The combination of both effects yield to an increase in the reliability of the system.

The conclusions to this study are shown in Table 6 for DPC, FBC and SPC options. SC has been discarded, as it does not allow the use in HSS due the limitations in the controllability of the storage devices.

Table 6. Configuration performance.

Parameter	DPC	FBC	SPC
Efficiency	Baseline for comparison	Smaller than DPC	Depends on currents sign
Electr. and therm. stress balancing	High mismatch in K_f at switches	K_f at switches evenly distributed	K_f at switches evenly distributed
Control regulation margins	Non-symmetric current control, lim. bandwidth	Symmetrical current control	Symmetrical current control
Control simplicity	Simple, independent current control for EB and UM		
Current ripple through UM	Baseline for comparison at switching frequency	Ripple at twice the switching frequency	Ripple at twice the switching frequency
Current ratings at EB leg switches	Rated for EB peak current	Rated for EB peak current	Rated for algebraic sum at UM and EB peak currents
Size	Baseline for comparison	Increased No. of legs	Same legs than DPC, smaller UM inductor

From the comparison, it can be seen how SPC presents a better electric and thermal stresses balancing than the DPC case. Given that the UM inductor presents half the inductance value than in the DPC case for the same target current ripple, higher power density might also be achieved. SPC also allows for extended control margin. On the other hand, as mentioned, SC does not allow for an independent current control of the storage devices, therefore preventing its use as hybrid storage solution. For SC and FBC cases, the thermal and stresses balance is similar to the SPC, however FBC presents increased power losses vs. SPC.

The comparative efficiency results show how the performance comparison between DPC and SPC depend on the signs of the currents; therefore, the control scheme determines the overall efficiency of the system. From the above discussion, the proposed SPC scheme is considered as a feasible option for non-isolated interfacing of highly mismatched voltage rating storage systems in multiport configurations, for low to medium power rated HSSs applications.

The key issue demonstrated in this work is that, regardless of the efficiency of the base-case (DPC), an increase in the efficiency, in the dynamic performance, and in the stresses distribution in the converter switches achieved by the SPC connection scheme will be obtained, provided that a set of operating constraints are met. In the performed comparison, the hardware setup has been kept constant, and therefore this gain does not yield to modification in the components count or in the basic control implementation requirements.

Future developments include the optimization of the system for increasing the efficiency and power density assuming SPC scheme as the target topology; the inclusion of the energy storage devices modeling as to refine the control algorithms performance; or extension of the proposed solution in other kind of applications apart from HSS.

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Author Contributions: Ramy Georgious and Jorge Garcia conceived the research and designed the experiments. Ramy Georgious performed the experiments and wrote the paper. All authors analyzed the data, and contributed in the discussion and conclusions

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Abbreviations

The following abbreviations are used in this manuscript:

DPC	Direct Parallel Connection
EB	Electrochemical Battery
ESS	Energy Storage System
FBC	Full-Bridge Converter
K_f	Form Factor
HSS	Hybrid Storage Systems
PEC	Power Electronic Converter
PECG	Grid-tied Power Electronic Converter
PECL	Power Electronic Converter at Load/Generator
SC	Series Connection
SPC	Series-Parallel Connection
UM	Ultracapacitor Module

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C.3 Publication III

R. Georgious, J. García, Á. Navarro-Rodríguez and P. García, "A study on the control loop design of non-isolated configurations for hybrid storage systems," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-6.

A Study on the Control Loop Design of Non-Isolated Configurations for Hybrid Storage Systems

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***Abstract*— This work focuses on the control strategies for different configurations of Non-Isolated Hybrid Energy Storage Systems. Basic strategies are proposed, studied and compared. Parting from the standard parallel connection of bidirectional boost converter in hybrid storage systems, a comparison with alternate topologies is presented. These alternative schemes overcome the problems that arise in the original configuration due the high mismatch in voltage ratings of the individual storage systems. A strategy to design the control loops of the resulting Hybrid Energy Storage System is proposed, studied, simulated and experimentally implemented on a 1.5 kW demonstrator. The control strategy is implemented in the standard bidirectional boost converter approach and also in the series-parallel connection of the storage units. The reported results show how the proposed control strategy applied to the series parallel connection presents a good performance in terms of dynamic and steady state operation.**

Keywords— Energy Storage System; Boost Converters; Hybrid; Series-Parallel Connection;

I. INTRODUCTION

Nowadays, the most common Energy Storage Systems (ESSs) implemented in DC microgrids are hybridized, thus combining a bulk ESS, usually presenting slow-dynamics (such as an electrochemical battery e.g. Lithium Ion Battery (LIB)) plus a high-power fast-dynamics storage module (e.g. a Supercapacitor Module, SM). Therefore, by using such a Hybrid ESS, the expected performance implies a decrease in the overall system costs (reducing the battery size and increasing the life span of the battery) and an increase in the system reliability (decreasing the stresses on the battery during transient stages) [1] – [15].

The simplest connection of the Hybrid ESS able to fully control the power flow from and into every storage device and the DC link is the Parallel Connection (PC), shown in Fig. 1, based on two bidirectional boost converters connected to the DC link itself. This scheme can also be defined as a H-bridge configuration [1]-[3], [6], [8], [9], [11], [15]. The main limitations of this connection come from the high voltage mismatch between the SM voltage ratings and the DC link bus voltage. Considering a battery rated voltage of around half the DC link voltage, then the duty ratio of the battery leg will be around 50%, thus optimizing the performance of such converter, in terms of stresses balancing, design complexity and control capability. However, provided that in some applications the SM voltage ratings are ranged from 20V to 40V, then for DC bus voltage ratings ranged from 500V to 900V the required gains for the dedicated interfacing converter will reach values up to 40:1 or even higher.

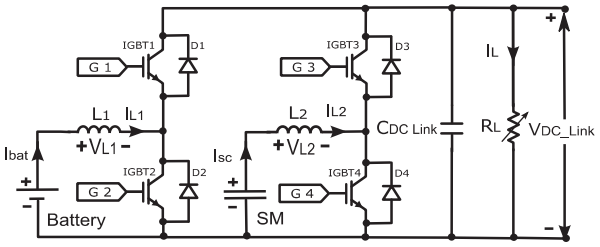

Fig. 1. Parallel Connection (PC) of two bidirectional boost converters connected to Lithium Ion Battery (LIB) and Supercapacitor Module (SM) and sharing the DC link.

Such requirements cannot be accomplished by the commonly used single-stage non-isolated converter topologies [16]. But even for practical gain values (say 10:1), the bidirectional boost converter experiences an increase in the stresses unbalancing on the IGBTs, a decrease the control margin of the converter, more sensitivity to parasitic elements, etc. [16]. To overcome these drawbacks, a solution without moving to more complex schemes (such as cascaded, multilevel or isolated approaches) is the Series-Parallel Connection (SPC) depicted in Fig. 2 [17]. The negative terminal of the SM is connected to the middle point of the leg connected to the battery.

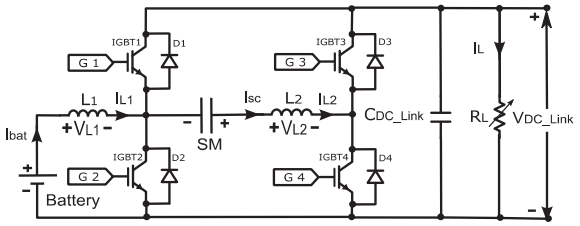

Fig. 2. Series-Parallel Connection (SPC) of two bidirectional boost converters connected to Lithium Ion Battery (LIB) and Supercapacitor Module (SM) and sharing the DC link.

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II. Comparison of Configurations

In order to demonstrate the operation of the proposed solution, the system under consideration has the following operating conditions: 300V nominal voltage battery (e.g. a Li-Ion battery), 30V rated SM voltage and 500V nominal voltage DC-link. The performance will be assessed in steady-state. Under PC scheme, the usual boost converter equations are fulfilled, therefore, the corresponding duty cycles at steady state for the IGBT 1 (at the leg connected to the battery) and IGBT 3 (at the leg connected to the SM), D_{Bat} and D_{SM}, respectively, follow the following expressions:

$$D_{Bat} = \frac{V_{Bat}}{V_{DC\_Link}} = 60\ \% \quad (1)$$

$$D_{SM} = \frac{V_{SM}}{V_{DC\_Link}} = 6\ \% \quad (2)$$

where, V_{Bat}, V_{SM} and V_{DC_Link} are the battery, the SM and the DC link voltage values in Volts, respectively.

Thus, IGBT 3 is turned on 6 % of the switching time, while the IGBT 4 is turned on 94 % of the switching time. The small duty cycle of the SM leg yields to thermal and electrical stresses mismatch on the switches. On the other hand, under SPC scheme, the following equation applies to the leg formed by IGBT 3 and IGBT 4:

$$V_{Bat} - V_{L1} + V_{SM} - V_{L2} = D_{SM} \cdot V_{DC\_Link} \quad (3)$$

Where, V_{L1} and V_{L2} are the voltages in the inductors connected to the battery and to the SM in Volts, respectively.

Upon steady state condition, the inductor voltages are null, therefore the value of the duty ratio at the SM leg is given by:

$$D_{SM} = \frac{V_{SM} + V_{Bat}}{V_{DC\_Link}} = 66\ \% \quad (4)$$

The value of the duty ratio at the battery leg is given by (1). With the same voltage values than in the PC case, IGBT 3 is turned on 66 % and IGBT 4 is turned on 34 % of the switching time in the SPC scheme. This yields to a balance in the thermal stress on the switches for the SM leg. In the aforementioned connection, the duty cycle of the IGBT 3 is a function of the supercapacitor voltage and battery voltage, not only of the supercapacitor voltage as in case of PC. Therefore, the stresses in the switches of the SM leg are much more balanced than in the previous case, yielding to a better performance in terms of reliability and increased control margin.

The main drawback is the appearance of circulating extra currents through the switches of the battery leg in the SPC. However, in the case of using a SM for transient compensation of power demands, where most of the time the current reference for the SM will be null, this issue is not a concern. Thus, the SPC is an option for some applications of Hybrid ESS with high voltage ratings mismatch. In order to assess its performance, a deep analysis of the control system required to govern the power flows in the converter is needed.

III. Proposed Control of the Series-Parallel Connection

For the PC in Fig. 1 considering now transient state, the following relationships for the duty cycles are found:

$$D_{Bat} = \frac{V_{Bat} - V_{L1}}{V_{DC\_Link}} \quad (5)$$

$$D_{SM} = \frac{V_{SM} - V_{L2}}{V_{DC\_Link}} \quad (6)$$

Through the V-I characteristic of these inductors, two independent current control loops can be implemented for each of the storage devices, simplifying the control design. For instance, the bandwidth of the storage systems can be made significantly different, therefore limiting the di/dt of the battery, forcing the SM to cope with the fast power variations required by the DC-link. The instant value of the duty ratios in the converters states the capability of providing a given transient voltage to the inductors in the converters, therefore yielding to a given current by those inductors. In addition to stresses unbalance in the switches and poor performance due extreme duty ratios, the main problem in PC comes from the fact that in the SM leg, the starting value of the duty ratio is quite small (6%).

If a high SM charging current is required, the control system acts providing a high duty ratio to this leg (say 80%), and therefore, the resulting voltage in the SM inductor increases noticeably (up to 450-500V), and therefore a very high SM charging current can be achieved. But in the opposite case, when a high discharging SM current is desired, the duty ratio of the SM leg cannot be smaller than 0, and therefore the discharging voltage in this inductor is limited to the SM voltage (say 30V), and therefore the discharging current is significantly smaller than the charging one. This results in a non-symmetric behavior of the control, which is not admissible for a transient compensating scheme.

However, In SPC the duty cycle of the IGBT 3 is a function also of the voltage at the inductor connected to the battery. This ultimately yields to an extension on the values that the SM inductor might take, and therefore extending the range of symmetrical behavior. From (1) and (3), for SPC in Fig. 2, the following relationships of the duty cycles are found:

$$D_{Bat} = \frac{V_{Bat} - V_{L1}}{V_{DC\_Link}} \quad (7)$$

$$D_{SM} = \frac{V_{SM} - V_{L2} + V_{Bat} - V_{L1}}{V_{DC\_Link}} \quad (8)$$

The control strategy proposed and implemented is discussed ahead. This control considers that the DC bus voltage is controlled by an inverter connected to the grid (not represented in the figures 1 and 2). The aim of the control is the SM delivers or absorbs the transient peak power and the LIB delivers or absorbs the rest of the transient power in order to improve the recovery of the DC link due to load variations. Fig. 3 shows the control scheme of the PC; as it can be seen, the total ESS power reference is generated by measuring the load power and filtering through a High Pass Filter (HPF) [7], [18]. This total ESS power reference is not directly applied to the system. Instead, another SM power reference is generated by using a different HPF (with a higher cut-off frequency). A limiter is used to ensure that the SM power limits are not exceeded. This SM power reference is applied to the SM control loop. Finally, the power reference for the battery control loop is obtained as a difference between the total ESS power and the SM power reference [9], [15]. Another limiter is

used to ensure that the LIB limits are not exceeded. The power expressions are defined as following:

$$P_{\text{L\_meas}} = I_{\text{L\_meas}} * V_{\text{DC\_meas}} \quad (9)$$

$$P_{\text{ESS\_ref}} = \frac{T_{ESS} * s}{1+T_{ESS} * s} * P_{\text{L\_meas}} \quad (10)$$

$$P_{\text{SM\_ref}} = \frac{T_{SM} * s}{1+T_{SM} * s} * P_{\text{L\_meas}} \quad (11)$$

$$P_{\text{Bat\_ref}} = P_{\text{ESS\_ref}} - P_{\text{SM\_ref}} \quad (12)$$

where:

- P_{L_meas} is the measured power of the load in Watts,
- P_{ESS_ref}, P_{SM_ref} and P_{Bat_ref} are the reference powers of the ESS, SM and LIB respectively in Watts,
- I_{L_meas} is the measured current of the load in Amps,
- V_{DC_meas} is the measured DC link voltage in Volts,
- T_{ESS} is the time constant of the HPF of the ESS power in Secs,
- T_{SM} is the time constant of the HPF of the SM power in Secs,
- s is the Laplace complex variable; $s=\sigma+j\omega d$.

Once the power reference values are obtained, the current references of the battery and SM loops are calculated by dividing by the battery and SM measured voltages, respectively. The current of the inductors connected to LIB and SM are the same the currents of the LIB and SM, respectively. As regulators, typical PI current controllers in ideal form (tuned by zero-pole cancellation considering the RL equivalents of the inductors) are used as in (13). The bandwidth (BW) of the SM current controller is higher than the BW of the battery current controller[2], thus guaranteeing that the SM will supply or absorb the peak transient power during load variations. The limits for the inductors voltage are calculated as in (13)-(16).

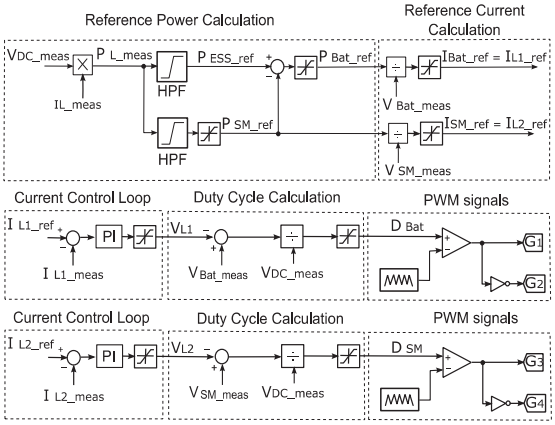

Fig. 3. Control of the Parallel Connection (PC) in order to provide or absorb transient power during load variations in order to improve the recovery of the DC link due to load variatons.

$$C(s) = K_p * (1 + \frac{K_i}{s}) \quad (13)$$

where:

- C(s) is the transfer function of the PI controller,
- K_p is the proportional gain,
- K_i is the integral gain.

$$V_{L1\_min} = V_{Bat\_meas} - V_{DC\_meas} \quad (14)$$

$$V_{L1\_max} = V_{Bat\_meas} \quad (15)$$

$$V_{L2\_min} = V_{SM\_meas} - V_{DC\_meas} \quad (16)$$

$$V_{L2\_max} = V_{SM\_meas} \quad (17)$$

where:

- V_{L1_min}, V_{L1_max}, V_{L2_min} and V_{L1_max}, are the minimum and maximum inductor voltages in Volts for the LIB and SM boost converters respectively.
- V_{Bat_meas} and V_{SM_meas} are the measured storage device voltages in Volts.

Figure 4 shows the proposed control in the SPC scheme, the difference between the two control schemes is the calculating of the duty cycle of the SM in each connection. The limits for the inductors voltage are the same as in (14), (15) and (17), however the maximum voltage of the inductor connected to the SM is calculated as following:

$$V_{L2\_max} = V_{SM\_meas} + V_{DC\_meas} \quad (18)$$

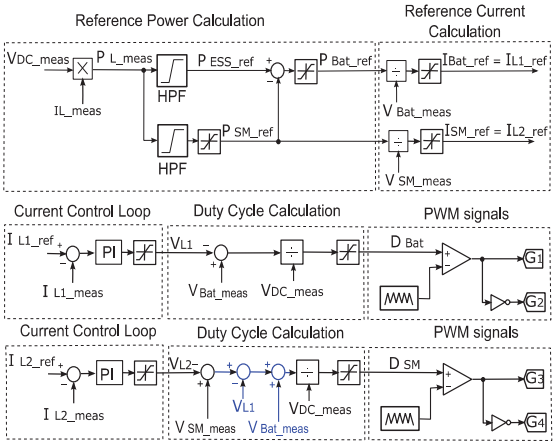

Fig. 4. Propsed control of the Series-Parallel Connection (SPC) in order to provide or absorb transient power during load variations in order to improve the recovery of the DC link due to load variatons.

IV. Validation of the Propsed Control through Simulation

The simulations carried out for demonstrating the proposed control performance have been done for the full Hybrid ESS, both in PC and SPC schemes. A State of Charge (SOC) of the battery of 50% is considered, and the rated SM voltage value

used for calculating the reference power for the battery is the same in all cases. The parameters used in the operating conditions are listed in Table 1 and the control parameters used are in Table 2.

A sudden load step of ±50% in a 1.5kW rated converter operation has been simulated, both for the PC and SPC schemes. The DC link voltage is controlled by a inverter connected to the grid in order to maintain the DC link voltage around 500 V. It is seen in Fig. 5 that the performance of the two Hybrid ESS is similar, the load power is changed from 833.3 W to 1666.7 W at 0.5 seconds and again to 833.3 W at 2.5 seconds. The SM delivered the transient peak power and the LIB delivered the rest of the transient power at 0.5 seconds. At 2.5 seconds, the SM absorbed the transient peak power and the LIB absorbed the rest of the transient power.

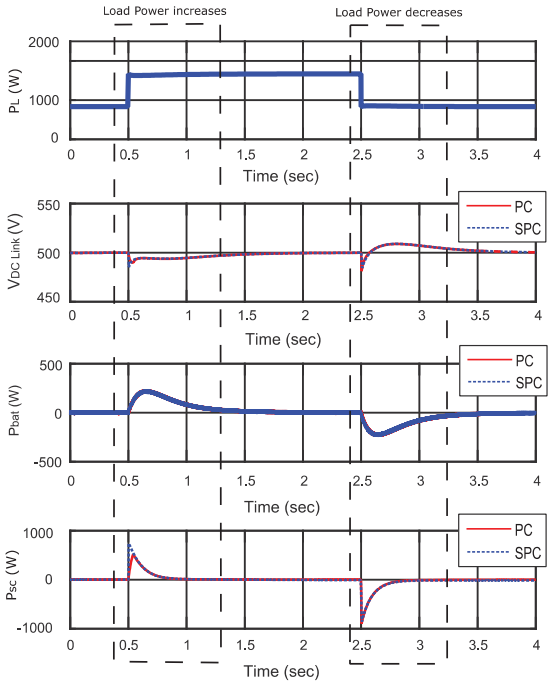

Fig. 5. Simulation results for the Parallel Connection (PC) and the Series Parallel Connection (SPC) where the load power is changed from 833.3 W to 1666.7 W at 0.5 seconds and then to 833.3 W again at 2.5 seconds.

Table 1. Parameters of the converters.

Parameter	Symbol	Value
Nominal Battery voltage	V_{Bat}	300 V
Nominal SM voltage	V_{SC}	30 V
Capacitance of the SM	C_{SC}	165 F
DC link voltage	V_{DC}	500 V
Capacitance of the DC link	C_{DC}	470 µF
Maximum load power	P_{L_max}	1666.7 W
Inductance of the inductors	L	21 mH
Resistance of the inductors	R	0.3 Ω

Table 2. Parameters of the control of the converters.

Parameter	Symbol	Value
HPF of the ESS Power		
Cut off frequency	F_{HPF_ESS}	0.7 Hz
HPF of the SM Power		
Cut off frequency	F_{HPF_SM}	1.5 Hz
Current Control Loop for LIB		
Bandwidth	BW_{LIB}	300 Hz
Proportional gain	K_{P_LIB}	39.564
Integral gain	K_{I_LIB}	22.8571
Current Control Loop for SC		
Bandwidth	BW_{SC}	500 Hz
Proportional gain	K_{P_SC}	65.94
Integral gain	K_{I_SC}	22.8571

However, the duty cycle of the SM leg is different; for the SPC scheme, the duty cycle of the SM leg is 0.66, as shown in Fig. 6. All the aforementioned problems of the too narrow duty ratio obtained for PC scheme is therefore solved in the SPC configuration. This yields to decrease the thermal and electrical stresses on the switches.

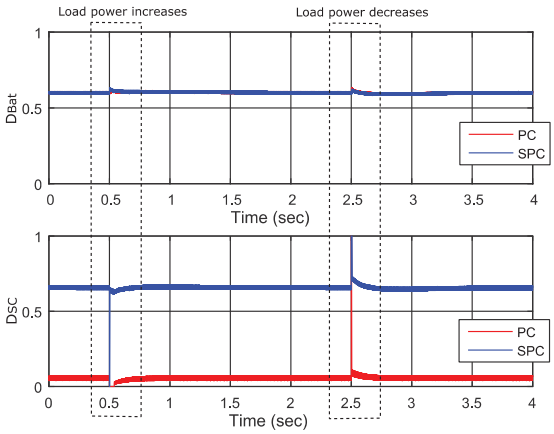

Fig. 6. Simulation Results of the Battery duty cycle (D_{Bat}) and Supercapacitor Module duty cycle (D_{SM}) for the Parallel Connection (PC) and the Series Parallel Connection (SPC) where the load power is changed from 833.3 W to 1666.7 W at 0.5 seconds and then to 833.3 W again at 2.5 seconds.

V. Validation of the Proposed Control by Experimental Results

The Experimental results are done in a 2 KW demonstrator setup shown in Fig. 7. Considering the DC link voltage is controlled by the grid inverter to maintain the DC link voltage around 500 Volts. In order to demonstrate the merits and the feasibility of the SPC, the current control is tested for the PC and SPC. A 5 Amps LIB current reference and 10 Amps SM current reference are applied. As shown in Fig. 8 and Fig. 9, the collector-emitter voltage of IGBT 2 (V_{CE2}) and the

collector-emitter voltage of IGBT 4 (V_{CE4}) are representing the duty cycles of the LIB and SM, respectively. The duty cycle of SM in PC is a very small value compared to the duty cycle of the LIB as in Fig. 8. However, in Fig. 9 the duty cycle of the SM is a little bit higher than the duty cycle of LIB. This yields to decrease the thermal and electrical stresses and increasing the life time of the IGBTs and solving the problem of voltage mismatch.

In order to demonstrate the feasibility of the proposed control strategy, the PC and SPC are tested. Fig. 8 is showing the performance of the PC and SPC when the load power is changed from 833.3 W to 1666.7 W at 0.5 seconds and then to 833.3 W again at 2.6 seconds. It is fully matched with the results obtained in Fig. 5 from simulations.

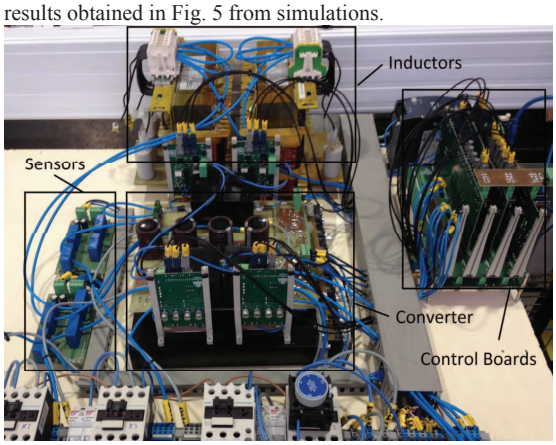

Fig. 7. Experimental setup and it can be Parallel Connection (PC) or Series-Parallel Connection (SPC).

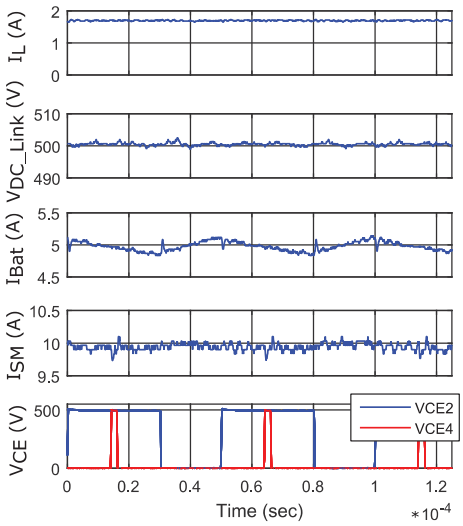

Fig. 8. Experimental results for the Parallel Connection (PC) where 5 Amps LIB current reference and 10 Amps SM current reference are applied and the DC link is controlled by the grid inverter.

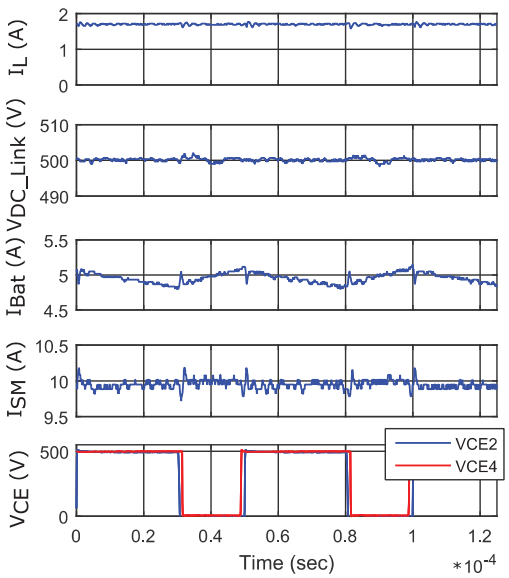

Fig. 9. Experimental results for the Series-Parallel Connection (SPC) where 5 Amps LIB current reference and 10 Amps SM current reference are applied and the DC link is controlled by the grid inverter.

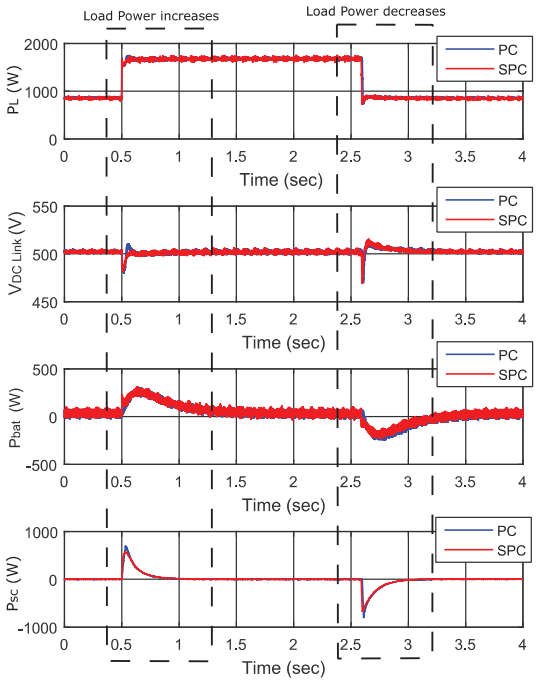

Fig.10. Experimental results for the Parallel Connection (PC) and the Series Parallel Connection (SPC) where the load power is changed from 833.3 W to 1666.7 W at 0.5 seconds and then to 833.3 W again at 2.5 seconds.

VI. Conclusions and Future Developments

In this paper, a control loop design strategy for the series-parallel connection (SPC) of Hybrid ESS is proposed, studied, simulated and experimentally validated at 2 KW demonstrator setup. The performance of this strategy is compared to the original parallel configuration of the storage units. The results show that the proposed control for the SPC scheme keeps the DC-link under control upon sudden load variations, with a non-isolated, transformerless simple solution. This solution decreases the thermal and electrical stress on the switches by balancing the voltage on the switches. This solution can be used in high voltage mismatch application in hybrid systems.

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C.4 Publication IV

R. Georgious, J. García, P. García and M. Sumner, "Analysis of hybrid energy storage systems with DC link fault ride-through capability," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8.

Analysis of Hybrid Energy Storage Systems with DC Link Fault Ride-Through Capability

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***Abstract*—In this work, a Fault Ride-Through control scheme for a non-isolated power topology for Hybrid Energy Storage Systems in a DC microgrid is presented. The Hybrid System is created from a Lithium-Ion Battery and a Supercapacitor Module coordinated to achieve a high-energy and high-power storage system; it is connected to a DC link to interface to the outer system. The power topology under consideration is based on the buck-boost bidirectional converter, and it is controlled through a bespoke modulation scheme in order to obtain low losses in nominal operation. The operation of the proposed control during a DC link short-circuit failure is shown as well as a modification to the standard control in order to achieve Fault Ride-Through once the fault is over. The operation of the converter is theoretically developed and it is verified through simulation and experimental validation.**

Keywords—hybrid; Energy Storage System; buck-boost converter; Fault Ride-Through capability;

I. Introduction

The simplest topology for interfacing the Energy Storage devices in Hybrid Energy Storage Systems (HESS) to a DC microgrid is the direct connection of two parallel bidirectional boost converters to the DC link, as shown in Fig. 1. This is a cost-effective and reliable solution for low-to-medium power range applications, as the number of elements and devices is relatively low [1]-[7]. This solution is valid if galvanic isolation is not a requirement. The case studied here considers the simple parallel connection of two distinct Energy Storage devices. One port consists of a Lithium-Ion Battery (LIB), which will provide a high energy density with slow dynamic response. The other port interfaces to a Supercapacitor Module (SM) intended to support a high power density and faster dynamic response [1]-[8]. Therefore, provided that the control strategy is managed correctly, the resulting HESS has a better overall performance than either of the individual systems, allowing for a sustained, high-power high-dynamic performance of the storage system, and potentially a longer battery lifetime.

In addition to the lack of galvanic isolation, a major disadvantage of this system is its sensitivity to short circuit faults on the DC link. If a short circuit occurs, the current drawn from both the LIB and the SM will increase without control, as the anti-parallel diodes of the upper switches in the legs of the boost converters would allow large short-circuit currents. This will cause damage to the inductors, the storage devices (LIB and SM), and the switches themselves. This paper describes a new circuit and control topology which will limit operation during DC side short circuit faults and can also recover quickly once the fault has been cleared.

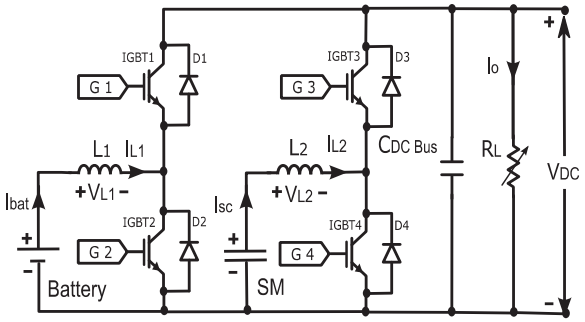

Fig. 1. Two parallel bidirectional boost converters connected to Lithium Ion Battery (LIB) and Supercapacitor Module (SM) and sharing the DC link.

II. Fault-Tolerent Topologies

The solution to the DC link fault ride through problem is the connection of a device that is able to limit/interrupt the fault currents coming from the storage units. One option is to connect switches in series with the storage units and the inductors of the converters (see Fig. 2). These switches can be opened during the fault in order to prevent the LIB and SM short-circuit currents. In addition, in order to allow a discharge path for any current flowing through the inductors when the series switches are opened, additional free-wheeling switches for each leg are required. Otherwise, a voltage spike will occur, causing arcing or even destruction of the switches. This yields a final configuration of two parallel bidirectional buck-boost converters, as shown in Fig. 3.

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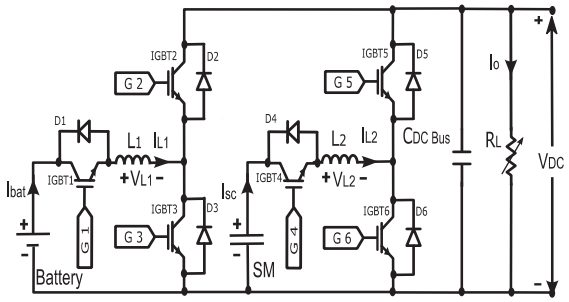

Fig. 2. Two parallel bidirectional boost converters with a switch in series between the storage devices and inductors.

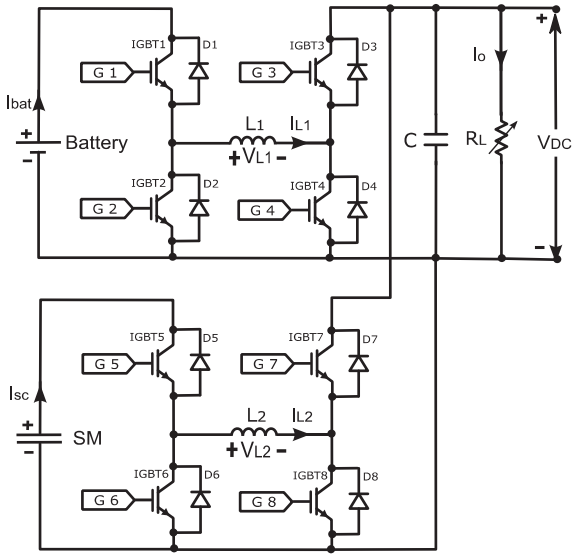

Fig. 3. Two parallel bidirectional buck-boost converters connected to Lithium Ion Battery (LIB) and Supercapacitor Module (SM) and sharing the DC link.

It can be seen that the inclusion of the short-circuit fault tolerant features in the converter adds four more switches compared to the original topology (Fig. 1), therefore resulting in higher costs and size than in the initial case. However, by using a proper control, (as will be demonstrated), the losses of the two topologies can be made very similar. The operation under fault mode will be discussed in this work; however, the studied system with the proposed control strategy has the capability of operating in a step-down voltage mode. Provided that a suitable control strategy is implemented, this voltage mode enables for a swift system reset once the fault is cleared. A proposal for such a fault ride-through feature will also be demonstrated in the following sections.

III. Proposed Control Strategy

In the case under study, the main goal of the control of the battery converter is to maintain the DC link voltage constant, while the aim of the control of the SM converter is to provide or absorb transient power during load variations. This control strategy is implemented through three control loops: one outer voltage control loop that controls the DC link voltage, plus two inner current loops in order to control the current flowing through the inductors [2],[3],[6], as shown in Fig. 4.

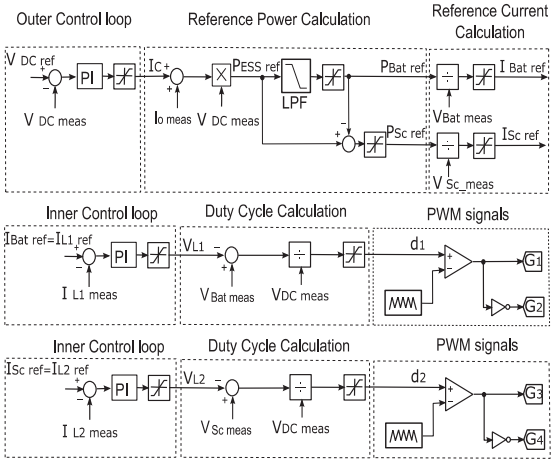

Fig. 4. Control of the two parallel bidirectional Boost Converters in order to maintain the DC link voltage constant (LIB converter) and provide or absorb transient power during load variations (SM converter).

The Energy Storage System (ESS) power reference is calculated from the control action of the voltage control loop (I_c) and the feedforward term (I_{o_meas}) to improve the recovery of the DC Link due to load variations. The limits of the control action are obtained from (1) and (2).

$$I_{c\_min} = \frac{-V_{dc\_ref}}{R_{L\_min}} \quad (1)$$

$$I_{c\_max} = I_{Bat\_max} - \frac{V_{dc\_ref}}{R_{L\_max}} \quad (2)$$

where:

- I_{c_min} and I_{c_max} are the minimum and maximum current limits of the DC link current in Amps,
- V_{DC_ref} is the reference DC link voltage is Volts,
- R_{L_min} and R_{L_min} are the minimum and maximum load resistance in Ohms and can be obtained from the load profile,
- I_{bat_max} is the LIB maximum current in Amps.

The SM reference power is calculated as the difference between the references for the ESS and LIB power values. A limiter is used to ensure that SM power limits are not exceeded. The LIB power reference is calculated by using a Low Pass

Filter (LPF) to ensure that the SM is providing or absorbing the peak transient power during load variations. Also another limiter is used here, to ensure that the SM provides (or absorbs) the excess power that LIB cannot provide (or absorb) during steady state. The power references are calculated according to the following equations:

$$P_{\text{ESS\_ref}} = (I_c + I_{\text{o\_meas}}) * V_{\text{DC\_meas}} \quad (3)$$

$$P_{\text{Bat\_ref}} = \frac{1}{1+\text{Ts}} * P_{\text{ESS\_ref}} \quad (4)$$

$$P_{\text{Sc\_ref}} = P_{\text{ESS\_ref}} - P_{\text{Bat\_ref}} \quad (5)$$

where:

- P_{ESS_ref}, P_{Bat_ref} and P_{Sc_ref} are the reference powers of the ESS, LIB and SM respectively in Watts,
- I_c is the current in the DC link (control action of the voltage controller) in Amps,
- I_{o_meas} is the measured output current of the two converters in Amps,
- V_{DC_meas} is the measured DC link voltage in Volts,
- T is the time constant of the LPF in Secs,
- s is the Laplace complex variable; s=σ+jωd.

The bandwidth of the controller for the current in L2 (inductor in SM converter) is faster than the bandwidth of the controller for inductor L1 (LIB converter). This control scheme considers the inductor voltages, V_{L1} and V_{L2} in Fig. 3 to be the control actions at the output of the current regulators. The limits for the inductor voltages are developed as in (6) - (9). Therefore an adaptation between these control actions and the applied duty cycles in both converters, d_1 and d_2, is implemented in the control (Duty Cycle Calculation blocks in Fig. 4).

$$V_{\text{L1\_min}} = V_{\text{Bat\_meas}} - V_{\text{DC\_ref}} \quad (6)$$

$$V_{\text{L1\_max}} = V_{Bat\_meas} \quad (7)$$

$$V_{\text{L2\_min}} = V_{Sc\_meas} - V_{\text{DC\_ref}} \quad (8)$$

$$V_{\text{L2\_max}} = V_{\text{Sc\_meas}} \quad (9)$$

$$d_1 = \frac{-V_{L1}+V_{Bat\_meas}}{V_{DC\_meas}} \quad (10)$$

$$d_2 = \frac{-V_{L2}+V_{SC\_meas}}{V_{DC\_meas}} \quad (11)$$

where:

- V_{L1_min}, V_{L1_max}, V_{L2_min} and V_{L1_max} are the minimum and maximum inductor voltages for the LIB and SM boost converters respectively.
- V_{Bat_meas} and V_{SC_meas} are the measured storage device voltages in Volts,
- d_1 and d_2 are the duty ratios of the LIB and SM converters respectively,
- V_{L1} and V_{L2} are the inductor voltages (control action of the current controller) for the LIB and SM boost converters respectively.

If these inductor voltage control schemes are implemented in the buck-boost converters, some modifications are required in order to calculate the duty cycle from the output of the regulator (Duty Cycle Calculation block), as shown in Fig. 5. With this direct approach, the diagonal switches (S1 and S4) and (S5 and S8) will commutate with the values of the duty cycle for the LIB and SM converters respectively, while the other diagonal switches (S2 and S3) and (S5 and S6) are complementary. This approach will increase the switching losses and the total efficiency of the system will drop. The expressions to calculate the duty ratio for both the LIB and SM converters and the limits for the inductor voltages in this case are shown in (12) - (17).

$$V_{\text{L1\_min}} = -V_{\text{DC\_ref}} \quad (12)$$

$$V_{\text{L1\_max}} = V_{Bat\_meas} \quad (13)$$

$$V_{\text{L2\_min}} = -V_{\text{DC\_ref}} \quad (14)$$

$$V_{\text{L2\_max}} = V_{\text{Sc\_meas}} \quad (15)$$

$$d_1 = \frac{V_{L1}+V_{DC\_meas}}{V_{Bat\_meas}+V_{DC\_meas}} \quad (16)$$

$$d_2 = \frac{V_{L2}+V_{DC\_meas}}{V_{SC\_meas}+V_{DC\_meas}} \quad (17)$$

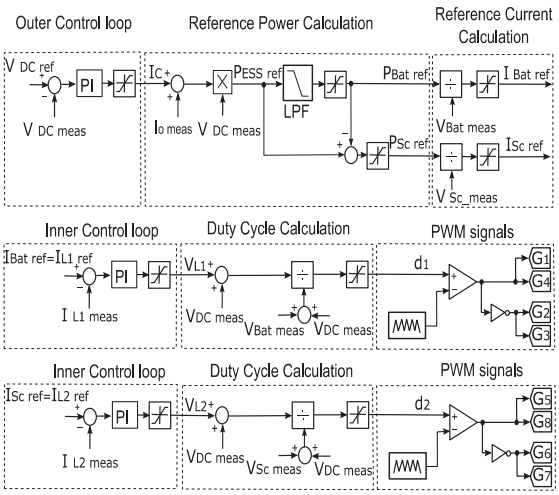

Fig. 5. Control of two parallel bidirectional buck-boost converters with the same carrier in order to maintain the DC link voltage constant (LIB converter) and provide or absorb transient power during load variations (SM converter) .

The idea of the proposed control strategy deals with using two independent modes of operation for each converter during the healthy condition (Normal Operation) i.e. Buck Mode and Boost Mode, aiming to decrease the number of commutating switches in each converter, in order to decrease the switching losses [9]-[11]. In order to achieve a swift transition between the two switching modes, a PWM modulation of the converters through a triangle waveform will be implemented. However, this modulation will be based on two different triangle carriers signals: one carrier for the Buck mode (using peak values of the triangular waveform from 0.0 to 0.5), and another carrier for the Boost mode (using values from 0.5 to 1.0).

This structure implies no overlapping of the switching intervals, which yields two different switching patterns for the switches. For example (as shown in Fig. 6.), if the desired duty cycle is between 0.0 and 0.5, the bidirectional buck-boost converter operates in Buck mode, and therefore switches S4 and S8 are turned off, while switches S3 and S7 remain turned on continuously. The switches S1 and S5 switch with the value of the duty cycle and the switches S2 and S6 are their complement. For the Boost mode, when the duty cycle is between 0.5 and 1.0, switches S1 and S5 are turned on and switches S2 and S6 remain off continuously. Switches S4 and S8 switch with value of the duty cycle and the switches S3 and S7 are their complement. Fig. 7 depicts the implementation of this dual carrier control for the two parallel bidirectional buck-boost converters. The limits of the inductor voltage are the same as the case of the boost converter (6) - (9).

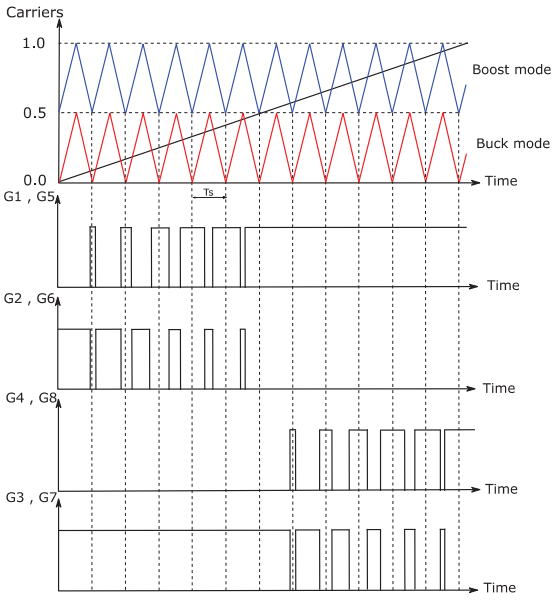

Fig. 6. PWM modulation of the two parallel bidirectional buck-boost converters based on two different carriers.

The possible short-circuit faults types in DC microgrids are short-circuit between positive and negative bus, or a short-circuit between any bus and ground [12]. Once a short-circuit fault is detected in the DC link (for instance by detecting a DC link voltage below a threshold level), all the switches of the storage converters will be turned off. This control scheme does not have ride-through capability, and therefore if the fault is removed, the system by itself has no ability for returning to the initial operation mode, unless the control is reset manually and the DC link is charged. By making a modification to the control scheme, as show in Fig. 8, the converter can still operate in a controlled manner under fault conditions, and can resume normal operation once the fault is over.

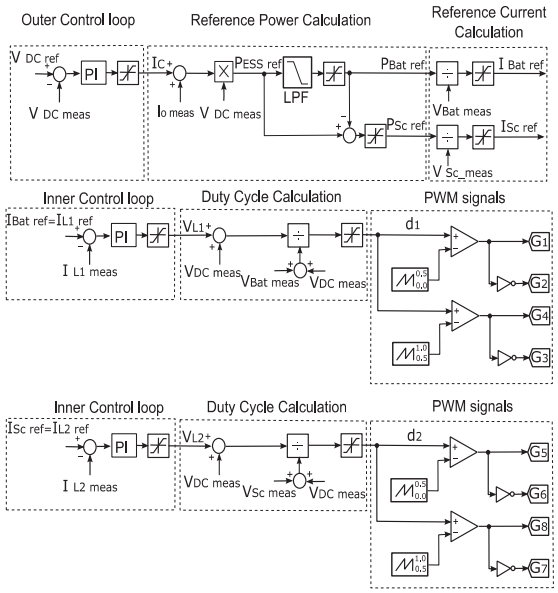

Fig. 7. Control of the two parallel bidirectional buck-boost converters with two different carriers in order to maintain the DC link voltage constant (LIB converter) and provide or absorb transient power during load variations (SM converter).

In this proposed control, while the short-circuit fault is present, a small safe current reference is applied to the LIB converter. This current reference depends on the DC link capacitance and how quickly the DC link charges after the fault is cleared. However, the switches of the SM converter will be turned off. The voltage across the inductor is limited and the duty cycle for LIB is therefore given by (18) to (20). Once the fault is cleared, this LIB current charges the DC link capacitors up to a specific value below the DC link reference voltage value. Once this value is detected, the control returns to the normal control scheme. If the fault is permanent, the control operates for a specific time and then the switches of the LIB converters will be turned off. Another advantage is that this control can be used to charge the DC link when the converter starts.

$$V_{\mathrm{L1\_min}} = 0 \qquad (18)$$

$$V_{\mathrm{L1\_max}} = V_{Bat\_meas} \quad (19)$$

$$d_1 = \frac{V_{L1}}{V_{Bat\_meas}} \quad (20)$$

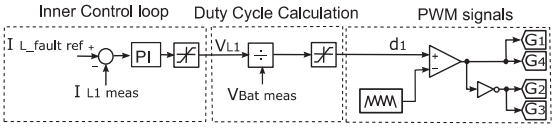

Fig. 8.Propsed control of the two parallel bidirectional buck-boost converters during the DC link fault.

IV. Validation of the System Operation Under Normal and Fault Conditions through Simulation

Simulations of the full system operation have been carried out with MATLAB/SIMULINK/PLECS. The operating conditions of the systems for these simulations are listed in Table 1. Considering the ideal form of PI controller which is tuned by zero-pole cancellation, the transfer function is given by (21). The control parameters of the converters are listed in Table 2. Special attention has been put on the calculation of the losses in the switches (both conduction and switching losses) during the normal operation of the converters. The conduction and the switching losses of the switches are calculated according to (22) – (27). With this calculation of the losses, a comparison between the original and the new buck-boost topologies has been carried out. As can be seen Table 3, the losses (switching and conduction) using the original switching mode are high. However, the switching losses using the proposed dual carrier control scheme are almost equal compared to the original boost converters, while the conduction losses are higher as switches 1 and 5 are turned on during boost mode. In general, the total losses with the dual carrier scheme are similar to the original boost converter case.

Table 1. Parameters of the converters.

Parameter	Symbol	Value
Nominal Battery voltage	V_{Bat}	300 V
Nominal SM voltage	V_{SC}	96 V
Capacitance of the SM	C_{SC}	82.5 F
DC link voltage	V_{DC}	500 V
Capacitance of the DC link	C_{DC}	470 µF
Maximum load power	P_{L_max}	1666.7 W
Inductance of the inductors	L	21 mH
Resistance of the inductors	R	0.3 Ω

$$C(s) = K_p * (1 + \frac{K_i}{s}) \quad (21)$$

where:

- C(s) is the transfer function of the PI controller,
- K_p is the proportional gain,
- K_i is the integral gain.

Table 2. Parameters of the control of the converters.

Parameter	Symbol	Value
Voltage Control Loop		
Bandwidth	BW_v	30 Hz
Proportional gain	K_{P_V}	0.088548
Integral gain	K_{I_V}	7.09
Current Control Loop for LIB		
Bandwidth	BW_{LIB}	300 Hz
Proportional gain	K_{P_LIB}	39.564
Integral gain	K_{I_LIB}	22.8571
Current Control Loop for SM		
Bandwidth	BW_{SM}	500 Hz
Proportional gain	K_{P_SM}	65.94
Integral gain	K_{I_SM}	22.8571
Cut off frequency of LPF	f_{LPF}	8 Hz

$$P_{avg.cond.} = P_{avg.cond.IGBT} + P_{avg.cond.Diode} \quad (22)$$

$$P_{avg.Cond.IGBT} = \frac{1}{T}\int_0^T [V_{ce}(t) * I_c(t)]\, dt \quad (23)$$

$$P_{avg.cond.Diode} = \frac{1}{T}\int_0^T [V_D(t) * I_c(t)]\, dt \quad (24)$$

where:

- $P_{avg.cond.}$ is the average conduction losses of the switch in Watts,
- $P_{avg.cond.IGBT}$ is the average conduction losses of the IGBT in Watts,
- $P_{avg.cond.Diode}$ is the average conduction losses of the anti-parallel diode in Watts,
- T is the switching time in Secs,
- V_{ce} is the on-state collector emitter voltage of the IGBT in Volts,
- I_c is the on-state collector current of the IGBT in Amps,
- V_D is on-state forward voltage of the anti-parallel diode in Volts.

$$P_{sw.} = P_{sw.IGBT} + P_{rec.Diode} \quad (25)$$

$$P_{sw.IGBT} = (E_{on} + E_{off}) * f_{sw} \quad (26)$$

$$P_{rec.Diode} = E_{rec.} * f_{sw} \quad (27)$$

where:

- $P_{sw.}$ is the switching losses of the switch in Watts,
- $P_{sw.IGBT}$ is the switching losses of the IGBT in Watts,
- $P_{rec.Diode}$ is the reverse recovery losses of the anti-parallel diode in Watts,

- E_{on} is the energy loss at IGBT turn on in Joules,
- E_{off} is the energy loss at IGBT turn off in Joules,
- f_{sw} is the switching frequency in Hz,
- $E_{rec.}$ is the energy loss of the reverse recovery of the antiparallel diode in Joules.

Table 3. The Losses in the topologies.

Topology	Conduction Losses (W)	Switching Losses (W)	Total losses (W)
Boost	10.67 W	49.93 W	60.61 W
Buck-Boost (original switching mode)	29.7 W	96 W	125.7 W
Buck-Boost (proposed 2 control modes)	22.2 W	49.93 W	72.13 W

Fig. 9 shows the operation of both the boost and the buck-boost with the dual carrier scheme solutions, under healthy conditions. The figure shows that these two solutions give the same performance during transient load steps. The LIB controls the DC link around 500V, while the SM delivers and absorbs the transient power required during the load steps (From 833.3 W to 1666.7 W and again to 833.3W) to avoid DC link voltage variation during the transients. This yields a fast recovery of the DC link voltage and a decrease in the power ratings and the stresses (including current ripple) in the battery.

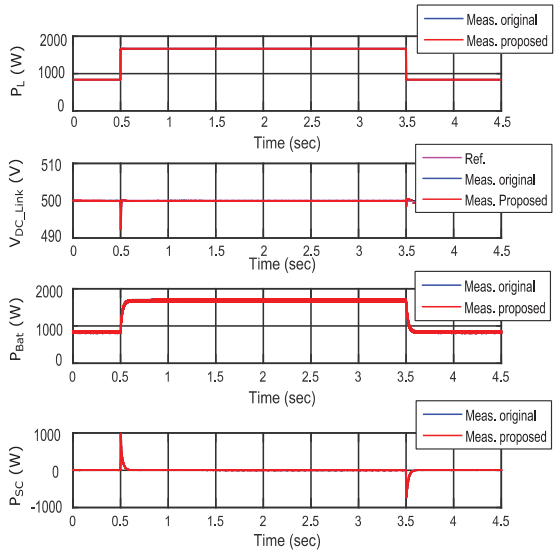

Fig. 9. Simulation results during normal operation for the original topology and the proposed one where the load power (P_L) is changed from 833.3 W to 1666.7 W and then to 833.3 W again.

The fault ride through capability of the buck-boost converter with the proposed dual-carrier control is shown in Fig. 10. The converters are operating under normal control, however when a DC link fault is detected at 0.5 sec (the DC link voltage below 15V threshold), the converters will operate under fault control. In fault control mode, a 4A reference current is applied to the LIB, while the SM leg is disconnected. When the fault is removed at 2.5 sec, this reference will charge the DC link to a specific value (500V threshold in this case). Then, the system is automatically reset to the normal control. The DC link will continue charging with a ramp until the DC link reference voltage value and the converter operate in normal mode.

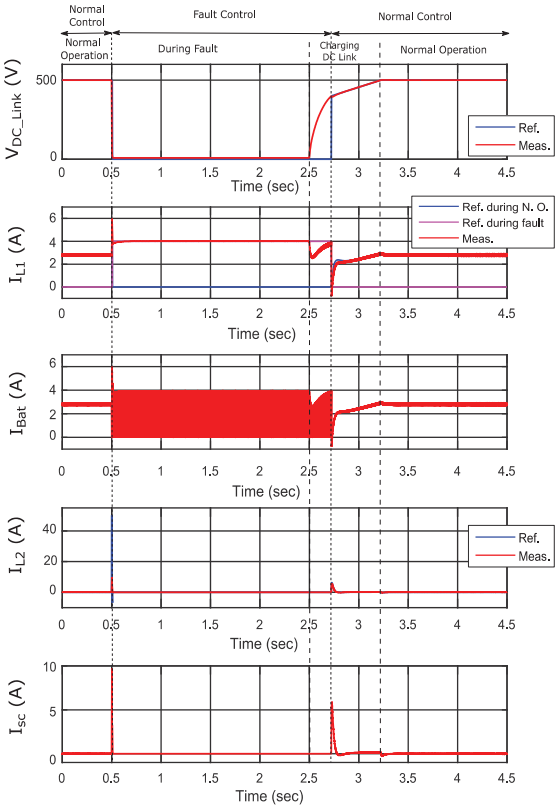

Fig. 10. Simulation results during fault and normal operation with the proposed control, the fault occurred at 0.5 sec and cleared at 2.5 sec.

V. Validation of the System by Experimental Results

The proposed control with the proposed topology are validated and tested using experimental setup as shown in Fig. 11. Fig. 12 shows the normal operation of the two parallel bidirectional boost converters and the two parallel bidirectional buck-boost converters. The load is changed at 0.5 sec from

833.3 W to 1666.7 W and at 3.6 sec is changed again to 833.3W. Fig. 12 fully matches with the simulation results in Fig. 9. Fig. 13 show the operation of the buck-boost converter with the proposed control during the normal operation and fault operation and again fully matches with Fig. 10 from simulations. The fault is occurred at 0.5 sec and is cleared at 2.5 sec.

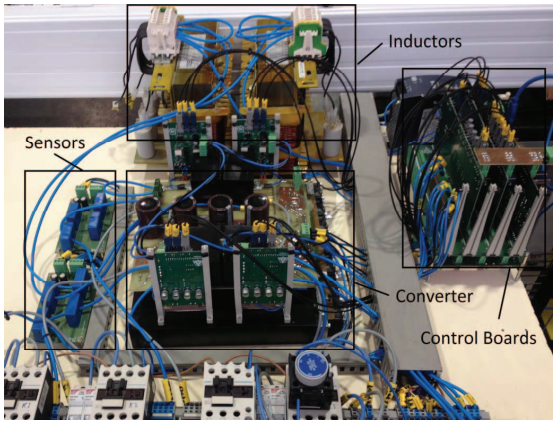

Fig. 11. Experimental setup of four legs of IGBTs and can be connected to be boost converter or buck-boost converter.

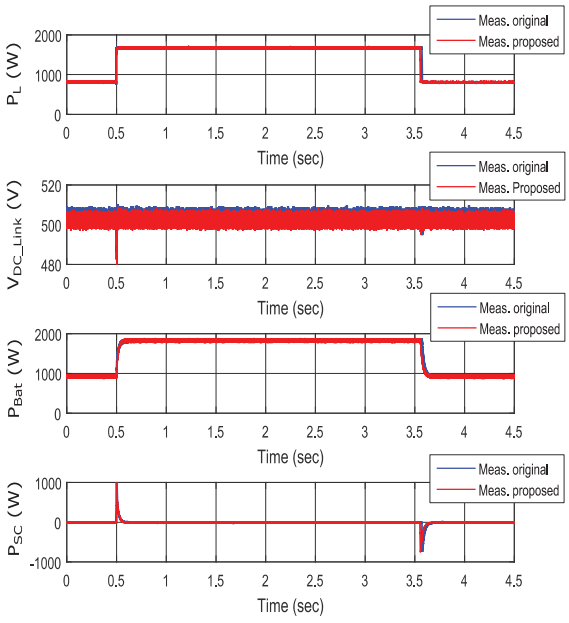

Fig. 12. Experimental results during normal operation for the original topology and the proposed one where the load power (P_L) is changed from 833.3 W to 1666.7 W and then to 833.3 W again.

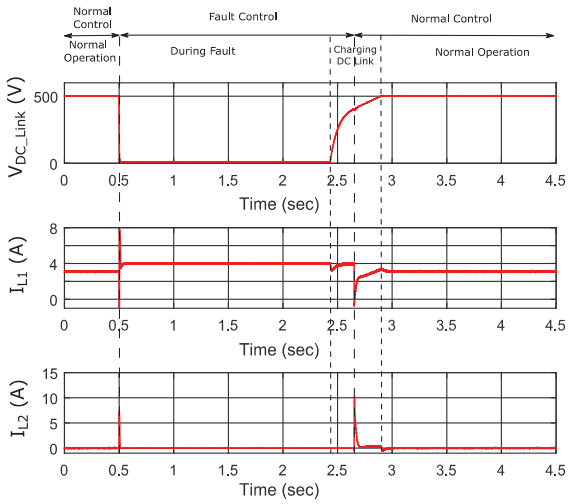

Fig. 13. Experimental results during fault and normal operation with the proposed control, the fault occurred at 0.5 sec and cleared at 2.4 sec.

VI. Conclusions and Future Developments

In this paper, a DC link short-circuit fault-tolerant, fault ride-through control scheme for a non-isolated topology for Hybrid Energy Storage Systems has been presented, analyzed and verified through simulations and validated by experiments. This configuration has a higher component count than the bidirectional boost version which is the simplest topology able to provide hybrid performance. However, it has been stated that the inclusion of the fault-tolerant, fault-ride through capability does not significantly increase the power losses in the switches. The proposed configuration, with the two control modes using two carrier signals can operate in buck or boost mode, making this scheme useful for different applications.

Acknowledgment

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C.5 Publication V

R. Georgious, J. Garcia, A. Navarro, S. Saeed and P. Garcia, "Series-Parallel Connection of Low-Voltage sources for integration of galvanically isolated Energy Storage Systems," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 3508-3513.

Series-Parallel Connection of Low-Voltage Sources for Integration of Galvanically Isolated Energy Storage Systems

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***Abstract*—This work explores the Series-Parallel Connection of a Low Voltage Supercapacitor Module to obtain a Hybrid Energy Storage System for grid support applications. The Hybrid System is formed by the Supercapacitor Module itself, intended to ensure fast performance upon peak power requirements, together with a battery that provides the energy requirements. In the full system, the front end converter and the load interfacing converter share a common DC link. The battery is connected to the DC link by means of a Full-Bridge Current-Source bidirectional DC-DC converter. The Supercapacitor Module is connected to the system using a Series-Parallel Configuration, which overcomes the main problems that arise with the most common topologies found in the literature. The full operation of the system has been demonstrated theoretically and by simulations. A demonstration of such connection is shown experimentally, in a converter operating at reduced power levels, in order to validate the feasibility of the system. Conclusions show how this scheme can be used in Hybrid Storage Systems.**

Keywords— Energy Storage Systems, Battery, Supercapacitor, Hybrid Storage Systems, Power Electronic Converters

I. INTRODUCTION

The increasing penetration of distributed generation and Energy Storage Systems (ESS) into the distribution grid is boosting the growth of Microgrids and Smartgrids [1]-[4]. The system under consideration is shown in Fig. 1, in which a Front-End Converter (FEC) connects a given load (which can be generalized as a Microgrid) to the three-phase distribution line. The main ESS, formed by the battery and a Main Storage Converter, is intended to support the DC link voltage in case of load variations or line fluctuations. In this work, the Full-Bridge Current-Source (FBCS) converter, shown in Fig. 2, has been selected as a suitable topology. This main ESS and its associated converter might have limitations in the power rating and bandwidth (due reliability, expected operating life or efficiency constraints). These limitations might affect the transient behavior of the storage system. Upon a power demand from the load, the power will initially be given by the DC link capacitor, which in turn will be discharged. It will take some time, depending on the design, for the ESS to be able to provide the required power to the DC link. This voltage drift might cause problems in the performance of the full system.

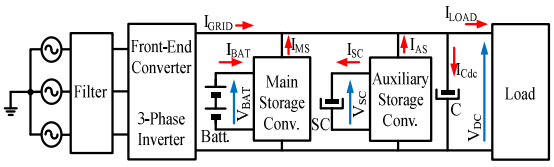

Fig. 1. Block Diagram of the system under consideration (Front-End Converter with ESS).

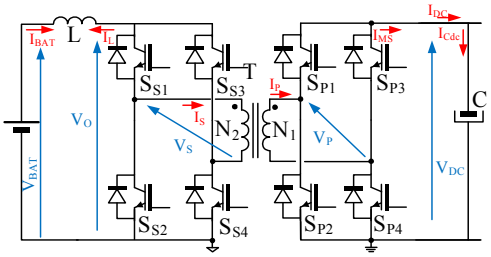

Fig. 2. Full Bridge Current Source (FBCS) converter for interfacing of a DC-link and a battery.

The most current solution is to add in parallel an additional auxiliary storage system, in order to form a Hybrid Energy Storage System (HESS), able to supplement the needed transient power requirements with a very fast dynamics [5]-[11]. This paper is focused on proposing an alternative for this application, based on a Supercapacitor (SC) module, connected to the DC link and the main ESS through a Series Parallel Connection (SPC), shown in Fig. 3 (shaded).

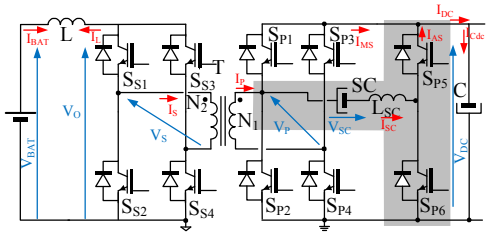

Fig. 3. Full Bridge Current Source (FBCS) converter with SPC connection of Supercapacitor Bank.

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II. The Main Energy Storage System

The Main Energy Storage System is connected to the DC link by means of a DC to DC bidirectional Converter. Among the most used isolated topologies, the Double Active Bridge (DAB) converter outstands as a mature, well-known and versatile solution. It provides possibility of soft commutations within some operation margins, and high power density, plus overall good performance. The main flaws of this converter come from the loss of performance at low power levels, and the high current harmonics in the input and output current waveforms [refs required]. In order to avoid such harmonics to flow though the output port (in this case the ESS), in this work, the Current Source version of the DAB has been selected.

The FBCS converter depicted in Fig. 2 is formed by a Full-Bridge structure (switches SP1 to SP4), connected to the primary side of a transformer [12]-[13]. At the secondary side, another Full-Bridge (switches SS1 to SS4) interfaces with a filter inductor, L in series with the battery itself. Unlike in a standard Voltage-Source Double Active Bridge (VSDAB), this inductor operates with high DC current values and relatively small ripples, yielding to a current source behavior in the battery side. This also yields to a more compact design of the inductor, as the AC magnetic field is smaller. This inductor is therefore filtering the current to the battery, thus increasing the system reliability. In addition, the current control through this inductor is also the battery current control, which simplifies the control design.

The switching scheme is depicted in Fig. 4.a, along with the main waveforms of the FBCS converter in steady state. The only control parameter is the duty ratio D that defines the modulation pattern. Fig. 4.b shows simulations of the FBCS operation. Fig. 5.a outlines the control scheme used for the full system. In order to compare the results, the performance of the FEC dynamics has been made equal in both cases (with and without battery). The current reference for the battery is calculated from the actual load step, as shown in Fig. 5.b.

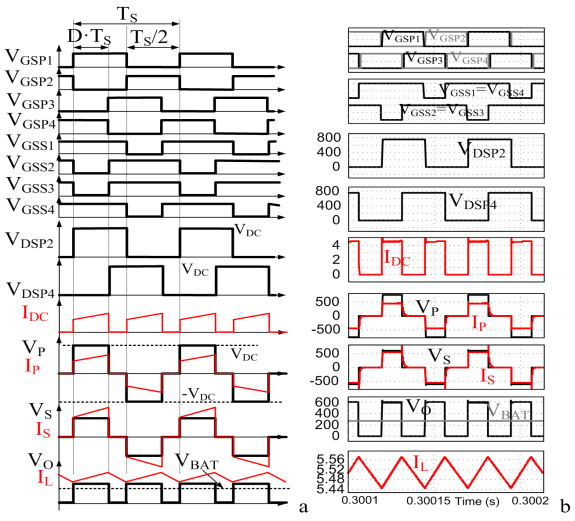

Fig. 4. Main theoretical (a) and simulated (b) waveforms of FBCS operation in steady state

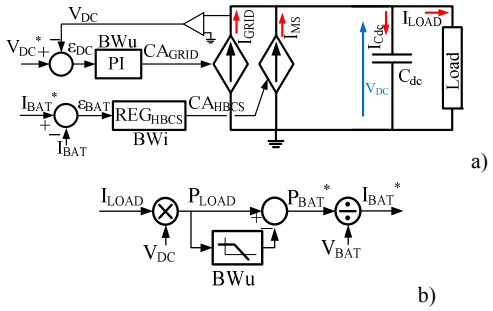

Fig. 5.a) Control scheme for main ESS alone. b) Generation of reference for battery current

Fig. 6 and Fig. 7 depicts the performance of this initial system, without and with the main ESS, for a load step of 1 kW, in a 700 VDC link voltage system. It can be seen how the DC voltage drift is substantially smaller in the system with the main ESS. The rest of the operating parameters are shown in Table I. A closer look to Fig. 7 shows a high di/dt in the initial response after the load step. This might yield to battery operating life shortening, etc. In order to solve this issue, a SC module can be placed in the system, to cope with such transient efforts.

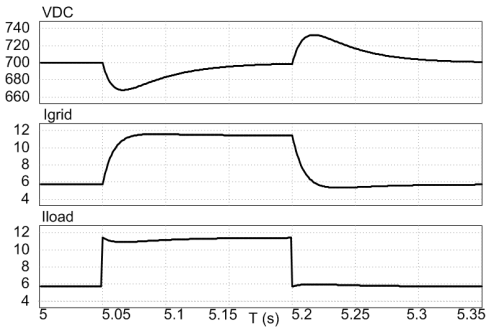

Fig. 6. Simulated waveforms without the main ESS, upon 1kW load step up and down.

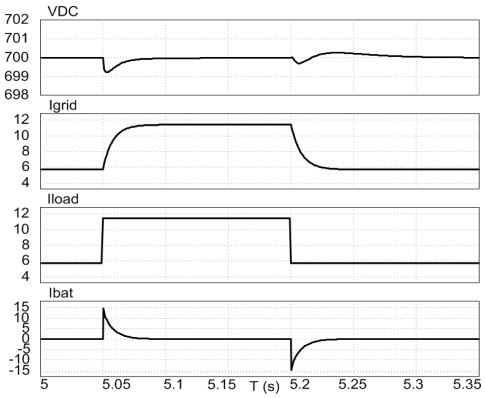

Fig. 7. Simulated waveforms with the main ESS, upon 1kW load step up and down.

TABLE I. PARAMETERS OF THE SIMULATED SYSTEM.

Parameter	Value
DC link ratings	700 VDC
Bandwidth of DC link Control	20 Hz.
Nominal Power (FEC)	10 kW
Battery Nominal Voltage	300 V
Bandwidth of Battery Current Loop	1 kHz.
Load Step	1 kW

III. THE PROPOSED INTEGRATION OF SUPERCAPACITOR

One option for this integration would be the use of a Solid State Transformer (SST), with an additional port for the supercapacitor bank [14]-[15]. This is especially suitable for this application, given the high mismatch voltage ratings among the three ports, which can be solved by selecting the proper turns-ratio of the transformer. However, this would provide high stresses in the transformer, as it must therefore be defined for high currents to avoid saturation during the transients. This work explores the integration of the SC module as an auxiliary leg in the primary side of the converter through SPC, different from the series connection presented in [16], as depicted in Fig. 3.

Ahead is a summary of the principle of operation of the SPC. The simplest connection of the HESS to manage the power flow from and into the storage devices is the Parallel Connection, shown in Fig. 8, based on a dedicated bidirectional boost converter connected to a DC link [17]-[24].

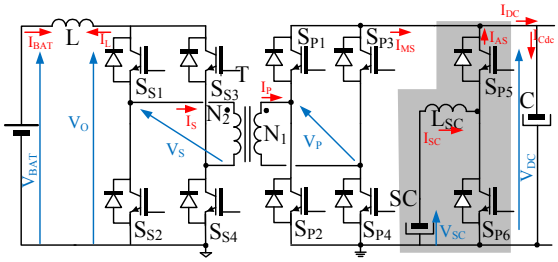

Fig. 8. Full Bridge Current Source (FBCS) converter with direct parallel connection of Supercapacitor Bank.

The main limitations of this connection come from the high voltage mismatch between the supercapacitor voltage ratings and the fixed DC bus voltage. Considering a battery nominal voltage of around half the DC link, then the duty ratio of the battery leg will be around 50%, which optimizes the converter performance, in terms of stresses, design complexity and control capability. However, provided that in some applications the supercapacitor nominal voltage ratings are ranged from 20V to 40V, then for DC bus voltage ratings ranged from 500V to 900V the required gain for the converter might reach values of 40:1 and higher. Such requirements prevent the use of such topology. To overcome this drawback, the Series-Parallel Connection of the supercapacitor modules (Fig. 3) can be carried out. The gain required for the supercapacitor module leg of the converter results in a much more reasonable value than before. Indeed, the drawback of the voltage mismatch at the bidirectional boost configuration is solved, as the average voltage at the midpoint of the supercapacitor module leg results in the addition of the supercapacitors plus the battery voltages. Assuming that the supercapacitor ratings are much smaller than the battery ones, this leg operates with a duty ratio similar to the battery leg. In addition, if the switching pulses are adequately synchronized, the current ripples in the converter might decrease.

Considering steady state, and given that the average voltage at the midpoint of the leg formed by switches S_{P1} and S_{P2} at the primary side equals $V_{DC}/2$, then the average voltage value at the midpoint of the SPC leg (Switches S_{P5} and S_{P6}) will be equal to $(V_{DC}/2)+V_{SC}$, as the average value of the SC inductor voltage is zero. This means that the duty ratio of S_{P5}, D_{SC}, can be calculated as follows:

$$D_{SC} = \frac{V_{SC}+\frac{V_{DC}}{2}}{V_{DC}} \quad (1)$$

Yielding to a value close to 50%, which allows for the operation of this leg with a high gain between the SC module and the DC link, but within the most adequate values for the duty ratio (current and voltage stresses matched, high control margin).

IV. RESULTS AND VALIDATION OF THE PROPOSED SCHEME

Fig. 9 shows theoretical and simulated waveforms of the FBCS converter with the SPC scheme. As it can be seen, the DC current is now the addition of the current given by the main ESS (I_{MS}, from the battery) plus the current given by the Auxiliary ESS (I_{AS}, from the SC module). Fig. 10 shows the control scheme implemented for the control of the converter. As it can be seen, the error of the battery current loop is the parameter that will provide the reference for the supercapacitor current. Fig. 11 shows the performance of the HESS. It can be seen how the main operating parameters are pretty close to the simple battery ones depicted in Fig. 7. However, now the current that the battery is providing has a much slower di/dt, given the peak power is supplied initially by the SC.

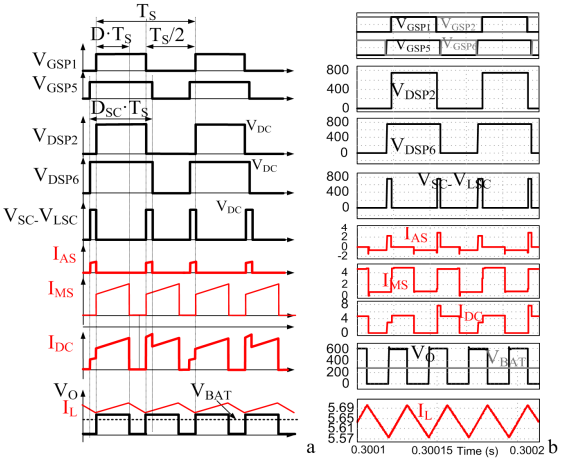

Fig. 9. Main theoretical (a) and simulated (b) waveforms of FBCS operation in steady state with SPC of Supercapacitors.

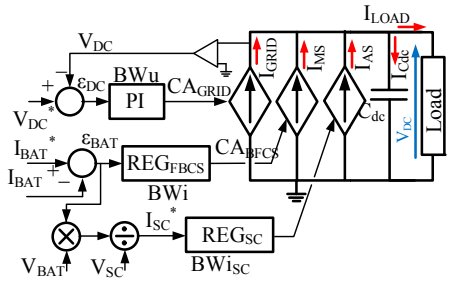

Fig. 10. Control scheme for main and auxiliary ESSs.

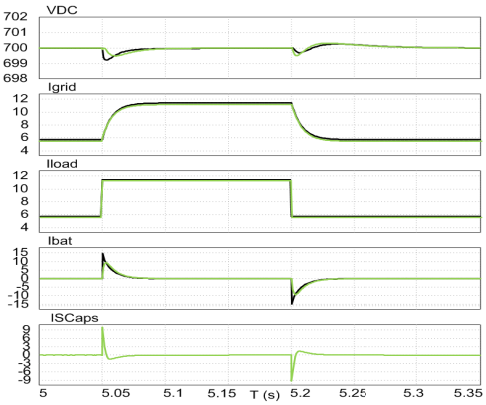

Fig. 11. Simulated waveforms of main ESS alone (black) vs SPC of Supercapacitor, SC, (green), upon 1kW load step up and down.

In order to demonstrate the feasibility of the system, several experimental tests have been carried out in two demonstrator. The first demonstrator consists of a 1kW, 600V_{DC} system, with a supercapacitor bank voltage of 30V_{DC}. Fig. 12 shows the captured data of the SPC scheme operating in steady state. As it can be seen, the leg of the SC (CH7) operates with a duty ratio close to the battery leg (CH6), for 30 V_{DC} and 300 V_{DC} operating voltages, respectively, for a DC link of around 600V.

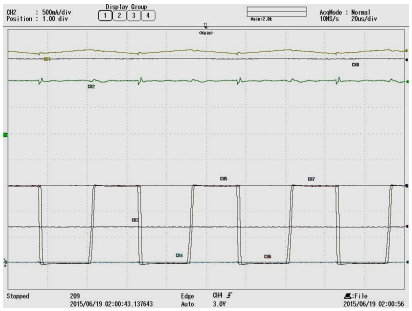

Fig 12. SPC operation of a demonstrator converter. CH1 (yellow): I_{BAT}, 1A/div. CH2 (green): I_{SCaps}, 0.5A/div. CH3 (magenta): V_{BAT}, 200V/div. CH4(cyan): V_{SC}, 50V/div. CH5 (red): V_{DC} , 200V/div, CH6(orange): u_{DSP1}, 200V/div. CH7 (blue): u_{DSP5}, 200V/div. CH8(violet): I_{LOAD},1AV/div. Time: 10us/div

The control system performance has been validated in a scaled prototype, with 200/300V_{DC} in the DC link, around 200V in the battery, 20 kHz switching frequency, and 30 V_{DC} in the supercapacitor bank. The main parameters of the scaled demonstrator are depicted in Table II

TABLE II. PARAMETERS OF THE EXPERIMENTAL SYSTEM.

Parameter	Value
DC link ratings	200/300 V_{DC}
Bandwidth of DC link Control	10 Hz.
Nominal Power (FEC)	1 kW
Battery Nominal Voltage	200 V
Supercaps	20 V
Bandwidth of Supercaps Current Loop	1 kHz.
Load Step	400 W

Fig. 13. shows the performance of a load step in the 300 V_{DC} DC link, and the 10 Hz dynamics of the grid converter. The first trace shows the DC link variation due this load current step (fourth trace), and a voltage ripple of around 10 V can be appreciated.

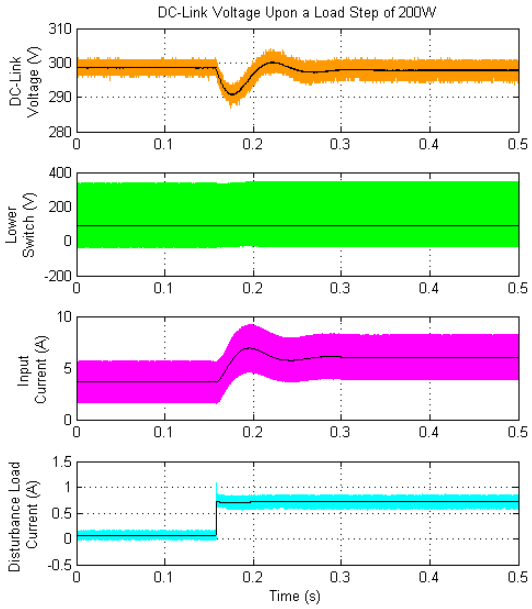

Fig 13. Load step in the DC link, without the supercapacitor module.

Fig. 14. shows the steady state operation of the battery charge, for a 1A charging current reference. The approximately 90º degrees phase shift in the primary side legs of the converter can be seen. Also, the battery current and the battery voltage itself are depicted. The V_{DC} link is in this case equal to 200 V_{DC}.

Fig. 15 shows the operation of the supercapacitor bank under SPC connection, again for 200 V_{DC} link voltage. A current step reference is provided, and the implemented control loop with a bandwidth of 1kHz is shown. As it can be seen, the system is able to track the reference within the desired 1 kHz bandwidth.

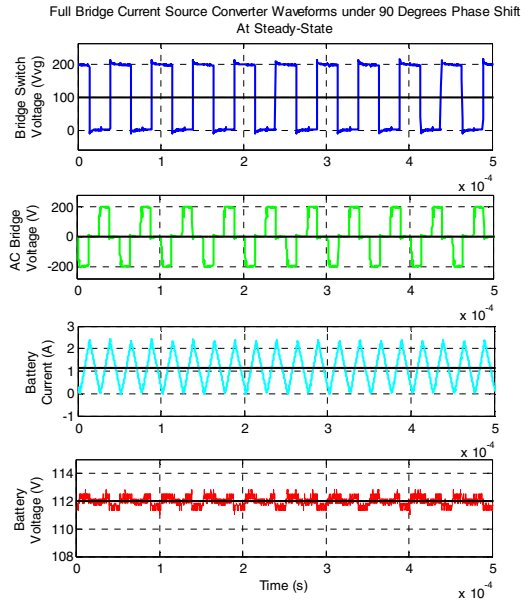

Fig 14. FBCS Converter. Traces (from upper to lower): Voltage in one of the bridge legs (blue); voltage in the primary of the transformer (green); battery current (blue), Battery voltage (red).

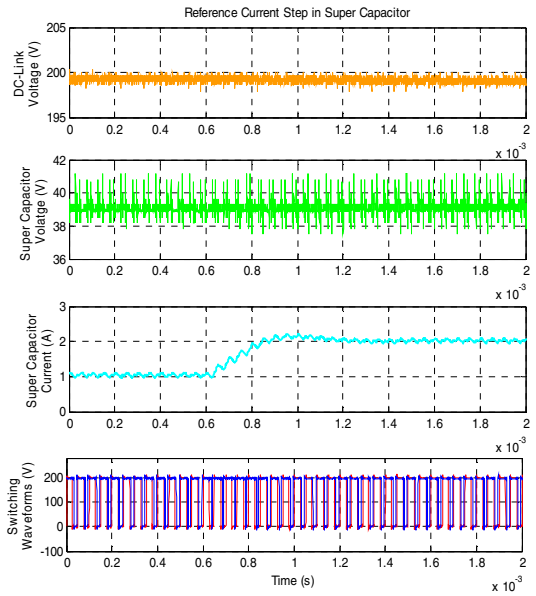

Fig 15. Supercapacitor reference current step. Traces (from upper to lower): DC link voltage (red), Supercaps voltage (green), supercaps current (blue), voltage at both legs of the inverter (lower plot).

V. Conclusion

This work has demonstrated theoretically and through simulations the feasibility of the SPC of a Low Voltage SC Module for interfacing with an ESS formed by a DC link and a Battery connected through the FBCS converter. The main features of this Hybrid System include operation of the system with a high voltage mismatch from the supercaps module to the DC link. It also shows the easy control scheme, design and tuning (fully decoupled control parameters for the main and the auxiliary ESSs). Theoretically this scheme provides higher efficiency than other isolated connections (as the SC energy does not need to flow though the transformer). These characteristics allow this solution to be considered for Hybrid Systems of medium voltage and power ratings.

Acknowledgment

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C.6 Publication VI

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Hybridization of Energy Storage Systems for Electric Transportation by Means of Bidirectional Power Electronic Converters

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Abstract–This paper deals with the design of a Hybrid Energy Storage System (HESSs) for electric transportation such as Electric/Hybrid Vessel and Electric/Hybrid Train. The association of more than one Energy Storage Systems (ESSs) e.g., batteries which have different dynamics permit to take the advantages of the characteristics of both ESSs obtaining simultaneously a high energy density and high power density. This yields to a decrease in terms of the size of the main ESS and the total cost and an increase in terms of life span. The emulation of the batteries and with required control algorithm for the HESS are proposed. The design and the control of the HESSs is validated with the simulation in MATLAB/SIMULINK® environment and also with the real-time emulation of batteries in a laboratory setup of a HESS. The real-time experimental results have been validated against PC simulations showing full consistency. The setup of the hardware of HESS can be used to test any technologies of batteries, being a low cost solution for testing and benchmarking.

Keywords–Energy Storage Systems, Hybrid Energy Storage Systems, Bidirectional Boost Converter, Electrical Transportation.

I. INTRODUCTION

The main purpose of Energy Storage Systems (ESSs) in applications such as electric transportation as well as microgrids or smart grids is to provide a temporary energy buffer between electrical power generators and loads or to provide a permanent energy to the loads in case of islanding mode [1]. These ESS, together with Power Electronic Converters (PECs) and required control algorithms provide the needed power flow versatility in the system. In the case of electrical transportation such as electric vehicles, electric vessel, electric train, etc., the power flow changes very fast depending on the operation mode of motors, generators and ESSs [2].

Hybrid ESS (HESS) provide a solution to obtain a joint enhanced performance of the global ESS with respect to the individual ESS constrained due each individual storage technology. On the other hand in applications of power system related to electric transportation (Electrical Charging Station, Vehicle to Grid (V2G), Power System Operation), the main purpose of ESS is to increase the power quality of the grid in case of line contingencies such as voltage transients, current distortions, phase unbalances, load fluctuations, islanding modes, etc [3]. Unfortunately, as mentioned previously, most current ESS ratings do not allow simultaneously a large energy capability and a fast response. This yields to the need for hybridization of at least two technologies of ESS with different characteristics, one with a high energy density and slow dynamics and other with a high power density and fast dynamics [3-8].

II. DESIGN SPECIFICATIONS

The system designed will be more suitable for Electric/Hybrid vessel and Electric/Hybrid train. It has the following operating conditions: Lithium Ion Battery (LIB) is selected for high power and Fast Dynamics ESS (FDESS) and Vanadium Redox Flow Battery (VRFB) is selected for high energy and Slow Dynamics ESS (SDESS). The control of VRFB is mainly to maintain the DC bus voltage constant and the control of the LIB is to provide or absorb transient power during load variations. This yields to a decrease in the power ratings of the main ESS (VRFB in this design).

The interface of both ESS is carried out by means of bidirectional boost converter as shown in Fig. 1. With this topology, the power flow of each storage device can be controlled independently thanks to the two DC/DC converters offering a high flexibility to manage the HESS [2], [9-16].

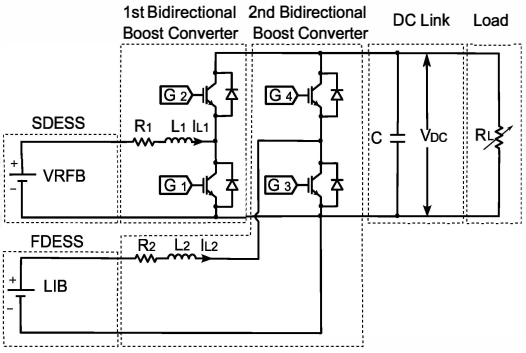

Fig. 1. The power circuit of the designed system.

III. DESIGN METHOD

The selection of the two batteries technologies was according to their advantages over other batteries technologies. The main advantages of VRFB are as following [4], [14-19]:

- It is an energy storage device which intended for energy rather than for power.
- Its storage efficiency is high as it can work for hours.
- It has a high scalability and is suitable for large scale storage applications because of electrolyte tanks.
- Instant recharge by electrolyte exchange.
- Long life cycle up to 10 000 charge/discharge cycles leads to lower through life costs.

- Low maintenance requirements because it uses pumps to circulate the electrolytes from the tanks to the cell.

Also, LIB has a lot of advantages as following [20], [21]:

- It is a power storage device compared to the VRFB.
- It has quick response than the VRFB.
- It operates through a wide range of temperatures and it has high efficiency.
- Easy charge controllability and low self-discharge.
- Suitable for short term applications.
- No pollution compared to other battery technologies.

Table 1 shows the parameters of VRFB and LIB used in the designed HESS system.

Table 1: Parameters of VRFB and LIB

VRFB		LIB	
Parameters	Values	Parameters	Values
E	50 KWh	E	13.2 KWh
P	25 KW	P	15 KW
$V_{nominal}$	302.4 V	$V_{nominal}$	311.6 V
V_{min}	150 V	V_{min}	252 V
I_{max}	166.7 A	I_{max}	50 A
Operating region	20-80%	Operating region	20-80%
No. of cells	230	No. of batteries	6

IV. EMULATION OF THE BATTERIES

Before Implementing the HESS with real batteries, which might be expensive, the control can be validated through the emulation of the batteries. Several options can be used to obtain the behavior of batteries.

- The first option is a real time simulation [14], however the equipment associated with this solution is very expensive.
- The second option consists on the emulation of the batteries by hardware construction by their equivalent circuit, nevertheless, if the battery parameters are changed, the hardware components should be modified as well.
- The third option is the emulation of the battery dynamics through real-time software running on a Digital Signal Processing (DSP) to get the virtual battery voltage. This last has the lowest cost and is the one analyzed in this paper.

1. Software part

The dynamic behavior of any battery can be modeled, among other options, by a simple circuit [1], [22], consisting of a series resistor (Rse) standing for the internal resistance of the battery, a capacitor (C_{SOC}) representing the state of charge (SOC) and a parallel capacitor (C_D) with a parallel resistance (R_D) representing the dynamics of the battery as shown in Fig. 2.

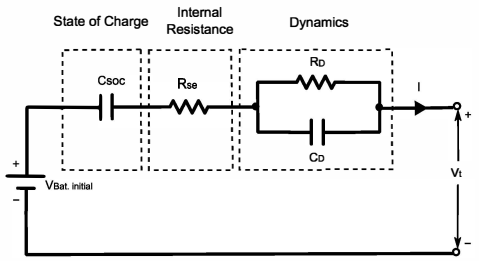

Fig. 2. Dynamic behavior equivalent circuit of any battery.

After some algebraic manipulations, the transfer function of the dynamic equivalent circuit is expressed as following:

$$G(s) = \frac{V_t(s) - V_{Bat.\ init.}}{I(s)} = -\frac{R_s s^2 + \left(\frac{1}{C_{SOC}} + \frac{R_{se}}{R_D C_D} + \frac{1}{C_D}\right)s + \frac{1}{R_D C_D C_{SOC}}}{s^2 + \frac{1}{R_D C_D} s} \quad (1)$$

where:

- $_t(s)$: is the terminal voltage of the equivalent circuit,
- (s) : is the current flowing in the equivalent circuit,
- $_{Bat.\ init}$: is the initial battery voltage,
- : is the Laplace transform.

The current is considered positive flowing out of the battery (Discharging mode), thus a negative sign appears in (1). The virtual voltage of the battery is calculated in (2) from the transfer function. Also, the initial conditions of the battery voltage are included in the virtual voltage. Equation (2) is implemented in the DSP to get the virtual battery voltage which presents the same dynamics as the real battery voltage. The parameters of the dynamic equivalents circuit of both batteries are shown in table 2.

$$V_{Bat.\ virtual}(s) = V_t(s) = V_{Bat.\ init.} + I(s) * G(s) \quad (2)$$

Table 2: Parameters of the dynamic equivalent circuits of VRFB and LIB

VRFB		LIB	
Parameters	Values	Parameters	Values
C_{SOC}	7594.9 Farads	C_{SOC}	0.0127 Farads
R_{se}	0.06826 Ohms	R_{se}	0.0628 Ohms
C_D	0.025 Farads	C_D	0.0127 Farads
R_D	0.0996 Ohms	R_D	0.1181 Ohms

2. Hardware part

To obtain the initial battery voltage in (2), a three phase uncontrolled rectifier as in Fig. 3. Capacitors are intended to decrease the ripples and smoothing the DC voltage. A charging resistance is used to initially charge the capacitor smoothly and then the bypass switch is closed. A blocking diode is used to prevent power return back to the three phase uncontrolled rectifier. A burning resistance is used to discharge the capacitor and in case of the power flowing from the DC bus through the bidirectional boost converter

to the three phase rectifier, the burning resistance will dissipate the power flowing back like in case of regenerative applicants. For this system, the two circuits of the FDESS and SDESS are similar, but with different initial voltage values.

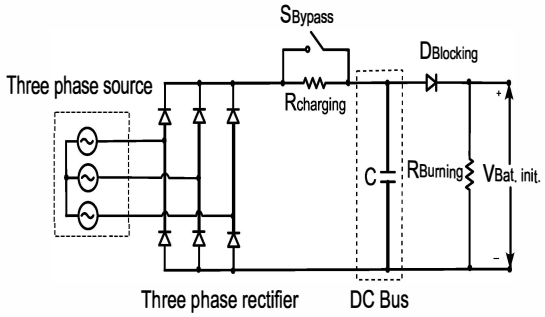

Fig. 3. Emulation of the battery to obtain the initial voltage of the battery and behaves as a battery.

V. CONTROL SCHEME OF THE CONVERTERS

As mentioned, the system consists of two bidirectional DC-DC boost converters. Each converter is connected to one battery and has its own control. One converter controls the DC link voltage to avoid stability problems, while the other converter delivers the peak transient power during load variations.

As discussed in the previous section, the virtual voltage of each battery will be calculated from (2) as in Fig. 4, however, each equivalent circuit has its own parameters. As the control of SDESS bidirectional boost converter is to maintain the DC link voltage constant. A typical cascaded control scheme is used, being the outer loop the DC link voltage control and the inner loop the inductor current control [6], [23]–[27] as shown in Fig. 5.

The control aim of the FDESS bidirectional boost converter is to provide the peak transient power when the load varies. This control will accelerate the recovery of the DC link voltage variations. Also cascaded control scheme is proposed, being the outer loop the power control and the inner loop the inductor current control as shown in Fig. 6.

The power reference is calculated by subtracting to the SDESS measured power its low frequency component by using a Low Pass Filter (LPF) to get the high frequency component.

To assure that the power of LIB is providing transient power during load variations, a PI controller is implemented. To increase the amount of power provided by the LIB, a gain K is multiplied by the power measured of the LIB. This means that more power will be released under sudden load variations, as the power error tends to increase the FDESS current reference. This will be helpful for the fast recovering of the DC link voltage. The value of the gain K goes from 0.1 to 1.0 and it depends on the maximum power of FDESS and the load variations. Table 3 shows the parameters of the control scheme of both converters.

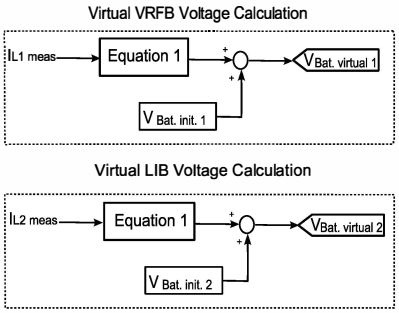

Fig. 4. Virtual voltage calculation for VRFB and LIB to get the battery dynamics.

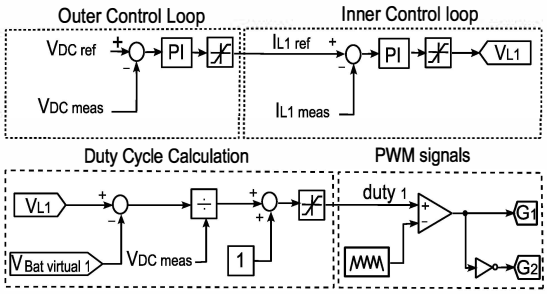

Fig. 5. SDESS converter control scheme to maintain the DC link voltage constant.

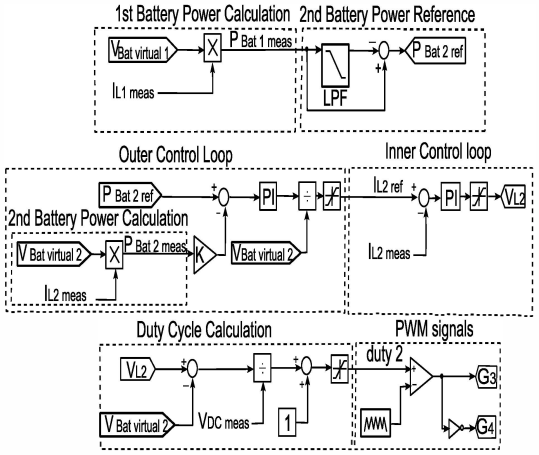

Fig. 6. FDESS converter control scheme to provide transient power during load variations.

Table 3: Parameters of the control scheme

Parameters	Values	Parameters	Values
$V_{VRFB\ init.}$	302.4 V	$V_{LIB\ init}$	311.6 V
SDESS converter control parameters			
$V_{DC\ ref}$	600 V	F_s	10 KHz
K_{pv}	0.19	K_{pi}	79.16
T_{iv}	0.3	T_{ii}	0.042
SDESS converter control parameters			
F_{LPF}	10 Hz	F_s	10 KHz
K_{pp}	1.56	K_{pi}	79.16
T_{ip}	1	T_{ii}	0.042

IV. Verification of the Designed System with Simulations

The simulations will consist on applying load variations upon the system once the demanded power has reached the steady state, with different values of gain K, using as a metric the DC link voltage variations.

A voltage reference of 600 V is used to validate the proposed control scheme for the designed HESS. The load is varied from 1.2 KW to 2.4 KW and again to 1.2 KW. The system is tested for two cases to check the effect of connecting LI-IB to VRFB.

- Case 1. Only VRFB is used, being connected to the DC link through the bidirectional boost converter.
- Case 2. Both VRFB and LI-IB are connected to the DC link by means of two bidirectional boost converters.

In Case 1, as shown in Fig. 7 that the DC link voltage drops 18 V when load varies from 1.2 KW to 2.4 KW and increases 19 V when load varies from 2.4 KW to 1.2 KW. These changes in the DC link voltage will increase if the load power is increased as the system designed for 25 KW.

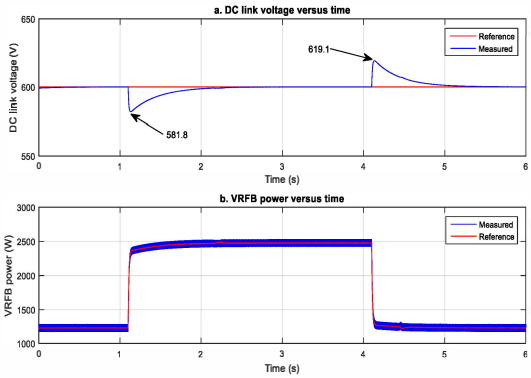

Fig. 7. Simulation Results at VRFB only: a) DC link voltage versus time b) VRFB power versus time.

In case 2, the gain K in Fig. 6 is changed to check the effect on the DC link voltage and the LI-IB current. As starting value, K = 1.0 is selected, the DC link voltage variations already exhibit a decrease, this is due to the power delivered by the LI-IB when load varied. By further decreasing K, the maximum voltage variations also improves, as it is shown in table 4, thus minimizing the effect of the load variations in the DC link voltage. The selected optimal value for K is 0.3 and the results are shown in Fig. 8.

Table 4: Simulation Results

	K	V_{DC_min} (V)	V_{DC_max} (V)	$P_{LIB\ max}$ (W)	$P_{LIB\ min}$ (W)
Case 1		581.9	619.1		
Case 2	1.0	587.9	612.7	465.8	-463.1
	0.7	588.5	612.2	531.3	-529.1
	0.5	588.8	611.2	581.8	-552.3
	0.3	589.9	610.4	655.7	-580.7

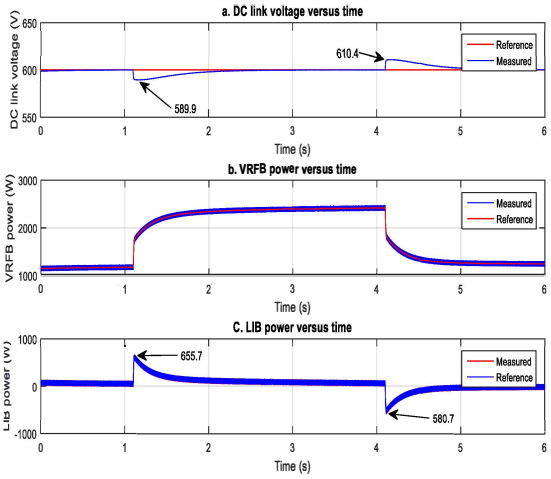

Fig. 8. Simulation Results when VRFB and LIB are connected at K = 0.3: a) DC link voltage versus time. b) VRFB power versus time. c) LIB power versus time.

VI. Verification of the Designed System with Experimental Setup

As it has been mentioned, the dynamic behavior of both the LDESS and FDESS will be implemented in real time software with parameters in Table 2, and the power will be absorbed or delivered to a dedicated DC bus. This scheme can be replicated for any ESS technology, provided that the dynamic behavior is known or can be calculated.

The experimental results in Fig. 9 and table 5 are to validate the emulation of the batteries and the proposed control scheme.

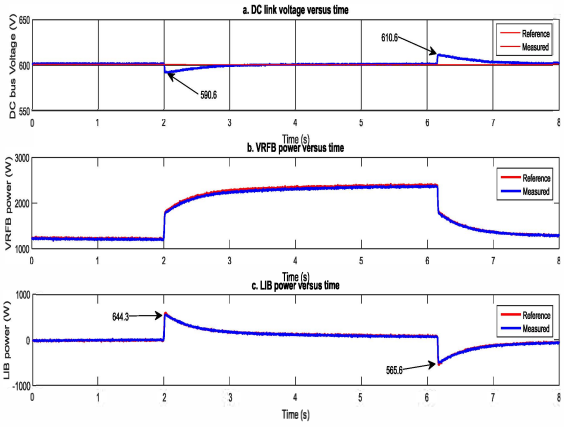

Fig. 9. Experimental Results when VRFB and LIB are connected at K = 0.3: a) DC link voltage versus time b. VRFB power versus time. c) LIB power versus time.

Table 5: Experimental Results

	K	V_{DC_min} (V)	V_{DC_max} (V)	$P_{LIB\ max}$ (W)	$P_{LIB\ min}$ (W)
Case 1		583	619		
Case 2	1.0	587.7	612.7	454.9	-442.5
	0.7	588.3	611.6	502	-503.2
	0.5	589.1	611.1	567.7	-523.8
	0.3	590.6	610.6	644.3	-565.6

V. Conclusion and Future Work

The designed HESS system for electric transportation decreases the total cost as there is no need to have a main ESS with a high energy density and a high power density simultaneously. Also it increases the life span of the main ESS.

The designed system with the proposed control scheme is validated by simulation and experiments. The simulation results are validated with the experimental results from emulation of the batteries. This emulation of batteries provide a low cost solution to test any technology of batteries and can validate any new control scheme before implementing HESS.

The technique used for emulation can be extended to different battery technologies, only requiring software changes. Further, the proposed control scheme can be used for any ESS technology such as supercapacitors, regular capacitors, etc.

Moreover, future developments of this work would include: increasing the number of ESS in the hybrid system and explore the applicability to other PEC topologies, such as isolated, multilevel, etc.

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