Analysis and Experimentation on a New High Power Factor Off-Line LED Driver Based on Interleaved Integrated Buck Flyback Converter

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***Abstract*— This paper presents a high power factor (PF), low total harmonic distortion (THD) light-emitting diode (LED) driver implemented by using an interleaved capacitor technique. Also, the driver presents dimming capability; in addition, the proposed technique ensures a high PF and low THD at all dimming range. An interleaved capacitor is placed between the rectifier and the integrated buck flyback converter (IBFC) operating in discontinuous conduction mode (DCM), in order to boost the conduction angle, and in return increase the PF and decrease the THD. Analyzing the operation of the proposed converter it is found that one diode of the conventional IBFC will not conduct and could be removed, which provides a reduction in the number of components. Furthermore the proposed technique offers a significant reduction in the output ripple of the converter, thus output capacitance reduction is achieved. The paper presents a prototype for the proposed converter supplying an LED luminaire of 37 V/ 0.67 A. The prototype shows a high PF equal to 0.997, very small THD of 2.5%, output current ripple of 6 %, and efficiency of 80 %.**

Keywords—current shaper; integrated buck-flyback converter; integrated converters; interleaved capacitor; LED drivers; power factor corrector; THD optimization

I. INTRODUCTION

Since 1960s when Light-emitting-diodes (LEDs) were first developed [1], they have been replacing little by little the conventional source of lighting, until they have become the most popular lighting source in a wide variety of applications. This has been owing to their longer lifetime as it is routinely quoted as 25,000 to 50,000 h, as declared by the LED manufacturers or standard organizations [2]-[4],as well as their higher efficacy compared to other source of lighting, as it is claimed by [5] that the incandescent lamps efficacy ranges between 14 to 17 lm/W, fluorescent tubes 100 lm/W, high pressure sodium reaches 120 lm/W; however the new generation of LED's will have an efficacy up to 250 lm/W even 300 lm/W as stated by [6]. In addition to its other features like its small size, fast response, robustness, reliability, and color rendering index [7]-[12]. However, LEDs cannot be connected directly to the mains, due to their low internal impedance, thus they have to be driven through a current controlled supply [1], [5], [13]-[15].

In order to assure the advantages offered by the LEDs, an electronic converter to drive the LEDs should be well designed to fulfill all standards. Working with a luminary load, fulfilling the IEC 61000-3-2 Class C [16] concerning the harmonic content in the input current became a must [17]. Also the PF has to be higher than the level specified by the U.S. Energy Star program [18] which is 0.9. The conventional drivers proposed to fulfill these standards are the two-stage LED drivers. The two-stage drivers are composed of a power-factor correction (PFC) stage and a constant-current-control dc/dc converter stage [19]. However, although two-stage converters show a significant good operation, it shows some drawbacks as well. The drawbacks are mainly expressed by its higher number of components, its lower efficiency and the fact that it contains two switches, which means two driver circuits, which means bigger size and higher cost. To overcome these obstacles many solutions were proposed, working in single stage and trying to fulfill the standards [20], or even keeping the two-stage but with new topologies that insure higher efficiency [21]. Also, a promising solution is the integrated converters, which are simply a two-stage converter but with a single switch, which means lower switching losses and only one driving circuit. Therefore, it keeps the good operation of the two-stage as well as offering some advantages of the single-stage converters [9],[10],[22]-[26].

In this work, the chosen converter is the Integrated Buck-Flyback converter (IBFC) shown in Fig. 1, owing to its high power factor operation, fast output regulation, low voltage at the Buck bus voltage, and the main switch handling less current. However, the IBFC shows a limitation in the PF and the THD, as well as the converter shows only good operation and full power, while with dimming the operation became worse. This paper presents a novel interleaved IBFC, by adding a capacitor between the Bridge and the converter. This will increase the conduction angle to reach theoretically 180º and in return a unity PF, and significant lower THD. The analysis proves that one diode of the conventional IBFC will not conduct anymore and could be removed, which means a reduction of number of components. The proposed technique insures an operation fulfilling the standards in all dimming ratio, as well as a lower ripple which means that a lower

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capacitance is needed. No extra switching devices are needed, as well as no need for any complex circuitry or any other extra sensors than the normal IBFC.

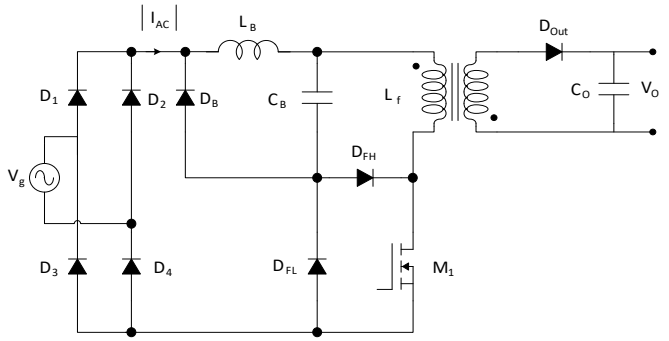

Fig. 1. Integrated Buck-Flyback Converter (IBFC).

This paper will be organized as following, in Section II the main drawbacks of the IBFC are illustrated and the interleaved IBFC will be illustrated. Section III shows the operational principles of the proposed interleaved IBFC, as well as the analysis, and an average model for the Interleaved IBFC. The design procedure will be illustrated in section IV. The experimental results are shown in section V. Last but not least, a brief conclusion for the contribution presented in the paper.

II. Derivation of the Interleaved IBFC

A. Conventional IBFC

The operation of the IBFC shown in Fig. 1, is equivalent to the operation of a Buck and Flyback converters working in cascaded mode. The flyback duty is to deliver the power to the output while the buck converter duty is to improve the input power factor, by pushing the Bulk voltage down as much as possible. Fig. 2 illustrates an explanation of how the voltage level of the bulk capacitor will fix the PF and THD. Knowing that buck converter will only conduct when the input voltage is higher than the output voltage. Thus, that creates a conduction angle as shown in Fig. 2 bottom plot, where a current is absorbed from the AC main. Therefore, decreasing the bulk voltage will increase the conduction angle, and in return the PF and THD will improve.

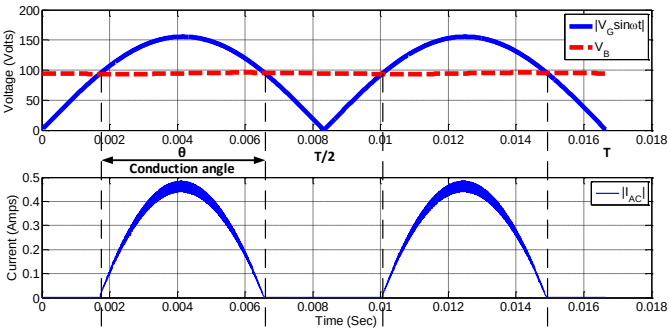

Fig. 2. Top: bridge voltage and bulk voltage. Bottom: current after the bridge.

Ideally speaking, the more the Bulk voltage is decreased, the more the PF and THD will improve. However, this is limited by two factors. First, if the voltage of the bulk capacitor is decreased, the voltage ratio between bulk voltage and line voltage will decrease, and in return the ripple of the bulk capacitor will increase [25]. Moreover, the increasing of the bulk voltage is done by increasing the buck inductance or by decreasing the magnetizing inductance of the flyback, and both options will be limited by the CCM limit.

In this type of converters, usually researchers investigate in order to find a trade-off between fulfilling standards, and the size and price.

B. Novel Interleaved IBFC

The interleaved IBFC shown in Fig. 3, solves all issues found in the conventional one. The idea simply is to add a third winding in the flyback transformer, with same polarity. This third winding goes to an interleaved capacitor, that connects the AC bridge to the Buck converter. There is a diode insuring the direction of the current going to the interleaved capacitor and not the reverse direction. The idea of the interleaved capacitor is previously proposed in [27], however it was used for improving the PF of a buck converter. The novelty here is that the PF will be theoretically equals to one, moreover it will operate with unity PF in all dimming ratio. As previously mentioned and shown in Fig. 2, the Buck converter only conducts when the input voltage is higher than the Bulk voltage. The presence of an interleaved capacitor makes a modification in the operation of the buck. In this case the Buck will conduct when the input voltage is higher than the Bulk voltage minus the interleaved voltage, as following;

$$v_L = v_{AC_{Bridge}} - (V_B - V_{int}) \quad (1)$$

Where; v_L is the voltage across the buck inductor, $v_{AC_{Bridge}}$ is the voltage at the bridge terminals, V_B is the bulk voltage, and V_{int} is the voltage of the interleaved capacitor.

As long as the turn ratio of the primary winding and the interleaved winding equals to 1:1, the interleaved voltage will be equal to the Bulk voltage. Therefore the Buck converter will conduct continuously, with a conduction angle of 180º.

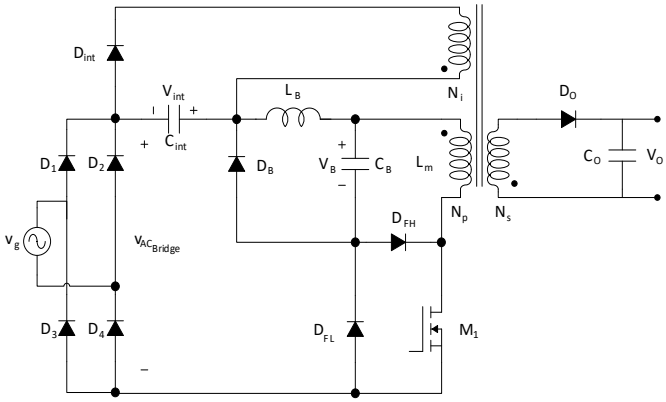

Fig. 3. Interleaved Integrated Buck-Flyback Converter schematic.

III. Operational Principles of the Proposed Interleaved IBFC

A. Operation Principle

Since the proposed converter is a single switch converter, there are only two states, on-state, and off-state. However, the DCM operation of the Buck and the Flyback splits the off-state into three intervals. Fig. 4, and Fig. 5 illustrate the equivalent circuits, and the main current waveforms within a high frequency switching period, respectively.

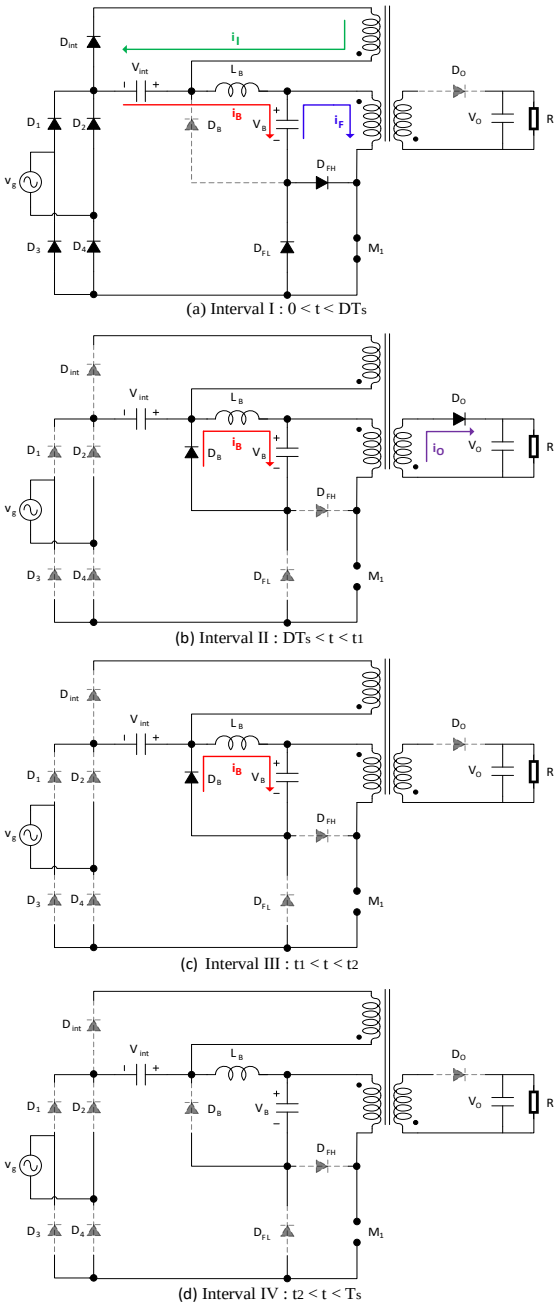

Fig. 4. Equivalent circuits of the Interleaved IBFC operating in DCM.

The principle of the operation is clear; however still there is missing information in the first interval, related to flyback current and the conduction principle of the two flyback diodes, D_{FH} and D_{FL}. Concerning the flyback current, as shown in Fig.6, a simple magnetic model for the transformer illustrated on it the flyback current and its parts. Related to the diodes, as shown in Fig. 7, the conduction will be determined according to the value of the flyback current and the buck current. As shown in Fig. 7 (a), if the flyback current i_F is higher than the Buck current i_B, then D_{FL} will conduct of the difference between the two currents, while D_{FH} will not conduct. In the case of the i_B is higher than i_f shown in Fig. 7 (b), the reverse will occur, D_{FH} will conduct of the difference between the two currents, while D_{FL} will not conduct.

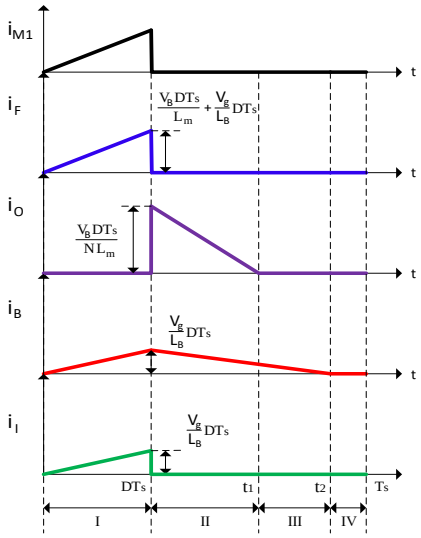

Fig. 5. Main currents waveforms of the Interleaved IBFC operating in DCM, within a high frequency switching period around the peak line voltage.

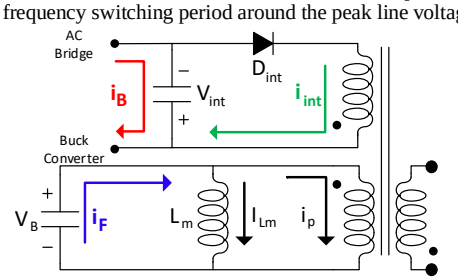

Fig. 6. A simple magnetic model for the flyback transformer, and the current in it during turn on.

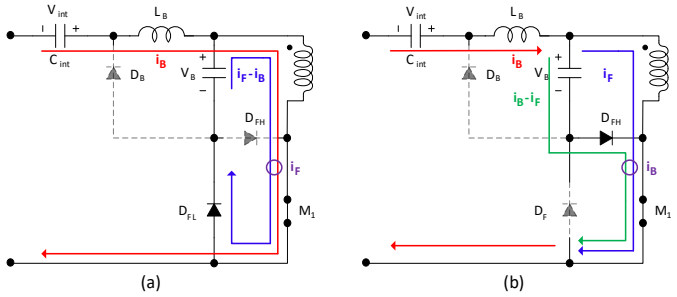

Fig. 7. Conduction operation of the flyback diodes. (a) if $i_F > i_B$, (b) if $i_B > i_F$.

Other advantage shown by the interleaved IBFC is the ripple reduction. As shown in Fig. 8 a comparison between the ripple of the conventional IBFC and the proposed technique for the output voltage and current. For a better comparison the values of capacitors used in the two converters are the same, and as shown the ripple reduced a lot in the proposed interleaved IBFC. The voltage ripple is 5 % for the IBFC and 1 % for the Interleaved IBFC, while the current ripple is 25 % for the IBFC and 5 % for the interleaved. For this application an output current ripple of 6 % is required, thus a significate big output capacitor of 100 µF is required to keep the ripple below 6 %. However, for getting this value of ripple using the conventional IBFC, the capacitance value should be at least 820 µF, which means an eight times bigger capacitor. The reason beyond the reduction of the low frequency ripple is the unbroken conduction of the interleaved IBFC. In other words, the small conduction angle of the conventional IBFC create a period where the Buck converter is not conducting, however the power delivered to the output is continuous. This

phenomena increases the gap between the input power and the output power, which in return increases the ripple. This is not the case concerning the Interleaved IBFC as the converter is intended to have a conduction angle of 180º.

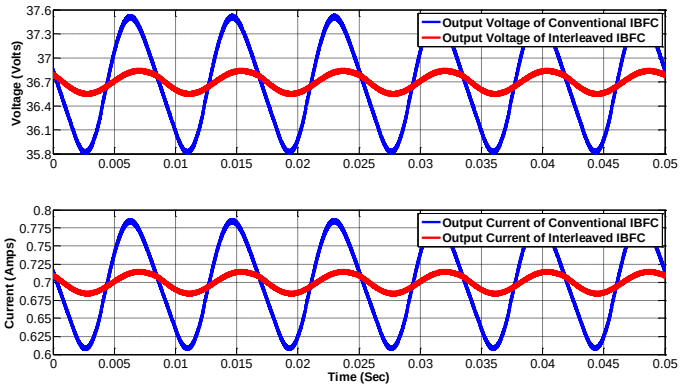

Fig. 8. output voltage (top) and currents (bottom)of the IBFC (in blue) and the Interleaved (in red).

B. *Mathematical Analysis*

In the following, the analysis of the currents in the converter, in order to obtain the important design characteristics, when both stages, Buck and Flyback operate in DCM is presented. For the sake of simplicity, the analysis will consider the converter in its ideal state. An ideally sinusoidal line voltage waveform will be considered, expressed as $v_g(t) = V_g \sin(2\pi f_l t)$.

In order to determine the operation of the two flyback diodes, D_{FL} and D_{FH}, the peak value of both buck and flyback currents have to be determined. Taking into account (1), and that V_{int} is selected to be equal V_B, the peak value of the interleaved buck current can be expressed as follows:

$$i_{B_{peak}} = \frac{D}{f_s L_B} v_{AC_{Bridge}} = \frac{DV_g}{f_s L_B} |\sin(2\pi f_l t)| \qquad (2)$$

Where, L_B is the buck inductance, f_s is the switching frequency, and D is the duty cycle.

Concerning the flyback current as in the proposed topology there is two secondary windings, it consists of two terms as shown in Fig. 6. The first term is the current that is stored in the magnetizing inductance and will be delivered to the output later during switching off, and it can be expressed as following;

$$I_{Lm_{peak}} = \frac{V_B D}{f_s L_m} \qquad (3)$$

Where, V_B is the bulk voltage, and L_m is the magnetizing inductance.

The second term of the flyback current is the current going to the interleaved capacitor. At steady state and ideally speaking, the power going the interleaved capacitor should be equal to the power extracted from it. Thus, the current going to the interleaved capacitor, should be equal to the current of the Buck converter in turn on. Therefore, the value of the second term of the flyback current can be expressed as following;

$$i_{p_{peak}} = \frac{N_i}{N_p} i_{int_{peak}} = n_i i_{B_{peak}} = \frac{n_i DV_g}{f_s L_B} |\sin(2\pi f_l t)| \qquad (4)$$

Where, N_i is the number of turns of interleave winding, N_p is the number of turns of primary, n_i is the turn ratio interleave to primary.

As this design is made in order to fix the interleaved voltage equal the bulk voltage, hence the turn ratio n_i is chosen to be 1. In returns the second term of the flyback current will be equal to the buck current, and the current of the flyback could be determined by the addition of (3) and (4) as following;

$$i_{F_{peak}} = \frac{V_B D}{f_s L_m} + \frac{DV_g}{f_s L_B} |\sin(2\pi f_l t)| \qquad (5)$$

In this way, the flyback current is continuously greater than the buck current. Thus, as aforementioned the D_{FH} will not conduct anymore and could be removed, as it conducts only if the buck current is higher. Summarizing, the proposed interleaved technique insures a flyback current greater than the buck current and in return D_{FH} is eliminated.

Regarding the operation of the converter, a full DCM has to be insured. Hence, a study for the boundaries is made in order to be able to choose the reactive elements. As the Buck converter is operated in DCM, the input stage will behave as a resistance for the line. However, an interleaved capacitor is used, the resistance value of the Buck converter is not affected and it could be expressed as following;

$$R_g = \frac{2L_B f_s}{D^2} \qquad (6)$$

Therefore, the value of the average line current can be calculated as following;

$$\langle i_g \rangle = \frac{v_g}{R_g} = \frac{D^2 V_g}{2L_B f_s} \sin(2\pi f_l t) \qquad (7)$$

The mean input power can then be calculated taking into consideration that both voltage and current waveforms will be sinusoidal, as following;

$$P_g = \frac{1}{2} V_g \langle i_g \rangle_{peak} = \frac{1}{2} V_g \frac{D^2 V_g}{2L_B f_s} = \frac{D^2 V_g^2}{4L_B f_s} \qquad (8)$$

Concerning, the flyback power delivered to the output, it can be expressed as following;

$$P_F = V_B \langle i_{Lm} \rangle = V_B \left(\tfrac{1}{2} I_{Lm_{peak}} D \right) \qquad (9)$$

Substituting (3) in (9), the following expression for the power of the flyback delivered to the output is found;

$$P_F = \frac{D^2 V_B^2}{2L_m f_s} \qquad (10)$$

Concerning, the output power it can be found using the equivalent resistance of the LED, as following;

$$P_{Out} = \frac{V_O^2}{R} \qquad (11)$$

Where, V_O is the output voltage, and R is the equivalent resistance of the LED load.

Ideally, the input power will be equal to the output power and equal the output power. Therefore, by equaling the three equations of the power a relation between the input voltage and the bulk voltage can be found, as well as a relation between the bulk voltage and the output voltage, respectively in (12), and (13);

$$\frac{V_g}{V_B} = \sqrt{\frac{2L_B}{L_m}} \tag{12}$$

$$\frac{V_O}{V_B} = D\sqrt{\frac{R}{2f_s L_m}} \tag{13}$$

The equations of the powers (8), and (10) are the two operation constrains. However, still to insure full DCM mode of operation more constrains has to be added, which are the boundaries of the DCM operation. Therefore t_1 shown in Fig. 5, has to be lower than the switching frequency period for a flyback DCM operation, as well as t_2 for a buck DCM operation. The procedure to find those two parameters, is to determine two expression for the peak current one in terms of the duty and the other one in terms of whether t_1 for the flyback or t_2 for the buck. The flyback current expression in terms of duty is found in (3), and can be found also as following;

$$I_{Lm_{peak}} = \frac{N_s}{N_p} I_{O\ Peak} = n_s \frac{V_O}{L_m}(t_1 - DT_s) \tag{14}$$

Where, N_s is the number of turns of primary winding, n_s is turn ratio secondary to primary, and T_s is the switching frequency period.

Matching (3), and (14) the following expression for t_1 is found;

$$t_1 = DT_s\left(\frac{V_B}{n_s V_O} + 1\right) \tag{15}$$

Likewise for t_2, the peak value of the buck current is found in terms of duty in (2), and also could be found as following;

$$I_{B_{peak}} = \frac{V_B}{L_B}(t_2 - DT_s) \tag{16}$$

Matching (2), and (16) the following expression for t_2 is found;

$$t_2 = DT_s\left(\frac{v_g}{V_B} + 1\right) \tag{17}$$

C. Average Model

For better illustration of the operation of the converter, an average model is defined as shown in Fig. 9. The average model is useful in terms of understanding the power-flow in the converter. As well as it is a faster way to check the magnitude of the voltages and currents in all parts without the high frequency effect.

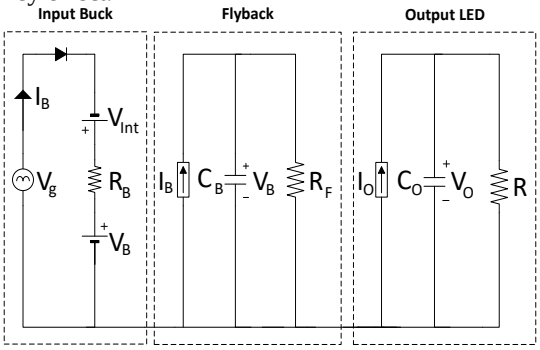

Fig. 9. Average model of the Interleaved Buck Flyback converter.

Using the average model with the previously driven equations, the relation between the bulk voltage and the inductor peak current with respect to the buck inductance is made, and shown in Fig. 10. The figure is drawn using the parameters shown in Table.1 and a switching frequency of 40 kHz and output power of 25.9 W. It is clear that the voltage as well as the peak buck inductor current are decreasing as if the buck inductance is increasing. However, this is in DCM but after CCM the behavior changes, at first increases then decreases in small deviations. Besides, that increasing the inductance after the CCM is ineffective, the operation as well as the PF and THD will be worse. Therefore the chosen buck inductance will be 900 µH.

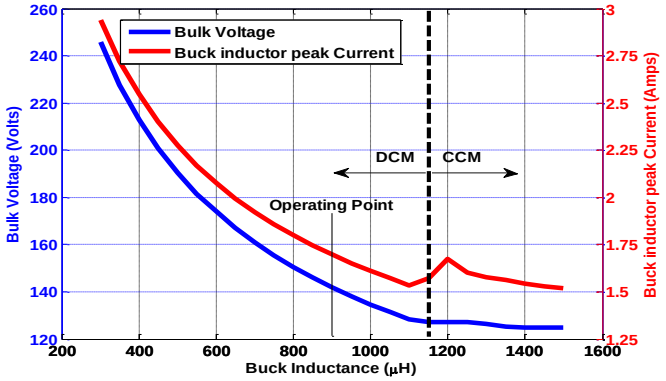

Fig. 10. Bulk voltage and inductor peak current with respect to the buck inductance.

IV. Design Procedure of the Laboratory Prototype

A. Power

Using the previously determined equations and the average model illustrated in Fig. 9, a design is made to supply an LED luminaire of 37 V/ 0.67 A, resulting in 25.9 W of output power. The line voltage is 110 V_{rms} and line frequency is 60 Hz. Seeking for better efficiency the converter is tested to work under quasi-resonant technique. The quasi-resonant technique shows a better efficiency as it reduces the switching losses, however the technique shows a drawback which is that the switching frequency is not fixed. On the other hand the value of the magnetizing inductance could fix the switching frequency to be around a given value.

A desired operation switching frequency is to be around 40 kHz, and to insure this operation the magnetizing inductance will be chosen to fix t_1 to be equal 80% of the switching period. This will insure that the switching frequency will be around the 40 kHz.

Concerning the buck inductance value it will be designed to optimize the operation of the converter. As shown in Fig. 10, this will occur at the boundary operating point between the DCM and CCM in order to decrease the bulk voltage and the inductor current as much as possible together with the best operation of PF and THD insured by the DCM. Accordingly, t_2 have to be equal to the switching period at the input peak voltage. However, this is ideally, so a margin of 20% is taken, in order to insure a DCM operation in practical implementation, that's why as shown in Fig. 10, the operating point is before the ideal margin of DCM and CCM.

Applying this constrains to equations (15), and (17) of t_1 and t_2 consecutively, the values of the buck inductance and the

magnetizing inductance additionally to the turns ratio are found. Table. 1, shows the parameters of the components driven for the laboratory prototype to supply the previously mentioned luminary.

TABLE I
COMPONENTS OF LABORATORY PROTOTYPE

Component	Value
Input Filter Inductor	*2.58 mH*
Input Filter Capacitor	*68 nF*
Buck Inductance	*ER2510/PC44,* $L_B = 900\ \mu H$, N = 60
Flyback Transformer	*PQ2625/3C90,* $L_m = 1.5\ mH$, $N_p = 25\ T$, $N_s = 6\ T$, $N_i = 25\ T$
Bulk Capacitor	47 µF, 250 V
Auxiliary Capacitor	100 nF, 250 V
Output Capacitor	100 µF, 50 V
M_1	SPA07N60C3
Bridge Diodes	DB156S
D_B & D_{FL}& D_{AUX}	MURS260T3G
D_{OUT}	STPS3150

B. Control

The quasi-resonant technique has been previously presented with the Flyback converter and shows an improvement in the efficiency of the flyback [28]-[30]. The quasi-resonant technique simply is to switch on the switch at the valley value of the voltage across the switch, so that the switching losses are decreased. The same technique will be used here as well with the interleaved IBFC. The IC used for the control is the Primary-Side LED driver controller RT7306 [31]. The controller IC shows great advantages; such as implementing the quasi-resonant technique, a constant output current regulation, compatible with dimming. Furthermore, the IC shows a great advantage which is a primary-side control, so controlling the output current by sensing the peak value of the flyback switch current. However, the interleaved IBFC affect this control technique, as the current through the switch will be the addition of the flyback current going to the output, and the current going to the interleaved capacitor. Solving this issue by sensing the current in the diode D_{FL}, knowing from the analysis that the current of this diode will be the current in the switch subtracted from it the interleaved current. Thus, it will conduct the flyback current going to the output, and behave same as the switch in normal flyback converter. An additional issue appears which is the direction of the current, though to solve this as well the place of the ground is replaced to be before the sensing resistance in order to give a positive signal to the control IC. Fig. 11 shows the detailed schematic diagram of the laboratory prototype, in both aspects power and control. Fig. 12, shows the prototype photography, and as shown the converter is very compact.

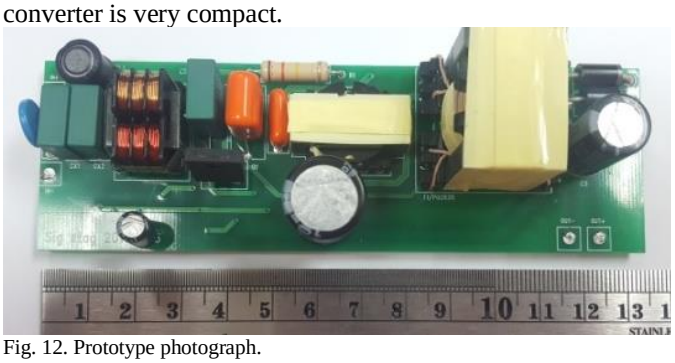

Fig. 12. Prototype photograph.

V. EXPERIMENTAL RESULTS

The line voltage and current waveform as well as the bulk voltage are shown in Fig. 13. As shown in Fig. 13, the current waveform is a pure sinusoidal waveform which illustrates that the proposed technique insures that the PF and the THD will be in their best conditions. Analyzing the input current waveform, the PF is equal 0.997 and the THD is equal 2.5%.

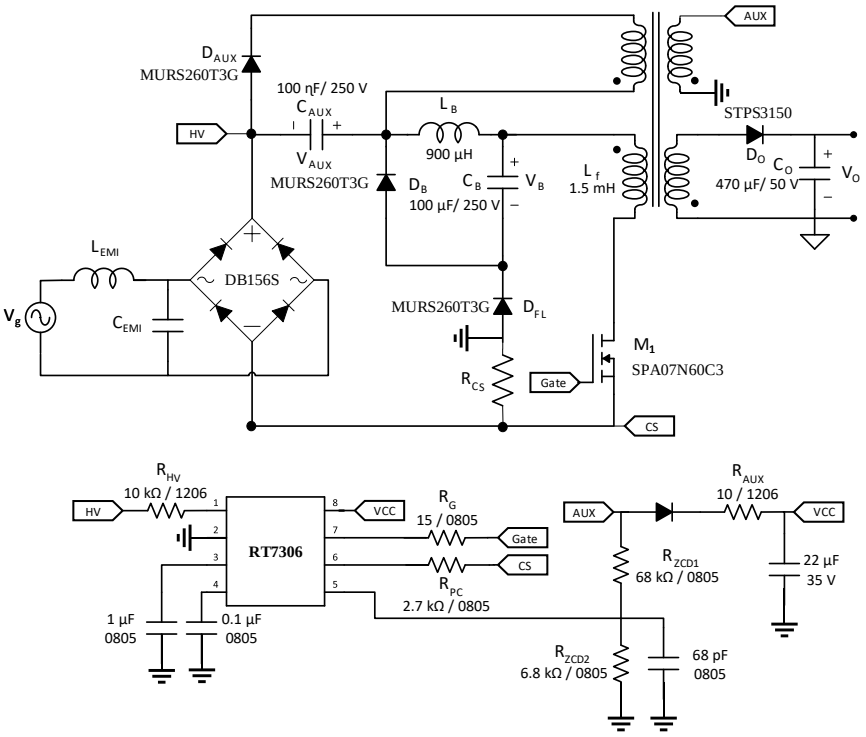

Fig. 11. Schematic diagram of the laboratory prototype.

The efficiency is found to be 80 %, and commenting on the result of the efficiency it is fair enough to justify that first this is a low power application 25 W, second it is a low voltage 37 V high current 0.7 A, and also the input voltage is 110 V so again low voltage.

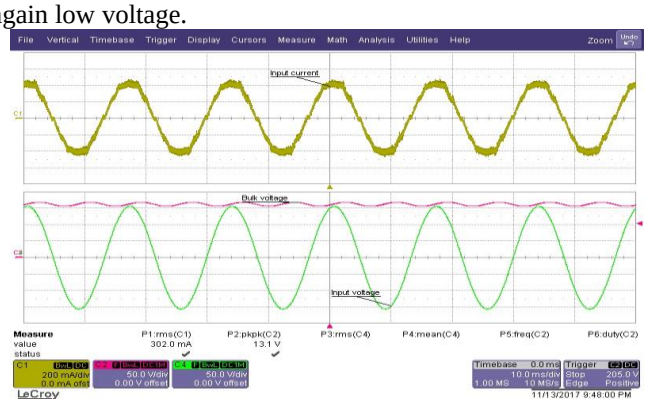

Fig. 13. Top: input current, and bottom: input sinusoidal voltage (green) and bulk voltage (red).

Fig. 14 shows the case of using the conventional IBFC, as shown, it is clear that the conduction angle is lower. However, the design of this converter was made in order to decrease the Bulk voltage as much as possible 85 V, further than this a CCM operation will occur. The PF in this case is 0.89 and the THD equal 23 % which is on the margin of the standards and for this application. Furthermore it couldn't be improved more with the conventional IBFC. Furthermore, as shown also in Fig. 14, the ripple voltage in the Bulk capacitor is too high reaching 30 %, which is not the case of the interleaved IBFC as it is found to be in the range of 8 % using the same capacitor ratings, as shown in Fig. 13.

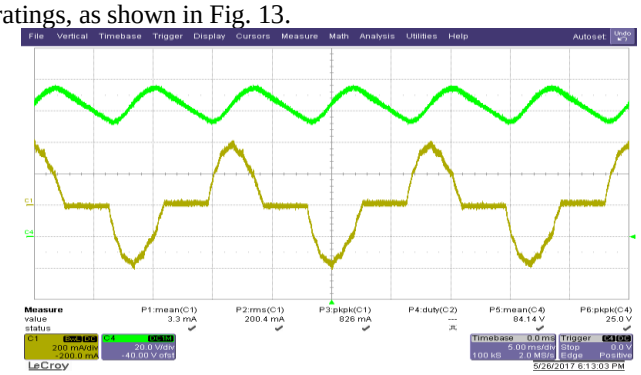

Fig. 14. Bottom: input current, and top: bulk voltage, for the conventional IBFC.

Fig. 15, shows the output voltage and current, it is clear that the control is perfectly working as the voltage and currents are fixed at the desired values 37 V and 0.67 A. Moreover, the converter shows a smooth and fast starting up process. The ripple in the voltage equals 2.2 V, while the ripple in the current equals 48 mA, knowing that most of these ripples are high frequency ripples.

Fig. 16, shows the switch voltage and the output Flyback current. As shown in Fig. 16, the quasi-resonant technique is perfectly implemented, as the switching-off occurs at the valley which is the lowest value for the voltage over the switch.

Fig. 17, shows the effect of the variation of the input voltage on the output current. The driver is tested for a variation of ± 20% of the rated input voltage. The driver shows an acceptable operation as the current is well controlled with just ± 4% of error. Fig. 18, shows the power factor with respect to the variation of dimming ratio. The practical results prove that the interleaved topology will insure a PF under standards for all dimming ratios, reaching a dimming ratio of 10%.

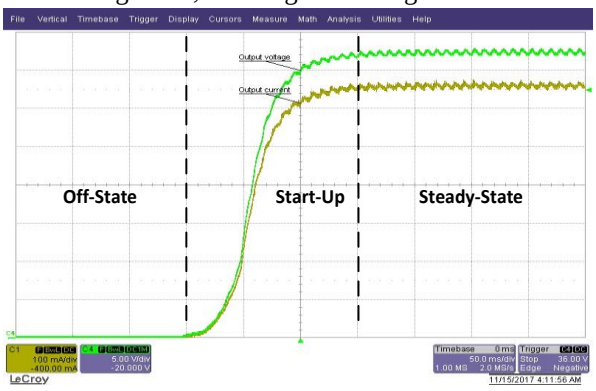

Fig. 15. Output current (yellow), and output voltage (green).

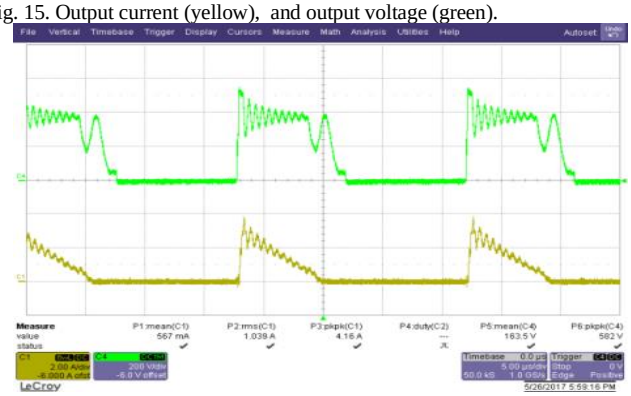

Fig. 16. Bottom: output flyback current, and top: voltage across the switch.

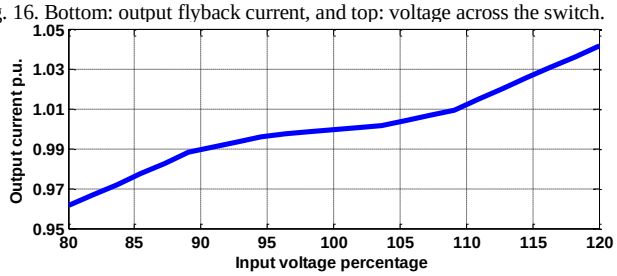

Fig. 17. Per unit output current with respect to the variation of input voltage.

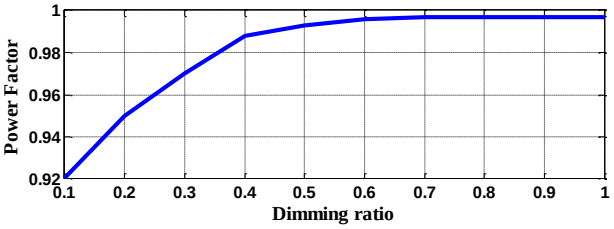

Fig. 18. Power factor with respect to dimming ratio.

CONCLUSION

The paper presents a new topology that enhances both PF and THD to be far below the limitation specified by the IEC 61000-3-2 standards. This is done by inserting an interleaved capacitor between the rectifier and the converter. The interleaved capacitor voltage is fixed by a third winding added to the Flyback transformer. The converter used for driving the LED is the IBFC double-stage converter. Furthermore, the proposed topology reduces the ripple by a factor of five which means a significant reduction for the output and bulk capacitor.

Last but not least, the proposed technique doesn't require any complex circuitry or any other extra sensors than the normal IBFC. The control technique is exactly the same used for controlling the IBFC. Regarding the power component, the proposed topology offers all these features by only adding an extra winding in the flyback transformer, and a capacitor of 100 nF. An extra diode is added, however the proposed technique insure that a diode of the conventional IBFC will not be conducting so it will be removed.

Finally, a prototype working at 110 V, 60 Hz, and 37 V output, driving a LED luminary of 25 W, has been designed to illustrate the application of the derived characteristics. Experimental results have proven that the harmonics content of the input current equals 2.5 %, and the power factor equals 0.997, so the converter meets the IEC-61000-3-2 standards for all dimming ratios, reaching a dimming ratio of 10%. The converter efficiency equals 80%, which is good considering the simplicity of the converter, the low power of the application, and also the good features offered by the converter.

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