

Optimization procedure of source/sink converters for DC power distribution nano-grids

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Abstract—DC-Power Distribution Systems require DC-DC converters to interface all their elements. These converters should provide a high power quality and be efficient, compact and inexpensive. Furthermore, the characteristics of the loads and sources connected to these converters are not known beforehand and may change widely (there is no regulation about the DC loads, such as IEC61000-3-2 in AC grids). As a consequence, the design procedure is neither standard nor obvious. This work proposes an optimized design procedure for any Bus Provider in a DC-Power Distribution System. It is based on models, hence extensible to different Bus-Provider topologies, and takes into account the main issues in DC-Power Distribution Systems, especially the design conditions imposed by the wide variety of loads, or even sources, which may be connected to the output bus. Experimental results obtained from three designs show a close match with the analytical models and verify that the proposed procedure minimizes converter losses and complies with the requirements.

Index Terms—dc-dc converters, design optimization, power distribution

I. INTRODUCTION

DC Power Distribution Systems (DC-PDSs) have become an increasingly popular alternative to traditional AC distribution in several applications such as telecom [1]–[4], transportation [4]–[6] and electrification of remote areas integrating Renewable Energy Sources (RES) and Energy Storage Systems (ESS) [7]. The main reasons for this technological change are the improved reliability, efficiency and power density that DC-PDSs provide at a lower cost than the traditional AC solutions [1], [8].

One of the main issues that arises during the planning of these DC-PDSs is the design of their power converters. They are required to interface the different elements which will be connected to the DC-PDS in an efficient and safe way while being compact and inexpensive [1]. These converters are also responsible for tightly regulating the voltage of their output buses where different loads or sources are connected. In many applications, these elements to be connected to the buses are totally undefined at the design stage of the DC-PDSs [8]–[10], making this process significantly more complex. Good

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examples of DC-PDSs with highly variable loads and sources are those for houses and occupied spaces, where the user could connect a vast variety of elements [1], [11].

Domestic DC-PDSs are commonly conceived as a multi-bus architecture, with different voltage levels [1], similar to the one shown in Fig. 1. A high-power Front-End Converter (FEC) is used as the interface between the utility and the high voltage DC distribution bus (380 V in Fig. 1). This general distribution bus is where the main RES, ESS and high-power loads such as high end computers, power tools, vacuum cleaners, kitchen appliances or electric vehicle chargers are connected. The low-voltage buses (24 V in Fig. 1, although different voltage levels have been proposed [1]) are obtained by means of bidirectional, isolated Bus Providers (iBPs). Internally, each of those iBPs consists of an isolated bidirectional Intermediate Bus Converter (iIBC) and several low-power non-isolated Bus Providers (niBPs). Every niBP provides an independent and regulated low voltage bus. Although this structure may change in several ways, it is a good example of what Emerge Alliance proposes [12].

The operating conditions of the iBPs (and consequently the iIBCs and the niBPs) will depend on how appliances are connected and used through the day. This adds a high degree of complexity to the design of the power converters that form part of the DC-PDSs. The power flow can vary greatly and even change direction and the dynamic behavior and the input impedance of the possible connected appliances may swing along a wide range.

In this paper a design procedure for the converters in any DC-PDS is proposed. The converter losses are minimized while ensuring that it complies with certain steady-state and dynamic requirements when the user connects different loads to its output. This procedure is independent from the converter topology and focuses on the wide range of loads that may be connected to them regarding power flow and dynamic behavior. It is conceived as a simple, automated procedure based on the desired magnetic core and MOSFETs and a small set of system level requirements.

The key design aspects are analyzed in Section II. In Section III, the design method is proposed and Section IV shows a design example with a synchronous buck converter. The experimental results from Section IV verify the proposed design procedure with three different prototypes. Finally, in Section V, some conclusions are drawn.

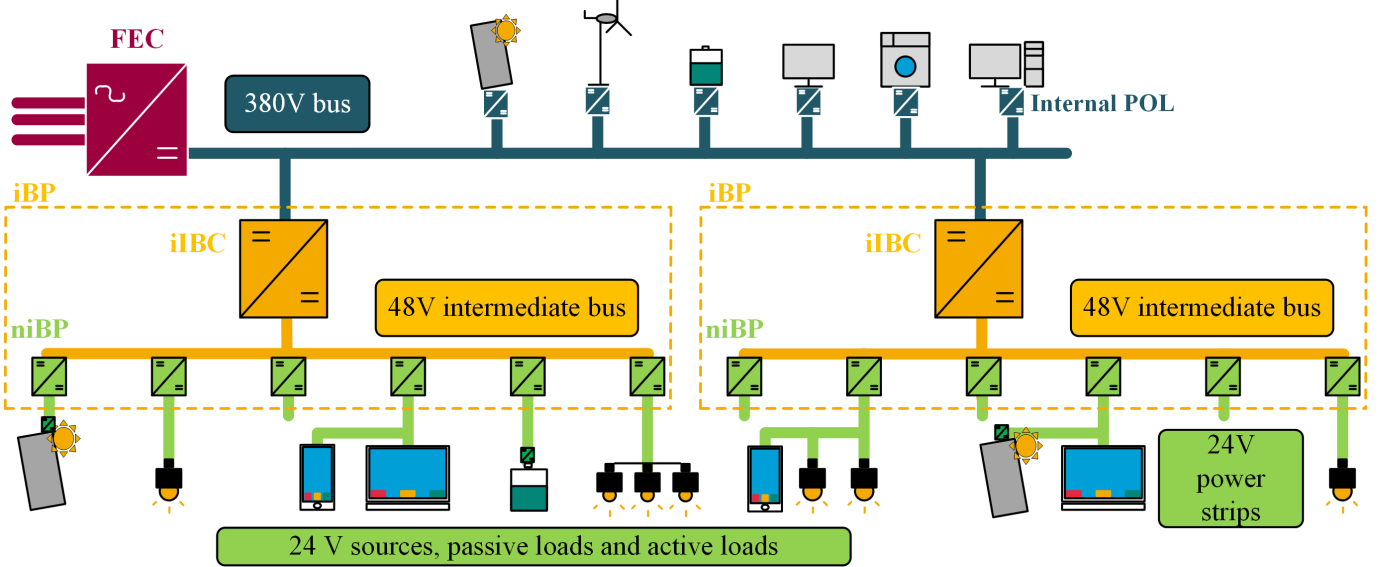


Fig. 1. Example of the proposed multibus architecture for domestic DC-PDS and the bidirectional iBP implementation based on Intermediate Bus Architecture.

II. CONVERTER DESIGN REQUIREMENTS IN A DC-PDS

No matter which topology is chosen to implement the iBP, there are some requirements that are imposed by the application. First, the loads and sources that the user can connect to the bus require a stable voltage level to operate properly. The iBP should be designed to provide a high level of power quality, which can be quantified by the voltage ripple or variation. It is important to ensure a low output voltage ripple (Δv_o), both during steady estate operation (Δv_{ot}) and load transients (Δv_{op}). Additionally, the elements connected to the output bus by the user will add external capacitive loads. The iBP should be able to remain stable and to maintain this regulation as long as the added capacitive load is under a certain limit C_e . This threshold should be dimensioned according to the bus voltage level and the maximum power delivered by each of the iBP outputs [13].

Previous works have defined design maps in order to ensure correct steady-state and transient operation for specific topologies [14], [15]. Based on a relatively large amount of design inputs, some of them being topology dependent, they provide an infinite amount of valid solutions for a single switching frequency. These maps, however, has several issues:

- They do not account for the existence of a capacitive load of up to C_e , which could significantly affect the stability of the control loop [16]. This can be easily solved analyzing the effects of the capacitive load on the plant of the chosen topology and control method and obtaining an additional lower limit on the value of the converter output capacitor (C).
- The switching frequency f_s is arbitrarily chosen by the designer based on experience and project requirements. The design map does not provide any information about the converter losses and can only give a rough estimation of its volume.

- Depending on the design inputs chosen by the designer, a map could have no valid designs for a given f_s .

Fig. 2 shows an example of the proposed design map for a synchronous buck converter, using voltage mode control and operating at a single, arbitrary f_s . This converter could be used as the niBP of the DC-PDS. The limits Δv_{op} and Δv_{ot} imposed on the output voltage by the power quality requirements set a lower bound for the buck output capacitor C . These minimum values $C(\Delta v_{op})$, that guarantees a maximum steady state Δv_{op} , and $C(\Delta v_{ot})$, which ensures a maximum Δv_{ot} during a load step of magnitude ΔI_o , can be calculated as in [14], [15].

Due to the chosen topology and control mode, two more limits are added to the map, defining the valid range of

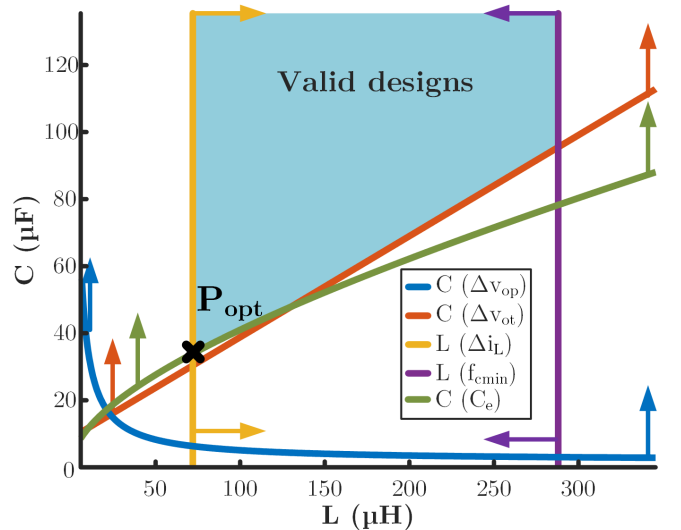


Fig. 2. Design map example for a buck converter output filter at a fixed switched frequency.

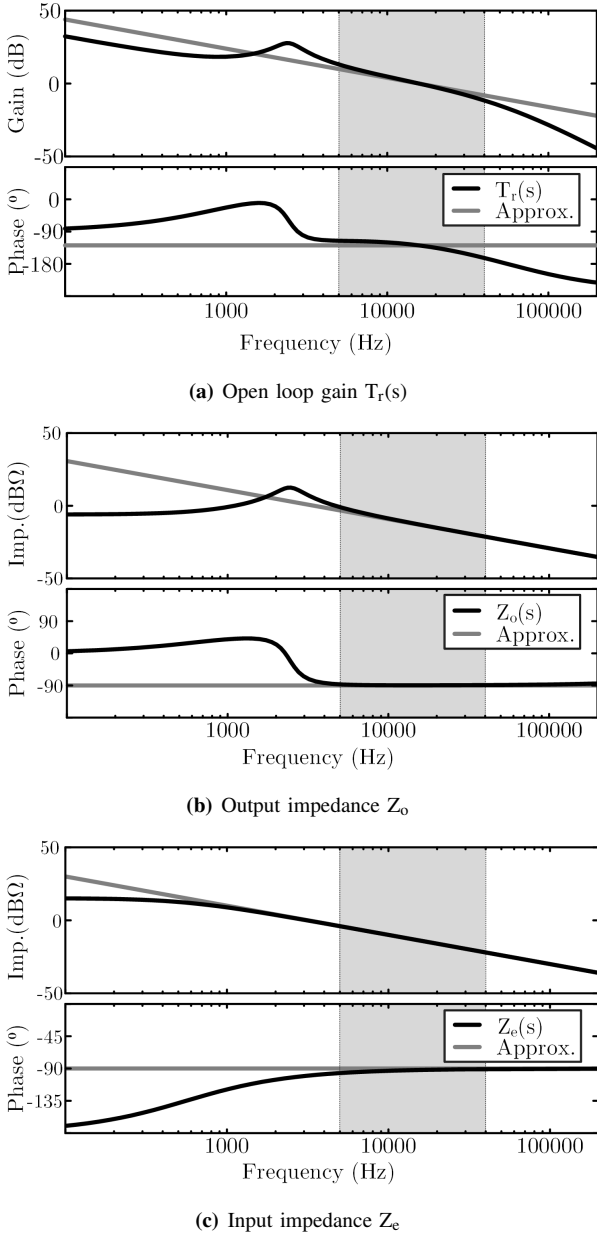


Fig. 3. Comparison of theoretical and approximated transfer functions.

inductor values (L). They are determined by the maximum allowable inductor current ripple (Δi_L) and the minimum acceptable control loop crossover frequency (f_c) [14], [15].

Yet another condition has to be added in order to ensure converter stability due to the aforementioned issue with the proposed design maps and their disregarding of the capacitive loads. When the user adds capacitive load to the bus, the control loop will be affected and could become unstable [13], [16]. This degradation depends on the open loop output impedance of the converter which is designed and the closed loop impedance of the converters connected to the bus [16].

In this example, where a synchronous buck converter with voltage control mode is designed, the evaluation of the open

loop gain degradation with the comprehensive equations can be too complex. However, simple approximations can be used to assess its effect on the loop bandwidth f_c , the resonant frequency f_r and the phase margin φ_v , as shown in Fig. 3:

- The open loop gain of the buck converter with a type III controller is shown in Fig. 3(a). In the shaded frequency interval around f_c , it can be approximated by (1).

$$T_r(s) \Big|_{f \approx f_c} \approx \frac{2\pi f_c}{s} e^{j(\varphi_v - \frac{\pi}{2})}. \quad (1)$$

- The open loop output impedance of the buck converter Z_o , shown in Fig. 3(b) can be approximated around f_c by (2) as the impedance of the output capacitor C .

$$Z_o \Big|_{f \approx f_c} \approx \frac{1}{Cs}. \quad (2)$$

- The closed loop input impedance Z_e of the external converters connected by the user to the bus will depend on their exact implementation. However, most of them can be modeled as a positive or negative resistor, depending on the power flow direction [17], in parallel with their input capacitor C_e . At power levels adequate for domestic applications and following the input capacitor recommendations given in [13], Z_e can be approximated by (3), as shown in Fig. 3(c).

$$Z_e \Big|_{f \approx f_c} \approx \frac{1}{C_e s}. \quad (3)$$

Using the expressions found in [16] and the approximations given in equations (1)-(3), the new loop bandwidth \check{f}_c when a capacitive load C_e is connected to the output bus can be easily calculated using (4). If \check{f}_c is within the frequency range where the approximation is valid, the value of φ_v is not affected.

$$\check{f}_c \Big|_{f \approx f_c} \approx f_c \frac{C}{C + C_e}. \quad (4)$$

In order to ensure that the buck converter is stable when the external capacitive load C_e is added to the output bus, the value of \check{f}_c should be greater than the new resonant frequency \check{f}_r , given by (5), to ensure that the approximations are valid and the phase margin is high enough.

$$\check{f}_r \approx \frac{1}{2\pi} \sqrt{\frac{R_e + R_L}{R_e L (C + C_e)}}. \quad (5)$$

Based on this condition, a new limit $C(C_e)$ can be determined in order to ensure that \check{f}_c is greater than N_e times the value of \check{f}_r . A value of 2.5 is chosen empirically for N_e to ensure a good match between the approximation and the model. The minimum value for $C(C_e)$ is calculated solving (6). As the maximum obtainable value of f_c is linked to L , and system parameters such as the input and output voltages (V_i and V_o) and the duty cycle limitations imposed by the controller circuit D_{\min} and D_{\max} [14], it is easy to add the new condition to the design map as shown in Fig. 2.

$$C(C_e) \geq \left(N_e^2 + \sqrt{N_e^4 + \frac{N_e^2 \pi^2 \min \{D_{\max} V_i - V_o, |D_{\min} V_i - V_o|\}^2 C_e}{L \Delta I_o^2}} \right) \frac{2L \Delta I_o^2}{\pi^2 \min \{D_{\max} V_i - V_o, |D_{\min} V_i - V_o|\}^2}. \quad (6)$$

If a different topology or control mode is used, the criterion to determine the minimum value for C to ensure stability should be adapted. For example, if a boost converter with current peak mode control is chosen for the implementation of the niBP, the approximations used in this work can be applied with little modifications. However, as that implementation does not show a second order response, only the relationship between f_c and the controller pole and zero positions has to be taken into account. When it comes to the design of the iIBC, there is no need to account for the variable capacitive load as the 48 V intermediate bus is no accessible to the user and the niBPs can be designed beforehand and taken into account when modeling the iIBC plant.

Even though several limits have been imposed, the design map shown in Fig. 2 still has an infinite amount of $\{L,C\}$ pairs which comply with all the requirements for a given f_s . The $\{L,C\}$ marked as P_{opt} provides both the minimum C and the smallest L which comply with all the requirements. Although this does not necessarily guarantee that the volume of this $\{L,C\}$ will be the smallest one due to commercially available values and fabrication technologies, the energy that its elements will store is minimum and it should provide a compact solution. Additionally, the condition imposed by the minimum f_c is no longer required with this design point.

Therefore, once the optimal filter design criterion is defined, a single $\{L,C\}$ pair is obtained for every f_s with just a small set of equations. However, these maps do not provide any information about which f_s should be chosen. On the one hand, a higher switching frequency reduces the filter energy storage, potentially reducing its volumen [18]. On the other hand, if the chosen value for f_s is too high, the efficiency of the converter will drop and it might even increase the required filter volume due to the need for special, high frequency materials [19]. Thus, it is important to choose an appropriate value for f_s .

Converter losses can be estimated in most topologies using relatively simple models and equations, which only depend on the switching frequency, system specifications and the chosen components. In a synchronous buck converter, power losses are mainly due to the pair of MOSFETs and the inductor. The current ripple through the capacitors is commonly small enough to consider their losses negligible [15], although it is also relatively easy to model if the capacitor series resistance and the current flowing through them is known.

The losses P_{sw} due to the MOSFETs are roughly linear with the switching frequency, as seen in (7).

$$P_{sw} \approx P_c + K_s f_s, \quad (7)$$

where P_c are the conduction losses and K_s is a coefficient which depends on the MOSFET parameters and electrical variables [20].

The inductor losses P_L are somehow more difficult to model as, when using the traditional design equations, they depend on the inductance value and the number of turns. However, for a fixed inductor current ripple Δi_L , it is possible to transform the equations provided in [21], [22] into an expression which only

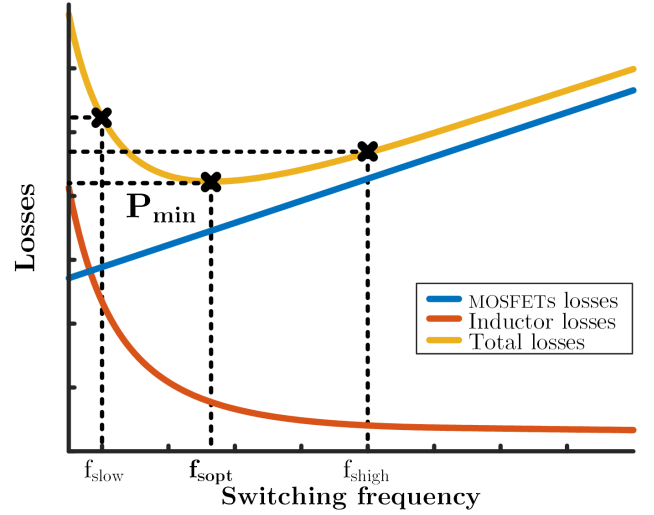


Fig. 4. Estimated converter losses for different switching frequencies and calculation of f_{sopt} .

depends on f_s , a coefficient K_{CO} related to core and winding characteristics and the core material loss coefficients α and β .

$$P_L \approx K_{CO} f_s^{2\frac{\alpha-b}{2+\beta}}. \quad (8)$$

The total losses of the converter P_t are thus determined by (9).

$$P_t = P_{sw} + P_L \approx P_c + K_s f_s + K_{CO} f_s^{2\frac{\alpha-b}{2+\beta}}. \quad (9)$$

Fig. 4 shows the trend of MOSFETs, inductor and total losses of a synchronous buck converter, for a given pair of MOSFETs and magnetic components. It can be seen how, at very low frequencies, the losses dramatically increase due to the inductor. Even though the losses in the MOSFETs are at their lowest, the efficiency of the converter is relatively low. At high switching frequencies, most of the converter losses are due to the switching processes in the MOSFETs and increase linearly with f_s . The lower total losses are obtained when a moderate switching frequency f_{sopt} is chosen. As the expression obtained in (9) for P_t only has a global minimum, the exact value of f_{sopt} can be easily calculated using (10).

$$f_{sopt} = \left(\frac{K_s}{2K_{CO} \frac{\beta-\alpha}{2+\beta}} \right)^{\frac{2+\beta}{2\alpha-3\beta-2}}. \quad (10)$$

Once f_{sopt} is known, it is possible to calculate the P_{opt} $\{L,C\}$ pair at said switching frequency and fully design the converter. If the chosen topology is not a synchronous buck, the values of the coefficients used in (7) and (8) will be modified but the exact same procedure can be used.

III. DESCRIPTION OF THE PROPOSED OPTIMIZED DESIGN

Fig. 5 shows the proposed design algorithm, which is based on the proposed design maps and the effect of f_s on the losses. It is comprised of the following steps:

A. Initial design conditions

Initially, a small set of inputs must be set by the designer:

- Voltage, current and power levels of the converter.
- Power quality criteria $\{\Delta v_{op}, \Delta v_{ot}\}$ and C_e .
- Maximum load transient ΔI_o .
- Maximum allowable total converter losses.

Depending on the chosen topology, additional inputs might be required. For example, for the synchronous buck converter, a moderate inductor current ripple (Δi_L) is chosen to keep losses low, especially at low loads, with good enough converter dynamics [14].

B. Selection of components

Once the converter topology and its electrical specifications are chosen, it is possible to calculate the stress that the components will withstand and to choose them accordingly. This selection will also depend on available space, budget and designer experience.

Another option could be the selection of these components based on different figures of merit. This way, the designer will have to evaluate a large amount of components but the best possible option would always be chosen.

C. Calculation of $f_{s,opt}$ and P_t

Using the process described in the previous section, the value of $f_{s,opt}$ can be obtained and used to determine the losses in each component and the total converter efficiency. If any of these loss components are too high for the specifications of the system, a different set of components should be chosen.

D. Magnetic components design

This step heavily depends on the chosen topology. For basic, non-isolated topologies such as buck, boost or buck-boost converters, the inductor is designed following the traditional methods. The designer should ensure that this inductor is feasible, the core does not saturate in any operating point and its temperature does not increase over the maximum allowable level. If an isolated topology has to be designed, a similar procedure has to be used to choose the most appropriate transformer implementation. If the minimum requirements cannot be met, the designer should choose a new set of components.

Additionally, most topologies have their maximum bandwidth limited by the inductance value [14]. In this step, the designer should verify that the the maximum obtainable value of f_c is adequate and that it can be achieved with the chosen control circuit.

E. Capacitor calculation and control loop design

Finally, the output capacitor of the converter is calculated to comply with the power quality and stability requirements. The control loop can now be calculated to finish the design. If the result of the design process is still not good enough, a different set of MOSFETs, magnetic core and, in the example of the buck converter, Δi_L can be chosen, iterating the design process.

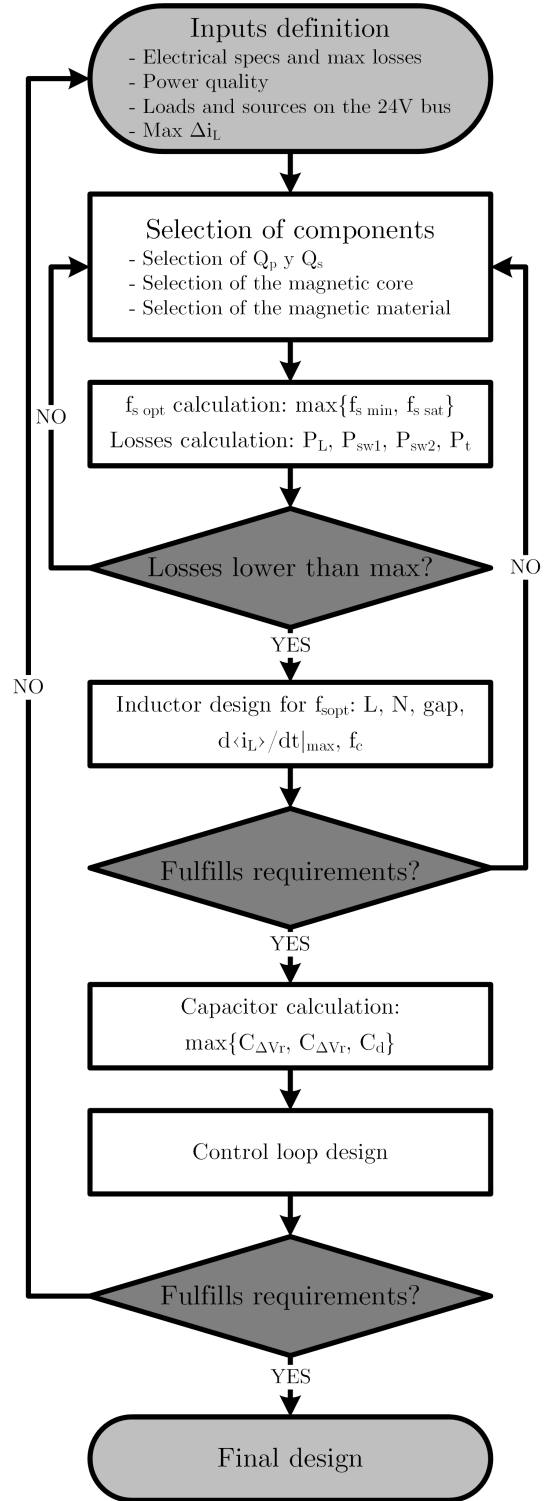


Fig. 5. Proposed design procedure, its details adapted to the synchronous buck converter with voltage mode control.

IV. DESIGN EXAMPLE FOR A SYNCHRONOUS BUCK CONVERTER

In order to verify the analytical results, an niBP is designed following the proposed procedure to provide a 24 V, ± 100 W

TABLE I
KEY PARAMETERS OF DIFFERENT NI_{BP} DESIGNS.

Parameter	Optimum Design	Design1	Design 2
f_s (kHz)	183.5	90	360
f_c (kHz)	14.7	7.2	28.8
L (μ H)	78.5	160.0	40.0
$C(\Delta v_{op})$ (μ F)	4.7	9.7	2.4
$C(\Delta v_{ot})$ (μ F)	39.0	79.6	19.9
$C(C_e)$ (μ F)	35.6	54.3	24.4
C (μ F)	39.0	79.6	24.4
P_L (W)	0.41	1.45	0.19
P_{sw} (W)	1.73	1.41	2.34
P_{aux} (W)	0.51	0.51	0.51
P_t (W)	2.65	3.36	3.03

output bus from an intermediate bus of 48 V. Δi_L is limited to 833 mA (20%) and the maximum ΔI_o is ± 4.16 A. Δv_T and Δv_o are limited to 120 mV and 1.2 V respectively and the maximum value of C_e is 100 μ F according to [23].

For this example, a synchronous buck converter is selected. It has already been stated that this has an effect on the equations to be used. However, the general design procedure proposed in the previous section could be applied to any other topology by simply changing the expressions used to calculate the steady-state and dynamic behavior of the converter as well as the losses estimation equations.

For this design, the OnSemiconductor FDB3502 MOSFET is used for both switches and an RM8 core with EPCOS N97 material is chosen. Voltage mode analog control is implemented with an OnSemiconductor MC33023 and its power consumption is measured and included as P_{aux} . It is important to note that this controller has a maximum duty cycle D_{max} of 0.9 which has to be taken into account during the design process.

In order to verify that the proposed procedure provides the optimum switching frequency which minimizes the total converter losses at full load, three different prototypes, shown in Fig. 6 are built. First, the Optimum Design is the one provided by the algorithm presented in the previous section with the aforementioned components. Design 1 and Design 2 have arbitrarily chosen switching frequencies but their power stage and control loop are calculated following steps *D*, *C* and *E* of the algorithm. Their key design parameters are shown in Table I. This table confirms the theoretical analysis:

- The control loop bandwidth f_c is reduced at low switching frequencies. This is due to the higher value of L needed to maintain the required Δi_L .
- As expected, the value of L is inversely proportional to f_s and the value of C also decreases with f_s . However, the condition imposed by the effect of the external capacitive load C_e on the loop stability prevents C from being inversely proportional to f_s .
- As previously shown in Fig. 4, the losses share between the inductor and the MOSFETs greatly depends on the switching frequency. When a low f_s is used as in Design 1, the MOSFETs switching losses are significantly reduced

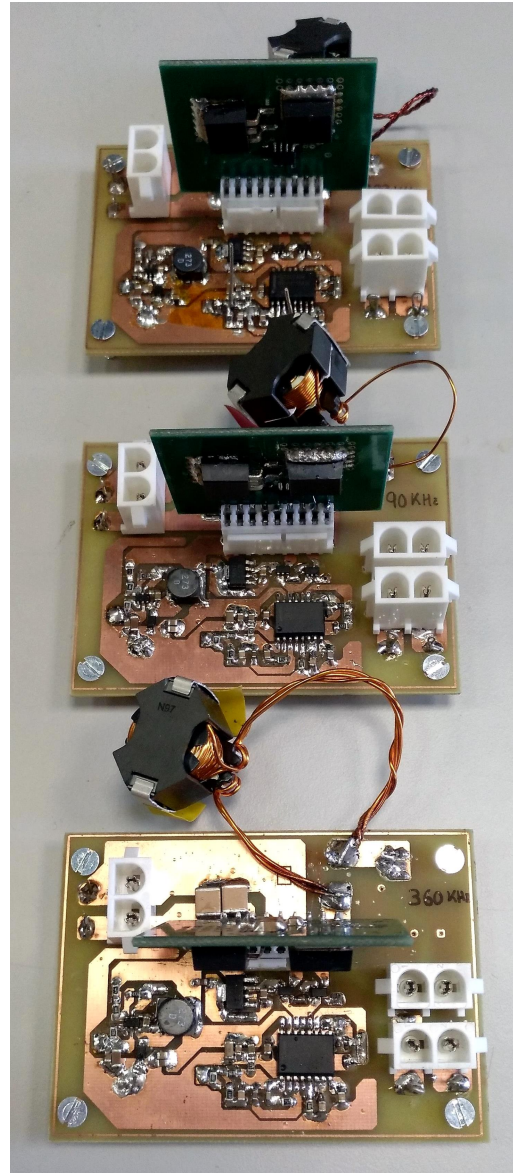


Fig. 6. Prototypes of the three synchronous buck converter designs. From top to bottom: Optimum Design, Design 1 and Design 2.

with respect to the Optimum Design. However, due to the increased required value of L , inductor losses are more than three times higher, reducing overall converter efficiency. When f_s is too high as in Design 2, the opposite effect is observed and, once again, the losses are higher than in the Optimum Design.

Due to the relatively small losses difference between Design 2 and the Optimum Design, it could be argued that, depending on the application, Design 2 could be more desirable. Although there is a slight increase of the overall losses, the required capacitor is smaller than in the Optimum Design, potentially reducing the manufacturing cost and converter volume. However, in these prototypes, it is the inductor and not the output capacitor which limits the power density of the converter.

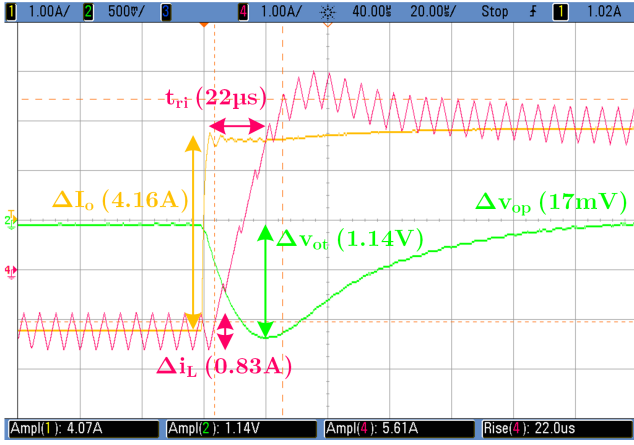


Fig. 7. Load current (CH1) step from -1.2 A to 3 A, showing output voltage (CH2) and inductor current (CH4).

V. EXPERIMENTAL RESULTS

The prototypes shown in Fig. 6 are thoroughly tested to verify that the proposed design procedure ensures the compliance with all the imposed requirements.

Fig. 7 shows the output voltage response of the Optimum Design to a load step from -1.2 A to 3 A. Besides showing bidirectional operation of the niBP, this is the worst case regarding Δv_{ot} , as the duty cycle is limited to 90% . This makes the effective inductor current slope smaller than during the equivalent falling step, as there is no minimum duty cycle limit. Several load steps have been applied at different operating points and the worst measured Δv_{ot} was 1.16 mV, which complies with the requirement. The measured value of Δv_{op} is 17 mV, well below the requirement due to C being much higher than $C(\Delta v_{op})$, as voltage ripple was not the most stringent requirement of the three imposed on power quality.

Fig. 8 shows an equivalent load step, in this case from 2.1 A to -2.1 A. As the inductor current has to decrease in this case and the duty cycle is not limited, the transition is faster. This leads to a smaller value of Δv_{ot} than the one measured in Fig. 7 with a load step of the same magnitude.

Fig. 9 shows the open loop gain of the Optimum Design at full load when different capacitive loads are connected to the output, measured with a Venable FRA6320 frequency response analyzer. The crossover frequency decreases as the external capacitor is increased but it is always kept well over the filter resonance frequency, which also shifts. Due to the correct design of the output capacitor, it is possible to guarantee a good phase margin in every condition. This ensures correct operation of the designed niBP when loads and sources connected to the bus add capacitive load up to the practical limit. Table II shows how the measured values of the modified loop bandwidth \check{f}_c and the modified phase margin $\check{\phi}_v$ closely match with the theoretical values obtained through the expressions used in [16].

Finally, Table III shows the expected and actual losses at full load of each design. It can be seen how, even with relatively simple loss models, the analytical values closely resemble

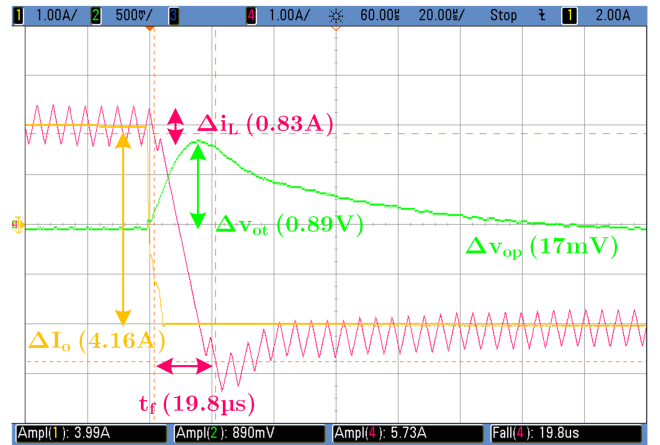


Fig. 8. Load current (CH1) step from 2.1 A to -2.1 A, showing output voltage (CH2) and inductor current (CH4).

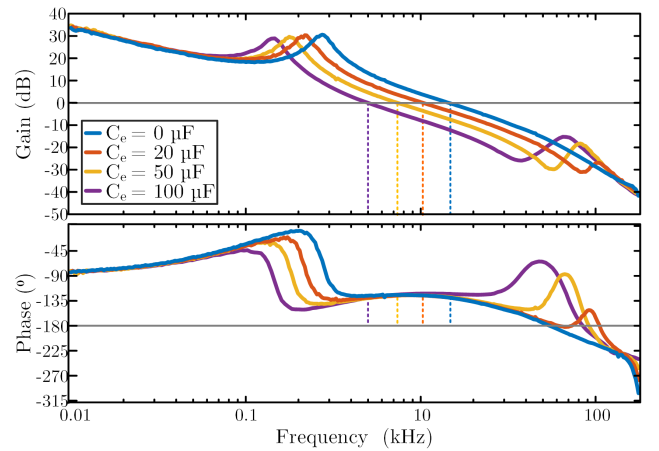


Fig. 9. Open loop gain of the Optimum Design for different capacitive loads.

the measurements. These results also verify that the proposed optimization procedure actually provides the best switching frequency f_{sopt} and alternative designs have a lower efficiency at full load.

VI. CONCLUSION

A procedure for designing converters for their integration in DC-PDSs has been proposed in this work. It is focused on providing a high-power quality and reducing the losses, cost and volume and it shows how important the capacitive load added by the user is regarding system stability. Only a

TABLE II
THEORETICAL AND MEASURED VALUE OF \check{f}_c AND $\check{\phi}_v$.

C_e (μF)	0	20	50	100
Theoretical \check{f}_c (kHz)	16.5	11.8	8.4	5.8
Measured \check{f}_c (kHz)	16.5	11.7	8.5	5.8
Theoretical $\check{\phi}_v$ ($^\circ$)	54.9	58.4	58.8	55.5
Measured $\check{\phi}_v$ ($^\circ$)	54.9	56.8	58.9	57.1

TABLE III
EXPECTED AND MEASURED LOSSES.

Parameter	Optimum Design	Design 1	Design 2
f_s (kHz)	183.5	90	360
Exp. Loss (W)	2.65	3.36	3.03
Meas. Loss (W)	2.87	3.48	3.15
Exp. Eff. (%)	97.4	96.7	97.0
Meas. Eff. (%)	97.2	96.6	96.9

small set of initial conditions, based on system specifications and budget constructive constraints, is required for the design. The procedure is automated in order to provide the optimum switching frequency and design the power stage and control loop accordingly.

In this work, the procedure is demonstrated with synchronous buck converters, which could be used as the non isolated interface with the end user in an Intermediate Bus Architecture. Two alternative designs are compared with the Optimum Design and the obtained results verify that the proposed design method both maximizes efficiency and ensures the correct operation of the converter in domestic power distribution applications.

Due to the procedure being somewhat generic and based on simple models, it can be easily adapted to any other topology or control mode. Although the equations to be used will be slightly different, the losses models will show similar trends for any topology and the power stage will mostly depend on the design requirements and the chosen switching frequency. Most commonly used control modes have been thoroughly studied and can also be modeled by simple equations [14].

Another option is to use the proposed design procedure as the core of an iterative process. If the designer provides a wide array of possible inputs and components, multiple quasi-optimum designs will be obtained from the design process. Based on these results, the designer could choose the one which is more appropriate for the application and budget constraints.

Finally, even though the example provided in this work is intended for domestic power distribution, the presented procedure could be used for different applications. Additional conditions should be added to the design maps and slightly different criteria will be used to define the design point P_{opt} , but the core of the proposed procedure will be unchanged. It is also possible to relax the conditions in some applications. As it was previously mentioned, some of the converters which will always operate with fixed, well-known loads, such as the iIBC shown in Fig. 1, can be designed for a fixed capacitive load and not too stringent power quality requirements.

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