Reducing Q_{rr} in High-Voltage SuperJunction MOSFETs by Using the Cascode Configuration

Juan Rodriguez, Alberto Rodriguez
and Diego G. Lamar
Electronic Power Supply Systems Group.
University of Oviedo
Campus de Viesques, s/n, 33204. Gijon, Spain
rodriguezmjuan@uniovi.es

Jaume Roig and Filip Bauwens
Power Technology Centre, Corporate R&D
ON Semiconductor
Oudenaarde, Belgium
Jaume.roig@onsemi.com

***Abstract*— In this paper, the reverse conduction behavior of a Cascode Configuration (CC), combining a High-Voltage (HV) SuperJunction MOSFET (SJ-FET) and a Low-Voltage silicon MOSFET (LV-FET) is deeply scrutinized by means of an analytical model and experimental data. The reverse recovery charge (Q_{rr}) of SJ-FETs in CC with LV-FETs (SJ-CCs) is investigated in this work. As a result of the study, it has been found that the proposed SJ-CC avoids or mitigates the conduction of the SJ-FET body diode during reverse conduction. As consequence, the Q_{rr} achieved by the CC is several times lower than in the case of the standalone configuration. Moreover, the Q_{rr} reduction achieved results in record-low Q_{rr} for 600 V-range silicon transistors at a fixed on-resistance (R_{DSON}).**

Keywords—Cascode configuration, SuperJunction MOSFET, reverse conduction, reverse recovery charge (Q_{rr}), silicon.

I. INTRODUCTION

As a result of an application-oriented strategy, High-Voltage (HV) SuperJunction MOSFETs (SJ-FETs) are optimized to reduce the Reverse Recovery (RR) when addressing specific circuit topologies (e.g. converters with synchronous rectification [1]-[2]), in order to mitigate its effect on switching losses [3]. The RR optimization normally implies reduction of RR charge (Q_{rr}), RR peak current (I_{rrm}) and RR time (t_{rr}), as well as softening waveform snappiness. Despite Schottky diodes co-integration was initially proposed [4], commercial SJ-FETs with enhanced RR are mainly based on irradiation process [5]. Device irradiation normally requires special facilities, thus adding cost and jeopardizing other electrical parameters such as threshold voltage (V_{TH}), on-resistance (R_{DSON}) or leakage current. Some studies propose methods to improve RR in SJ-FETs by complex circuit topologies and driving techniques [6]-[8]. Other works suggest the use of SiC or GaN transistors to efficiently tackle RR, disregarding their unviability in cost-sensitive applications [9]. Differently from the prior literature, this paper proposes a Cascode Configuration (CC) combining a SJ-FET and a Low-Voltage silicon MOSFET (LV-FET) to improve RR with a low-cost full-silicon solution.

During the last 5 years, the CC has become the preferred approach for some semiconductor companies to achieve normally-off GaN and SiC power switches [10]-[14]. In [15]-[16], the use of a SJ-FET in CC with a LV-FET (SJ-CC) is proposed to reduce switching losses (see Fig. 1a). The authors of the present paper recently published a theoretical model of the switching mechanism during forward conduction of SJ-CCs with special focus on the critical parasitic elements [17].They also demonstrated that the SJ-CC outperforms the SJ-FET in standalone configuration when is used in some ultra-fast hard-switching and high-forward-current operation conditions [18]. However, none of the previous works deep dives into the reverse conduction behavior of the SJ-CC.

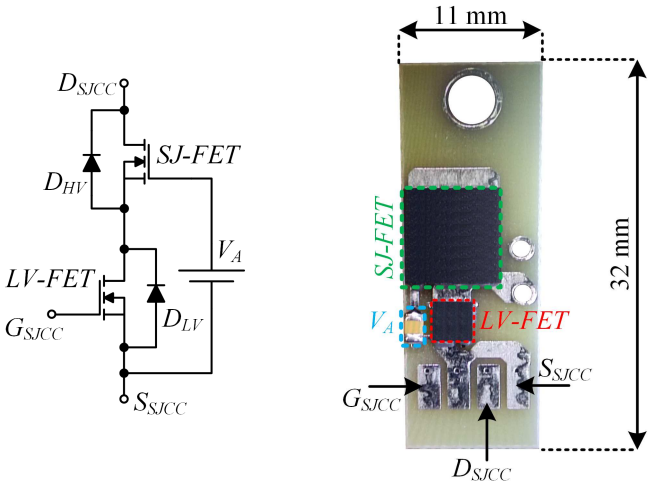

Fig. 1. SuperJunction MOSFET in Cascode Configuration with a Low-Voltage silicon MOSFET (SJ-CC): (a) Ideal circuit schematic. (b) Plug-in board with SJ-CC prototype.

The aim of this paper is to model the reverse conduction behavior and to prove the Q_{rr} reduction achieved when a SJ-FET optimized for hard-switching is used in CC instead of in standalone configuration. Moreover, the Q_{rr} improvement is evaluated by comparison with the state-of-the-art of irradiated SJ-FETs. The paper is organized as follows. The reverse conduction of SJ-CC is detailed in section II. This section includes the reverse conduction analytical model, its validation by measured reverse conduction curves and the benefits and drawbacks of the SJ-CC in comparison with the standalone configuration. Section III is focused on Q_{rr} measurements. It includes the details of the test bench developed to measure Q_{rr}, a deep analysis of the Q_{rr} results of SJ-CCs and the improvement with respect to Q_{rr} provided by SJ-FETs in standalone configuration. The comparison with the Q_{rr} achieved by

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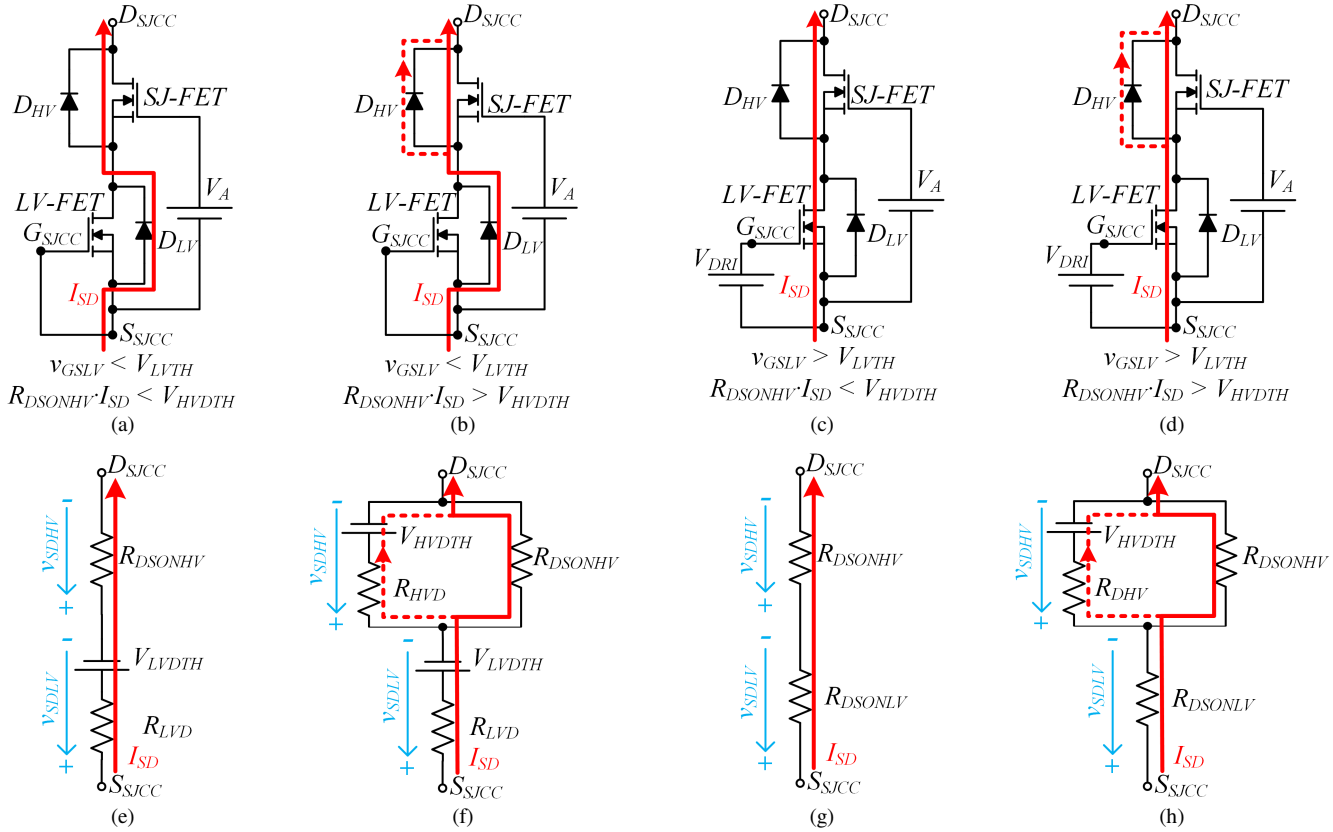

Fig. 2. SJ-CC circuits during reverse conduction: (a) Regime 1. (b) Regime 2. (c) Regime 3. (d). Regime 4. (e) Equivalent circuit during regime 1. (f) Equivalent circuit during regime 2. (g) Equivalent circuit during regime 3. (h) Equivalent circuit during regime 4.

irradiated SJ-FETs is also covered in this section. Finally, conclusions are gathered in section IV.

II. SJ-CC Reverse Conduction

A. *SJ-CC operation regimes in reverse conduction*

Four different operation regimes can be identified during the reverse conduction of a SJ-CC. The operation regime depends on the LV-FET gate to source voltage (v_{GSLV}), the LV-FET threshold voltage (V_{LVTH}), the SJ-FET on-resistance (R_{DSONHV}), the SJ-CC source to drain current (I_{SD}) and the knee-voltage of the SJ-FET body diode (V_{HVDTH}).

- Regime 1 (Fig. 2a): $v_{GSLV}<V_{LVTH}$ and $R_{DSONHV}\cdot I_{SD}<V_{HVDTH}$. The LV-FET channel is not created because v_{GSLV} is lower than V_{LVTH}. As consequence, the current flows through the LV-FET body diode (D_{LV}), defining the source to drain voltage of the LV-FET (v_{SDLV}) according to expression (1). Note that R_{LVD} denotes the dynamic resistance of D_{LV} whereas V_{LVDTH} is the knee-voltage of the LV-FET body diode. The gate to source voltage of the SJ-FET (v_{GSHV}) is equal to the voltage applied between the SJ-FET gate and the LV-FET source (V_A) plus v_{SDLV}. The value is higher than the SJ-FET threshold voltage (V_{HVTH}). Hence, the current flows through the SJ-FET channel, which defines the source to drain voltage of the SJ-FET (v_{SDHV}) according to expression (2). Note that in this regime, I_{SD} is low enough to define a V_{SDHV} value lower than V_{HVDTH}, which typically ranges between 0.6 and 0.8 V. As consequence, there is not current drift through the SJ-FET body diode (D_{HV}). Fig. 2e shows the equivalent circuit during this regime.

$$v_{SDLV} = V_{LVDTH} + I_{SD} \cdot R_{LVD}, \tag{1}$$

$$v_{SDHV} = I_{SD} \cdot R_{DSONHV}. \tag{2}$$

- Regime 2 (Fig. 2b): $v_{GSLV}<V_{LVTH}$ and $R_{DSONHV}\cdot I_{SD}>V_{HVDTH}$. The reasoning related to the LV-FET behavior that has been detailed for regime 1 remains valid for this regime. As consequence, the current flows through D_{LV} and expression (1) is valid to model the voltage drop at the LV-FET. In this case, the greater value of I_{SD} imposes a V_{SDHV} value high enough to cause a current drift through D_{HV}. Expression (3) models the voltage drop at the SJ-FET taking into account the previous consideration. Note that R_{HVD} denotes the dynamic resistance of the SJ-FET body diode. Fig. 2f shows the equivalent circuit during this regime.

$$v_{SDHV} = \left(I_{SD} + \frac{V_{HVDTH}}{R_{HVD}}\right) \cdot \frac{R_{DSONHV} \cdot R_{HVD}}{R_{DSONHV} + R_{HVD}}. \tag{3}$$

- Regime 3 (Fig. 2c): $v_{GSLV}>V_{LVTH}$ and $R_{DSONHV}\cdot I_{SD}<V_{HVDTH}$. In this regime the LV-FET channel is created because v_{GSLV} is higher than V_{LVTH}. As consequence, the current flows through the LV-FET channel, determining v_{SDLV} according to expression (4). Note that R_{DSONLV} denotes the LV-FET on-resistance. v_{GSHV}

is higher than V_{HVTH} and, therefore, the current flows through the SJ-FET channel. Moreover, as in the case of regime 1, the I_{SD} value is low enough to avoid the D_{HV} activation. Expression (2) is also valid to model the voltage drop at the SJ-FET. Fig. 2g shows the equivalent circuit during this regime.

$$v_{SDLV} = I_{SD} \cdot R_{DSONLV}. \quad (4)$$

- Regime 4 (Fig. 2d): $v_{GSLV} > V_{LVTH}$ and $R_{DSONHV} \cdot I_{SD} > V_{HVDTH}$. As in the case of regime 3, the current flows through the LV-FET channel and expression (4) is valid to model the voltage drop at the LV-FET. In this case, the I_{SD} value is high enough to define a V_{SDHV} value that causes a current drift through D_{HV}. Expression (3) is also valid to model the voltage drop at the SJ-FET. Fig. 2h shows the equivalent circuit during this regime.

From a theoretical point of view, an I_{SD} value high enough could impose a current drift through D_{LV} and a fifth regime would have to be taken into account. However, the required I_{SD} value makes no sense due to the low R_{DSONLV} value (tens of mΩ).

B. SJ-CC reverse conduction curves

The SJ-CC reverse conduction model presented in the previous section was validated by measuring experimentally the third-quadrant curve of SJ-CC prototypes. In order to study the impact of the characteristics of the LV-FET and the SJ-FET, different SJ-CC combinations were built by using commercially available devices. Fig. 1b shows one of the SJ-CC prototypes. Note that the implementation was made with discrete devices. It is important to note that SJ-FETs optimized for hard-switching from the major manufactures were used in these implementations. The main electrical parameters of both the SJ-FETs and the LV-FETs are summarized in Table I and Table II respectively.

Fig. 3 shows the analytical (following (1) to (4) equations) an experimental reverse conduction curves of different SJ-CC designs, highlighting the four different regimes into a circle. Designs used in Fig. 3a have the same SJ-FET and different LV-FET. It can be seen that a change in the LV-FET has minor impact on the SJ-CC static reverse conduction behavior. Note that this does not imply that both designs provide the same Q_{rr}. This point will be studied in section III.B. The designs used in Fig. 3b have the same LV-FET and different SJ-FET. It can be seen that a change in the SJ-FET has major impact on the SJ-CC static reverse conduction behavior. V_{HVDTH} is similar in both SJ-FETs, therefore, the SJ-FET voltage drop needed to activate D_{HV} is the same. For the same I_{SD} level, v_{SDHV} is higher in the case of the SJ-CC implemented with SJ-FET 1 due to the greater R_{DSONHV} value. As consequence, the boundary I_{SD} value (I_{SDBOU}) that separates regimen 1 from regime 2 and regime 3 from regime 4 is higher in the case of the SJ-CC implemented with SJ-FET 3.

Fig. 4 shows the reverse conduction curves of the same SJ-FET in standalone configuration and in CC. Note that in the case of the standalone configuration, three regimes can be identified. Regime A appears when v_{GS} is lower than V_{HVTH} and, therefore, I_{SD} completely flows through D_{HV}. Regime B appears when a voltage higher than V_{HVTH} is applied between gate and source of the SJ-FET (v_{GS}) and I_{SD} completely flows through the SJ-FET channel. Regime C, appear when v_{GS} is higher than V_{HVTH} and a current drift through the SJ-FET body diode occurs due to the greater I_{SD} value. Note that I_{SDBOU} is the same in both configurations because the SJ-FET used is the same.

TABLE I. MAIN ELECTRICAL PARAMETERS FOR SJ-FETS USED IN THE DIFFERENT SJ-CC PROTOTYPES.

SJ-FET	BV_{dss} (V)	R_{DSON} (mΩ)	Q_{GD} (nC)	Q_G (nC)	Q_{OSS}* (nC)
1	600	178	27	51	124
2	600	136	22	48	153
3	650	123	11	35	239

* at V_{DS} = 400 V

TABLE II. MAIN ELECTRICAL PARAMETERS FOR LV-FETS USED IN THE DIFFERENT SJ-CC PROTOTYPES.

LV-FET	BV_{dss} (V)	R_{DSON} (mΩ)	Q_{GD} (nC)	Q_G (nC)	Q_{OSS} (nC)
1	30	8.1	1.7 [1]	5.5 [1]	11 [1]
2	12	7.5	0.76 [2]	3.1 [2]	5.7 [2]
3	30	4.4	1.4 [1]	5.2 [1]	7.2 [1]

[1] at V_{DS} = 15 V, [2] at V_{DS} = 6 V

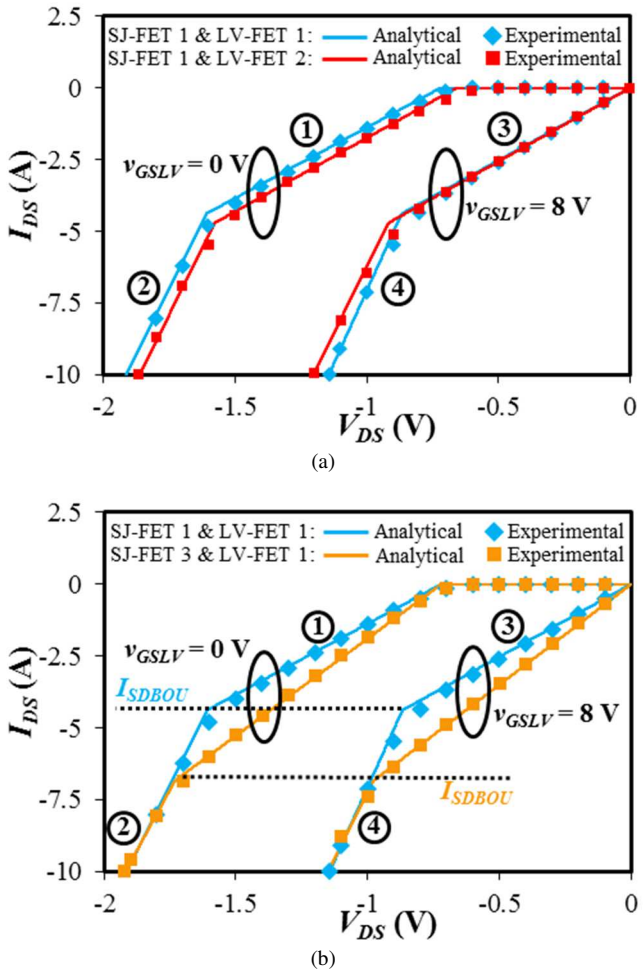

Fig. 3. Analytical (solid lines) and experimental (markers) reverse conduction curves of different SJ-CC designs including the four regimes identification: (a) Two SJ-CC designs with the same SJ-FET and different LV-FET. (b) Two SJ-CC designs with the same LV-FET and different SJ-FET.

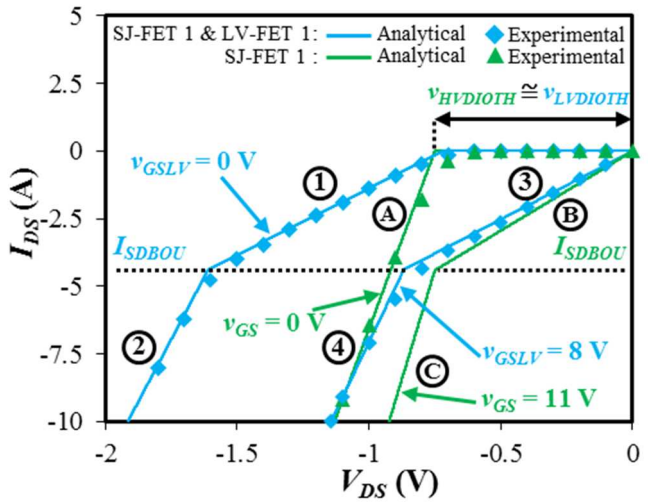

Fig. 4. Analytical (solid lines) and experimental (markers) reverse conduction curves of SJ-FET 1 in standalone configuration and in CC with LV-FET 1 including the different regimes identification.

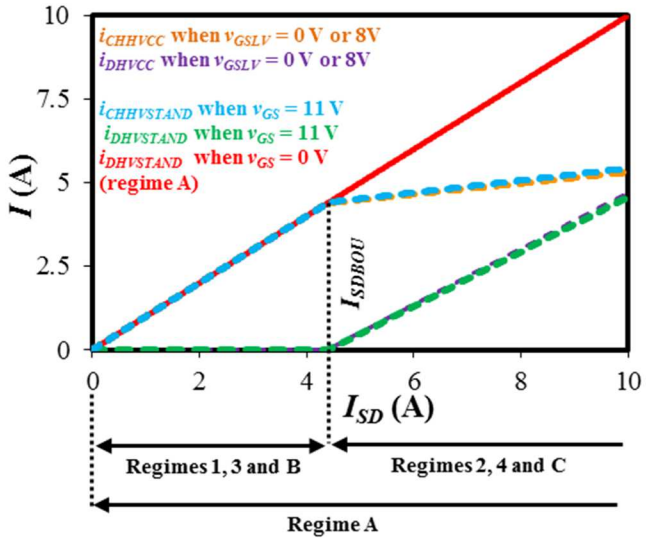

Fig. 5. Theoretical current that flows through the SJ-FET 1 channel in standalone configuration ($i_{CHHVSTAND}$), through the SJ-FET 1 channel in CC with LV-FET 1 (i_{CHHVCC}), through D_{HV} in standalone configuration ($i_{DHVSTAND}$) and through D_{HV} in the CC (i_{DVHCC}) depending on the operating regime.

C. *Suitable operating regimes to reduce Q_{rr}*

There are four sources of Q_{rr} in a SJ-CC. The major contribution comes from D_{HV}. The charge of the SJ-FET C_{OSS} (i.e. SJ-FET Q_{OSS}) constitutes the second most relevant source of Q_{rr}. The contribution of D_{LV} and the charge of the LV-FET C_{oss} are the remaining source of Q_{rr} in a SJ-CC. However, last two ones have minor impact in comparison with the two first sources. In this sense, the desired reverse conduction must avoid as far as possible the D_{HV} activation in order to mitigate its Q_{rr} contribution. According to this, regimes 1 and 3 are preferred. Note that in converters with synchronous rectification, regime 1 will appear during dead times whereas regime 3 appears along the rest of the switch reverse conduction time. Fig. 5 shows the theoretical current (following (1) to (4) equations) that flows through the SJ-FET 1 channel in standalone configuration ($i_{CHHVSTAND}$), through the SJ-FET 1 channel in CC (i_{CHHVCC}), through D_{HV} in standalone configuration ($i_{DHVSTAND}$) and through D_{HV} in CC (i_{DVHCC}) depending on the operating regime.

Focusing on the comparison between a SJ-FET in CC and in standalone configuration, the regimes that appear under the same conditions (i.e. same I_{SD} and either high or either low state of the gate to source voltage) must be compared.

During dead times (i.e. the gate to source voltage is in low-state), regimes 1 and 2 of the SJ-CC and regime A of the standalone configuration must be considered. If I_{SD} is lower than I_{SDBOU}, the SJ-CC operates in regime 1 whereas the SJ-FET in standalone configuration operates in regime A, regardless of I_{SD}. Differently from the standalone configuration, the SJ-CC avoids the D_{HV} activation during regime 1 (Fig. 4). In this regime, conduction losses are higher due to the lower resistance of D_{HV} with respect to the sum of R_{DSONHV} and R_{LVDIO} on-resistance of the SJ-FET. As Fig. 4 shows, the values of v_{LVDTH} and v_{HVDTH} are almost the same. Note that they determine the initial voltage drop for the SJ-CC and for the standalone configuration respectively. Expression (5) models the extra voltage drop of the SJ-CC with respect to the standalone configuration in regime 1. If I_{SD} is higher than I_{SDBOU}, the SJ-CC operates in regime 2 whereas the SJ-FET in standalone configuration keeps operating in regime A. There is current flowing through D_{HV} in both configurations. However, the current is distributed between the channel and D_{HV} in the SJ-CC whereas the whole current flows through D_{HV} in the case of the standalone configuration. As consequence, the Q_{rr} contribution of D_{HV} is always lower in the case of the SJ-CC. In the same way, the SJ-CC conduction losses are higher in this situation (Fig. 4). Expression (6) models the extra voltage drop in regime 2.

During the rest of the switch reverse conduction time (i.e. the gate to source voltage is in high-state) and if I_{SD} is lower than I_{SDBOU}, the SJ-CC operates in regime 3 whereas the SJ-FET in standalone configuration operates in regime B. The current flows through the channel of the SJ-FET in the standalone configuration and through the channels of the SJ-FET and of the LV-FET in the case of the CC. The main difference between them is the extra conduction losses of the SJ-CC due to the additional on-resistance of the LV-FET. However, as [18] indicates, these extra conduction losses can be neglected in practice. If I_{SD} is higher than I_{SDBOU}, the SJ-CC operates in regime 4 whereas the SJ-FET in standalone configuration operates in regime C. In both regimes, there is a part of I_{SD} that flows through D_{HV} and as Fig. 5 shows, this current level is almost the same in both cases. Another time, SJ-CC have negligible extra conduction losses.

$$v_{ExtraReg1} = V_{LVDTH} - V_{HVDTH} + (R_{LVD} + R_{DSONHV} - R_{HVD}) \cdot I_{SD}, \tag{5}$$

$$v_{ExtraReg2} = V_{LVDTH} + \frac{1}{R_{DSONHV} + R_{HVD}} \cdot \{[R_{LVD} \cdot R_{DSONHV} + R_{HVD} \cdot (R_{LVD} - R_{HVD})] \cdot I_{SD} - R_{HVD} \cdot V_{HVDTH}\}. \tag{6}$$

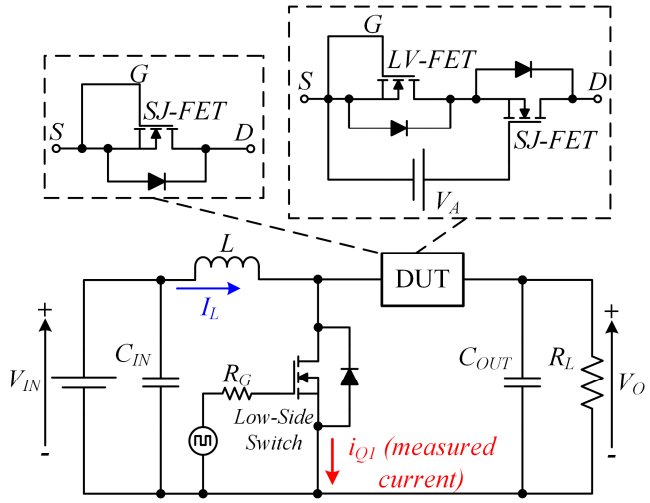

Fig. 6. Schematic of the boost converter used to measure Q_{rr} of the DUT (either SJ-FETs in standalone configuration or SJ-CCs).

In summary, when the gate to source voltage of the switch is in high-state, the reverse recovery behavior of both the SJ-CC and the standalone configuration is almost the same. The difference appears when the gate to source voltage is in low-state. Under this condition, the Q_{rr} contribution of D_{HV} is always smaller in the case of the SJ-CC (null if it operates in regime 1). The price to pay is that SJ-CC has higher conduction losses in this situation.

III. Reverse Recovery Charge Measurements

A. Test details

Q_{rr} was experimentally measured in a boost converter where the power rectifier was replaced by a switch with a short circuit between its gate and its source (see Fig. 6). The rest of the boost converter components were fixed, including the SJ-FET in standalone configuration that was used as low-side switch. The switching frequency is 100 kHz and the inductor was designed to ensure a negligible current ripple. Q_{rr} which comes from regimes 1 and 2 of a SJ-CC and A of a SJ-FET in standalone configuration can be measured with this configuration. These regimes were considered interesting because, as was detailed in section II.C, they show the difference in Q_{rr} between SJ-CC and SJ-FET in standalone configuration.

The Q_{rr} of the Device Under Test (DUT) used as high-side switch was obtained by measuring the drain to source current of the low-side switch (i_{Q1}) during its turn-on. An example is given in Fig. 7. It is important to note that the Q_{rr} contribution of D_{HV} rises with *di/dt* during the turn-on of the low-side switch, the conduction time of the diode and the value of the current that flows through it [19]. Q_{OSS} of the SJ-FET rises with V_{DS} and achieves the 80% of the final value when v_{DS} is around 20 V [20]. Fig. 8 shows C_{OSS} and Q_{OSS} measurements of SJ-FET 3. It can been seen that Q_{OSS} achieves the 80% of its final value at V_{DS} equal to 17 V. Due to this, an output voltage of 50 V allows us to measure most of the SJ-FET Q_{OSS} contribution. Note that although this voltage level is several times lower than the drain to source voltage rating of the SJ-FETs, it is enough to characterize the Q_{rr} of the DUT. *di/dt* was controlled by the gate resistance of the low-side switch an it was fixed to 130 A/µs.

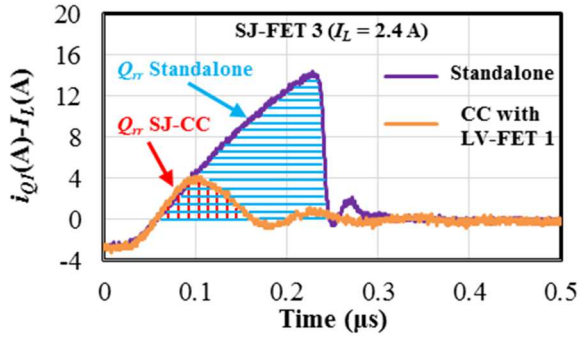

Fig. 7. Comparison of measured current and Q_{rr} between SJ-FET 3 in CC or in standalone configuration when I_L is equal to 2.4 A.

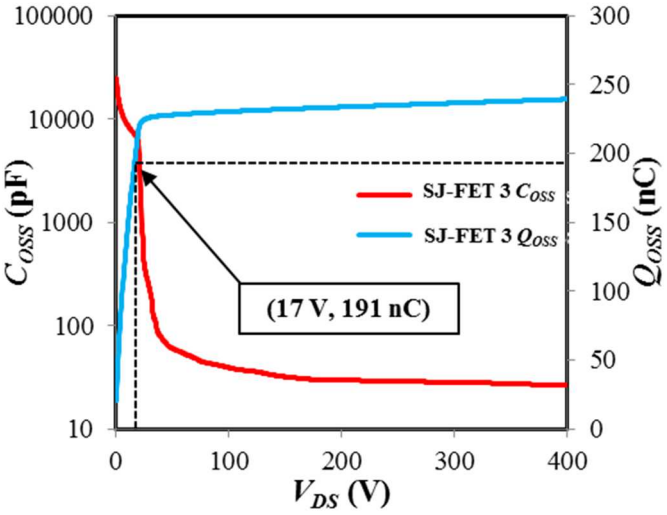

Fig. 8. Measured C_{OSS} and Q_{OSS} of SJ-FET 3. Note that Q_{OSS} achieves the 80% of its final value at 17 V.

The conduction time was fixed to 2.5 µs. Note that the input voltage and output voltage were 12.5 V and 50 V respectively during all tests. Q_{rr} was measured for 3 current levels through the inductor (I_L): 1.2 A, 2.4 A and 6 A. The current waveform was captured in less than one second in order to mitigate the temperature impact.

B. SJ-CC Q_{rr} analysis

Fig. 9 shows the measured Q_{rr} for three SJ-CC designs that have the same LV-FET. According to Fig. 3, I_{SDBOU} is 4 A and 6 A for SJ-FET 1 & LV-FET 1 and SJ-FET 3 & LV-FET 1 respectively. Note that SJ-FET 2 & LV-FET 1 should have an intermediate I_{SDBOU} value due to its $R_{DSONNHV}$ value. As consequence, when the current level is 1.2 A or 2.4 A, the three SJ-CC designs are in regime 1. There is no appreciable increase in the measured Q_{rr}, which implies that there is no contribution from the SJ-FET body diode and the main source of Q_{rr} is the Q_{OSS} of the SJ-FET as was detailed in section II.C. Note that the measured Q_{rr} matches the Q_{OSS} of the SJ-FET in standalone configuration. When the current is 6 A, SJ-CC designs implemented with SJ-FET 1 and 2 are in regime 2 whereas SJ-FET 3 & LV-FET 1 operates in the limit of regimes 1 and 2. The raise in the measured Q_{rr} values indicates the activation of D_{HV}. The higher increase of SJ-FET 1 & LV-FET 1 with respect to

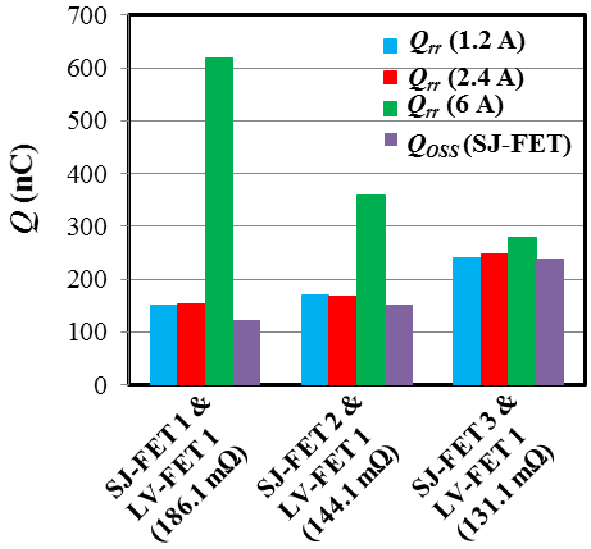

Fig. 9. Q_{rr} measurements for three SJ-CC designs with the same LV-FET but different SJ-FET.

the increase of SJ-FET 2 & LV-FET 1 is due to its greater R_{DSONHV} value. As detailed in section II-B, this causes a higher v_{SDHV} value for the same I_L level and, therefore, higher current flowing through D_{HV}.

Fig. 10 shows the current waveforms for the three SJ-CC designs. Note that the differences in the RR behavior are also visible in this figure.

The small dependence of the SJ-CC Q_{rr} on the LV-FET is shown in Fig. 11. It can be seen the measured current waveforms of three SJ-CC designs implemented with the same SJ-FET but different LV-FETs. The similarity of the results is due to the small impact of the LV-FET Q_{rr} on the whole SJ-CC Q_{rr} in comparison with the SJ-FET Q_{OSS}.

C. Q_{rr} comparison

In order to evaluate the Q_{rr} improvement achieved by the SJ-CC, Q_{rr} was also measured for SJ-FETs in standalone configuration. In this sense, three groups of switches can be identified. The first group contains SJ-FETs optimized for hard-switching in standalone configuration. The second group is based on SJ-FETs with enhanced RR (irradiated SJ-FETs) in standalone configuration. Finally, the third group implements SJ-FETs from the first group in CC. Fig. 12 shows the measured Figure-of-Merit $R_{DSON}{\cdot}Q_{rr}$ at three different current levels (1.2 A, 3 A and 6 A). Results at 6 A are omitted for the first group due to too high self-heating and possible malfunction. As expected, SJ-FETs with enhanced RR show $R_{DSON}{\cdot}Q_{rr}$ that ranges from four to eight times lower than SJ-FETs from the first group. However, $R_{DSON}{\cdot}Q_{rr}$ can be even lower when SJ-FETs from the first group are used in SJ-CC. Effectively, SJ-CC 1 and SJ-CC 2 show lower $R_{DSON}{\cdot}Qrr$ than any other SJ-FET for 1.2 A and 2.4 A, whereas SJ-CC 3 has the best compromise of $R_{DSON}{\cdot}Q_{rr}$ in a wider range of current.

IV. Conclussions

The benefits of a SJ-FET in CC for specific application (i.e. synchronous rectification) are addressed in this work by

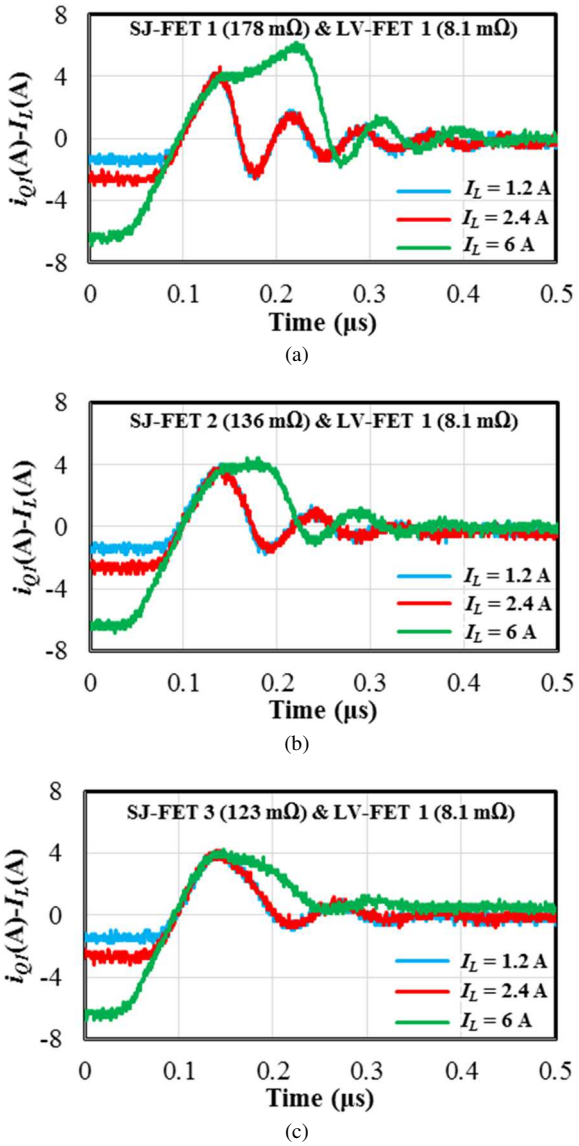

Fig. 10. Measured current waveforms for three SJ-CC designs with the same LV-FET but different SJ-FET: (a) SJ-FET & LV-FET 1. (b) SJ-FET 2 & LV-FET 1. (c) SJ-FET 3 & LV-FET 1.

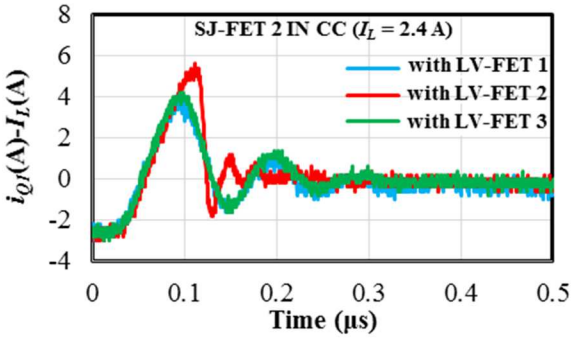

Fig. 11. Measured current waveforms for three SJ-CC designs with the same SJ-FET but different LV-FET when the I_L is 2.4 A.

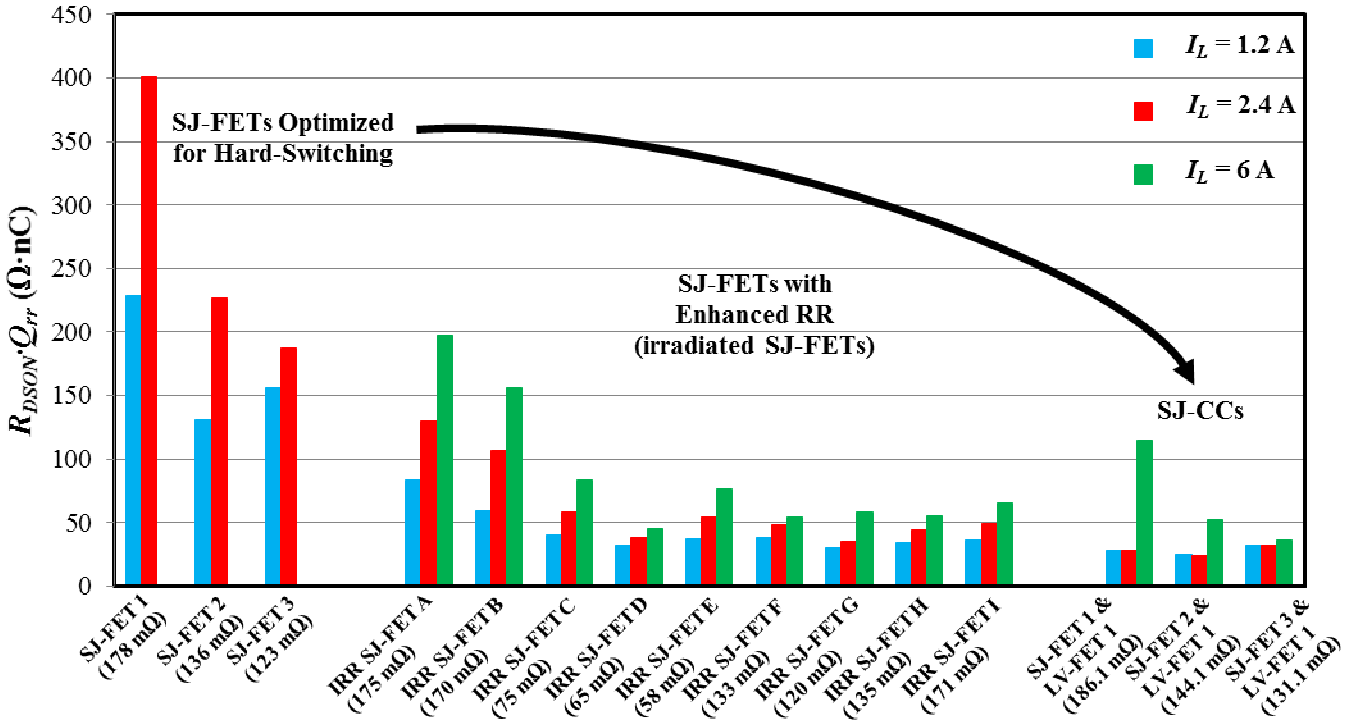

Fig. 12. R_{DSON}·Qrr Figure-of-Merit for different SJ-FET commercial technologies (three major SJ-FET manufacturers included).

extensive exploration of its reverse conduction behavior. Theoretical and experimental data give insight into the physical mechanisms related to reverse recovery behavior. It has been concluded that the Q_{rr} contribution of the SJ-FET body diode can be mitigated and even avoided by using the CC. As consequence, a SJ-CC provides lower Q_{rr} than the same SJ-FET in standalone configuration. Moreover, the presented experimental results show that SJ-CC exhibits best-in-class Q_{rr} for silicon power switches in the 600 V range. Taking into account that the reduction of switching losses achieved by the SJ-CC has already been prove when it is used in ultra-fast hard-switching and high-forward-current operation conditions [18], the SJ-CC seems to be an attractive solution to be used in converters with synchronous rectification.

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