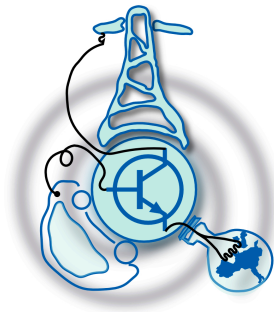# DC-link Ripple Cancellation in Single Phase Converters

by

Lucas Nicieza Moro

Submitted to the Department of Electrical Engineering, Electronics,
Computers and Systems
in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Energy Conversion and Power Systems

at the

UNIVERSIDAD DE OVIEDO

July 2017

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Certified by. . . . .
Jorge García García
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DC-link Ripple Cancellation in Single Phase Converters

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Abstract

Single phase AC/DC converters have a pulsating power that flows from the ac line to the dc bus. As a result, a low frequency ripple voltage appears on the dc-link. The most common way to solve this problem is to filter out the voltage ripple with a bulky electrolytic capacitor. With a large size and a low lifetime such a solution might not be acceptable in many applications. In order to replace the bulky electrolytic capacitor by a small film capacitor, several decoupling units have been proposed in the literature. The control strategy of these decoupling units require them to be combined with the PWM rectifier giving rise to a unique converter. To avoid this limitation, a Universal Power Decoupling Unit that can be separately built from the single phase AC/DC converter is proposed in this thesis. It makes use of a bidirectional boost converter to absorb the undesired voltage ripples. Its analysis and design are validated by simulation and experimental results.

Thesis Supervisor: Jorge García García
Title: Associate Professor

Acknowledgments

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Glossary

Acronyms

ITRI	Industrial Technological Research Institue
AC	Alternating Current
DC	Direct Current
MOSFET	Metal-Oxide-Semiconductor-Field-Effect-Transistor
IGBT	Insulated Gate Bipolar Transistor
GTO	Gate Turn-off Thyristor
EMI	Electromagnetic Interference
RFI	Radio Frequency Interference
ESR	Series Resistance
VSC	Voltage-Source Converter
DCM	Discontinuous Conduction Mode
CCM	Continuous Conduction Mode
NPC	Neutral-Point Clamped
MMC	Modular Multilevel Converter
PWM	Pulse-Width Modulation
PI	Proportional-Integral
THD	Total Harmonic Distortion
FFT	Fast Fourier Transform
UPDU	Universal Decoupling Unit
TI	Texas Instruments
ePWM	Enhanced Pulse Width Modulator

Chapter 1

Introduction

The growth of the environmental awareness over the last few decades combined with the continuous technology development in the field of the power electronics, is giving rise to a new breed of single-phase improved power quality ac-dc converters (IPQs). A direct implication of this rapidly development has been the emergence of new solid state full controlled devices such as metal-oxide-semiconductor-field-effect-transistors (MOSFETs), insulated gate bipolar transistors (IGBTs) and gate turn-off thyristors (GTO) [1]. They allow a gradual transition from the basic thyristors rectifiers to a new generation of power converters that are able to provide controlled and uncontrolled dc power with unidirectional and bidirectional power flow. However, even though this technology has reached a matured level, there are still many concerns related with the power factor improvement, mitigation of harmonic currents, cancellation of voltage and current ripples at the dc output, reduction of electromagnetic interference (EMI) and radio frequency interference (RFI). Each of these issues can be considered as a separate research line with a big number of studies and solutions already carried out and proposed. Among the different concerns mentioned before, this thesis is focused on the cancellation of the voltage and current ripples at the dc output.

1.1 Power Decoupling Principle

Considering an ac-dc converter as the one shown in Fig. 1-1, the ac supply voltage and current are given by:

$$V_{ac(t)} = V_m \sin(\omega t) \tag{1.1}$$

$$I_{ac(t)} = I_m \sin(\omega t - \varphi) \tag{1.2}$$

where ω is the grid frequency, V_m and I_m are the voltage and current maximum values, respectively; φ is the angle between the supply voltage and current. Assuming unity power factor $(\varphi = 0)$, the instantaneous power provided by the input ac source is given by:

$$P_{ac(t)} = \underbrace{\frac{V_m I_m}{2}}_{P_{const}} - \underbrace{\frac{V_m I_m}{2} \cos(2\omega t)}_{P_{ripple}} \tag{1.3}$$

As it can be seen, the instantaneous power consists of two parts: the constant power P_{cte}, and a pulsating power oscillating at twice the line frequency. The second term is commonly known as the ripple power P_{ripple} and it is undesirable since it is the responsible for generating large ripple voltage and ripple currents in the load side [2],[3].
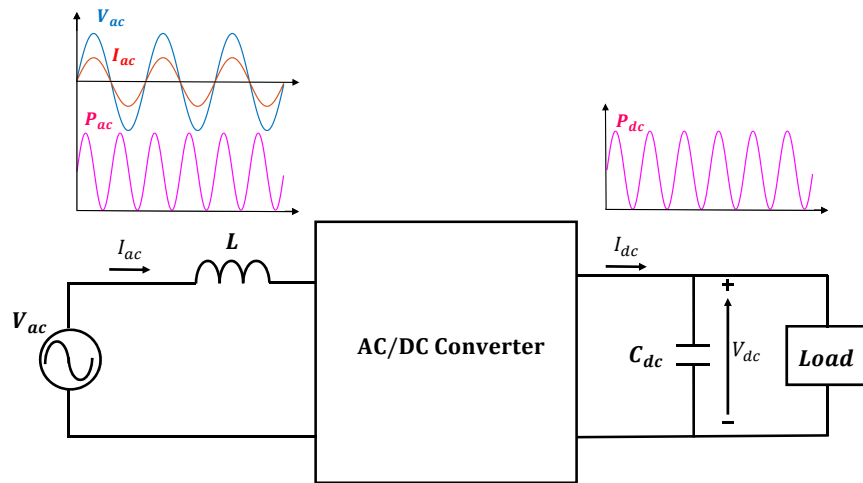
Figure 1-1: Input and output power of a single phase ac-dc converter [4].

For DC systems, the voltage and ripple currents at the DC output are considered as a major power quality issue. If for instance a single stage light-emitting-diode application is considered, the power ripple would cause flicker at twice the line frequency leading to an undesirable visual strain. In the case of PV applications, any variation from the optimum operating point will affect its operation and decrease the efficiency [5]. Also, the performance of batteries and fuel cells can be worsened if large ripple voltage or ripple currents are present. The common way to reduce the low-frequency ripple is to make use of bulky electrolytic capacitors, passive L-C resonant circuits or by placing additional dc-dc stages. They are used as a decoupling capacitor that stores the energy of the ripple power as Fig. 1-2 shows.
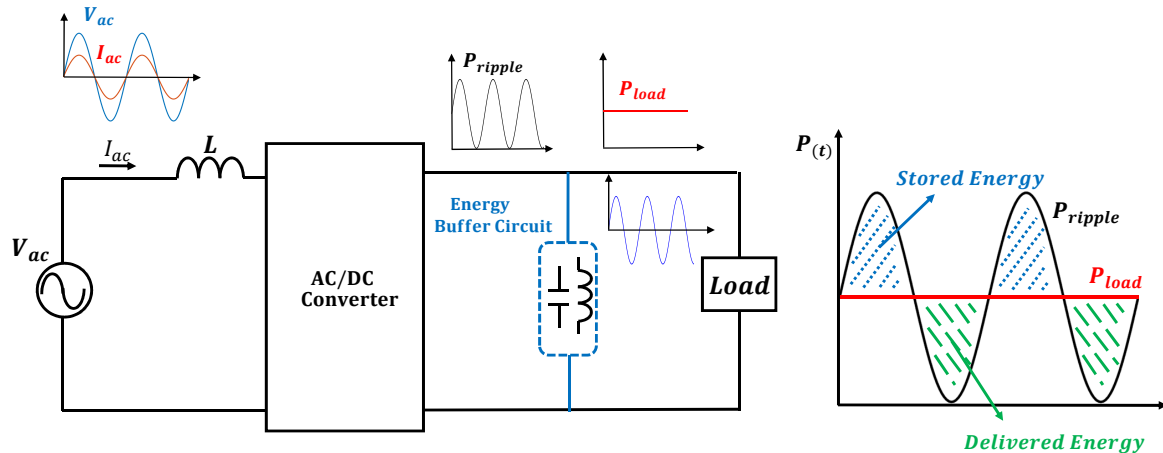
Figure 1-2: Power ripple processed by the decoupling capacitor. [6].

When the ripple power is positive the capacitor is charged, and when the ripple power is negative the capacitor is discharged. In this way the output voltage is smooth and the power going to the load equals the constant power of the input ac source. However, with a large size and a much smaller lifetime than the rest of the system, electrolytic capacitors cannot be considered as an acceptable solution in many applications and new proposals need to be developed. In the next chapter a brief review of the main approaches developed in the literature is addressed. Moreover, this thesis proposes a new control scheme to deal with the low-frequency voltage ripples.

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1.2 Objectives

The objective of this thesis is to provide a new control scheme for a decoupling unit in order to cancel the low frequency ripple voltages that appear in the dc-link capacitors of single phase AC/DC converters. A real decoupling unit will be designed and built with the tools and components available in ITRI's laboratories. The prototype built will be combined and tested with a single phase AC/DC converter and with a standalone mode inverter that are being currently developed by ITRI's work team. Thus, the performance of the new control proposed will be tested and validated.

To achieve the final objective of developing a new decoupling unit the following stages need to be attained:

- Enquire about the previous works proposed through the literature. The operating principles of the proposed topologies and their control schemes must be reviewed and understood.

- Selection of one topology for the decoupling unit to be developed. A detailed analysis of why that topology was selected need to be provided. The analysis need to be supported by PSIM simulations.

- Description of the proposed control scheme. Detailed analysis of how the system works and why is it innovative must be given and supported with PSIM simulations.

- Overview of the components used to build the decoupling unit. Fully description of how to design the magnetic components must be given.

- Identification of the challenges found in the software implementation. This stage shouldn't be focused on the code lines used but on the procedure followed to develop the code.

- Experimental set-up. A set of tests need to be carried out in the laboratory. The results obtained and their difference with the simulations need to be understood and discussed.

1.3 Document flow

This thesis is organized as follows:

- Chapter 2. The state of the art of the active power decoupling methods proposed through the literature is addressed in this chapter.

- Chapter 3. A comparative analysis between the buck, boost and buck-boost converters used as ripple eliminators is provided in this chapter. Their operating principles are described and some PSIM simulations results are discussed. The advantages and disadvantages of each topology are assessed and the motivation to use a boost converter in the proposed decoupling unit is justified.

- Chapter 4. The concept of the Universal Power Decoupling Unit is introduced in this chapter. A detail analysis of the new control proposed is provided and some PSIM simulation results are presented and discussed.

- Chapter 5. The design procedure of the inductor used in the proposed decoupling circuit is fully detailed in this chapter. The components used to make-up the decoupling unit are also presented and their selection is justified.

- Chapter 6. This chapter provides a glance of the challenges found when programming the code of the decoupling unit. The programming procedure and the test developed to check the code are also presented in this chapter.

- Chapter 7. The tests carried out to check the performance of the proposed decoupling unit are presented in this chapter. First, the performance of the proposed decoupling unit combined with a single phase AC/DC converter is evaluated. Then, a brief understanding of the power decoupling principle in standalone mode inverters is provided. The improvements introduced by the proposed decoupling unit to the standalone mode inverter are also discussed in this chapter.

- Chapter 8. The conclusions and possible future developments are drawn in this chapter.

Chapter 2

State of the art

The issue of the power ripple at twice the line frequency in single-phase systems was introduced in Chapter 1. To deal with this problem it is common to use a capacitor in the dc link able to balance the instantaneous power difference between the input and output of the converter. Usually, the capacitor used to buffer the undesired power ripple is a bulky electrolytic capacitor. However, with a high series resistance (ESR) and a short lifetime (even worsened by the voltage and current ripples), electrolytic capacitors are not a practical solution in many applications. Ceramic and film capacitors have a much better performance in terms of energy density, reliability and ripple current capability. Fig. 2-1 shows a performance comparison of electrolytic, film and ceramic capacitors and it also shows the relation between ripple current rating and capacitance required for high and low ripple current applications [7].
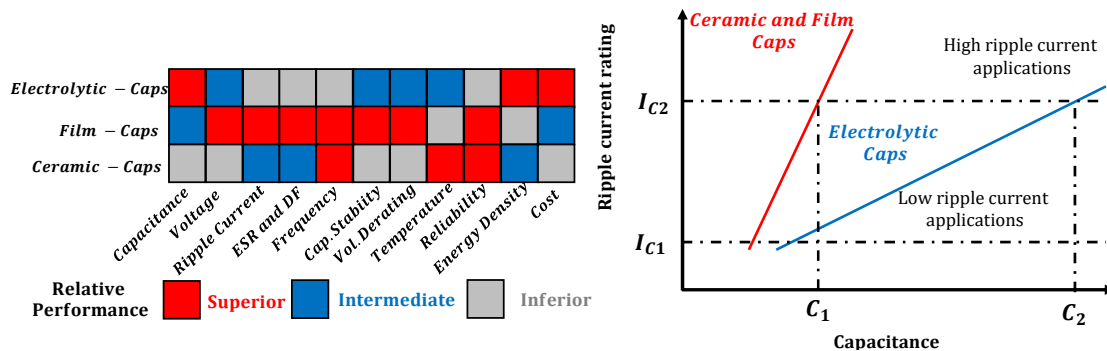
Figure 2-1: Performance comparison of electrolytic, film and ceramic capacitors [7].

As it can be seen, with a well-balanced performance and a smaller capacitance requirement in both low and high ripple current applications, film capacitors give a more cost-effective and compact structure. It is therefore interesting to find new solutions able to reduce the energy storage requirement in the dc link so that electrolytic capacitors can be replaced by film capacitors [7]. In the literature several topologies have been proposed to cope with this problem, all of them following the active power decoupling method. Their basic principles and achieved results are reviewed in this chapter.

2.1 Active power decoupling method: topology review

The main objective of the active power decoupling method is to divert the ripple power to another energy storage device with lower size and longer lifetime such as a film capacitor [8]. By doing so, the performance of the converter is improved and its life is expanded. However, extra circuitry wich involve power losses and costs is required. Fig. 2-2 shows the basic idea of the active power decoupling method.
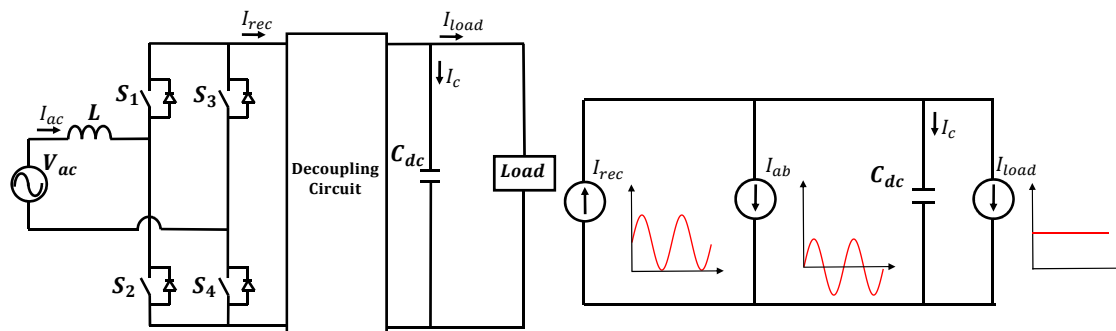
Figure 2-2: Basic idea of the active power decoupling method. [8].

As it can be seen, a constant load current can be achieved if all the ripple current is absorbed by the decoupling circuit. The single phase converter can be a voltage-source converter (VSC) or a current source converter (CSC). Generally, if it is a VSC type the decoupling circuit is connected in parallel and in case of the CSC type the

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decoupling circuit is connected in series. However, this is not always the case and some alternative configurations can be found in the literature. In [9] an off-line LED electronic driver based on a bidirectional series converter was proposed. The decoupling circuit was connected in series with the LEDs assembly and the low frequency ripples that appear in the dc-link were effectively reduced, ensuring thus a DC constant current through the LEDs. In [10] another LED driver able to provide a smooth LED current was proposed. They made used of an optimized cascade structure to compensate the low frequency ripple at the system output. For simplicity purposes, only the single-phase VSC with the decoupling circuit connected in parallel is considered in this thesis.

Decoupling circuits can be classified as capacitive or inductive energy storage circuits. In the first case the energy is stored in the electrostatic field of a capacitor while in the second case it is stored in the electromagnetic field of an inductor [8]. In both cases decoupling of the pulsating power can be effectively achieved. However, it is usually preferable to use capacitors since they have lower weight and higher power density. The most relevant topologies proposed in the literature for each of the cases will be reviewed below.

2.1.1   Capacitive Energy Storage Decoupling Circuits

Fig. 2-3 shows three different solutions that make use of a bidirectional dc-dc converter as the energy storage circuit connected at the dc side of the single-phase converter [3], [11], [12]. The operating principle of all of them is very similar but their achieved results differ a little bit. In this section a brief understanding of their operation will be addressed and a detailed analysis between the three circuits will be carried out in the next chapter.

A bidirectional buck, boost and buck-boost converters were proposed as an auxiliary ripple energy storage circuit to effectively suppress the ripple voltage and therefore reduce the converter energy storage capacitance [3]. When the ripple current is pos-
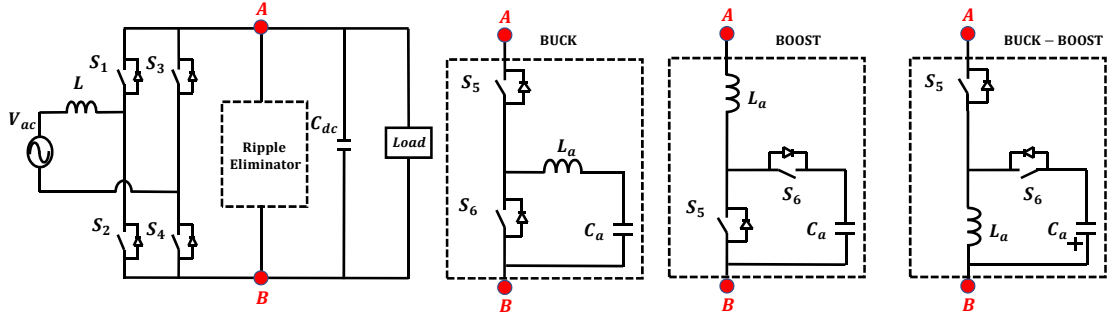
Figure 2-3: Active decoupling circuit based on a bidirectional dc-dc converter (buck, boost and buck-boost). [3], [11], [12].

itive the energy is stored in the auxiliary capacitor, and when the ripple current is negative the auxiliary capacitor releases its energy to the load. The dc-dc converter can be operated in continuous conduction mode (CCM) or in discontinuous conduction mode (DCM) depending on the control strategy pursued. In both cases, the current flowing trough the load has only a dc component and the ripple voltage is considerably reduced. It should be noted that the voltage of the auxiliary capacitor is usually controlled to be a rectified sinusoidal which involves complex control and high-order harmonics. This can be solved by adding an offset to the capacitor reference voltage. However, this means that the capacitor voltage will never drop to zero and therefore is neither fully charge nor fully discharge thus wasting its capabilities [13].

Fig. 2-4 shows another topology based on capacitive energy storage devices [14]. In this case, the circuit consists of an additional leg in the dc side, two filter inductors and two filter capacitors in the ac side. By properly controlling the six switches, the ripple energy in the dc side is transferred and stored to the input capacitors.
In principle, the reference voltage in this case is not a rectified waveform and therefore the fully capacitance is used [13]. However, the results seen in [14] show that the voltages in the input capacitors are very distorted, leading to current stresses in the rectifier legs. Nevertheless, the ripple current is reduced 10 times and the input ac voltage is not affected ensuring unity power factor.
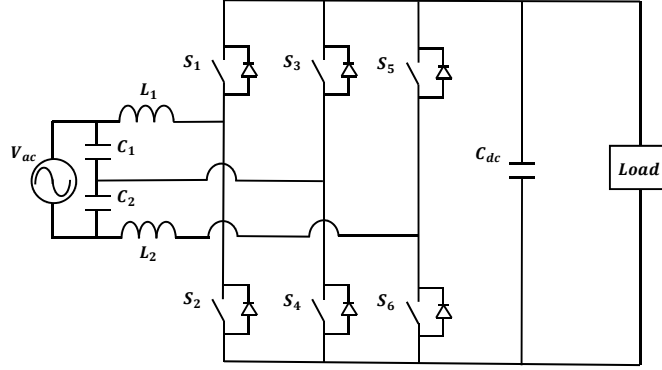
Figure 2-4: Active power decoupling circuit based on two input filter inductor, two input filter capacitors and an additional leg. [14].

In [13] the topology shown in Fig. 2-5 was proposed. It can be considered as a three-phase unbalanced system in which a series capacitor and a smoothing inductor is used to store the power unbalance. Compared with previous topologies, the reference voltage is a pure sinusoidal wave that ensures a complete charge and discharge of the capacitor. It should be noted that even if the phase-B current is affected by the compensating current i_c, the grid current is not affected allowing low stresses on the power devices. However, a complex control with low bandwidth is required. Thus, this topology is adequate for high-power applications with low switching frequency such as railway traction drives but it could have worst performance than the topologies seen before for low power applications.
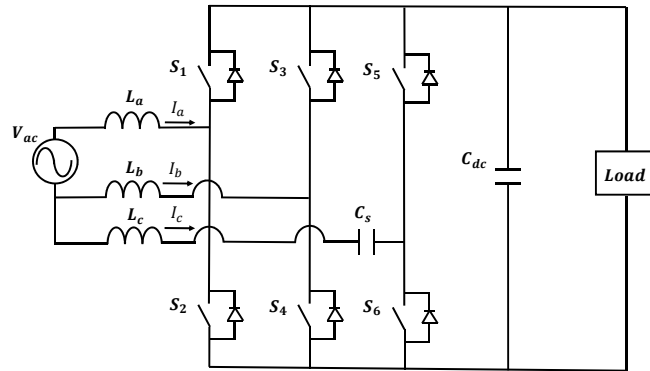
Figure 2-5: Active power decoupling circuit based on a third leg, an energy-storage capacitor and a smoothing inductor. [13].

Another topology based on a symmetrical half-bridge circuit that uses the dc-link capacitors to absorb the ripple power was proposed in [15]. Fig. 5-5 shows the circuit proposed. Only a couple of switches and a smoothing inductor are added to the circuit. The capacitor voltages are controlled to be sinusoidal ensuring their maximum utilization.
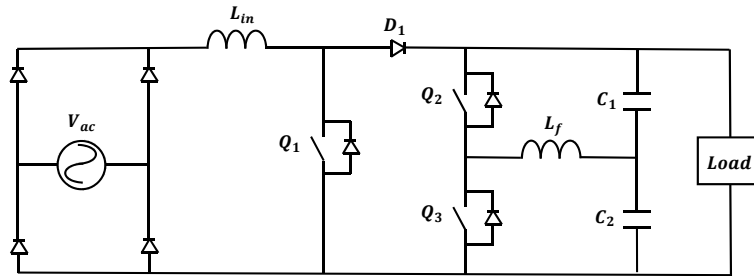
Figure 2-6: Active power decoupling circuit based on a half-bridge cell [15].

As it happened with the previous topologies, by properly switching Q_2 and Q_3, the ripple power is absorbed by the dc link capacitors. The main drawback of this topology is the efficiency drop caused by the additional leg (2.3%) and its main advantage is the dc link capacitor reduction (about 10 times smaller) compared with the passive filter solution (use of a electrolytic capacitor). Moreover, the authors in [15] stated that their half bridge cell could be used in neutral point-clamped (NPC) converters and modular multilevel converters (MMCs) to absorb the ac-side harmonics and reduce the bulky electrolytic capacitors respectively. However, this possibility is still under discussion and more studies should be carried out.

2.1.2 Inductive Energy Storage Decoupling Circuits

The need for effective railway operation between countries with different supply voltage and frequency was the main motivation that prompted the authors in [16] to develop the circuit shown in Fig. 2-7. Their idea was to pass from the use of a bulky electrolytic capacitor to use an active filter able to operate on both 16 2/3Hz, 15kV and 50Hz, 25kV with a unique configuration and only changing the control of the converter.
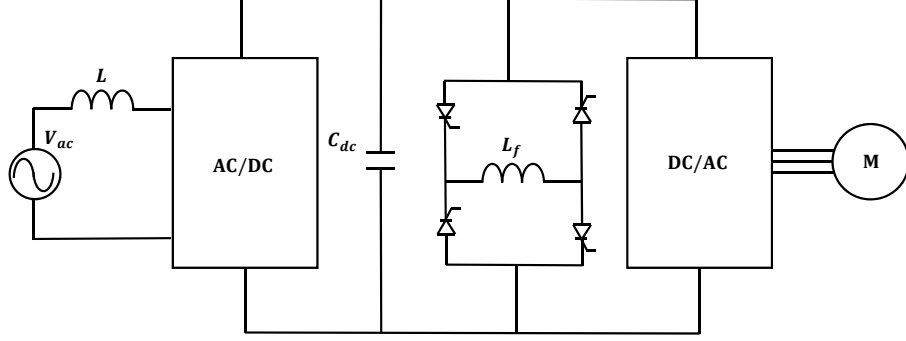
Figure 2-7: Active power decoupling circuit based on a energy storage inductor and four GTOs. [16].

Similarly to the previous topologies, the dc link voltage is kept constant but in this case the ripple power is absorbed by the filter inductor L_f. When the ripple power is positive the GTOs are controlled in order to transfer the energy from the DC link to the filter inductor, and vice-versa in the case of a negative ripple power. To achieve proper operation with two different frequencies, a tolerance band current control based on the derivative of the filter inductor current was proposed. The peak value of the filter inductor current and its derivative value are given by (2.1) and (2.2) respectively.

$$i_{Lpeak} = \sqrt{\frac{2V_{dc}I_{Load}}{\omega L_f}\alpha}; \quad \alpha = \text{security margin factor} \tag{2.1}$$

$$\left|\frac{di_L}{dt}\right| = \frac{V_{dc}}{L_f} \tag{2.2}$$

As it can be seen there is a trade-off, if the filter inductor is decreased, an easier control (high current derivative allows simpler control) is achieved but the inductor peak current is also increased. This problem could be solved by having a variable inductance with a tap changer. However, simplicity is lost and the cost is increased. The authors in [16] stated that their topology is cheaper and more reliable than the electrolytic capacitor, but still with a considerable cost. However, this paper was proposed a long time ago and the GTOs could be changed by new solid state self commutating devices such as IGBTs, reducing thus the price of the converter.

Another decoupling circuit that converts the ripple energy into magnetic energy of an inductor was proposed in [17]. Fig. 2-8(a) shows the topology proposed. Small number of components (two switches and one inductor) are required in this case compared to other topologies. However, the control of the active filter is combined with that of the PWM rectifier, thus involving a high level of complexity.
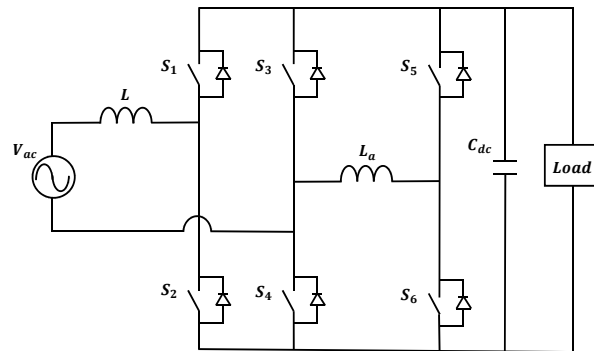
(a)
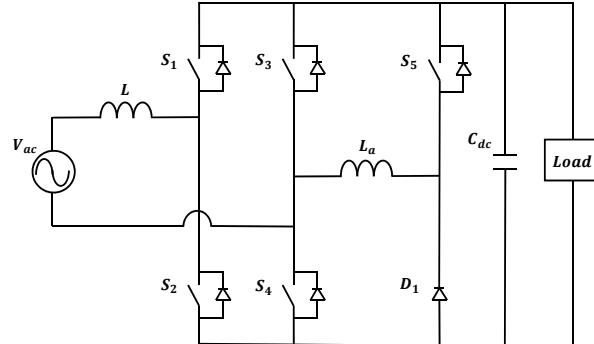
(b)

Figure 2-8: (a) Active power decoupling circuit based on two switches and a smoothing inductor. (b) Improved version with one diode. [17],[6]

For the topology shown in Fig. 2-8(a) two control methods were proposed in [17] being one of them able to effectively eliminate all the ripple current. An improved version of this converter was proposed in [6] and is presented in Fig. 2-8(b). In this case, the use of the bottom switch is saved and it is replaced by a diode. A simple control strategy was proposed and the dc link capacitor was reduced 10 times.

This chapter reviews some of the different topologies that are able to cope with the low frequency ripple voltages at the system output. It has been seen how both capacitive and inductive solutions can reduce the dc-link capacitance requirement allowing the use of small film capacitors. However, with a lower weight and higher power density, the decoupling circuits based on the capacitive energy storage are preferred in this thesis. Within the different topologies that use a capacitor to store the ripple energy, the ripple eliminators proposed in [3], [11] and [12] are the ones providing the highest capacitance reduction and therefore the ones preferred for the UPDU proposed in this thesis. A comparative analysis between the three of them will be carried out in the next chapter.

Chapter 3

Comparative analysis between buck, boost and buck-boost converters used as ripple energy storage circuits

As it was stated in the objectives, the purpose of this thesis is to provide a universal power decoupling unit based on one of the ripple energy storage circuits proposed in [3], [11] and [12]. Since each of the circuits has different features that make them more or less attractive, it is the aim of this chapter to go through the pros and cons of each of the three topologies so the one giving the best cost-effective solution can be selected and used in the universal power decoupling unit.

This chapter is arranged as follows: first the operation and control scheme of each topology is studied and then some simulation results are compared and discussed.

3.1 Operation principle and control scheme

As it was explained in the previous chapter, the main objective of the ripple eliminator is to divert the ripple power to an auxiliary capacitor making use of an additional pair of switches and an energy transfer inductor. To do so, three different topologies

have been proposed in [3], [11] and [12] as Fig. 3-1 shows.
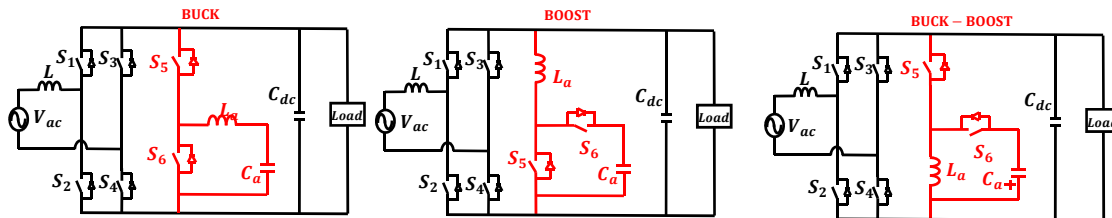
Figure 3-1: Topologies proposed to act as a ripple eliminator. [3], [11], [12].

The fundamental operation and control scheme of the three topologies is very similar and for this reason this chapter will focus on the performance of the boost converter but taking especial attention to the differences with the buck and buck-boost converters.

The PWM rectifier is used to control the dc bus voltage while the ripple eliminator is used to control the undesired pulsating power. Thus, S_5 and S_6 must be controlled to ensure that all the ripple energy is transferred to the auxiliary capacitor so only a high switching frequency component flows to the dc bus, allowing thus the use of a small film capacitor. Two control strategies can be pursued: instantaneous current control in CCM or average current control in DCM. In the first case the switches are controlled in complementary mode while in the second case only one of the switches is controlled during each half cycle of the ripple current ($i_{ripple} > 0$, S_5 on and S_6 off; $i_{ripple} < 0$, S_5 off and S_6 on) [11]. Both strategies have some pros and cons. If CCM operation is pursued, instantaneous tracking is achieved which in principle should provide a better performance than the average current control. However, the auxiliary inductor must be large enough to keep the ripple current continuous. In case DCM operation is chosen, a much smaller inductor can be used but a higher peak current will flow through the inductor and therefore through the power switches. However, the duty cycle needed to control the power switches can be easily calculated and there is no need to use a current controller as it will be seen later in this section [12].

The authors in [11] used CCM operation while the authors in [3] and [12] followed the DCM control strategy. To perform the comparative analysis DCM operation was

chosen and [12] was used as the main guideline to state equations of the three topologies. Fig. 3-2 shows the operation modes of the bidirectional boost converter used as the ripple eliminator circuit.
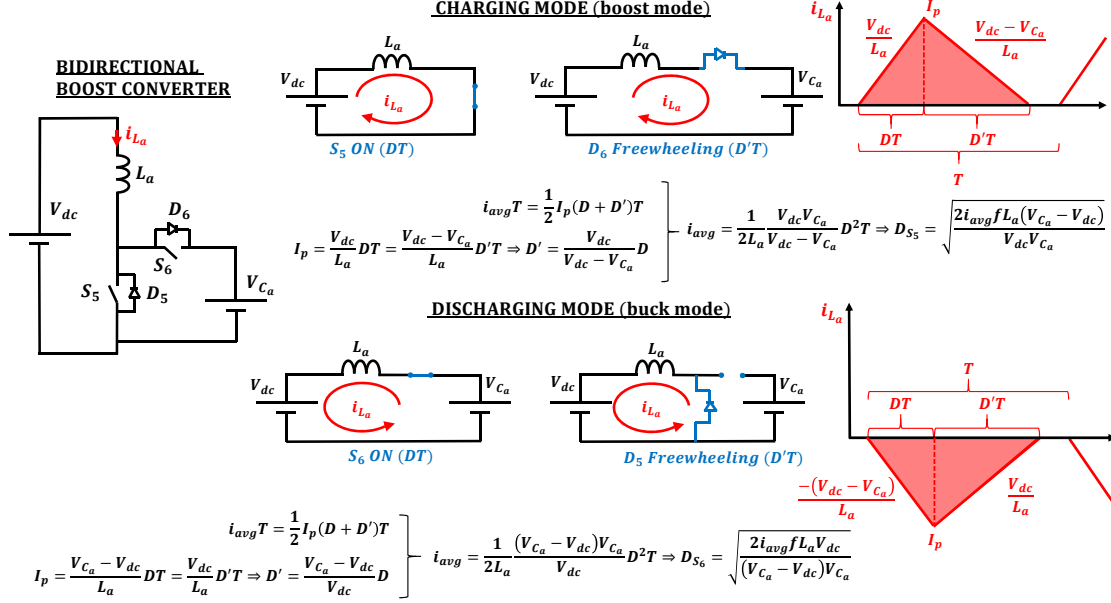
Figure 3-2: Operation modes of the bidirectional boost converter as the ripple eliminator circuit.

The following discussion considers positive current ripple with the references of Fig. 3-2. For negative current ripple, analogue conclusions can be derived, changing the current signs in the discussion. For positive current, the energy must be transferred from the dc bus C_{dc} to the auxiliary capacitor C_a. Thus, C_a is being continuously charged and discharged and therefore two modes can be distinguished: the charging mode and the discharging mode. During the charging mode the converter is operated in boost mode and S_6 is always turned off. Firstly S_5 is turned on and the energy is absorbed by the auxiliary inductor and then S_5 is turned off and D_6 is freewheeling so the inductor can release its energy to the auxiliary capacitor. In the discharging mode the reverse process occurs. The converter operates in buck mode having S_5 always turned off. In this case the energy is firstly transferred from the auxiliary capacitor to the dc bus (S_6 on) and then the auxiliary inductor releases its energy to the dc bus (D_5 freewheeling).

Fig. 3-2 shows the inductor current during both the charging and discharging modes. As it can be seen, the inductor releases all its energy during each switching cycle thus ensuring DCM operation. It should be noted as well that the switching frequency is much higher than that of the ripple current (120Hz) and therefore the auxiliary inductor can be considered linearly charging and discharging during each switching cycle [3].

The control objective is to make the average current of the inductor current equal to the reference ripple current when there is energy being absorbed/injected from/to the dc bus (shaded triangular area) [3]. By doing so, the duty cycle of switches S_5 and S_6 can be directly calculated and ripple current compensation can be effectively achieved. Fig. 3-2 shows how to get the average current equations and therefore the duty cycles from the inductor current waveform. As it can be seen by replacing i_{avg} by the reference ripple current, the gate signals for the power switches can be straightly obtained.

The same procedure seen for the boost converter applies for the buck and buck-boost converters. Fig. 3-3 and Fig.3-4 show the operation modes of the buck and buck-boost converters respectively. Two things should be noted:

1. The auxiliary capacitor voltage in the boost converter must be greater than that of the dc bus whereas in the buck case it must be smaller and in the buck-boost converter it can be both greater or smaller. The stored ripple energy E_r of the auxiliary capacitor is given by:

$$E_r = \frac{1}{2} C_a V_{C_a dc}{}^2 \tag{3.1}$$

   where $V_{C_a dc}$ is the dc component of the auxiliary capacitor voltage. Thus, with a higher $V_{C_a dc}$, boost and buck-boost converter can have a smaller auxiliary capacitor [12].

2. The shaded triangular area in both buck and buck-boost converter does not cover the full inductor current waveform because during some intervals of the

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switching cycle there is no energy absorbed/injected from/to the dc bus. It is not relevant but it should be taken into account to calculate the duty cycles.
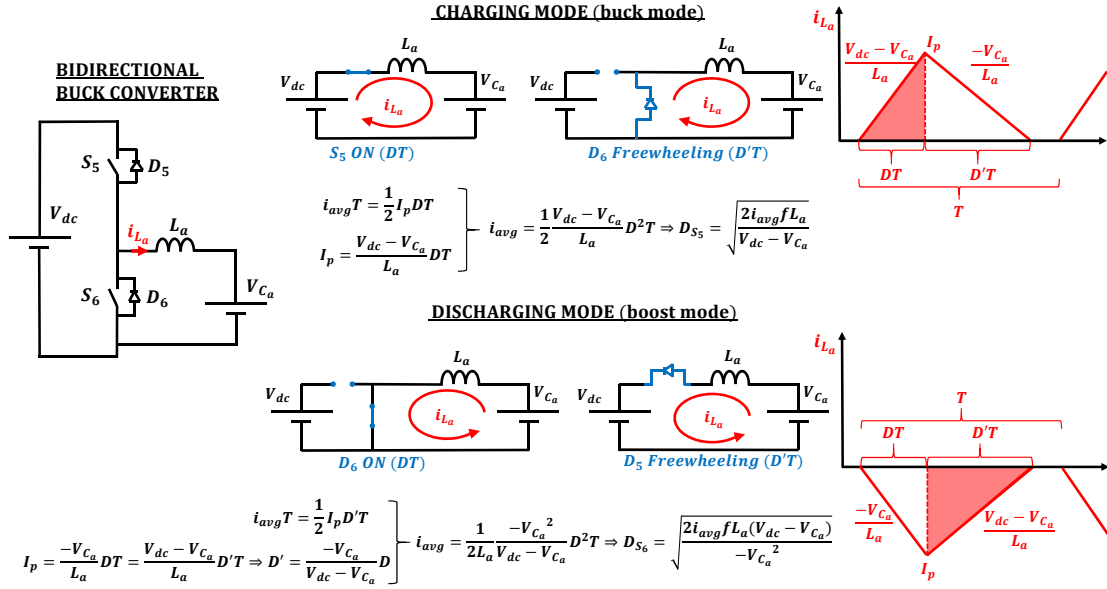
Figure 3-3: Operation modes of the bidirectional buck converter as the ripple eliminator circuit.
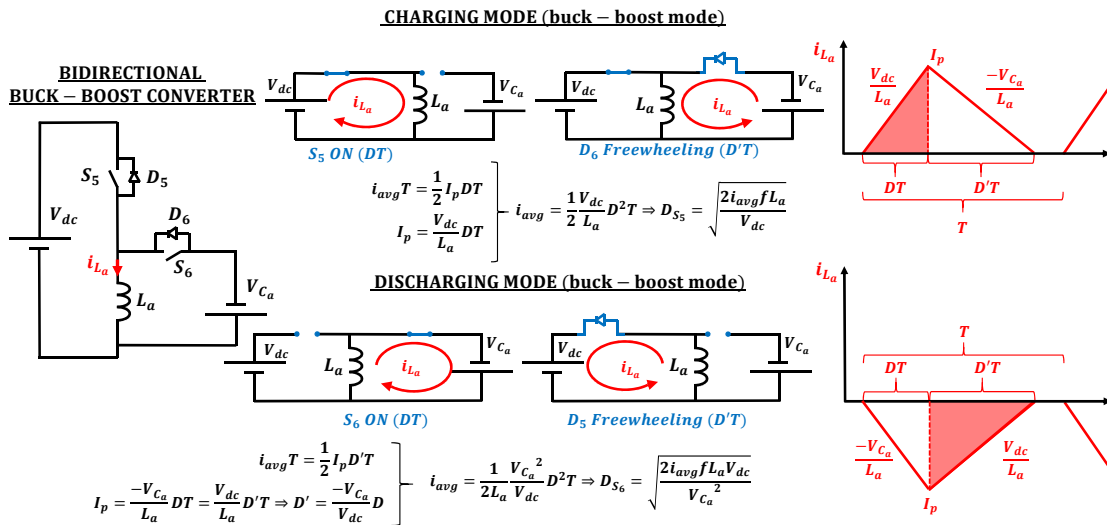
Figure 3-4: Operation modes of the bidirectional buck-boost converter as the ripple eliminator circuit.

Once the operation modes and duty cycle calculations of the boost converter have been understood, the control scheme of the whole system can be sketched. Fig. 3-5 shows the control diagram of both the PWM rectifier and the bidirectional boost converter.
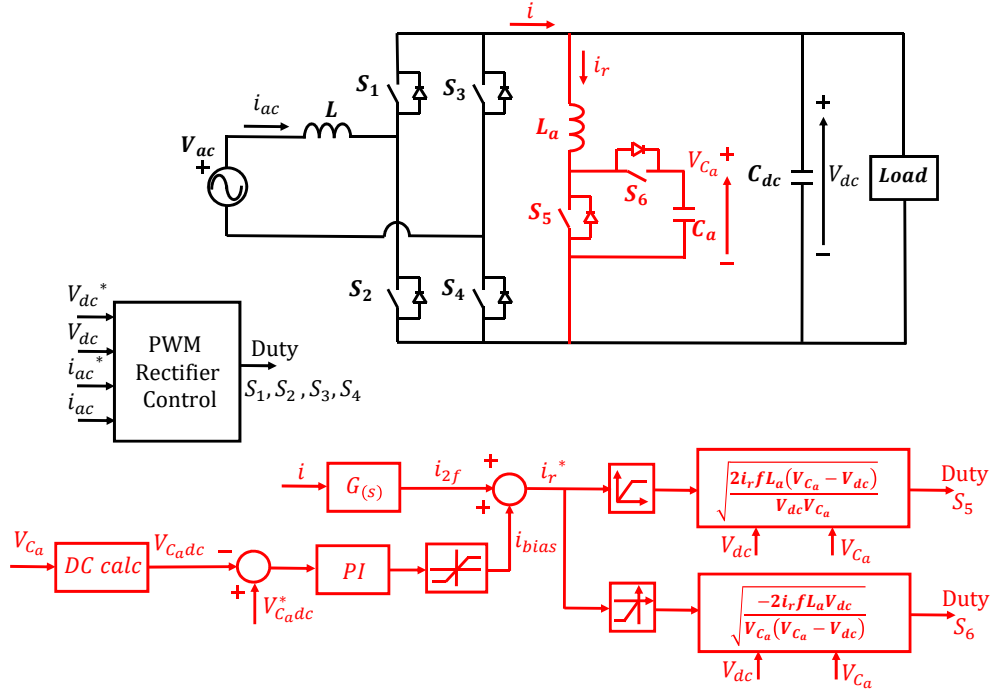
Figure 3-5: Control diagram of the PWM rectifier and the bidirectional boost converter.

The PWM rectifier control scheme cannot be fully detailed in this thesis due to intellectual property rights issues. It is a cascaded control with an outer voltage loop for the dc bus capacitor voltage V_{dc} and an inner current loop for the input inductor current i_{ac}. Once the duty signal is obtained it is compared with a carrier triangular waveform in order to get the PWM signals of switches $S_1 - S_4$.

In the case of the ripple eliminator, the rectified current is sensed and passed through a second order band-pass filter to obtain its second order harmonic component i_{2f}. The equation of the band-pass filer is is given by

$$G_{(s)} = \frac{kBs}{s^2 + Bs + \omega_0{}^2}; \quad f_0 = \frac{\omega_0}{2\pi}; \quad f_b = \frac{B}{2\pi} \tag{3.2}$$

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where f_0 is the center frequency and f_b is the frequency width of the passing band. To ensure a stable auxiliary capacitor voltage its dc component $V_{C_a dc}$ must be controlled. Thus, $V_{C_a dc}$ is firstly calculated and compared with the reference. The error is sent to a PI controller whose output signal can be considered as the dc bias current (i_{bias}) required to charge the auxiliary capacitor [12]. It should be noted that in [12] the dc component was obtained with a hold filter while in this case it was calculated through a C block in PSIM. Once the reference ripple current $i_r{}^*$ is obtained, its sign is evaluated to determine the converter's operation mode. Then, the duty cycles for switches S_5 and S_6 are directly calculated by making use of the equations developed in Fig. 3-2. In the same way as in the PWM rectifier, the duty cycles are compared with a carrier triangular waveform to obtain the gate signals.

The control scheme of the buck and buck-boost converters is exactly the same as the one of the boost converter being the only difference the equations used for the duty cycles calculation.

3.2   Simulation Results and Discussion

Some simulations were carried out in PSIM to verify the performance of the proposed ripple eliminators. It is not the purpose of this chapter to develop a detailed analysis on how to design and select the converter parameters. Thus, the parameters proposed in [12] which are summarized in Table 3.1 were used to carry out the PSIM simulations.

As it can be seen, the system under study is a 1-kW prototype with a supply frequency of 50 Hz. This means that the undesired pulsating power should appear at 100 Hz. To control the PWM rectifier seen in Fig. 3-5, per unit (p.u) system was used being the base voltage 800 V and the base current 100 A (arbitrarily selected). The time constant and proportional gain of the PI voltage and current controllers are summarized in Table 3.2.

Table 3.1: Parameters of the PWM rectifier and ripple eliminators under study [12].

Parameters	Values
Supply voltage (RMS)	230 V
Supply frequency f	50 Hz
Switching frequency of the PWM-controlled rectifier	10 kHz
Switching frequency of the ripple eliminator	18 kHz
AC-side inductor L	2,2 mH
DC-bus capacitance C_{dc}	110 μF
DC-bus voltage V_{DC}	400 V
Rectifier load (resitor R_o)	170 Ω
Auxiliary inductance L_a	0,55 mH
Auxiliary capacitance C_a	165 μF

Table 3.2: Proportional gain and time constant of the PI controllers.

		PWM Rectifier (Vpu = 800 V, Ipu = 100 A)	Ripple Eliminator
Voltage Controller	Kp	0,29	0,01
	Ti	0,015	0,02
Current Controller	Kp	3	-
	Ti	0,0003	-

For the PWM rectifier, the tuning of the current PI controller was started by applying zero-pole cancellation and the voltage PI controller was tuned to be at least 4 times slower. Then, some tuning through trial and error was carried out to improve the performance of the system. In the case of the ripple eliminator, the values proposed in [12] were used in the simulations.

The parameters shown in Tables 3.1 and 3.2 are valid for the three ripple eliminators under study. Following the same procedure of the previous section, the performance of the boost converter will be firstly demonstrated and then the main differences with the buck and buck-boost converters will be discussed.

3.2.1 Simulation results of the boost converter used as the ripple eliminator in DCM

To prove the operation of the boost converter, one simulation was carried out considering steady state condition (dc capacitor charged to 400V and auxiliary capacitor charged to 600V) and activating the ripple eliminator in $t = 0.2$ seconds. Fig 3-6 shows the input ac current i_{ac}, the output dc voltage V_{dc} and the voltage of the auxiliary capacitor V_{Ca} while Fig. 3-7 shows the rectified current i; its second order harmonic component i_{100Hz}; the gate signals for switches $S5$ and $S6$; the auxiliary capacitor voltage and auxiliary inductor current i_{La}.

As it can be seen, the PWM rectifier is able to control the dc bus voltage at 400V, but, since a small film capacitor ($C_{dc} = 110\mu F$) was used, a ripple voltage equal to 68.37V (17.1% of the total volage) is present. It should be noted as well that the ripple power also affects the input current making it to be distorted and with a quite poor total harmonic distortion ($THD = 17.9\%$). In $t = 0.2$ seconds, the ripple eliminator starts to operate. When i_{100Hz} is positive, S_5 is controlled and the capacitor is charged, and when i_{100Hz} is negative, S_6 is controlled and the capacitor is discharged. In Fig. 3-7 it can be noted how the inductor current is fully charged and discharged during each switching cycle ensuring thus DCM operation. Once steady state is reached, the ripple eliminator is able to reduce the dc bus voltage ripple to 3.08V (0.77% of the total dc bus voltage) and the THD current is improved to 13%.

Fig. 3-8 shows the Fast Fourier Transform (FFT) analysis of the dc bus current. As it can be seen, before the ripple eliminator is activated, there is a low frequency component in the dc bus current, but, once the compensation is achieved, there is only a high switching frequency component. Thus, a small film capacitor able to filter this component can be placed in the dc bus.
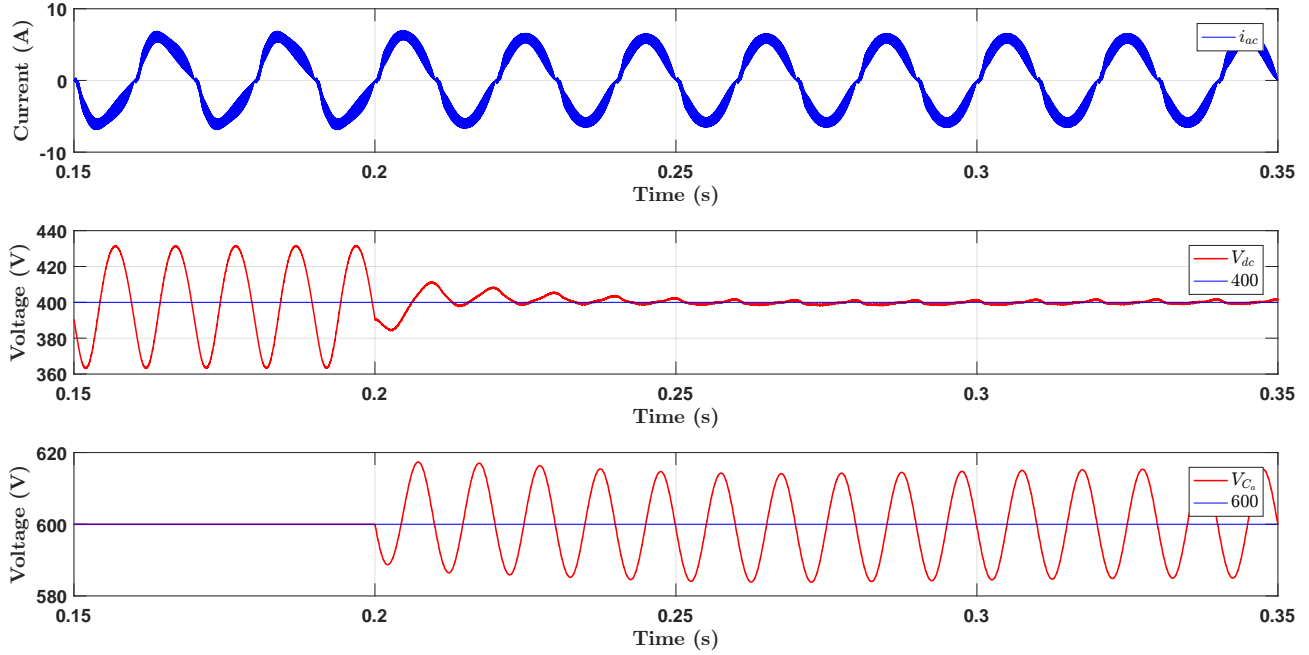
Figure 3-6: Input ac current, output dc voltage and voltage of the auxiliary capacitor when the boost converter used as the ripple eliminator is activated in $t = 0.2$ seconds.
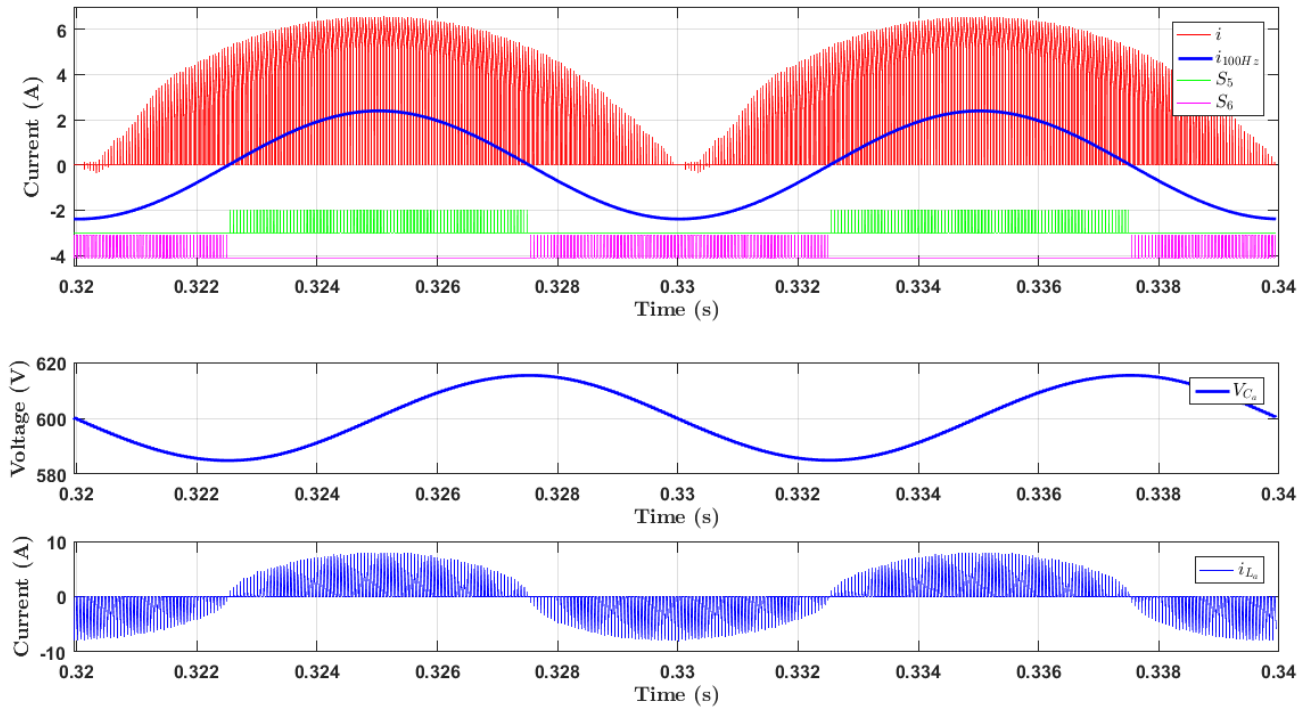
Figure 3-7: Rectified current and its second order harmonic component, gates signals for switches S_5 and S_6, auxiliary capacitor voltage and auxiliary inductor current of the boost converter under normal operation.

44
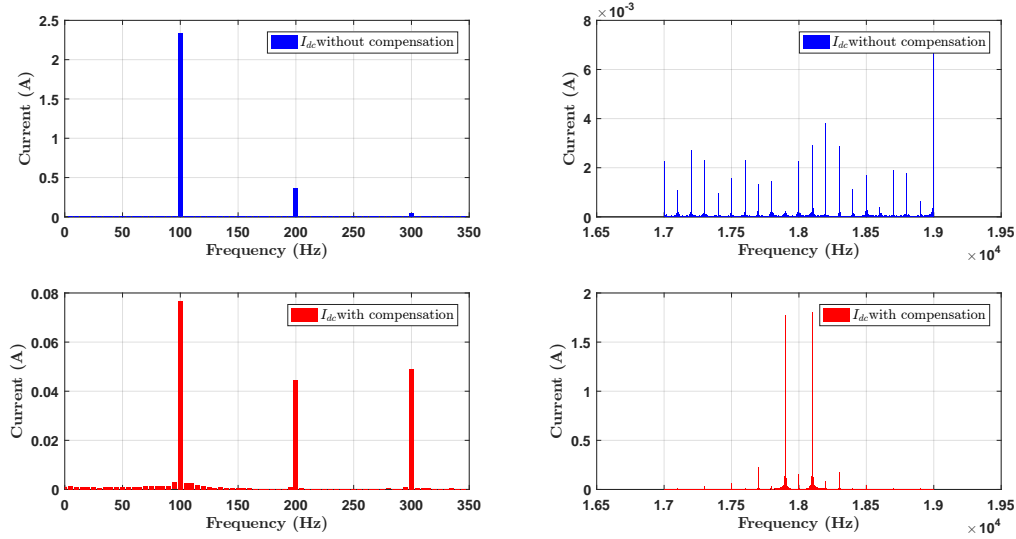
Figure 3-8: FFT of the dc bus current with and without compensation of the power ripple.

The performance of the bidirectional boost converter used to absorb the power ripple has been proven. If the same ripple ratio wants to be achieved with an electrolytic capacitor, the required capacitance would be 18 times bigger ($C_{dc} = 1.98mF$). This involves a much higher volume and lower lifetime. Nothing comes for free, however, and the system losses are increased which involve lower efficiency and bigger heat sink. Nevertheless, the overall improvement is considerable and the use of a ripple eliminator is justified.

3.3   Performance difference between buck, boost and buck-boost converters.

Two simulations were carried out to see the performance of the buck and buck-boost converters. Since the buck converter is a step-down converter, V_{C_a} must be lower than V_{dc}. In the case of the buck-boost converter, V_{C_a} can be bigger or smaller V_{dc}. With 400 V in the dc-link, a V_{C_a} equal to 300 V and 600 V was used for simulating the buck and buck-boost converters respectively. Fig. 3-9 shows the dc-link voltage and the auxiliary capacitor's voltage for the three converters.

45
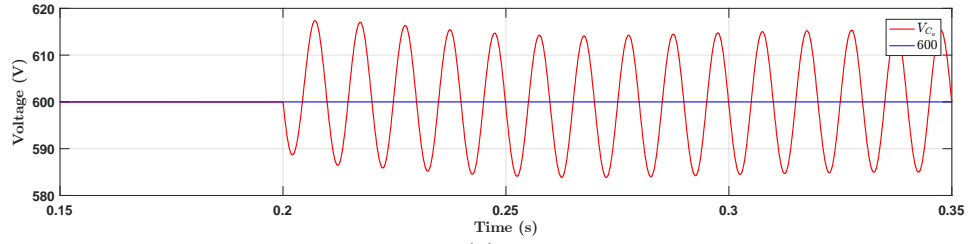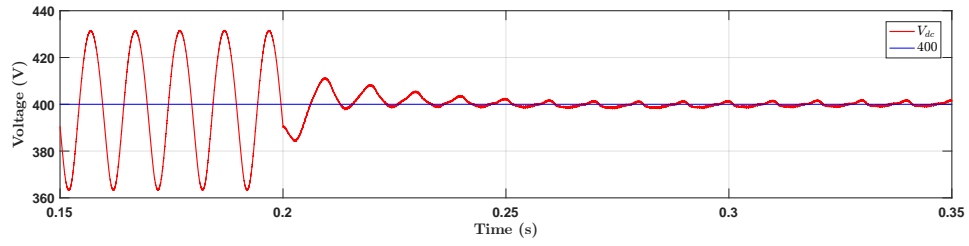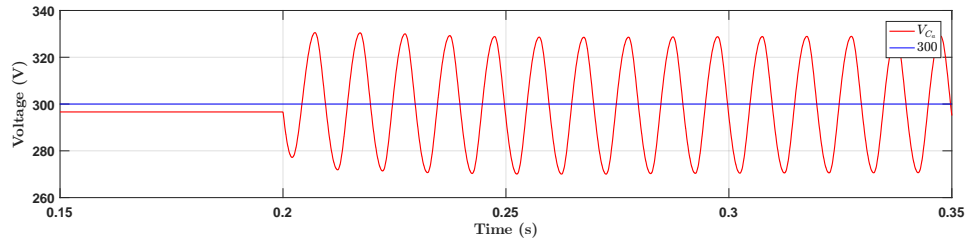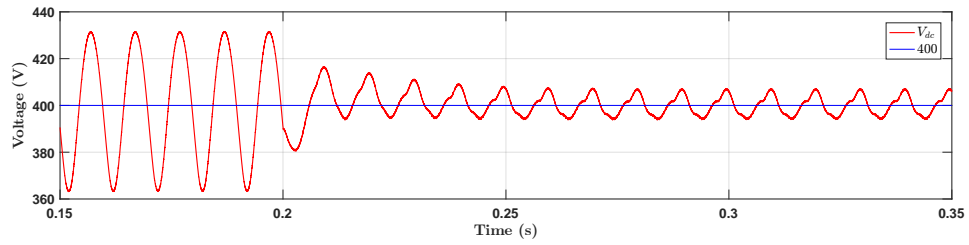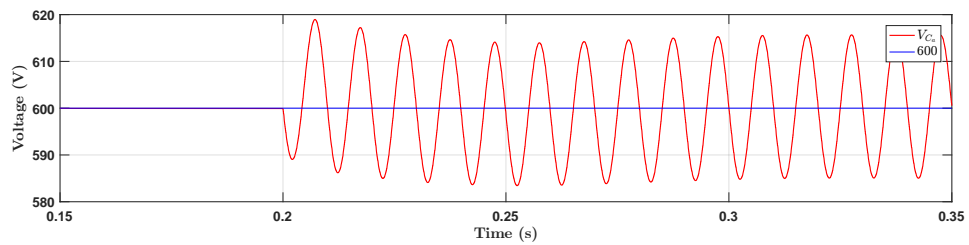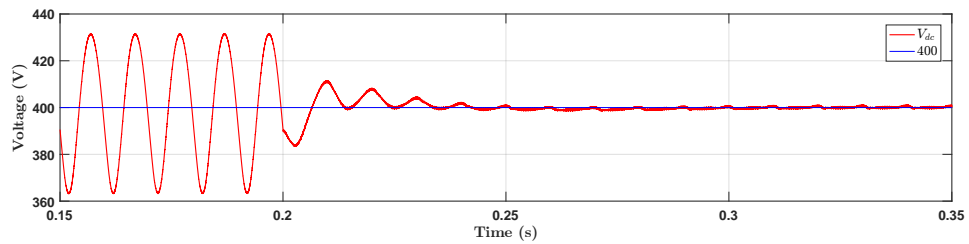
Figure 3-9: V_{dc} and V_{Ca} when the (a)boost, (b)buck, (c)buck-boost converter used as the ripple eliminator is activated in $t = 0.2$ seconds.

Three facts can be noted.

1. The three converters can significantly reduce the dc bus ripple voltage.

2. With a ripple voltage equal to 1.76V, the buck-boost converter is the one giving the greatest ripple voltage reduction (buck = 13.21V, boost = 3.08V).

3. The ripple voltage in the auxiliary capacitor for the boost and buck-boost converters is almost half of the one for the buck converter.

2 and 3 can be explained with the equation of the ripple energy seen below [11].

$$E_r \approx C_a V_{C_a dc} \Delta V_{C_a} \tag{3.3}$$

For the same auxiliary capacitance value, the higher is $V_{C_a dc}$, the higher is the ripple energy that can be absorbed by the capacitor and the lower is the ripple voltage. To prove (3.3), some simulations were carried out in PSIM keeping $C_a = 165 \mu F$ and changing V_{C_a-dc} between 500V and 800V. Fig. 3-10 shows the results obtained.
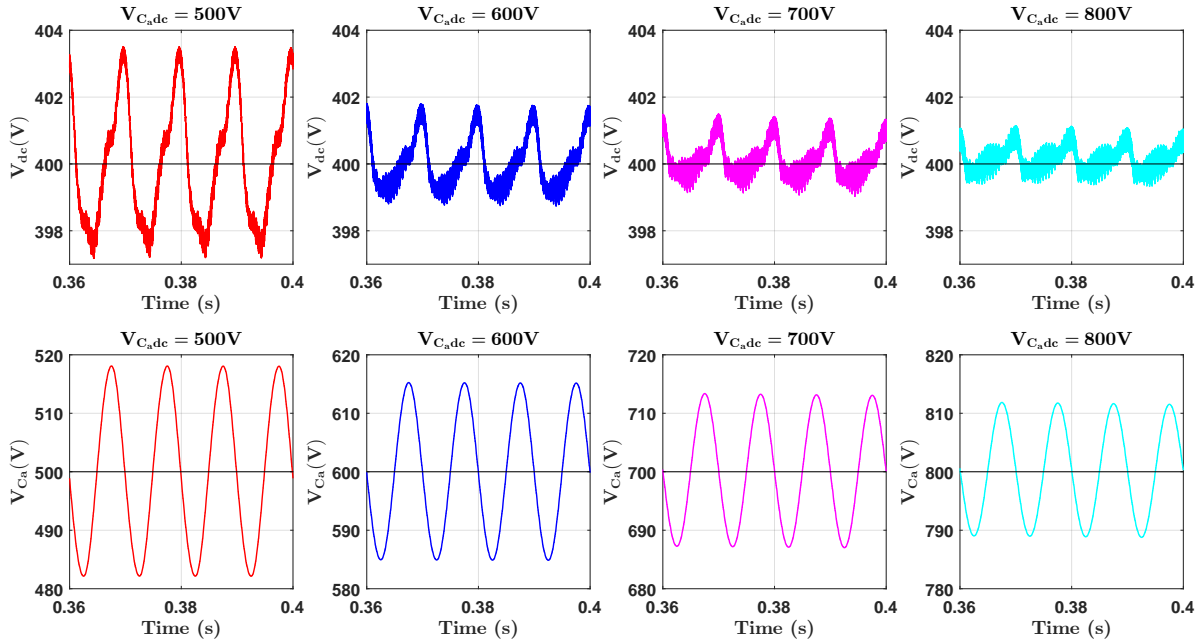
Figure 3-10: Dc bus volatage V_{dc} and auxiliary capacitor's voltage V_{Ca} of the boost converter when C_a is equal to $165 \mu F$ and $V_{C_a dc}$ is changed between 500V and 800V.

As expected, the higher is V_{C_adc}, the lower are the voltage ripple of the auxiliary and dc capacitors. Thus, in principle, boost and buck-boost converter are preferred instead of the buck converter. However, this is a simple analysis and more things should be taken into account. Table 3.3 summarizes the voltage and current stresses of the power switches, auxiliary capacitor and auxiliary inductor for the three topologies.

Table 3.3: Voltage and current stresses of the power switches, the auxiliary capacitor and the auxiliary inductor for the three ripple eliminators proposed (voltages in V, currents in A).

Topology\Parameter	V_{C_adc}	$\Delta V_{C_{dc}}$	Reduction %	V_{C_amax}	ΔV_{C_a}	I_{C_amax}	I_{L_amax}	V_{S_5max}	I_{S_5max}	V_{S_6max}	I_{S_6max}	I_{dcmax}
Buck-Boost	600	1,76	97,43	615	30,59	13,9	13,9	1016	13,9	1016	13,9	15,98
	300	4,33	93,67	331	61,07	13,9	13,9	731	13,9	731	13,93	15,97
Boost	600	3,08	95,5	615	30,33	8	8	616	8	616	7,96	10,25
Buck	300	13,21	80,68	329	58,36	6,8	6,8	406	6,8	406	6,87	9,7

As it can be seen, the rating of the power switches ($V_{S5max}, I_{S5max}, V_{S6max}, I_{S6max}$) for the buck-boost converter is almost double that the buck converter and about 1.5 times bigger than the boost converter. In the case of the auxiliary capacitor voltage, boost and buck-boost converter provide a higher value and therefore the capacitance size can be reduced. In the case of the inductor current, buck and boost are the ones with a lower value and therefore the ones that allow a lower inductor size. It should be noted as well that the buck converter allows the use of commercially available three phase IGBT modules. This means that the power switches required for the ripple eliminator could be easily integrated using the third leg of a three phase module. However, the amount of ripple reduction is the lowest one.

It can be seen that it is not possible to categorically state that one topology is the best one, since at the end it is a trade-off between the ripple reduction and cost requirements for a certain application. However, with a quite high percentage of ripple reduction and an intermediate cost of the power devices, the boost converter was selected as the best option for the universal decoupling unit proposed in this thesis.

Chapter 4

DC-link ripple cancellation based on a Universal Power Decoupling Unit

So far, the topologies reviewed in this thesis that are able to solve the issue of the power ripple in single phase converters have something in common. They can have an independent or dependent control with the PWM rectifier, but, in any case, all of them need to sense the rectified current or they need to have access to other information of the PWM rectifier such as the modulation index. This may not seem important but it creates a limitation. These topologies need to be built as an integrated converter where the AC/DC converter and the ripple eliminator are considered as one converter. If the AC/DC converter is considered as one separate unit where there is no access to the rectified current and there is only the possibility to place voltage sensors in the output capacitor, there would be a lack of data for these topologies to operate. Thus, it is the objective of this thesis to propose a new control scheme able to eliminate the voltage ripple in the single phase converters without requiring any further information rather than the voltage of the dc-link capacitor. Fig. 4-1 provides a scheme of the proposed idea. As it can be seen, the universal decoupling unit is connected to the input and output terminals of the AC/DC converter, but it does not need any information such as internal currents or other parameters.
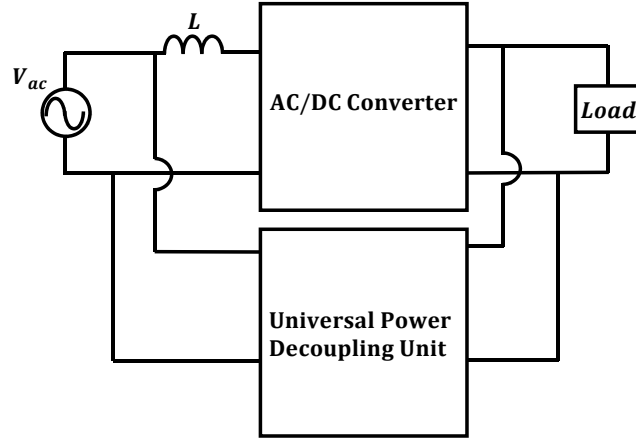
Figure 4-1: Universal Power Decoupling Unit scheme.

This chapter is arranged as follows: first the control proposed is explained, then a description on how to select the auxiliary inductor and capacitors is provided and, finally, the performance of the control proposed is validated through some simulations carried out in PSIM.

4.1 Control scheme of the Universal Power Decoupling Unit

Fig. 4-2 shows the control proposed for the Universal Power Decoupling Unit (UPDU). It makes use of a bidirectional boost converter to cancel the voltage ripple in the dc-link capacitor. Although it uses the same topology as the ripple eliminator seen in the previous section, its control is rather different. First of all there is no need to measure the rectified current and the control is based on the voltage ripple of the auxiliary capacitor and on the auxiliary inductor current. The second difference is that the converter is operated in continuous conduction mode so the current ripple can be instantaneously diverted and therefore a greater reduction of the voltage ripple can be achieved. It should be noted that the gate signals cannot be directly calculated with equations as it happened in the ripple eliminator and switches S_5 and S_6 are controlled in complementary mode.
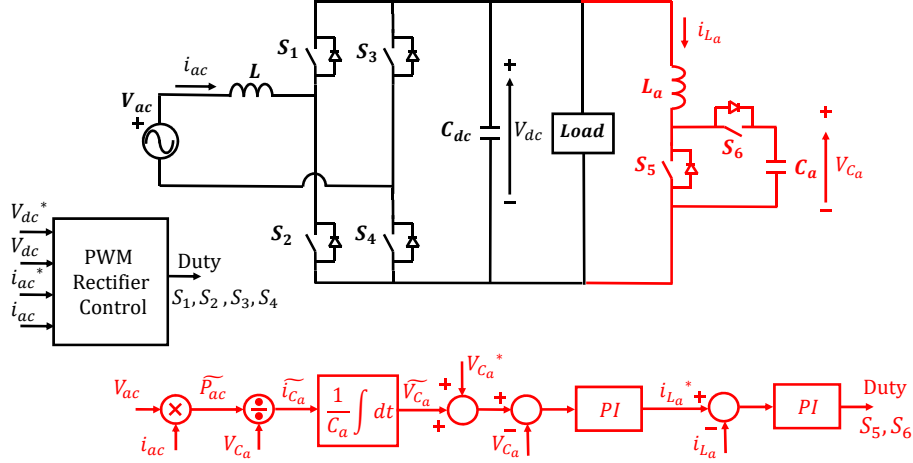
Figure 4-2: Control diagram of the Universal Power Decoupling Unit proposed.

As it can be seen, there is an outer voltage loop to control the voltage ripple in the auxiliary capacitor $\widetilde{V_{C_a}}$, and an inner current loop to control the current of the auxiliary inductor i_{L_a}. Special attention must be paid to the voltage loop since the way to obtain the voltage ripple is not straightforward. As mentioned before, the objective of the decoupling unit is to absorb the dc-link voltage ripple $(\widetilde{V_{dc}})$ in the auxiliary capacitor. As it was introduced in Chapter 1, there is a second order harmonic component in the input power $(\widetilde{P_{ac}})$ that is responsible for causing the voltage and current ripple in the dc output. In order to eliminate the voltage ripple in the dc-link, the UPDU should absorb all the power ripple coming from the AC source. Looking at the circuit diagram of Fig. 4-2, if the power losses of the input inductor are neglected $(P_L \simeq 0)$, the power ripple in the dc-link can be considered to be the same as the input power ripple. Then, since the control objective is to absorb this power ripple in the auxiliary capacitor, the following equations can be written:

$$
\left.\begin{array}{l}
\widetilde{P_{ac}} = V_{ac}i_{ac} \\[2mm]
P_L \simeq 0
\end{array}\right\}
\left.\begin{array}{c}
\overbrace{\widetilde{P_{ac}} \approx \widetilde{P_{C_a}}}^{\text{Control Objective}} \\[4mm]
\widetilde{P_{C_a}} = V_{C_a}\widetilde{i_{C_a}}
\end{array}\right\}
\widetilde{P_{ac}} = V_{ac}i_{ac} = \widetilde{P_{C_a}} = V_{C_a}\widetilde{i_{C_a}} \Rightarrow \widetilde{i_{C_a}} = \frac{\widetilde{P_{ac}}}{V_{C_a}}
\qquad (4.1)
$$

Once the current ripple through the auxiliary capacitor $\left(\widetilde{i_{C_a}}\right)$ is obtained, the voltage ripple can be directly calculated by considering the relation between voltage and current in a capacitor.

$$\widetilde{V_{C_a}} = \frac{1}{C_a} \int \widetilde{i_{ac}} dt \tag{4.2}$$

The voltage ripple is added to the command reference and compared with the real voltage of the auxiliary capacitor. The error signal is sent to a PI controller that gives the required inductor current reference to charge or discharge the capacitor. The inductor current is sensed and sent as the feedback signal for the current controller. To ease the tuning of the controller the output of the current PI controller can be considered as the inductor voltage V_{L_a}. Then, considering the average voltage of the inductor in a boost converter, the duty cycle of the power switches can be calculated with the following equation.

$$V_{L_a} T = dV_{dc} T + (1 - d)(V_{dc} - V_{C_a}) T \Rightarrow d = \frac{V_{L_a} - V_{dc}}{V_{dc}} + 1 \tag{4.3}$$

The duty signal is then compared with a triangular waveform and the gate signals for switching S_5 and S_6 in complementary mode are obtained.

4.2 Auxiliary inductor and capacitor selection

Before going into detail about the auxiliary circuit design, some comments about the PWM rectifier design must be made. Table 4.1 summarizes the parameters of the PWM rectifier. It consists of a 1kW, 60 Hz system with an input voltage equal to 220V and an output dc-link voltage of 400V.

In low power single phase converters, the percentage of the input impedance ($\%x$) should be generally below 5%. Its equation is given by

$$\frac{\%x}{100} = \frac{\omega L I_{nom\_RMS}}{V_{ac}} \tag{4.4}$$

Table 4.1: Parameters of the PWM rectifier connected to the Universal Power Decoupling Unit.

Parameters	Values
Supply voltage (RMS)V_{ac}	220 V
Supply frequency f	60 Hz
Switching frequency	9.6 kHz
DC-bus voltage V_{DC}	400 V
Output Power P_{dc}	1000W
Efficiency η	95%
Input Power P_{ac}	1052.63W

Thus, to fulfil with the 5% requirement with the parameters seen in the table, the following input inductor should be used at the input of the PWM rectifier.

$$I_{nom\_RMS} = \frac{P_{ac}}{V_{ac}} = 4.787A \tag{4.5}$$

$$L = \frac{V_{ac}}{\omega I_{nom\_RMS}\%x} = \frac{220}{2\pi 60 \cdot 4.787 \cdot 0.05} = 6.1mH \tag{4.6}$$

In the case of the dc-link capacitor, its voltage ripple is given by [11]

$$\Delta V_{C_{dc}} \approx \frac{E_{rC_{dc}}}{C_{dc}V_{C_{dc}dc}} \tag{4.7}$$

The lower the capacitance value the bigger the voltage ripple. Since the objective of this chapter is to show the performance of the UPDU, a small film capacitor of 0.1163 mF was selected for the PWM rectifier. This would involve a voltage ripple equal to 60V (15%) in the output dc-link.

(4.7) also applies for the voltage ripple in the auxiliary capacitor. Since the control objective is to absorb the dc-link voltage ripple in the auxiliary capacitor, it yields:

$$E_{rC_a} \approx C_a V_{C_a dc} \Delta V_{C_a} \approx E_{rC_{dc}} \Rightarrow C_a = \frac{E_{rC_{dc}}}{V_{C_a dc}\Delta V_{C_a}} \tag{4.8}$$

$$r_a = \frac{\Delta V_{C_a}}{V_{C_a dc}} \qquad C_a = \frac{E_{rC_{dc}}}{r_a}V_{C_a dc}^2 \tag{4.9}$$

where r_a is known as the ripple ratio. Thus, the higher is r_a or $V_{C_a dc}$, the smaller is the capacitance size.

In the case of the auxiliary inductor, its value must be selected to ensure continuous conduction mode operation. This is satisfied if the amplitude of the inductor current ripple Δi_{L_a} meets the following equation [11]

$$\Delta i_{L_a} \leq 2 I_{L_a\_peak} \tag{4.10}$$

where $I_{L_a\_peak}$ is the maximum value of the inductor current. The current ripple and duty cycle of a boost converter are given by

$$\Delta i_{L_a} = \frac{V_{C_{dc}dc}}{L_a} DT = \frac{V_{C_a dc} - V_{C_{dc}dc}}{L_a} (1 - D) T \tag{4.11}$$

$$D = 1 - \frac{V_{C_{dc}dc}}{V_{C_a dc}} \tag{4.12}$$

Combining (4.10),(4.11) and (4.12), the minimum auxiliary inductance required to operate the converter in CCM is given by

$$L_a \geq \frac{\left(1 - \frac{V_{C_{dc}dc}}{V_{C_a - dc}}\right) V_{C_{dc}dc}}{f_{sw} 2 I_{L_a\_peak}} \tag{4.13}$$

where f_{sw} is the switching frequency of the UPDU. It is obvious that the lower is the switching frequency the higher is the inductance required. It should be noted as well that the inductance value is also affected by the dc voltage component of the dc-link and the auxiliary capacitor. The lower is $V_{C_{dc}dc}$ or the higher is $V_{C_a dc}$, the higher is the inductance required. Thus, there is a trade-off between minimizing the auxiliary capacitor size and minimizing the auxiliary inductor size.

Fig. 4-3 shows the required C_a size for different ripple ratios and different dc voltage components, and it also shows the required L_a size for different switching frequencies and different dc voltage components. Within the mentioned trade-off, a final auxiliary dc voltage capacitor equal to 700V and a switching frequency equal to 30 kHz were selected. These parameters involve an auxiliary inductor of 1.1 mH and an auxiliary capacitor of 57 μF.
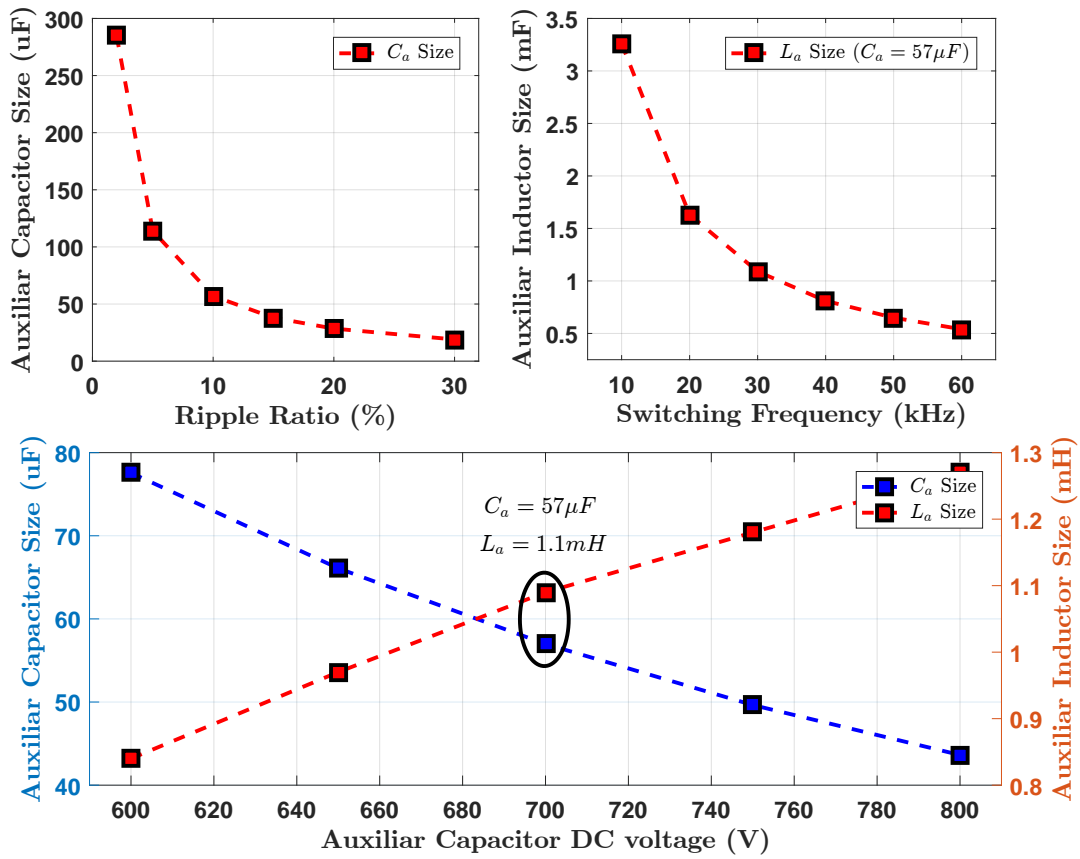
Figure 4-3: Auxiliary capacitor size for different ripple ratios and diferrent dc voltage components; and auxiliary inductor size for different switching frequencies and dc voltage components.

4.3 Simulation results and discussion

Some simulations were carried out in PSIM to validate the performance of the control proposed. The parameters used in the simulation are the ones shown in Table 4.1. The control was done in the per unit system being the base voltage 1000 V and the base current 35 A. The time constant and proportional gain of the PI voltage and current controllers are summarized in Table 4.2.

Fig. 4-4 shows the input ac voltage and current V_{ac}, i_{ac}, the input power P_{ac}, the calculation of the auxiliary capacitor current $\widetilde{i_{C_a}}$ and its correspondent capacitor voltage ripple $\widetilde{V_{C_a}}$. As it can be seen the input power is oscillating between 0 and 2 kW at twice the line frequency (120 Hz). In order to calculate the current ripple as seen in (4.1), the dc component of P_{ac} must be firstly calculated and then subtracted

Table 4.2: Proportional gain and time constant of the PI controllers used in the PWM rectifier and the UPDU (Vpu = 1000 V, Ipu = 35 A) .

		PWM Rectifier	Universal Power Decoupling Unit
Voltage Controller	Kp	0,2	28.5
	Ti	0,003	0,01
Current Controller	Kp	7	1.05
	Ti	0,0005	0.0063
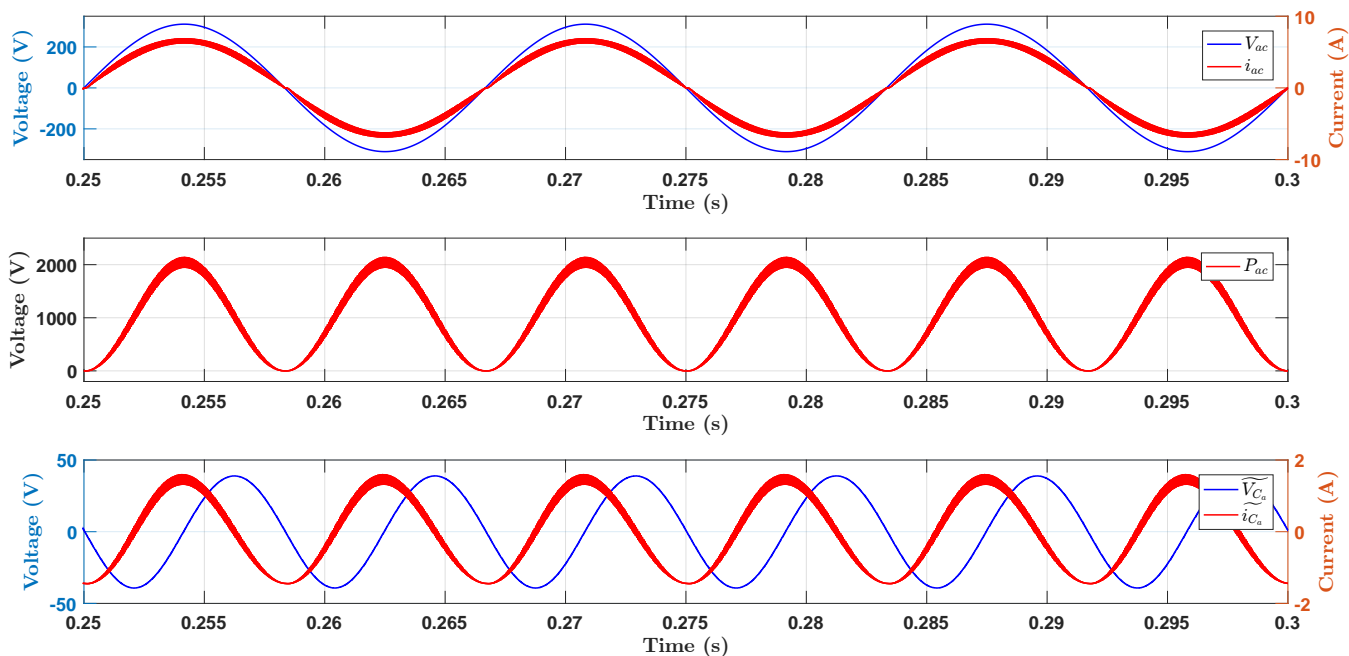
Figure 4-4: Input voltage and current V_{ac}, i_{ac}; input power P_{ac}; calculation of the auxiliary capacitor current $\widetilde{i_{C_a}}$ and its correspondent capacitor voltage ripple $\widetilde{V_{C_a}}$ of the UPDU.

from P_{ac}. In this way, a power ripple component oscillating between -1 kW and 1kW (aligned with 0) would be obtained. Then, dividing by the sensed voltage of the auxiliary capacitor the capacitor current ripple was obtained. It is also oscillating with 120 Hz and with a a peak to peak value of 3 A. From it, the voltage ripple in the auxiliary capacitor was calculated ($\widetilde{V_{C_a}} = 78V$) and added to the reference ($V_{C_a dc} = 700V$). Fig. 4-5 shows the input current, the dc-link voltage and the auxiliary capacitor voltage when the UPDU is connected to the PWM rectifier and it is activated in $t = 0.15$ seconds.
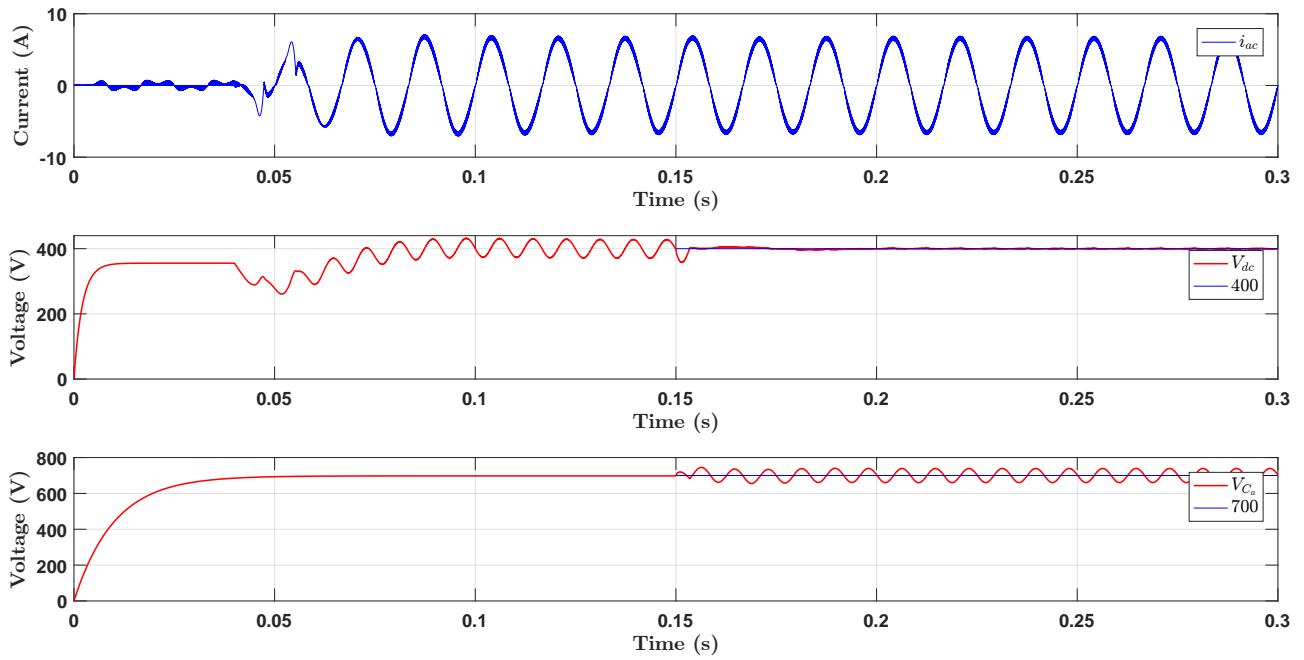
Figure 4-5: Input ac current; dc-link voltage and auxiliary capacitor voltage when the UPDU is connceted to the PWM rectifier and it is activated in $t = 0.15$ seconds.
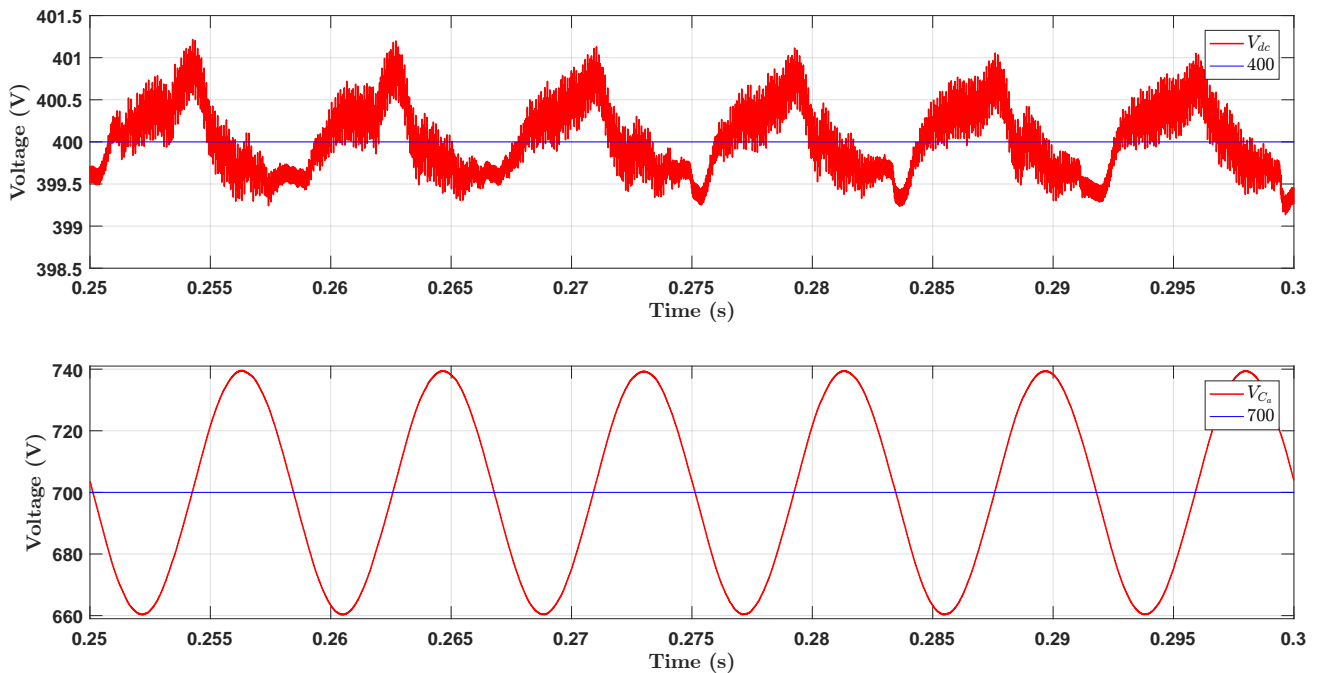
Figure 4-6: Zommed area of the dc-link voltage and auxiliary capacitor voltage when the UPDU is under normal operation.

As it can be seen, the dc-link is firstly precharged to 375 V and the load is connected in $t = 0.04$ seconds. After a transient, the PWM rectifier is able to control the dc-link voltage to 400 V. Since a small film capacitor was used in the dc-link, there is a voltage ripple equal to 58 V (14.5% of the total voltage). In the case of the UPDU, it is firstly precharged to 700V. Once it is activated, it is able to reduce the dc-link voltage ripple to 2 V (0.5% of the total voltage) by absorbing a voltage ripple of 78 V in the auxiliary capacitor. This can be clearly seen in Fig. 4-6 where a zoomed area of the dc-link voltage and the auxiliary capacitor voltage is shown. If an electrolytic capacitor were used instead of the UPDU, a capacitance 29 times bigger (3.37 mF) would be needed to get the same voltage ripple.

The performance of the proposed control for the Universal Decoupling Unit has been proved in this chapter. A significant theoretical reduction of the dc-link capacitor can be achieved with the UPDU based on the bidirectional boost converter. It is therefore interesting to built a real prototype of the UPDU and develop some experimental results in order to demonstrate the proposed control strategy.

Chapter 5

Hardware implementation

This section is focused on the design and selection of the components that make up the Universal Power Decoupling Unit. The design of the PWM rectifier is out of the scope of this thesis since an existent PWM rectifier developed for a previous application by ITRI's work team was used to perform the tests.

The chapter is organized as follows: the design of the auxiliary inductor is firstly explained and then the selection of the components that were used to build the Universal Decoupling Unit is justified and described.

5.1   Inductor design

This chapter is not intended to provide a guideline on how to design an inductor but rather to make use of the tools and concepts introduced in [18]. According to [18], the design of the inductor depends on 4 factors:

1. Desired inductance, L.

2. Mean current, I_{mean}.

3. Current ripple, ΔI.

4. Power loss and temperature.

Considering the bidirectional boost converter used in the UPDU, the mean current and the current ripple can be computed with the equations seen in Fig. 5-1.
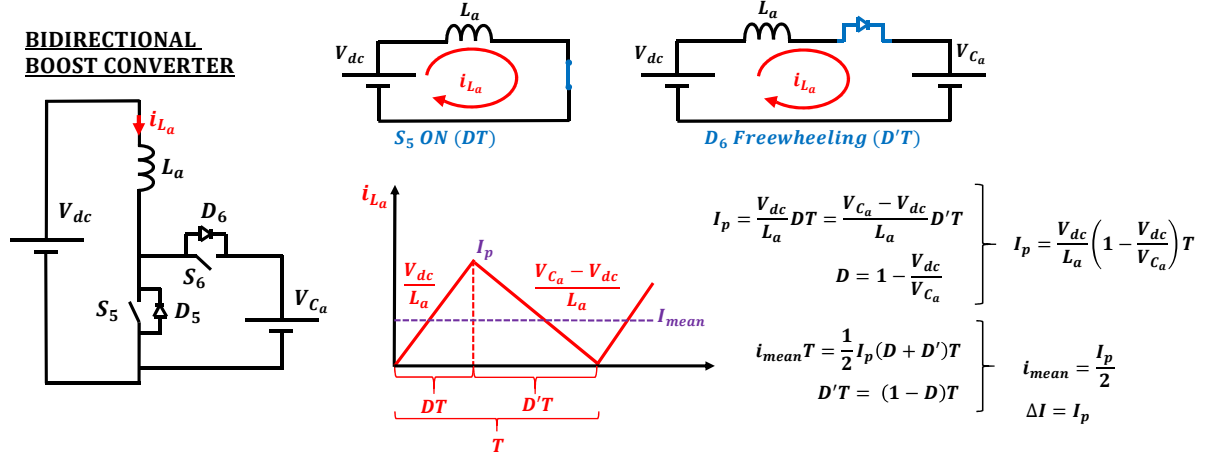
Figure 5-1: Peak current and mean current in a bidirectional boost converter.

Combining these equations with the parameters of the UPDU introduced in the previous chapter ($V_{C_a} = 700V$, $V_{dc} = 400V$, $L = 1.1mH$), a peak current equal to 5.2 A and a mean current equal to 2.6 A were obtained. However, some simulations were performed to take into account the transient response of the UPDU when there is a change from full load to no load and vice-versa. The simulations show that a peak current equal to 17 A appeared in the auxiliary inductor. Thus, to avoid the saturation of the inductor, the 17 A was used instead of the 5.2 A.

With the requirements established, the second step of the design process is to select the magnetic material and the magnetic core that provide the best performance with the lower cost and size. There are several materials available such as silicon steel, nickel iron or ferrites. Each of them has some properties like saturation flux density (B_s), permeability (μ) or resistivity (ρ) that make them more or less attractive. In all cases, once the core and material are selected, an electrical resistance appears in the core that is responsible for what is known as the core loss of the inductor. Selecting the right material and thickness is critical since the core loss can be minimize thus preventing overheating or other problems [18].

Amorphous materials provide a high saturation flux density that allow a lower component size. However, nothing comes for free and the highest is the flux density the smallest is the efficiency. Regarding the magnetic core construction, two types can be used: a shell type where the core surrounds the coil, or a core type where the coils are outside of the core [18]. Taking this into account and preferring a smaller inductor size rather than higher efficiency, an amorphous C-core 2605SA1 from Metglas was selected.

The next step in the design process is the selection of the core dimensions, wire diameter (D_{wire}), air-gap length (l_g) and number of turns (N) of the inductor. Fig. 5-2 shows the core dimensions and winding arrangement of the C core selected and in (5.1) and (5.2) the relationship between L, N, and the core dimensions can be founded. In (5.3) the relationship between the wire cross-section area A_{c_wire} and the current requirement is provided.
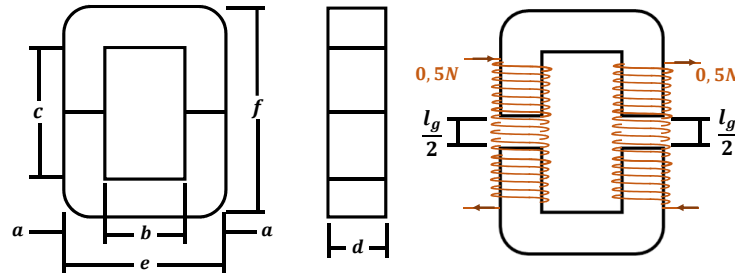
Figure 5-2: Metglas C-Core dimensions and inductor winding arrangement [19].

$$N = \frac{LI_p}{B_s A_c} \tag{5.1}$$

$$l_g = \frac{\mu_0 N^2 A_c}{L} \tag{5.2}$$

$$A_{c\_wire} = \frac{\pi}{4} D_{wire}{}^2; \quad A_{c\_wire} = \frac{I_{mean}}{J} \tag{5.3}$$

A_c is the cross-section area of the core, μ_0 is the permeability of the air and J is the current density of the wire. Before going into detail with the values selected, some comments must be done.

- Given a certain material, the higher is its resistance to the flux or more commonly known as reluctance ($\Re$), the lower is the flux produced for a given magnetomotive force. With a much higher permeability, the air has a very low reluctance compare with the magnetic material. Thus, if an air-gap is added to the magnetic core, the reluctance and therefore the flux density of the core can be controlled by the air-gap [18].

- From (5.1) it is clear that the smaller is the cross-section area or the higher is the peak current requirement, the higher is the number of turns required to make up the inductor.

- The magnetic core has a maximum flux density that it can withstand. If this value is exceeded, the core gets saturated and an increase in the current does not imply and increase in the flux density. Fig. 5-3 shows the flux density of a certain material when an external magnetizing force is applied [18].
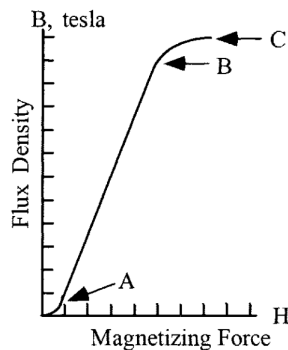
Figure 5-3: Typical magnetizing curve [18].

As it can be seen, there is a linear region where the flux is proportional to the magnetizing force and, at some point, saturation is reached making the coil to behave as an air-core [18].

- If there is a current with a dc and an ac component flowing through a wire, the distribution of the current through the wire is not uniform. As a consequence, some high frequency copper losses appear. This is commonly known as the skin effect and it should be taken into account when selecting the wire diameter

of the inductor coils. To avoid this problem the following equation must be fulfilled.

$$A_{wire} \geq A_{skin\_effect}; \quad A_{skin\_effect} = 2\frac{6.62}{10\sqrt{f}}[mm] \tag{5.4}$$

were f is the switching frequency. With the UPDU switching at 30 kHz, the wire diameter should be greater than $0.00764mm^2$ to avoid the skin effect.

- Not all the available window area (AW) of the magnetic core can be used to place the inductor coils. There is a window utilization factor K_u that takes this into account and states that the required area (A_{req}) to place the conductors should be around 40% $(K_u = 0.4)$ of the available window area.

With this facts in mind and taking into account the resistance of the wire (R), its correspondent copper losses (P_{copper}) and the power losses of the core (P_{core}), the required number of turns and air-gap length for the different core dimensions provided by Metglas [19] were calculated and are summarized in Table 5.1.

$$R = \rho\frac{l_{coil}}{A_{c\_wire}}; \quad P_{copper} = RI_{mean}{}^2; \quad P_{core}\left(W/kg\right) = 6.5f\left(kHz\right)^{1.51}B\left(T\right)^{1.74} \tag{5.5}$$

Table 5.1: Inductor parameters for different the core dimensions provided by Metglas.

Core Nº	A_c	b	c	AW	A_{req}	K_u	Mass(kg)	a	d	length/N(m)	length(m)	R(mΩ)	N	l_g	P_{core}	P_{copper}	P_{loss}
AMCC6.3	160	11	33	168	103,63	61,68%	0,154	10	20	0,06	7,01	136,03	116,88	2,50	0,75	0,96	1,71
AMCC8	180	13	30	200	92,11	46,06%	0,172	11	20	0,062	6,44	124,95	103,89	2,22	0,84	0,88	1,72
AMCC10	180	13	40	280	92,11	32,90%	0,198	11	20	0,062	6,44	124,95	103,89	2,22	0,96	0,88	1,85
AMCC16A	230	13	40	280	72,09	25,75%	0,248	11	25	0,072	5,85	113,56	81,30	1,74	1,21	0,80	2,01
AMCC16B	230	13	50	360	72,09	20,02%	0,281	11	25	0,072	5,85	113,56	81,30	1,74	1,37	0,80	2,17
AMCC20	270	13	50	360	61,41	17,06%	0,337	11	30	0,082	5,68	110,17	69,26	1,48	1,64	0,78	2,42
AMCC25	270	15	56	510	61,41	12,04%	0,379	13	25	0,076	5,26	102,11	69,26	1,48	1,85	0,72	2,57

It should be noted that a,b,c,d and l_g are in mm and the areas A_c, AW and A_{req} are in mm^2. With $I_{mean} = 2.6A$ and $J = 3A/mm^2$, a cross-section area of $0.89mm^2$ (much bigger than the skin-effect requirement) was selected for the wire.

Since it was the first time for the author of this thesis to develop the inductor winding, a utilization factor smaller than the normalized one was used $(K_u = 0.25)$. The core dimensions and correspondent N ($81.3 \simeq 82$ turns) and l_g ($1.74mm$) selected are the ones highlighted in the table.

Being the saturation flux density equal to 1.56 T [19], the saturation limit was checked as it is given below:

$$B = \frac{LI_{mean}}{A_c N} = \frac{1.1 \cdot 2.6}{230 \cdot 82} = 0.15 mT \ll B_s = 1.56T \Rightarrow \text{No Saturation} \tag{5.6}$$

Once the inductor design was finished, it was built following the process shown in Fig. 5-4(a). First, two bobbins were made and then two coil windings with 41 turns each were rolled over the bobbins. With the winding finished, half of the air-gap length was made with paper and place in each of the C core sides. It should be noted that if the placement of the two halves is not proportional, the core could be structurally unbalanced with an air-gap greater than the required and therefore with a different inductance than desired. Finally the two cores were assembled by making use of a band material and a buckle as Fig. 5-4(a) shows [18]. The inductor obtained and its impedance value is shown in Fig. 5-4(b). As it can be seen the inductor value obtained (1.06 mH) is very closed to the desired one (1.1 mH).

(a)   (b)
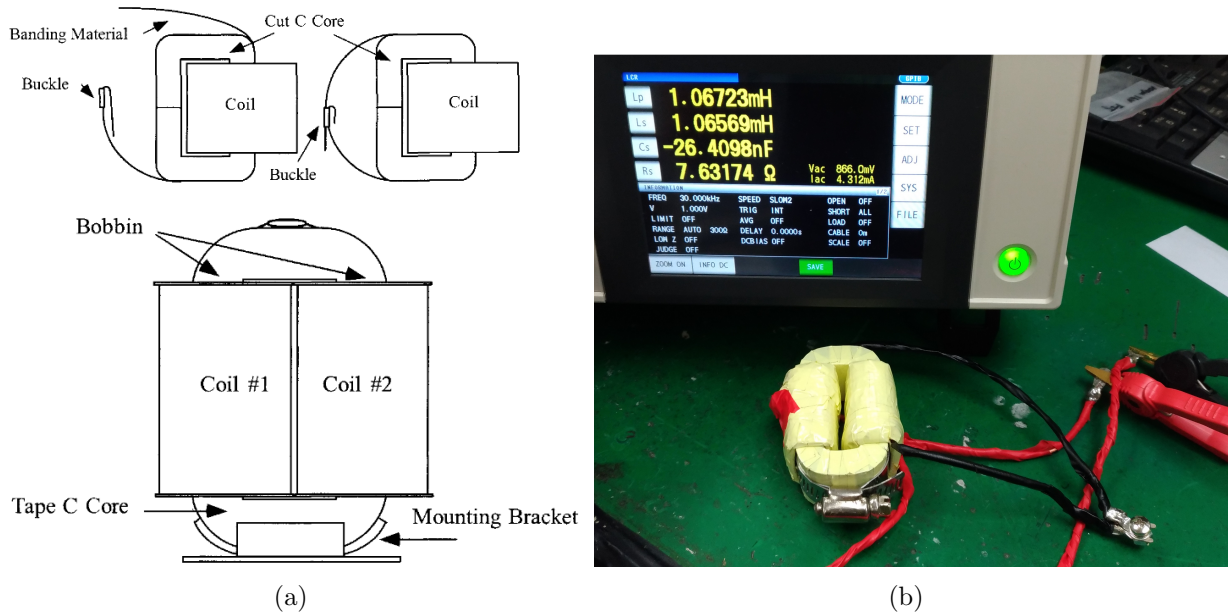
Figure 5-4: (a) Inductor building process [18], (b) Real inductor and its inductance measured with an impedance analyzer.

Once the inductor was built a saturation current test must be performed. If the design and built process were properly developed, the saturation current of the inductor should be greater than the peak current requirement. Fig. 5.1 shows the scheme of the circuit used to test the saturation current of the inductor. As it can be seen the circuit consists of two input capacitors, two power switches and a dc source. To determine if the current is saturated, an input voltage is applied to the inductor, and following the equation of an inductor $\left(V_L = L\frac{di}{dt}\right)$, the inductor current should be linearly increasing. If the current starts to be non-linear this means that the inductor is saturated. The circuit is operated as follows: the bottom switch is always turned off and a gate signal is provided to the gate-emitter terminals of the top switch; when the IGBT1 is turned on the inductor is charged and then the current freewheels through the diode D_6 when the switch is turned off. Fig. 5.1 shows the gate-emitter voltage and the inductor current obtained in the test.

(a)   (b)
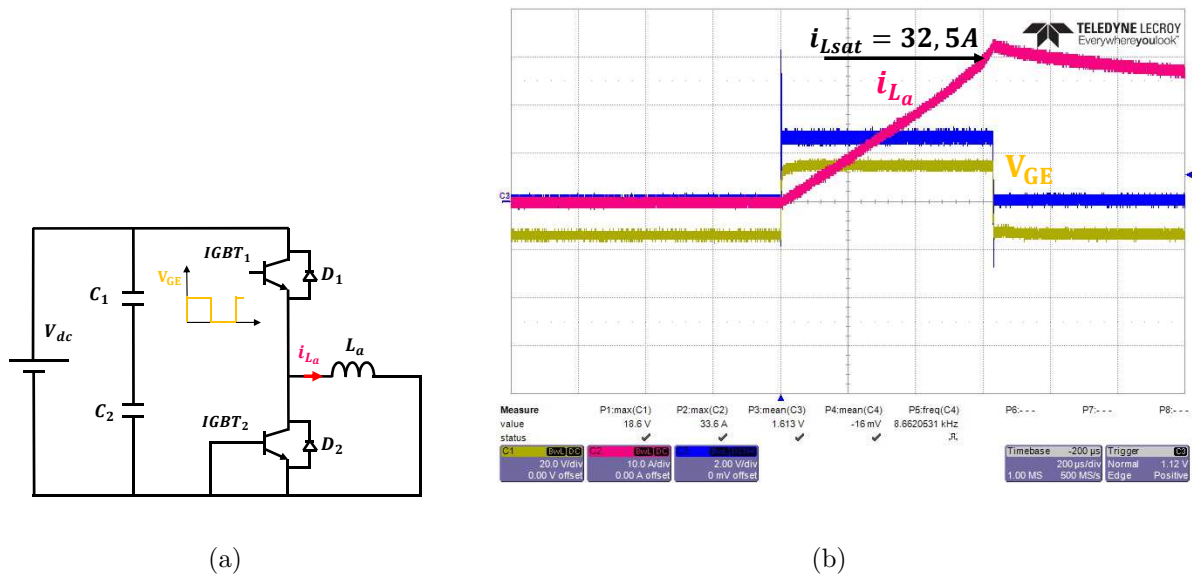
Figure 5-5: (a) Circuit used for the inductor current saturation test, (b) Gate-emitter voltage (V_{GE}) and inductor current (i_{L_a}) obtained during the saturation current test.

As it can be seen the inductor starts to get saturated when the current reaches a value of 32.5 A. This is much greater than the 17 A requirement. Thus, the inductor can be considered to be successfully designed.

5.2 Components selection and construction

Multiple PCBs were used to build the UPDU. All of them were provided by ITRI and, in most cases, the PCBs were "recycled" from previous projects developed by ITRI's work team. However, the requirements of the previous applications were not the same as those of the UPDU and several modifications were needed. Fig. 5-6 shows the power stage of the UPDU. Looking at it from right (input) to left (output), there is a current sensor followed by 4 power MOSFETS with their corresponding gate driver circuit and heat sink. Four capacitors make up the dc link and there is a voltage sensor at the output of the PCB to measure the dc-link voltage. It can be noted that the PCB is prepared to have bigger size and bigger number of capacitors. A fuse, a relay and an EMI filter can also be incorporated to the PCB. However, for the UPDU these components are not of interest.
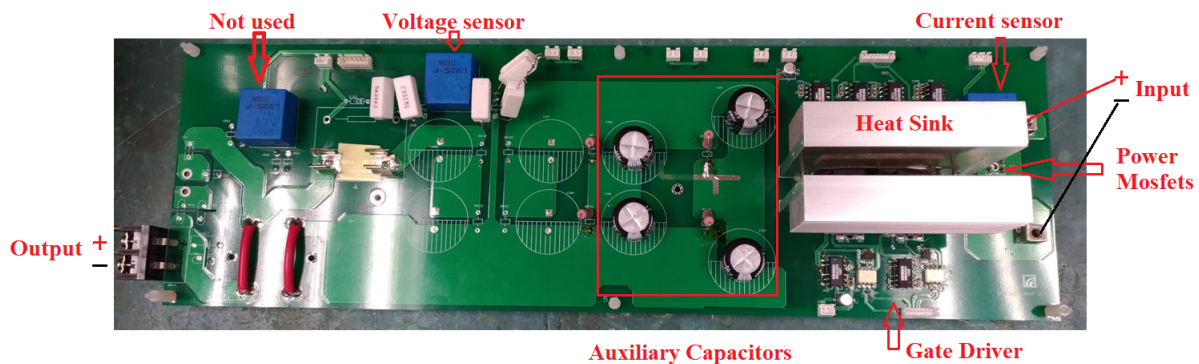
Figure 5-6: Power stage of the Universal Power Decoupling Unit.

The original design of the UPDU required a film capacitor of 57 μF, 800 V. Such capacitor was not available in the laboratory and 4 Nichicon Aluminium Electrolytic Capacitors of 56 μF, 450 V were used instead. They have a capacitance tolerance of $\pm20\%$ at 120 Hz. The capacitance was measured and a final value of 49 μF was found for the 4 capacitors.

Only two of the four power MOSFETS are needed for the UPDU. They must withstand the maximum voltage of the auxiliary capacitor ($\simeq 750$V) and the peak current through the inductor (17 A). It is well known that SiC MOSFETS have a low on-state

resistance and an excellent switching performance that make them very attractive. They also have an intrinsic body diode that allow them to have a compact structure. For these reasons, SiC MOSFETS of 1.2 kV, 90 A were used in the power stage PCB. Their detailed specifications can be found at the end of this document.

The voltage and current sensors used are based on a current transducer that uses the Hall effect. The current sensor can be directly placed in the PCB but in the case of the voltage sensor, a resistance must be placed in series with the primary circuit. The manufacturer recommends to place this resistance to ensure a primary current of 10 mA when the nominal voltage is applied to the voltage sensor. Considering a nominal voltage of 1000 V (p.u value), 5 resistances of 20 kΩ and 5 W were placed at the input of the voltage sensor. Fig. 5-7 shows the design procedure followed to select these resistances.
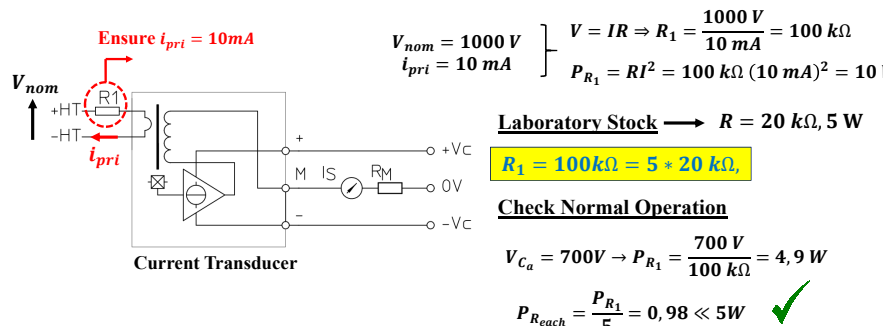
Figure 5-7: Process followed to calculate the input resistance of the voltage sensor.

So far, the components of the power stage PCB have been reviewed. However, another four PCBs were used to make up the UPDU. Fig. 5-8 shows the PCBs used and Fig. 5-9 shows the scheme of their wire connections. A precharge unit was used to charge the auxiliary capacitors. It consists of two DC relays and a precharge resistor. In order to control the converter, a microcontroller from texas instruments was used (TMS320F28377D). It is located on the control board and to connect it and program it with the computer, a Blackhawk USB560v2 System Trace (STM) Emulator was used. The sensed signals and the PWM signals of the power stage cannot be directly connected to the Control Board, and an Interface Board is required. Finally the last PCB used is a Digital to Analog Converter (DAC).
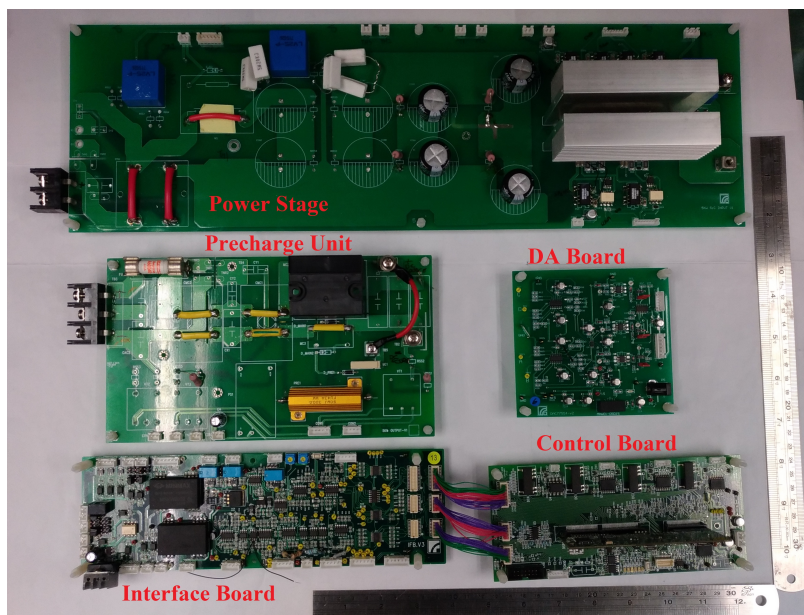
Figure 5-8: PCBs used to make up the Universal Power Decoupling Unit.
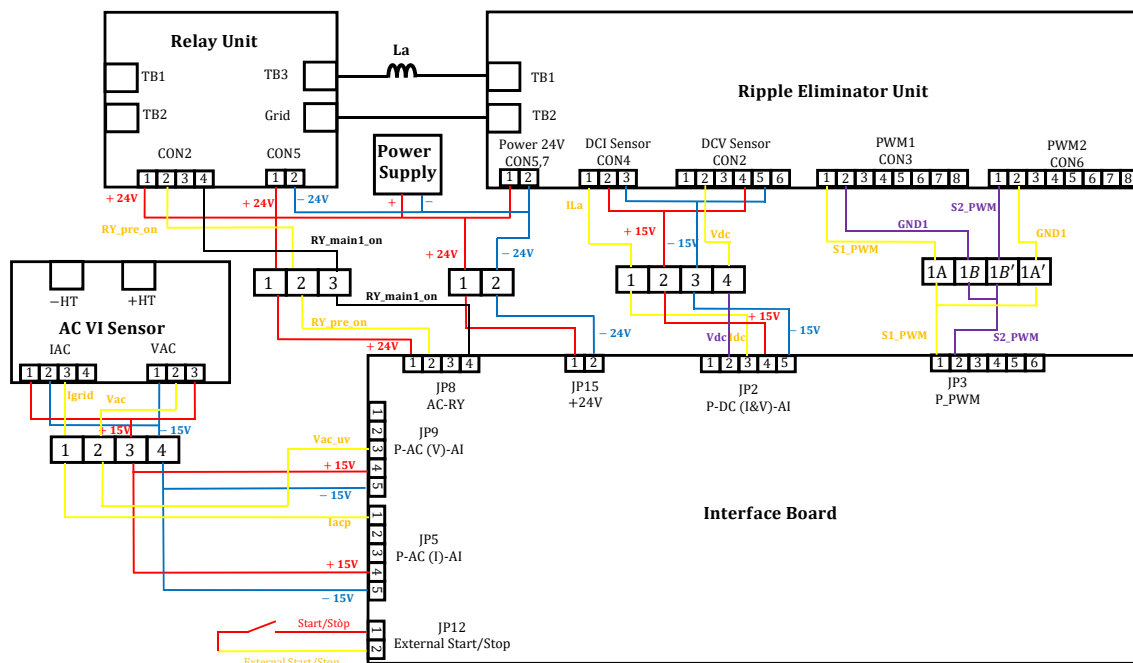
Figure 5-9: Wire connections for the PCBs that make up the UPDU.

Chapter 6

Software Implementation

Te Code Composer Studio and the TMS320F28377D from TI were used to implement the software. When programming a microcontroller to control a converter such as the one of the UPDU, one cannot think to do the whole code all at once and this must be split into several parts. Thus, the code was split into the following stages:

1. PWM and ADC configuration.

2. Overcurrent protection, overvoltage protection and open loop code.

3. DC-link precharge code.

4. Ramp-up command code.

5. Close loop code.

6. Close loop control + control of voltage ripple code.

Hereafter, a brief summary of the challenges found when programming each of the different stages will be given. For a full understanding the technical reference manual provided by TI should be reviewed [20].

The enhanced pulse width modulator (ePWM) peripheral of the TMS320F28377D has 6 PWM channels each of them with two PWM outputs: ePWMxA and ePWMxB. From them, only the ePWM1A and ePWM1B were needed since the UPDU has only two switches. They were configured to switch in complementary mode and since a

short circuit would happen if the two switches were closed the same time, a dead time of 1 μs was added to the gate signals. Fig. 6-1 shows the ePWM1A and ePWM1B measured at the interfaced board for a 50% fixed duty cycle.
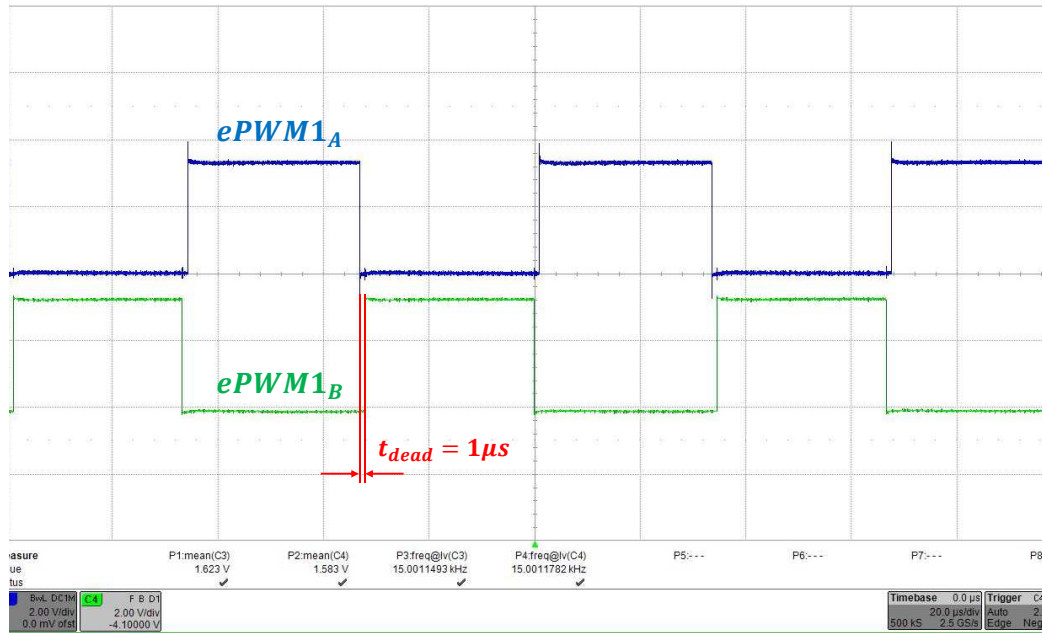
Figure 6-1: PWM outputs for channel 1 when a 50% fixed duty cycle is provided to the microcontroller.

The ePWM1A anb ePWM1B were configured to be the trigger source that starts the conversion of the ADC channels. Four signals were used in the control and therefore 4 channels were to be converted: auxiliary capacitor voltage V_{C_a}, input ac voltage V_{ac}, auxiliary inductor current i_{L_a}, and input ac current i_{ac}. V_{ac}, i_{L_a} and i_{ac} can have positive and negative polarity that must be taken into account when doing the ADC conversion. Some test where done to check the accuracy of the ADC conversion. One thing must be commented before going into detail with the results obtained. The interface board has an input resistor for all the sensed signals. The design of this resistor must be understood in order to set the p.u value. Fig. 6-2 shows the circuit diagram of one of the ADC channels of the interface board.

70
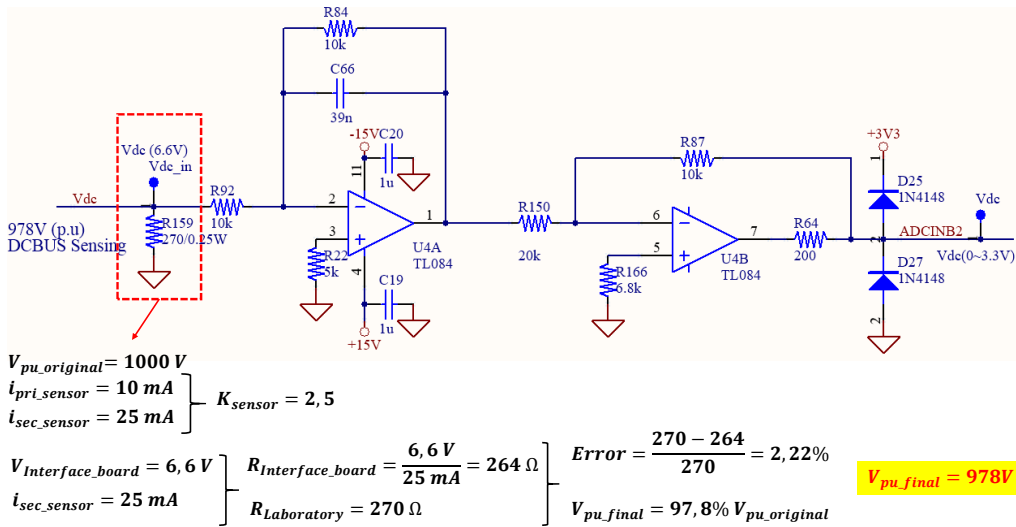
Figure 6-2: PWM outputs for channel 1 when a 50% fixed duty cycle is provided to the microcontroller.

The input resistance must be designed to ensure a maximum voltage of 6.6 V when the sensed signal takes its maximum value (p.u value). Considering 1000 V to be the original p.u value for the voltage measurements, a resistor of 264 Ω is required. However, such a resistor was not available in the laboratory and a 270 Ω resistor was used instead. As a consequence, an error of 2.22 % will appear in the ADC result if the p.u value is not changed. Taking this into account a final p.u value of 978 V was set for the voltage measurements. In the case of the sensed currents, the resistors needed to ensure the input 6.6 V were found in the laboratory and thus 35 A was maintained as the p.u value.

Tables 6.1, 6.2, 6.3 and 6.4 show the ADC conversion results. As it can be seen, for the positive polarity of the bipolar signals, the ADC error is below 1 %. However, when looking at the negative polarity, the ADC error is between 1 % and 3 %. For the auxiliary capacitor voltage, the ADC error is quite big for low voltage commands and around 3 % for the normal operating voltage (700V).

A calibration factor must be included in the ADC conversion to account for this errors. Otherwise, there would be a mismatch between the real and the sensed signal. If this happen the performance of the converter could be considerably worsened.

Table 6.1: Auxiliary inductor current ADC conversion test.

| ILa TEST (p.u value = 35 A) | | | | | | | |
| NEGATIVE POLARITY | | | | POSITIVE POLARITY | | | |
IDC Source	IDC (p.u)	ADC result	Error %	IDC Source	IDC (p.u)	ADC result	Error %
-1	-0,0286	-0,0278	-2,7	1	0,0286	0,0283	0,95
-2	-0,0571	-0,0556	-2,7	2	0,0571	0,0566	0,88
-3	-0,0857	-0,0834	-2,7	3	0,0857	0,0854	0,32
-4	-0,1143	-0,1123	-1,738	4	0,1143	0,1137	0,5125
-5	-0,1429	-0,1406	-1,58	5	0,1429	0,142	0,6
-6	-0,1714	-0,1684	-1,767	6	0,1714	0,1704	0,6
-7	-0,2	-0,1967	-1,65	7	0,2	0,1987	0,65

Table 6.2: Input ac current ADC conversion test.

| IAC TEST (p.u value = 35 A) | | | | | | | |
| NEGATIVE POLARITY | | | | POSITIVE POLARITY | | | |
IDC Source	IDC (p.u)	ADC result	Error %	IDC Source	IDC (p.u)	ADC result	Error %
-1	-0,0286	-0,0273	-4,31	1	0,0286	0,0288	-0,8
-2	-0,0571	-0,0551	-3,575	2	0,0571	0,0576	-0,8
-3	-0,0857	-0,083	-3,167	3	0,0857	0,0859	-0,2167
-4	-0,1143	-0,111	-2,875	4	0,1143	0,1142	0,075
-5	-0,1429	-0,1396	-2,28	5	0,1429	0,143	-0,1
-6	-0,1714	-0,1679	-2,058	6	0,1714	0,1713	0,075
-7	-0,2	-0,1962	-1,9	7	0,2	0,199	0,5

Table 6.3: Input ac voltage ADC conversion test.

| VAC TEST (p.u. value = 978 V) | | | | | | | |
| NEGATIVE POLARITY | | | | POSITIVE POLARITY | | | |
VDC Source	VDC (p.u)	ADC result	Error %	VDC Source	VDC (p.u)	ADC result	Error %
-10	-0,0102	-0,0098	4,5472	10	0,0102	0,0103	-0,245
-50	-0,0511	-0,0508	0,6743	50	0,0511	0,0513	-0,2646
-100	-0,1022	-0,1015	0,733	100	0,1022	0,1025	-0,245
-150	-0,1534	-0,1528	0,3744	150	0,1534	0,1533	0,0484
-200	-0,2045	-0,204	0,244	200	0,2045	0,2045	-0,0005
-250	-0,2556	-0,2548	0,3222	250	0,2556	0,2553	0,1266
-300	-0,3067	-0,3062	0,1951	300	0,3067	0,3066	0,0484
-350	-0,3579	-0,3574	0,1322	350	0,3579	0,3579	-0,0075
-400	-0,409	-0,4086	0,0973	400	0,409	0,4086	0,0973

Table 6.4: Auxiliary capacitor voltage ADC conversion test.

| VCa TEST (p.u. value = 978 V)			
VDC Source	**VDC (p.u)**	**ADC result**	**Error %**
50	0,051	0,0459	10,005
100	0,102	0,0952	6,7078
150	0,1532	0,1445	5,6602
200	0,2042	0,1938	5,0894
250	0,2553	0,2434	4,6675
300	0,3064	0,2927	4,4843
350	0,3575	0,3422	4,2701
400	0,4085	0,3918	4,085
450	0,4596	0,4418	3,8753
500	0,5107	0,4916	3,7468
550	0,5618	0,5422	3,4817
600	0,613	0,5915	3,5051
650	0,6641	0,643	3,1788
700	0,7156	0,694	3,0244
750	0,7668	0,7456	2,7608
800	0,8179	0,7971	2,5472

As explained in the previous section, the auxiliary inductor has a saturation current equal to 32.5 A that cannot be surpassed. Thus the code must be configured to trip the overcurrent protection for values greater than 32.5 A. When the protection is tripped, the switches must be turned off ensuring that the converter is not operating. The converter will be able to operate again once the fault is cleared by reseating the control board. Fig. 6-3(a) shows the results of the overcurrent protection test. The test was done in such a way that the inductor current is half of the one seen in the oscilloscope. As it can be seen when the current is around 65 A (real current = 32.5 A), the PWM is disabled and the converter stops its operation.

The auxiliary capacitors have a maximum voltage rating of 450 V. Since 4 capacitors were used (2 series and 2 in parallel), the maximum voltage should be lower than 900 V. A smaller scale test was done configuring the code to trip the overvoltage protection for 380 V. Fig. 6-3(b) shows the results obtained. It can be seen how the converter stops its operation when the voltage is greater than 380 V. The GPIO48 was configured to show that the protection is latched even if the voltage is recovered ($V_{C_a} < 380V$). For normal operation, the power supply must be turned off and on.
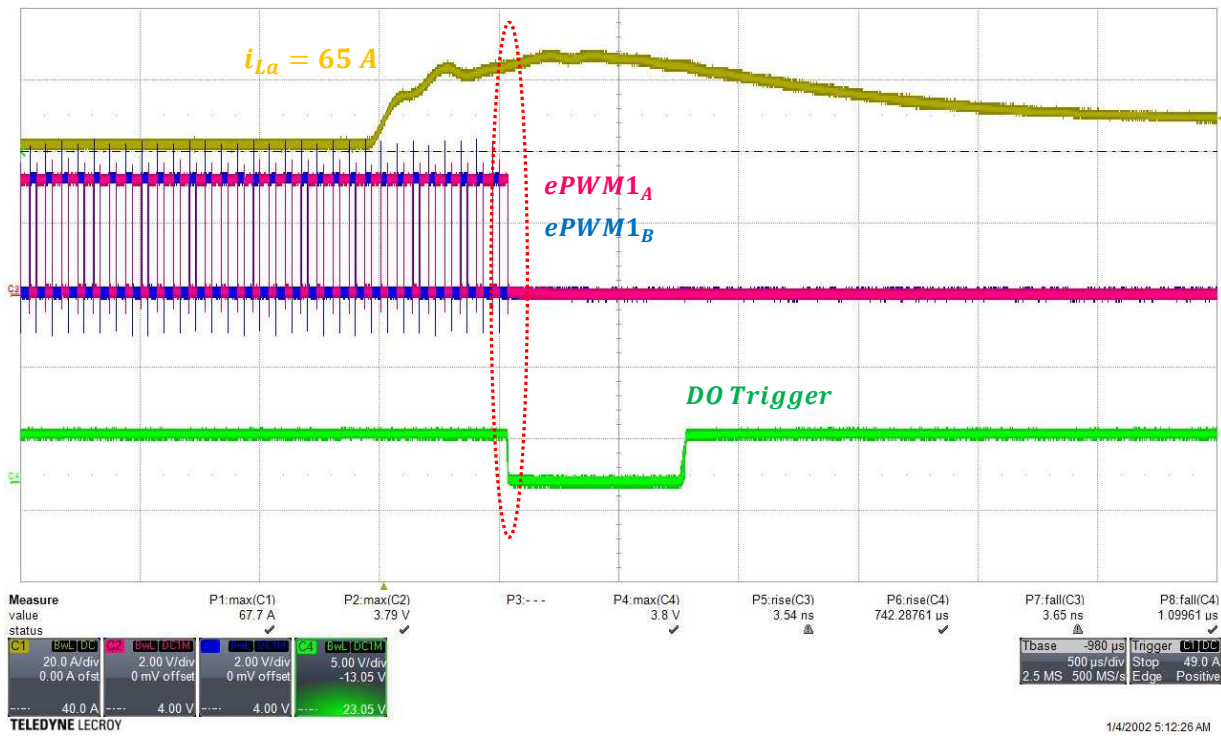
(a)
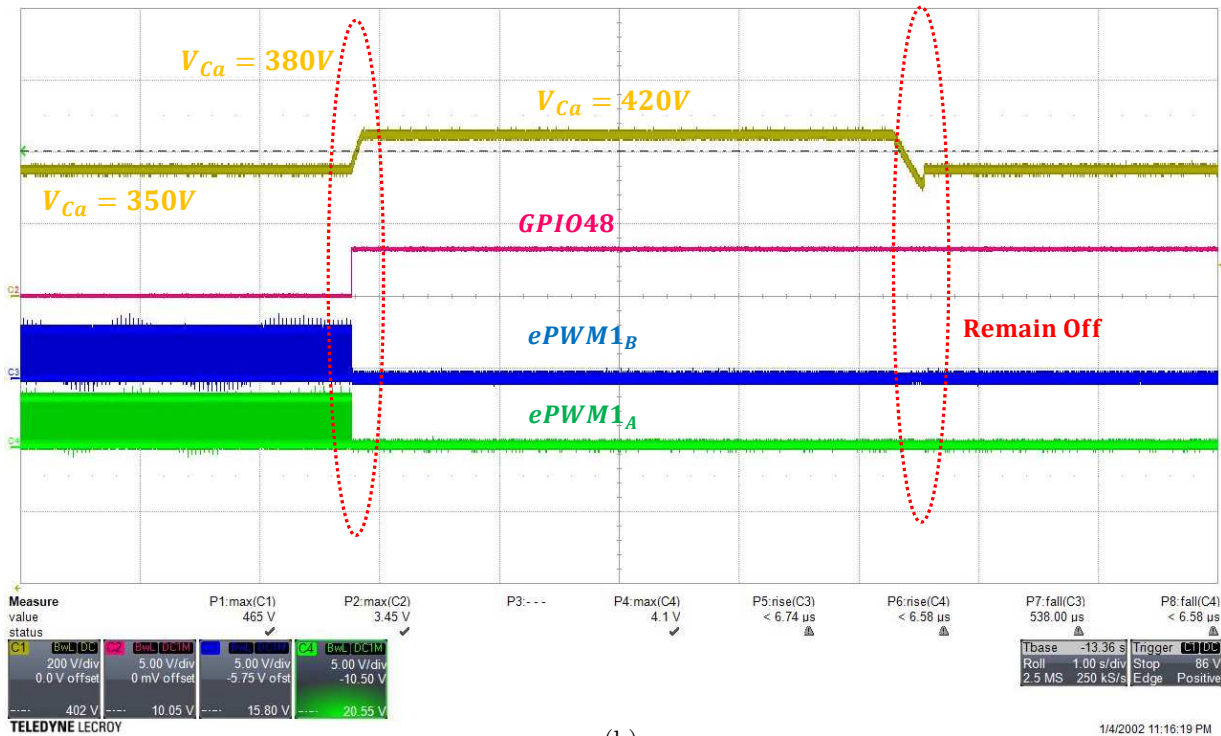
(b)

Figure 6-3: (a) Auxiliary inductor current, PWM gate signals and trigger signal when the overcurrent protection is configured to tripped for currents greater than 32.5 A. (b) Auxiliary capacitor voltage, PWM gate signals and latch signal (GPIO48) when the overvoltage protection is configured tor trip for voltages greater than 380 V.

Once the protection was configured the performance of the converter was tested in open loop. The input voltage was set to 400 V and a fixed duty cycle equal to 42.85% was sent to the PWM generator. By doing so the converter should boost the voltage from the 400 V to 700 V. Fig. 6-4 shows the results obtained.
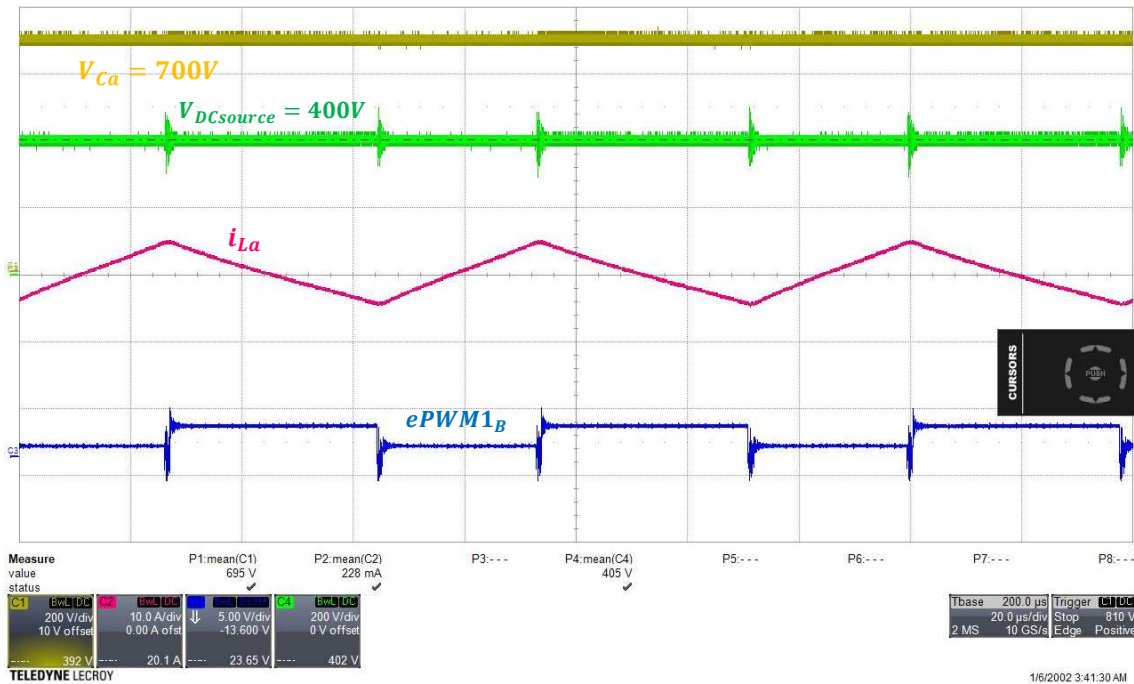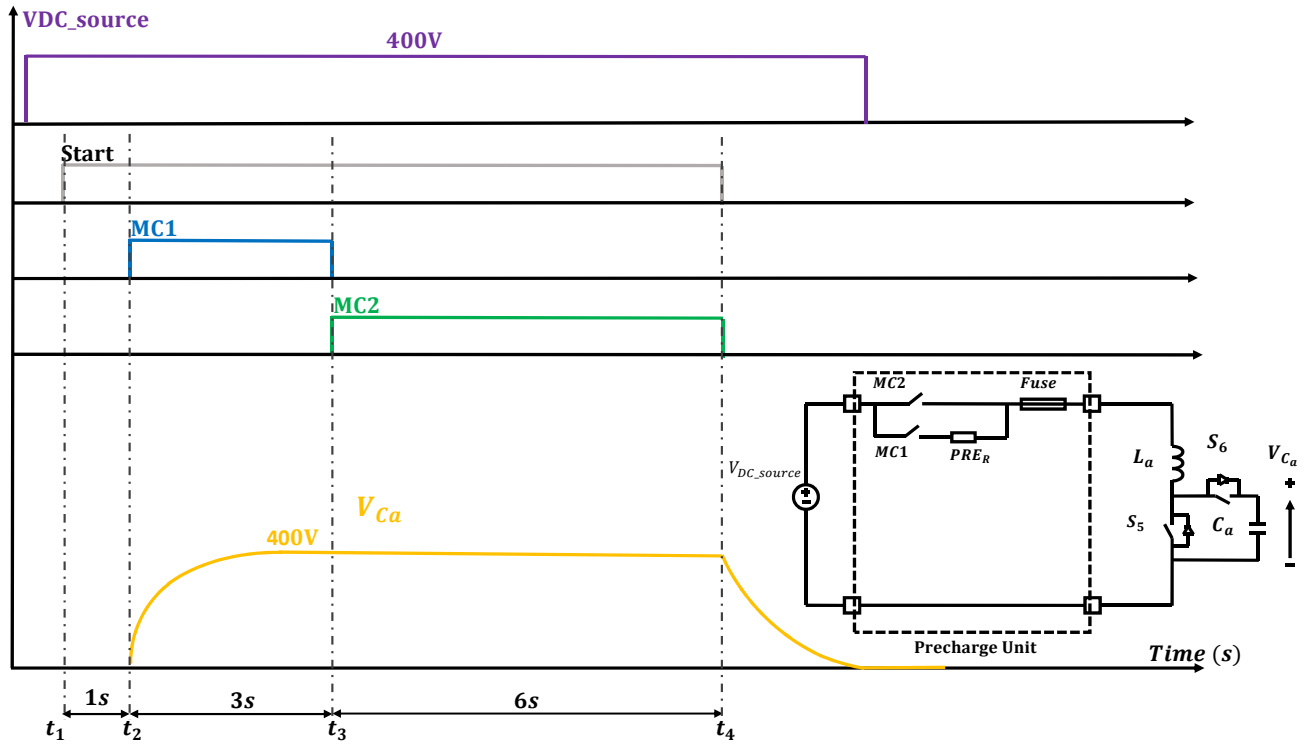

Figure 6-4: Auxiliary capacitor voltage, input dc source voltage, auxiliary inductor current and pwm command of the bottom switch when the converter is operated in open loop with a fixed 42.85% duty cycle.

As it can be seen the inductor is linearly charged and discharged during each switching cycle and the auxiliary capacitor voltage is properly boosted to 700 V. With the open loop performance validated, the precharge sequence of the converter was tested as Fig. 6-5(a) shows. An external switch was used to start the precharge sequence and the converter was supplied with the expected dc-link voltage (400 V). In t_1 the switch is closed and after 1 second, MC1 is turned on and the capacitor should be charged to 400 V. Once the capacitor is charged ($t_3 = 3s$), MC1 is turned off and MC2 is turned on. Fig. 1-2 shows the results obtained. As it can be seen the capacitor was charged to 400 V in approximately 0.2 seconds. Such a short time is caused by the low capacitance used and the low value of the precharge resistor.

(a)
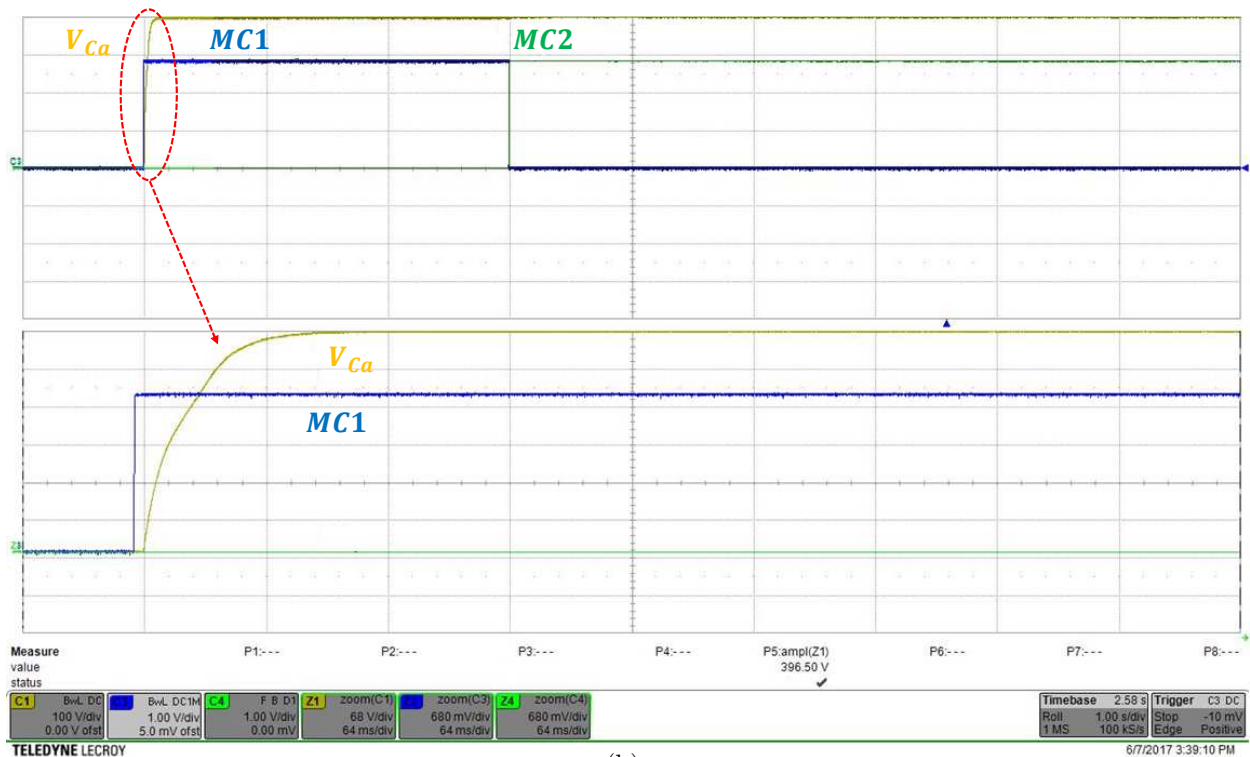
(b)

Figure 6-5: (a) Precharge unit scheme (b) Auxiliary capacitor voltage and relay unit signals MC1, MC2.

After the precharge unit was configured the close loop control of the converter was tested. A $K_p = 8$ and $T_i = 0.01$ were used for the voltage controller while a $K_p = 1$ and a $T_i = 0.0006$ were used for the current controller. In order to be able to connect the UPDU to the PWM rectifier, three things should be tested:

1. The converter must be able to slowly charge from the real dc-link value to 700 V. Thus a ramp-up module was configured. The voltage command must be firstly updated with the value of the dc-link voltage and then the command is slowly increased so the capacitor reaches 700 V after 4 seconds. Fig. 6-6(a) shows the ramp-up module scheme and Fig. 6-6(b) shows the results obtained. As it can be seen the capacitor was successfully charged to 700 V.

2. The code must be configured so the converter can be started and stopped several times without affecting its performance. Fig. 6-7(a) shows the start-stop sequence used in the test and Fig. 6-7(b) shows the results obtained. As it can be seen the ramp-up sequence was repeated three times and the converter was able to successfully reach the 700 V in all cases.

3. In Chapter 5 it was seen how for a 1 kW prototype a voltage ripple equal to 78 V would appear in the auxiliary capacitor. Thus the auxiliary capacitor must be able to control a voltage ripple command. To ensure a safety margin, a voltage ripple 1.5 times higher than the one obtained in the simulations (114 V) was added to the voltage command. Fig. 6-8(a) shows the sequence of the voltage ripple control test and Figs 6-8(b) shows the results obtained. As it can be seen, once the converter was controlled to 700 V, the voltage ripple was added to the voltage reference. Fig. 6 shows a zoomed area of the voltage ripple control. V_{Ca} was able to effectively track V_{Ca-ref}. It seems that there is a shift between the two signals but this is just a delay introduced by the integral part of the PI controllers. It should be noted that the DAC board was used to check the signals (PWM_{cmd}, V_{Ca}, V_{Ca-ref}) and therefore the values are scaled between -10 V and 10 V.
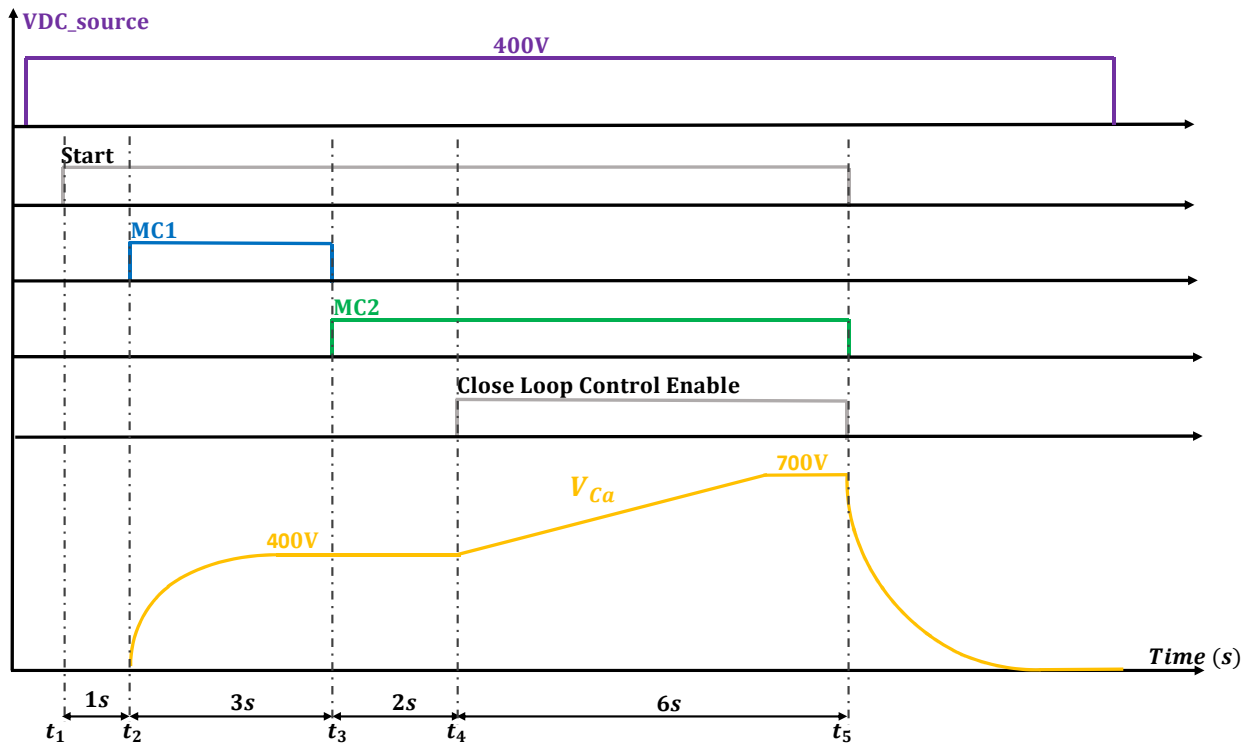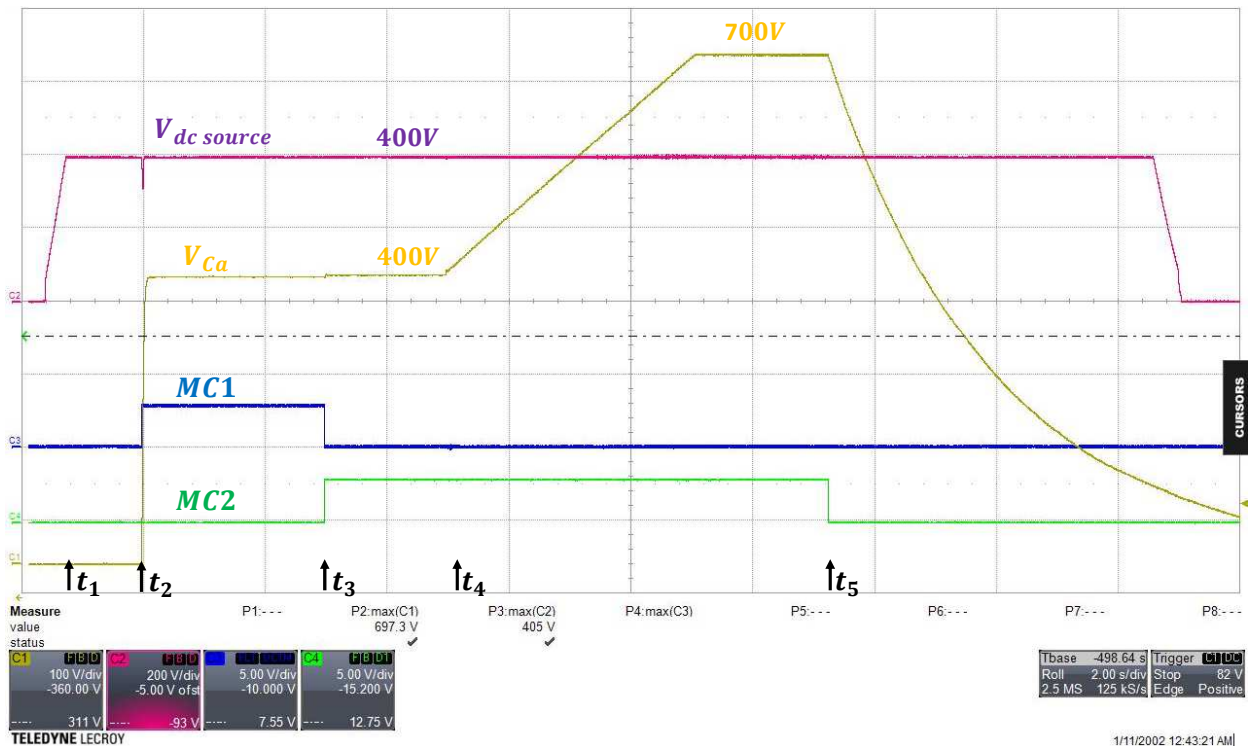
Figure 6-6: (a) Ramp-up module scheme (b) DC source voltage, auxiliary capacitor voltage and relay unit signals when the converter is charge from the dc-link value to 700 V in 4 seconds.
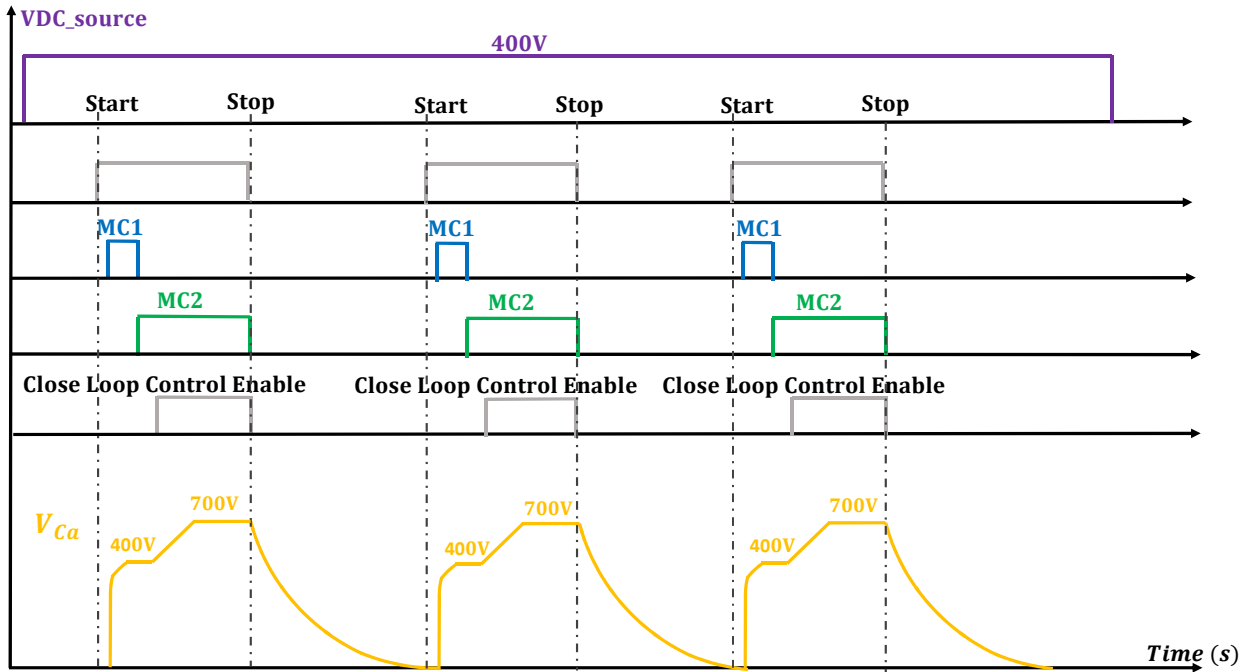
(a)
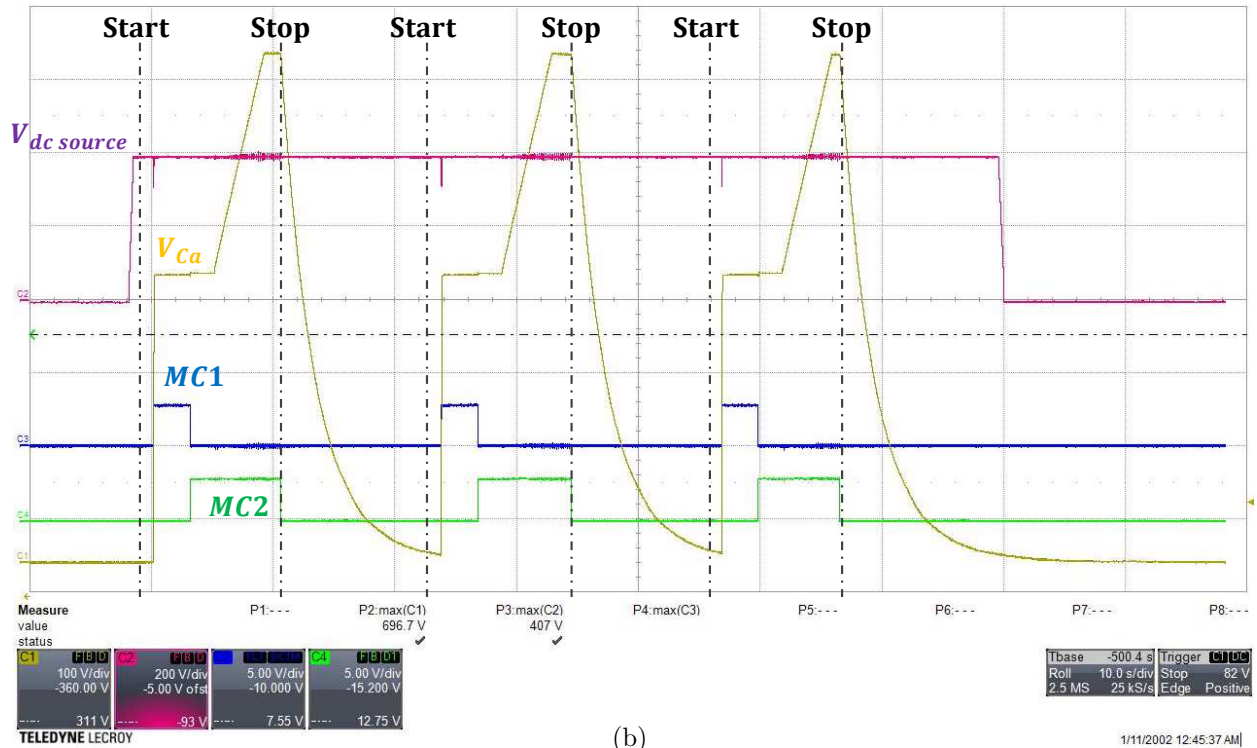
(b)

Figure 6-7: (a) Start-stop sequence (b) DC source voltage, auxiliary capacitor voltage and relay unit signals when the ramp-up sequence is repeated three times.
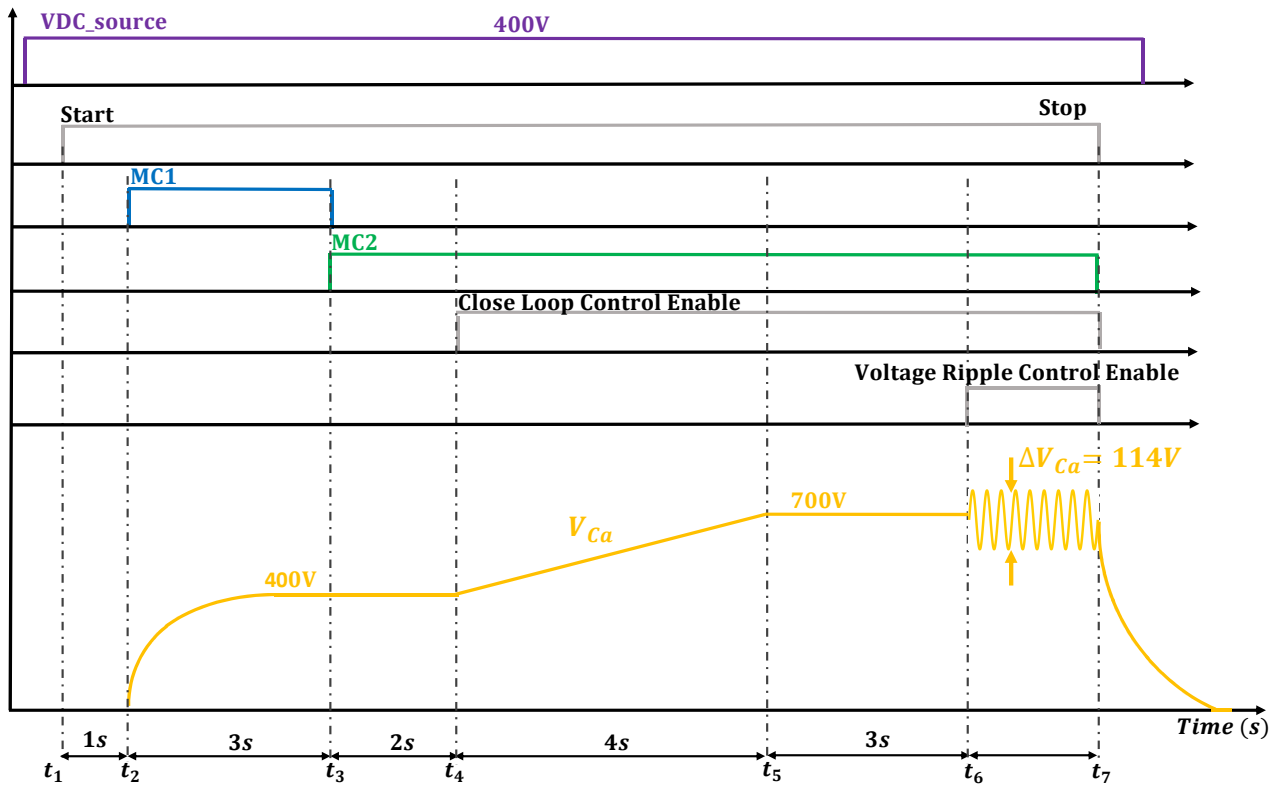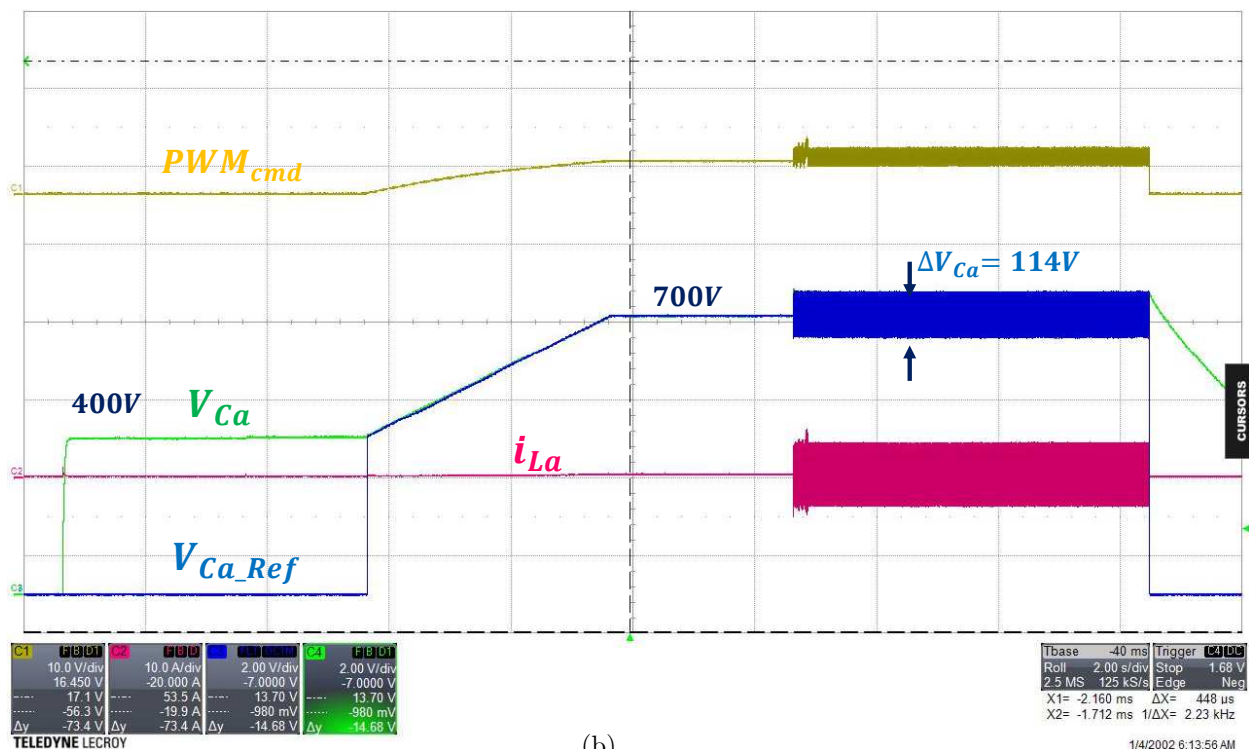
Figure 6-8: (a) Voltage ripple control sequence (b) PWM command, auxiliary capacitor voltage reference, auxiliary capacitor voltage and auxiliary inductor current when a voltage ripple equal to 114 V is added to the voltage command.
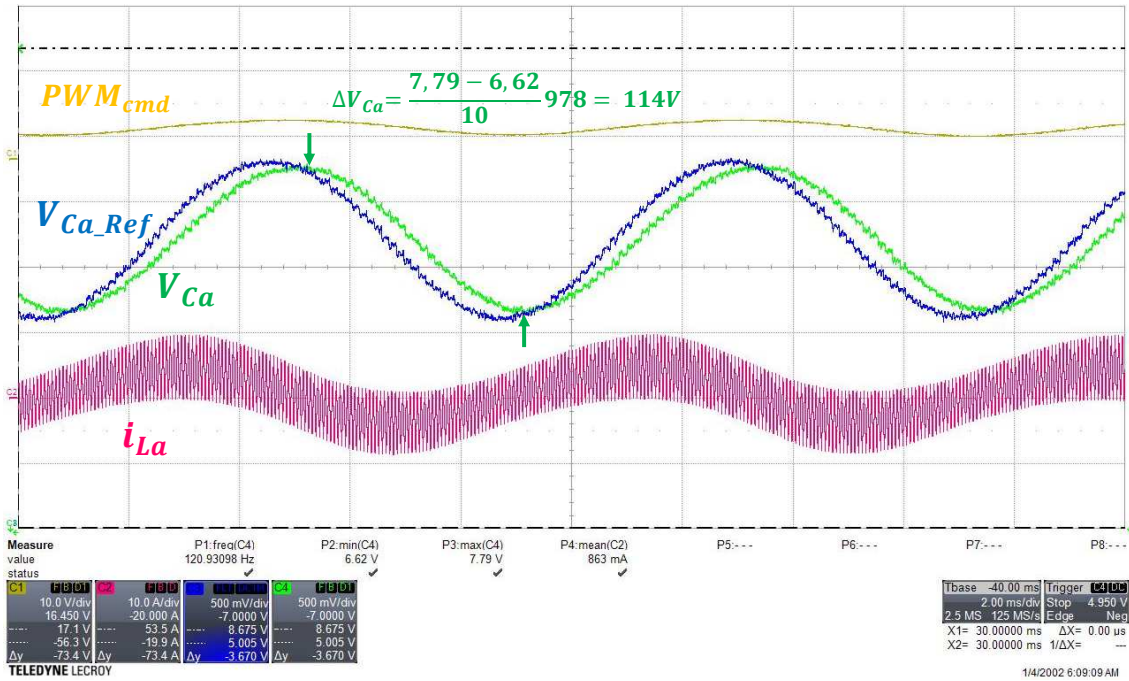
Figure 6-9: Zoomed area of the PWM command, auxiliary capacitor voltage reference, auxiliary capacitor voltage and auxiliary inductor current when a voltage ripple equal to 114 V is added to the voltage command (Scale between -10 V and 10 V, to calculate the real values the signals must be divided by 10 V first and then multiplied by the correspondent p.u value ($V_{pu} = 978V$, $I_{pu} = 35A$)).

Once the performance of the close loop control was tested and validated, the UPDU was ready to be connected with the PWM rectifier. To check the performance of the whole system some experiments were carried out in the laboratory and are explained in the next chapter.

Chapter 7

Experimental Results

To validate the performance of the UPDU and the proposed control, some tests were carried out in the laboratory.

1. UPDU combined with a single phase AC/DC converter (full load and half load).

2. UPDU combined with a standalone mode inverter (linear and non-linear load).

Since each test has different test conditions, this chapter has dedicated one separate section for each of the tests.

7.1 UPDU combined with a single phase AC/DC converter

The UPDU was combined with a singe phase AC/DC converter that is currently being developed by ITRI's work team. Fig. 7-1 shows the circuit diagram of the converters used in the tests and their parameters are summarized in Table 7.1.

As it can be seen the parameters of the single phase AC/DC converter are widely different from those used in the simulations. The system is a 1.6 kW with a much bigger capacitor ($1.125mF$ instead of $0.11mF$) and a significant smaller inductor ($2.8mH$ instead of $6.1mH$). Such a big capacitor will involve a small voltage ripple at the dc-link and therefore the room of improvement for the UPDU should be reduced.
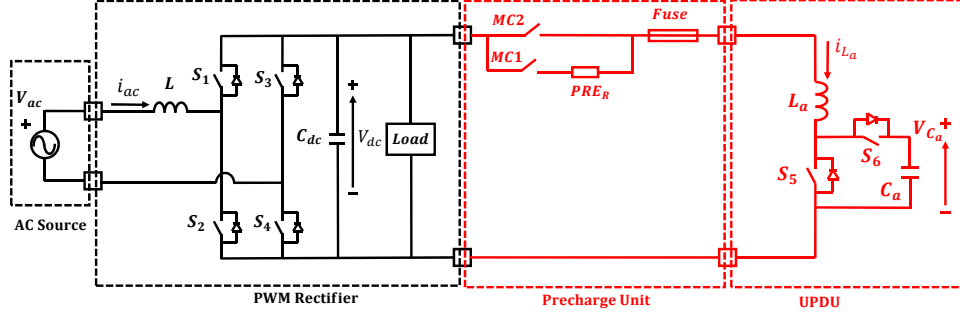
Figure 7-1: Circuit diagram of the UPDU combined with the single phase AC/DC converter tested in the laboratory.

Table 7.1: Parameters of the UPDU and the single phase AC/DC converter tested in the laboratory.

Sinple phase AC/DC Converter		UPDU	
Parameter	Value	Parameter	Value
Input Voltage V_{ac}	$220V$	Auxiliary Capacitor Voltage V_{C_a}	$700V$
DC-link Voltage V_{dc}	$400V$	Switching frequency f_{sw_a}	$30kHz$
Grid frequency f	$60Hz$	Auxiliary Inductor L_a	$1,1mH$
Switching frequency f_{sw}	$15kHz$	Auxiliary Capacitor C_a	$49\mu F$
Input Inductor L	$2.8mH$		
DC-link Capacitor C_{dc}	$1,125mF$		
Power P	$1,6kW$		
Load R_{load}	96Ω		

Fig. 7-2 shows the sequence of the test carried out in the laboratory. In t_1 the system is started and the dc-link is precharged to 250 V. In t_2 the control of the single phase AC/DC converter is enabled and the dc-link capacitor voltage is controlled to 400 V. Once the system is stable the load is connected (t_3). With the single phase AC/DC converter in steady state condition (t_4), the UPDU is precharged to the dc-link voltage value (400V). After 5 seconds (t_5), the ramp-up module of the UPDU is enabled and the auxiliary capacitor is charged to 700 V. Then, in t_6, the ripple voltage control is activated. From that point on, the UPDU is under normal operation. In t_7, the UPDU is stopped, the auxiliary capacitor is discharged and the single phase AC/DC converter returns to its original operation.

Fig. 7-3 shows the dc-link voltage when the UPDU's ripple voltage control is activated. Fig. 7-4(a) and Fig. 7-4(b) show the dc-link voltage and the input current before and after the operation of the UPDU.
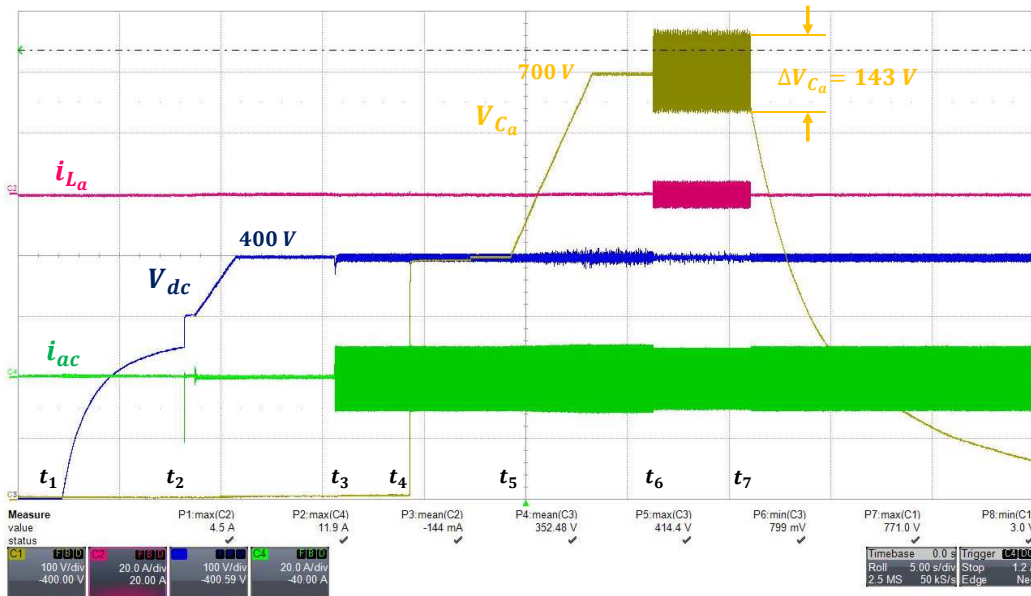
Figure 7-2: Operating sequence of the test carried out in the laboratory. Measured signals: auxiliary capacitor voltage V_{C_a}, auxiliary inductor current i_{L_a}, dc-link voltage V_{dc}, input ac current i_{ac}.
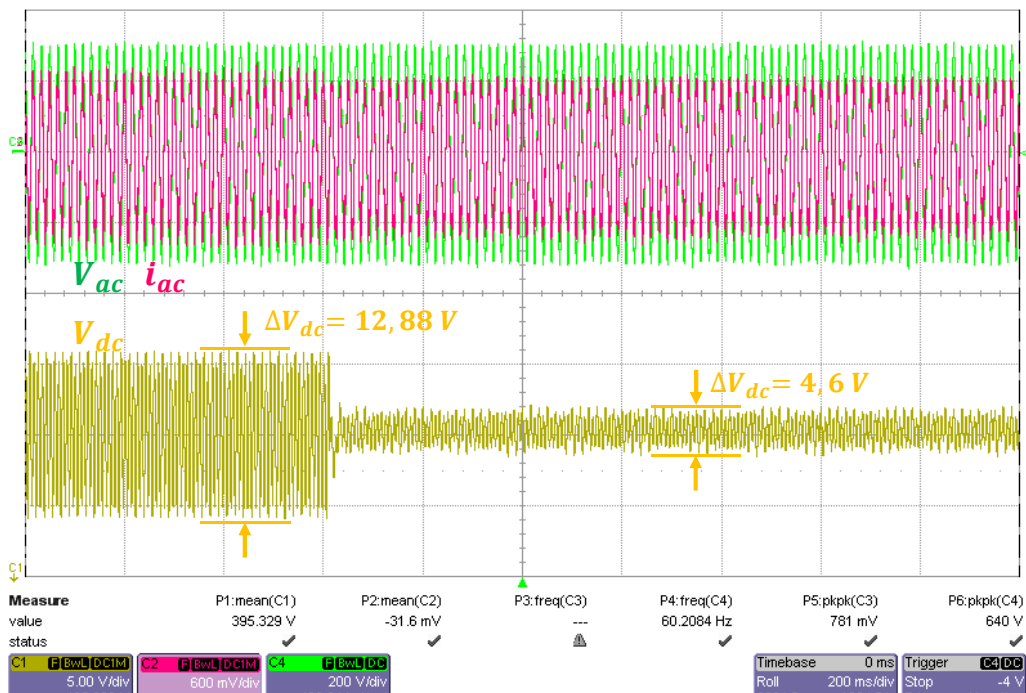
Figure 7-3: Input ac voltage V_{ac}, input ac current i_{ac} and dc-link voltage V_{dc} when the voltage ripple control of the UPDU is activated.
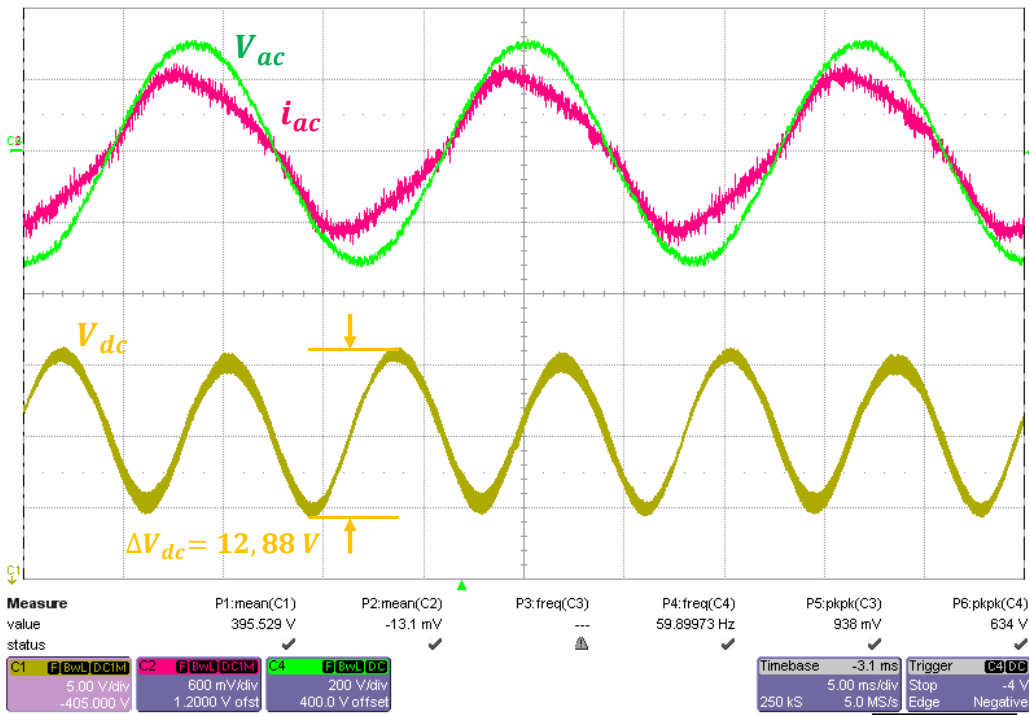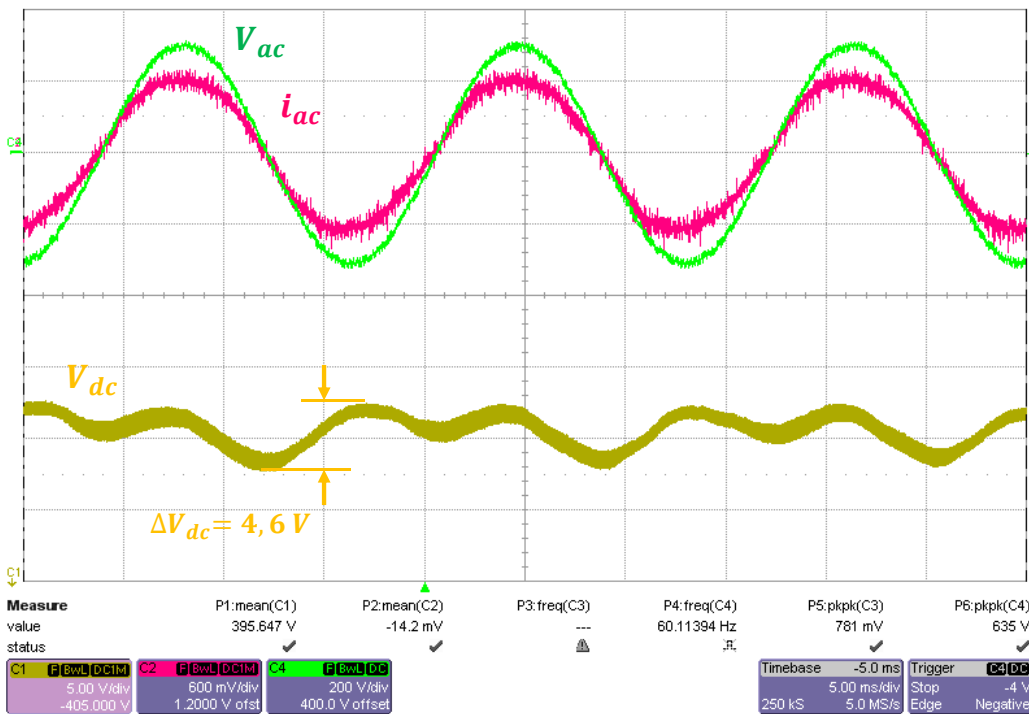
Figure 7-4: Input ac voltage V_{ac}, input ac current i_{ac} and dc-link voltage V_{dc} (a) before, and (b) after the UPDU's ripple voltage control is enabled.

As it can be seen before the UPDU's ripple voltage control is enabled, the expected voltage ripple caused by the 2nd order harmonic of the input power appears in the dc-link capacitor. It has a value of 12.88 V and a frequency of 120 Hz. Once the UPDU is under normal operation, the auxiliary capacitor experiences a voltage ripple of 144 V. It is much bigger than the one seen in the simulations (78 V). This is due to two facts:

- The input power is 1.6 kW instead of 1 kW. Thus, the voltage ripple of the auxiliary capacitor should be 1.6 times bigger than the expected ($78V \cdot 1.6 = 124V$).

- The real capacitance of the auxiliary capacitor is 49 μF instead of the 57 μF given by design. Thus, the voltage ripple of the auxiliary capacitor should be 1.18 times bigger than the expected ($124V \cdot 1.18 = 144V$).

Once the UPDU's ripple voltage control is enabled the dc-link voltage was reduced to 4.6 V (2.8 times). A 29 capacitance reduction was achieved in Chapter 4. Such a big difference in the obtained results is due to the following facts:

- A big electrolytic capacitor was used in the single phase AC/DC converter. As a consequence, the dc-link voltage ripple is only 3.22 % of the total value. Taking into account that it is impossible to completely eliminate the dc-link voltage ripple, the room of improvement for the UPDU was reduced with such a big dc-link capacitor.

- PSIM software allows to simulate electric circuits in ideal conditions. Thus, the proportional gain of the voltage controller was highly increased ($K_p = 28.5$) and no problems arise in the simulations. However, when testing the real converter, the K_p was limited to 8. A bigger value involves a very big current that trips the overcurrent protection. Thus the PSIM simulation was too ideal and a smaller K_p (and therefore bigger ripple voltage) should have been used.

In any case the proposed control for the UPDU can be validated since it has been proved that the voltage ripple was effectively reduced.

Having the single phase AC/DC converter a cascaded control with an outer voltage loop and an inner current loop, any dc-link voltage fluctuation has a direct impact on the input current. This, together with the use of a small input inductor can make the input current to be quite distorted. This is the case seen in Fig. 7-4(a) where the input ac current was highly distorted compared with the input ac voltage. Then, with the dc-link voltage improvement the input current was highly improved as Fig. 7-4(b) shows. The input current THD was measured with a power meter before and after the compensation. Fig. 7-5(a) and Fig. 7-5(b) show the obtained results respectively.

(a)   (b)
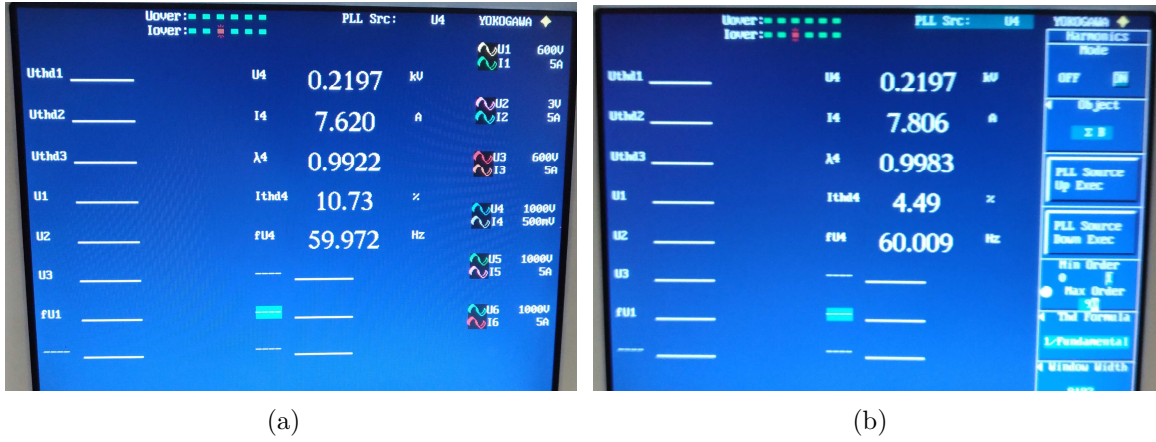
Figure 7-5: Input current THD (a) before compensation (b) after compensation.

As it can be seen the input current THD was highly reduced from 10.73% to 4.49%. However, nothing comes for free and the power efficiency was reduced when the UPDU was activated. Fig. 7-5(a) and Fig. 7-5(b) also show the input power measurement. It can be noted that once compensation was achieved, the input power was increased. This is because the UPDU introduced some power losses, and, since the load power must be constant, the input power must be increased to account for the UPDU's power losses. The efficiency was therefore reduced 2.34% as shown below:

$$\eta_{before} = \frac{P_{load}}{P_{input}} = \frac{\frac{V_{dc}^2}{R_{load}}}{V_{ac}i_{ac}} = \frac{\frac{396.7^2 V}{96\Omega}}{219.7V \cdot 7.62A} = \frac{1639W}{1674W} 100 = 97.92\% \qquad (7.1)$$

$$\eta_{after} = \frac{P_{load}}{P_{input}} = \frac{\frac{V_{dc}^2}{R_{load}}}{V_{ac}i_{ac}} = \frac{\frac{396.7^2 V}{96\Omega}}{219.7V \cdot 7.81A} = \frac{1639W}{1714W} 100 = 95.58\% \qquad (7.2)$$

Another test with half load (0.8 kW, $R_{load} = 192\Omega$) was carried out in the laboratory. Fig. 7-6(a) and Fig. 7-6(b) show the input power and input current THD measured with the power meter before and after compensation respectively. Fig. 7-7(a) and Fig. 7-7(b) show the input voltage, input current and dc-link voltage before and after compensation respectively.

(a)　　　　　　　　　　　　　(b)
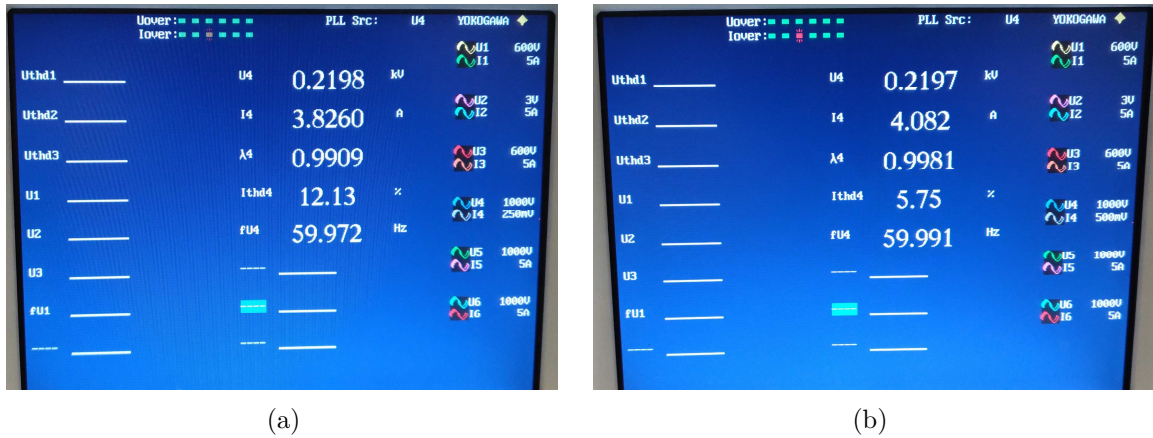
Figure 7-6: Input current THD (a) before compensation (b) after compensation with half load condition.

The efficiency in this case was reduced from 97.46% to 91.39% and the input current THD was improved from 12.13% to 5.75%. Thus with a lower input power the power losses introduced by the UPDU have a bigger impact (efficiency reduced 6.1%).

For the dc-link voltage, half power means almost half dc-link voltage ripple (6.9V). After compensation, a voltage ripple equal to 3 V was measured in the dc-link capacitor. This means that the possible capacitance reduction was decreased from 2.3 with full load to 2.1 with half load. This validates the idea that the smaller is the dc-link voltage ripple, the lower is the room of improvement for the UPDU. Thus, for a future work, it would be interesting to check the operation of the UPDU with high power single phase AC/DC converters and with small film dc-link capacitors.
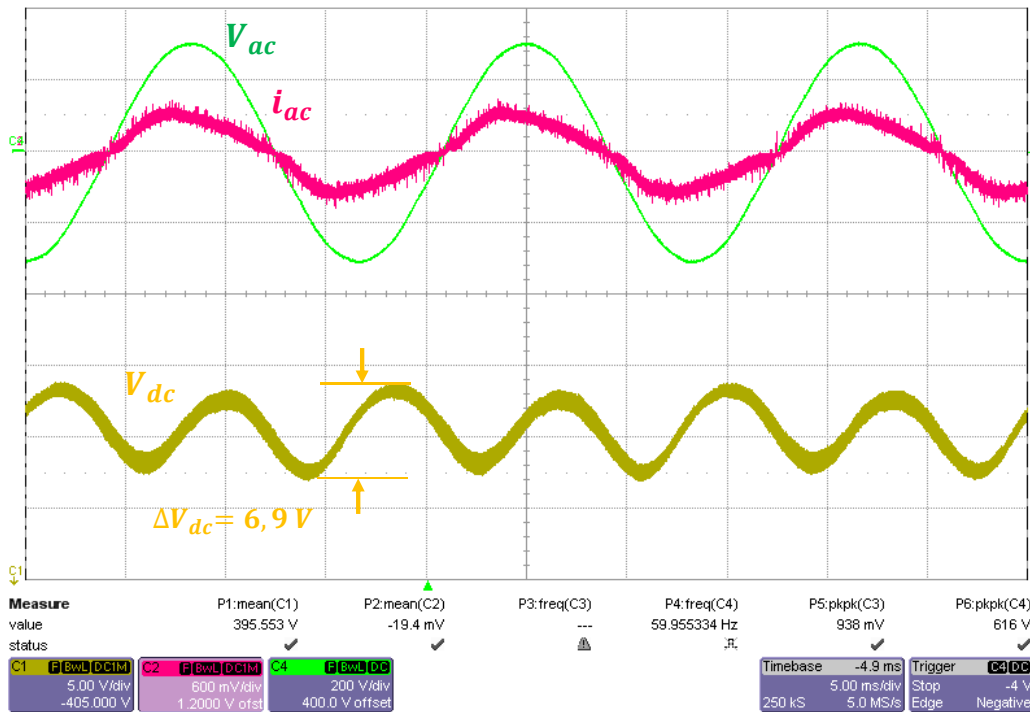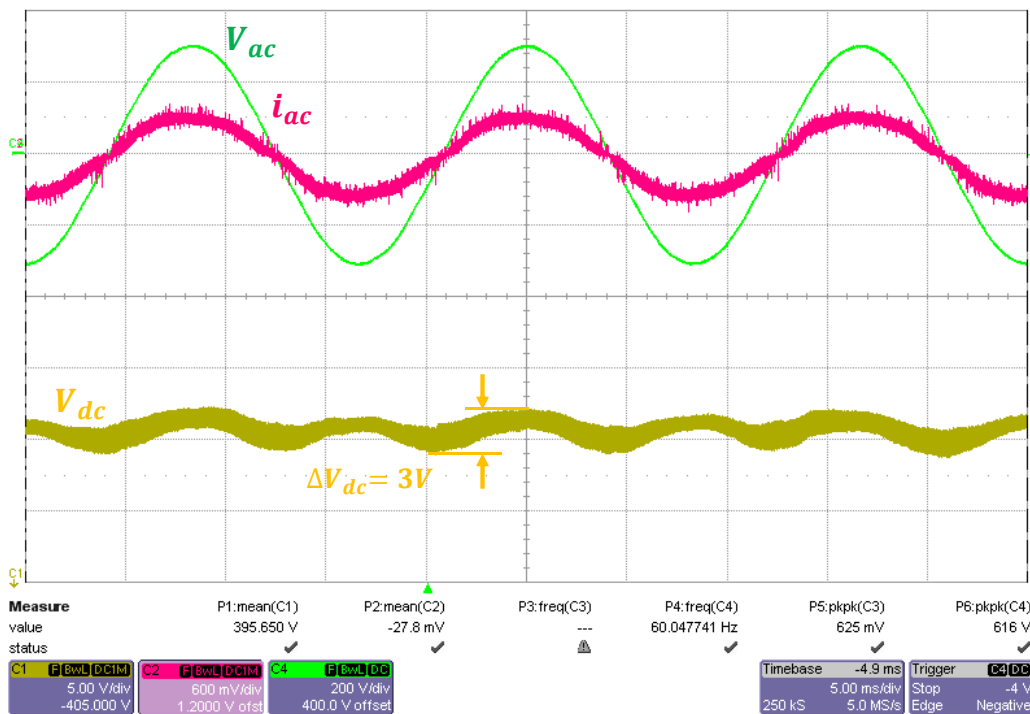
Figure 7-7: Input ac voltage V_{ac}, input ac current i_{ac} and dc-link voltage V_{dc} (a) before, and (b) after the UPDU's ripple voltage control is enabled with half load condition.

7.2 UPDU combined with a standalone mode inverter

A second test was carried out in the laboratory combining the UPDU with a standalone mode inverter that is currently being developed by ITRI's work team. The standalone mode inverter was designed for a home energy storage application. The basic idea is to have a battery controlled by a DC/DC converter that is connected to the house through a DC/AC inverter. Fig. 7-8 shows the circuit diagram of the UPDU combined with the standalone mode inverter tested in the laboratory. Their parameters are summarized in Table 7.2.
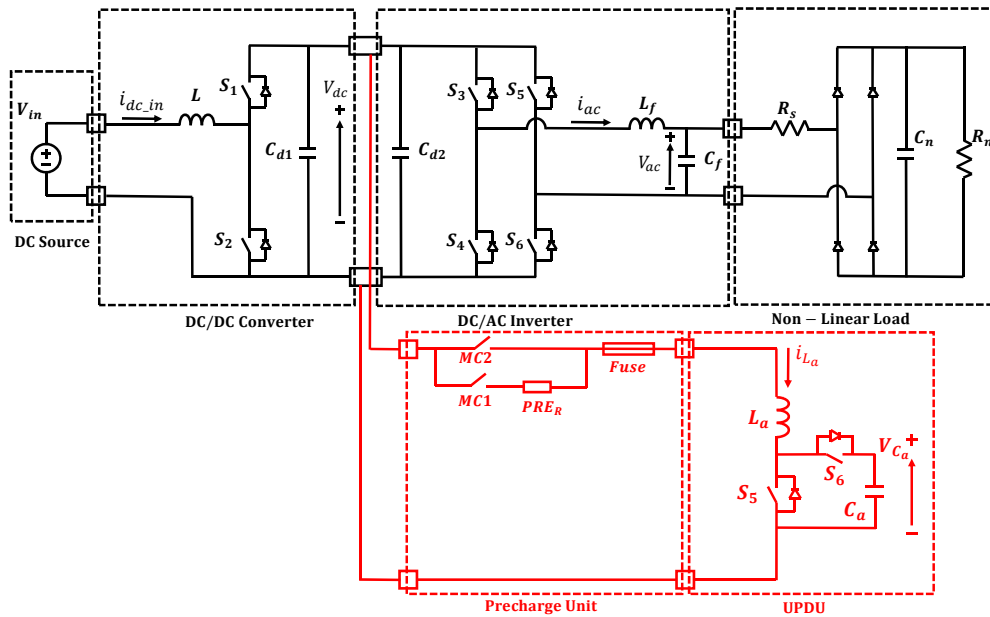
Figure 7-8: Circuit diagram of the UPDU combined with the standalone mode inverter tested in the laboratory.

To do the test the battery was replaced by a DC source and the house was emulated with a non-linear load. The design of the DC/DC converter, DC/AC inverter and the non-linear load are out of the scope of this thesis.

In the standalone mode inverter, there is a power fluctuation at the inverter's output. If no action is taken, the osctillating power flows to the input side of the dc/dc converter. With a constant dc-link voltage, oscillating power means oscillating current

Table 7.2: Parameters of the UPDU and standalone mode inverter tested in the laboratory.

DC/DC Converter		AC/DC Converter		UPDU		Non-linear Load	
Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
Input Voltage V_{in}	220V	DC-link Voltage V_{dc}	380V	Auxiliary Capacitor Voltage V_{C_a}	700V	Input Resistance R_s	6,2Ω
DC-link Voltage V_{dc}	380V	Switching frequency $f_s w_{ac/dc}$	6kHz	Switching frequency	30kHz	Capacitor C_n	680μF
Switching frequency $f_s w_{dc/dc}$	30,6kHz	Filter Inductor L_f	1,1mH	Auxiliary Inductor L_a	1,1mH	Resistor R_n	19,6Ω
Input Inductor L	2,48mH	Filter Capacitor C_f	1930μF	Auxiliary Capacitor C_a	49μF	Power P_n	1kW
DC-link Capacitor C_{dc1}	1930μF	DC-link Capacitor C_{dc1}	1440μF				

flowing through the battery. Such a ripple current will cause overheating and will shorten the lifetime of the battery. This problem is commonly avoided by making use of a big electrolytic capacitor that absorbs the ripple power. Thus, the objective of the UPDU in this case will be the same as in the single phase AC/DC converter. It must absorb all the ripple power. However, the benefit is not to have a lower dc-voltage ripple but a lower dc input current ripple. Fig. 7-9 shows the basic idea of the UPDU combined with the standalone mode inverter.
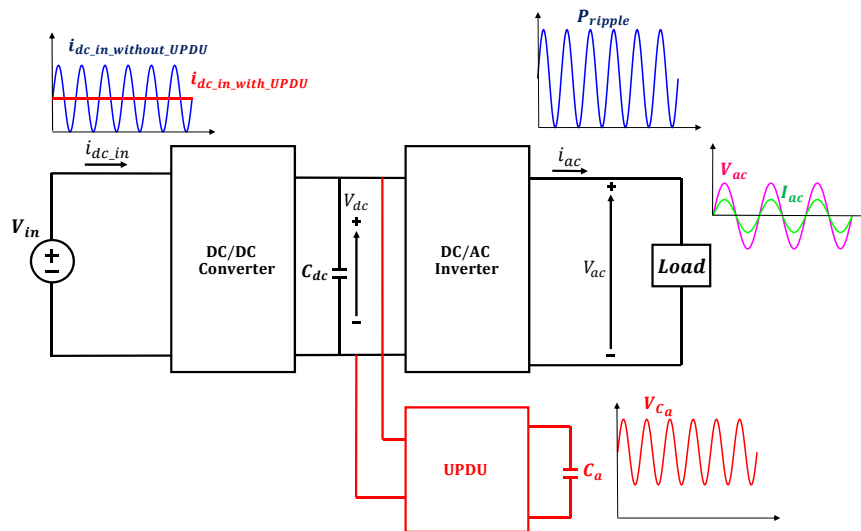
Figure 7-9: Basic idea of the UPDU combined with the standalone mode inverter.

The performance of the UPDU was firstly tested with a linear load and once the operation was validated, a test with a non-linear load was carried out. Fig. 7-10(a) and Fig. 7-10(b) show the ac voltage V_{ac}, ac current i_{ac}, ac power P_{ac}, input dc current i_{dc-in} and auxiliary capacitor voltage V_{C_a} before and after the connection of the UPDU with a 2.5 kW load.
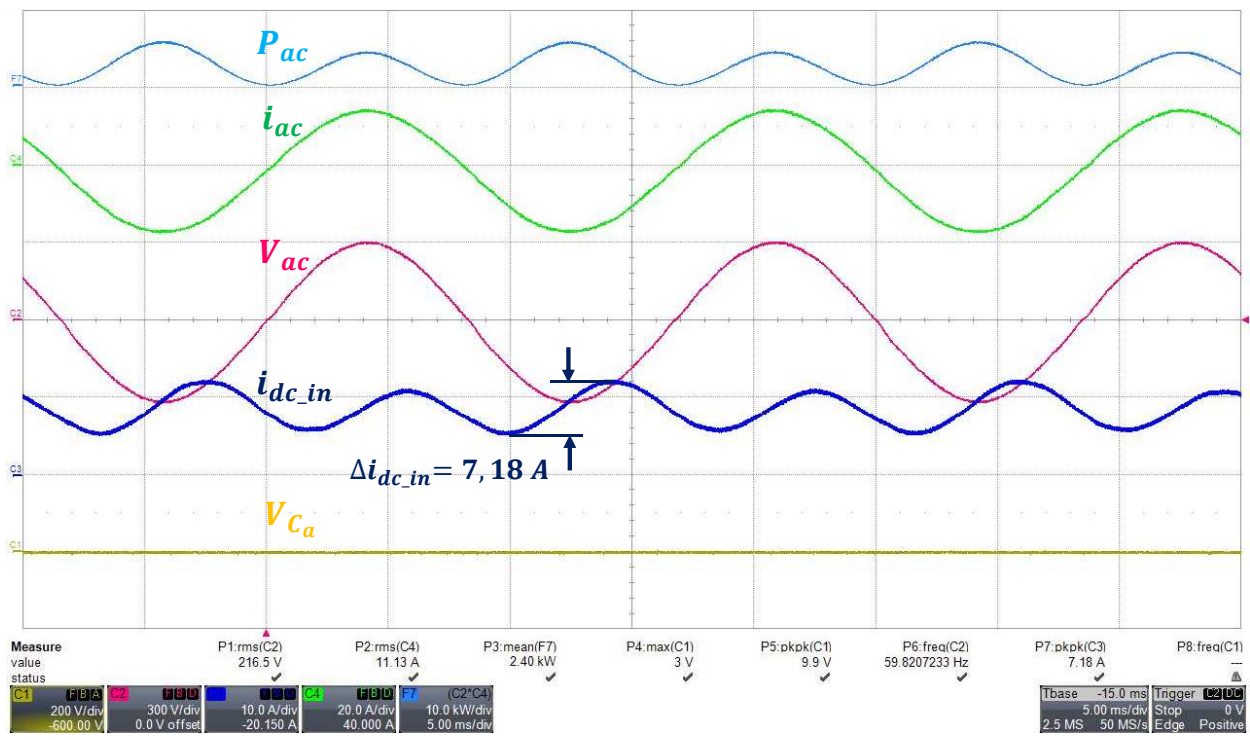
(a)
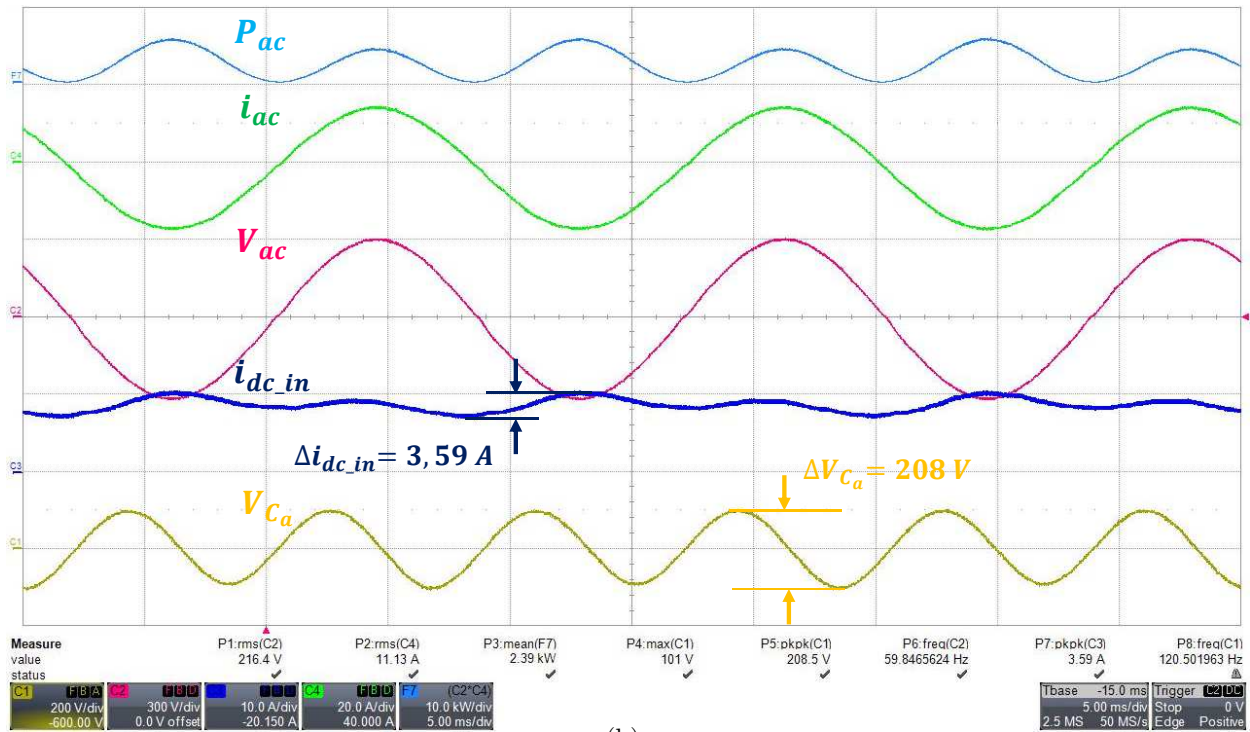
(b)

Figure 7-10: Measured ac voltage V_{ac}, ac current i_{ac}, ac power P_{ac}, input dc current i_{dc-in} and auxiliary capacitor voltage V_{C_a} (a) before and (b) after the connection of the UPDU with a 2.5 kW linear load.

As it can be seen in Fig. 7-10(a), due to the DC/AC inverter operation there is a pulsating power at 120 Hz at the system output. As a result the input dc current is oscillating with the same frequency and with a peak-to-peak value of 7.18 A. Once the UPDU was activated, a voltage ripple equal to 208 V appeared in the auxiliary capacitor. The power ripple was thus being absorbed by the UPDU and the input current ripple was reduced to 3.59 A (2 times). The dc input current was not completely smooth but the UPDU operation was validated. Some tests were done decreasing the load power in steps of 0.5 kW. Table 7.3 summarizes the results obtained.

Table 7.3: Amount of input current reduction for different loads.

| Power (kW)	$\Delta V_{C_a}(V)$	$\Delta I_{dc-in_{before}}(A)$	$\Delta I_{dc-in_{after}}(A)$	Improvement
2,5	208,5	7,18	3,59	2
2	170,6	5,89	2,98	1,98
1,5	129,4	4,6	2,56	1,75
1	93,2	3,17	2,11	1,5
0,5	58,1	1,79	1,58	1,33

As it happened with the single phase AC/DC converter, the bigger is the power the bigger is the room of improvement. However, the ripple currents obtained with the UPDU might not be acceptable for some applications and a redesign stage of the UPDU used might be required.

A last test under non-linear load conditions was carried out in the laboratory. It should be noted that the non-linear load injects harmonics that distort the ac voltage and ac current. Thus, the ripple power and therefore the input dc current are also distorted. Fig. 7-11(a) and Fig. 7-11(b) show the ac voltage V_{ac}, ac current i_{ac}, ac power P_{ac}, input dc current i_{dc-in} and auxiliary capacitor voltage V_{C_a} before and after the connection of the UPDU with a 1 kW non-linear load.

As expected the non-linear load was injecting harmonics and therefore i_{ac}, V_{ac} and consequently P_{ac} and i_{dc-in} were distorted. However, the performance of the UPDU was not affected and the input ripple current was reduced from 5.88 A to 2.61 A (2.25 times). The UPDU performance can be thus validated but as it happened with linear conditions a new design might be needed if a smoother dc current is required.
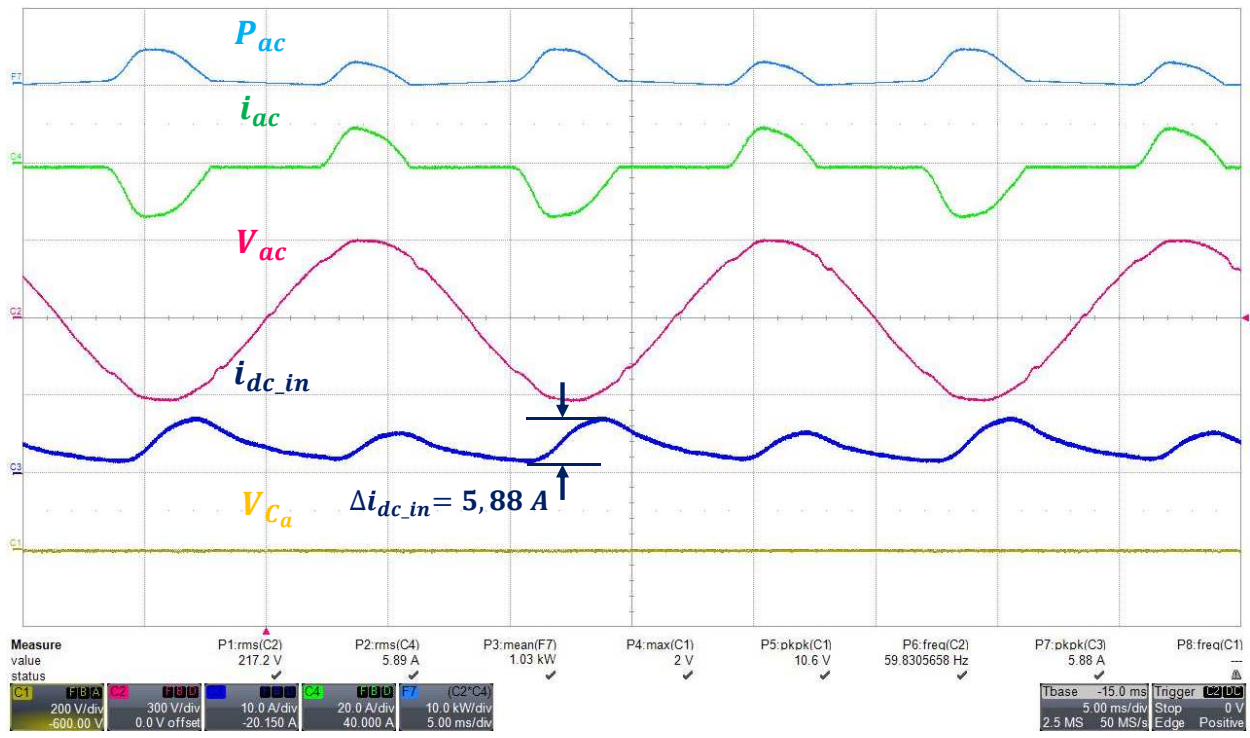
(a)
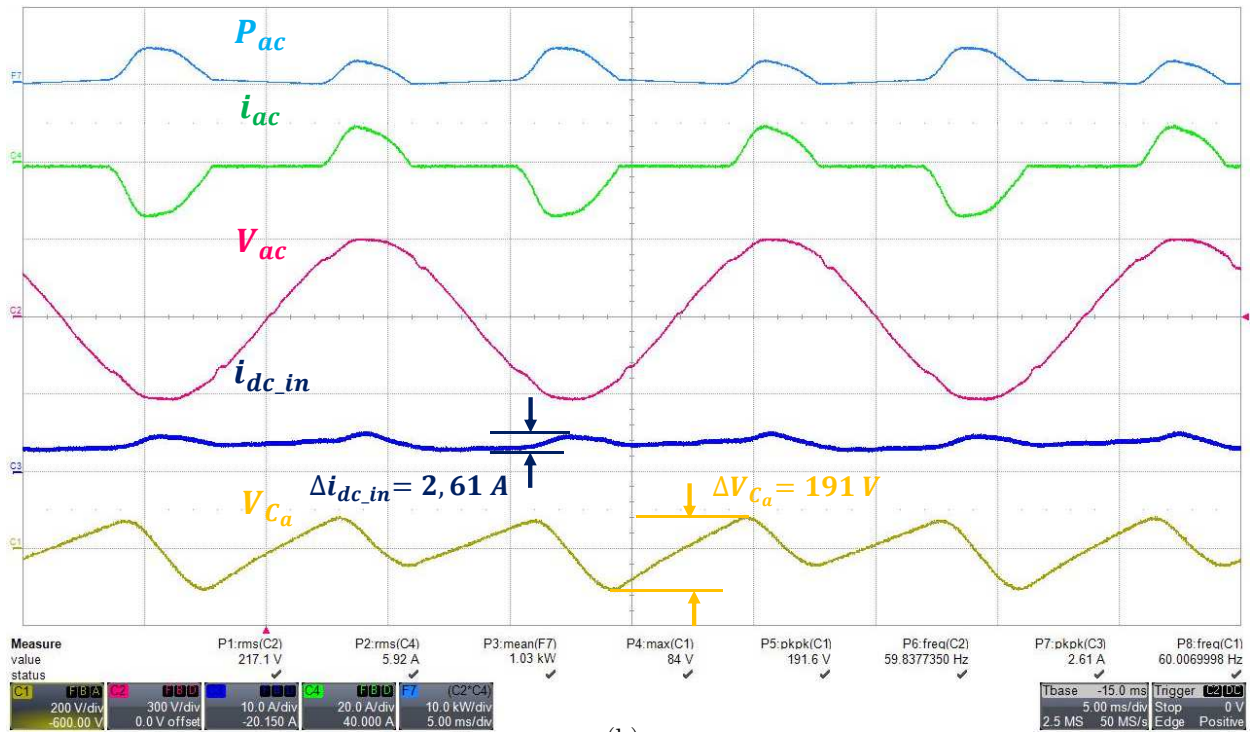
(b)

Figure 7-11: Measured ac voltage V_{ac}, ac current i_{ac}, ac power P_{ac}, input dc current i_{dc-in} and auxiliary capacitor voltage V_{C_a} (a) before and (b) after the connection of the UPDU with a 1 kW non-linear load.

Chapter 8

Conclusions and future developments

A Universal Power Decoupling Unit able to reduce the low frequency voltage ripple that appear in the dc-link of single phase AC/DC converters has been proposed in this thesis. The operational principles of the buck, boost and buck-boost converters used as ripple eliminators were analysed. It was seen how all of them are able to reduce the dc-link capacitance requirement avoiding thus the use of big electrolytic capacitors. After comparing the advantages and disadvantages of each topology, the bidirectional boost converter was considered to be the best option for the UPDU.

It was seen how the topologies proposed through the literature have a limitation. They need to be combined with the single phase AC/DC converter giving rise to a unique converter. To avoid this limitation, a new control strategy based on the voltage control of the UPDU's auxiliary capacitor was proposed and described. Its performance was validated through some PSIM simulations. It was seen how the proposed control allows to theoretically reduce 29 times the dc-link capacitor. To validate the theoretical analysis, some tests were carried out in the laboratory. A big electrolytic capacitor was placed in the dc-link of the single phase AC/DC converter. As a result, the room of improvement was reduced and only a 2.8 capacitance reduction was achieved. The input current THD was highly improved at the expense of a

2.34% efficiency reduction. With the performance of the control proposed validated, some test were done combining the UPDU with a standalone mode inverter. It was seen how the UPDU can reduce the input dc current ripple to half of its value under linear and non-linear conditions.

As a future work, new tests should be carried out in the laboratory. The following facts should be considering when performing the new tests.

1. The big electrolytic capacitor used in the dc-link must be replaced by a small film capacitor.

2. The ac source input power must be increased.

By doing so, the maximum performance of the UPDU should be achieved. In the case of the standalone mode inverter application, some simulations should be carried out in PSIM and a new redesign stage of the UPDU components might be required.

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