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High Voltage 4H-SiC Power MOSFETs with Boron doped gate oxide

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***Abstract*—A new process technology for 4H-SiC planar power MOSFETs based on a Boron diffusion step to improve the SiO_2/SiC interface quality is presented in this work. Large area (up to 25 mm^2) power MOSFETs of three voltages ratings (1.7 kV, 3.3 kV and 4.5 kV) have been fabricated showing significant improvements in terms of inversion channel mobility and on-resistance in comparison with counterparts without Boron oxide treatment. Experimental results show a remarkable increase of the channel mobility, which raises the device current capability, especially at room temperature. When operating at high temperature, the impact of the high channel mobility due to Boron treatment on electrical forward characteristics is reduced as the drift layer resistance starts to dominate in the total on-state resistance. In addition, the 3rd quadrant characteristics approximate to those of an ideal PiN diode, and the device blocking capability is not compromised by the use of Boron for the gate oxide formation. The experimental performance in a simple DC/DC converter is also presented.**

***Index Terms*— Gate dielectric, High Voltage, Power MOSFET, SiC, Wide Band Gap Semiconductors.**

I. INTRODUCTION

TODAY, electricity accounts for 40% of primary energy consumption, which is expected to increase with the full introduction of renewable energies. It is expected that 80% of electricity will pass through some kind of power electronics by 2030 [1]. Power electronics plays a key role in the generation-storage-distribution cycle of the electric energy since the main portion of the generated electric energy is consumed after undergoing several transformations through power electronic converters. The largest portion of the power losses in power electronic converters is dissipated in their power semiconductor devices, and consequently the improvement of these power devices technologies is crucial to achieve a more rational use of the electric energy together with considerable improvements in efficiency, size and robustness of power converters.

At present, most power devices are based on the very well-established Silicon technology, covering a huge market of applications as low as 20 V up to several kV. However, Silicon material properties limit power devices' performances regarding blocking voltage capability, operation temperature and switching frequency. Therefore, new generations of power devices based on Wide Band Gap (WBG) semiconductor materials are mandatory for high efficiency power converters.

Silicon Carbide (SiC) is one of the most advanced WBG materials for power devices as far as commercial availability of starting high quality material (wafers and epitaxial layers) and maturity of their technological processes is concerned [2, 3]. However, the SiC high voltage capability is not fully exploited yet. SiC diodes have been available in the market for more than 15 years (recently up to 15 kV [4]), becoming key components in various power applications. SiC switches are relatively new in the market and systems designers are becoming familiar with them. The development of low resistance SiC power MOSFETs has been delayed due to the very low inversion channel mobility values (μ_{fe}), high threshold voltage (V_{TH}) instability, reduced maximum negative gate voltage and leakage through the channel at 0 V gate bias. These problems are mainly caused by a poor MOS interface quality, affected by large interface trap density (D_{it}) values. Improvements in the MOS interface quality have allowed the appearance of commercial SiC MOSFETs up to 1.2 kV - 1.7 kV [5, 6], and full SiC power modules with current capabilities in the range of 100 A [5-7]. It is expected that SiC MOSFETs will compete with Silicon IGBTs and will replace them up to 5 kV breakdown voltage in a near future.

This paper presents an innovative process technology for high voltage SiC power MOSFETs with a Boron doped gate oxide to improve the SiO_2/SiC interface quality. In the next sections, design considerations, process technology and experimental results of fabricated devices will be discussed. As it will be shown, significant improvements in terms of μ_{fe}, on-resistance (R_{DSon}), and 3rd quadrant behavior are obtained in comparison with counterparts without Boron treatment.

Manuscript received November 30, 2016; revised May 19, 2017; accepted May 26, 2017. This work has been partially supported by the EU through the SPEED FP7 Large Project (NMP3-LA-2013-604057) and by the research program from the Spanish Ministry of "Economía y Competitividad" HiVolt-Tech (TEC2014-54357-C2-1-R) cofunded by the EU-ERDF (FEDER).

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II. Design and Process Considerations

Fig. 1 shows the schematic cross-section of a vertical SiC power MOSFET. Several considerations arising from the SiC material properties must be taken into account for a proper device design.

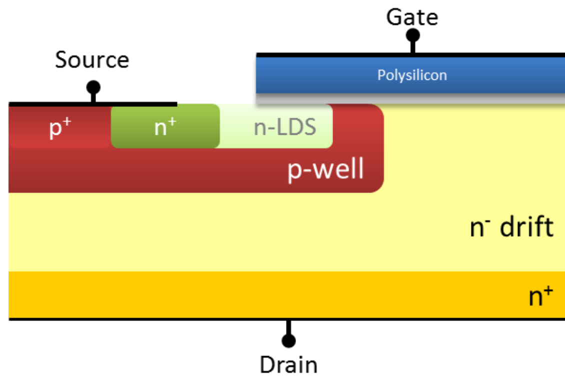
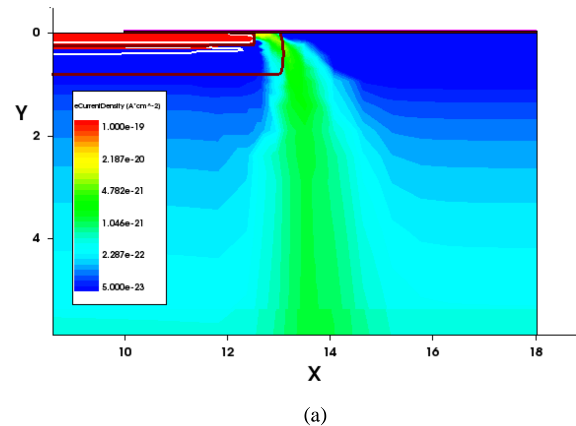


Fig 1. Schematic cross-section of a SiC power MOSFET half-unit cell.

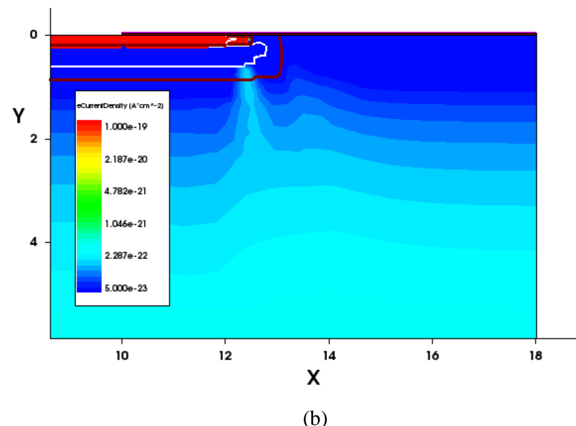
First, doped regions in SiC cannot be obtained by impurities thermal diffusion due to their low diffusion coefficient values. Hence, these regions are usually defined by multiple high energy ion implantations although shallow junction depths are obtained (typically below 1 μm). In addition, the epilayer doping level for a given blocking voltage is higher than that needed for a Silicon power MOSFET. Consequently, the extension of the depletion region within the p-well in the off-state can easily reach the n^+-source leading to a premature punch-through breakdown. Therefore, the p-well doping profile must be carefully designed to avoid the punch-through while maintaining the desired V_{TH} [8, 9]. Fig. 2 (a) highlights the punch-through of a power MOSFET with a non-optimized p-well doping profile by means of numerical simulations [10].

Another strategy to prevent the punch-through phenomenon is to increase the channel length but this has a negative impact on the device R_{DSon}, especially due to the low μ_{fe} values. Therefore, submicron channel lengths together with a suitable design of the p-well region are needed to reduce R_{DSon} and, at the same time, to avoid the punch-through. Fig. 2 (b) depicts the numerical simulation of the same power MOSFET with a higher p-well doping profile. As it can be inferred from this figure, the p-well doping level prevents the depletion region to reach the n^+-source.

The p-well doping profiles used for the simulation results shown in Fig. 2 are plotted in Fig. 3. In both cases, the resulting doping profile has been obtained by multiple Aluminum implantations allowing achieving a high doping level deep inside the p-well while maintaining a relatively low value at the surface in order to not compromise the V_{TH} value. The submicron channel length is obtained with a self-aligned process using a polysilicon layer through which both p-type and n-type impurities are implanted. After the p-type implantation, the polysilicon layer is oxidized, and then the n-type implantation is performed. The lateral length of the oxidized polysilicon defines the channel length.



(a)



(b)

Fig. 2. Simulated electrical current distributions in a SiC power MOSFET with (a) a non-optimized, and (b) an optimized p-well doping profile. V_{DS}=1.3 kV.

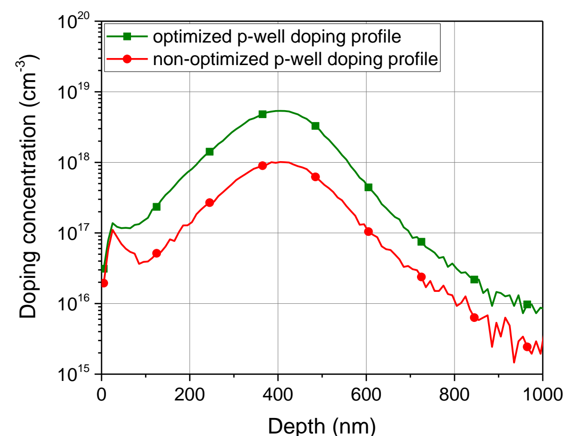


Fig. 3. Simulated one-dimensional p-well doping profiles.

On the other hand, one of the main issues in the SiC MOSFET technologies is the quality of the SiO_2/SiC interface. The large D_{it} values and the surface roughness severely affect μ_{fe} increasing the device R_{DSon} and compromising reliability. μ_{fe} values in SiC MOSFETs are more than one order of magnitude lower than in Silicon. Hence, new gate oxide configurations must be considered to improve the interface oxide quality and then μ_{fe}. Several technological solutions

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have been proposed to improve the MOS interface quality, such as the use of Nitrogen [11] or Phosphorus [12, 13] doping during post-oxidation. More recently, alkaline earth elements (Sr, Ba) [14, 15] have also been proposed to passivate charge traps and to generate counter doping effect at the SiO_2/SiC interface. In addition, different ionic species have been used to passivate the interface, for example Sb (μ_{fe} = 100 cm^2/(V·s)) [16] or La (μ_{fe}=130 cm^2/(V·s)) [17]. Recently, Okamoto et al [18] have proposed Boron diffusion in dry oxide to passivate dangling bonds, thus decreasing D_{it}. This approach allows obtaining high μ_{fe} values (μ_{fe}=100 cm^2/(V·s)) with a higher V_{TH} stability. Other groups have also obtained encouraging results by Boron treatments [19] with μ_{fe} up to 115 cm^2/(V·s).

An important issue in designing a SiC MOSFET is to prevent high electric field values at the gate oxide interface. Although the critical electrical field strength in SiC is one order of magnitude higher than in Silicon, the existence of high electric fields at the SiO_2/SiC interface could compromise either the gate oxide integrity or its reliability due to hot electrons injection into the oxide. Consequently, a shielded SiC MOSFET design is needed to ensure relatively low electric field values at the gate oxide interface [9].

Another design consideration is the use of a Low Doped Source (LDS) structure (see Fig. 1). It consists in a highly doped n^+-source tied to a lower doped n-region. Although this structure penalizes R_{DSon}, it allows limiting the μ_{fe} reduction effect and decreasing hot carrier injection into the oxide [20].

III. Design and Process Technology

4H-SiC vertical power MOSFETs of voltage classes targeting 1.7 kV, 3.3 kV and 4.5 kV have been fabricated with a process technology having 13 photolithographic steps. Table I shows the SiC epilayer properties used to fabricate devices of three voltage classes. The mask set includes small and large area (up to 25 mm^2) power MOSFETs, lateral n-MOSFETs and test structures. The p-well doping profile used for all the devices is the optimized one shown in Fig. 3. Fig. 4 shows a picture of the fabricated monitor chip.

TABLE I
SiC epilayer parameters

Voltage class (kV)	Thickness (µm)	Doping concentration ($\times 10^{15}$ cm^{-3})
1.7	15	5
3.3	34	1.5
4.5	40	1

A new gate oxide configuration based on a Boron diffusion step has been considered. Unlike [18], where a simple thermal dry oxide was used, the gate oxide presented in this work consists of a rapid thermal oxide (RTO) grown in N_2O ambient similar to the one in [21], in which Boron diffusion is carried out by means of BN planar sources [22, 23]. Finally, a PECVD TEOS oxide is deposited on top (see Fig. 5), resulting in total oxide thickness around 100 nm. Boron concentration is equally distributed in the thermal oxide, and no Boron impurities have been found in the TEOS. SIMS measurements have also shown that Boron atoms do not penetrate into the SiC crystal [23,24]. In addition, these measurements have also evidenced a lack of Boron concentration uniformity across the wafer and, consequently, more effort will be further required to optimize the Boron diffusion process to avoid spreading in device performance.

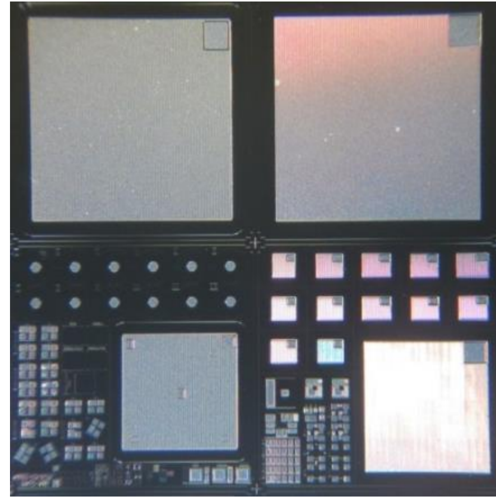

Fig. 4. Photograph of the monitor chip showing four large area power MOSFETs and test structures.

Furthermore, the power MOSFET edge termination consists in a Junction Termination Extension (JTE) with p-well guard rings surrounded by additional JTE rings with a total length of 158 µm [25]. Simulation results have shown good edge termination efficiency (defined as the ratio between breakdown voltage and parallel plane voltage) for all the three voltage class devices, and have also been confirmed on test structures showing efficiencies close to 90% [26, 27].

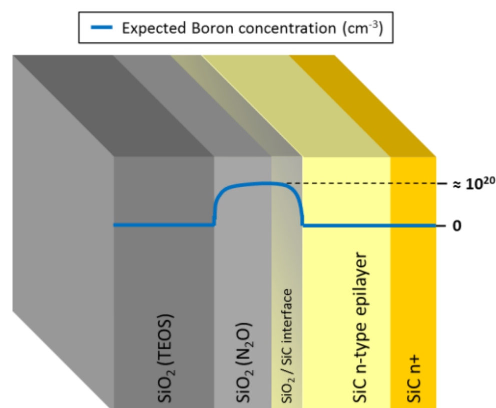

Fig. 5. Schematic cross-section of the gate oxide, SiO_2/SiC interface, and expected Boron concentration.

IV. Experimental Results

Fig. 6 shows the measured forward blocking characteristics of a power MOSFET for the three voltage classes.

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Independently of the voltage capability, similar blocking voltages have been obtained in devices with or without Boron diffusion into the gate oxide. This fact demonstrates that the Boron diffusion process does not affect either the edge termination area or its efficiency.

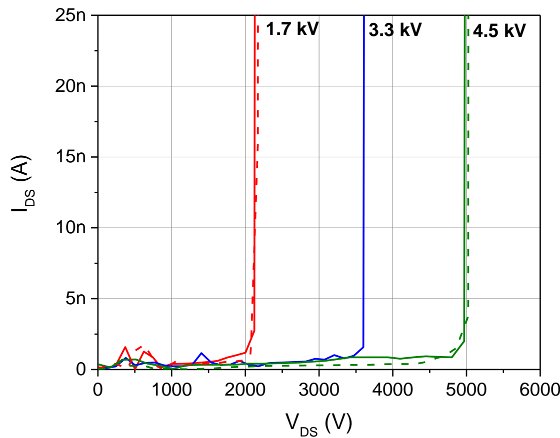


Fig. 6. Forward blocking characteristics of 25 mm^2 power MOSFETs with (solid) and without (dashed) Boron treatment.

Fig. 7 depicts the transfer characteristics of 25 mm^2 4.5 kV power MOSFETs with and without Boron diffusion treatment. As it can be seen, Boron significantly reduces the channel resistance component and also decreases the V_{TH} value. This V_{TH} reduction allows the use of both thicker gate oxides and higher p-well doping profiles, which are useful to prevent a premature punch-through as mentioned before. The V_{TH} (V_{GS} at which I_{DS} is equal to 1 mA) mean value is between 4 V and 5 V for the three voltage class devices with Boron diffusion process.

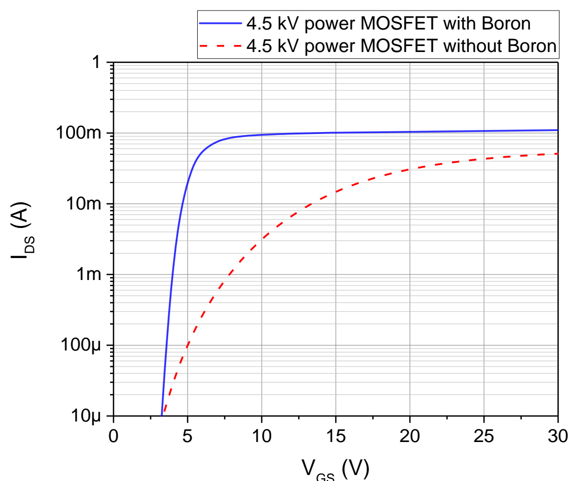
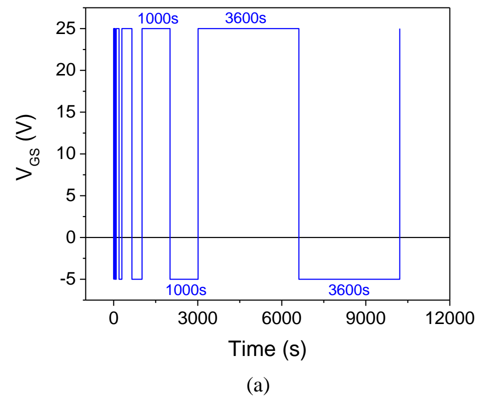
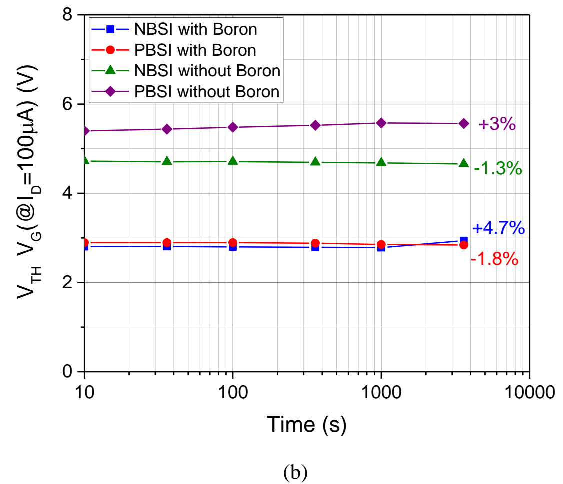


Fig. 7. Transfer characteristics of 25 mm^2 4.5 kV power MOSFETs. V_{DS}=0.1 V.

The maximum gate voltage before oxide degradation was 55 V, which is slightly lower than that measured on wafer without Boron (~ 60 V). Consequently, the Boron doping of the gate oxide does not significantly impact the gate oxide integrity. Moreover, it has only a slightly influence on V_{TH} stability. In this sense, Bias Stress Instability (BSI) tests have been carried out biasing the MOSFET gate between -5 V and +25 V following the sequence shown in Fig. 8 (a). Fig. 8 (b) depicts the resulting V_{TH} drift of power MOSFETs with and without Boron treatment under PBSI and NBSI stress.



(a)



(b)

Fig. 8. (a) Bias Stress Instability test sequence. (b) V_{TH} drift of 9 mm^2 power MOSFETs with and without Boron treatment under PBSI and NBSI stress at room temperature.

As it can be seen, after the last bias step of 3600s the V_{TH} drift of the power MOSFET with Boron is lower than 5% under negative BSI (NBSI) and 2% under positive BSI (PBSI). Hence, the V_{TH} stability is not significantly affected by the Boron gate oxide treatment. However, some improvements are still needed to reach the stability levels of commercial gate oxides showing nearly zero V_{th} drift after 1000 hours BSI test [28, 29]. On the other hand, the comparison of test structures with and without LDS structure on the same wafer has revealed that the LDS does not influence the V_{TH} stability. However, the V_{TH} drift under NBSI increases until 12% when the negative gate test bias is set to -10 V. These drift values are not as good as those obtained in novel power MOSFET generations. The trade-off between high mobility and V_{TH} stability is still a challenge we improved in this work but further optimizations are still needed.

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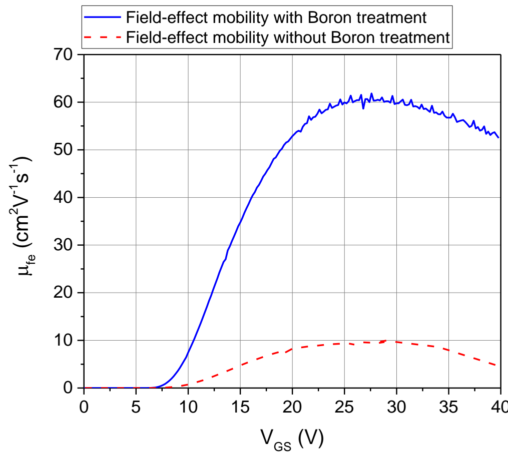


Fig. 9. Boron impact on the field-effect mobility. V_{DS}=0.1 V, L_{CH}=12μm.

Fig. 9 plots μ_{fe} obtained from the transconductance curves of lateral n-MOSFET test structures according to $\mu_{fe}=L(WC_{ox}V_{DS})^{-1}dI_{DS}/dV_{GS}$, where L and W are the channel length and width, and C_{ox} is the oxide capacitance per unit area. As it can be seen, the Boron treatment significantly increases μ_{fe} with values as high as 60 cm^2/(V·s) for normal gate operation biases. These values are lower than those reported in [18] because the p-well has been performed by multiple high-energy implantations. In our case, other lateral n-MOSFETs with the same gate oxide configuration fabricated on p-type epitaxied substrates exhibit μ_{fe} values as high as 160 cm^2/(V·s) [23, 30] which is 60% higher than the results reported in [18].

The experimental $I_{DS}(V_{DS})$ output characteristics of a large area 4.5 kV power MOSFET is presented in Fig. 10. The average measured R_{DSon} of the device active area at V_{GS}=20 V is 28 mΩ·cm^2, 45 mΩ·cm^2 and 62 mΩ·cm^2 for 1.7 kV, 3.3 kV and 4.5 kV devices at room temperature. These values are relatively high due to the large conservative cell pitch dimensions (36 μm). By reducing the cell pitch using stepper lithography the above mentioned values could be reduced by at least a factor of 2.

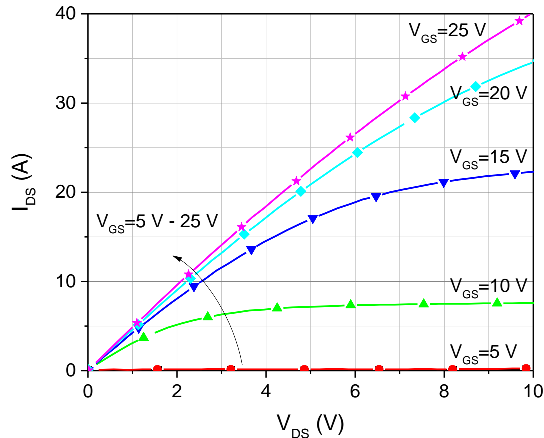
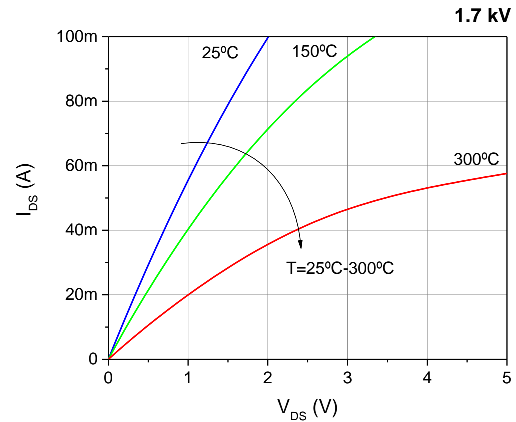
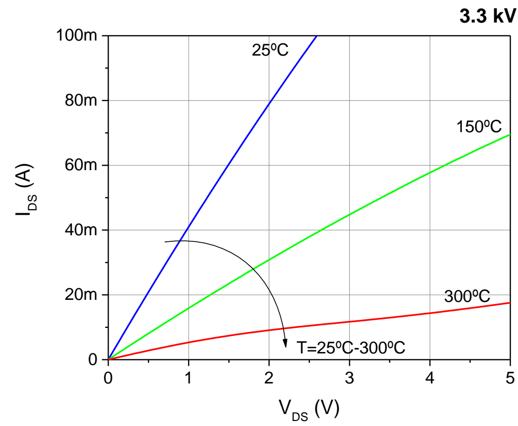


Fig. 10. Experimental output characteristics of a fabricated 25 mm^2 4.5 kV power MOSFET.



(a)



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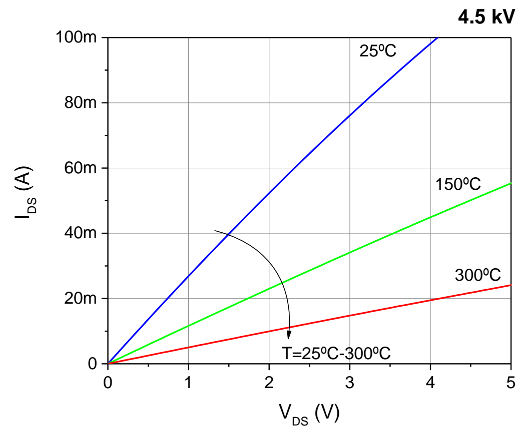

(c)

Fig. 11. Impact of temperature on the output characteristics of 0.8 mm^2 power MOSFETs with Boron treatment. (a) 1.7 kV, (b) 3.3 kV and (c) 4.5 kV. V_{GS}=20 V.

R_{DSon} values of power MOSFETs without Boron treatment are 4 to 5 times higher, thus showing the efficiency of the gate oxide Boron doping in reducing the on-state losses. As mentioned before, the μ_{fe} increase due to the Boron diffusion strongly raises the current capability at room temperature for all blocking voltage classes, and this current value decreases when raising temperature. However, power MOSFETs with and without Boron treatment show a different temperature behavior since the scattering mechanisms that affect μ_{fe} show

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different temperature dependences. Scattering with phonons are more effective at higher temperatures while scattering with surface interface traps becomes less effective as increasing temperature since the faster moving carriers interact less effectively with them. In the case of MOSFETs without Boron treatment (high D_{it}) the current capability increases as the temperature is raised from room temperature up to 150 ºC and then starts decreasing at higher temperatures. This is a due to the fact that, first mobility increases with temperature since scattering with interface traps predominate while at higher temperatures the mobility decreases due to phonon scattering. On the other hand, the current capability in devices with Boron diffusion in the gate oxide (low D_{it}) always decreases when increasing temperature due to the phonon scattering predominance. Figs. 11 and 12 show the impact of temperature on the output characteristics measured on small area power MOSFETs with and without Boron, respectively (only the output characteristics of structures with Boron treatment are represented in the case of 3.3 kV power MOSFETs since their counterparts without Boron were not fabricated). As it can be inferred from these figures, at 300ºC the current capability is very similar for devices with and without Boron diffusion for each blocking voltage since the major contribution of the drift layer to the R_{DSon}.

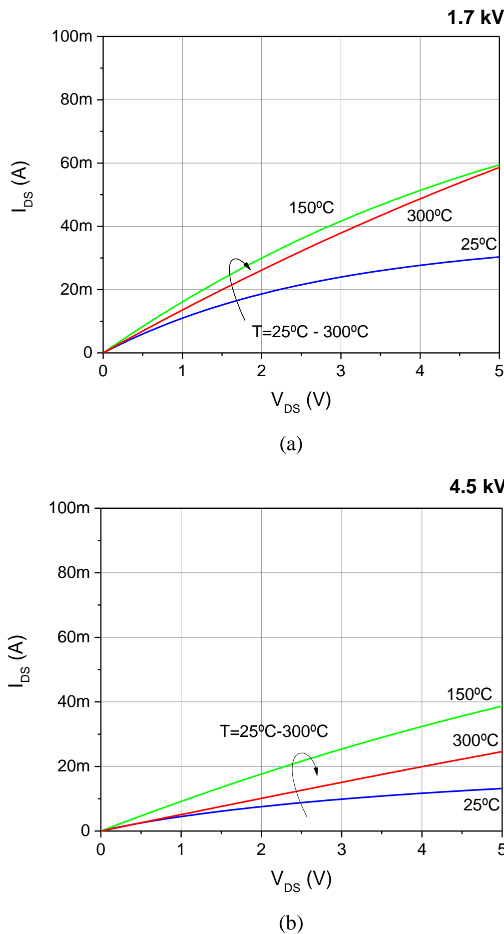

Fig. 12. Impact of temperature on the output characteristics of 0.8 mm^2 power MOSFETs without Boron treatment. (a) 1.7 kV and (b) 4.5 kV. V_{GS}=20 V.

The interface quality improvement by the Boron treatment of the gate oxide can also be inferred from the 3rd quadrant MOSFET characteristics [31, 32]. In this operation mode, there are two interacting paths for the current flow; i.e., through the PiN diode and through the MOS channel. The current through the channel is determined by the MOS gate bias which suffers from a V_{TH} reduction due to the body-effect [31]. The current through the channel is strongly affected by the interface quality, and can be suppressed by applying a negative gate voltage. The I(V) characteristics of fabricated devices have been measured to check the channel current flow at 0 V and at -4 V gate biases (see Fig. 13). As it can be seen, at V_{GS}=0 V current starts increasing for drain voltages lower than the p-n built-in potential (~2.5 V) although these voltages are higher in the case of devices with Boron treatment. Given that all fabricated devices have the same cell structure design, it could be another indication that Boron treatment improves the interface quality since the I(V) curve is closer to that of a PiN diode.

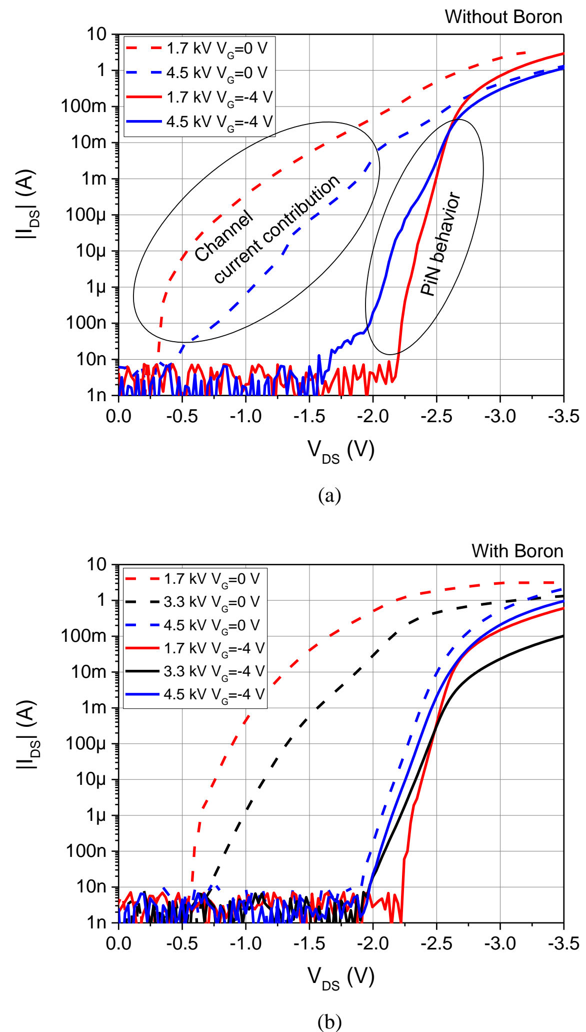

Fig. 13. 3rd quadrant I(V) characteristics at V_{GS}=0 V and V_{GS}=-4 V of 25 mm^2 fabricated power MOSFETs (a) without Boron treatment, (b) with Boron treatment.

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It is also clearly seen that the current through the channel is reduced when applying a -4 V gate bias as shown in commercial devices [32]. Concerning devices with Boron treatment, epilayers targeting 1.7 kV and 3.3 kV show different knee voltages at 0 V and -4 V while there is almost no difference for epilayers targeting 4.5 kV (both curves approach to that of an ideal PiN diode). In any case, a further negative increase of the gate voltage does not shift the diode characteristics.

The switching performance of fabricated MOSFETs has been preliminary tested using a resistive circuit. A low switching frequency ($f_{sw}\approx 1$ kHz) signal is applied to the gate of the 3.3 kV power MOSFET with a signal generator. The voltage applied to the gate to turn on and off the MOSFET are 20 V and -5 V respectively. Fig. 14 shows the experimental switching waveforms. The performance of the power MOSFETs under test has been analyzed in a simple DC/DC converter. A prototype of a boost converter was developed and used to test the switching behavior under inductive load. A PWM signal has been applied to the MOSFET gate using a driver to increase switching speed. The applied gate voltages to turn the MOSFET on and off were also 20 V and -5 V, and the switching frequency is 50 kHz. The experimental waveforms at V_{in}=0.5 kV, V_{out}=1 kV by the boost converter of approximately 1 kW are shown in Fig. 15. In this operation point, the efficiency of the boost converter was around 95%.

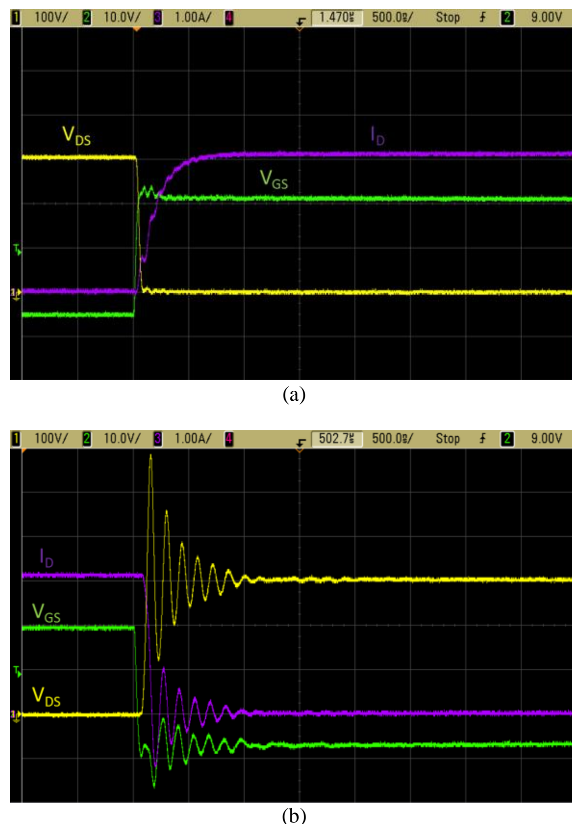

Fig. 14. Switching waveforms of a 3.3 kV MOSFET under resistive load. (a) turn-on and (b) turn-off.

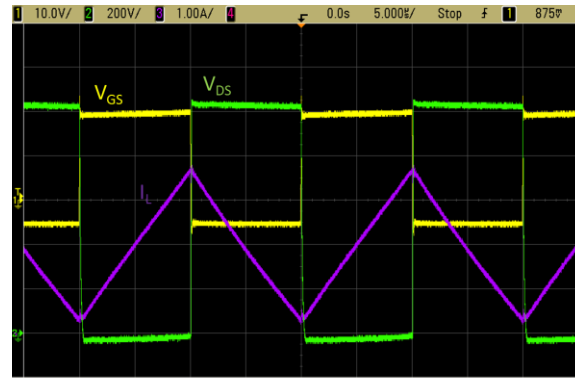

Fig. 15. Experimental waveforms of the boost converter at V_{in}= 500 V, V_{out}= 1000 V and P=1 kW.

V. Conclusion

The Boron gate oxide treatment presented in this work significantly improves the electrical characteristics of high voltage planar power MOSFETs with respect to counterparts without Boron diffusion. High voltage devices with voltage ratings up to 4.5 kV have been fabricated. The improvements include increase of inversion channel mobility and reduction of specific on-resistance. Moreover, the forward blocking capability and the threshold voltage stability are not significantly affected by the Boron treatment. Nevertheless, further improvements on V_{TH} stability are still needed. High temperature measurements have also shown that the channel contribution to the total on-resistance lowers as the temperature is increased. In addition, switching performance has been successfully tested in a simple DC/DC converter.

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2017.2723865, IEEE Transactions on Industrial Electronics

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2017.2723865, IEEE Transactions on Industrial Electronics

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