Modeling the Switching Behaviour of SuperJunction MOSFETs in Cascode Configuration with a Low Voltage Silicon MOSFET

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***Abstract*— This work presents a piecewise model to predict electrical waveforms of SuperJunction Cascode Configurations (SJ-CCs) during hard-switching operation. This ultra-fast high-voltage switch is composed of a SuperJunction MOSFET (SJ-FET) in Cascode Configuration (CC) with a Low-Voltage silicon MOSFET (LV-FET). SJ-CCs have been recently proposed as the first solution fully-based on silicon technologies that outperforms standalone SJ-FETs in high-frequency power converters. The model deeply explains its switching behaviour and it takes into account the most relevant parasitic elements and the strong non-linearity of the SJ-FET capacitances. Moreover, the model is validated with experimental measurements in a 240W boost converter using a SJ-CC composed of discrete devices.**

Keywords—Cascode configuration, hard-switching behaviour, model, silicon, SuperJunction MOSFET.

I. INTRODUCTION

High-Voltage (HV) SuperJunction MOSFET (SJ-FET) in the range of 600 V is one of the most used switches due to the mature and low price of its silicon technology. However, ultimate SJ-FETs are close to their theoretical limit of current density capability [1] which, in its turn, implies a limit on lowering its parasitic capacitances. In order to overcome the switching limitation of silicon technology, a recent work [2] proposed the use of a SJ-FET in Cascode Configuration (SJ-CC) with a Low-Voltage silicon MOSFET (LV-FET). Fig. 1 shows the schematic circuit of the ideal SJ-CC. The superior efficiency achieved by the SJ-CC in comparison with the same SJ-FET in standalone configuration was justified and demonstrated by simulation and experimentation in [3]. Despite of this, there is a lack of deep switching behaviour analysis of the SJ-CC.

The main purpose of this paper is to explain and to model the switching process of the SJ-CC during hard-switching operation. In order to achieve high accuracy, the developed model takes into account the main parasitic elements of the switch and the non-linearity of the SJ-FET capacitances. It should be noted that existing models for HV Wide Bandgap (WBG) transistors in Cascode Configuration (CC) with a LV-FET [4]-[6] do not provide an acceptable accuracy when a SJ-FET is used as HV switch. The causes are the contrasts between these WBG devices and the SJ-FETs. The main differences are the following:

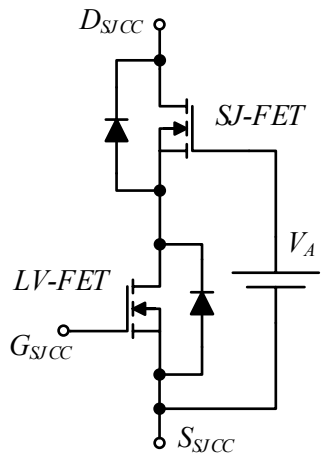

Fig. 1. Schematic circuit of the ideal SJ-CC.

1) The SJ-CC requires a constant voltage connected beetween the gate of the SJ-FET and the source of the LV-FET due to the positive threshold voltage of this HV device (see Fig. 1).

2) The magnitude of the parasitic capacitors and their non-linearity are more accentuated in a SJ-FET. Due to these facts the SJ-FET requires higher accuracy in the modeling.

This paper is organized as follows. In section II, the basis operation principle of the SJ-CC and the general description of the model are presented. Section II also includes the deep analysis of the turn-on and turn-off transitions. The experimental validation of the model by the use of a 240W boost converter is done in Section III. Finally, some conclusions are outlined in section IV.

II. SUPERJUNCTION CASCODE CONFIGURATION (SJ-CC) HARD-SWITCHING MODEL

A. Basic Operation Principle

The SJ-CC is composed of a SJ-FET as the HV switch driven by the constant voltage source V_A, and a LV-FET (see Fig. 1). During the off-state, the SJ-FET blocks most of the voltage and

the LV-FET blocks a voltage that is lower or equal to the avalanche voltage of its parasitic diode (V_{AV}). This work assumes that this parasitic diode always achieves the avalanche state. The gate to source voltage of the LV-FET (v_{GSLV}) is fixed by the output voltage of the driver (i.e. low-state) while the gate to source voltage of the SJ-FET (v_{GSHV}) is the difference between V_A and V_{AV}. During the on-state, v_{GSLV} is fixed by the output voltage of the driver (i.e. high-state) and v_{GSHV} is equal to the difference between V_A and the conduction voltage drop in the LV-FET (practically negligible). Hence, the channel of both MOSFETs conducts, being typically the 90% of the total on-resistance provided by the SJ-FET.

B. General Description of the Model

Fig. 2(a) shows the schematic circuit used to model the hard-switching process of the SJ-CC. It includes the nomenclature of the elements involved, and voltage and current references. The SJ-FET and the LV-FET are modelled as ideal switches that have a parasitic diode (D_{SJ} and D_{LV}) and their parasitic capacitances between gate and source (C_{GSHV} and C_{GSLV}), drain and source (C_{DSHV} and C_{DSLV}), and drain and gate (C_{DGHV} and C_{DGLV}). In the case of the SJ-FET, C_{DSHV} and C_{DGHV} are strong non-linear versus the drain to source voltage. Therefore, these capacitances suffer variations of several orders of magnitude during both transitions. A simple way to model this phenomenon is to consider two different values of C_{DSHV} and C_{DGHV} [7]. If the drain to source voltage of the SJ-FET is below a certain value (i.e. a frontier value that is typically fixed between 30V and 60V), both capacitances present a value of nF (C_{DSHV1} and C_{DGHV1}). On the other hand, if the voltage is above the frontier, these values are in the order of pF (C_{DSHV2} and C_{DGHV2}). These parameters should be extracted from the datasheet of the SJ-FET.

With respect to the parasitic inductors, the model assesses the role of the inductor that appears between the source of the SJ-FET and the drain of the LV-FET (L_{PAR}). It models the part of inductance introduced by the PCB and by the internal connection of the package of the each discrete MOSFET. As it will be detailed in sections II.C and II.D, the switching process hardly depends on this inductance. The parasitic inductors that exist in the drain connection of the SJ-FET, in the source connection of the LV-FET and in the gate connection of both MOSFETs are not included because they increase the complexity of the model. However, as will be demonstrated in section III, the accuracy provided by the model is high enough.

The LV-FET driver has been modelled as a PWM voltage source in series with a resistance (R_{GLV}) which includes the driver output resistance, the external gate resistance and the internal gate resistance of the LV-FET. In the case of the SJ-FET, there is a gate resistance (R_{GHV}) which includes the internal gate resistance of the SJ-FET and a possible external gate resistance.

The freewheeling diode D has been modelled has a SiC Schotky diode. This implies that there is not reverse recovery effect caused by the elimination of the minority carriers during the reverse recovery state. Hence, the only contribution to its turn-off comes from the charge of its parasitic capacitance (C_D). Due to this fact, this capacitance has been only taken into account during the turn-on of the SJ-CC. It is important to note that the effect of C_D during the turn-off of the SJ-CC is negligible.

The current source I_{LOAD} represents the current that flows through the inductive load. Always there is a certain amount of ripple current in the inductor of a converter. Therefore, the I_{LOAD} value should be changed depending on the transition. V_O represents the voltage that the SJ-CC must block during the off-state (i.e. the output voltage of a boost converter or the input voltage of a buck converter).

Equations (1)-(5) are obtained when net analysis is applied to the schematic circuit shown in Fig. 2(a). In a similar way, (6)-(10) are obtained after applying nodal analysis. The proposed model divides each transition in different stages. Every stage ends when an event that changes the behaviour of the SJ-CC occurs (i.e. a fully discharge of a parasitic capacitor, a change in the operation region of a MOSFET, etc.). In each stage, the standard equations shown below are particularized and solved numerically by MATLAB® due to the high complexity of the system. These particularizations will be described in next section. Moreover, at the end of each stage, the values of the voltages in the capacitors and the current through L_{PAR} are saved and used as the initial conditions of next stage. TABLE I shows the initial conditions of the beginning of each transition.

$$R_{GLV} \cdot i_{GLV}(t) + v_{GSLV}(t) = v_{DRI}(t), \tag{1}$$

$$v_{DSLV}(t) = v_{GSLV}(t) + v_{DGLV}(t), \tag{2}$$

$$L_{PAR} \cdot \frac{\partial i_{LPAR}(t)}{\partial t} + v_{DSLV}(t) + R_{GHV} \cdot i_{GHV}(t) + v_{GSHV}(t) = V_A, \tag{3}$$

$$v_{GSHV}(t) + v_{DGHV}(t) = v_{DSHV}(t), \tag{4}$$

$$v_{DSSJCC}(t) = v_{DSLV}(t) + L_{PAR} \cdot \frac{\partial i_{LPAR}(t)}{\partial t} + v_{DSHV}(t), \tag{5}$$

$$C_{GSLV} \cdot \frac{\partial v_{GSLV}(t)}{\partial t} = C_{DGLV} \cdot \frac{\partial v_{DGLV}(t)}{\partial t} + i_{GLV}(t), \tag{6}$$

$$C_{DGLV} \cdot \frac{\partial v_{DGLV}(t)}{\partial t} + C_{DSLV} \cdot \frac{\partial v_{DSLV}(t)}{\partial t} + i_{CHLV}(t) = i_{LPAR}(t), \tag{7}$$

$$C_{DGHV} \cdot \frac{\partial v_{DGHV}(t)}{\partial t} + i_{GHV}(t) = C_{GSHV} \cdot \frac{\partial v_{GSHV}(t)}{\partial t}, \tag{8}$$

$$C_{DSHV} \cdot \frac{\partial v_{DSHV}(t)}{\partial t} + i_{CHHV}(t) + C_{GSHV} \cdot \frac{\partial v_{GSHV}(t)}{\partial t} = i_{LPAR}(t), \tag{9}$$

$$i_{DSJCC}(t) = C_{DSHV} \cdot \frac{\partial v_{DSHV}(t)}{\partial t} + i_{CHHV}(t) + C_{DGHV} \cdot \frac{\partial v_{DGHV}(t)}{\partial t}. \tag{10}$$

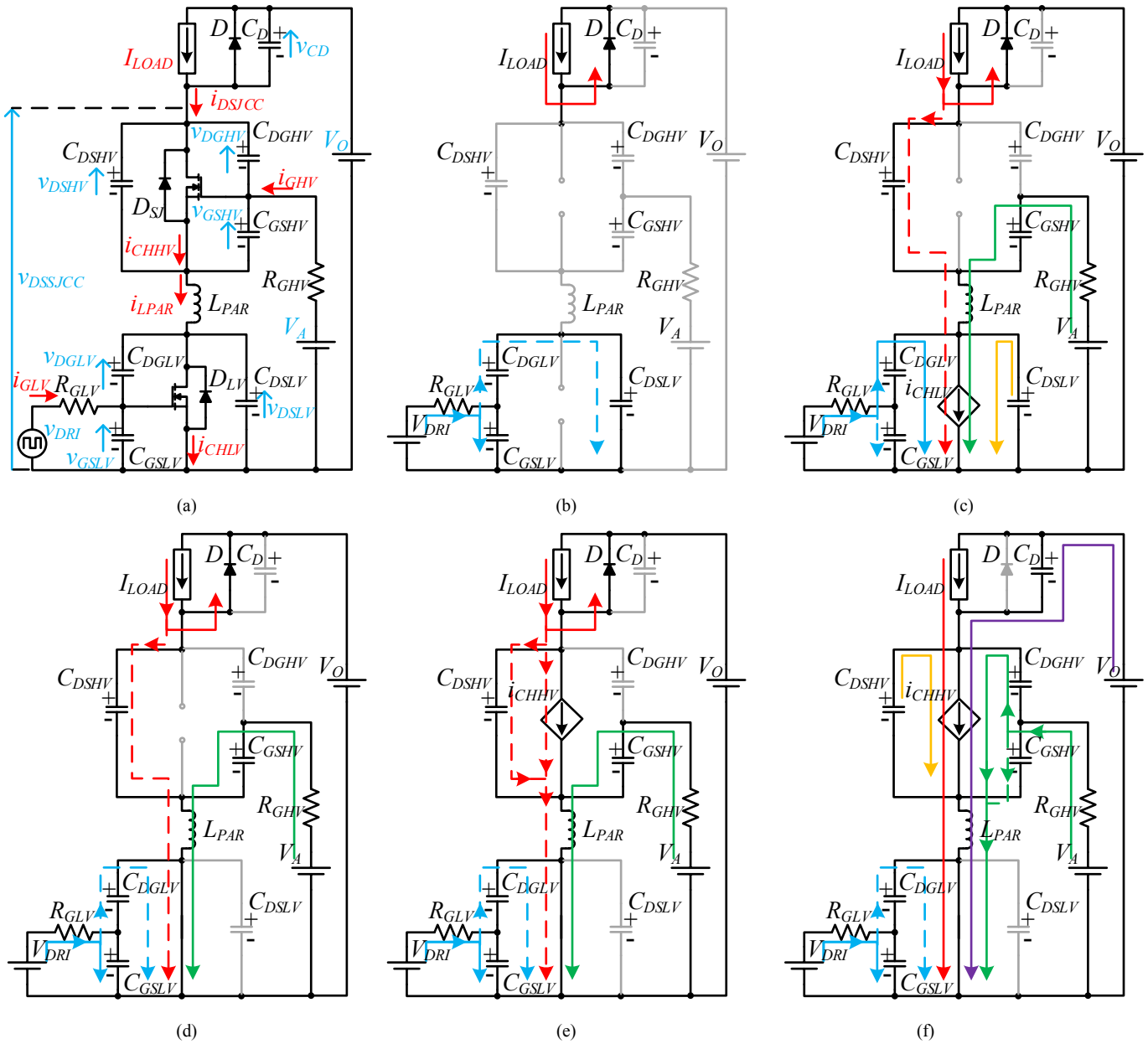

Fig. 2. (a) Schematic circuit used to model the switching process of the SJ-CC. Equivalent circuits during the turn-on transition: (b) stage I. (c) stage II. (d) stage III. (e) stage IV. (f) stage V.

As was indicated before, the parasitic capacitor of the freewheeling diode is only relevant during the turn-on. Due to this, (11) and (12) should be applied in this transition:

$$v_{CD}(t) + v_{DSSJCC}(t) = V_O, \tag{11}$$

$$I_{LOAD} + C_D \cdot \frac{\partial v_{CD}(t)}{\partial t} = i_{DSJCC}(t). \tag{12}$$

Fig. 2 also shows the equivalent circuit for each stage of the turn-on transition while the circuits for the turn-off can be found in Fig. 3. These stages will be introduced in sections II.C and II.D respectively. The components highlighted in grey represent

TABLE I: Initial conditions of the first stage of each transition.

	Turn-On	Turn-Off
$v_{GSLV}(0)$	0	V_{DRI}
$v_{DSLV}(0)$	V_{AV}	0
$v_{DGLV}(0)$	V_{AV}	$-V_{DRI}$
$v_{GSHV}(0)$	$V_A - V_{AV}$	V_A
$v_{DSHV}(0)$	$V_O - V_{AV}$	$R_{DSHV} \cdot I_{LOAD}$
$v_{DGHV}(0)$	$V_O - V_A$	$R_{DSHV} \cdot I_{LOAD} - V_A$
$v_{CD}(0)$	0	$V_O - R_{DSHV} \cdot I_{LOAD}$
$i_{LPAR}(0)$	0	I_{LOAD}

the elements that do not suffer any change either in their voltages or currents during the stage. The schematics also highlight the current paths depending on the source that injects the current:

Blue: current provided by the LV-FET driver.

Green: current provided by the constant voltage source V_A.

Red: current provided by the inductive load.

Purple: current provided by the constant voltage source V_O.

Orange: current provided by the discharge of a parasitic capacitor.

Current paths printed as a dash line represent the path that carries a current level much lower than the current that flows through other paths of the same source (i.e. same color). It is important to note that a current represented as a dash line could be bigger than other represented as a continuous line which comes from a different source (i.e. different color).

C. Turn-On Transition

Before the turn-on, both MOSFETs are modelled as open circuits (expressions (13) and (14) should be applied) and the current of the inductive load (I_{LOAD}) flows through the freewheeling diode *D*. Hence, its parasitic capacitance is discharged (15) and the voltage V_O is blocked by the SJ-CC. The model of the turn-on divides the transition into five stages and it starts when the output voltage of the driver changes from low-state to high-state. Therefore, (16) should be applied during all the turn-on transition.

$$i_{CHLV}(t) = 0, \tag{13}$$

$$i_{CHHV}(t) = 0, \tag{14}$$

$$v_{CD}(t) = 0, \tag{15}$$

$$v_{DRI}(t) = V_{DRI}. \tag{16}$$

Stage I: LV-FET Delay Period (Fig. 2(b)). v_{GSLV} raises because the driver charges C_{GSLV} and discharges C_{DGLV}. The small part of the current that flows through C_{DGLV} also flows through C_{DSLV}. However, v_{DSLV} hardly raises due to the little magnitude of the current and, therefore, it can be modeled as a constant voltage source with a value equal to its initial voltage (17). As a consequence, the variation of v_{GSHV} is negligible and the current through L_{PAR} is almost 0 (18). The stage ends when v_{GSLV} reaches the threshold voltage (V_{LVTH}) of the LV-FET.

$$v_{DSLV}(t) = V_{AV}, \tag{17}$$

$$i_{LPAR}(t) = 0. \tag{18}$$

Stage II: Current Source at the LV-FET Channel (Fig. 2(c)). The LV-FET channel behaves as a current source that depends on v_{GSLV} (19). As this voltage raises, the current increases. This current source discharges C_{DSLV} while the voltage source V_A starts to charge C_{GSHV}. The rise of v_{GSHV} is delayed with respect to the fall of v_{DSLV} due to L_{PAR}. Differently from the CCs composed of a WBG transistor as the HV switch [4]-[6], this delay is big enough to cause that the final event of this stage is the fully discharge of C_{DSLV}. During this stage, most of the current delivered by the driver flows through C_{DGLV} so v_{GSLV} remains almost constant (the Miller Effect occurs at the LV-FET). Unlike in standalone MOSFETs turn-on [8], v_{DSLV} falls and i_{CHLV} raises at the same time. It is important to note that C_{DGHV} can only be considered to be clamped while the freewheeling diode *D* remains in conduction state by considering R_{GHV} negligible (i.e. $R_{GHV} = 0$). At this point, an argument about internal gate resistance at SJ-FET must be developed. If an external resistance is not placed, R_{GHV} is equal to the internal gate resistance of the SJ-FET, and its value strongly depends on the architecture of the device (i.e. between 0.2 Ω and 6 Ω [9]). Taking into account these values, if an external resistance is not placed, R_{GHV} could be negligible for some SJ-FET architectures because (20) could be applied with no appreciable loss of accuracy. However, the model does not consider this simplification for the sake of being useful for different SJ-FET architectures. In order to reduce complexity, the explanation and the figures actually assume this simplification. Hence, the variation of the voltage of C_{GSHV} also is reflected in C_{DSHV}, which is charged by a small part of the current of the inductive load (see Fig. 5). The remaining part of I_{LOAD} keeps flowing through the freewheeling diode. This reasoning also will be valid during stages III and IV. Moreover, as v_{DSLV} falls, the voltage between the drain of the SJ-FET and the drain of the LV-FET rises (i.e. serial connection of C_{DSHV} and L_{PAR}). As was said before, the stage ends when v_{DSLV} achieves 0 V.

$$i_{CHLV}(t) = g_{mLV} \cdot (v_{GSLV}(t) - V_{LVTH})^2, \tag{19}$$

$$v_{DGHV}(t) = V_O - V_A. \tag{20}$$

Stage III: SJ-FET Delay Period (Fig. 2(d)). The LV-FET channel behaves as a resistance. In regular LV-FETs, this resistance is equal or lower than 20 mΩ. It can be considered a short circuit without appreciable loss of accuracy (21). Due to this, V_A continues charging C_{GSHV}, but now through a low resistive path (the current provided by V_A is higher than in the previous stage) that is composed of R_{GHV} and L_{PAR}. The Miller effect at the LV-FET has finished and C_{GSLV} and C_{DGLV} are charged and discharged respectively as fast as R_{GLV} allows. Due to the negligible on-resistance of the LV-FET channel, these charge and discharge are independent of the rest of the circuit. The stage ends when v_{GSHV} reaches the threshold voltage (V_{HVTH}) of the SJ-FET.

$$v_{DSLV}(t) = 0. \tag{21}$$

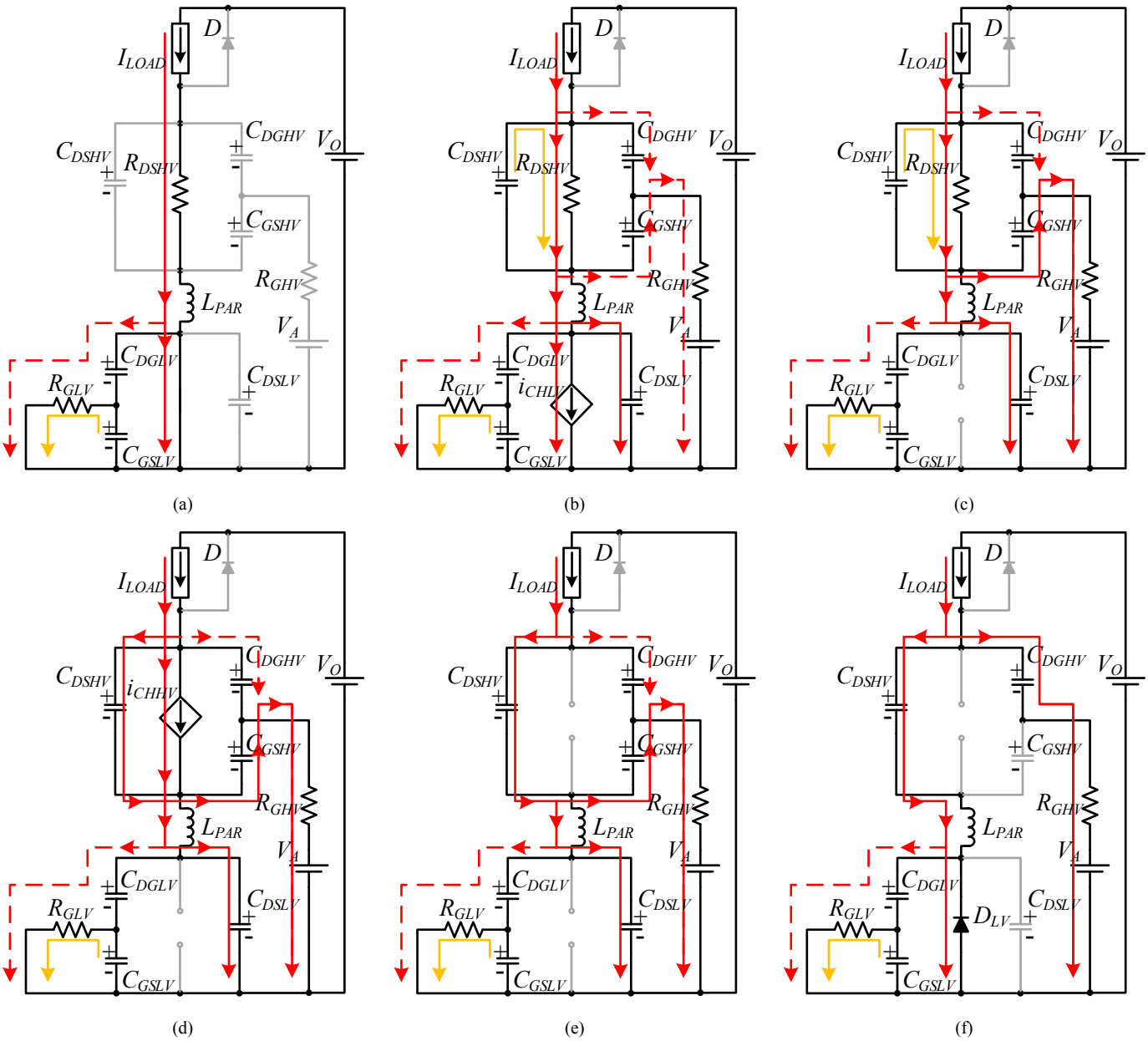

Fig. 3. Equivalent circuits during the turn-off transition: (a) stage I. (b) stage II. (c) stage III. (d) stage IV. (e) stage V. (f) stage VI.

Stage IV: Current Source at the SJ-FET Channel (Fig. 2(e)). The SJ-FET channel is modelled as a current source that depends on v_{GSHV} (22). The level of the current source comes from a part of the current of the inductive load and its magnitude increases as v_{GSHV} raises. As i_{CHHV} rises, the current through the freewheeling diode D falls. The stage ends when the whole drain current of the SJ-CC (i_{DSJCC}) is equal to I_{LOAD}.

$$i_{CHHV}(t) = g_{mHV} \cdot (v_{GSHV}(t) - V_{HVTH})^2. \tag{22}$$

Stage V: Fall of the SJ-FET Drain to Source Voltage (Fig. 2(f)). The SJ-FET channel is modelled as a current source that conducts I_{LOAD} and an extra level of current caused by the discharge of C_{DSHV}. The reverse recovery effect of the freewheeling diode occurs. Therefore, the SJ-FET channel also conducts the current that charges C_D (expression (15) is not applied). In addition, C_{DGHV} is not clamped during this stage. It starts to be discharged by a current provided by V_A. This current also flows through the channel of the SJ-FET. During this stage, the current that flows through C_{GSHV} is negligible. Hence, v_{GSHV} remains almost constant. In other words, the Miller effect occurs at the SJ-FET. At this point, it is important to say that the gate resistance of the SJ-FET implies a limitation of the current delivered by V_A. The lower value of R_{GHV}, the less significant Miller effect. The stage ends when v_{DSSJCC} is equal to $I_{LOAD} \cdot R_{DSHV}$ (being R_{DSHV} the on-resistance of the SJ-FET). Note that the dependence of C_{DSHV} and C_{DGHV} with v_{DSHV} should be applied in

this model for shaping the non-linearity of these capacitances during this stage.

D. Turn-Off Transition

Before the turn-off transition starts, the SJ-CC conducts all the current of the inductive load (23) while the diode *D* blocks V_O - I_{LOAD}·R_{DSHV}. As was previously said, the LV-FET channel is modelled as a short circuit (21). In the case of the SJ-FET, its on-resistance (R_{DSHV}) is not negligible. Hence, (24) should be applied. The transition starts when the output voltage of the driver changes from high-state to low-state and (25) should be applied during all the transition. The model divides this transition into six stages.

$$i_{DSJCC}(t) = I_{LOAD}, \tag{23}$$

$$v_{DSHV}(t) = R_{DSHV} \cdot i_{CHHV}(t), \tag{24}$$

$$v_{DRI}(t) = 0. \tag{25}$$

Stage I: LV-FET Delay Period (Fig. 3(a)). C_{GSLV} is discharged and injects current to the driver. A small part of I_{LOAD} flows through C_{DGLV} to compensate the fall of v_{GSLV}. The stage ends when v_{GSLV} reaches a value ($v_{GSLVLIN}$) that provides that the LV-FET enters into linear region. Assuming negligible the current through C_{DGLV}, $v_{GSLVLIN}$ can be obtained from (26).

$$g_{mLV} \cdot (v_{GSLVLIN} - V_{LVTH})^2 \cong I_{LOAD}. \tag{26}$$

Stage II: Current Source at the LV-FET Channel (Fig. 3(b)). The LV-FET channel behaves as a current source that depends on v_{GSLV} (27). As v_{GSLV} continues falling, the conductive capability of the LV-FET channel decreases and is not able to conduct all the current provided by the inductive load. The remaining I_{LOAD} charges C_{DSLV} and discharges C_{GSHV}. Moreover, other small part of I_{LOAD} continues flowing through C_{DGLV} in order to compensate the variations of v_{GSLV} and v_{DSLV}. The fall of v_{GSHV} is delayed with respect to the rise of v_{DSLV} due to L_{PAR}. As a consequence, the magnitude of the current that flows through C_{DSLV} during this stage is greater than the current that flows through C_{GSHV}. In addition, the raise of v_{DSLV} causes a partial discharge of C_{DSHV}. Finally, other part of I_{LOAD} charges C_{DGHV} in order to compensate the variations of v_{GSHV} and v_{DSHV}. The stage ends when v_{GSLV} achieves the threshold voltage of the LV-FET.

$$i_{CHLV}(t) = g_{mLV} \cdot (v_{GSLV}(t) - V_{LVTH})^2. \tag{27}$$

Stage III: Open Circuit at the LV-FET Channel (Fig. 3(c)). The previous reasoning about I_{LOAD} distribution is also valid during this stage. However, there are two differences. The first one is that there is no current flowing through the channel of the LV-FET because it is modelled as an open circuit (28). The second one is that the initial delay in the discharge of C_{GSHV} with respect to the charge of C_{DSLV} has expired and the magnitude of the currents that flow through both capacitances is similar. The stage ends when v_{GSHV} falls to a value ($v_{GSHVLIN}$) that causes that the SJ-FET enters into linear region. Assuming a negligible current through C_{DGHV} and a negligible current provided by the discharge of C_{DSHV}, $v_{GSHVLIN}$ can be obtained from (29).

$$i_{CHLV}(t) = 0, \tag{28}$$

$$g_{mHV} \cdot (v_{GSHVLIN} - V_{HVTH})^2 \cong I_{LOAD}. \tag{29}$$

Stage IV: Current Source at the SJ-FET Channel (Fig. 3(d)). The current paths are similar to the previous stage. The main difference is regarding that the SJ-FET channel is not able to conduct all I_{LOAD} because it behaves as a current source that depends on v_{GSHV} (30). As this voltage falls, the current through the channel decreases. Due to this, most of the remaining current of I_{LOAD} charges C_{DSHV} and a lower part charges C_{DGHV}. The sum of the currents that flow through C_{DSHV} and through the SJ-FET channel is distributed between C_{GSHV}, C_{DSLV} and C_{DGLV}. As in the previous stage, the magnitude of the currents that flow through C_{GSHV} and C_{DSLV} is similar while the magnitude of the current that flows through C_{DGLV} is lower. The stage ends when v_{GSHV} achieves the threshold voltage of the SJ-FET.

$$i_{CHHV}(t) = g_{mHV} \cdot (v_{GSHV}(t) - V_{HVTH})^2. \tag{30}$$

Stage V: Open Circuit at the SJ-FET Channel (Fig. 3(e)). The current paths are similar to the previous stage, but now there is not current flowing through the SJ-FET channel because it is modelled as an open circuit (31). The stage ends when v_{DSLV} achieves a value that causes that the LV-FET parasitic diode (D_{LV}) achieves avalanche state.

$$i_{CHHV}(t) = 0. \tag{31}$$

Stage VI: Remaining Charge of C_{DSHV} and C_{DGHV} (Fig. 3(f)). D_{LV} remains in avalanche state conducting most of the current that comes from the C_{DSHV} charge. D_{LV} can be modelled as a constant voltage source with the capability of flowing current

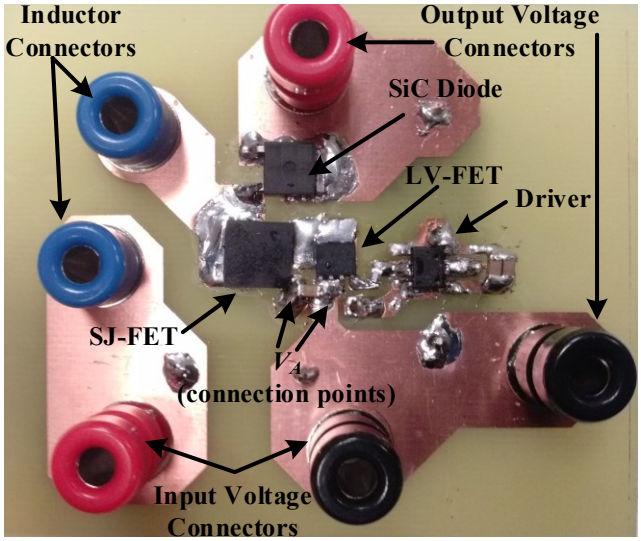

Fig. 4. 240W boost converter with a SJ-CC as the main switch.

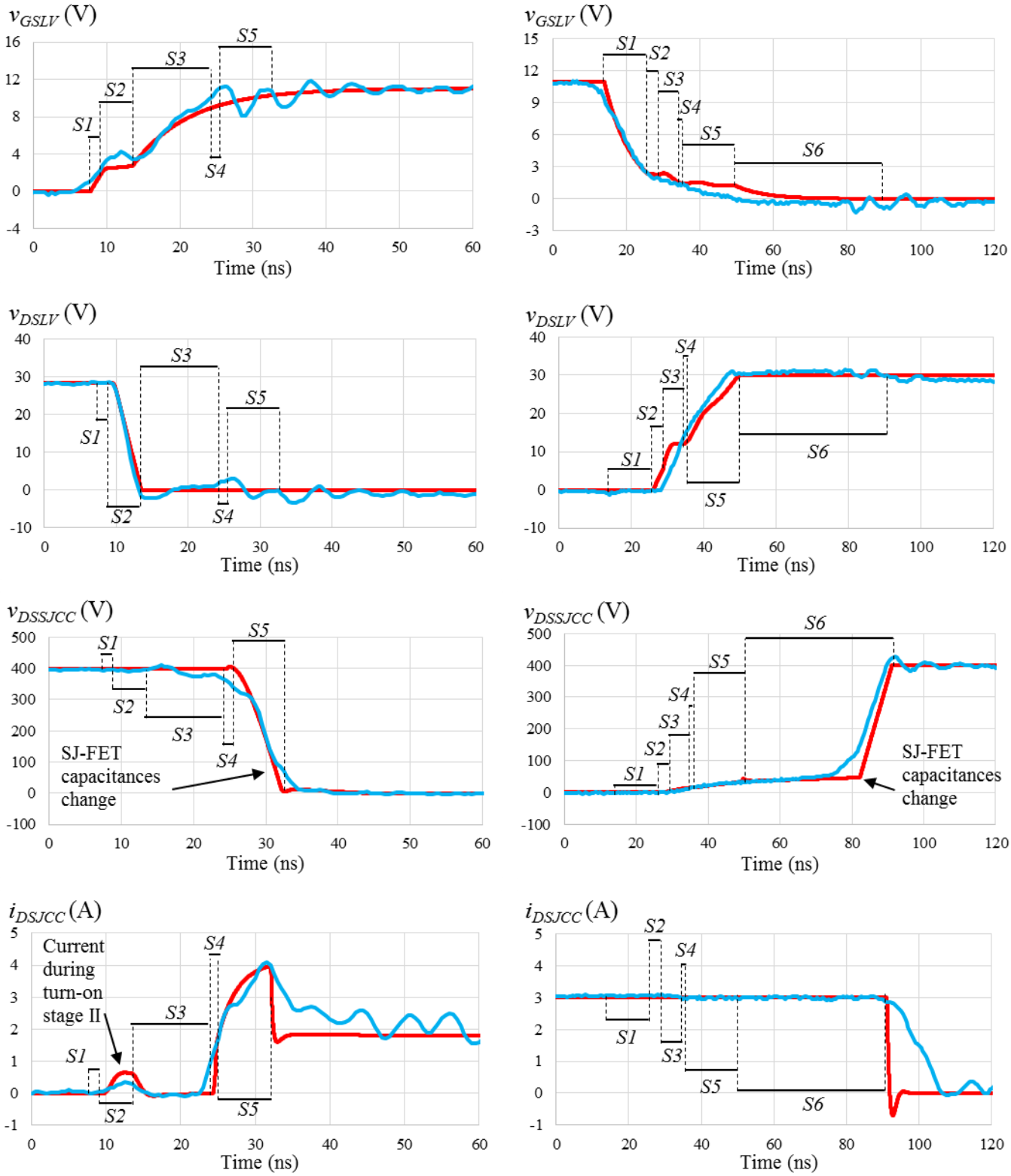

Fig. 5. Comparison between experimental (blue line) and provided by the model (red line) waveforms during the turn-on and the turn-off.

through it (32). The variation of the values of C_{DSHV} and C_{DGHV} versus v_{DSHV} should be applied when v_{DSHV} achieves the frontier. The stage ends when v_{DSSJCC} achieves a value that forward biases the freewheeling diode (i.e. equal to V_O plus the forward voltage drop of D). C_{GSHV} can be considered to be clamped because v_{DSLV} is a constant value during this stage.

Hence, v_{GSHV} is equal to (V_A - V_{AV}). However, overshooting voltage will appear once the stage ends and L_{PAR} stops conducting current abruptly.

$$v_{DSLV}(t) = V_{AV}. \quad (32)$$

III. Experimental Validation

In order to verify the model of the hard-switching process of the SJ-CC, the boost converter shown in Fig. 4 was built. v_{DSSJCC}, i_{DSJCC}, v_{DSLV} and v_{GSLV} were measured to compare experimental waveforms to the provided by the model. The input and output voltages of the converter are 100 V and 400 V respectively, while the output power is 240 W. The switching frequency is 100 kHz and the boost prototype operates in continuous conduction mode with 1.8 A at the turn-on and 3 A at the turn-off. Both MOSFETs and the SiC Schotky diode are surface mounted devices in order to reduce the impact of the parasitic inductances. An SMD capacitor was added between the SJ-FET gate and the LV-FET source to stabilize V_A. This voltage is obtained from the driver power supply. Taking into account the parasitic inductances introduced by the package of both MOSFETs and estimating the inductance introduced by the PCB, L_{PAR} was fixed to 6 nH in the model. Regarding the commercial MOSFETs, the 650V SJ-FET has an on-resistance of 134 mΩ while the LV-FET has 8.1 mΩ. Moreover, V_{DRI} and V_A were set to 11 V. The confidentiality policy of the company that promotes this work does not allow to provide more information about the devices.

Fig. 5 shows a comparison between the measured waveforms and the waveforms provided by the model during both transitions. It also includes the different stages detailed in sections II.C and II.D (identified as S1, S2, etc.). In general, the model achieves high accuracy, especially in the voltage waveforms. However, there are some differences that should be mentioned. The measured v_{GSLV} and v_{DSLV} shows some oscillations that do not appear in the waveforms of the model. This can be attributed to the parasitic inductances that exist at the gate connection and at the source connection of the LV-FET and at the gate connection of the SJ-FET. Regarding v_{DSSJCC}, the measured and the estimated waveforms show the variation of *dv/dt* caused by the non-linearity of C_{DSHV} and C_{DGHV}. In the case of the model, the step in the values of these capacitors shows a substantial change of *dv/dt*, especially during the turn-off.

With respect of current waveforms, they show an acceptable accuracy during the turn-on. As was detailed in section II.C, during the stage II of the turn-on there is significant part of I_{LOAD} that flows through C_{DSHV}. Experimental reverse recovery charge (Q_{rr}) of the SiC diode is a bit larger than the provided by the model. During the turn-off, there is a high difference between the experimental and estimated *di/dt*. This is because *D* is modelled as an ideal diode and the parasitic inductances mentioned before and the inductance that appears between the SJ-FET drain and the diode anode are not considered. Therefore, i_{DSJCC} shows a step in this transition. The cause of this step is that once the v_{DSSJCC} is equal to V_O plus the forward voltage drop of *D*, this diode starts to conduct instantaneously. It is important to note that i_{DSJCC} is the sum of the currents that flow through C_{DSHV}, through C_{DGHV} and through the SJ-FET channel. The last one is the current that experience a progressive fall during the turn-off transition, but it can not be measured.

IV. Conclusions

A model that deeply explains the hard-switching behaviour of the SJ-CC is reported and experimentally proven in this paper. Existing models for SJ-FET in standalone configuration are not suitable for SJ-CC because they do not take into account the interaction between the LV-FET, the SJ-FET and V_A during switching transitions. Therefore, they can not predict some situations that only occur in the cascode configuration (i.e. the avalanche of the LV-FET during the turn-off, the less resistive gate path of the SJ-FET, the simultaneously rise of the channel current and fall of the drain to source voltage of the LV-FET during the turn-on, etc.). In addition, the model is based on important characteristics of the SJ-FET, like the high non-linearity of its drain to source and drain to gate capacitances with v_{DSHV}, and some parasitic elements that have high impact on the switching process, like the inductance between the source of the SJ-FET and the drain of the LV-FET. As experimental waveforms show, the model achieves a high accuracy.

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