Impulse Transformer Based Secondary-Side Self-Powered Gate-Driver for Wide-Range PWM Operation of SiC Power MOSFETs

Jorge Garcia
Dept of Electrical Engineering, University of Oviedo
LEMUR Research Group
Gijon, SPAIN
garciajorge@uniovi.es

Emre Gurpinar, Alberto Castellazzi
The University of Nottingham
PEMC Research Group
Nottingham, UK
alberto.castellazzi@nottingham.ac.uk

***Abstract*—This work proposes a solution for an isolated gate driver for SiC MOSFETs, based on a magnetic transformer that simultaneously provides to the secondary side the turn-on and turn-off gate signals and the power required for an adequate gate control. This avoids the use of a dedicated DC-DC isolated converter and optocoupler. The original pulse signal is converted into impulses, avoiding transformer saturation at any duty ratio operation. The small size of the resulting transformer enables an overall size reduction vs. conventional solutions (based either in magnetic or optocoupler + power supply). This enables much more compact designs, which are critical in high-power density applications and multilevel converters. After describing the basic operation of the driver, experimental results on a 2kW prototype demonstrate the feasibility of the proposal. It is worth mentioning that this design is also suitable for GaN devices with minor design changes**

Keywords—Power Electronics, Wide Band-Gap Devices, Gate Drivers.

I. INTRODUCTION

The usual solution for an isolated SiC MOSFET gate-driver is a combination of an optocoupler plus a dedicated isolated DC-DC power supply to feed an output power stage [1][2]. The drawbacks of this solution are the relatively large area required and low dv/dt immunity, which may cause harmful circulating currents [2][3]. Alternatively, several transformer-based gate signal converters have been proposed [4][5]. However, these solutions have the inherent problem of saturation for wide duty ratio ranges. If a series blocking capacitor is used to avoid saturation, problems arise when fast dynamics are required in the duty ratio command. A magnetic driver solution based on symmetrical pulses has been reported for pulsed power applications [6]. However, this solution is not intended for WBG based generic applications under continuous HF operation, and needs complex circuitry to generate the input pulses.

The proposed work aims to solve these issues, by proposing an isolated gate driver for SiC MOSFETS based in an impulse transformer. This transformer provides both power and signal to the secondary side, therefore there is no need for an extra isolated power source. This enables much more compact designs, which are critical in high-power density applications and multilevel converters [7]. After discussion, and in order to demonstrate the feasibility of the proposal, two prototypes of the driver have been built and tested on a 400V/2kW DC-DC buck-boost synchronous converter with C2M0080120D SiC MOSFETs from CREE, switching at 100 kHz. An analysis of these results is finally provided.

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II. BASIC OPERATION OF THE PROPOSED DRIVER

The following section deals with the basic operation strategy of the proposed circuit. The first idea is to use a single isolation component (transformer) in order to simultaneously send the switching information (turn-on and turn-off pulses) and the energy needed to effectively turn on and off the power device. The proposed topology uses an impulses transformer.

Fig. 1 shows the block diagram of the circuit. The original pulse waveform 1), $u_P(t)$, is converted into an impulses waveform 2) $u_d(t)$ by a RC derivative network. This signal is amplified by a BJT complementary stage, and supplied to the primary side of the pulse transformer 3). It must be noticed how saturation free operation of the transformer is ensured, since the derived signal $u_d(t)$ has no DC component for any duty ratio. At the secondary side, a diode bridge rectifies the pulsed signal to obtain a single-polarity waveform, 4), $u_{rect}(t)$. After filtering this signal through a capacitive filter, the resulting signal 5), $u_o(t)$, is practically a DC signal, therefore behaving as a DC source. This source supplies the secondary side logic and driving circuits of the driver. A reference value generated ad-hoc, 6) $u_{Ref}(t)$ provides the negative voltage required for turn off of WBG devices.

Additionally, signal $u_d(t)$ is divided into rising 7) and falling 8) pulses, $u_s(t)$ and $u_r(t)$, connected to the set and reset inputs, respectively, of an edge-triggered SR flip-flop. This flipflop has been implemented by means of a fast Operational Amplifier (LM6172). The output of such block, Q is supplied to a power stage (again a BJT complementary stage), connected to the gate and source terminals of the main device, ensuring the on/off gate-to source voltage levels 9) and the high dv/dt required for a proper switching of the power device [1][2][7].

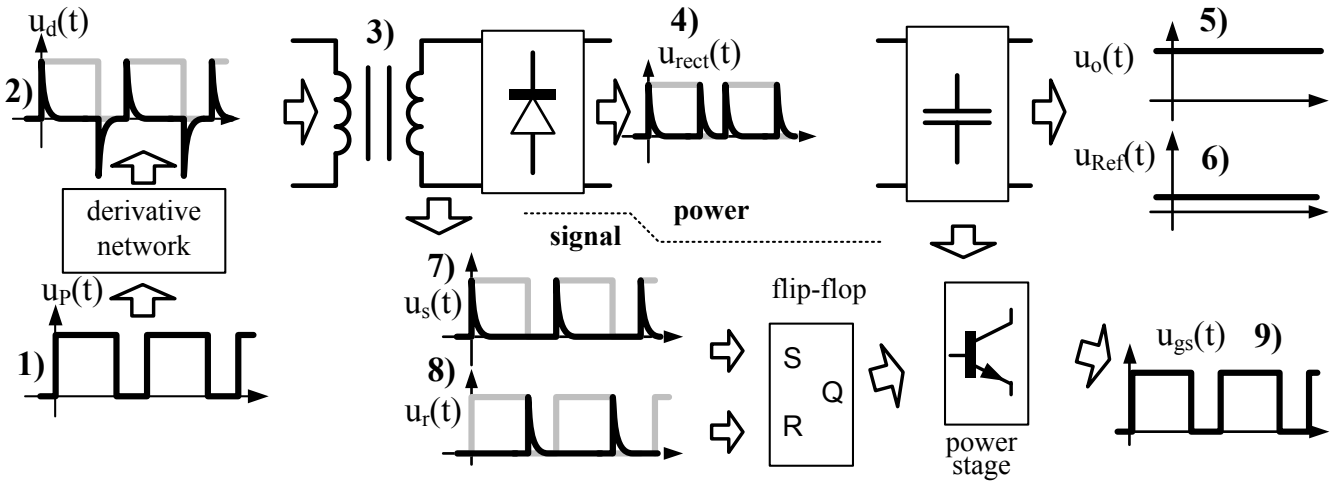

Fig.1 Block Diagram of the proposed Gate Driver

III. Key Specific Aspects of the Proposed Driver

A. The Impulse Transformer

As it has been mentioned in the previous section, each switching period, two impulses are sent to the secondary side, a positive polarity voltage upon the rising edge of the PWM signal, and a negative polarity impulse on the falling edge (see Fig. 2). The use of this approach implies that in order to transmit effective power, the impulses must be provided in a regular basis, therefore this driver cannot work providing the switch fully turned on (100% duty ratio), and will not provide negative voltage when the switch is fully turned off (0% duty ratio). However, in the real application, the limit values achieved are 10%-90%.

These impulses are generated though a RC derivative network. The derivative network is connected at the output with a DC reference equal to Vcc/2, as depicted in Fig. 3. This enables the symmetric, balanced operation of the power stage formed by the BJT complementary stage (still looking at Fig. 3). Therefore, the signal at the output of the BJT stage, $u_{TR}(t)$, has a DC value equal to Vcc/2. However, this signal is also connected to the other terminal of the primary side of the transformer, ensuring no DC component in the transformer, and therefore avoiding core saturation.

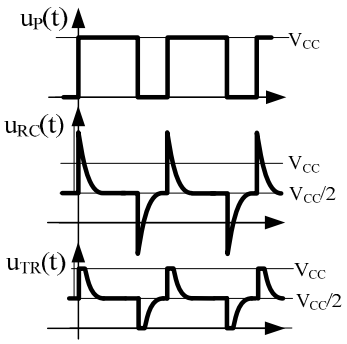

Fig. 2: Waveforms at the impulse generation section.

However, due this DC component, the signal at the output of the complementary BJT stage, $u_{TR}(t)$, is clamped at V_{CC} and 0V (actually the saturation voltages of the BJTs must be taken into account, however they are neglected in this discussion). Therefore, the AC peak amplitude of the impulses during this clamping is roughly equal to $V_{CC}/2$. In this manner, the RC parameter is related with the width of the impulse that will effectively send energy to the secondary side, as Fig. 2 depicts. This parameter (RC parameter) is the design variable used to tune the amount of energy delivered to the secondary side. The larger RC, the longer the impulse. However, the longer the impulse, the minimum duty ratio can be reached for regular operation.

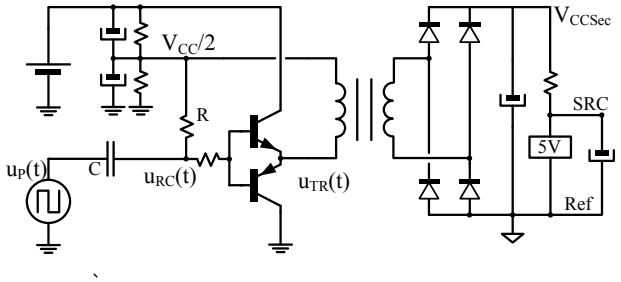

Fig. 3: Scheme of the impulse generator and the output power source section

On the other hand, at the moment of the impulses, current will flow through the transformer, and therefore the output bridge of the driver will be turned on. In that case, and considering steady state, the secondary side voltage V_{CCSec} is given by the turns ratio and the primary side voltage during clamping mode. Therefore, the turns ratio parameter can be fixed as to obtain a given output voltage.

B. The Negative Turn-off Voltage Generation

At the secondary side, a voltage reference IC providing 5V is used to generate the reference node that will be connected to the Source of the Power Device, thus enabling for a negative voltage to turn off the device, as depicted in Fig. 3.

C. *The RS Flip-Flop Implementation*

The flip-flop is implemented with the scheme shown in Fig. 4. The two transistors implemented by means of a BSL306N IC, are used to trigger the SET and RESET inputs of the flip-flop with the positive and the negative impulses at the secondary side of the transformer, respectively. These signals come from the terminals at the secondary side, with two additional peak detectors implemented with Schottky diodes and a dedicated RC circuit, as depicted in Fig. 4.

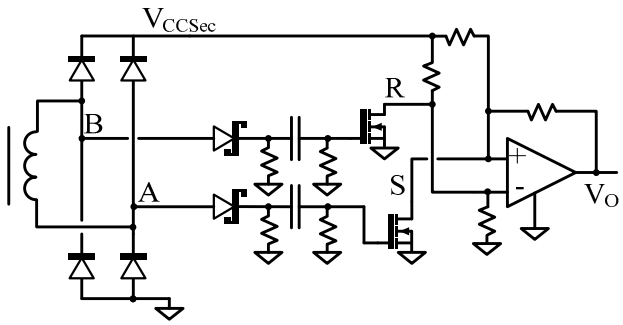

Fig. 4: Scheme of the flip-flop output section.

IV. Design Considerations

The initial design has been simulated in LTSPICE™, and all the elements in the final circuit have been selected considering the parasitic components, as well as the complete SPICE models providing an accurate operation of all the elements in the design. The most significant waveforms in the design are depicted in Fig. 5. It can be seen the original PWM waveform, the voltage at the transformer primary and secondary sides, the Set and Reset signals of the OpAmp as well as the output Gate-to-Source waveforms at the power device.

The most critical component in the operation of the driver in terms of the Common Mode Immunity (CMI) is the magnetic transformer, as it's providing the isolation between primary and secondary sides, and therefore states the parasitic impedance path for recirculating currents that yield to CM issues. Table I summarizes the parameters of the transformer after the analysis carried out (open circuit, short circuit and primary-to-secondary characterizations):

TABLE I. Parameters of the Transformer

Parameters of the Transformer at 100 kHz		
Parameter	***Symboi***	***Subhead***
Magnetizing inductance (primary side)	L_{μ}	3.16mH
Parallel resistor (primary side)	R_p	10kΩ
Leakage inductance at primary side	L_{LKp}	19.4µH
Series resistor at primary side	R_{sp}	0.433Ω
Leakage inductance at primary side	L_{LKp}	1.03µH
Series resistor at secondary side	R_{ss}	0.022 Ω
Coupling capacitor (between primary and seconadry side)	C_c	3.41pF

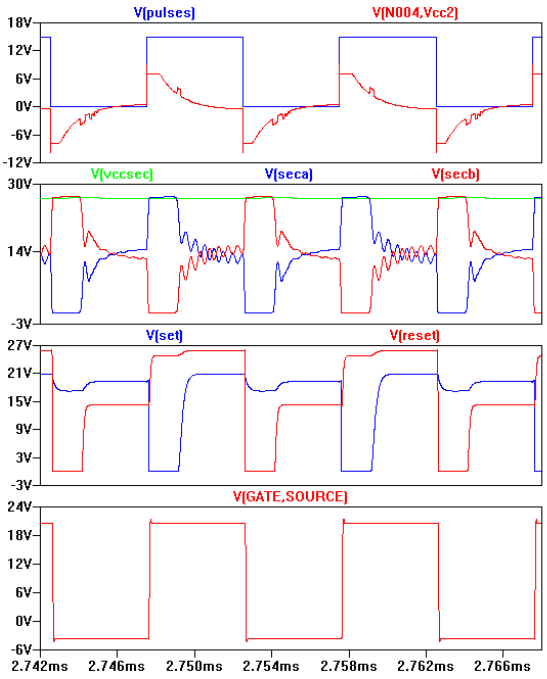

Fig. 5: Simulations of the proposed scheme. Plot 1: Original PWM pulses (blue) and primary side voltage (red). Plot 2: voltage at both secondary side terminals (red and blue), and Vcc voltage at the secondary side (green). Plot 3: Set (blue) and reset (red) signals (falling edge-triggered flip-flip). Plot 4: Gate-to-Source voltage at the power device (red)

As it can be seen in Table I, the coupling capacitor between primary and secondary side is small enough as to guarantee a good behavior in terms of CMI.

The output stage is formed by a BJT complementary stage. This stage gets the pulses from the OpAmp output, V_O. At the output of this stage, a series resistor is used to limit the dV/dt at the power MOSFET. The final value of this resistor is selected in the experimental section, as to limit oscillations in the gate driver. At turn-on and turn-off.

V. Experimental Results

After the theoretical analysis discussed, and once the design of the circuit is refined after simulations, a prototype of the gate driver, depicted in Fig. 6, has been built and tested on an existing 400V/2kW DC-DC buck-boost synchronous converter with C2M0080120D SiC MOSFETs from CREE.

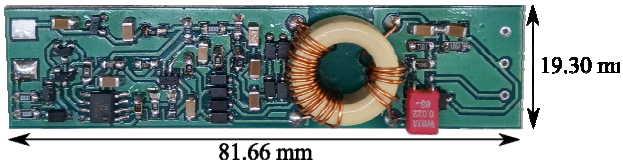

Fig. 6: Built prototype of the Gate Driver.

It is estimated that a size reduction in a factor of 3 to 4 can be achieved in future versions of the driver, as the reported prototype is a single layer design, using large SMT footprints 1206 discrete components.

Fig. 7 shows the main power SiC switches experimental waveforms at 100 kHz, at 1.8kW load level. In this experiment, the input voltage at the buck-boost converter is 400 V_{DC}, the output current is 5A, and the average inductor current is 10A. The efficiency of the converter on these working conditions reaches 95%.

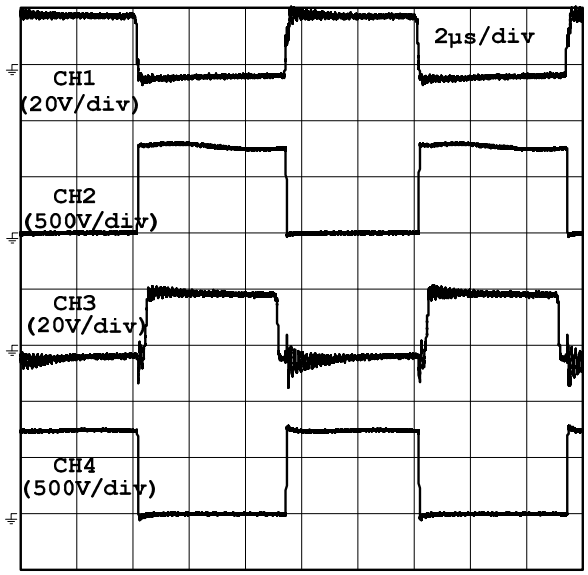

Fig. 7: Experimental waveforms at a bidirectional buck-boost converter. CH1: $u_{GS}(t)$ at Switch S1 (output switch), CH3: u_{DS} at S1. CH3: $u_{GS}(t)$ at Switch S2., CH4: u_{DS} at S1. 400Vdc input, 100 kHz switching frequency, 5A output.

Fig 8 shows the details of the gate to source and drain to source voltages of one of the power switches at turn on and turn off. It can be seen how the V_{DS} voltage slope reaches 20 V/ns at both turn on and turn off.

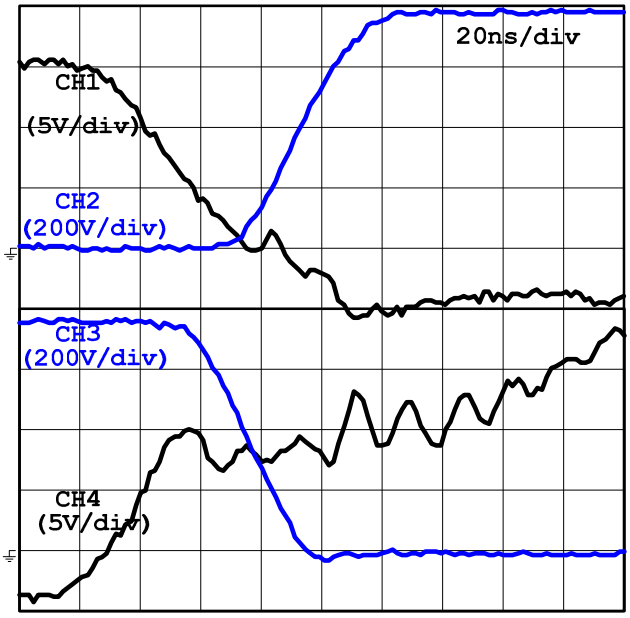

Fig. 8: Detailed waveforms of Fig. 3, at turn off (upper traces) and at turn on (lower traces). CH1, CH4: uGS(t) at Switch S1. CH2, CH3: uDS at S1.

Fig. 9 shows the V_{DS} rise and fall times vs the V_{DS} voltage at 100 kHz, at 50% duty-ratio and at 5 A output current. The output series resistor of the drier is fixed in 15Ω, in order to limit the oscillations that are present in the gate voltage. The propagation delay from the logic to the RC waveforms is 100ns. The circuit can operate at duty ratios from 10% to 90%, and at switching frequencies up to 200 kHz.

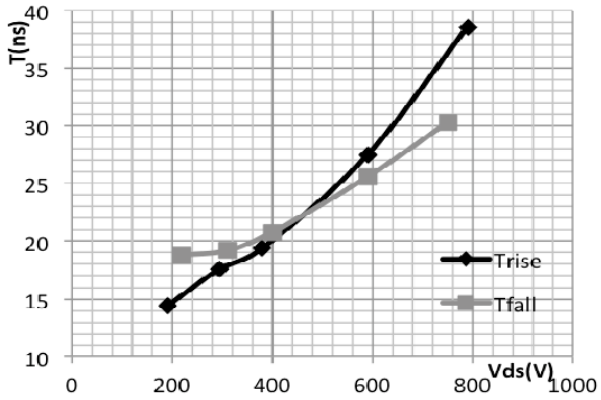

Fig 9. **V_{DS} rise and fall times vs the V_{DS} voltage, for the converter operating at 100kHz, 50% duty-ratio and 5A output current.**

In an additional experiment, the driver has been loaded with different RC circuits that model the gate resistance and capacitance of SiC devices without drain-source voltage. This is intended to demonstrate the functionality of the design for different rated SiC MOSFETs. Fig. 10 shows the driver rise and fall times for the given RC combinations.

These preliminary results show the feasibility of the proposed SiC MOSFET driver.

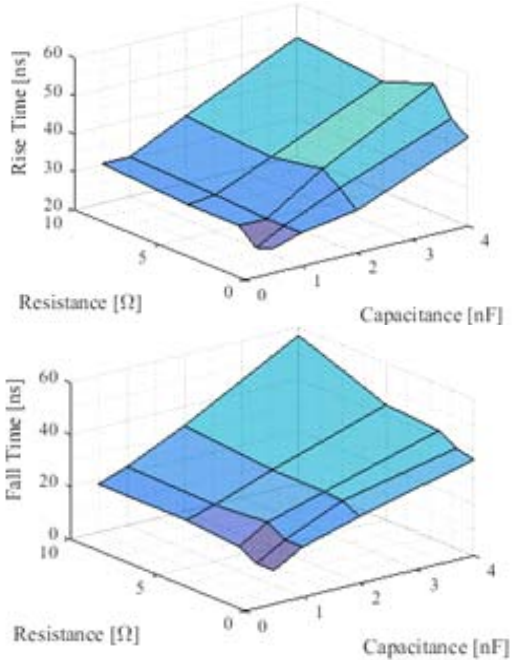

Fig. 10: Rise (up) and fall (down) time at the driver output for several R and C values

VI. Conclusions and Future DEvelopments

The present work proposes a topology for a gate driver for SiC power devices, based on a single magnetic transformer, that provides simultaneously the pulses information and the power required to effectively drive the power device with voltage levels of +20V/-5V.

The operation of the circuit has been detailed, and an analysis of the main aspects of the circuit has been carried out in this work. Detailed SPICE models of all the elements in the driver have been used for undertaking a tight design of the proposed driver. Two working prototypes of the driver have been characterized and operated in a 2kW converter, based on C2M0080120D SiC MOSFETs from CREE.

Results of the operation show the expected behavior, turning on and off the power device within reasonable times, with high dV/dt, and able to switch at frequencies up to 200 kHz, with duty ratios from 10% to 90%.

Future developments include an enhanced design in terms of size (a target size reduction in a factor of 3 to 4 can be achieved in future versions of the driver), consumption, and reliability.

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