Virtual Admittance Loop for Voltage Harmonic Compensation in Microgrids

Cristian Blanco[1], David Reigosa[1], Juan Carlos Vasquez[2], Josep M. Guerrero[2] and Fernando Briz[1]

[1] University of Oviedo. Dept. of Elect., Computer & System Engineering.
Gijón, 33204, Spain

[2] Aalborg University. Department of Energy Technology,
Aalborg 9220, Denmark

blancocristian@uniovi.es, diazdavid@uniovi.es, juq@et.aau.dk, joz@et.aau.dk, fernando@isa.uniovi.es

Abstract— The use of the virtual admittance concept for harmonic and/or unbalance compensation in microgrids when multiple inverters operate in parallel is proposed in this paper. The virtual impedance concept has been traditionally used for these purposes. However, one drawback of the virtual impedance is that it can only be applied to distributed generation (DG) units operating in voltage control mode (VSI-VCM), but is not applicable to DG units working in current control mode (e.g. current regulated voltage source inverters, VSI-CCM). Contrary to this, the proposed method can be used in any converter topology and control mode, including VSI-CCM and VSI-VCM.

Index Terms— Virtual admittance, virtual impedance, power quality, voltage harmonics, voltage unbalance, power sharing.

I. INTRODUCTION

DURING the last decade the role of microgrids has evolved rapidly. Initially, the final goal of a microgrid was to provide power and heat to a relatively small area [1], often with a limited electrical infrastructure. Later on, the microgrid paradigm was extended with the goal of reducing the transmission lines congestion and losses. In recent years, due to the increased power demand, environmental concerns and applications like off-grid or military, new microgrid facilities are growing progressively in number and size. To fulfill the microgrid requirements, new supervision and control concepts have been developed whenever parallel-connected inverters operate in a microgrid, including islanding detection [4], frequency and magnitude restoration [5], power flow optimization [6], power sharing [7] and power quality improvement [8].

To improve the power quality in microgrids, several approaches have been proposed. Dedicated equipment like active power filters [14] (shunt, series or hybrid) can be used for the case of critical loads. Alternatively, the DG units can be used to improve the power quality at the point of common coupling (PCC) of the microgrid. Both centralized and distributed control strategies have been proposed for this purpose [14]-[16].

In these strategies for islanded microgrids, parallel-connected inverters can be required to inject high frequency current components to the PCC to compensate harmonic components e.g. due to non-linear loads present in the microgrid. Thus, each inverter injects an amount of current in order to contribute to the high frequency voltage compensation. A key issue for these strategies is which share how much current each inverter must inject. The virtual impedance concept is a mechanism that can be applied for this purpose.

The virtual impedance concept can be used as a cooperative mechanism to share unbalance and harmonic compensation among several parallel-connected inverter in a microgrid, and without the need of a centralized control [7, 19]. Furthermore, it can also be applied to inverter soft-starters [20], or combined with droop control methods for active and reactive power sharing [20]. The main drawback of the virtual impedance concept is that it can only be applied to voltage source inverters operating in a voltage control mode (VSI-VCM), its use with voltage source inverters working in current control mode (VSI-CCM) not being feasible.

This paper proposes the use of a virtual admittance for harmonic and/or unbalance compensation sharing when multiple inverters operate in parallel. The proposed method responds to the same physical principles as the virtual impedance concept [7, 19]. However, contrary to virtual impedance based methods, the virtual admittance can also be used when VSI-CCMs participate in a cooperative compensation. Though the proposed concept has similarities with methods that have already been proposed for non-sinusoidal current regulation [26], to deal with unbalances in three phase rectifiers [28] and also to emulate the behavior of generation units using synchronous generators with electronic power converters [29], the use of the virtual admittance for unbalance compensation sharing is, to the best of authors knowledge, an original contribution of the proposed paper.

The paper is organized as follows. Section II presents the basics of the proposed concept. The use of virtual admittance control loop for harmonic compensation is presented in Section III. Simulation and experimental results validating the proposed method are presented in Sections IV and V respectively. Finally, the conclusions are presented in Section VI.

II. VIRTUAL ADMITTANCE CONCEPT

The main goal of the virtual admittance concept proposed in this paper is to share among multiple parallel connected inverters the required actions to eliminate the harmonic content and unbalances from the PCC voltage in islanded microgrids. The use of non-linear loads (NLL) in islanded microgrids makes that voltage harmonic components are commonly found at the PCC. In order to compensate these unwanted harmonic components, each parallel-connected inverter is required to inject harmonic currents to the NLL.

The virtual admittance concept will be thus used in order to designate how much harmonic current each inverter injects.

Fig. 1 shows *Norton* equivalent circuit of a voltage source, with a virtual admittance, Y_v, connected in parallel with the inverter output. It is noted that for the case of a VSI connected to the grid through an output filter (*L, LC* or *LCL*), the virtual admittance can be connected in principle either at the inverter output or at the filter output.

The virtual admittance could be connected in principle either at the inverter output or at the filter output. It is noted that for the particular case of LCL filters, the virtual admittance could be also connected in parallel with the filter capacitor. Placing the virtual admittance at the filter output is not adequate for harmonic compensation. This is due to the fact that if the harmonic voltage is fully compensated (i.e. $u_{out_{dqh}} = 0$), no virtual current will be consumed by the virtual admittance, therefore there will be no impact on the actual harmonic current supplied by the inverter. On the contrary, placing the virtual admittance either at the inverter output or in parallel with the filter capacitor in the case of LCL filters, will affect to the actual harmonic current supplied by the inverter, and consequently to the harmonic current share among inverters. It is noted however that placing the virtual admittance in parallel with the LCL filter capacitor is not trivial. The LCL filter capacitor voltage is not measured in practice; consequently, it needs to be estimated from the output LCL filter voltage (which is typically measured), the commanded inverter voltage and the filter current.

It is concluded that placing the virtual admittance at the inverter output (LCL filter input) provides the simplest implementation, this option will be considered hereafter.

Fig. 2 shows the schematic representation of a three-phase VSI feeding an LCL filter using the proposed virtual admittance control strategy. This block diagram is applicable both for harmonic compensation, as well as for unbalance compensation (in this case the harmonic order is h=-1) [35-38].
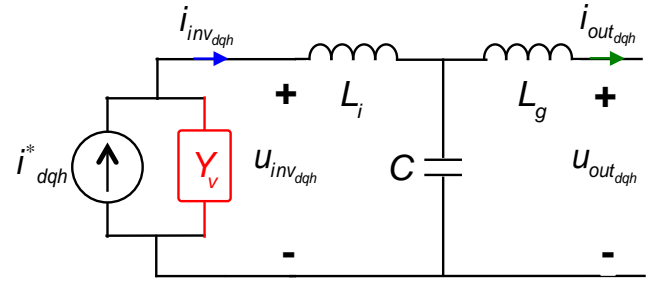

Fig. 1. Inverter´s Norton equivalent circuit with parallel virtual admittance Y_v.

The implementation shown in Fig. 2 uses a VSI-CCM. It is noted however that the method can be equally applied to VSI-VCM. A PI resonant controller (PI-RES, Fig. 3), (1)-(3), is used to control both the fundamental component and harmonic components of the inverter output current. The harmonic current consumed by the virtual admittance is obtained from the commanded harmonic voltage to the inverter. A band-pass filter (BPF in Fig. 2) is used to isolate the commanded harmonic component ($u_{inv_{dqh}}$) from the PI-RES output ($u_{inv_{dq}}$).

Since the virtual admittance, Y_v, is connected at the inverter output and in parallel with the filter, it will affect to the current phase angle of the *overall* output current (4), and consequently to the inverter output power factor. To prevent from this to happen, the magnitude of the current consumed by the virtual admittance (5) is forced to be in phase with the current command i^*_{dqh}. The control mechanism proposed in this paper is called *non-phase-disturbing* virtual admittance. It is noted that the phase angle of the current command $\left(i^*_{dqh}\right)$ $j_{i_{dqh}^*}$ is needed for this purpose (see Fig. 2). A unit vector with an angle $j_{i_{dqh}^*}$ is built and multiplied by the magnitude of the current consumed by the virtual admittance $\left|i_{Y_v}\right|$, guaranteeing therefore that the virtual current does not affect to the inverter output power factor (6).
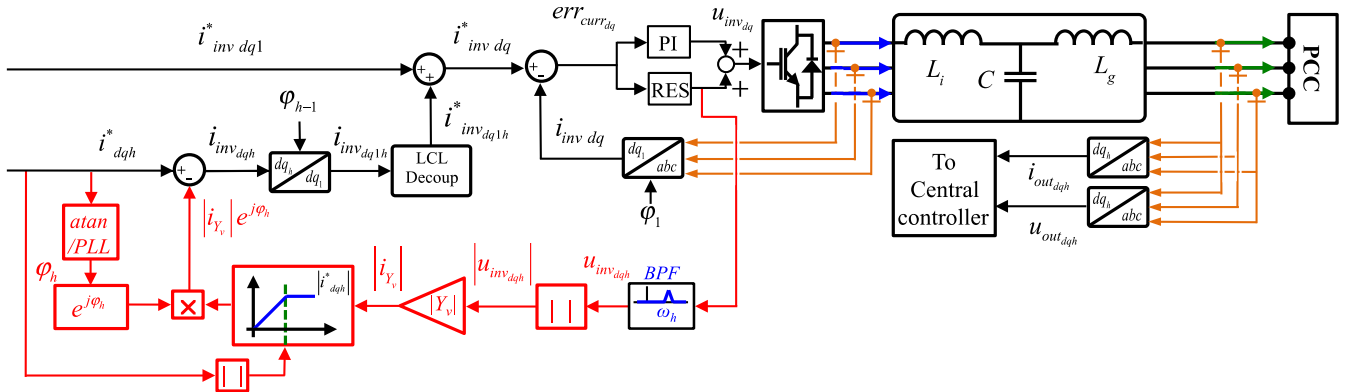
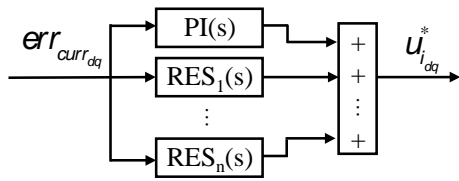

Fig. 2. Proposed virtual admittance control loop.

Fig. 3- PI-RES block diagram.

$$PI\text{-}RES(s) = PI(s) + RES_n(s) \tag{1}$$

$$PI(s) = K_p + \frac{K_i}{s} \tag{2}$$

$$RES_n(s) = \frac{K_{p_{RES\_n}} \times s^2 + K_{p_{RES\_n}} 2 \times C \times s + \left(n \times W_0\right)^2 + C^2}{s^2 + \left(n \times W_0\right)^2} \tag{3}$$

$$i_{inv\,dqh} = i^*_{dqh} - Y_v \times u_{inv_{dqh}} \tag{4}$$

$$\left| i_{Y_v} \right| = \left| Y_v \right| \times \left| u_{inv_{dqh}} \right| \tag{5}$$

$$i_{inv_{dqh}} = i^*_{dqh} - \left| i_{Y_v} \right| \times e^{j \angle i^*_{dqh}} \tag{6}$$

It is observed from (6) that large values of $\left| i_{Y_v} \right|$ might result in a change in the sign of the current reference i^*_{dqh}, and consequently in a phase shift of 180º between i^*_{dqh} and $i_{inv\,dqh}$. To prevent from this to happen $\left| i_{Y_v} \right|$ is limited to a maximum magnitude of i^*_{dqh}.

The same current control strategy is applicable both to VSI-CCM and VSI-VCM, the only difference being the way the current command $i^*_{inv\,dq1}$ is obtained. For the case of a VSI-VCM, $i^*_{inv\,dq1}$ comes from an outer voltage controller while for the case of a VSI-CCM, it typically comes from other control loops (e.g. power controller) [34]. However, type of control of the inverter does not affect to the performance of the proposed method.

III. HARMONIC COMPENSATION SHARING USING THE VIRTUAL ADMITTANCE

As already mentioned, the main objective of the proposed method is to share among multiple parallel connected inverters the required actions to eliminate the harmonic content and unbalances from the PCC voltage in islanded microgrids. The virtual admittance allows to determine the contribution of each inverter to the overall current needed to clean up the PCC voltage.

a)   Central controller design

Fig. 4 shows the scenario that will be used both for simulation and experimental verification. It consists of two VSIs with an output LCL filter each connected in parallel and a central controller. One of the converters is configured as a VSI-VCM (e.g. *Master inverter* setting the voltage magnitude and frequency), while the other operates as a VSI-CCM (e.g. *Slave inverter*). The master inverter feeds a local resistive linear load (LL) and a non-linear-load (NLL, Fig. 7), while the slave

inverter feeds a local resistive linear load. The proposed virtual admittance based control (see Fig. 2) is implemented in the local controller of master and slave inverters. A central controller implements the harmonic voltage control and sends to each converter both the resulting current commands as well as the selected virtual admittances (see Figs. 4, 5 and 6).
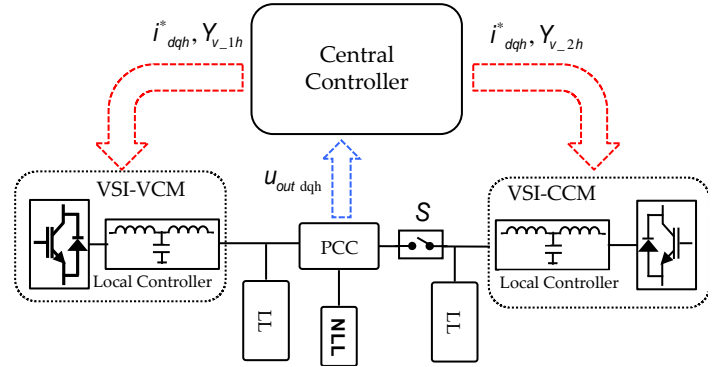

Fig. 4. Setup used for simulation and experimental verification. NLL stands for non-linear load, the rest of loads in the figure being linear (LL).

The voltage harmonics to be compensated are measured at the PCC, transformed to a reference frame synchronous with each harmonic (see Fig. 2) and transmitted to the central controller using a communication interface, e.g. a *WiFi* link.

Fig. 5 shows a simplified representation of the proposed control strategy. The central controller transmits to the local control of each inverter the current command and the virtual admittance for each harmonic. Criteria for the optimal selection of the virtual admittances would include distance to the PCC (i.e. impedance), rated power and load level for the inverters injecting harmonic current. At the same time, it would involve a power flow analysis for each particular microgrid configuration. Optimal selection of the virtual admittance is not therefore straightforward, being a topic of ongoing research. Fig. 6 shows the proposed control block diagram of the central controller.
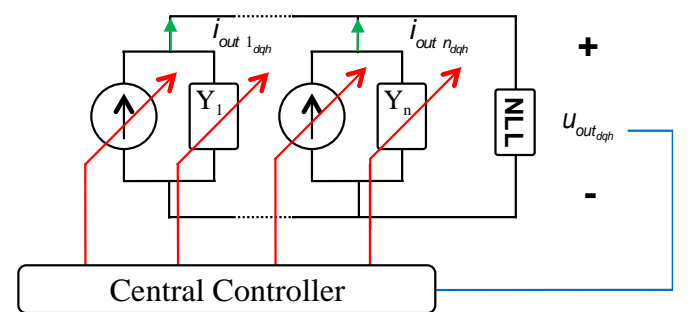

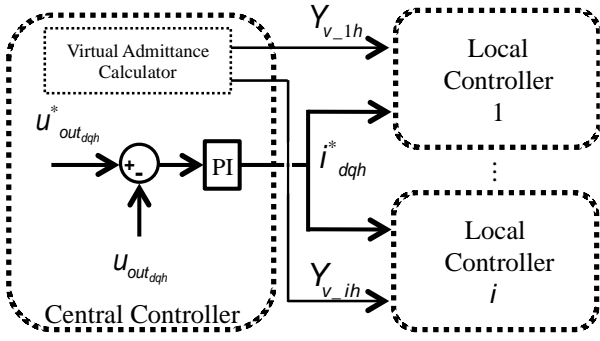Fig. 5. Schematic representation of the proposed centralized control.

Fig. 6. Block diagram of the proposed centralized harmonic compensation strategy. Note that this scheme is repeated for each harmonic being compensated.

The reference for each harmonic included in the control ($u^*_{out_{dqh}}$, see Fig. 6) is typically set to 0, meaning that that harmonic will be fully cancelled at the PCC. A synchronous PI regulator, same design as (2) is used for this purpose. It is possible to implement the harmonic compensation strategy locally in each inverter to avoid the use of communications. In this case, each inverter would use a preset value of virtual admittance. This implementation has not been thoroughly studied yet, especially the effects of connecting/disconnecting inverters.   On the other hand, the proposed centralized implementation provides substantial advantages it terms of simplicity and robustness, as adding or removing inverters would be "*plug and play*".

The output of the PI controller i^*_{dqh} is transmitted to each local controller (see Fig. 6), where it feds the virtual admittance controller, as shown in Fig. 2. The output current command in the h harmonic reference frame, $i_{inv_{dqh}}$, is then rotated to the fundamental synchronous reference frame ($i_{inv_{dq1h}}$).

b)   Filter decoupling

The inverter current reference feeds an LCL-decoupling block, which is used to compensate for the effect of the output LCL filter using (7). By doing this, all the inverters inject in phase at the PCC. It is noted in this regard that decoupling of the LCL filter might not be required for the compensation of low-order harmonics, since the effect of the LCL filter is expected to be negligible at low frequencies. However, in case of low cut-off frequency LCL filters or when high-order harmonics are compensated, the LCL filter effect might not negligible, compensation of its effects being therefore necessary.

$$i^*_{inv_{dq1h}} = \frac{C \times L_i \times s^2 + C \times R_{L_g} \times s + C \times R_c \times s + 1}{C \times R_c \times s + 1} i_{inv_{dq1h}} +$$

$$+ \frac{C \times s}{C \times R_c \times s + 1} u_{out_{dqh}} \qquad (7)$$

c)   Effects of the virtual admittance on the microgrid stability

The virtual admittance behaves as a passive load which dynamically modifies the share of harmonic current among inverters. A potential risk of instability could occur if an inverter change the sign of the injected harmonic current due to the use

of an unrealistically large value for the virtual admittance. Implemented mechanisms to avoid any adverse impact of the virtual admittance on the microgrid stability are summarized following:

- It is guaranteed that the virtual admittance current consumption, $|i_{Y_v}|$ (see Fig. 2), does not surpass the current command, i^*_{dqh} . Depending on the selection of the virtual admittance, one inverter might not contribute with harmonic current (i.e. its harmonic current will be fully consumed by its virtual admittance) but it is guarantee that the inverter will never inject harmonic current in counter-phase.

- The concept of *non-phase-disturbing virtual admittance* (Fig. 2) guarantees a constant angle of the current injected by the inverter regardless of the virtual admittance value and grid impedances. It is noted that the effect of the output LCL filter is decoupled, meaning that all inverters will inject in phase ant the PCC.

- It is noted that the centralized controller (i.e. voltage controller) bandwidth must be selected to be more than one decade smaller than the smallest local PI-RES bandwidth [39].
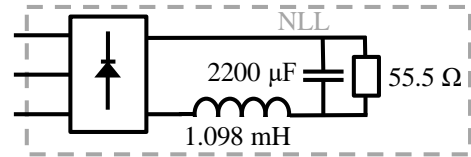

Fig. 7. Non-linear load block diagram.

IV.   SIMULATION RESULTS

Table I shows the parameters for the simulation scenario in Fig 4. A *Multiple-Complex Coefficient-Filter Phase Locked Loop* (MCCF-PLL) [2] has been used for the synchronization of the power converters and to measure the magnitude and phase of the harmonics to be compensated for. The -5th and 7th harmonics are compensated. The centralized PI regulator and the local PI-RES parameters (see Fig. 3, (1), (2) and (3)) are shown in Table I.

Fig. 8 shows the response of the proposed strategy for different values of the virtual admittance. At t=0.3 s switch *S* is closed (Fig. 4) and at t=0.6 s compensation of -5th and 7th harmonics is enabled. Fig. 8a shows the commanded virtual admittances. Fig. 8b and 8c show the injected magnitude, -5th ($|i_{-5}|$) and 7th ($|i_7|$) harmonics, by each inverter. Fig. 8d shows the magnitude of the PCC voltage harmonics (both positive and negative sequence) until order 11th, and the total harmonic distortion (THD). It is observed from Fig. 8b and 8c that from t=0.6 s to t=1.5 s the magnitude of the injected current harmonics by both inverters is the same, as both virtual admittances are set to zero. From t=1.5 s to t=2.5 s, the VSC-VCM decreases the magnitude of the injected current harmonics as its virtual admittance is bigger than that of the VSC-CCM.

Table I – Setup Parameters			
VSI-VCM Inverter		VSI-CCM Inverter	
Rated power	50kW	Rated power	50kW
Capacitor ESR	0.052 Ω	Capacitor ESR	0.052 Ω
Inductor ESR	0.05 Ω	Inductor ESR	0.05 Ω
Inverter-side inductor	2.4 mH	Inverter-side inductor	2.196 mH
Capacitor filter	10 µF	Capacitor filter	10 µF
Grid-side inductor	1.6 mF	Grid-side inductor	2.196 mF
Switching frequency	10 kHz	Switching frequency	10 kHz
Centralized controller			
Kp_{-5}	0.07	Ki_{-5}	0.9
Kp_7	0.3	Ki_7	0.9
Local PI-RES			
Kp	8	Ki	3000
$Kp_{RES\,6}$	1	C	300
N	6		

This situation is reversed from t=2.5 s to 3.5 s. As expected, the smaller the virtual admittance is, the larger the current injected by the inverter is. At t=3.5 s, the virtual admittances are set to zero again.
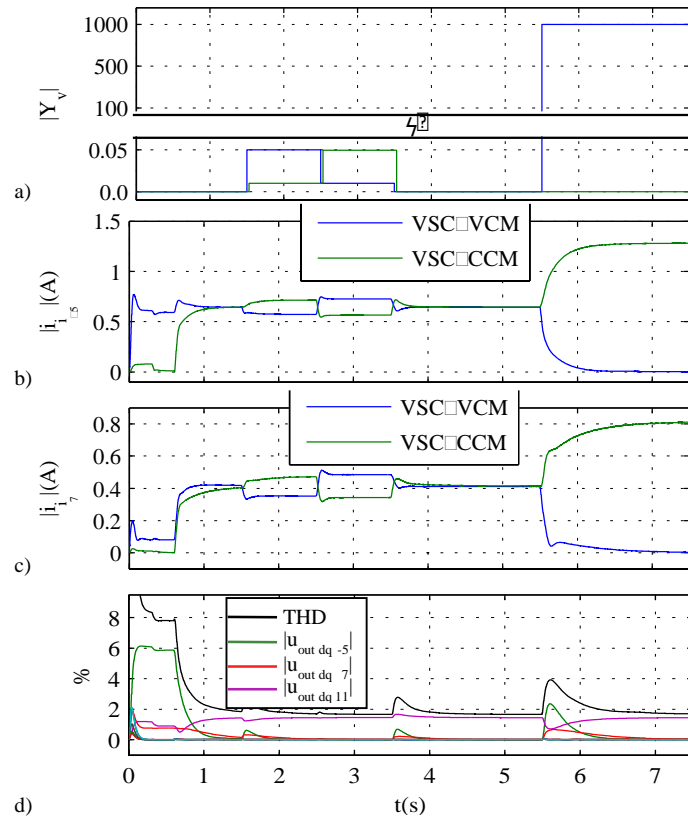

a)

b)

c)

d)

Fig. 8. Simulation results. Voltage harmonic compensation for different values of the virtual admittance. a) Virtual admittance. b) and c) magnitude of the resulting -5th and 7th current harmonics; d) Magnitude of the voltage harmonics and THD, shown as a percentage of the fundamental voltage.

For t>5.5 s, the virtual admittances of the VSI-CCM and VSI-VCM are set to 0.01 Ω⁻¹ and 1000 Ω⁻¹ respectively (Fig. 8a). It is seen in Fig. 8b and 8c that for very large magnitudes of the virtual admittance (infinite in the limit), the VSI-VCM does not inject any harmonic current, i.e. its virtual admittance *consumes* all the inverter harmonic current. Consequently, the rest of the inverters (VSI-CCM) must supply all the current needed to eliminate the voltage harmonics at the PCC.

It is observed from Fig. 8d that once the compensation is enabled (t=0.6 s), the -5th and 7th voltage harmonics are fully cancelled, the THD decreasing from ≈7.9% to ≈2%. It is also observed from Fig. 8 that the transient following changes in the virtual admittance lasts around 500*ms*. After that, the controls are readapted to the new configuration and the voltage harmonics are fully cancelled again. It is noted in this regard that the centralized controller has been intentionally set to a relatively low bandwidth (≈10 Hz) in order to emulate a low-bandwidth communication channel. This bandwidth can be higher in a real scenario if a high-speed communication channel is used. This will result in a faster transient response since the resonant current controller bandwidth is typically high enough to track the centralized current commands in the range of *ms* or tens of *ms* (Fig. 2 and Table I).
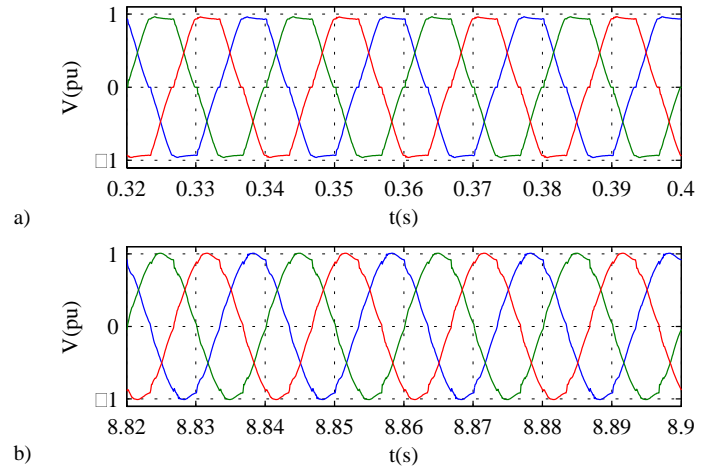

a)

b)

Fig. 9. Simulation results. Detail of the PCC voltages a) before and b) after the compensation.

Finally, Figs. 9a and 9b show the phase voltages at the PCC before and after the compensation is enabled, the 5th and 7th harmonics of the PCC voltage being effectively eliminated by the proposed method.

It is concluded from the preceding discussion that the higher the virtual admittance and the output LCL filter impedance of the inverter are, the lower the current injected by the inverter is (see Fig. 8b and 8c). On the contrary, if all the virtual admittances are set to have similar magnitudes and the output impedances (e.g. LCL filter impedance) also have similar values, the harmonic current will be evenly split among the inverters.

In the results shown in Fig. 8, it was assumed that the impedance of the lines connecting each inverter and the PCC were the same.

The effect of having different line impedances between the PCC and the inverter is shown in Fig. 10. In this simulation, a transmission line (TL) with $R_{TL}=6\Omega$ and $L_{TL}=5mH$ connecting the VSI-VCM and the PCC is considered. It can be observed from Fig. 10a that until t=2 s both virtual admittances are set to zero, and both inverters inject almost the same amount of harmonic current (Figs. 10b and 10c). At t= 2 s the virtual admittances are increased, the VSI-VCM injecting less harmonic current than the VSI-CCM, due its higher virtual admittance ($0.05 \ \Omega^{-1}$ vs. $0.01 \ \Omega^{-1}$). It is noted however that, in this case, the VSI-VCM injects less harmonic current than in the previous simulation (e.g. 0.43A vs. 0.58A for the 5th harmonic). This is due to the VSI-VCM higher output impedance (LCL+TL), which results in a lower current for the same harmonic voltage. It is important to note that the same current as the previous experiment could be obtained using a different virtual admittance magnitude. Such behavior is clearly observed when both inverters have the same virtual admittance (t>3 s): VSI-VCM inverter always injects less current than VSI-CCM inverter. It is also observed from Fig. 10b (t>4 s) that the higher the magnitude of the virtual admittance of both inverters is, the lower is the current injected by the inverter with the highest output impedance.

V. EXPERIMENTAL RESULTS

Laboratory-scaled experimental results are presented in this section. Details of the experimental setup can be found in Fig. 4 and Table I. The central controller (Figs. 2 and 4) has been programmed in a computer using *Matlab-Guide*. The PCC voltage, current references and virtual admittance magnitudes are shared between the central controller and the DSP controlling each inverter via *WiFi* link. The sampling frequency of the centralized controller is 5 Hz.

Fig. 11 shows the experimental results for the same operating conditions used in Fig. 8 for simulation.

At t=1 s the compensation of the -5th harmonic is enabled. It is observed from Fig. 11b that, as expected, both inverters inject a similar amount of harmonic current when the virtual admittances are set to zero. Conversely, the inverter with the larger virtual admittance injects less harmonic current to the non-linear load. The magnitude of the -5th harmonic is reduced to zero once the compensation is enabled, the THD reducing from ≈8.2% to ≈2% (see Fig. 11c).

Fig. 12 shows an oscilloscope capture of the PCC voltages before and after the compensation is enabled.
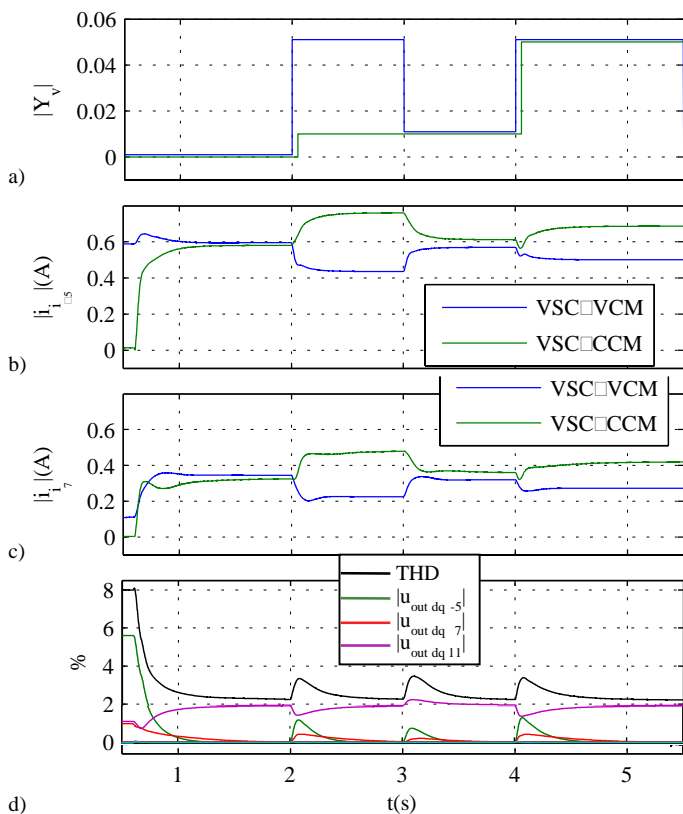

a)
b)
c)
d)

Fig. 10. Simulation results. Voltage harmonic compensation for different values of the virtual admittance and different line impedances between inverters. a) Virtual admittance. b) and c) magnitude of the resulting -5th and 7th current harmonics; d) Magnitude of the voltage harmonics and THD.
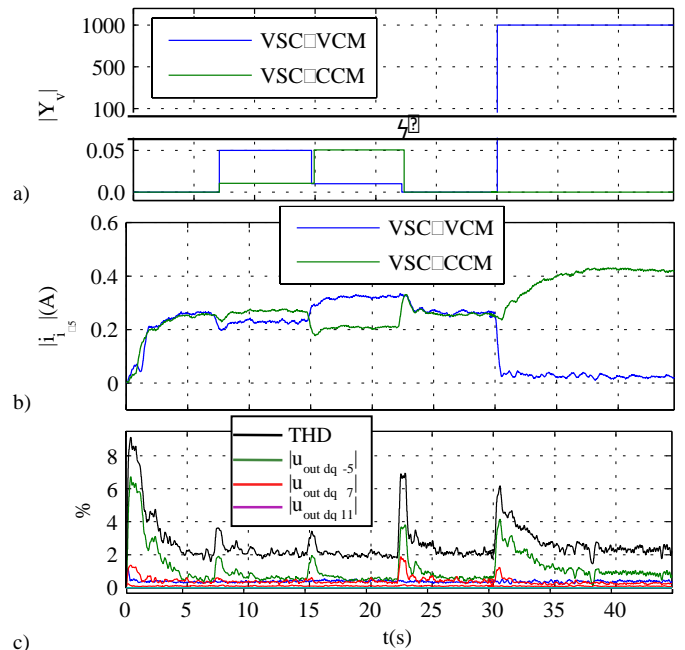

a)
b)
c)

Fig. 11. Experimental results. Voltage harmonic compensation for different values of the virtual admittance. a) Virtual admittance. b) magnitude of the resulting -5th current harmonic; c) Magnitude of the voltage harmonics and THD, shown as a percentage of the fundamental voltage.

For t>30s the virtual admittance of the VSI-CCM and the VSI-VCM are set to $0.01\Omega^{-1}$ and $1000\Omega^{-1}$ respectively (see Fig. 11a). It is observed from Fig. 11b that when the virtual admittance of an inverter is set to infinite (VSI-VCM, see Fig. 11a), that inverter does not contribute to the harmonic compensation.
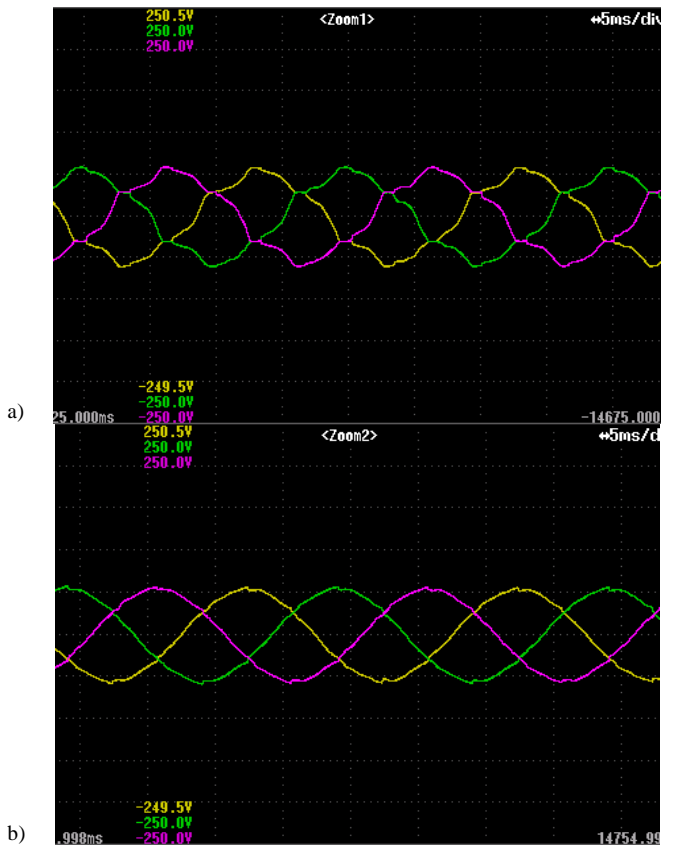
a)

b)

Fig. 12. Experimental results. Harmonic compensation. Detail of the PCC voltages a) before and b) after the compensation.
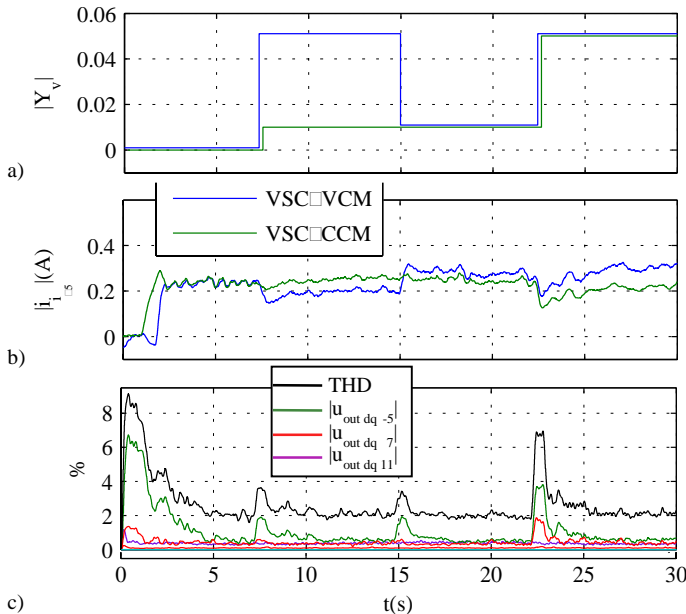

a)

b)

c)

Fig. 13. Experimental results. Voltage harmonic compensation for different values of the virtual admittance and different line impedances between the inverters. a) Virtual admittance. b) magnitude of the resulting -5th current harmonic; c) Magnitude of the voltage harmonics and THD, shown as a percentage of the fundamental voltage.

Thus, the rest of the inverters (i.e. VSI-CCM) are required to provide all the current needed to realize the compensation. It is observed that the experimental results are in good agreement with simulation results (Fig. 8).

One reason for the differences between simulation and experimental results comes from the fact that the current required to compensate for each harmonic (Fig. 11b) is close to the sensitivity limit of the current sensors, therefore decreasing the signal-to-noise ratio and reducing the accuracy of the PI-RES current control loop in the real implementation. This effect does not occur in simulation.

Finally, Fig. 13 shows the experimental results when different line impedances exist between the inverter and the PCC. The transmission line was emulated using a series connection of a resistance (R_{TL}=2Ω) and an inductance (L_{TL}=2mH), placed between the output LCL filter of the VSC-CCM and the PCC. Fig. 13a shows the virtual admittances used in this experiment.

Until t=7.5 s both virtual admittances are set to zero, the experimental results showing the same tendencies as the simulation results in Fig. 10b, with both inverters injecting a similar amount of current. For 7.5 s<t<15s, the virtual admittances are different. The VSI-VCM has the higher virtual admittance (Y_v=0.05Ω^{-1}), and consequently injects less harmonic current than the VSI-VCM. For t>15 s, both inverters have the same virtual admittance, the VSI-VCM injecting more current than the VSI-CCM. As for the simulation results, the higher the virtual admittance of both inverters is, the lower the current injected by the inverter with the higher output impedance is (VSI-CCM, see Fig. 13b). This is a very interesting result. If the same virtual admittance is used for all the inverters, those with a higher impedance to the PCC will inject less harmonic current (see Fig. 13b, 15s<t<30s). On the contrary, inverters closer to the PCC and therefore with a lower impedance, will inject more harmonic current, transmission losses being therefore reduced [33].

VI. Conclusions

A method for harmonic current sharing between parallel-connected inverters based on the use of virtual admittances has been presented in this paper. Though the concept shares some characteristics with virtual impedance based methods, it has the advantage of being applicable to any inverter topology and/or mode of operation, including VSI-VCM and VSI-CCM.

A centralized harmonic compensation strategy has been presented to test the feasibility of the proposed virtual admittance concept. The design of the virtual admittance control loop includes a *non-phase-disturbing* control loop and the decoupling of the output filter effects. This guarantees that all the inverters inject the required harmonic current in phase at the PCC. The proposed method also has the benefit of reducing the transmission losses, as inverters located farther from the PCC inject less harmonic current than inverters located closer to the PCC.

Simulation and experimental results have been provided to demonstrate the viability of the proposed method.

REFERENCES

[1] R. Lasseter, "MicroGrids," IEEE-PES, pp. 305–308, New York, Jan. 2002

[2] X. Guo, W. Wu, and Z. Chen, «Multiple-Complex Coefficient-Filter-Based Phase-Locked Loop and Synchronization Technique for Three-Phase Grid-Interfaced Converters in Distributed Utility Networks», IEEE Trans. Ind. Electron, 58(4): 1194 -1204, Apr. 2011.

[3] J. C. Vasquez, J. M. Guerrero, M. Savaghebi, J. Eloy-Garcia, and R. Teodorescu, «Modeling, Analysis, and Design of Stationary-Reference-Frame Droop-Controlled Parallel Three-Phase Voltage Source Inverters», IEEE Trans. Ind. Electron, 60(4): 1271-1280, Apr. 2013.

[4] D. Reigosa, F.Briz, C. B. Charro, P. Garcia, and J. M. Guerrero, «Active Islanding Detection Using High-Frequency Signal Injection», IEEE Trans. on Ind. App., 48(7): 1588 -1597, Oct. 2012.

[5] Shafiee, Q.; Guerrero, J.M.; Vasquez, J.C., "Distributed Secondary Control for Islanded Microgrids—A Novel Approach," IEEE Trans. Pow. Electr, 29(2): 1018-1031, Feb. 2014.

[6] A.G.Tsikalakis and N.D.Hatziargyriou, «Centralized Control for Optimizing Microgrids Operation», IEEE Trans. on Energy Conv., 23(1): 241 -248, Mar. 2008.

[7] J. He, Y. Li, J. Guerrero, F.Blaabjerg, and J. Vasquez, «An Islanding Microgrid Power Sharing Approach Using Enhanced Virtual Impedance Control Scheme», IEEE Trans. on Pow. Electr. 28 (11), 5272-5282, Nov 2013.

[8] T.Vandoorn, B.Meersman, J. De Kooning, and L.Vandevelde, «Controllable Harmonic Current Sharing in Islanded Microgrids: DG Units With Programmable Resistive Behavior Toward Harmonics», IEEE Trans. on Power Delivery, 27(2): 831 -841, Apr. 2012.

[9] K. T. Tan, X. Y. Peng, P. L. So, Y. C. Chu, and M. Z. Q. Chen, «Centralized Control for Parallel Operation of Distributed Generation Inverters in Microgrids», IEEE Trans. on Smart Grid, 3(4): 1977–1987, Dec. 2012

[10] J. A. Oliver, R. Lawrence, and B. B. Banerjee, «How to specify power-quality-tolerant process equipment», IEEE Ind. Appl. Magazine, 8(7): 21-30, Sep. 2002.

[11] A. M. Blanco, R. Stiegler, and J. Meyer, «Power quality disturbances caused by modern lighting equipment (CFL and LED)», en PowerTech (POWERTECH), IEEE Grenoble, pp. 1-6, 2013.

[12] «IEEE Guide for Design, Integration, and Operation of Distributed Resource Island Systems with Electric Power Systems«, IEEE Std. 1547.4.2011.

[13] «IEEE Recommended Practice for Interconnecting Distributed Resources with Electric Power Systems Distribution Secondary Networks», IEEE Std 1547.6-2011, pp. 1 -38, 2011.

[14] El-Habrouk, M.; Darwish, M. K.; Mehta, P., "Active power filters: a review," IEE Proceedings Elec. Pow. Appl., , 147(7): 403,413, Sep 2000

[15] S. Lu, N. Samaan, R. Diao, M. Elizondo, C. Jin, E. Mayhorn, Y. Zhang, and H. Kirkham, «Centralized and Decentralized Control for Demand Response», in Innovative Smart Grid Technologies (ISGT), IEEE-PES, pp. 1 -8. Jan 2011

[16] S. Lu, M. A. Elizondo, N. Samaan, K. Kalsi, E. Mayhorn, R. Diao, C. Jin, and Y. Zhang, «Control Strategies for Distributed Energy Resources to Maximize the Use of Wind Power in Rural Microgrids», IEEE-PES, pp. 1 -8, Jul. 2011.

[17] C. Yuen, A. Oudalov, and A. Timbus, «The Provision of Frequency Control Reserves From Multiple Microgrids», IEEE Trans. Ind. Electron, 58(1): 173 -183, Jan 2011.

[18] D. Reigosa, F. Briz, C. Blanco, P. Garcia, and J.M. Guerrero, «Active Islanding Detection for Multiple Parallel-Connected Inverter-Based Distributed Generators Using High Frequency Signal Injection», IEEE Trans. on Pow. Electr. Early access.

[19] J. M. Guerrero, L. Garcia de Vicuna, J. Matas, M. Castilla, and J. Miret, «Output Impedance Design of Parallel-Connected UPS Inverters With Wireless Load-Sharing Control», IEEE Trans. on Ind. Electron., vol. 52, n.º 4, pp. 1126 - 1135, Aug. 2005.

[20] J. M. Guerrero, J. Matas, L. G. de Vicuña, M. Castilla, and J. Miret, «Wireless-Control Strategy for Parallel Operation of Distributed-Generation Inverters», IEEE Trans. on Ind. Electron., 53(7): 1461-1470, Oct. 2006.

[21] Ali Emadi, «Handbook of Automotive Power Electronics and Motor Drives», CRC Press 2005

[22] J. M. Guerrero, M. Chandorkar, T.-L. Lee, and P. C. Loh, «Advanced Control Architectures for Intelligent Microgrids Parts I and II: Decentralized and Hierarchical Control», IEEE Trans. Ind. Electron, 60(4), Apr. 2013.

[23] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna, and M. Castilla,"Hierarchical Control of Droop-Controlled AC and DC Microgrids—A General Approach Toward Standardization," IEEE Trans. Ind. Electron., 58(1): 158–172, Jan. 2011.

[24] J. He, Y. W. Li, D. Bosnjak, and B. Harris, «Investigation and Active Damping of Multiple Resonances in a Parallel-Inverter-Based Microgrid», IEEE Trans. on Power Electron., 28(1): 234 -246, Jan. 2013.

[25] D. Reigosa, P. Arboleya, C. Gonzalez-Moran, and J. Gomez-Aleixandre, «An Improved Control Scheme Based in Droop Characteristic Control for Microgrid Converters», IEEE-ICEMS, pp. 1-6, Nov. 2009.

[26] Cao Hai-Yan, «Virtual admittance Based Current Control Strategy for Grid-connected Inverters in Microgrid». PRZEGLAD ELEKTROTECHNICZNY (Electrical Review), R. 87 NR 12a/

[27] M. Castilla, J. Miret, J. Matas, L. G. de Vicuña, and J. M. Guerrero, «Linear Current Control Scheme with Series Resonant Harmonic Compensator for Single-Phase Grid-Connected Photovoltaic Inverters», IEEE Trans. Ind. Electron., 55(7): 2724 -2733, Jul. 2008.

[28] 2011Y. Wang, X. Wu, and Y. Yu, «A Virtual Admittance Control Strategy of Three-Phase Voltage Source PWM Rectifier Under Unbalanced Input Voltage Conditions», APPEEC, pp. 1 -6, Mar. 2010

[29] P. Rodriguez, I. Candela, C. Citro, J. Rocabert, y A. Luna, «Control of grid-connected power converters based on a virtual admittance control loop», IEEE-EPE, pp. 1-10, Sep. 2013.

[30] Z. Zou, Z. Wang, y M. Cheng, «Modeling, Analysis, and Design of Multifunction Grid-Interfaced Inverters With Output LCL Filter», IEEE Trans. on Pow. Electr., 29(7): 3830-3839, Jul. 2014.

[31] K. Ogata. «Modern control Engineering». Pearson, 2009

[32] V. Blasko and V. Kaura, «A New Mathematical Model and Control of a Three-Phase AC-DC Voltage Source Converter», IEEE », IEEE Trans. on Pow. Electr. 12(1): 116 -123, Jan 1997.

[33] F. Briz, D. Reigosa, C. Blanco and J.M. Guerrero, "Coordinated Operation of Parallel-Connected Inverters for Active Islanding Detection Using High Frequency Signal Injection," IEEE Trans. on Ind. Appl. Early Access

[34] D. Reigosa, P. Arboleya, J.M. Guerrero, P. Garcia and F. Briz, " Analysis of grid connected converters using a feed-forward disturbance decoupling current control," IEEE-IPEC, pp. 2976 -2983, July 2010.

[35] Ashish Ranjan Dash, B.Chitti Babu, K.B.Mohanty and Rahul Dubey, "Analysis of PI and PR Controllers for Distributed Power Generation System under Unbalanced Grid Faults," International Conference on Power and Energy Systems,1-6, 2011.

[36] G. Escobar; A. A. Valdez; J. Leyva-Ramos; P. Mattavelli, "Repetitive-Based Controller for a UPS Inverter to Compensate Unbalance and Harmonic Distortion," IEEE Trans. Ind. Electr., 54(1), 504-510, Feb. 2007.

[37] F. Briz, P. García, M.W. Degner, D. Diaz and J.M. Guerrero, "Dynamic Behavior of Current Controllers for Selective Harmonic Compensation in Three-phase Active Power Filters", IEEE Trans. on Ind. Appl., 49(3), 1411-1420, May-June 2013.

[38] C. Blanco, D. Diaz, F. Briz, and J.M. Guerrero, "Strategies for the Connection of Distributed Power Generation Units to Distorted Networks," IEEE Trans. on Ind. App., 51 (5), 4111-4120, Sept.-Oct. 2015

[39] K. Ogata. «Modern control Engineering». Pearson, 2009