The Voltage-Controlled Compensation Ramp: A Waveshaping Technique for Power Factor Correctors

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This paper has been presented at the 2008 IEEE Applied Power Electronics Conference (APEC) in Austin, Texas, on February 27th with the same title and the same authors.

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Abstract- **This paper deals with a new control method for Power Factor Correctors. Control is carried out by a standard IC controller for peak current-mode dc-dc converters, with only an additional compensation ramp generator and peak detector. Neither an analog multiplier nor an input voltage sensor is needed to achieve quasi-sinusoidal line waveforms, which makes this method very attractive. The method is similar to the One-Cycle Control method, but can be very easily adapted for use with topologies different to the boost converter, i.e. flyback, buck-boost, SEPIC, Cuk and zeta topologies. Moreover, as the line current is cycle-by-cycle controlled, the resulting input current feedback loop is extremely fast, thus allowing the use of this type of control with high frequency lines.**

I. INTRODUCTION

Power Factor Correctors (PFCs) are widely used as the first stage in many ac-dc power supply systems, especially if the total power handled by the system is above 75 W. Among the methods proposed to control PFCs [1-14, 17-19], the following three are the most popular:

A. Voltage-Follower Control [2-9]

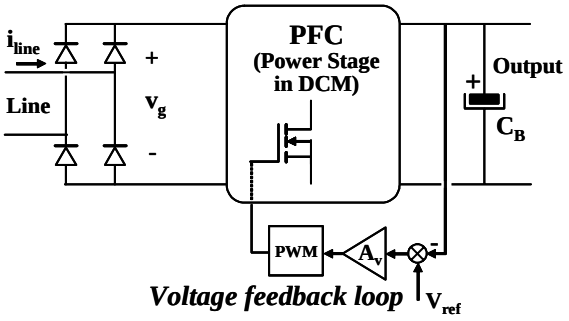
A very simple solution providing an almost sinusoidal (in the case of the boost converter [3]) or completely sinusoidal (in the case of the flyback family of converters [4-7]) line current waveform consists in designing the topology to always operate in the Discontinuous Conduction Mode (DCM) [4-7, 15]. In this case, only one voltage feedback loop (see Fig. 1a) is needed [2-9]. Since only one feedback loop is used to control the converter, and as any conventional switching-mode power supply controller can be used for this purpose, the control circuitry is hence extremely simple. Another advantage of this option is that the output diode does not exhibit reverse recovery problems because it is not conducting any current when the transistor is turned on.

However, this option also has certain drawbacks. For example, the peak value of the current passing through many components (transistor, diode, inductor, input and output filter capacitors, etc.) is about twice as high as in the case of operating in Continuous Conduction Mode (CCM). Consequently, the conduction losses are clearly higher. Even the switching losses when the transistor is turned off are higher than in the case of operating in CCM.

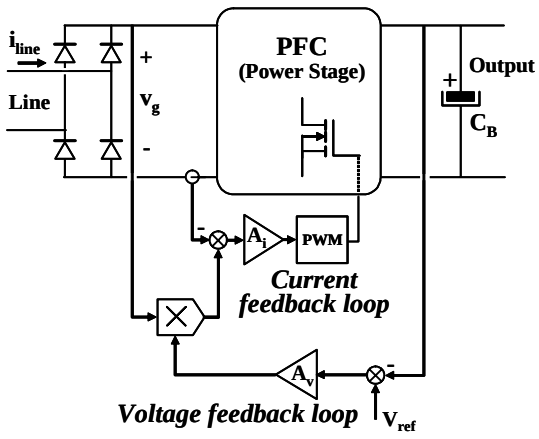
B. Analog-Multiplier based Control [1, 2]

The classical method for obtaining a perfectly sinusoidal line waveform consists in using a control strategy based on two feedback loops, one input-current feedback loop and an output-voltage feedback loop. Furthermore, an analog multiplier must be used in the control circuitry (see Fig. 1.b). This option means that the converter can work in both modes of operation (DCM and CCM). By designing the converter to operate in CCM at heavy loads, the current stress is clearly lower than in the case of operating in DCM at these loads. Therefore, efficiency is higher using this option.

The main disadvantage of this option is the complexity of the control circuitry and its cost. Several controllers can be used for this purpose, but they are not cheap, especially in comparison with standard controllers for



(a)



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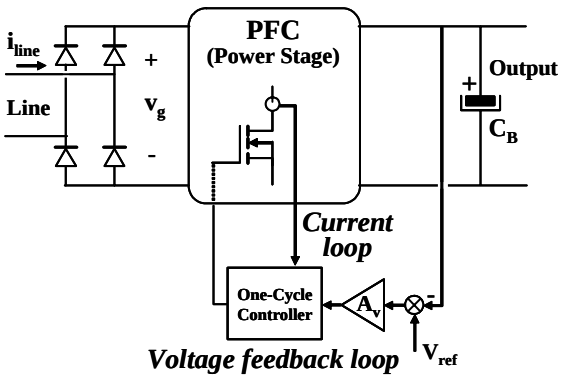


(c)

Fig. 1: Three of the most popular methods for controlling PFCs. a) Voltage-Follower Control. b) Analog-Multiplier Based Control. c) One-Cycle Control.

switching-mode power supplies. If the converter has to be a very low-cost one, the use of PFC controllers based on an analog multiplier becomes relatively expensive. Finally, the available controllers based on this technique cannot operate above 400 Hz due to their limited input-current error amplifier bandwidth, which means that this method is unsuitable for use in the case of high-frequency lines (clearly above 400 Hz).

C. One-Cycle Control [18-22]

In the last years, some authors have proposed different low cost control strategies for PFCs operating in CCM [16-22]. The objective of these control strategies is to simplify the existing control circuitry based on an analog multiplier. This simplification makes sense in the case of relatively low-power and wide input voltage range applications, as PFCs for many types of PC power supplies, electronic ballast and battery chargers in the range of 100-500 W. The One-Cycle Control (OCC) technique is a significant low cost strategy to control PFCs based on the boost converter topology. It was introduced in [18] for any type of switching converter. This type of control is proposed in [19] to be used in PFCs (see Fig. 1.c), where it is termed Linear Peak Current Mode Control (LPCMC). In [20], the idea of OCC is generalized to obtain a general pulsewidth modulator, which is particularized in [21] to be used in PFC applications. For the particular case of the boost PFC, this general pulsewidth modulator becomes the same as the LPCMC [21], and it is called again OCC in [22]. It is quite simple because it does not need to use an analog multiplier, in spite of being used in PFCs operating in CCM. Moreover, no input voltage sensing is needed using OCC. As it has been mentioned, the implementation of this control method is quite simple in the case of PFCs based on boost converters, because only one signal integrator is needed. It should be noted that the integrator time constant must match the switching period [18, 19] for proper operation. In the case of PFCs based on converters belonging to the flyback family (i.e. buck-boost, SEPIC, Cuk and zeta), either two matched integrators or a current sensor with an integrator with reset must be used [20,21]. This fact makes this method less attractive in the case of the flyback family of converters.

A new low-cost control strategy for wide PFCs is presented in this paper. This control strategy is called Voltage-Controlled Compensation Ramp (VCCR) Control. It allows the use of conventional peak current-mode controllers for switching-mode power supply to control wide input voltage range PFCs operating in CCM. Thus, both low-cost (due to the controller used) and high efficiency (due to the CCM operation) are achieved. Moreover, input current is cycle-by-cycle controlled. Therefore, the input current feedback loop is extremely fast, thereby allowing this type of control to be used with relatively high frequency lines (clearly above 400Hz). It should be noted that the line

frequency used in the electrical power distribution system in aircrafts is 400 Hz and higher frequencies have been under consideration. The price to pay for these advantages is the quality of the line waveform, which will be very sinusoidal at full load, but will be less sinusoidal when the load decreases. However, this is not a major problem, since regulations (especially IEC-1000-3-2, [23, 24]) must be met only at full load and due to the fact that the line waveform maintains a very high Power Factor (PF) under all operating conditions.

The implementation of VCCR Control for the case of PFCs based on the boost converter is very similar to the OCC implementation for the same PFC [22]. However, the VCCR control method avoids critical matching between the integrator time constant and the switching period [20, 21, 22] and can be very easily modified for use with PFCs based on the flyback family of converters.

II. COMPARISON BETWEEN OCC AND VCCR CONTROL

Figure 2 shows three controllers for PFCs. The first one (Fig. 2a) corresponds to the OCC for the boost PFC, whereas the second and the third (Fig. 2b and Fig. 2c) belong to the VCCR type. The main voltage waveforms for the control method shown in Fig. 2a are given in Fig. 3a. As this figure shows, the converter's duty cycle is determined by the instant when the voltage v_{EA}- $i_S R_S$ ($i_S R_S$ being the voltage across the current sensor) equals the

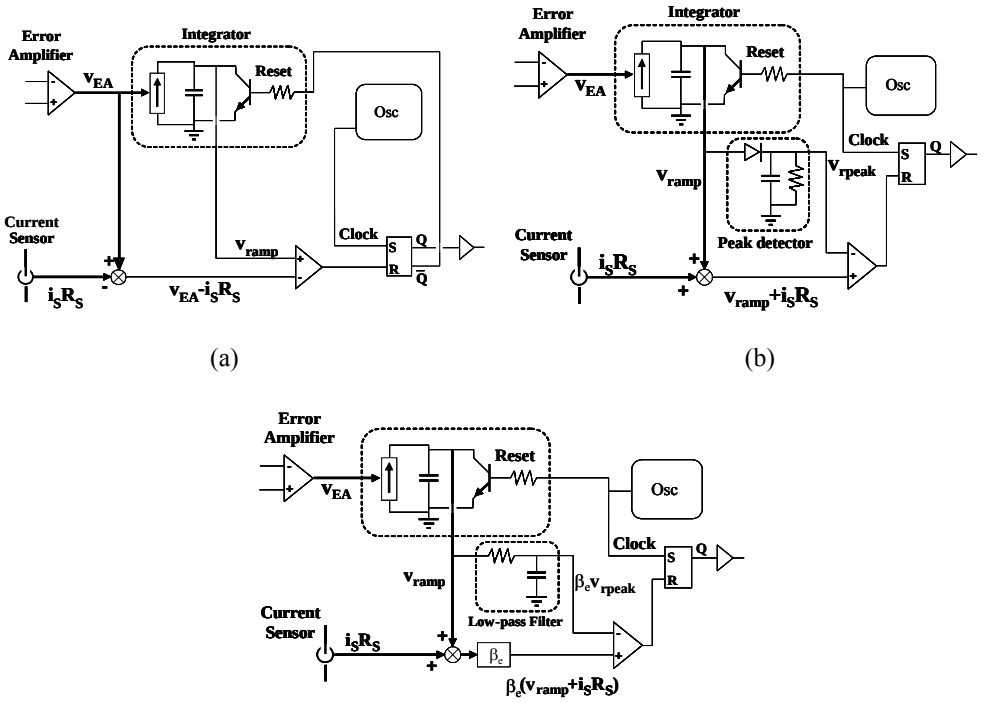
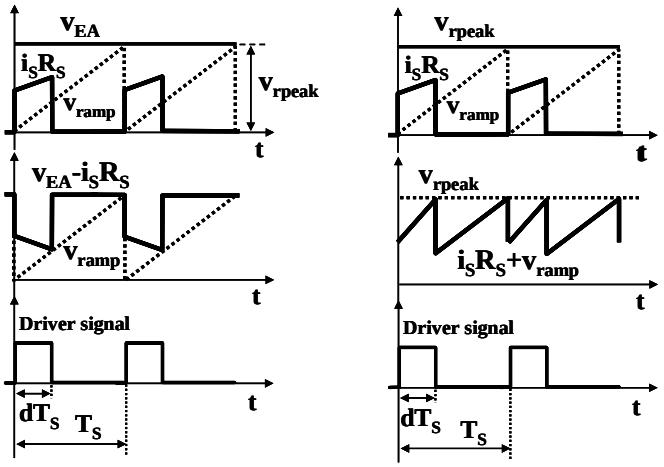


Fig.2: a) Implementation of the OCC for the boost PFC. b) Implementation of the VCCR Control with peak detector. c) Implementation of the VCCR Control with low-pass filter.



(a) (b)

Fig.3: a) Main waveforms in Fig. 2a. b) Main waveforms in Fig. 2b.

value of the integrator output at that instant [22]. For this method to operate properly, the time constant of the integrator must be equal to the switching period T_S. As a consequence of this, the peak value of the ramp, v_{rpeak}, is equal to the control signal, v_{EA}.

On the other hand, the converter's duty cycle in the circuit shown in Fig. 2b is determined by the instant when the voltage $v_{ramp}+i_S R_S$ equals the peak value of the ramp, v_{rpeak} (see Fig. 3b). Therefore, no matching between the time constant of the integrator and the switching period T_S is needed. Two implementations are possible to determine v_{rpeak}. The first one is based on the use of a peak detector to calculate v_{rpeak} (Fig. 2b). The second one is based on the fact that the dc component of a compensation ramp waveform is always proportional to its peak value, β_e being the proportionality constant. In the case of a linear compensation ramp β_e equals 0.5. Consequently, the converter's duty cycle can be obtained by using a very simple RC low-pass filter, as is shown in Fig. 2c.

In summary, OCC and VCCR Control are very similar methods. However, the main difference between them is the way of determining the peak value of the ramp waveform, v_{rpeak}. In the case of OCC, the time constant of the integrator must be adjusted to obtain $v_{rpeak} = v_{EA}$, whereas VCCR Control obtains the value of v_{rpeak} either by a peak detector or by a low-pass filter, but with no any particular matching in the integrator time constant. It should be noted that this matching is not a major problem if the integrator is based on an operational amplifier. However, if the integrator is based on a general purpose PNP bipolar transistor in order to maintain the cost as low as possible, this matching is very difficult because the integrator time constant depends on the transistor gain h_{FE}, which can differ from one transistor to another. Moreover, when OCC is implemented in an IC (like IR 1150) [22], this matching

process is achieved internally and the integrator capacitor is not externally accessible. This fact makes it impossible to modify the integration process to adapt it to be used for other PFCs, as it will be described for VCCR Control in Section V.

For conventional dc-dc converters, OCC has the advantage of faster response if v_{EA} undergoes extremely fast variations. However, this advantage disappears when controlling PFCs, since v_{EA} undergoes slow variations due to the bandwidth limitations of the output-voltage feedback loop [1,2]. This is due to the fact that a 10-20 Hz low-pass filter is placed into the error amplifier of the voltage feedback loop to obtain a low distortion of the line current. Hence, the use of either the peak detector or of the low-pass filter (see Fig 2b and Fig. 2c) in VCCR control, both designed to operate according to the switching frequency (around 100 kHz), does not represent any appreciable additional bandwidth limitation in comparison to the one due to the error amplifier. Moreover, the implementation of VCCR Control has the advantage of being suitable for other type of compensation ramps, which will make it possible to use this control method with PFCs based on other types of converters besides the boost converter.

III. INPUT CURRENT STATIC ANALYLIS OF THE BOOST PFC WITH OCC AND VCCR CONTROL

Figure 4.a shows a boost PFC with either OCC or VCCR Control. The control waveforms for this converter operating in CCM are shown in Fig. 3. These waveforms can be synthesized in the waveforms given in Fig. 4b. If the converter is operating in DCM, the main waveforms become the ones given in Fig. 4c. In both cases, the converter duty cycle d is determined by the control signal v_{rpeak}. The relationship between v_{EA} and v_{rpeak} is:

$$v_{rpeak} = k_0 + k_i v_{EA}, \tag{1}$$

where k_0 and k_i are constant parameters (k_0 is zero and k_i is 1 in the case of OCC). From geometric relationships in these waveforms, we can easily obtain:

$$i_{S2} = \frac{v_{rpeak}(1-d)}{R_S}, \tag{2}$$

where i_{S2} is the value of transistor current just before it stops conducting. The remaining equations needed to study the converter operation depend on the conduction mode.

A. Operation in Continuous Conduction Mode (CCM)

In this case, Faraday's law applied to both the transistor and the diode conduction periods yields:

$$v_g = Lf_S \frac{i_{S2} - i_{S1}}{d}, \tag{3}$$

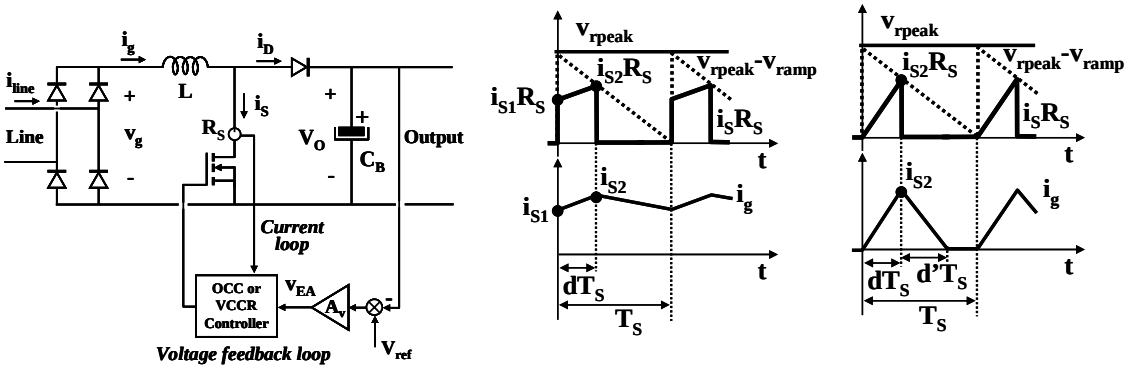
$$V_o - v_g = Lf_S \frac{i_{S2} - i_{S1}}{1 - d}, \tag{4}$$

where i_{S1} is the value of transistor current when it starts conducting, f_S is the switching frequency ($f_S=1/T_S$), v_g is the input voltage and V_O is the output voltage. From (2)-(4), we can easily obtain:

$$i_{S2} = \frac{v_g}{V_o} \cdot \frac{v_{rpeak}}{R_S}, \tag{5}$$

$$i_{S1} = \frac{v_g}{V_o}\left[\frac{v_{rpeak}}{R_S} - \frac{V_o - v_g}{Lf_S}\right]. \tag{6}$$

The value of the average inductor (and line) current i_{gav} is:



(a) (b) (c)

Fig.4: a) Boost PFC with OCC or VCCR Control. b) Waveforms in CCM. c) Waveforms in DCM.

$$i_{gav} = \frac{i_{S2} + i_{S1}}{2}, \tag{7}$$

and from (5)-(7), we can obtain:

$$i_{gav} = \frac{v_g}{V_o}\left[\frac{v_{rpeak}}{R_S} - \frac{V_o - v_g}{2\,Lf_S}\right]. \tag{8}$$

This last equation shows that if the product Lf_s satisfies the relationship

$$Lf_S >> \frac{V_o - v_g}{2} \cdot \frac{R_S}{v_{rpeak}}, \tag{9}$$

then i_{gav} and v_g will be proportional, performing ideal power factor correction.

B. Operation in Discontinuous Conduction Mode (DCM)

Figure 4.c shows the same waveforms as those shown in Fig. 4.b, though now with the converter operating in DCM. In this case, i_{S1} is always zero and (3) and (4) become:

$$v_g = Lf_S \frac{i_{S2}}{d}, \tag{10}$$

$$V_o - v_g = Lf_S \frac{i_{S2}}{d'}. \tag{11}$$

From (2) and (10), we can obtain:

$$i_{S2} = \frac{v_{rpeak}}{R_S} \cdot \frac{1}{1 + \frac{Lf_S v_{rpeak}}{v_g R_S}}. \tag{12}$$

The value of i_{gav} is, in this case:

$$i_{gav} = \frac{i_{S2}(d + d')}{2}, \tag{13}$$

and from (10)-(13), we finally obtain:

$$i_{gav} = \frac{1}{2}\left(\frac{v_{rpeak}}{R_S}\right)^2 \frac{v_g V_o}{(V_o - v_g) Lf_S} \cdot \frac{1}{\left(\frac{v_{rpeak}}{R_S} + \frac{v_g}{Lf_S}\right)^2}. \tag{14}$$

C. Boundary between both conduction modes

The value of i_{S1} is given by (6) in CCM, whereas it is equal to zero in DCM. Therefore, (6) must be equal to zero just on the boundary between both modes, That is:

$$v_{rpeak\_crit} = R_S \frac{V_o - v_g}{Lf_S}, \tag{15}$$

where v_{rpeak_crit} is the value of v_{rpeak} that determines the boundary between modes. A dimensionless parameter K will be used to study the boundaries between CCM and DCM:

$$K = \frac{2Lf_S v_{rpeak}}{R_S V_{gP}}, \tag{16}$$

where V_{gP} is the peak value of the line voltage:

$$v_g = V_{gP}\left|\sin\omega_L t\right|. \tag{17}$$

Moreover, we shall define another dimensionless parameter M as follows:

$$M = V_o / V_{gP}. \tag{18}$$

From (15)-(18), we can define the boundary value of K:

$$K_{crit} = 2(M - \left|\sin\omega_L t\right|). \tag{19}$$

K_{crit} has different values depending on the line angle. Hence, its maximum and minimum values are, respectively:

$$K_{crit\_max} = 2M, \tag{20}$$

$$K_{crit\_min} = 2(M-1). \tag{21}$$

Therefore, three operation modes are possible: Always in CCM, if $K > K_{crit\_max}$, in both modes (depending on the line angle), if $K_{crit\_max} > K > K_{crit\_min}$ and always in DCM, if $K_{crit\_min} > K$.

It should be noted that the converter will pass through these three modes in many standard designs, from heavy load (always CCM) to light load (always DCM). Figure 5 shows line current waveforms for different design, different input voltage and load conditions. Each input current waveform in Fig. 5a and Fig. 5b is normalized to its peak value and each input current waveform in Fig. 5c and Fig. 5d is normalized to the peak value of the input current at full load. As Fig. 5 shows, the line current waveform depends on the value of M and K. When M is relatively low (Fig 5a), the line current is very sinusoidal if $K>K_{crit\_max}$, which means that the converter is operating always (for any line angle) in CCM at full load. When M is relatively high (Fig. 5b), the line current is always very

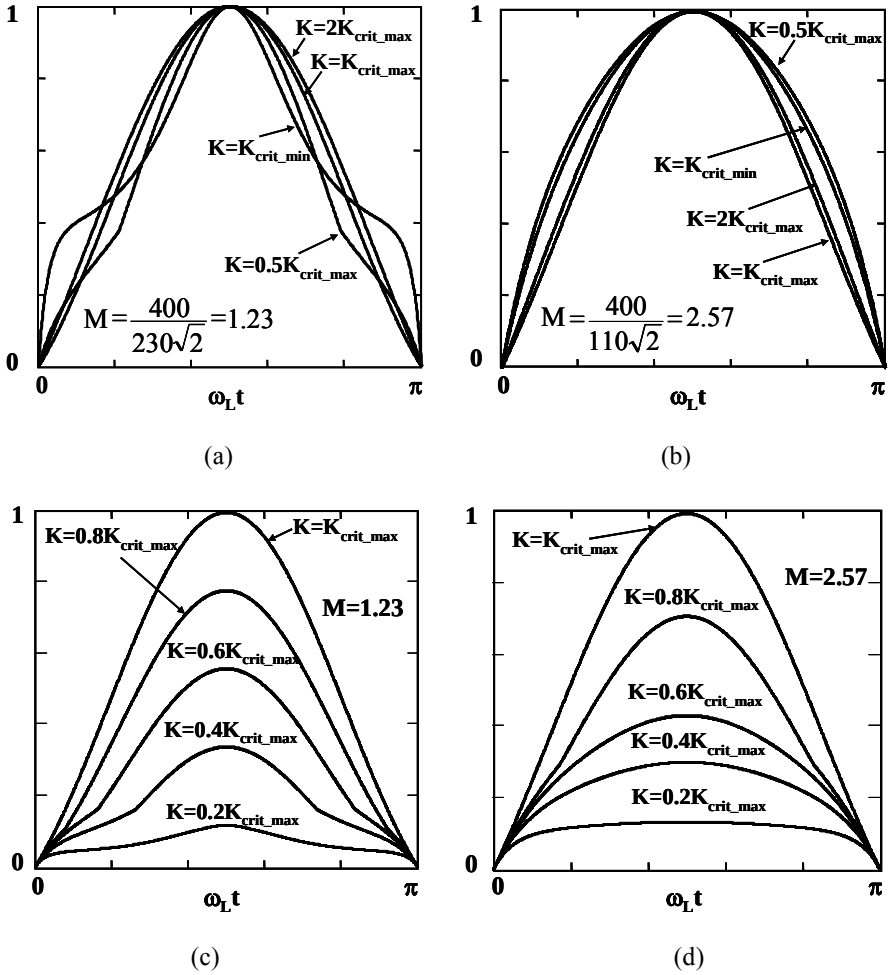


Fig.5: Different line current waveforms for a boost PFC with OCC or VCCR Control: a) M=1.23 and different K values at full load. b) M=2.57 and different K values at full load. c) M=1.23, $K=K_{crit\_max}$ at full load, and different K values (K= 0.8, 0.6, 0.4 and 0.2 of K_{crit_max}, which correspond with 76.4%, 53.1%, 31% and 10.9% of the full load respectively). d) M=2.57, $K=K_{crit\_max}$ at full load, and different K values (K= 0.8, 0.6, 0.4 and 0.2 of K_{crit_max}, which correspond with 70.3%, 47.3%, 34.4% and 16.7% of the full load respectively).

sinusoidal. Both previous conditions are not very exigent. Therefore, the condition in equation (9), and the similar ones derived, does not compromise the PFC design. Also, the PF and the Total Harmonic Distortion (THD) of the waveforms shown in Fig. 5 are given in Fig. 6.

As (16) shows, the K value increases when the input voltage decreases. As a consequence of this (Fig.6), the distortion of the input current decreases when the input voltage decreases. This conclusion is very important to make possible the use of VCCR control in the case PFCs working in the universal range of input voltage. In this case the

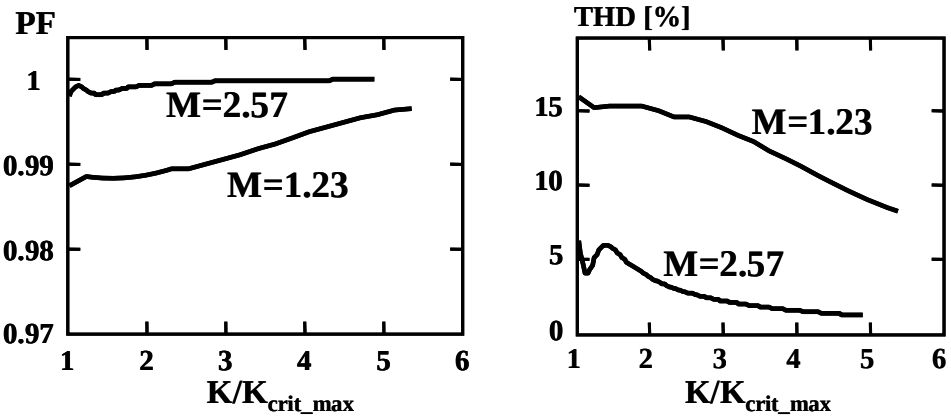


Fig.6: Power Factor (a) and Total Harmonic Distortion (b) corresponding to waveforms shown in Fig. 5.

criterion is very simple: The PFC must be designed to have the desired PF and THD at the highest nominal input voltage. It should be noted that the PF and THD will have better values at the lowest nominal input voltage.

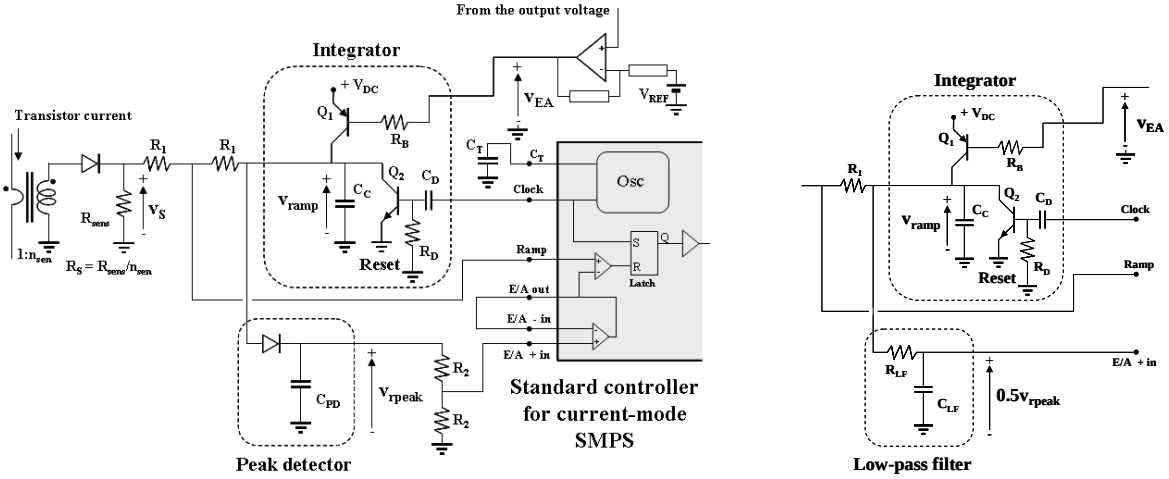
D. Implementation of the VCCR Control

Figure 7 shows the use of a standard peak current mode controller to implement VCCR Control in a boost PFC. The ramp voltage v_{ramp} is generated by the integrator block. It has a peak value, v_{rpeak}, which is determined by the voltage v_{EA} (output of the error amplifier placed in the output voltage feedback loop) according to (1). In this implementation, k_0 is positive and k_i is negative. The voltage-controlled ramp is used as a compensation ramp, as in any standard peak current-mode control. The proposed control method has accordingly been called Voltage-Controlled Compensation Ramp (VCCR). Figure 7a shows the circuitry to obtain the peak value of the voltage controlled ramp, v_{rpeak}, by using a peak detector. As the circuit actually calculates $0.5(i_S R_S+v_{ramp})$ instead of $i_S R_S+v_{ramp}$, v_{rpeak} must be divided by 2 to operate properly (the resistor divider make up of resistors R_2 performs this function).

The implementation of this control with a low-pass filter can be easily carried out by substituting the peak detector for a low-pass filter and removing the resistor divider (resistors R_2), as shown in Fig 7b.

IV. Input current static analylis of the Flyback Family of PFCs with VCCR Control

A. Operation in Continuous Conduction Mode (CCM)



(a) (b)

Fig.7: Implementation of the VCCR Control for a boost PFC using two different solutions to determine the v_{rpeak} value: a) Peak detector. b) Low-pass filter.

Figure 8 shows a flyback PFC with VCCR Control. The analysis carried out here for this converter is also valid for SEPIC, Cuk and zeta PFCs. In these cases, (3) is also valid and (4) and (7) become:

$$V_o = nLf_S \frac{i_{S2} - i_{S1}}{1-d}, \tag{22}$$

$$i_{gav} = \frac{i_{S2} + i_{S1}}{2} d, \tag{23}$$

and from (2), (3), (22) and (23), we can obtain:

$$i_{gav} = \frac{nv_g V_o}{\left(V_o + nv_g\right)^2}\left[\frac{v_{rpeak}}{R_S} - \frac{V_o}{2nLf_S}\right]. \tag{24}$$

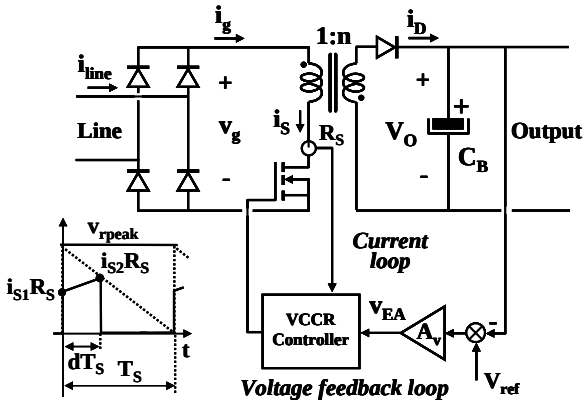


Fig.8: Flyback PFC with VCCR Control.

B. Operation in Discontinuous Conduction Mode (DCM)

In the case of the flyback family of converters in DCM, (10) is also valid and (13) becomes:

$$i_{gav} = \frac{i_{S2}d}{2}. \tag{25}$$

From (2), (3) and (25) we can obtain:

$$i_{gav} = \frac{v_g}{2Lf_S} \cdot \frac{\left(v_{rpeak}/R_S\right)^2}{\left(v_{rpeak}/R_S\right)^2 + \left(v_g/Lf_S\right)^2}. \tag{26}$$

C. Boundary between both conduction modes

The value of i_{S1} for this converter in CCM can be easily obtained from (2), (3) and (22):

$$i_{S1} = \frac{nv_g}{V_o + nv_g}\left[\frac{v_{rpeak}}{R_S} - \frac{V_o}{nLf_S}\right]. \tag{27}$$

The values of v_{rpeak_crit} and K_{crit} will thus be:

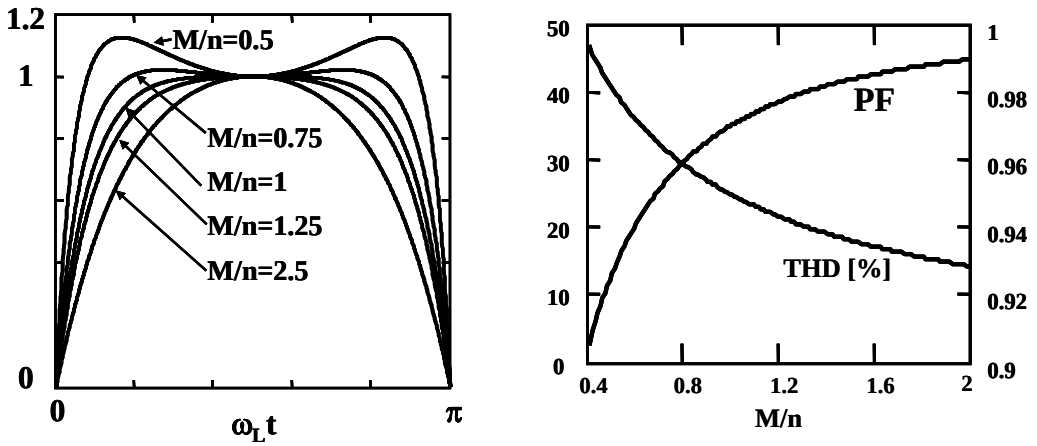
$$v_{rpeak\_crit} = \frac{V_o R_S}{nLf_S}, \tag{28}$$

$$K_{crit} = 2M/n. \tag{29}$$

Therefore, the boundary between modes does not depend on the line angle in the case of these converters. Hence, only two operation modes are possible in this case: Always in CCM, if $K > K_{crit}$ and always in DCM, if $K < K_{crit}$.

It should be noted that the shape of the line current waveform in CCM (24) does not depend on the value of v_{rpeak}; it only depends on the values of V_O, V_{gP} and n. In other words, this shape does not depend on K, but only depends on M/n, as is shown in Fig. 9a. For values of M/n selected for a standard design (between 0.5 and 1.5), the values of the THD and PF are not very desirable, as Fig. 9b shows.

However, examination of these waveforms shows that the main difference between them and a perfect sinusoidal waveform occurs just near the zero crossing, the waveform obtained being higher than the sinusoidal. This means that the duty cycle value obtained with VCCR Control and a linear ramp is excessive and a less distorted waveform could be obtained if the duty cycle were lower. A lower duty cycle near the zero crossing can be easily obtained if the linear ramp is substituted by an exponential ramp.



(a) (b)

Fig.9: a) Line waveforms in a flyback PFC with VCCR Control operating in CCM. b) PF and THD values as a function of M/n.

V. INPUT CURRENT STATIC ANALYLIS WITH AN EXPONENTIAL RAMP

The line current waveforms obtained in the case of the flyback family of converters (Fig.9a) can be improved if an exponential ramp is used instead of a linear one (Fig. 10). In this case, (2) is not valid and the relationship between v_{rpeak}, i_{S2} and d is:

$$i_{S2} = \frac{v_{rpeak}}{R_S} \cdot \frac{e^{-d\mu} - e^{-\mu}}{1 - e^{-\mu}}, \qquad (30)$$

where $\mu = T_S/\tau$, τ being the time constant of the exponential ramp.

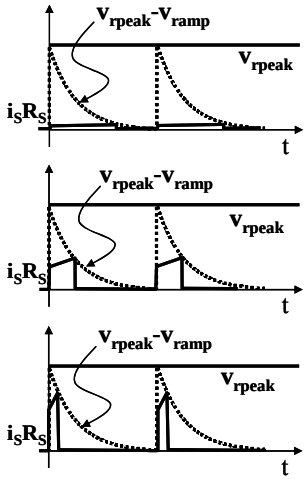


Fig.10: Main control waveforms for different line angle, from the zero crossing (top) to the peak line (bottom) for VCCR Control with an exponential compensation ramp.

A. Operation in Continuous Conduction Mode (CCM)

From (3), (22), (23) and (30), we can obtain the values of i_{gav} and i_{S1} in CCM:

$$i_{gav} = \frac{V_o}{V_o + nv_g}\left[\frac{v_{rpeak}\left(e^{-\frac{V_o}{(V_o+nv_g)}\mu} - e^{-\mu}\right)}{R_S(1-e^{-\mu})} - \frac{V_o v_g}{2Lf_S(V_o+nv_g)}\right], \qquad (31)$$

$$i_{S1} = \frac{v_{rpeak}\left(e^{-\frac{V_o}{(V_o+nv_g)}\mu} - e^{-\mu}\right)}{R_S(1-e^{-\mu})} - \frac{V_o v_g}{Lf_S(V_o+nv_g)}. \qquad (32)$$

B. Operation in Discontinuous Conduction Mode (DCM)

In DCM operation we can calculate the values of i_{S1}, i_{S2} and i_{gav}, from (10), (25) and (30). However, we obtain a transcendent equation that must be numerically solved.

C. Operation in Discontinuous Conduction Mode (DCM)

The limits between CCM and DCM can be found from (32):

$$v_{rpeak\_crit} = \frac{V_o R_S v_g}{Lf_S(V_o+nv_g)} \cdot \frac{1-e^{-\mu}}{e^{-\frac{V_o}{(V_o+nv_g)}\mu} - e^{-\mu}}. \qquad (33)$$

This equation can be rewritten as follows:

$$K_{crit} = \frac{2M\left|\sin\omega_L t\right|}{(M+n\left|\sin\omega_L t\right|)} \cdot \frac{1-e^{-\mu}}{e^{-\frac{M}{(M+n\left|\sin\omega_L t\right|)}\mu} - e^{-\mu}} \cdot \tag{34}$$

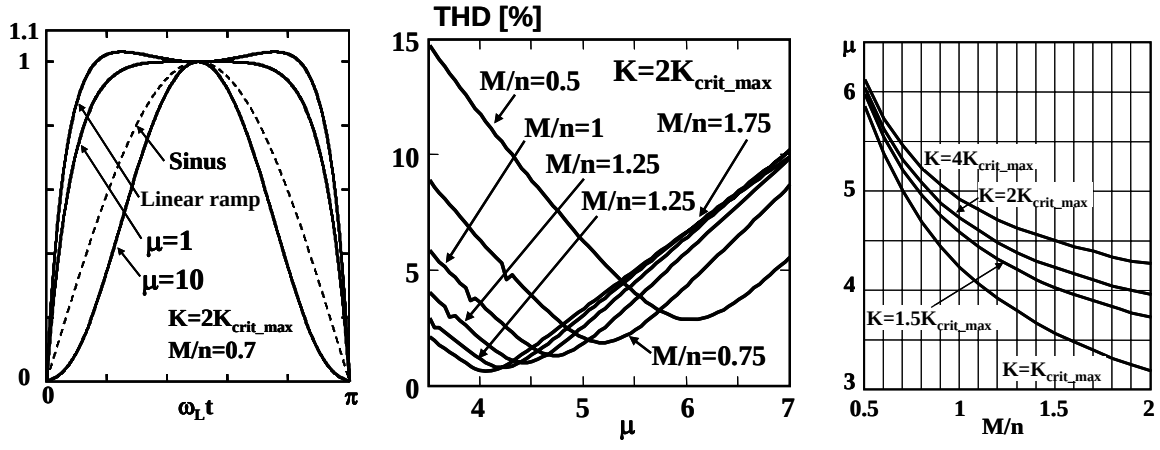
As (34) shows, K_{crit} has different values depending on the line angle. Hence, the maximum value of K_{crit} is:

$$K_{crit\_max} = \frac{2M(1-e^{-\mu})}{n\,\mu\,e^{-\mu}} \cdot \tag{35}$$

and the minimum value of K_{crit} is:

$$K_{crit\_min} = \frac{2M}{(M+n)} \cdot \frac{1-e^{-\mu}}{e^{-\frac{M}{(M+n)}\mu} - e^{-\mu}} \cdot \tag{36}$$

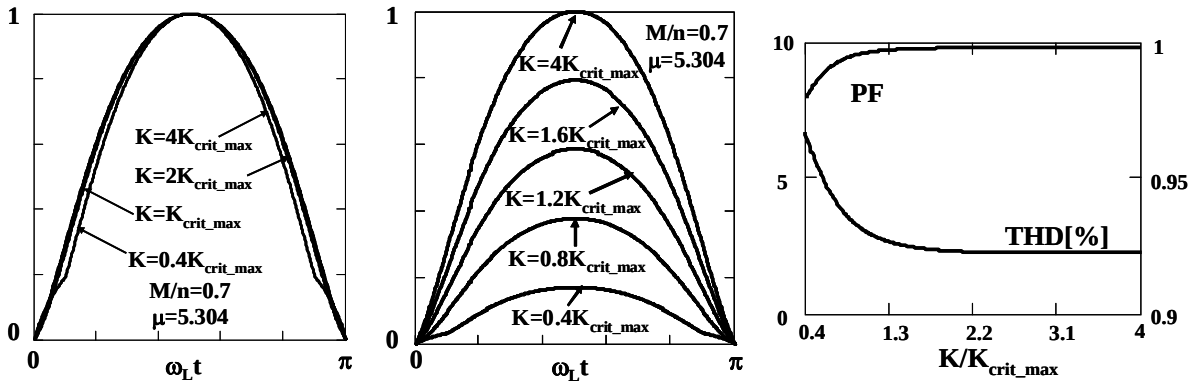
Therefore, the PFC operates in CCM for the entire line angle if $K > K_{crit\_max}$. Figure 11a shows the waveforms in CCM for several values of μ and the same design conditions (M/n=0.7, $K=2K_{crit\_max}$), whereas the THD for different values of M/n and μ are given in Fig. 11.b (in this case, $K=2K_{crit\_max}$ as well). The value of μ which optimizes the THD for any design case was obtained using a Mathcad spreadsheet. The results are shown in Fig. 11c.



(a) (b) (c)

Fig.11: a) Normalized line current for different values of μ. b) THD as a function of μ when $K=2K_{crit\_max}$.c) Values of μ to minimize the THD for different design conditions (M/n and K).

The value of μ must be chosen in order to minimize THD at nominal conditions, which are the conditions to comply with the regulations. However, if the PFC operates in a different point to the nominal one then the converter can operate in three modes: always in CCM, always in DCM and in both modes. Figure 12a shows line current waveforms for the above mentioned design (M/n=0.7, $K=2K_{crit\_max}$ and μ=5.304) when the value of K changes.



(a) (b) (c)

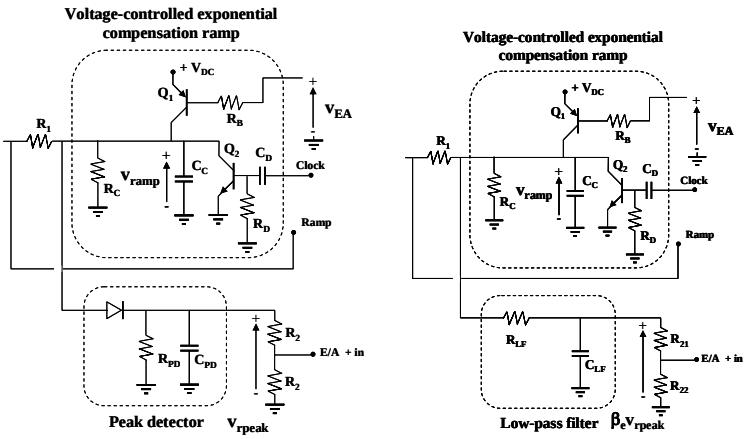
Fig.12: a) Line current waveforms for different operation points of the flyback PFC with the optimized exponential ramp. b) Line current waveforms for different loads. c) PF and THD corresponding to waveforms shown in Fig. 12a and 12b.

These waveforms have been normalized to their peak value. It should be noted that the value of K can change due to either an input voltage variation or a load variation, according to (16). The waveforms corresponding to the load variations have been represented in Fig.12b, where they have been normalized to the peak value of the input current at full load. Their PF and the THD values are given in Fig. 12c.

As can be seen in Fig. 12, the line waveforms obtained are slightly distorted for operation points different than the nominal one.

D. Implementation of the VCCR Control

In the case of flyback PFC two implementations are possible to determine v_{rpeak} too. The first one is based on the use of a peak detector to calculate v_{rpeak} (Fig. 13a).The second one is based on the fact that the dc component of an exponential ramp waveform can be easily calculated:



(a) (b)

Fig.13: VCCR Control with an exponential compensation ramp. a) Implementation with peak detector (only a resistor, R_C, has been added to the circuit shown in Fig. 7a). b) Implementation with low-pass filter (only resistors, R_C, R_{21}, R_{22} have been added to the circuit shown in Fig. 7b).

$$\bar{v}_{ramp} = \left(1 - \frac{1 - e^{-\mu}}{\mu}\right) v_{rpeak} = \beta_e \, v_{rpeak} \,. \qquad (37)$$

As (37) shows, v_{rpeak} can be easily obtained from the average value of the exponential ramp.

VI. Experimental Results

Two prototypes of PFCs controlled by the proposed method were built and tested. Their control was implemented using an IC UC3824, which is a controller for peak current-mode dc-dc converters. Some low cost external elements (Fig.7 and Fig. 13) were added to complete the overall controller. Moreover, some additional bias voltages (not shown in Fig. 7) were used to allow the use of the aforementioned IC.

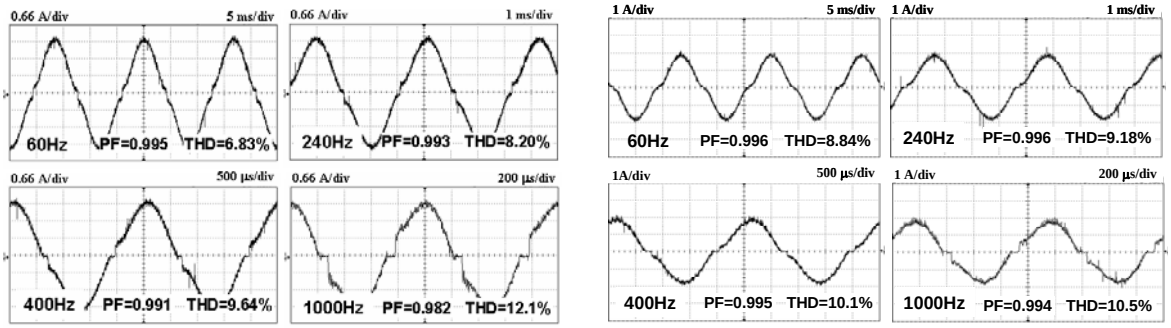
Boost case: The main characteristics of this converter are: $v_{g\,RMS}$ = 110V, V_O = 200V, P_O = 250W and f_S=80 kHz. Figure 14 shows the main results obtained at full load and different line frequencies (from 60Hz to 1kHz) for the two different ways to determine the ramp peak value. Figure 15 shows the waveforms at 60 Hz for different load conditions. As it was expected, the line waveforms are very similar to the ones obtained in [21] with OCC, using an IC IR1150. The waveforms given in Fig. 14 and in Fig. 15 show that the power factor is very high in all operating conditions. Table 1 shows the harmonic content of the input current and the compliance with IEC 1000-3-2 regulations at nominal input voltage and full load.

Finally, Fig. 16 shows the main control waveforms with a low-pass filter to determinate the peak value of the

Peak detector					Low-pass filter				
Harmonic order	**RMS current (A)**	**Limits Class (A)**	**Limits Class C (A)**	**Limits Class D (A)**	**Harmonic order**	**RMS current (A)**	**Limits Class (A)**	**Limits Class C (A)**	**Limits Class D (A)**
3	0,336	2,300	0,052	0,850	**3**	0,333	2,300	0,051	0,850
5	0,092	1,140	0,770	0,475	**5**	0,083	1,140	0,766	0,475
7	0,035	0,770	0,258	0,250	**7**	0,028	0,770	0,257	0,250
9	0,021	0,400	0,180	0,125	**9**	0,005	0,400	0,180	0,125
11	0,019	0,330	0,129	0,088	**11**	0,007	0,330	0,129	0,088
13	0,017	0,210	0,077	0,074	**13**	0,012	0,210	0,077	0,074
15	0,011	0,150	0,016	0,064	**15**	0,011	0,150	0,016	0,064
17	0,010	0,132	0,016	0,057	**17**	0,010	0,132	0,016	0,057
19	0,010	0,118	0,016	0,051	**19**	0,008	0,118	0,016	0,051
21	0,008	0,107	0,016	0,046	**21**	0,007	0,107	0,016	0,046
23	0,007	0,098	0,016	0,042	**23**	0,007	0,098	0,016	0,042
25	0,007	0,090	0,016	0,039	**25**	0,006	0,090	0,016	0,039
27	0,006	0,083	0,016	0,036	**27**	0,006	0,083	0,016	0,036
29	0,005	0,078	0,016	0,033	**29**	0,005	0,078	0,016	0,033
31	0,005	0,073	0,016	0,031	**31**	0,005	0,073	0,016	0,031
33	0,005	0,068	0,016	0,029	**33**	0,050	0,068	0,016	0,029
35	0,004	0,064	0,016	0,028	**35**	0,004	0,064	0,016	0,028
37	0,004	0,061	0,016	0,026	**37**	0,004	0,061	0,016	0,026
39	0,003	0,058	0,016	0,025	**39**	0,004	0,058	0,016	0,025

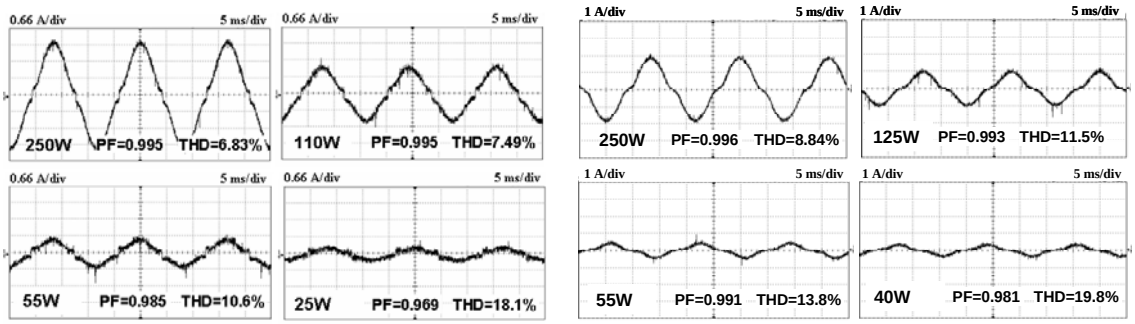
Table 1: Harmonic content in the prototypes of boost PFC.

controlled linear ramp. As this figure shows, the input current and control waveforms match with the static study presented in this paper.



(a) (b)

Fig. 14: Boost case: Line current at full load (250 W) for different line frequencies. a) Peak detector. b) Low-pass filter



(a) (b)

Fig. 15: Boost case: Line current at full load (250 W) for different line frequencies. a) Peak detector. b) Low-pass filter

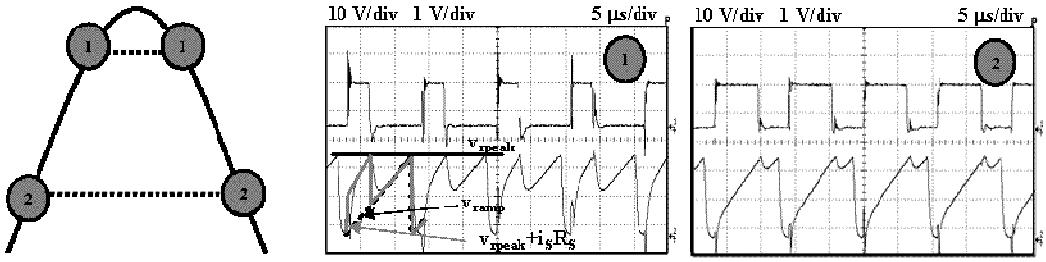
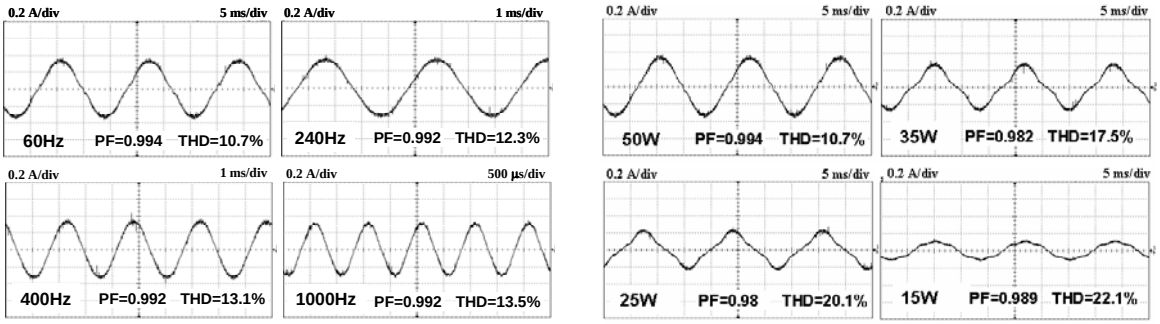


Fig. 16: a) Control waveforms using the low-pass filter

Flyback case: The main characteristics of this converter are: $v_{g\,RMS}$ = 110V, V_O = 12V, P_O = 50W and f_S=80 kHz. This prototype was only implemented with the low-pass filter technique. Figure 17a shows the line current at full load for different line frequencies, whereas Fig. 17b shows the waveforms for different load conditions. The harmonic content of the input current and the harmonic limits according with IEC 1000-3-2 are given in Table 2.



(a) (b)

Fig. 17: a) Flyback case: Line current at full load (250 W) for different line frequencies. b) Flyback case: Line current at 60 Hz for different output powers

Harmonic order	RMS current (A)	Limits Class (A)	Limits Class C (A)	Limits Class D (A)
3	0,027	2,300	0,010	0,170
5	0,012	1,140	0,156	0,095
7	0,001	0,770	0,052	0,050
9	0,003	0,400	0,037	0,025
11	0,005	0,330	0,026	0,018
13	0,005	0,210	0,016	0,015
15	0,004	0,150	0,016	0,013
17	0,004	0,132	0,016	0,011
19	0,004	0,118	0,016	0,010
21	0,003	0,107	0,016	0,009
23	0,002	0,098	0,016	0,008
25	0,002	0,090	0,016	0,008
27	0,002	0,083	0,016	0,007
29	0,002	0,078	0,016	0,007
31	0,001	0,073	0,016	0,006
33	0,001	0,068	0,016	0,006
35	0,001	0,064	0,016	0,006
37	0,000	0,061	0,016	0,005
39	0,000	0,058	0,016	0,005

Table 2: Harmonic content in the prototype of flyback PFC.

VII. CONCLUSION

A new method to implement One-Cycle Control in CCM PFCs has been presented in this paper. The method is based on the use of standard controllers for peak current-mode converters, employing neither an analog multiplier nor an input voltage sensor. Therefore this control method is useful for designing relatively low-cost PFCs .This

implementation can be used not only with the boost PFC, but it can be easily adapted for its use with the flyback family of converters, by employing an exponential ramp, instead of a linear one.

The results obtained show that PFs in the range of 0.99 have been measured at full load, whereas they slightly decrease at light load (0.98). In all cases the THD is better than 22% and the compliance with the IEC 61000-3-2 regulations is guarantied (in all Classes).

Moreover, the input current feedback loop is extremely fast, thus allowing this type of control to be used with relatively high frequency lines. The experimental results also show excellent PFs (0.99) and THD (better than 13%) at high lines frequencies and full load.

ACKNOWLEDGMENT

This research has been supported by the Spanish Ministry of Education and Science under project TEC2007-66917/MIC and grant AP2006-04777.

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