

### Universidad de Oviedo

### Department of Electrical, Computer and Systems Engineering

**P**rograma de Doctorado en Control de Procesos, Electrónica Industrial e Ingeniería Eléctrica

**D**octorate Program in Process Control, Industrial Electronics and Electrical Engineering

### Synchronization, islanding detection and power quality improvement in distributed power generation systems

**by** Cristian Blanco Charro

Dissertation submitted in fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering with International Mention

Gijón, June 2015



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To my family... Juan, Maxi, Nelson and Cristel

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## Resumen

La presente tesis se enmarca en la temática de la generación distribuida de energía eléctrica. En los últimos años la generación distribuida ha sido foco de gran actividad investigadora debido al aumento de la demanda energética y a la concienciación medioambiental. Tradicionalmente, la generación de energía eléctrica se ha venido realizado de forma centralizada, mediante el uso de grandes plantas generadoras, por lo que la energía eléctrica ha de transmitirse a través de largas distancias hasta los consumidores finales. En contra, mediante el uso de la generación distribuida, generadores de menor potencia se conectan a la red principal lo más cerca posible de los consumidores, con el objetivo de reducir las pérdidas de transmisión y el número y tamaño de las líneas de transmisión. No obstante, el uso de sistemas de generación distribuida plantea nuevos retos relacionados con la sincronización, detección de estado de islanding, problemas de calidad de red, reparto de carga...

Tres temas principales se discuten en la presente tesis:

- Sincronización de generadores distribuidos. La conexión entre unidades de generación distribuidas (habitualmente convertidores de potencia) y la red principal requiere que la tensión de salida del convertidor de potencia coincida (en magnitud y fase) con la tensión de red. El uso de métodos de sincronización es por lo tanto imprescindible para realizar una conexión física suave y asegurar un control de potencia preciso. En esta tesis se presentan tres algoritmos de sincronización: uno para sistemas monofásicos y dos para sistemas trifásicos.
- Detección de estado de islanding. Comúnmente se define la detección de islanding como la detección de si el convertidor de potencia se encuentra conectado a la red principal o aislado de la misma. Los convertidores de potencia deben detectar si están aislados o conectados a la red con el objetivo de adaptar sus algoritmos de control al estado de conexión.

Se presentan en esta tesis cinco algoritmos de detección de islanding, todos ellos basados en la estimación de la impedancia de salida de alta frecuencia del convertidor de potencia.

• Mejora de la calidad de red. Un convertidor de potencia debe cumplir un conjunto de normativas de conexión a red en cuanto a calidad de la energía se refiere. Habitualmente se implementan mecanismos para la reducción de la tasa de distorsión armónica (THD) y reducción de la tasa de variación de frecuencia y magnitud de la tensión de la red principal. Se proponen en la presente tesis dos algoritmos para la mejora de la calidad de red: un algoritmo para la mejora del THD y un algoritmo para la conexión suave de convertidores de potencia a redes distorsionadas.

# Abstract

This thesis is focused on distributed power generation (DPG) issues. In the last decades the use of DPG has been widely investigated due to the increase of electricity demand and environmental concerns. Traditionally, the electric power was generated in large centralized power plants and transmitted over long distances. Opposite to this, in the DPG concept generators are connected to the utility grid near where the electric power is used. This reduces the transmission losses as well as the size and number of power lines needed. However, some concerns as synchronization, islanding detection, grid stability, power quality, dispatchability,... arise due to the use of DPG units.

Three main topics are discussed in this thesis:

- Synchronization of DPG units. Connection of DPG units to a microgrid/utility grid requires the DPG unit output voltage to match the microgrid/utility grid voltage, (both in magnitude and phase) for smooth transition from island to grid-connected, also a correct synchronization of a DPG unit is required for to precisely control the generated active and reactive powers. Three synchronization methods are presented in this thesis: one for single-phase and two for three-phase DPG units.
- Islanding detection of DPG units, i.e. detection of whether the DPG unit is isolated or connected to the utility grid/microgrid. DPG units are required to detect if they are isolated or connected to the utility grid/microgrid to adapt their control algorithms to the operating conditions. Five islanding detection techniques are presented in this thesis, all of them based on the grid high frequency impedance estimation.
- DPG power quality enhancement. DPG units must comply with power quality grid codes. Algorithms to increase the power quality, e.g. total harmonic distortion reduction or rate of magnitude and frequency change reduction, are commonly implemented. Two algorithms for

power quality improvement are presented in this thesis, targeted towards THD improvement and smooth connection of DPG units to distorted grids respectively.

# Nomenclature

- $\vec{u}$  Complex vector.
- $\omega_0$  Fundamental positive-sequence pulsation.
- n Harmonic order.
- $\omega_n$  Pulsation of the  $n^{th}$  component.
- $\omega_{hf}$  Generic high frequency pulsation.
- $u_{\mu q}$  Inverter output filter voltage.
- $u_g$  Utility grid voltage.
- $U_n$  Magnitude of the  $n^{th}$  voltage component.
- $i_i$  Inverter-side injected current.
- $i_g$  Grid-side injected current.
- $x_{dq\,1}$  Fundamental positive-sequence voltage/current in SRF.
- $x_{dq n}$  Voltage/current in the  $n^{th}$  SRF.
- $u_{hf}$  Generic high frequency voltage signal.
- $i_{hf}$  Generic high frequency current signal.
- $Z_{dqhf}$  High frequency impedance.
- |Z| High frequency impedance magnitude
- $\phi_Z$  High frequency impedance phase angle
- $L_i$  Inverter-side LCL inductance
- $R_i$  Inverter-side LCL ESR
- $L_g$  Grid-side LCL inductance
- $R_g$  Grid-side LCL ESR
- C LCL Capacitor
- $R_c$  LCL Capacitor ESR
- $Z_{TL}$  Transmission line impedance
- $R_{TL}$  Transmission line resistance
- $L_{TL}$  Transmission line inductance

# Abbreviations and acronyms

DPG	Distributed Power Generation.
VSI	Voltage Source Inverter.
CSI	Current Source Inverter.
APF	Active Power Filter.
PCC	Point of Common Coupling.
PWM	Pulse-Width Modulation.
THD	Total Harmonic Distortion.
$\mathbf{FLL}$	Frequency Locked Loop.
$\mathbf{PLL}$	Phase Locked Loop.
ATO	Angle Tracking Observer.
$\mathbf{QSG}$	Quadrature Signal Generator.
$\mathbf{SRF}$	Synchronous Reference Frame.
PFS	Pre Filter Stage.
PDC	Phase Delay Compensator.
$\mathbf{FoL}$	Filter on the Loop.
ANF	Adaptive Notch Filter.
MAF	Moving Average Filter.
SOLC	Second Order Lead Compensator.
$\mathbf{NDZ}$	Non-detection Zone.
AFD	Active Frequency Drift.
$\mathbf{SMS}$	Slip Mode frequency Shift.
SFS	Sandia Frequency Shift.
$\mathbf{SVS}$	Sandia Voltage Shift.
PLC	Power Line Communications.
$\mathbf{AC}$	Alternating Current.
$\mathbf{DC}$	Direct Current.
DSP	Digital Signal Processor.
VCO	Voltage Controlled Oscillator.
PD	Phase Detector.
$\mathbf{LF}$	Loop Filter.

PI	Proportional Integral (controller).
RES	Resonant (controller).
IEEE	Institute of Electrical and Electronics Engineers.
$\mathbf{FIR}$	Finite Impulse Response (filter).
IIR	Infinite Impulse Response (filter).
$\mathbf{IGBT}$	Insulated-Gate Bipolar Transistor.
MSE	Mean Squared Error.
$\mathbf{RCF}$	Real Coefficient Filter.
$\mathbf{CCF}$	Complex Coefficient Filter.
$\mathbf{BSF}$	Band Stop Filter.
$\mathbf{FS}$	Filtering Stage.
$\mathbf{ESR}$	Equivalent Series Resistance.
DDSRF	Double Decoupled Synchronous Reference Frame.
DSOGI	Dual Second Order Generalized Integrator.
MCCF	Multiple Complex Coefficient Filter.
$\mathbf{CCCF}$	Cascade of Complex Coefficient Filter.
NFOL	Notched Filter On the Loop.
FOAP	First Order All Pass.

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## Chapter 1

# Introduction

#### 1.1 Background on microgrids and smart grids

Traditionally, electricity generation was performed in large centralized power plants, the use of small or medium size generation units being restricted to remote areas with a marginal or without an adequate access to the primary grid busbar. These small generation spots where usually isolated from the main grid, feeding a group of loads or customers.

Centralized generation is a mature technology with good economies of scale, coal, gas, oil, nuclear and hydropower being the primary resources. However, energy needs to be routed through long distances, what increases the transmission losses, and consequently the emissions.

In recent years, due to the unstoppable increased electricity demand, natural resources decrease and environmental concerns, distributed power generation (DPG) has grown steadily. Actually only a small part of worldwide energy is generated by DPG, which includes both renewable (wind, solar, etc...) as well as non-renewable (fuel cells, micro gas turbines, etc...) energy resources, meaning that, globally speaking, the new paradigm is at an early stage. Although DPG is usually related to small or medium size power plants, it is expected that in the medium term each home-user can become an autonomous entity, with the capability not only of demanding but also of injecting power into the grid, which is commonly known as micro-generation.

Benefits of DPG include reduction of size, number and level of saturation of transmission lines as well as reduction of the transmission losses. Massive utilization of DPG places however several challenges regarding stability and



Figure 1.1: Microgrid architecture

dispatchability issues, due to the variability of renewable energy resources and the absence of a proper market design.

A very extended and suitable way to insert the DPGs into the actual electrical system is throughout microgrids. This concept was first defined as a system with renewable and no-renewable energy resources, including loads, energy storage and heat to a local area. An example of generic microgrid architecture is shown in Fig. 1.1. It typically consists of non-renewable generation units, i.e. diesel generation, renewable generation units, i.e. wind turbines or photovoltaic (PV) systems, storage systems, i.e batteries, and heating devices providing heat and domestic hot water to a customer of group of customers. Each unit, e.g. diesel, storage units, wind turbines or PV systems can be connected or disconnected by using a power switch. Also the whole microgrig can be connected or disconnected from the main grid by a power switch. The development of power electronics has boosted the implantation of DPG based on microgrids. A large variety of power converter topologies can be used, the two-level voltage source inverter (VSI) being the most popular choice in practice.

During the last decade, significant attention has been paid to enhance the actual energy generation and distribution scenario: development of lowlosses, high voltage/current power modules, modulation techniques with reduced harmonic content, enhanced algorithms for current, voltage and power regulation, islanding detection, synchronization, power quality improvement .... Furthermore, challenges for the future include optimal sizing of the microgrid, with energy storage sizing playing an major role; implementation of intelligent energy routing devices, allowing to optimize the energy routing depending on factors like congestion, demand or economic constraints; and the massive implantation of clean generation units in order to reduce the overall emissions.

#### **1.2** Objectives and thesis motivation

This thesis focuses on synchronization, islanding detection and power quality improvements of microgrids. A deep review of the state of the art of each technology will be done, highlighting strengths and weaknesses of the existing methods. From this analysis, novel techniques that overcome the limitations of previously published methods will be proposed.

The motivation for the development of novel synchronization methods arises from the fact that the grid voltage is nowadays more polluted. E.g. distributed power generation units using power electronics and non-linear loads increase the grid harmonic content; single-phase loads usually induce unbalances among phases, .... Most of the previously published single and three phase synchronization methods do not implement mechanisms to deal with grid disturbances, or have limitations in their response. Developing of more robust and reliable methods is therefore required.

Synchronization and physical connection of a DPG to a distorted network using only the fundamental PCC voltage could induce large overcurrents due to the voltage mismatch between the circuit breaker terminals, which could damage microgrid equipment or produce breakdowns. The method for synchronization of DPG units to a distorted network proposed in this thesis overcomes this problem.

The connection of microgrids to the utility grid is required to meet standards normally regulated either by the country (local) authorities or by standardizing institutions as IEEE and IEC. Among other requirements, the microgrid is required to have the ability to detect if it is connected or disconnected to the utility grid, which is normally referred as islanding detection. Islanding detection standards establish the minimum requirements for islanding detection methods. However, the faster the islanding situation is detected, the faster the control algorithms of all microgrid's DPGs can be adapted to the new situation, which is beneficial in terms of microgrid stability. A critical aspect of islanding detection methods is the so call non detection zone (NDZ), i.e. the uncertainty region in which a particular islanding detection technique cannot precisely detect the islanding condition. Development of faster islanding detection methods, with reduced or even zero NDZ, is therefore a topic of great interest. This thesis will propose various islanding detection methods that will overcome some of the limitations of the existing methods.

Another important issue regarding to the DPG implantation is the power quality, complying with grid codes [11]-[68]. In order to increase the power quality, several strategies can be found in the literature to compensate the PCC harmonics, the virtual impedance concept being widely used for this purpose. The drawback of the virtual impedance concept is that it can only be applied to voltage source inverters (VSIs) working in voltage control mode. However, a large number of VSIs working in current control model typically exists in a microgrid. This thesis proposes a method for harmonic compensation between several microgrid VSIs working in current control mode. The proposed method is based on the virtual admittance concept, which can be applied to VSIs working both in voltage and current control mode, therefore the limitations of the virtual impedance concept are removed.

#### **1.3** Outline of the Document

This thesis is organized in six Chapters.

- Chapter 2 introduces VSIs power converters topologies, both for single and three-phase systems. PWM methods, filtering stages and VSIs control strategies are analyzed.
- Chapter 3 analyzes single and three-phase synchronization techniques. A review of synchronization techniques state of the art will be presented

first. Three novel grid synchronization techniques, two for three-phase systems and one for single-phase systems, will be proposed.

- Chapter 4 introduces and analyzes islanding detection techniques. Following the same structure as Chapter 3, a full analysis of the existing techniques is provided firstly, new active islanding detection methods being proposed later.
- Chapter 5 focuses on microgrid power quality issues. Review of harmonic compensation techniques is presented first. A method for harmonic compensation based on the virtual admittance concept is then proposed. A grid connection strategy for distorted networks is finally presented.
- Chapter 6 summarizes the contributions of this thesis and outlines future research lines.

### Chapter 2

# Voltage source inverters: topologies and control

### 2.1 Introduction

This chapter briefly discusses single and three-phase PWM power converter topologies commonly used in in DPG units, as well as modulation and control strategies. Single and three-phase PWM power converter topologies will be analyzed. The basis of the current, voltage and power DPG control strategies will be analyzed too.

### 2.2 Power converters for distributed generation

Most of the actual DPG units are connected to the utility grid/microgrid through electronic power converters. DC/AC power converters are used whenever the primary power source is DC, e.g. PV panels, batteries, etc. On the contrary, if the primary power source is AC (e.g. wind turbine), the AC power is commonly converted to DC first by either a controlled or uncontrolled AC/DC power converter (rectifier), and later converted to AC to connect with the grid.

Generally speaking, DC/AC power converters topologies can be classified into Voltage Source Inverters (VSIs) and Current Source Inverters (CSIs), VSIs being more widely used. Consequently, all the discussion presented in this thesis is based on VSIs.



Figure 2.1: Single-phase half-bridge VSI

#### 2.2.1 Voltage source inverters (VSIs)

VSI converts a DC voltage into an AC voltage. VSIs used in microgrids can be either single phase and three phase.

#### 2.2.1.1 Single-phase half-bridge VSI

Fig. 2.1 shows a single-phase, half-bridge, two level VSI. It is composed by an upper (S1) and a lower (S2) power switches. Antiparalell diodes allow bidirectional power flow. Two capacitors are used to create a neutral point, each capacitor supporting half of the DC bus voltage under balanced conditions. The voltage applied to the load can be made positive or negative.

#### 2.2.1.2 Single-phase full-bridge VSI

Fig. 2.2 shows a single-phase, two level full-bridge VSI. It is composed by two half-bridge legs which are connected in parallel. The voltage applied to the load can be positive, negative or zero.

#### 2.2.1.3 Three-phase full-bridge VSI

A three-phase full-bridge two level VSI is shown in Fig. 2.3. It consists of three half-bridge legs connected in parallel.



Figure 2.2: Single-phase full-bridge VSI



Figure 2.3: Three-phase full-bridge VSI



Figure 2.4: PWM schematic diagram



Figure 2.5: Fourier series definition of the inverter output voltage

#### 2.2.2 Basis of pulse-width modulation (PWM)

The gate signals both for single-phase and three-phase inverters are commonly generated using PWM methods. PWM methods are aimed to produce the desired fundamental voltage at the power converter output, with reduced harmonic distortion and switching losses.

A simple way to produce the PWM signal is by comparing the reference waveform voltage with a symmetric triangular carrier waveform. Fig. 2.4 shows a general block diagram of the PWM generation module. The modulating signal m(t) is compared with the carrier signal c(t). The intersections between the modulating and carrier signals produce the gating signals for the corresponding phase, i.e. S1 and S2 (see Fig. 2.1).

Fig. 2.5 shows the spectrum of the output voltage waveform of a PWM-VSI. It is observed that, in addition to the desired fundamental voltage, a large number of switching harmonics are induced in the output voltage. A filtering stage including inductors is required to limit harmonic content of the current to reasonable limits. Those inductors serve also as boost inductors in the event that the VSI needs to operate as a controlled rectifier.



Figure 2.6: L filtering stage model

#### 2.3 Filtering topologies

Different types of filters can be found in VSIs, including L, LC and LCL. They are briefly discussed in this section.

#### 2.3.1 L Filter

Inductive filters are the simplest filter design. A simplified equivalent circuit is shown in Fig. 2.6. Though not shown in the figure, an equivalent series resistance exist. The output current vs. input voltage transfer function is given by (2.1). Fig. 2.6 shows the L filter Bode plot (2.1) for different inductance values, a 20 dB/dec attenuation being observed.

It is observed from Fig. 2.6 that the higher the inductance is, the lower the filter bandwidth is. Therefore a good harmonic rejection capability will require a large inductance, which increases the filter size and cost.

$$i_o = \frac{u_{PCC} - u_i}{R_i + L_i s} \tag{2.1}$$

L filters are relatively ease to produce, but have limited filtering capabilities.

#### 2.3.2 LC Filter

To improve the L filter attenuation ratio, a capacitor can be added in parallel connected to the PCC (see Fig. 2.8). This increases the filter order.

The LC filter transfer function is given by (2.2), while the filter output current can be obtained from (2.3). It is observed that the filter output current depends both on the input and output voltages.



Figure 2.7: L filtering stage Bode plot as a for different values of L. An equivalent series resistance  $R_i = 10m\Omega$  has been used.



Figure 2.8: LC filtering stage model
$$\frac{u_{PCC}}{u_i} = \frac{Zc}{Zc + Zi} = \frac{CR_c s + 1}{CL_i R_i s^2 + CR_c s + 1}$$
(2.2)

$$i_{o} = u_{PCC} \frac{CL_{i}R_{i}s^{2} + L_{i}R_{c}R_{i}s - CR_{c}s - R_{c}^{2} - 1}{CL_{i}R_{c}R_{i}s^{2} + (L_{i}R_{i} + R_{c}^{2} + L_{i}R_{i})s} + u_{i} \frac{CR_{c}s + R_{c}^{2} + 1}{CL_{i}R_{c}R_{i}s^{2} + (L_{i}R_{i} + R_{c}^{2} + L_{i}R_{i})s}$$

$$(2.3)$$

Fig. 2.9 shows the LC filter Bode plot. As expected, the LC filter shows an attenuation ratio of 40 dB/dec, improving therefore the performance of the L filter. One of the drawbacks of the LC filter is that it shows a resonance peak, the resonance frequency  $f_r$  being (2.4). Selection of LC filters resonance frequency has been widely investigated. A popular criteria is to select the LC resonance between 1/3 and 1/2 of the switching frequency [95]. However, the LC filter resonant frequency also depends on the PCC impedance, which is usually unknown and can change during normal operation, being therefore an important drawback of this filter design. A number of active/passive damping strategies to mitigate or remove the effect of the filter resonance can be found in the literature [59], [105], [106], [107], [136] and [24].

$$f_r = \frac{1}{2\pi\sqrt{LC}}\tag{2.4}$$

## 2.3.3 LCL Filter

LCL filters (see Fig. 2.10) overcome some of the limitations of the LC filter. One advantage of LCL filters are that they reduce the sensitivity to the grid impedance. In addition LCL filters increase the filter attenuation, therefore reducing the filter cost and weight.

The LCL filter transfer function is 2.5, its Bode plot being shown in Fig. 2.11. The LCL attenuation is 60 dB/dec, which results from the series connection of an L filter and an LC filter. As for the LC case, the LCL filter has a resonant peak, the resonance frequency,  $f_r$  being 2.7, a number of strategies to damp this resonance can be found in the literature.

$$\frac{u_{PCC}}{u_i} = \frac{Zc}{Zc + Zi} \frac{1}{Z_g} = \frac{F}{As^3 + Bs^2 + Ds + E}$$
(2.5)



Figure 2.9: LC filtering stage Bode plot



Figure 2.10: LCL filtering stage model



Figure 2.11: LCL filtering stage Bode plot

$$A = CL_gL_i$$
  

$$B = CL_gR_c + CL_gR_i + CL_iR_g + L_gL_iR_c$$
  

$$D = CR_cR_g + CR_gR_i + L_gR_c^2 + L_gR_cR_i + L_iR_cR_g + Lg$$
  

$$E = R_c^2R_g + R_cR_gR_i + R_g$$
  

$$F = CR_cs + R_c^2 + 1$$
(2.6)

$$f_r = \frac{1}{2\pi} \sqrt{\frac{L_i + L_g}{L_i L_g + C}} \tag{2.7}$$

A extended rule of thumb to select the LCL resonance frequency (2.7) is to choose it to be between ten times the fundamental frequency component and one tenth of the switching frequency.



Figure 2.12: Clarke transformation

# 2.4 Complex vector notation and reference frames

A three-phase voltage system can be represented in an  $\alpha\beta$  stationary reference frame (2.8) by using the Clarke transformation (2.9).

$$\vec{u} = u_{\alpha} + ju_{\beta} \tag{2.8}$$

$$\begin{pmatrix} u_{\alpha} \\ u_{\beta} \end{pmatrix} = \begin{bmatrix} T_{\alpha\beta} \end{bmatrix} \begin{pmatrix} U_a \\ U_b \\ U_c \end{pmatrix} = \frac{2}{3} \begin{pmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} U_a \\ U_b \\ U_c \end{pmatrix}$$
(2.9)

Assumed that the three phase voltages are a set of sinusoidal, balanced three-phase system, the resulting components in the stationary reference frame  $(\alpha\beta)$  will have the same magnitude and frequency. As shown in Fig. 2.12, the  $\alpha$  component is aligned with phase a, the  $\beta$  component being shifted by 90 degrees from the  $\alpha$  component (see (2.8)).

Variables in the  $\alpha\beta$  stationary reference frame can be transformed to a rotating dq reference frame using (2.10), Fig. 2.13.

Being  $\omega_0$  the fundamental frequency of  $\vec{u}_{\alpha\beta}$ , by selecting  $\theta = \omega_0 t$ , the resulting dq reference frame will rotate synchronously with the fundamental excitation. The resulting transformation is commonly known as Park



Figure 2.13: Park transformation

transformation. The most relevant effect of the Park transformation is that variables which are sinusoidal in the stationary reference frame, become DC when transformed to the synchronous reference frame.

$$\begin{pmatrix} u_d \\ u_q \end{pmatrix} = \begin{bmatrix} T_{dq} \end{bmatrix} \begin{pmatrix} u_\alpha \\ u_\beta \end{pmatrix} = \frac{2}{3} \begin{pmatrix} \cos(\theta^*) & \sin(\theta^*) \\ -\sin(\theta^*) & \cos(\theta^*) \end{pmatrix} \begin{pmatrix} u_\alpha \\ u_\beta \end{pmatrix}$$
(2.10)

# 2.5 VSI control

This section introduces the basics of VSIs control. Current, voltage, power and harmonic control modes will be considered. All control strategies will be analyzed in a dq reference frame synchronous with the fundamental excitation.

Fig. 2.14 shows the schematic diagram of a three-phase, full-bridge twolevel VSI (see 2.2.1.3), feeding an LCL filter (see 2.3.3), where  $i_i$  is the the inverter-side current,  $u_{\mu g}$  is the output filter voltage and  $i_g$  is the grid-side current.

Fig. 2.15 shows the control block diagram of a VSI. Typically consists of an inner current control loop used to control the inverter output current  $i_i$ , and an outer voltage control loop for output filter voltage control,  $u_{\mu g}$ . The power control loop is not represented in Fig. 2.15, it can be cascaded both to the voltage or current loop, depending on the implementation being used.

## 2.5.1 Current control

VSI operated in a current controlled mode (VSI-CCM), typically controls the inverter output current,  $i_i$ , see Fig. 2.14. Alternatively, the grid-side



Figure 2.14: Three-phase VSI feeding an LCL filter



Figure 2.15: VSI voltage control block diagram

current, i.e. output filter current, could be controlled. However, since  $i_i$  is not directly controlled in this case, transient overcurrents at the inverter output can occur, which could damage the power switches.

Synchronous PI regulator (2.11) are normally used to control the current, the output of the PI regulator  $u_{dq\ cmd}^*$  being the inverter voltage command. The synchronous PI current regulator guarantees zero steady state error for the fundamental component of the current.  $K_p$  and  $K_i$  are the proportional and integral gains of the synchronous PI current regulator (2.11)

$$PI(s) = K_p + \frac{K_i}{s} \tag{2.11}$$

## 2.5.2 Voltage control

VSI voltage control mode (VSI-VCM) is used to control the output filter voltage,  $u_{dq \ \mu g}$  (see Fig. 2.14). The VSI-VCM block diagram is shown in 2.15 where  $u^*_{dq \ \mu g}$  is the voltage reference,  $u_{dq \ \mu g}$  is the filter output voltage, and  $i^*_{dq \ i}$  is the output of the *PI* voltage regulator, which is the command to the current regulator. As for the current regulator, the synchronous PI voltage regulator provides zero steady state error for the fundamental component of the voltage.

#### 2.5.3 Power control

The power control mode (VSI-PCM) in VSIs is used to control the active and reactive power delivered by the VSI to the grid. The active and reactive power is calculated from the filter output voltage  $u_{dq \mu g}$  and current  $i_{dq g}$  (see Fig. 2.14).

The grid current can be measured or estimated from the inverter output current and output filter voltage. The inverter instantaneous active power P and reactive power Q are obtained as (2.12).

$$P = u_{\mu g \ d} \cdot i_{g \ d} + u_{\mu g \ q} \cdot i_{g \ q}$$

$$Q = u_{\mu g \ q} \cdot i_{g \ d} - u_{\mu g \ d} \cdot i_{g \ q}$$

$$(2.12)$$



Figure 2.16: VSI power control feeding the voltage loop



Figure 2.17: VSI power control feeding the current loop

# 2.5.4 Harmonic control

Some control techniques used for synchronization or harmonic compensation purposes require PCC voltage harmonics control. Typically harmonic  $-1^{st}$  are due to unbalances among phases while harmonics  $-5^{th}$ ,  $7^{th}$ ,  $-9^{th}$ ,  $11^{th}$ , etc are due to nonlinear loads.

When a complex vector (voltage or current) in the stationary reference frame is transformed to a reference frame synchronous with the fundamental excitation, each harmonic of order  $n \mbox{ in } \alpha\beta$  (Fig. 2.18(a)) produces a harmonic of order (n-1) (Fig. 2.18(b)). I.e. the  $-5^{th}$  and the  $7^{rd}$  harmonics in the stationary reference frame produces two harmonics,  $-6^{th}$  and  $6^{rd}$ , in a reference frame synchronous with the fundamental excitation.

Control of symmetric harmonics can be realized using resonant (RES) controllers. Alternatively to the use of RES controllers, harmonic components could be also controlled in a dqn reference frame synchronous with the harmonic frequency by using synchronous PI regulators. However, one controller per harmonic is needed in this case, the implementation being therefore more difficult.

Fig. 2.19 shows the modified voltage and current control loops to control both the fundamental and harmonic components, where  $RES_n(s)$  is a



(a) PCC harmonics in  $\alpha\beta$  stationary reference frame



(b) PCC harmonics in dq synchronous reference frame

Figure 2.18: Harmonics in stationary or synchronous reference frames

resonant controller of order n, (2.14). A PI resonant controller (PI - RES (2.13), Fig. 2.19), is used to control both the fundamental component and harmonic components of the inverter output voltage/current, where  $K_{p RES_n}$  is the proportional gain of the resonant controller (2.14),  $\omega_0$  is the fundamental frequency and n is the harmonic order. The PI controller (2.11), as previously explained, controls the fundamental voltage/current component, while each RES controller of order n, (2.14), controls two harmonic components, i.e. positive and negative sequence components.

$$PI - RES(s) = PI(s) + RES(s)$$
(2.13)

$$RES_n(s) = \frac{K_{p RES_n} s^2 + 2K_{p RES_n} Cs + (n\omega_0)^2 + C^2}{s^2 + (n\omega_0)^2}$$
(2.14)

# 2.6 Conclusions

This chapter has briefly discussed the VSI power converters topologies and filters commonly used in DPG units.



Figure 2.19: VSI PI - RES control block diagram

Three filtering topologies, L, LC and LCL, have been analyzed. The L filter requires a higher inductance value to provide good harmonic rejection meanwhile the LCL filter shows better harmonic rejection capability. However, they show a resonant behavior, which needs to be considered.

Finally, current, voltage, power and harmonic control strategies have been reviewed.

# Chapter 3

# Synchronization

# **3.1** Introduction

Distributed energy resources are typically connected to the utility grid or microgrid through electronic power converters. Estimating the magnitude and phase of the point of common coupling (PCC) positive sequence voltage component (fundamental component) is of paramount importance to guarantee stable operation and precisely control the active and reactive power injected by the power converter. Also obtaining a clean and accurate estimation helps to implement robust control strategies for islanding detection, harmonic compensation or power dispatching.

During grid-connected operation, power quality (harmonics and unbalances), islanding detection, frequency shifts and maximum magnitude deviation regulations must be fulfilled [], precise measurement of the fundamental voltage phase angle and magnitude being needed for this purpose. However, harmonics typically due to high non-linear loads, unbalances or power transients, produce a distortion of the PCC voltage. Development of synchronization methods able to work in high-distorted grids being therefore needed in this case.

The fact that practically all electronic power converters used in microgrids use some type of digital signal processor (DSP) for its control, has boosted the development of digital synchronization techniques, e.g. digital frequency locked loop (FLL) and digital phase locked loop (PLL) techniques. PLL based methods are the most popular choice due to their simplicity, robustness and ability to implement different filtering stages.

This chapter will give a full review of single and three-phase synchroniza-

tion techniques. Also, three novel methods will be proposed: three-phase pre-filter stage CCCF-CPLL, three-phase filter on the loop stage NFOL-CPLL and single-phase FOAP-CPLL synchronization methods. The design, tuning and stability of the existing and proposed methods will be discussed.

# **3.2** Synchronization methods: an overview

Synchronization methods obtain the frequency, phase and sometimes the magnitude of an input signal. Synchronization of the power converter with the main grid is one of the key issues for the inverter control. As previously mentioned, the power converter can work islanded, i.e. isolated from the grid, or grid connected. If the inverter is not accurately synchronized with the grid voltage phase and magnitude previous to its connection to the grid, undesirable overcurrents may be induced when the physical connection between the power converter and the grid occurs, which can damage the equipment or produce unwanted operating breakdowns. If the inverter is grid connected, errors estimating the PCC magnitude, frequency and phase may produce noticeable power mismatches, affecting to the overall system stability.

Synchronization is needed both in single and three-phase systems. In both cases, synchronization techniques can be open-loop or closed-loop. Open-loop methods are based on the detection of the grid voltage zero crossing after applying a filtering stage to the grid voltage. Closed-loop methods are based on locking one characteristic of the input signal, e.g. the frequency or phase. Typical examples of closed-loop methods are the conventional single phase PLL and the synchronous reference frame PLL (SRF-PLL), which have been widely used in three-phase applications. Closed-loop methods are highly reliable even under high distorted conditions. Existing synchronization methods both for the case of single phase and three phase systems are discussed following.

# 3.3 Single-phase synchronization methods

This section reviews the most relevant single-phase synchronization methods. They can be roughly divided into methods that implement a dedicated single-phase synchronization method or methods that emulate a three-phase balanced system over a single-phase signal. They are discussed following.



Figure 3.1: Narrow Pulse Zero Crossing Detector

# 3.3.1 The zero-crossing method

The most intuitive way to extract the grid frequency is by detection of zero crossing of the grid voltage, namely zero crossing methods (ZCM). Changes in the polarity of the grid voltage are detected by comparators. The ZCM was originally developed using analog implementations [46], digital implementations were also been proposed later [134].

Two main ZCM approaches have been proposed: producing a narrow pulse when zero crossings are detected, Fig. 3.1, or a square wave signal in phase with the input signal, Fig. 3.2. The number of zero crossings are counted to estimate the input signal frequency. The grid phase angle is estimated by integrating the grid frequency, without any phase controller.

The dynamic performance of the ZCM is relatively poor, i.e. the frequency can only be estimated each half cycle of the grid voltage, meaning that the phase between the zero crossings needs to be interpolated. Moreover, the frequency is assumed to be constant during at least one half cycle, which is not always true. Another significant drawback is that fake zero crossings can be detected under harmonic conditions. To improve these limitations, modified ZCD have been proposed [134]. However, this is at the prize of increasing the complexity of the system, while still showing poor performance when the grid voltage includes low-frequency harmonics or frequency deviations from the rated value.



Figure 3.2: Square Wave Zero Crossing Detector

# 3.3.2 Single-phase frequency locked loop (FLL) method

FLL closed-loop synchronization techniques are aimed to lock the frequency of its input signal. The FLL block diagram is shown in Fig 3.3, it consists of the following blocks:

- 1. Frequency detector (FD). It is used to obtain an output signal that  $\overline{\text{depends on the frequency}}$  difference between the two input signals, v and  $\hat{v}$ . This output signal is composed by a DC component that reflects the frequency error  $\epsilon_f$  and a set of unwanted AC terms whose frequency is at integer multiples of the fundamental frequency.
- 2. Loop Filter (LF). This block is used to remove the unwanted AC components induced by the FD. It usually behaves as a low-pass filter thanks to the proportional integral (PI) controller 2.11, a first-order low-pass filter can also be used. The output signal of the LF is the estimated frequency f, of the input signal v
- 3. Voltage Controlled Oscillator(VCO). The VCO output is a sinusoidal  $\overline{\text{signal whose frequency} f}$  is proportional to the magnitude of the DC component of the input signal.

FLL methods change the VCO frequency accordingly to the frequency difference of its inputs (v and  $\hat{v}$ ). FLLs guarantee perfect estimation of the



Figure 3.3: Schematic representation of a generic FLL method



Figure 3.4: Schematic representation of a generic PLL method

input signal frequency in steady state (locked condition). However, FLL methods do not guarantee that the input and output signals are in phase, which can produce large overcurrents during the synchronization process, as well as errors controlling the active and reactive power flows in grid connected mode.

## 3.3.3 Single-phase phase locked Loop (PLL) method

PLL are closed-loop methods that shares some similarities with the FLLs. However, PLLs are aimed to lock the phase, providing zero error in the estimated phase in steady state. The PLL block diagram is shown in Figure 3.4. It is composed by a phase detector (PD) unit, a loop filter (LF) and a voltage controlled oscillator (VCO). The PD unit feeds the LF with a signal that depends on the phase difference between the input signal v and the estimated output signal  $\hat{v}$ . The LF ouput obtains the estimated frequency, f, from the phase error. The estimated output signal is finally obtained by feeding the VCO with f.

The estimated frequency is obtained as the output of the LF, f. This block is usually pre-charged with the grid rated frequency in order to improve the dynamic performance whenever the PLL is reset. Once the phase (and



Figure 3.5: Schematic representation of a PLL based on a multiplier phase detector (LPLL)

thus the frequency) of the output signal is locked with the input voltage, then the phase error between the input and output signals,  $\epsilon_{\theta}$  is driven to zero, the PLL therefore providing perfect estimations of both frequency and phase of the input signal.

Several phase detectors implementations can be found in the literature. It can be easily implemented by using a multiplier, see Fig. 3.5. A linear PLL (LPLL) is defined as a synchronization method that uses the multiplier phase detector, a PI controller, and an integrator and a cosine function as VCO.

Moreover, a group of phase detectors based on hardware elements like EXOR gates, JK flipflops or phase-frequency detectors have been historically implemented into high frequency analog communication systems. All of these PLLs can be also digitally implemented in existing microcontrollers.

When an input voltage v(t) of the form given by (3.1) feeds a basic LPLL, Fig. 3.5, the estimated output signal can be expressed by (3.2). The phase error (3.4), which is obtained by multiplying v(t) by (3.1) is composed by two components: a low frequency component, whose frequency is  $(\omega_v - \hat{\omega}_v)$ , and which contains the phase difference between v and  $\hat{v}$  and a high frequency component whose frequency is  $(\omega_v + \hat{\omega}_v)$  and which does not contain information of interest.

A method to remove the high frequency component and obtain a clean estimation of the frequency is therefore required, i.e. PI in Fig. 3.4. Once the high frequency component is removed (3.5) and the frequency of the estimated signal is close to the frequency of the of the input signal ( $(\omega_v - \hat{\omega}_v) \approx 0$ ), then the LPLL phase error signal can be safely assumed to be (3.6). It is observed that the phase error signal is affected by the magnitude of the input signal, some type of normalization to avoid this dependency being advisable.

$$v(t) = U\sin\left(\omega_v t + \theta_v\right) \tag{3.1}$$

$$\hat{v}(t) = \cos\left(\hat{\omega_v}t + \hat{\theta_v}\right) \tag{3.2}$$

$$\epsilon_{\theta} = v(t) \cdot \hat{v}(t) = U \sin\left(\omega_v t + \theta_v\right) \cos\left(\hat{\omega_v} t + \hat{\theta_v}\right)$$
(3.3)

$$\epsilon_{\theta} = \frac{U_1}{2} \left[ \sin \left( \left( \omega_v - \hat{\omega_v} \right) t + \left( \theta_v - \hat{\theta_v} \right) \right) + \sin \left( \left( \omega_v + \hat{\omega_v} \right) t + \left( \theta_v + \hat{\theta_v} \right) \right) \right]$$
(3.4)

$$\epsilon_{\theta} = \frac{U_1}{2} \left[ \sin \left( \left( \omega_v - \hat{\omega_v} \right) t + \left( \theta_v - \hat{\theta_v} \right) \right) \right]$$
(3.5)

$$\epsilon_{\theta} = \frac{U_1}{2} \left[ \left( \theta_v - \hat{\theta_v} \right) \right] \tag{3.6}$$

The LPLL method uses a PI controller to adapt the estimated frequency. The frequency estimation  $\hat{\omega}_v$  is the sum of the controller output,  $\omega$ , and the rated grid frequency  $\omega_r$ . Finally, the estimated angle  $\hat{\theta}_v$  is obtained by simple integration of the estimated frequency, which is feedback to the PD unit to close the loop.

Fig. 3.6 shows the LPLL linearized model, where  $K_n$  is used to make the phase difference independent of the input magnitude,  $K_n = \frac{2}{U_1}$ .

#### 3.3.3.1 The enhanced PLL (EPLL)

The enhanced EPLL, see Fig. 3.7, is a single-phase synchronization method similar to the linear PLL (Fig. 3.5) through a modification of the multiplier phase detector (PD). The EPLL uses an adaptive notch filter (ANF) to feed the LPLL. The  $v_{ANF}$  signal is subtracted from the input signal v to produce output of the ANF, v', that becomes zero when  $v_{ANF}$  has the same frequency and phase as the input signal, v. By doing this, disturbances at the multiplier PD output are removed, the fundamental component of the input signal phase  $\theta_v$  being extracted by using a conventional PI-based single-phase PLL.



Figure 3.6: LPLL Linearized model



Figure 3.7: EPLL block diagram



Figure 3.8: Three-phase PLL over a single-phase block diagram

#### 3.3.3.2 Use of three-phase PLLs with single-phase systems

Three-phase PLLs can be used with single-phase systems. A fictitious  $\alpha\beta$  stationary reference frame needs to be defined for this purpose, see Fig. 3.8. One approach is making the  $\alpha$  component equal to the phase voltage v, and the  $\beta$  component equal to zero [112]. However, this produces a mirror-frequency component that needs to be removed, a filtering stage or a decoupling network being commonly used for this purpose.

Alternatively, it is possible to avoid the mirror-frequency by making the  $\beta$  component,  $v_q$  (quadrature signal), equal to the  $\alpha$  component shifted by 90 degrees. The 90-deg block in Fig. 3.8 is commonly known as quadrature signal generator (QSG). The QSG is a crucial element for this solution, several QSG implementations that have been proposed in the literature are discussed following.

#### 3.3.3.2.1 Transport delay QSG

The transport delay QSG obtains the quadrature signal by using a firstin first-out (FIFO) buffer that delays the input signal a number of samples corresponding to one fourth of the fundamental component period (T/4).

Limitations of this method include an high sensitivity to frequency deviations, the need of a relatively large buffer and the absence of a methodology to deal with harmonic distortion.

#### 3.3.3.2.2 Hilbert transform QSG

It is possible to generate the quadrature component by using the Hilbert transform [22]. Being v(t) a real signal, its Hilbert transform is defined as (3.7).

$$v(t) = \frac{1}{\pi} \int_{-\infty}^{\infty} \frac{v(\tau)}{t - \tau} d\tau$$
(3.7)



Figure 3.9: Inverse Park QSG

The Hilbert QSG produces a phase delay of 90 degrees for each harmonic component. Unfortunately, the Hilbert transform QSG implies the use of a non-causal system, which obviously is not feasible. Hilbert QSG can be implemented either as Finite Impulse Response (FIR) or as Infinite Impulse Response (IIR) digital filters. IIR Hilbert QSG phase response is approximated in a range of frequencies while its magnitude response follows an all-pass behavior. Conversely, FIR Hilbert QSG performs a magnitude approximation in a given range of frequencies, its phase response being always maintained in all frequencies [131]. IIR Hilbert transformers can present instability and they are sensitive to the rounding in their coefficients; FIR filters stability is guaranteed. Due to this, and taking into account that FIR Hilbert realization shows a higher complexity instead to the corresponding IIR filter realization, FIR Hilbert QSGs are commonly found in practice [131].

## 3.3.3.2.3 Inverse-Park generation QSG

The inverse-park generation QSG (Fig. 3.9) uses the inverse Park transformation of an internally generated three-phase balanced system to obtain the quadrature signal  $v_q$ .

The input single-phase signal (v) is used as the  $\alpha$  component of the complex vector  $(u_{\alpha\beta})$  in the stationary reference frame feeding the Park transformation block. The corresponding complex vector in the synchronous reference frame  $u_{dq}$  is obtained after the Park transformation.

If  $v_{\alpha}$  and  $v_{\beta}$  are not perfectly in quadrature, the  $(u_{\alpha\beta})$  complex vector is composed both by a fundamental positive and a negative sequence components. Thus, the  $v_d^b$  and  $v_q^b$  signals being composed by a DC component and a harmonic component of twice the fundamental frequency. In order to mitigate the effect of the harmonic component,  $u_{dq}$  is filtered by using lowpass filters that feed to an inverse Park transformation block, the resulting  $\beta$  component being in quadrature respect to the input signal (v).



Figure 3.10: SOGI-QSG block diagram

The main advantage of the inverse-Park QSG is that it is relatively easy to implement, requiring the use of two low-pass filters, and a direct and an inverse Park transformation blocks. Conversely, the presence of two coupled nonlinear loops makes the three-phase PLL PI controller (Fig. 3.8) tunning and the low-pass filter tunning difficult.

## 3.3.3.2.4 Second order generalized integrator (SOGI-QSG)

In the SOGI-QSG, the quadrature component is generated by a block that acts as a variable-frequency band-pass filter, whose outputs are shifted by 90 degrees (see (3.8) and (3.9)). (3.8) shows the transfer function between the in-phase component u' and the input u while (3.9) is the transfer function linking the quadrature component qu' with input u. The DSOGI-QSG block diagram is shown in Fig. 3.10. As strong point, the SOGI-QSG include frequency-adaptive behavior while as a main drawback it shows a smooth harmonic rejection characteristic.

$$D(s) = \frac{u'}{u} = \frac{k\omega's}{s^2 + k\omega's + {\omega'}^2}$$
(3.8)

$$Q(s) = \frac{qu'}{u} = \frac{k\omega'^2}{s^2 + k\omega's + \omega'^2}$$

$$(3.9)$$

Fig. 3.11 shows D(s) and Q(s) SOGI-QSG bode plots; it can be observed that the magnitude of the component at the grid rated frequency (50 Hz) remains unchanged, the u' component being in phase with the input signal, u, (Fig. 3.11(a)), the qu' component lagging 90 degrees behind u' (Fig. 3.11(b)). The band-pass filtering characteristic of the SOGI-QSG are controlled by adequate selection of gain k, the lower k is, the narrower is the band-pass filter and the longer stabilization time is as well A critically-damped response is achieved when  $k = \sqrt{2}$ .

Drawbacks of the SOGI-QSG are that it is sensitive to DC offsets on the input signal. Such DC offsets can be produced e.g. by the voltage sensors. It was shown in [42], that DC offsets produce an oscillation at the grid frequency in the estimated frequency and phase angle.

# 3.4 Three-phase synchronization methods

Distributed power generation units (DPGs) are commonly connected to a three-phase grid, especially high power DPGs. Consequently, three-phase synchronization methods have received intensive attention during the last decades. The most important three-phase synchronization methods are discussed in this section.

#### 3.4.0.3 Synchronous Reference Frame PLL

SRF-PLL, also known as dq-PLL, is one of the most used and wellknown three-phase synchronization methods. As explained in Chapter 2, a three phase voltage signal,  $U_{abc}$ , can be expressed as a complex vector either in the stationary (2.9) or synchronous reference frame (2.10) by using the Clarke/Park transformations.

Fig. 3.12 shows the SRF-PLL control block diagram. The Park transformation angle ( $\theta^*$ ) is estimated by controlling the *q*-axis voltage component to zero. In steady state and with ideal grid voltages, i.e. without harmonics and unbalances, the *d*-axis component equals the magnitude of the grid voltage  $U_1$  while  $\theta^*$  corresponds to its phase angle. Note that the error signal, i.e. the PI regulator input, depends on the input signal ( $U_1$ ) magnitude (3.12), some type of normalization being therefore advisable.

$$u_q = u_\alpha - \sin(\omega_i t + \theta^*) + u_\beta \cos(\omega_i t + \theta^*)$$
(3.10)

$$u_q = -U_1 \cos(\omega_0 t + \theta_0) \sin(\theta^*) + U_1 \sin(\omega_0 t + \theta_0) \cos(\theta^*)$$
(3.11)



Figure 3.11: SOGI-QSG function bode plots



Figure 3.12: SRF-PLL block diagram

$$u_q = U_1 \sin\left((\omega_0 - \hat{\omega}_i)t + (\theta_0 - \theta^*)\right)$$
(3.12)

$$u_q = U_1 \left( \theta_0 - \theta^* \right) \tag{3.13}$$

The SRF-PLL provides excellent performance under balanced conditions; however it suffers significant deterioration when the grid voltage is unbalanced or contains harmonic components.

The grid voltage complex vector when an unbalance and a harmonic component of order n is present, can be represented as (3.14). The *q*-axis component of the resulting complex vector, (3.16), which is the input of the PI controller, is seen to contain a component at twice the fundamental frequency due to the unbalance, and a harmonic component of order n-1. Both terms induce harmonic components at the same frequencies in the estimated grid voltage magnitude, frequency and phase.

One possible solution to mitigate the induced harmonics is to reduce the PI controller bandwidth. However, this is at the price of a degradation of the dynamic performance of the SRF-PLL, which is not acceptable solution in most of the cases. Alternatively, the induced harmonics could be filtered off by means of a filtering stage (e.g. pre-filter or filter on the loop stages). This will be discussed in further sections.

$$U_{\alpha\beta} = U_1 e^{j\omega_0 t + \theta_0} + U_{-1} e^{-j\omega_0 t + \theta_{-1}} + U_n e^{jn\omega_0 t + \theta_n}$$
(3.14)

$$u_{q} = U_{1} \sin\left((\omega_{0} - \hat{\omega}_{i})t + (\theta_{0} - \theta^{*})\right) + U_{-1} \sin\left((\omega_{0} + \omega_{i})t + (\theta_{-1} - \theta^{*})\right) + U_{n} \sin\left((-n\omega_{0} - \omega_{i})t + (\theta_{n} - \theta^{*})\right)$$

$$(3.15)$$



Figure 3.13: Complex PLL block diagram

$$u_{q} = U_{1} \sin(\theta_{0} - \theta^{*}) + U_{-1} \sin\left((2\omega_{0}i)t + (\theta_{-1} - \theta^{*})\right) + U_{n} \sin\left(\left((n-1)\omega_{0}\right)t + (\theta_{n} - \theta^{*})\right)$$
(3.16)

#### 3.4.0.4 Angle Tracking Observer (ATO)

The ATO, also known as  $\alpha\beta$ -PLL or complex-PLL, is commonly used three-phase PLL, its block diagram being shown in Fig. 3.13. The ATO approach is similar to the LPLL (see subsection 3.3.3), but extending the multiplier phase detector to three-phase complex vectors. The error signal  $\epsilon_{\theta}$ (3.17) is obtained as the vector cross-product between the input signal  $(u_{\alpha\beta})$ and the estimated unitary vector  $\bar{u}_{\alpha\beta} = e^{j\theta^*}$ , whose phase angle is the ATO phase angle estimation.

$$\epsilon_{\theta} = u_{\alpha\beta} \otimes \bar{u}_{\alpha\beta} = = real(u_{\alpha\beta}) \cdot \sin(\hat{\omega}_i t + \theta^*) - imag(u_{\alpha\beta}) \cdot \cos(\hat{\omega}_i t + \theta^*)$$
(3.17)

If (3.17) is expanded, (3.18)-(3.19) are obtained, the same phase error as for the SRF-PLL being obtained (3.12). Assuming  $(\hat{\omega}_i - \omega_0) \approx 0$ , the phase error can be expressed as (3.20). As for the SRF-PLL, the phase error depends of the input magnitude, normalization being therefore advisable.

$$\epsilon_{\theta} = U_1 \cos(\omega_0 t + \theta_0) \sin(\hat{\omega}_i t + \theta^*) - \sin(\omega_0 t + \theta_0) \cos(\hat{\omega}_i t + \theta^*) \quad (3.18)$$

$$\epsilon_{\theta} = U_1 \sin\left((\hat{\omega}_i - \omega_0)t + (\theta^* - \theta_0)\right)$$
(3.19)

$$\epsilon_{\theta} = U_1 \Big(\theta^* - \theta_0\Big) \tag{3.20}$$

As for the LPLL, the basic ATO uses a PI controller as loop filter. The PI transfer function is expressed by (2.11), its output (3.21) being added to the rated grid frequency  $\omega_r$  (e.g. 50 Hz), to produce the estimated grid frequency (3.22). The estimated phase,  $\theta^*$ , is obtained by the integration of the estimated frequency. The unit vector,  $\bar{u}_{\alpha\beta}$  is obtained from (3.24).

$$\hat{\omega} = \epsilon_{\theta} \left( K_p + \frac{K_i}{s} \right) \tag{3.21}$$

$$\hat{\omega}_i = \hat{\omega} + \omega_r \tag{3.22}$$

$$\theta^* = \frac{\omega_i}{s} \tag{3.23}$$

$$\bar{u}_{\alpha\beta} = \cos(\theta^*) + j \cdot \sin(\theta^*) \tag{3.24}$$

Similarly as the SRF-PLL, the ATO suffers significant deterioration under unbalanced and grid harmonic conditions. Assumed that the grid voltage feeding the ATO includes, in addition to the desired positive sequence voltage, a negative sequence voltage and a harmonic component of order n, (3.14), the resulting phase error is given by (3.26). Two harmonic components, located at twice and n-1 with respect to the fundamental frequency are induced. These harmonic components will show up in the estimated magnitude, frequency and phase (in a lesser degree due to the low-pass behavior of the phase integrator).

As for the SRF-PLLO, one possible solution to deal with these unwanted harmonic components is to reduce the PI controller bandwidth. However, this will reduce the ATO dynamic response. Alternatively, filtering stages can also be used for this purpose.

$$\epsilon_{\theta} = U_1 \sin\left((\hat{\omega}_i - \omega_0)t + (\theta^* - \theta_0)\right) + U_{-1} \sin\left((\hat{\omega}_i + \omega_0)t + (\theta^* - \theta_{-1})\right) + U_n \sin\left((\hat{\omega}_i - \omega_0)t + (\theta^* - \theta_n)\right)$$
(3.25)



Figure 3.14: Pre-filter stage block diagram

$$\epsilon_{\theta} = U_1 \sin(\theta^* - \theta_0) + U_{-1} \sin\left((2\omega_0 i)t + (\theta^* - \theta_{-1})\right) + U_n \sin\left(\left((n-1)\omega_0\right)t + (\theta^* - \theta_n)\right)$$

$$(3.26)$$

## **3.4.1** Pre-filter stage methods

Pre-filter stage (PFS) methods have been extensively used as mechanisms to remove specific disturbances as unbalances and harmonic components. Pre-filter stages (see Fig. 3.14), eliminate the disturbances before they reach the SRF-PLL or ATO.

A PFS can be typically implemented as a cascade of notch filters or by using a decoupling network. The following subsections describe different approaches for their implementation.

## 3.4.1.1 Double Decoupled Synchronous Reference Frame PLL (DDSRF-PLL)

DDSRF-PLL method decouples unbalances by using two reference frames rotating in the positive direction (positive sequence) and negative direction (negative sequence) respectively. DDSRF-PLL block diagram is shown in Fig. 3.15, where the  $abc/\alpha\beta$  block is the Clarke transformation and the  $\alpha\beta/dq$  blocks is the Park transformation.

The block diagram of the DSRF-PLL is shown in Fig. 3.16. A lowpass filter is used at each DSRF output since the amplitude of the twicefrequency oscillating term in each synchronous reference frame (both positive and negative) depends on the mean value of the cross-coupling term, see Fig. 3.15.

The DDSRF-PLL method includes a simple SRF-PLL that is fed by the estimated positive sequence component  $(U_{sdq^{+1}})$  (Fig. 3.15). The estimated



Figure 3.15: DSRF-PLL block diagram



Figure 3.16: DSRF-PLL block diagram and decoupling network



Figure 3.17: DSOGI-PLL block diagram

angle  $\theta^*$  is feedback to each DSRF block to make the decoupling process frequency adaptive.

The main drawback of the DDSRF method is that it does not provide a mechanism to deal with harmonics, its use being therefore not advisable in distorted networks .

# 3.4.1.2 Dual Second Order Generalized Integrator PLL (DSOGI-PLL)

Fig. 3.17 shows the DSOGI-PLL block diagram. A SOGI-QSG (subsection 3.3.3.2.4) is used to filter and obtain a 90 degree phase shifted signal for the  $\alpha$  and  $\beta$  voltage components. These signals are fed to a positive sequence calculator (PSC) based on the instantaneous symmetrical components method. The positive-sequence voltages,  $u_{\alpha\beta}$ , are fed to a SRF-PLL for magnitude, phase and frequency, estimation. The DSOGI-PLL is made frequency-adaptive by using the estimated frequency to feedback each SOGI-QSG.

The DSOGI-PLL uses a set of two second order generalized integrators (SOGI, 3.3.3.2.4) to obtain the in-phase and quadrature signals required by the PSC. The SOGI block diagram is shown in Fig. 3.10. The transfer functions of the SOGI are (3.8) and (3.9) respectively, where  $\omega'$  and k are the SOGI natural frequency and damping factor respectively.

An important characteristic of the SOGI-QSG is that qu' is always shifted 90 degrees with respect to u', independently of k and  $\omega'$ . This feature has boosted the interest in SOGI methods as a mean to generate the quadrature component for the PSC.

The magnitude and phase of the u' and qu' components may have errors with respect to u if the estimated frequency,  $\hat{\omega}_i$ , does not perfectly match the frequency of the input signal, u. The magnitude and phase of the PSC frequency response function are defined by 3.27 and 3.28 respectively. Fig. 3.18 shows the PSC corresponding Bode plot. A damping factor  $k = \sqrt{2}$ has been used, as recommended in [97]. The PSC acts as a band-pass filter for the positive sequence component (50 Hz) and as a notch filter for the negative sequence component (-50 Hz). Finally, the harmonic components are filtered off by the band-pass behavior of the SOGI-QSG.

$$|u_{\alpha\beta}(\omega)| = \frac{k\omega'}{2} \sqrt{\frac{(\omega+\omega')^2}{(k\omega\omega')^2 + (\omega^2 - \omega'^2)^2}}$$
(3.27)

$$\angle u_{\alpha\beta}(\omega) = sign(\omega) \tan\left(\frac{\omega^{\prime 2} - \omega^2}{k\omega\omega^{\prime}}\right) - \frac{\pi}{2}\left(1 - sign\left(\frac{\omega^2 + \omega\omega^{\prime}}{\omega^{\prime}}\right)\right) \quad (3.28)$$

#### 3.4.1.3 Multiple Complex Coefficient Filter PLL (MCCF-PLL)

MCCF-PLL method estimates the grid voltage harmonics in the stationary reference frame. These harmonics can then be eliminated from the measured grid voltage by means of a decoupling network, allowing a clean estimation of the positive sequence voltage component, which can be used to feed a simple SRF-PLL. The estimated frequency can be used to feedback each band-pass filter, making the filtering process frequency adaptive.

The MCCF-PLL block diagram is shown in Fig. 3.19. It uses a set of variable frequency band-pass complex coefficient filters (CCF in Fig. 3.19) to estimate each harmonic component. These harmonics are then substracted from the input signal. The CCF transfer function is shown in (3.29). At the same time, the band-pass real coefficient filter (BP-RCF) transfer function is shown in (3.30).

$$BP - CCF(s) = \frac{\omega_c}{s - j\omega_0 + \omega_c} \tag{3.29}$$



Figure 3.18: PSC bode plot



Figure 3.19: MCCF-PLL block diagram



Figure 3.20: CCF vs RCF Bode plots

$$BP - RCF(s) = \frac{\omega_o s}{s^2 - \omega_0 s + \omega_o}$$
(3.30)

Fig. 3.20 shows the frequency response function of a generic BP-CCF (blue color) and a BP-RCF (black color), whose central frequency has been set to 50Hz. It is observed that the BP-RCF shows identical behavior for positive and negative frequency components (i.e. is not able to distinguish both components), while the BP-CCF has the capability to isolate only the positive sequence component.

Each BP-CCF can be implemented using the structure shown in Fig. 3.21, where n is the harmonic order, which can be positive or negative, a BP-CCF being used for each component that needs to be decoupled.

# 3.4.2 Filter on the loop methods (FoL)

FoL synchronization methods remove the harmonic components by introducing a filtering stage in the closed loop of the SRF-PLL/ATO. The basic



Figure 3.21: CCF implementing structure



Figure 3.22: Filter on the loop block diagram

block diagram of a FoL and its linearized model are shown in Figs. 3.22 and 3.23 respectively. It is observed that the filtering stage, F(s), is placed before the PI controller of the SRF-PLL. The FoL can be implemented by using notch filters, second order lead compensators (SOLC) or moving average filters (MAF).

#### 3.4.2.1 Adaptive Notch Filter (ANF) FoL

The typical ANF FoL implementation [23] is shown in Fig. 3.24. It consists of a set of cascaded notch filters before the SRF-PLL PI controller.

The transfer function of a generic second order ANF can be expressed as (3.31), where  $\zeta$  sets the depth and the width of the filter and  $\Omega_h$  is the notch frequency. Fig. 3.25 shows the Bode diagram of a ANF tuned to reject a



Figure 3.23: Filter on the loop linearized model



Figure 3.24: ANF Filter on the loop block diagram

harmonic at twice the fundamental frequency  $(2\Omega_0)$ .

$$NF(s) = \frac{s^2 + \Omega_h^2}{s^2 + \zeta \cdot s + \Omega_h^2}; \Omega_h = n \cdot \Omega_o$$
(3.31)

The ANF FoL strategy shows an excellent behavior when the grid frequency does not change, the performance of the ANF depending in this case on its bandwidth and spectral separation with the grid frequency (wider notch filters allow greater frequency shifts). The ANF method can be easily made frequency adaptive by feeding back the estimated frequency, the resulting ANF-PLL block diagram being shown in Fig.3.26.

Regardless of its appealing properties, the ANFs induce delays in the feedback loop which, which combined with other system poles, may result in instabilities. This delay is observed in the phase behavior in Fig. 3.25. If ANFs delay is not adequately compensated, VSI control may become eventually unstable.



Figure 3.25: Notch Filter bode plot



Figure 3.26: Three-phase ANF-PLL block diagram



Figure 3.27: Lead-Lag Bode plot

# 3.4.2.2 Second Order Lead Compensator (SOLC) Filter on the Loop technique

SOLCs have been proposed to overcome the delay introduced by the notch filters of the ANF structure. SOLCs transfer function, L(s), can be written as 3.32, where  $\omega_h$  is the frequency of the harmonic to be rejected. Note that  $(\omega_h < \omega_p)$ .

$$L(s) = \frac{s^2 + \omega_h^2}{s^2 + \omega_p^2}$$
(3.32)

Fig. 3.27 shows the SOLC frequency response. It is shown that it has a notch peak at  $\omega_h = 2w_0$ , and a resonant peak at  $\omega_p = 6w_0$ . In contrast to the ANF, the SOLC does not introduce any delay at the other frequencies.

The SOLC replaces the ANF block in Fig. 3.26 to form a FoL synchronization method. Harmonic components can be rejected by using a set of cascaded SOLC as for the ANF case in Fig. 3.24.
#### 3.4.2.3 Moving Average Filters (MAF) Filter on the Loop technique

MAFs have been extensively used in electric power applications because of their excellent harmonic rejection capabilities [refs]. MAFs are linear-phase finite impulse response (FIR) filters that can act as ideal low-pass filters.

MAF can be expressed in continuous-time domain by 3.33, where v(t) in the input signal,  $\bar{v}(t)$  is the output signal and  $T_w$  is the window length applied to the input signal. The MAF transfer function is given by 3.34, with  $T_w$  being the time required to reach steady-state.

$$\bar{v}(t) = \frac{1}{T_w} \int_{-t+T_w}^t v(\tau) d\tau$$
(3.33)

$$MAF(s) = \frac{\bar{v}(t)}{v(t)} = \frac{1 - e^{-T_w s}}{T_w s}$$
(3.34)

$$|MAF(s)| = \frac{\sin\left(\omega T_w/2\right)}{\omega T_w/2} \tag{3.35}$$

$$\angle MAF(s) = -\omega T_w/2 \tag{3.36}$$

MAF frequency response function is given by 3.35 and 3.36 respectively, Fig. 3.28 showing the corresponding Bode diagram for  $T_w = 10^{-2}$ . MAF shows a 0 dB gain at DC and does not introduce any phase delay at this frequency. MAF also removes the frequency components of integer multiples of  $\frac{1}{T_w}$  (Hz).

The MAFs can be made frequency-adaptive, a detailed analysis can be found in [ref].

Advantages of using MAFs include easiness of implementation and reduced computational burden. However, making MAFs frequency-adaptive is not as easy as for the ANF or SOLC methods.



Figure 3.28: MAF Bode plot

# 3.5 Summary

This section has introduced the basis of the single and three-phase synchronization methods. An extended review of synchronization methods has been presented, including primitive open loop strategies and advanced close loop methodologies.

Potential limitations of reviewed synchronization methods include: resonances at frequencies near to the fundamental frequency, what can result in overshoots in those frequencies are excited, reduced harmonic rejection capability and increased sensitivity to unbalances in the grid voltages, what compromises their performance in polluted networks. Also some of these methods are not configurable to reject more than one harmonic components, or do not exhibit good response for some or all the disturbances that can occur in the grid, their performance not being therefore optimal in a general scenario.

In the following sections, a set of advanced single and three phase methods are proposed to overcome these drawbacks.



Figure 3.29: Schematic representation of the CCCF-CPLL method

# 3.6 Three-phase pre-filter stage CCCF-CPLL synchronization method

A previously stated, both SRF-PLL, 3.4.0.3, and ATO, 3.4.0.4, have been traditionally used in three-phase systems, their performance being poor under harmonic or unbalanced conditions, methods to deal with these unwanted effects being analyzed in 3.4.1 and 3.4.2.

A three-phase synchronization technique is proposed in this section. It will be shown that the proposed method improves some of the limitations of actual three-phase techniques: it shows maximum unitary gain at the fundamental component frequency, it is frequency-adaptive and it can remove unbalances and harmonic components by using a pre-filter stage based on complex coefficient filters (band-pass and band-stop). The filtering stage will allows to isolate and reject components taking into account its sequence (positive or negative). The proposed method is simple and intuitive, with good dynamic response, and robust against unbalances and/or distorted line voltages.

# 3.6.1 Proposed method: cascade of complex coefficient filter with complex PLL (CCCF-CPLL)

Fig. 3.29 shows the structure of the proposed method. It consists of two major blocks: a pre-filter stage and an ATO. The pre-filter stage isolates the positive sequence component of the line voltage vector, while the ATO stage obtains its frequency, which is later used to feedback the pre-filter stage, thus making the pre-filter stage filter adaptive. The design and operation of both stages is discussed following.



Figure 3.30: Frequency response function magnitude

# 3.6.2 Pre-filter stage design

In addition to the positive-sequence fundamental component, the voltage vector in actual distribution lines often includes a negative-sequence of the fundamental frequency (if unbalanced conditions) as well as high order harmonics multiples of the fundamental frequency. The goal of the pre-filter stage is to isolate the positive-sequence fundamental component from the overall complex voltage vector. This can be done either through filtering techniques or decoupling networks.

One disadvantage of the DSOGI and MCCF pre-filter stages is that although they provide unitary gain at the fundamental frequency, they exhibit a gain bigger than one at frequencies nearby, see Fig. 3.30(a), that can produce overshoots if those frequencies are excited during transients. At the same time, conventional pre-filter techniques apply identical, real coefficients filters (3.30), to the *d* and *q*-axis components (real coefficient filters are symmetric respect to the frequency axis). As a consequence, both positive and negative sequence components are equally rejected/isolated, as shown in Fig 3.30(b).

To overcome both problems, the use of cascaded complex-coefficient filters (CCF) is proposed in this thesis. It is noted that conceptually, a CCF can also be represented as a real coefficient filter with cross-coupling between the d and q-axes. Examples of first-order band-pass (BP-CCF) and band-stop (BS-CCF) complex-coefficient filters are shown in (3.37) and (3.38), their corresponding frequency response function and block diagram being shown in Fig. 3.31 and 3.32 respectively.

In the proposed method, a pre-filter stage consisting of a cascade of a BP-CCF (3.37) that feeds a cascade of n BS-CCFs (3.38) are used to isolate the positive-sequence fundamental component of the grid voltage.





(a) Frequency response function magnitude of a band-pass complex coefficient filter

(b) Frequency response function magnitude of a band-stop complex coefficient filter



(c) Phase response function magnitude of a band-pass complex coefficient filter



(d) Phase response function magnitude of a band-stop complex coefficient filter

Figure 3.31: Frequency response function magnitude (top) and phase (bottom) of BP-CCF and BS-CCF



Figure 3.32: Block diagram of a first order BP-CCF and BS-CCF using complex vector notation

$$BP - CCF(s) = \frac{\omega_{bw\_bp}}{s - jn\omega_0 + \omega_{bw\_bp}}$$
(3.37)

$$BS - CCF(s) = \frac{s - jn\omega_0}{s - jn\omega_0 + \omega_{bw\_bs}}$$
(3.38)

Fig. 3.33 shows the overall pre-filter stage structure in the stationary reference frame ( $\alpha\beta$  coordinates). It consists of a BP-CCF (3.37) series connected with a set of *n* BS-CCFs (3.38) are used to isolate the positivesequence fundamental component of the grid voltage. The BP-CCF is tuned for a center frequency  $\omega_0=50$  Hz (European grid) and a bandwidth  $\omega_{bw\_bp}$ . The output of the BP-CCF block feeds a set of cascaded *n* BS-CCFs, tuned to rejected fundamental frequency-dependent harmonics ( $-1^{st}$ ,  $-5^{th}$ ,  $7^{th}$ ,  $-11^{th}$ ,  $13^{th} \dots$ ) which are typically present in distorted grids, the bandwidth of the BS-CCF being  $\omega_{bw\_bsn}$ . Fig. 3.34(a) and 3.34(b) show the frequency response function magnitude and phase for the proposed pre-filter scheme.

CCFs intrinsically distinguish between positive and negative sequence components. Furthermore, BP-CCF provides unitary gain at the fundamental frequency, the gain monotonically decreasing as the frequency moves apart from this value.



Figure 3.33: Schematic representation of the proposed method



Figure 3.34: Magnitude and phase of the frequency response function of CCCF-CPLL

Once the fundamental frequency dependent harmonics have been removed from the measured line voltage, the frequency is estimated by using an ATO (see Fig. 3.33). The estimated frequency is used to make the filtering process frequency-adaptive. The phase of the fundamental voltage being obtained by integration of the ATO estimated frequency. As shown in Section 3.4.0.4, the ATO consists of a PI based closed-loop system whose input is the crossproduct between the filtered input signal  $(\bar{u}_{\alpha\beta})$  and a unitary vector rotating at the estimated phase angle  $e^{j\hat{\theta}}$  (3.39), being  $|\bar{u}_{\alpha\beta}|$  the voltage vector module. The ATO error  $\epsilon_{\theta}$  is proportional to the *sine* of the difference between the estimated ( $\hat{\theta}$ ) and the real angle ( $\theta$ ) (3.39),  $\sin(\theta - \hat{\theta}) \approx \theta - \hat{\theta}$  can be safely assumed if the angle error is small.

The ATO closed-loop transfer function and the overall output transfer function are given by (3.39) and (3.41) respectively, with  $G_{PI}(s)$  being the transfer function of the PI controller.

$$\varepsilon = \bar{u}_{\alpha\beta} \otimes e^{-j\hat{\theta}} = |\bar{u}_{\alpha\beta}|\sin(\theta - \hat{\theta})$$
(3.39)

$$\frac{\hat{\theta}(s)}{\theta(s)} = \frac{G_{PI}(s)}{s + G_{PI}(s)}, G_{PI}(s) = K_p \left(1 + \frac{K_i}{s}\right)$$
(3.40)

$$\frac{\hat{\omega}_i(s)}{\theta(s)} = \frac{s \cdot G_{PI}(s)}{s + G_{PI}(s)} \tag{3.41}$$

## 3.6.3 Tuning methodology

This subsection describes how to tune the ATO PI controller. Since a simulation and experimental comparative between different synchronization methods will be performed, a tunning methodology has been systematized in order to perform a fair analysis. Table 3.1 summarizes the simulation and experimental setup used for the optimization process.

The mean squared error (MSE) (3.42), between the real phase ( $\theta$ ) and the estimated phase ( $\hat{\theta}$ ), was chosen as a reliable figure of merit, its minimization using numerical optimization has been used for the gain selection for each method. The MSE will be function of the proportional and integral gains of the controller,  $K_p$  and  $K_i$ , color maps were found to be adequate to show

Sim. Step	Grid parameters	Harmonics	Freq. Jump	Unbalance	Amp. Jump
$10^{-4}s$	380V, 50 Hz	10% pu $(-5^{th})$	50Hz to 48Hz	$\begin{array}{c} 0.7 \ pu \\ \text{phase} \ C \end{array}$	0.5 pu

Table 3.1: Simulation scenario for the CCCF-CPLL method

this dependence. Similarly to (3.42), the MSE can also be calculated using the error in the estimation of the fundamental voltage magnitude (3.43) and of the fundamental voltage frequency (3.44), where subscripts *dist* refers to type the disturbance being applied, with f standing for a frequency step, mstanding for an amplitude step, u for an unbalance in the grid voltage and hfor the grid voltage containing harmonics.

$$MSE_{phase,dist}(t) = \frac{1}{T} \int \left(\theta - \hat{\theta}\right)^2(t) dt$$
(3.42)

$$MSE_{amp,dist}(t) = \frac{1}{T} \int \left( \left| u_{\alpha\beta} \right| - \left| \hat{u}_{\alpha\beta} \right| \right)^2(t) dt$$
(3.43)

$$MSE_{freq,dist}(t) = \frac{1}{T} \int \left(\omega - \hat{\omega}\right)^2 (t) dt$$
(3.44)

$$MSE_{phase,global} = w_f MSE_{phase,f} + w_m MSE_{phase,m} + w_u MSE_{phase,u} + w_h MSE_{phase,h}$$
(3.45)

Fig. 3.35 shows the CCCF-CPLL error color maps obtained for the different types of distortions and transient conditions of the line voltage: frequency deviations from the rated value (Fig. 3.35(a)), magnitude deviations (Fig. 3.35(b)), unbalanced (Fig. 3.35(c)) and harmonic conditions (Fig. 3.35(d)).

It is observed from the figure that the cases in 3.35(b), 3.35(c) and 3.35(d) have similar color maps, meaning that the same set of gains provides near optimal results (i.e. minimum MSE) for those type of disturbances. It is noted however that the regions with lowest error in Fig. 3.35(a) occurs for

-2

-4

-6

-8

-10



(a) fundamental voltage frequency steplike change



0

2

4

6°

like change

10 20

, 30 Ki

(b) fundamental voltage amplitude step-

40 50

Kp

Figure 3.35: CCCF-CPLL color maps showing the MSE (3.42) as a function of the controller gains for different types of disturbances and varying conditions in the line voltage

different values of the gains. Choosing a set of  $K_p$  and  $K_i$  gains adequate for all the disturbances considered can be done by combining the MSEs in Figs. 3.35(a) to 3.35(d) into a global  $MSE_{phase,global}$  (3.45).

The purpose of the weights  $w_x$  is to prioritize the type of disturbance that should be better rejected. For example, sudden step-like changes of the frequency are less likely to occur than other kind of distortions, due to the large inertia of the generators [133], [14]. Then, a smaller value for  $w_f$ , compared to the rest of weights in (3.42), could be used. Fig. 3.35(e) shows the *MSEphase,global* when  $w_h = w_u = w_m = 0.33$  and  $w_f = 0.01$ . According to Fig. 3.35(e), values of the gains  $K_p=0.3$  and  $K_i \approx 38$  would be adequate choices, as *MSEphase,global* is small and has low sensitivity to changes of  $K_p$  and  $K_i$ . It is also observed from Fig. 3.35(e) that other regions with low values of  $MSE_{phase,global}$  exist, but shows a larger sensitivity to variations of  $K_p$  and  $K_i$ . Fig. 3.36 shows the  $MSE_{phase,global}$  color maps obtained using the tuning methodology described for all synchronization methods considered. The  $MSE_{phase,global}$  color maps are shown as a function of the PLL PI regulator gains,  $K_p$  and  $K_i$  respectively, for the scenarios described in Table 3.1.

The same weights as for the CCCF-CPLL were used. It is observed from Fig. 3.36(a) and 3.36(c) that for the case of the DSOGI-PLL and BP-CCF-CPLL, there is a region of low values of  $MSE_{phase,global}$ , and with a relatively smooth transition to the regions with larger values. This means that these methods have a good disturbance rejection capability, the MSE selection of the gains, therefore not being critical, i.e. slight changes in the gains do not have a critical impact on the performance of the method. Opposite to this, significantly larger variations of the  $MSE_{phase,global}$  are observed in Fig. 3.36(b) for the case of the DSRF-PLL, meaning that this method is more sensitive to the tuning process. The results of optimization stage for each method are summarized in Table 3.1.

While DSRF-PLL and DSOGI-PLL methods do not need to configure any extra block (see Fig. 3.15 and 3.17), MCCF-PLL and CCCF-CPLL methods use a first-order CCF (see Fig. 3.32) for each component being removed/isolated. MCCF-PLL method (Fig. 3.19) uses three BP-CCFs: one for fundamental component, one for  $-1^{st}$  harmonic (to isolate the negative sequence component due to unbalance) and another to isolate the -5th fundamental dependence harmonic. The CCCF-CPLL method uses one BP-CCF to isolate the fundamental component and two BS-CCFs being used to reject the  $-1^{st}$  and  $-5^{th}$  harmonics. The bandwidths  $w_{bw}$  selected for each method are shown in Table 3.2.



Figure 3.36: Color maps showing the  $MSE_{phase,global}$  as a function of the controller gains for the different methods. Same scale as in Fig. 3.35 was used

DSOGI – PLL	$K_p = 3.72$		$K_i = 28.72$
DSRF - PLL	$K_p = 3.72$		$K_i = 28.72$
MCCF – PLL	$K_p = 1.06$	$K_i = 0.71$	$w_{bw\ mccf} = 300 rad/s$
CCCF - PLL	$K_{p} = 0.3$	$K_i = 38.48$	$w_{bw\ bp-ccf} = 300 rad/s$ $w_{bw\ bs-ccf(-1)} = 100 rad/s$ $w_{bw\ bs-ccf(-5)} = 300 rad/s$
BP - CCF - PLL	$K_p = 1.98$	$K_i = 104.2$	$w_{bw\ bp-ccf} = 300 rad/s$

Table 3.2: Gains resulting form the optimization stage



Figure 3.37: CCCF-CPLL Simulation Setup

## 3.6.4 Simulation results

The proposed synchronization technique has been tested using the simulation scheme shown in Fig 3.37. Four different scenarios have been considered:

- 1. Frequency deviations from the grid rated value
- 2. Magnitude deviations from the grid rated value
- 3. Grid unbalanced conditions
- 4. Polluted grid including harmonics

Simulation were performed using Matlab. Tustin was used for the discretization of the continuous transfer functions. For each case, the performance of the proposed method is compared with the results obtained using the following synchronization methods: DSRF-PLL, DSOGI-PLL, MCCF-PLL and BP-CCF-CPLL.

Fig. 3.38 shows the estimated frequencies and amplitudes (in p.u., referred to the rated grid values, Table 3.1) for different type of disturbances in the line voltage, including changes in the fundamental voltage frequency and magnitude, unbalanced conditions and harmonics. Fig. 3.39 shows the MSE for the estimated fundamental voltage phase (3.42), magnitude (3.43) and frequency (3.44). The bars for each case were normalized by dividing by the worst case, the maximum value for each case being therefore equal to one.

Fig. 3.38(a) shows the simulation results when the frequency changes from 1 to 0.96 p.u. at t=1s. It is observed that CCCF-CPLL shows the slowest response, while MCCF-PLL, DSOGI-PLL, BP-CCF-CPLL and DSRF-PLL show similar, faster response, being the DSOGI-PLL the method with shortest settling time. Fig. 3.39(a) summarizes the MSE for the case of



(a) step-like change of line voltage frequency





1.1 t(s)

1.2

1.02

0.98

1

1

mag (p.u.)

(b) step-like change of the line voltage magnitude



(d) line voltage containing harmonics

Figure 3.38: Simulation Results. Estimated frequency (left) and magnitude (right) of the fundamental voltage by the different methods

a step-like change in the frequency, confirming the results observed in Fig. 3.38(a).

A 50% amplitude jump has been introduced in Fig. 3.38(b), t=1s. It is observed from Figs. 3.38(b) and 3.39(b) that the BP-CCF-CPLL shows an overall better behavior, followed by the CCCF-CPLL. On the other hand, an amplitude change produces oscillations in the estimated frequency, DSRF-PLL showing the worst behavior in this regard. Regarding the error in the estimation of the frequency and phase terms, the behavior of DSRF-PLL, DSOGI-PLL and MCCF-PLL are the worst, showing a fast but oscillating response. It is finally noted that either for amplitude, frequency or phase MSE, the best methods to deal with changes in the amplitude are the BP-CCF-CPLL and the CCCF-CPLL. Conversely, DSRF-PLL shows the worst frequency and phase MSE, while MCCF-PLL exhibits the biggest amplitude MSE.

Fig 3.38(c) shows the simulation results for the case of a 30% unbalance in phase C. It can be observed that the DSOGI-PLL shows the most appealing behavior, followed by the CCCF-CPLL, being the BP-CCF-CPLL the method with the lowest unbalance rejection capability. It is also noted that although the DSOGI-PLL shows good unbalance rejection, it has poor harmonic rejection capability (Fig. 3.38(d)). This is explained because the DSOGI-PLL has two SOGI-QSGs (see Fig. 3.17) that extract the positive sequence component, removing the negative sequence. However it does not have any extra block to remove high order fundamental dependence harmonics. The different MSEs during the unbalance for each method are summarized in Fig 3.39(c). The CCCF-CPLL and the DSOGI-PLL are the methods with lowest MSE in all cases (amplitude, frequency and phase), while the BP-CCF-CPLL is the method with the poorest performance, as it does not reject the negative sequence component as it only uses a band-pass-filter for the positive sequence component.

The impact of phase voltage harmonics on the estimated fundamental frequency and fundamental voltage magnitude are shown in Fig. 3.38(d). It is observed that MCCF-PLL and CCCF-CPLL almost totally reject all the harmonics. On the other hand, BP-CCF-CPLL, DSOGI-PLL and DSRF-PLL show lower harmonic rejection capability; significant oscillations in the estimated frequency being observed for both methods. Fig. 3.39(d) summarizes the simulation results when harmonics in the grid voltage are present.





(b) step-like change of the line voltage

(a) step-like change of line voltage frequency



magnitude

Figure 3.39: Simulation results: MSE of the estimated amplitude (3.43), frequency (3.44) and phase (3.42) for all the methods and for the different type of disturbances

## 3.6.5 Experimental results

The experimental setup is shown in Fig. 3.40. A diesel generator "G" rated 100kVa, 380V and 152A, was used as the primary power source for the master and slave inverters. LCL filters, with a resonance frequency of 575Hz are used to connect the inverters to the grid. The master inverter was programmed to produce the same type of disturbances discussed in the simulation tests. A *TMS320F28335* DSP has been used for the implementation of the algorithms. A sampling frequency of 10 kHz was used, which is equal to the switching frequency. As for the simulation results, Tustin transformation was used for the discretization of the continuous transfer functions. The gains for the different methods have been tuned to the values obtained during the optimization process described in the previous section (see Table 3.2).

Fig. 3.41 shows the experimentally measured frequency and amplitude



Figure 3.40: CCCF-CPLL Experimental Setup

for the same disturbances and transient conditions discussed in section 3.6.4, Fig. 3.42 shows the MSEs for all the cases that are discussed following. Fig. 3.41(a) shows the results when a step-like frequency variation from 1 to 0.96 p.u. (t=0.5) occurs. It is observed that all methods show a similar response, except the proposed method that is slower updating the grid frequency, so it causes an additional phase shift. The experimental results mostly agree with the simulation results. It is noted that this behavior is not considered a critical issue since such kind of transient is not expected to occur in practice.

Fig. 3.41(b) shows the response of the different methods when a steplike variation of 50% is applied to the fundamental voltage magnitude. The dynamic response of all methods is very similar, which is also confirmed by Fig. 3.42(b). Some disagreement is observed among the experimental results in Fig. 3.42 and the simulation results in Fig. 3.39. This discrepancy would be explained by the fact that, contrary to the simulation (see Fig. 3.38(b) ), the output voltage amplitude of the master inverter cannot be changed instantaneously (see Fig. 3.41(b)).

An unbalance of 30% was introduced in the phase C of the master inverter output voltage. Fig. 3.41(c) shows the estimated frequency and amplitude by each synchronization method. As for the simulation results, the BP-CCF-CPLL method exhibits a slightly worse unbalance rejection capability, with a negative sequence component showing up both in amplitude and frequency. The performance of the remaining methods is very similar.

Fig. 3.41(d) shows the estimated amplitude and frequency for all synchronization methods when a  $-5^{th}$  harmonic of magnitude 0.1p.u. is present in the grid voltage. The DSRF-PLL exhibits the poorest performance, with the rest of synchronization methods showing a similar behavior. Still, according to Fig. 3.42(d), the CCCF-CPLL shows the lowest combined error (amplitude, frequency and phase), which is in accordance with the simulation results presented in section 3.6.4. The differences between simulation and experimental results are due, as for the case of the unbalanced voltage, to the low-pass behavior of the synchronization control strategy of the slave inverter.

Table 3.3 summarizes the results obtained for each method according to the following criteria:

- Simplicity: conceptual complexity of each method.
- Flexibility: possibility of adapting the system, e.g. rejected/isolated harmonics, to the grid behavior.
- Application on active power filter (APF): possibility to measure high order harmonics to be further compensated by an APF.
- Tuning sensitivity: Sensitivity of the performance for each method to small changes in the controller gains. This is related to the smoothness of the MSE color map.
- Dynamic response: evaluates the settling time when a change in the line frequency occur.

Conceptually, the proposed method is relatively simple, as it consists of a BP-CCF, several BS-CCFs (depending on the harmonics that want to be rejected) and an ATO series connected, not being necessary decoupling networks (e.g. DSOGI-PLL or MCCF-PLL), which would increase the complexity of the method. CCCF-CPLL method also has good flexibility, as only one BS-CCF is needed for each component being rejected. DSOGI-PLL and DSRF-PLL do not provide a mechanism to decouple harmonics.

All methods are frequency-adaptive so they can change the central frequency of their filters if a change in the fundamental frequency occurs. The estimation of the frequency with the proposed method has slower dynamics compared to the others methods. However, it is noted that the rate of frequency variation of a grid is small [14] (e.g. the UNE-EN 5016 limits the maximum frequency shifts: for interconnected systems the mean frequency value, calculated each 10s, should not exceed  $\pm 1\%$  during the 99.5% of a week, though exceptionally deviations between +4% and -6% are permitted).

If the synchronization method is to be used in an APF, the MCCF-PLL and the BP-CCF-CPLL would be in principle appealing options, as they



(d) line voltage containing harmonics

Figure 3.41: *Experimental Results*. Estimated frequency (left) and magnitude (right) of the fundamental voltage by the different methods



(a) step-like change of line voltage frequency



1 Error(pu) 0.5 0 Mag Freq Phase

(b) step-like change of the line voltage magnitude



Figure 3.42: Experimental results: MSE of the estimated amplitude (3.43), frequency (3.44) and phase (3.42) for all the methods and for the different type of disturbances

	CCCF	DSOGI	DSRF	MCCF	BP-CCF
	CPLL	PLL	PLL	PLL	PLL
Simplicity	low	high	high	medium	low
Flexibility	excellent	low	low	excellent	medium
Freq. adapt	yes	yes	yes	yes	yes
Application to APF	no	no	no	yes	yes
Tune Complexity	medium	low	high	low	low
Execution Time (us)	7.22	4.98	8.32	6.94	7.42
Time response	medium	medium	medium	excellent	excellent
Unbalance response	excellent	excellent	good	excellent	low
Harmonic Rejection	excellent	medium	low	excellent	medium

Table 3.3: Comparison of synchronization methods

provide the amplitude and phase of each harmonics to be compensated. Regarding their tuning, the CCCF-CPLL shows a smooth and wide tuning area so it is easy to tune. Contrary to this, DSRF-PLL method is rather sensitive to variations of the parameters. As for the computational requirements, DSOGI-PLL has the lower burden, though it is at the price of lower performance. Finally, regarding unbalanced line voltages and harmonic rejection, both CCCF-CPLL and MCCF-PLL have excellent performance, with DSRF-PLL and BP-CCF-CPLL being the worst in this aspect.



Figure 3.43: NFOL-PLL control structure

# 3.7 Three-phase filter on the loop stage NFOL-CPLL synchronization method

The main drawback of the CCCF method that has been analyzed in 3.6 is that the phase error depends on the input magnitude. Additionally, pre-filter stage methods, e.g. the proposed CCCF-CPLL method, are conceptually more complicated and difficult to tune than filter on the loop methods.

To overcome these limitations, this section presents a filter on the loop synchronization technique called notched filter on the loop with complex PLL (NFOL-CPLL). NFOL-CPLL will be shown to be easy to tune, frequency adaptive, with excellent disturbance rejection capability and in which the phase error does not depends on the input signal magnitude.

# 3.7.1 Notched filter on the loop with complex PLL (NFOL-CPLL)

Fig. 3.43 shows the block diagram of the proposed Notched Filter in the Loop with Complex PLL (NFOL-CPLL) method. The signal processing used to estimate the fundamental voltage component magnitude and phase is explained following.

An ATO with a filter in the loop stage is used to estimate the phase of the fundamental component (positive sequence). For discussion purposes, it will be first assumed that the input signal,  $u_{\alpha\beta}$ , 3.46, consists of the fundamental component and two harmonics, one being a positive sequence component of order -n. The

error signal 3.47 is obtained as the vector cross-product between the input signal  $(u_{\alpha\beta})$  and the estimated unit vector  $(e^{j\hat{\theta}})$ , whose phase is the estimated phase of the input signal. The input signal  $(u_{\alpha\beta})$  is normalized by dividing by the estimated fundamental magnitude  $(\hat{U}_1)$ , making the phase error independent of the input magnitude. Assuming perfect tracking of the fundamental component, i.e.  $\hat{\theta} = \omega_0 t$ , the error signal, 3.47, can be expressed as 3.48.

$$u_{\alpha\beta} = U_1 e^{j\omega_0 t} + U_m e^{jm\omega_0 t + \phi} + U_n e^{-jn\omega_0 t + \gamma}$$

$$(3.46)$$

$$\epsilon_{\theta} = \frac{u_{\alpha\beta} \otimes e^{j\hat{\theta}}}{\hat{U}_{1}} = \frac{real(u_{\alpha\beta}) \cdot \sin(\hat{\theta}) - imag(u_{\alpha\beta}) \cdot \cos(\hat{\theta})}{\hat{U}_{1}} =$$
$$= \frac{\sin(\hat{\theta})}{\hat{U}_{1}} \left[ U_{1}\cos(\omega_{0}t) + U_{m}\cos(m\omega_{0}t + \phi) + U_{n}\cos(-n\omega_{0}t + \gamma) \right] - (3.47)$$
$$- \frac{\cos(\hat{\theta})}{\hat{U}_{1}} \left[ U_{1}\sin(\omega_{0}t) + U_{m}\sin(m\omega_{0}t + \phi) + U_{n}\sin(-n\omega_{0}t + \gamma) \right]$$

$$\epsilon_{\theta} = \frac{U_m}{\hat{U}_1} \sin\left((m+1)\omega_0 t - \phi\right) - \frac{U_n}{\hat{U}_1} \sin\left(-(n-1)\omega_0 t - \gamma\right)$$
(3.48)

Assuming  $\phi = \gamma = 0$ , 3.48 can be further simplified if certain values are assumed for *n* and *m*. It is noted that this assumption is realistic considering the harmonic orders commonly found in practice. E.g. for the case of n=-5 and m=7, a 6<sup>th</sup> harmonic is induced in the error signal 3.48, its amplitude being a linear combination of the amplitude of both harmonics. Similarly, for the case of *n*=-11 and *m*=13, a 12<sup>th</sup> harmonic is induced in the error signal. It is concluded that the error signal will contain harmonics at frequencies  $h \cdot 6 \cdot \omega_0$ , with h=1,2,3,....

When a nonlinear load is fed by a unbalanced three phase voltage system through an impedance, the voltage vector at the load terminals,  $(u_{\alpha\beta})$ , can be expressed as (3.49). Both positive and negative odd harmonics are induced in the PCC grid voltage due to the current harmonics flowing across the nonlinear load (see Fig. (3.44(a))). As a consequence, the error signal 3.48 (see Fig. 3.43) contains all even harmonics. Fig. (3.44(a)) (red) shows the ATO input spectrum under unbalanced conditions while Fig. (3.44(b)) shows



Figure 3.44: ATO harmonics for case of balanced and unbalanced voltage.

the error signal spectrum, harmonics at frequencies  $h \cdot \omega_0$  (h=2,4,6,8,...) being readily visible.

$$u_{\alpha\beta} = \sum_{\substack{h=\pm(2p+1)\\p=0:1:\infty}} U_h e^{j(h\omega_0 t + \theta_h)}$$
(3.49)

Fig. 3.44(a) shows the spectrum of the input signal to the ATO PI controller. In blue is shown the case of a balanced voltage, (harmonic -1 not present), and in red the case of unbalanced conditions (harmonic -1 is present). Fig. 3.44(b) shows the error signal spectrum for both balanced case (blue) and unbalanced case (red), the differences being readily observable.

To estimate the magnitude of the fundamental voltage component,  $U_1$ , the scalar product between the grid voltage,  $u_{\alpha\beta}$ , and the unit vector  $e^{j\hat{\theta}}$  is performed, with the phase angle of the unit vector being estimated by the ATO (see Fig. 3.43). A filtering stage is placed after the scalar product to provide a disturbance rejection mechanism for the magnitude estimation.

Similarly to the phase extraction procedure discussed previously, if the input complex voltage vector is balanced (3.46), the scalar product will be of the form shown by (3.51). For the case of  $\theta = \gamma = 0$ , the spectrum of  $\hat{U}$  consists of a DC component, whose amplitude is the fundamental component of the grid voltage  $(U_1)$ , and a set of harmonic components located at  $h \cdot 6 \cdot \omega_0$ 



Figure 3.45: ATO harmonics for case of balanced and unbalanced grid voltage.

(h=1,2,3,...). The corresponding frequency spectrum is shown in Fig. 3.45. Conversely, if the input complex vector of the magnitude estimation block is that of an unbalanced-fed nonlinear load defined by (3.49), the spectrum of  $\hat{U}$  (3.52) is composed by a DC component, whose amplitude is the grid fundamental voltage component  $(U_1)$ , and harmonic components located at  $h \cdot 2 \cdot \omega_0$  (h=1,2,3,...).

$$\hat{U} = u_{\alpha\beta} \cdot e^{j\hat{\theta}} = real\left(u_{\alpha\beta}(t)\right) \cdot \cos(\hat{\theta}) + imag\left(u_{\alpha\beta}(t)\right) \cdot \sin(\hat{\theta}) \qquad (3.50)$$

$$\hat{U} = U_1 + \sum_{h=0:1:\infty} U_h \cos\left(6 \cdot h \cdot \omega_0 \cdot t\right)$$
(3.51)

$$\hat{U} = U_1 + \sum_{h=0:1:\infty} U_h \cos\left(2 \cdot h \cdot \omega_0 \cdot t\right)$$
(3.52)

## 3.7.2 Filtering stage design

As already mentioned, the frequency spectrum of the PI regulator input (3.48) and amplitude estimation (3.52) will be of the form  $h \cdot 6 \cdot \omega_0$  for the case of a balanced grid voltage and  $h \cdot 2 \cdot \omega_0$  for the case of an unbalanced grid voltage, with h=1,2,3,... Cascaded second order notch filters are used to remove specific harmonic components. The notch filters transfer function must have the zeros located on top of the unit circle at the notch frequency  $(e^{\pm \omega_n})$ , and the poles located within the unit circle and near to the zeros, to assure unitary gain for the non-notch band. The nearer the poles to the unit circle are, the smaller the bandwidth of the notch filter is [137]. To reject the disturbances modeled in the previous subsection, a filtering stage consisting



Figure 3.46: Filtering stage block diagram

of n cascaded notch filters is proposed (see Fig. 3.46). Their design, tuning, stability analysis and digital implementation is addressed in section 3.7.3.

The transfer function of a generic second order ANF can be expressed as (3.53), where  $\zeta$  sets the depth and the width of the filter and  $\Omega_n$  is the notch frequency. Since the proposed NFOL-CPLL method is intended to be implemented digitally, the system design and stability analysis will be performed in the discrete time domain. Tustin discretization will be used (3.54) to transform from the continuous domain to the discrete domain, (3.55) being obtained by discretization of (3.53).

$$NF(s) = \frac{s^2 + \Omega_n^2}{s^2 + \zeta \cdot s + \Omega_n^2}; \Omega_n = n \cdot \Omega_o$$
(3.53)

$$s = \frac{2}{T_s} \frac{z-1}{z+1}$$
(3.54)

$$NF_{\omega_n}(z) = b \cdot \frac{1 - 2 \cdot \cos(\omega_n) z^{-1} + z^{-2}}{1 - 2 \cdot b \cdot \cos(\omega_n) z^{-1} + (2 \cdot b - 1) z^{-2}}$$
(3.55)

$$\omega_n = \frac{n \cdot \omega_0}{f_s/2} \tag{3.56}$$

$$b = \frac{1}{1+\beta} \tag{3.57}$$



Figure 3.47: Digital notch filter design

$$\beta = \frac{\sqrt{1 - A^2_{-3dB}}}{A_{-3dB}} \tan\left(\frac{BW}{2}\right); BW = \frac{\Delta w}{f_s/2}$$
(3.58)

$$FS(z) = \prod_{n=1}^{N} NF_{\omega_n}(z) = \frac{\prod_{i=1}^{C} (z - c_i)}{\prod_{k=1}^{P} (z - p_k)}$$
(3.59)

where  $\omega_n$  is the notch frequency (3.56),  $\omega_0$  stands for the rated grid frequency,  $100\pi$  rad/s in Europe,  $T_s$  and  $f_s$  are the sampling time and the sampling frequency respectively, BW is the notch filter bandwidth and  $A_{-3dB}$ is the notch filter magnitude at -3dB ( $10^{-3/20} = \sqrt{2}/2$ ) (See Fig. 3.47).

The international standards for grid-connected converters, [11], [14], [12], [13], [5], [7], [10], [6], [3], [8], [1], [2], [9], [4] and [68], limit the maximum overall voltage harmonic distortion (THD) to 5%, with each individual harmonic magnitude being smaller than 4% for harmonic orders lower than 11<sup>th</sup>, 2% for the harmonic orders between 11<sup>th</sup> and 17<sup>th</sup>, 1.5% for harmonic orders between 17<sup>th</sup> and 23<sup>rd</sup>, 0.6% for harmonic orders between 23<sup>rd</sup> and 35<sup>th</sup> and 0.3% for orders higher than 35<sup>th</sup>. Since each notch filter adds an additional phase shift in the estimated phase angle of the fundamental voltage, it is convenient to limit the number of notch filters being cascaded. Therefore, only harmonics whose order is lower than 11<sup>th</sup> will be considered for the filtering process. The proposed filtering stage consists of three notch filters, (3.55), located at  $\omega_2=2 \cdot w_0$  (100 Hz),  $\omega_4=4 \cdot w_0$  (200 Hz) and  $\omega_6=6 \cdot w_0$  (300Hz), which corresponds to  $-1^{st}$ ,  $3^{rd}$ ,  $-3^{rd}$ ,  $5^{th}$ ,  $-5^{th}$  and  $7^{th}$  harmonics of the grid voltage. Adding new harmonic components would be straightforward.



Figure 3.48: Filtering stage zero-pole map.

Finally, a low-pass filter could be added to the filtering stage in order to deal with noise coming from the sensors and power electronics. It is not necessary to add this filter to the ATO, as the PI regulator can effectively act like a low-pass filter. However, it can be placed after the scalar product used for magnitude estimation. A 3 kHz low-pass filter has been used in this case.

Fig. 3.48 shows the zero-pole map when the proposed notch filter design (3.59) is used for the selected notch frequencies, with bandwidth of 7.95 Hz (50 rad/s). It is observed that all zeros are placed on the unit circle, the poles being close to the zeros and inside the unit circle, following therefore the design principles.

## 3.7.3 Tuning methodology and stability analysis

The tuning methodology of the ATO PI controller to guarantee the system stability and provide adequate dynamic response is analyzed in this subsection. The linearized model of the proposed ATO is shown in Fig. 3.49, where the ATO error,  $\epsilon_{\theta}$  ((3.47) and Fig. 3.43), is proportional to the *sine* of the difference between the estimated ( $\hat{\theta}$ ) and the real angle ( $\theta$ );  $\sin(\theta - \hat{\theta}) \approx \theta - \hat{\theta}$ can be safely assumed if the angle error is small enough. The ATO closedloop transfer function and the overall transfer function are given by (3.60) and (3.61) respectively, with  $G_{PI}(s)$  (3.62) being the transfer function of the PI controller and FS(s) the transfer function of the filter stage.

$$\frac{\theta(s)}{\theta(s)} = \frac{FS(s) \cdot G_{PI}(s)}{s + FS(s) \cdot G_{PI}(s)}$$
(3.60)



Figure 3.49: ATO linear model.

$$\frac{\omega^*(s)}{\theta(s)} = \frac{s \cdot FS(s) \cdot G_{PI}(s)}{s + FS(s) \cdot G_{PI}(s)}$$
(3.61)

$$G_{PI}(s) = K_p + \frac{K_i}{s} \tag{3.62}$$

Different figures of merit were considered for the selection of  $G_{PI}(s)$  gains,  $K_p$  and  $K_i$ , to assess stability and dynamic performance. These included frequency based and time based criteria. Finally, the difference between phase margin and a target value (70°), *PhMar*, maximum overshoot, *Over*, and settling time, *setTime* were selected to be the more relevant. A global performance index, *GPI*, of the form shown by (3.63) was be defined, with the weights  $w_{phMar}$ ,  $w_{over}$  and  $w_{setTim}$  being set according to the importance given to each criteria.

$$GPI = w_{phMar} \cdot phMar + w_{over} \cdot over + w_{setTim} \cdot setTim$$
(3.63)

Color maps were found convenient for visualization purposes of the tuning procedure. The optimum value for the phase margin was selected to be  $70^{\circ}$ . On the other hand, for the overshoot and time response, the lower is their value, the better is the behavior of the system. Fig. 3.50(a) shows *PhMar*, which is defined to be *PhMar*=|*Phase margin*- $70^{\circ}$ |, i.e. the absolute value of the difference between the actual and the target phase margin, as a function of  $K_p$  and  $K_i$ . Figs. 3.50(b) and 3.50(c) show the overshoot in % and the settling time respectively, as a function of  $K_p$  and  $K_i$ . The weight of each color map,  $w_{phMar}$ ,  $w_{over}$  and  $w_{setTim}$ , in (3.63) is chosen in the following way:

60

40 20

100



(a) absolute value of the difference between the system Phase Margin (phMar)and target value (70 deg)



(d) global performance index (d) (f) (f)

0

£ 500

1000

0

50

Ki

(b) overshoot (*over*) in %

Figure 3.50: Color maps as a function of the controller gains.

relatively large values would normally be assigned to  $w_{phMar}$ , since stability is key, while smaller values would be used for  $w_{over}$  and  $w_{setTim}$ .

For the results shown in Fig. 3.50(d),  $w_{phMar}=0.9$ ,  $w_{over}=0.01$  and  $w_{setTim}=0.1$  were used. It is observed from Fig. 3.50 that the color map has smooth transitions, meaning that slight changes in the controller gains do not have a sharp impact on the overall stability. The gains that provide the best global performance (minimum in the color map in Fig. 3.50(d)) are  $K_p=328.9$  and  $K_i=17.31$ .

## 3.7.4 Simulation results

Simulation results showing the validity of the theoretical analysis are presented in this subsection. Fig. 3.51 shows the proposed simulation setup while Table 3.4 shows the maximum deviations allowed for the magnitude for grid-connected systems. A programmable AC source was used to produce different types of disturbances in the grid voltage:

1. Grid frequency deviations



Figure 3.51: Three-phase NFOL simulation setup

	Maximum value	Clearance time (s)	
Frequency deviation	$47 \le f_{Hz} \le 53$	0.2	
Voltage deviation	$0.8 \le \mathcal{V}_{pu} \le 1.2$	0.2	
Unbalance factor	4%	-	
Harmonic distortion	4% individual harmonic	-	

Table 3.4	Grid	narameter	houndaries	hv	normative
1abic <b>5.4</b> .	onu	parameter	Doundaries	IJУ	normative

- 2. Grid voltage magnitude deviations
- 3. Grid unbalanced
- 4. Harmonics
- 5. Simultaneous deviations of the grid frequency and magnitude
- 6. Simultaneous deviations of the grid frequency and harmonic

For each type of disturbance, the performance of the proposed NFOL-CPLL method is compared with two synchronization methods: MCCF-PLL (subsection 3.4.1.3) and CCCF-CPLL (section 3.6). Although a large number of synchronization methods could be found in the literature, the MCCF-PLL and the CCCF-CPLL were selected since they are widely used and especially indicated for highly polluted networks.

Both the MCCF-PLL and the CCCF-CPLL were configured to reject  $-1^{st}$ ,  $-5^{th}$  and  $7^{th}$  harmonics. The bandwidth of the band-stop filters was set to 7.95 Hz (50 rad/s) for all methods, while the band-pass filter for the fundamental component in MCCF-PLL and CCCF-CPLL has been set to 95.50 Hz (600 rad/s). The low-pass magnitude filter bandwidth for the proposed method is set to 3 kHz ( $6000\pi rad/s$ ).

Since the CCCF-CPLL method uses the same ATO as the proposed method, they have been tuned identically in both cases. The same tuning methodology described in the previous section was used for the MCCF-PLL, the optimal gains for the PI obtained being  $K_p=231.42$  and  $K_i=8.37$ .

The applied disturbances have been selected according to grid codes limits [11], [14], [12], [13], [5], [7], [10], [6], [3], [8], [1], [2], [9], [4] and [68] (see Table 3.4), where the clearance time refers to the detection and disconnection time from the main grid. Simulation results are shown in per unit, rated grid voltage and frequency being 220 V and 50 Hz respectively. The magnitude, frequency and phase error signals will be shown since these signals are relevant for different purposes, including synchronization, magnitude/frequency restoration, droop control and power calculation.

Ramp-like and step-like frequency changes were used for the frequency deviation test (Fig. 3.52), with the voltage magnitude being kept constant. The corresponding profiles are shown in Fig. 3.52(a) and 3.52(b). They include a frequency ramp-like change of 3 Hz in 0.2s and a step-like change of 6 Hz (see Table 3.4), which are intended to emulate the inertia of synchronous generators and/or the connection/disconnection of large loads in weak grids or islanded and droop-controlled microgrids.

The profile used to check out the performance of the methods in the event of changes in the magnitude is shown in Fig. 3.53(b), with the frequency being kept constant (Fig. 3.53(a)).

While the transient response of all methods being considered is correct for the case of ramp-like changes, a high frequency oscillation, which fades away in a few ms, shows up in the tracked frequencies, magnitudes and phases for the case of step-like variations.

Unbalanced conditions are caused mainly by unbalanced loads and single phase loads, which create unbalanced load currents, eventually resulting in non-symmetrical voltage drops in the phase voltage. The voltage unbalance factor (VUF) is usually defined as the ratio between the negative sequence and the positive sequence voltage components, the acceptable limits being shown in Table 3.4 (4%). Two values of the voltage unbalance factor were tested (see Fig. 3.54(b)), with the frequency remaining unchanged (see Fig. 3.54(a)). Initially, a 4% unbalance factor (normative limit) was produced for 1s < t < 2s; then, a 10% unbalance factor (Above notrmative limit) was used produced for t > 2s. All the methods show good unbalance rejection capability, both in estimated magnitude (Fig. 3.54(c)), frequency (Fig. 3.54(d)) and phase (Fig. 3.54(e)).



Figure 3.52: Simulation results showing the response to frequency deviations



Figure 3.53: Simulation results showing the response to changes in the magnitude



Figure 3.54: Simulation results showing the response to an unbalance in the phase voltages

Historically, electric machines (mainly transformers, and electric machines and to a lesser extent) were the main sources of harmonics in power systems. However, the power electronic equipment that is commonly used nowadays, has become one of the primary sources for harmonic distortion. Section 3.7.3 and Table 3.4 describe the maximum harmonic distortion allowed for grid-connected equipment.

Fig. 3.55 shows the simulation results when a  $5^{th}$  harmonic is applied, its magnitude being shown in Fig. 3.55(b). The fundamental frequency remains constant (see Fig. 3.55(a)). It is observed from Fig. 3.55 that MCCF-PLL and CCCF-CPLL methods do not completely reject the harmonics, oscillations being observed both in magnitude and frequency (Figs. 3.55(c), 3.55(d) in steady state. These oscillations do not show up in the estimated phase due to the low-pass filter behavior of the integrator (Fig. 3.55(e)).

Fig. 3.56 shows the response when frequency (Fig. 3.56(a)) and magnitude (Fig. 3.56(b)) changes (including ramp-like and step-like patterns) occur simultaneously. This could occur in practice due to the connection/disconnection of large loads to weak grids, or for the case of islanded and droop-controlled microgrids. The errors in this case are seen to combine the effects already observed in Figs. 3.52 and 3.53.

Fig. 3.57 shows the simulation results when frequency deviations (Fig. 3.57(a)) and a 5<sup>th</sup> harmonic (Fig. 3.57(b)) are applied simultaneously. This test is intended to confirm the harmonic rejection capability when the frequency changes, and some frequency error can therefore be expected. It is observed from Fig. 3.57(c), 3.57(d) and 3.57(e) that the results for all the three methods follow the tendency shown in Fig. 3.52 and Fig. 3.55.

To summarize the simulation results, the proposed method shows a good magnitude tracking capability with zero steady state error. Conversely, the other two methods show a small (<1%) steady state magnitude error, as well as oscillations in the estimated magnitude in the presence of disturbances. All the three methods show similar frequency tracking capability, with negligible steady-state errors.

#### 3.7.5 Experimental results

Experimental results showing the performance of the proposed method, the MCCF-PLL and CCCF-CPLL methods, are presented in this section. The experimental setup is shown in Fig. 3.58, where the breaker connecting both inverters is open. The resonance frequency for both LCL filters is 575 Hz. A sampling frequency of 10 kHz was used, which is equal to the


Figure 3.55: Simulation results showing the response to harmonic conditions



Figure 3.56: Simulation results showing the response to simultaneous changes in magnitude and frequency



Figure 3.57: Simulation results showing the response to changes in frequency including harmonic conditions



Figure 3.58: Three-phase NFOL experimental setup

switching frequency. The master inverter is configured to produce the same disturbances discussed in the previous section. The different synchronization methods have been tuned using the optimization strategy described in Section 3.7.3.

Fig. 3.59 shows the experimental results under ramp-like (t=1, 4s) and step-like (t=2, 3s) frequency deviations. It is noted that there is a slight increase of both the frequency and phase errors during the transient following a step-like frequency change. These transient response is seen to fade away in a few *ms*. However, this type of deviation is unlikely to occur in practice due to the large inertia of power generators.

Fig. 3.60 shows experimental results when the master inverter produces ramp-like and step-like variations of the output voltage magnitude (see Fig. 3.60(b)). A negative sequence component was injected by the master inverter, its magnitude being shown in Fig. 3.61(b). Fig. 3.62 contains the experimental results when a 5<sup>th</sup> harmonic is injected by the master inverter. The corresponding magnitude is shown in Fig. 3.62(b), the frequency was maintained constant (Fig. 3.62(a)).

The response to simultaneous changes in the frequency and magnitude of the master inverter output voltage are shown in Fig. 3.63(a) and Fig. 3.63(b) respectively. Experimental results are seen in good agreement with simulation results.

Finally, frequency changes (Fig. 3.64(a)) and harmonics (Fig. 3.64(b)) are applied simultaneously. It is observed that the proposed method exhibits the best overall performance both in steady state and during transients.

A good agreement between simulation and experimental results is observed. Table 3.5 summarizes the conclusions for each method. All the three methods show good performance, although the proposed NFOL-CPLL method exhibits the best transient response capability, negligible steadystate error and better noise cancellation, both in the estimated frequency



Figure 3.59: Experimental results showing the response to changes in the frequency



Figure 3.60: Experimental results showing the response to changes in the magnitude



Figure 3.61: Experimental results showing the response to unbalanced conditions



Figure 3.62: Experimental results showing the response to harmonic conditions



Figure 3.63: Experimental results showing the response with changes in the frequency and magnitude occur simultaneously



Figure 3.64: Experimental results showing the response when changes in the frequency and harmonics occur simultaneously

## 3.7 Three-phase filter on the loop stage NFOL-CPLL synchronization meth $\partial \mathbf{3}$

	CCCF-CPLL	MCCF-PLL	NFOL-CPLL
Simplicity	MEDIUM	HIGH	LOW
Response time	GOOD	GOOD	EXCELLENT
Unbalance response	GOOD	GOOD	EXCELLENT
Harmonic rejection	GOOD	GOOD	EXCELLENT

Table 3.5: Comparison of synchronization methods

and phase, compared to the other two methods.

## 3.8 Single-phase FOAP-CPLL synchronization method

## 3.8.1 Introduction

In recent years, due to the implantation of the end-user generation, low voltage and single-phase systems have grown noticeably. Consequently, singlephase synchronization methods have been the focus of significant research activity.

This section proposes a single-phase synchronization method that overcomes most of the limitations of single-phase synchronization methods discussed in 3.3. It will be shown that the method is frequency adaptive and with an excellent disturbance rejection capability.

Fig. 3.65 shows the proposed single-phase synchronization method, called first order all-pass filter PLL (FOAP-PLL). It consists of four major blocks:

- 1. A QSG, which emulates a three-phase balanced system.
- 2. A modified three-phase ATO to estimate the frequency and phase of the input signal.
- 3. A pre-filter stage (PFS) to remove the voltage harmonics.
- 4. A phase delay compensator (PDC), designed to compensate the phase delay introduced by the PFS

These four blocks are discussed following.

## 3.8.2 Quadrature signal generator using all-pass filters

Several approaches have been proposed to implement a QSG, including transport delay QSG, Hilbert transform QSG, inverse-Park QSG and SOGI-QSG, they are discussed in subsection 3.3.3.2.

To overcome the limitations of the previous QSGs, the use of an all-pass filter QSG (APF-QSG) is proposed. The all-pass filter is a powerful tool that has been used in other fields like audio processing, speech coding, and time delay estimation [101], [124]. The general form of an analog first order APF is shown in (3.64). Its main feature is that it provides unitary gain at



Figure 3.65: FOAP-PLL control structure

all frequencies (3.65), the phase response being given by (3.66). At the  $\omega_q$  frequency, often referred as the corner frequency, the all-pass filter shifts the input signal by 90 degrees.

$$APF_q(s) = \frac{s - w_q}{s + w_q} \tag{3.64}$$

$$|APF_q(s)| = 1 \tag{3.65}$$

$$\angle APF_q(s) = \phi_{QSG} = 180 - 2 \cdot \arctan\frac{\omega}{\omega_q} \tag{3.66}$$

Fig. 3.66 shows the APF frequency response function when  $\omega_q$  equals the frequency of the fundamental component (e.g. 50 Hz). The phase angle for higher order harmonics is given by ((3.66)). It is clear from ((3.66)) that errors in the phase angle of the quadrature component will occur if the actual grid frequency is different from  $\omega_q$  in ((3.64)). A real time estimation of the corner frequency is therefore required. The frequency estimated by the ATO (see Fig. (3.65)) will be used for this purpose.

## 3.8.3 ATO

For discussion purposes, it will be first assumed that the QSG input signal (3.67) (v' in Fig. 3.65), consists of the fundamental component and



Figure 3.66: FOAP-PLL control structure

a harmonic component of order n, where  $\phi_1$  and  $\phi_n$  are the phase angle of the fundamental component and the  $n^{th}$  harmonic respectively. It is also assumed that the QSG corner frequency matches the fundamental frequency. Thus there is a phase shift of 90 degree between the QSG output and the fundamental component of the voltage, while the  $n^{th}$  harmonic at the APF-QSG output is shifted  $\phi_{QSG}$  degrees (3.66) with respect to the input. The  $u_{\alpha\beta}$  complex voltage vector is given by (3.69).

$$v' = U_1 \cdot \cos(\omega_0 t - \phi_1) + U_n \cdot \cos(n\omega_0 t - \phi_n) \tag{3.67}$$

$$v'_{q} = U_{1} \cdot \cos(\omega_{0}t - \phi_{1} - \frac{\pi}{2}) + U_{n} \cdot \cos(n\omega_{0}t - \phi_{n} - \phi_{QSG})$$
(3.68)

$$u_{\alpha\beta} = \alpha + j\beta = v' + jv'_q \tag{3.69}$$

$$u_{\alpha\beta} = U_1 e^{j\omega_0 t} + U'_{-n} e^{nj\omega_0 t} + U'_n e^{-nj\omega_0 t}$$
(3.70)

Assuming  $\phi_1 = \phi_n = 0$ , the resulting  $u_{\alpha\beta}$  voltage complex vector consist of three components (3.70): a component rotating at the fundamental frequency of magnitude  $U_1$  and two components rotating at  $-n\omega_0$  and  $n\omega_0$  respectively, their magnitudes depending on  $\phi_{QSG}$  since the QSG creates

a harmonic component that is not in quadrature with the harmonic input (3.66) (see Fig. 3.66).

An ATO is used to estimate the frequency and phase angle of the fundamental component  $(U_1)$ . The error signal (3.71) (see Fig. 3.65) is obtained as the vector cross-product between the input signal  $u_{\alpha\beta}$  and the estimated unitary vector  $e^{j\hat{\theta}}$ . The error signal  $\epsilon_{\theta}$  is normalized by using the estimated fundamental voltage magnitude,  $\hat{U}_1$ , therefore making the dynamics of the phase error independent of the input magnitude. Assuming perfect tracking of the fundamental component, i.e.  $\hat{\theta}_v = \omega_0 t$ , the error signal (3.71) can be expressed as (3.72). It is observed that the phase error consists of two harmonic components of orders  $n \pm 1$ . It is noted that if the QSG input signal, v', contains more than one harmonic component, each input harmonic of order n will produce two harmonics of order  $n \pm 1$  in the phase error signal.

$$\epsilon_{\theta} = \frac{u_{\alpha\beta} \otimes e^{j\hat{\theta}}}{\hat{U}_{1}} = \frac{real(u_{\alpha\beta}) \cdot \sin(\hat{\theta}) - imag(u_{\alpha\beta}) \cdot \cos(\hat{\theta})}{\hat{U}_{1}} =$$

$$= \frac{\sin(\hat{\theta})}{\hat{U}_{1}} \Big[ U_{1}\cos(\omega_{0}t) + U_{n}\cos(n\omega_{0}t) \Big] -$$

$$- \frac{\cos(\hat{\theta})}{\hat{U}_{1}} \Big[ U_{1}\sin(\omega_{0}t) + U_{n}\cos(n\omega_{0}t) \Big]$$

$$\epsilon_{\theta} = \frac{U_{n}}{2\hat{U}_{1}} \Big[ \sin\left((n+1)\omega_{0}t\right) - \sin\left((n-1)\omega_{0}t\right) -$$

$$- \cos\left((n+1)\omega_{0}t - \phi_{QSG}\right) - \cos\left((n-1)\omega_{0}t - \phi_{QSG}\right) \Big]$$
(3.71)
$$(3.72)$$

To estimate the magnitude of the fundamental voltage component  $\hat{U}$  in Fig. 3.65), a scalar product between the grid voltage  $u_{\alpha\beta}$  and the unit vector  $e^{j\hat{\theta}}$  is used (3.73) (see Fig. 3.65). The estimated magnitude  $\hat{U}$  consists of a DC component, whose magnitude is equal to the magnitude of the fundamental component of the grid voltage  $\hat{U}_1$ , and a set of harmonic components. If the input voltage consists of more than one frequency component, each harmonic of order n will produce two harmonics of order  $n \pm 1$  in the estimated magnitude. Since the harmonic components will be removed by the PFS, a low-pass filter (LPF) would only be required to remove e.g. noise coming from the sensors and switching harmonics due to the power electronics.

$$\hat{U} = u_{\alpha\beta} \cdot e^{j\hat{\theta}} = real(u_{\alpha\beta}) \cdot \cos(\hat{\theta}) - imag(u_{\alpha\beta}) \cdot (\hat{\theta})$$
(3.73)

$$\hat{U} = U_1 + \frac{U_n}{2} [\cos((n+1)\omega_0 t) + \cos((n-1)\omega_0 t) + \\ + \sin((n+1)\omega_0 t - \phi_{QSG}) - \sin((n-1)\omega_0 t - \phi_{QSG})]$$
(3.74)

## 3.8.4 Pre-filter stage

A mechanism to provide harmonic rejection to the proposed method is to reduce the ATO PI controller bandwidth. However, this solution is unsatisfactory as the microgenerator stability relies on the ATO dynamic response. In addition, the output APF-QSG quadrature signal depends on the estimated ATO frequency. Therefore, the implementation of a specific mechanism to remove the harmonic content from the input voltage is advisable.

Two different approaches are typically used for harmonic rejection: a pre-filter stage (subsection 3.4.1) or a filter within the ATO closed loop (subsection 3.4.2). Being N the number of harmonics to be removed, a pre-filter stage configuration requires N notch filters while the filter in the ATO loop configuration requires  $2 \cdot (N + 1)$  filters. Therefore, a pre-filter configuration will be used as it is advantageous in this regard. Three notch filters (3.75), corresponding to  $\omega_3 = 3 \cdot \omega_0$  (150 Hz),  $\omega_5 = 5 \cdot \omega_0$  (250 Hz) and  $\omega_7 = 7 \cdot \omega_0$  (350 Hz), will be implemented.

$$NF_{\omega_n}(z) = b \cdot \frac{1 - 2 \cdot \cos(\omega_n) z^{-1} + z^{-2}}{1 - 2 \cdot b \cdot \cos(\omega_n) z^{-1} + (2 \cdot b - 1) z^{-2}}$$
(3.75)

$$\omega_n = \frac{2}{T_s} \cdot \tan\left(\omega_n \cdot \frac{T_S}{2}\right) \tag{3.76}$$

$$\omega_n = \frac{n \cdot \omega_0}{fs/2}; b = \frac{1}{1+k} \tag{3.77}$$

$$b = \frac{1}{1+k} \tag{3.78}$$

$$k = \frac{\sqrt{1 - A_{-3dB}}}{A_{-3dB}} \cdot \tan\left(\frac{BW}{2}\right) \tag{3.79}$$

$$BW = \frac{\Delta\omega}{fs/2} \tag{3.80}$$

#### 3.8.5 Phase delay compensator

The delay introduced by the filtering stage discussed previously can adversely impact the performance of the method, implementation of a phase delay compensation strategy being therefore required. The phase delay is estimated from the filter transfer function (3.75) in real time and later compensated (see Fig. 3.65). Substituting (3.81) into the notch filter transfer function, (3.75) is obtained. By separating the numerator and denominator of the filter transfer function into their real and imaginary components, (3.82), the notch filter phase delay at the grid frequency, D, is obtained using (3.83).

$$z = e^{j\omega_v T_s} \tag{3.81}$$

$$NF_{\omega_n} = \frac{real(num) + j \cdot imag(num)}{real(den) + j \cdot imag(den)}$$
(3.82)

$$D = \arctan\left(\frac{imag(num)}{real(num)}\right) - \arctan\left(\frac{imag(den)}{real(den)}\right)$$
(3.83)

## 3.8.6 Simulation results

Fig. 3.67 and Table 3.6 show the configuration used for the simulation of the proposed method. A programmable AC source is used to produce different disturbances in the grid voltage, including 1) grid voltage magnitude deviations, 2) grid frequency deviations and 3) harmonics. As already mentioned, the pre-filter stage was designed to reject the  $3^{rd}$ ,  $5^{th}$  and  $7^{th}$ harmonics, the magnitude of the disturbances have been selected to comply with the grid codes [11], [14], [12], [13], [5], [7], [10], [6], [3], [8], [1], [2], [9], [4] and [68].



Figure 3.67: FOAP-PLL control structure

Table 3.6:	Simulation	and	experimental	$\operatorname{setup}$	parameters	for	the	FOAP-CI	PLL
$\mathrm{method}$									

Symbol	Description	Value
$L_i$	Inverter-side inductance	2.196mH
$R_i$	Inverter-side resistance	$0.05\Omega$
C	Capacitor Filter	$10\mu F$
$R_c$	Capacitor ESR	$0.05\Omega$
$L_g$	Grid-side inductance	1.3mH
$R_g$	Grid-side resistance	$0.05\Omega$
$U_1$	Positive-sequence voltage magnitude (rms)	230 V
$\Delta \omega$	Notch filter bandwidth	10 Hz
$K_p$	ATO proportional gain	100
$K_i$	ATO integral gain	5000



Figure 3.68: Simulation results showing the response to a step-like change in the output voltage magnitude from 1 p.u. to 0.85 p.u at t=1s



(a) Input (v', Fig. 3.65) and output  $(v'_q, (b)$  phase delays (D (3.83), Fig. 3.65) Fig. 3.65) of the QSG extracted by the PDC.

Figure 3.69: Simulation results showing the response of the QSG and PDC blocks to a step-like frequency change from 50 Hz to 53 Hz in t=1 s



Figure 3.70: Simulation results showing the response to a step-like frequency change from 50 Hz to 53 Hz in t=1 s

In the simulation and experimental results following, magnitudes and frequencies are shown in per unit relative to the rated grid voltage and frequency (i.e. 220 V and 50 Hz).

Fig. 3.68 shows the simulation results when the AC source produces a step-like change in the output voltage magnitude. Fig. 3.68(a) shows both the grid voltage ( $v_g$  in Fig. 3.67) (black) and the voltage estimated by the proposed method ( $v_{\mu g}$  in Fig. 4) (red). Fig. 3.68(b)-3.68(d) show the magnitude, frequency and phase error. It is observed form Fig. 3.68(b) that the maximum magnitude error is 0.055 p.u., being below 0.03 p.u. in around 5 ms. Also, a maximum error in the estimated frequency of  $\approx 0.05 p.u.$  is observed (see Fig. 3.68(c)), which is compensated by the ATO PI controller after 5 ms. Finally, the maximum transient phase error is  $\approx 2$  degrees (Fig. 3.68(d)) which is also compensated by the ATO in less than 5 ms.

Figs. 3.69 and 3.70 show the simulation results for the case of a steplike frequency change. Fig. 3.69(a) shows the input and output signals to the QSG block, a 90 degrees phase shift between  $v'_q$  and v' is observed, independently of the input signal frequency.

Fig. 3.69(b) shows the phase shifts obtained by the PDC block for each



Figure 3.71: Simulation results showing the behavior of the PFS when  $3^{rd}$ ,  $5^{th}$  and  $7^{th}$  harmonics are added to the grid voltage at t=1s

notch filter and the total phase delay. The phase shifts agree with the predictions given by (3.83). It is observed that the resulting phase delay is frequency-dependent ( $\approx 2.1$  deg. at 50Hz and  $\approx 2$  deg. at 53 Hz), the nearer the notch frequency to the fundamental component, the bigger the phase delay that it produces.

Fig. 3.70(a) shows the grid voltage and estimated voltage. Small transient magnitude and frequency errors ( $\approx 0.02$  p.u. in Fig. 3.70(b),  $\approx 0.06$  p.u. in Fig. 3.70(c) respectively) are observed when the frequency changes, which fade away in less than three cycles of the fundamental voltage. It is finally observed from Fig. 3.70(d) that a maximum phase error of  $\approx 7.5$  deg. is obtained, which is corrected after 60 ms.

Figs. 3.71 and 3.72 show the simulation results when  $3^{rd}$ ,  $5^{th}$  and  $7^{th}$  harmonics are added to the grid voltage, all harmonics having a magnitude of 5% of the fundamental voltage (Table 3.6). Fig. 3.72(b) shows the output of the proposed PFS. It is observed that the disturbance due to the injected harmonics is compensated in less than two cycles of the fundamental component.

Fig. 3.72(a) shows the estimated grid voltage, the effects off the harmonics injected by the AC source being totally eliminated. Fig. 3.72(b) shows the amplitude of the error between the fundamental component of the grid voltage  $v_g$  and the estimated voltage  $v_{\mu g}$ . The error observed in the figure is due to the transient response of the PFS used to remove the grid disturbances. It has a maximum value of 0.18 pu, and is removed by the PFS after 50 ms. A similar behavior is observed for the frequency error (Fig. 3.72(c)), the maximum frequency error being 0.05 pu. Finally, the maximum transient phase error is smaller than 1 deg. (see Fig. 3.72(d)), being completely removed after 50 ms.



Figure 3.72: Simulation results showing the response when  $3^{rd}$ ,  $5^{th}$  and  $7^{th}$  harmonics are added to the grid voltage at t=1s

## 3.8.7 Experimental results

Fig. 3.73 and Table 3.6 show the experimental setup configuration and parameters. It consists of two single-phase voltage source converters (Master and Slave in Fig. 3.73). The master inverter is used to emulate a programmable AC source (see Fig. 3.67), while the slave inverter implements the proposed single-phase synchronization method. Rated power of both master and slave inverters is 50 kW, each inverter feeding a local resistive load of 30  $\Omega$ . The same tests used in simulation were repeated experimentally.

Fig. 3.74 shows the experimental results when the grid voltage magnitude



Figure 3.73: FOAP-PLL control structure



Figure 3.74: Experimental results showing the response to a step-like change in the output voltage magnitude from 1 p.u. to 0.85 p.u at t=1s

varies from 1 p.u. to 0.85 p.u. in t=1s. The PCC voltages are shown in Fig. 3.74(a), the magnitude, frequency and phase errors between the  $v_g$  and  $v_{\mu g}$  being shown in Fig. 3.74(b), 3.74(c) and 3.74(d) respectively. It is observed in Fig. 3.74(a) that the proposed method shows an excellent performance tracking changes in the magnitude. The magnitude error (Fig. 3.74(b)) has a peak value of  $\approx 0.08$  pu, being compensated after  $\approx 20$  ms. Frequency (Fig. 3.74(c)) and phase (Fig. 3.74(d)) errors are negligible. The differences between simulation (Fig. 3.68) and experimental (Fig. 3.74) results are due to the fact that the inverter used to produce the disturbances in the experimental setup implements voltage and current control loops, what limits the bandwidth of the disturbances.

Fig. 3.75 shows the experimental results when a frequency step-like change of the grid voltage occurs. Fig. 3.75(a) shows the actual and estimated voltage. A small peak magnitude error (i.e.  $\langle \approx 0.01 \text{ pu} \rangle$ ) is observed (Fig. 3.75(b)) at the instant of time in which the grid frequency changes, the peak grid frequency error being  $\langle 0.05 \text{ pu} \rangle$ . Both errors are corrected after  $\approx 10 \text{ ms}$  by the PLL-ATO.

A negligible phase error is observed in Fig. 3.75(d). Again the differences between the simulation and experimental results are due to the control



Figure 3.75: Experimental results showing the response to a frequency step-like change of the grid voltage  $v_q$  from 50 Hz to 53 Hz at t=1 s

bandwidth of the master inverter. It is noted in this regards that in a real scenario the grid frequency is not expected to change instantly due to the inertia of the power generators.

Finally, Fig. 3.76 shows the experimental results when  $3^{rd}$ ,  $5^{th}$  and  $7^{th}$  harmonics are added to the grid, the magnitude for each harmonic being 0.05 pu. It is observed in Fig 3.76(a) that the proposed method cancels the effects due to the harmonics. Similar as for the simulation results (see Fig. 3.70(b)), both the magnitude error (Fig. 3.76(b)) and the frequency error (Fig. 3.76(c)) show a an oscillating response produced by the PFS transient response, with a peak value <0.09 pu and <0.04 pu respectively, which fades away in  $\approx$ 50 ms.

It is finally observed that the phase angle error is almost negligible due to the low-pass behavior of the integrator used to extract the grid voltage phase angle. It can be concluded that there is a good agreement between simulation and experimental results.



Figure 3.76: Experimental results showing the response when  $3^{rd}$ ,  $5^{th}$  and  $7^{th}$  harmonics are added to the grid voltage at t=1s

## **3.9** Conclusions

This chapter has provided a review of the state-of-the art of grid synchronization techniques, both for single and three phase systems.

To overcome some of the limitations of existing single and three-phase grid synchronization techniques, three new methods have been proposed: a pre-filtering stage method (CCCF-CPLL) and a filter on the loop method (FOL-CPLL) for the case of three-phase systems, and a FOAP-CPLL for the case of single phase systems.

- CCCF-CPLL is a three-phase pre-filter stage method. The method improves some of the limitations of actual three-phase pre-filter stage methods. One strength of the proposed method presents is its high disturbance rejection capability, which is unafected by magnitude and frequency deviations. Additionally, it is simple and intuitive, with shows good dynamic response.
- FOL-CPLL is a three-phase filter on the loop method. Conceptually, the method is simpler than pre-filter stage methods, its tuning being also easier. Additionally, the method is frequency adaptive, with excellent disturbance rejection capability. Also, the error signal does not depends on the input signal magnitude.
- FOAP-CPLL is a single-phase, frequency adaptive, filter on the loop method. The method is based on the emulation a three-phase system from a single-phase signal by using a quadrature signal generator based on all-pass filters. It shows an excellent disturbance rejection capability and the error signal is independent of the input signal magnitude. A pre-filter stage is used to reject disturbances as well as a phase delay compensator is used to remove the delay introduced by the notch filters.

Two tuning methodologies of the controller gains have also been proposed, the results of the optimization parameters being shown in color maps. From these color maps its easy to get the optimal values and observe how sensitive the method is to different tunning parameters.

All proposed methods have been evaluated for six disturbances (including ramp like and step like variations) types to verify the validity of the proposed methods:

• Magnitude deviations from the grid rated value

- Frequency deviations from the grid rated value
- Unbalanced conditions
- Grid polluted with harmonic components
- Simultaneous magnitude and frequency deviations
- Simultaneous frequency deviations including harmonic components

## Chapter 4

# Islanding

## 4.1 Introduction

Microgrids could be understood as small-scale versions of the classical, large centralized electric distribution system, having the ability to operate connected or isolated from the utility grid, without affecting to the microgrid's loads (ideally). The interconnection of microgrids and/or distributed energy resources to the utility grid is regulated by local, regional and national authorities, while standardizing institutions (e. g. *Institute for Electrical and Electronic Engineers (IEEE)* or *International Electrotechnical Commission* (*IEC*)) publish standards and recommendations for interconnecting DPG units with the electric power systems. In all cases, each DPG unit is required to have the ability to detect if it is connected or disconnected from the utility grid, which is normally referred as islanding detection. Islanding situation can be caused by faults, accidental opening of the main switch that connects the microgrid/DPG and the main grid, human errors or nature causes.

Islanding detection standards require the islanding detection within a period of time after the islanding situation occurs, e.g. the IEEE-1547 [12], UL-1741 [6], IEC-62116 [3], AS-4777 [2] and IEEE-929 [5], requires islanding detection within 2 seconds after the islanding situation occurs. The German (DIN-VDE-0126) [8], Swiss [4] and Australian [2] standards established the grid impedance variation within a period of time as the islanding detection methodology; 1 Ohm in 2 seconds for the German standard and 0.5 Ohms in 5 seconds for the Swiss and Australian standards. Generally speaking, the faster the islanding situation is detected, the faster the control algorithms of all microgrid DPGs can be adapted, which is beneficial in terms of microgrid

stability and power quality.

This chapter makes an overview of islanding detection algorithms and discusses new techniques that overcome some of the limitations of existing islanding detection methods.

## 4.2 Islanding detection methods: an overview

Islanding detection methods can be classified into three major groups: passive, active and communication based methods.

## 4.2.1 Passive islanding detection methods

Passive islanding detection methods are typically based on monitoring variations of one or more microgrid variables, including PCC voltage, frequency, phase, total harmonic distortion (THD)....

## 4.2.2 Non-detection zone (NDZ)

A useful indicator to test the viability of a passive islanding detection method is the non-detection zone (NDZ). The NDZ is defined as a region of active and reactive power mismatch ( $\Delta P$  and  $\Delta Q$  respectively) where the islanding condition cannot be detected. The limits of the NDZ are based on the active (4.3) and reactive (4.4) power mismatch definitions shown in 4.1 and 4.2 respectively [ref SandiaLabs]. Note that UV and OV refer to under and overvoltage conditions respectively while UF and OV are the under and overfrequency conditions

$$P_{load} = P_{DPG} + \Delta P \tag{4.1}$$

$$Q_{load} = Q_{DPG} + \Delta Q \tag{4.2}$$

Fig. 4.1 shows the normalized (IEEE-1547 islanding detection test standard) islanding test circuit, where a RLC load, resonant at the fundamental grid frequency, is fed both by a DPG unit and the main grid. The DPG unit injects active ( $P_{DPG}$ ) and reactive power ( $Q_{DPG}$ ) to the load, the remaining active ( $\Delta P$ ) and reactive ( $\Delta Q$ ) power required by the load being imported from the grid.

$$UV \le \frac{\Delta P}{P_{DPG}} \le OV = \left(\frac{V}{V_{max}}\right)^2 - 1 \le \frac{\Delta P}{P_{DPG}} \le \left(\frac{V}{V_{min}}\right)^2 - 1 \quad (4.3)$$



Figure 4.1: Islanding generic setup

$$UF \le \frac{\Delta Q}{Q_{DPG}} \le OF = 1 - \left(\frac{f}{f_{max}}\right)^2 \le \frac{\Delta Q}{Q_{DPG}} \le 1 - \left(\frac{f}{f_{min}}\right)^2 \quad (4.4)$$

If the DPG unit is generating more active power than the load required active power ( $P_{DG} > P_{load}$ ), and an islading condition occurs, the voltage magnitude at the PCC will increase, inducing therefore an overvoltage situation (OV). Conversely, if the load demands more active power than the DPG can generate, the DPG will decrease its voltage and an undervoltage (UV) condition will be induced.

The same behavior is applied to frequency and reactive power variation. If the DPG is generating more reactive power than the load demands, and an islading condition occurs, the PCC voltage frequency will increase, reaching an overfrequency (OF) condition. On the other hand, if the load is importing reactive power from the grid and the breaker is opened, the PCC voltage frequency will start decreasing, reaching an underfrequency (UF) situation.

The worst case regarding not detecting the islanding condition occurs when the load power matches the DPG generated power ( $PQ_{load} = PQ_{DPG}$ ). Thus, when the microgrid is disconnected, the PCC voltage magnitude and frequency will not change.

Also small differences between the DPG generated power and loads consumption makes difficult to detect the islanding condition since produces small changes in the magnitude and frequency, which might remain within the grid code limits.

Passive islanding detection procedures found in the literature are introduced below.

Signal	Minimum	Maximum		
Frequency	49 Hz	51 Hz		
Magnitude	0.9 p.u.	1.1 p.u.		

Table 4.1: PCC voltage and frequency deviations by EN 50160 normative

#### 4.2.2.1 Grid voltage magnitude and frequency monitoring

As previously stated, all DPG units must implement over/under voltage protections (OVP/UVP) and over/under frequency protection (OFP/UFP). The grid voltage and frequency limits, according to EN 50160 normative, are summarized in Table 4.1. PLLs can be used to estimate the grid voltage magnitude and frequency (Chapter 3).

In addition to voltage and frequency normative limits, the islanding situation can be also detected based on the rate of change of voltage (ROCOV) and rate of change of frequency (ROCOF). ROCOV and ROCOF are typically negligible for grid-connected operation, while they can be noticeable in island operation.

One drawback associated to PCC voltage magnitude and frequency tracking methods is that there is that thew show large NDZ, these methods being considered in general inaccurate [72].

## 4.2.2.2 Phase jump detection

The phase jump detection method tracks the angle difference between the inverter output voltage and current. Commonly, an islanding condition induces a phase jump between the inverter output voltage and current due to a reactive power mismatch when the islanding condition occurs, the islanding situation being detected when a sudden jump occurs.

Typically, DPG units work in current control mode when they are connected to the grid. The DPG output current, at its filter output, is often in phase with the main grid voltage, since the inverter usually works with unit power factor. If the island condition occurs, the inverter output current remains unchanged due to the inductive nature of the output filter, while the output voltage could potentially change, as it is not longer fixed by the main grid. This phase change (phase jump) can potentially be used for islanding detection purposes. A practical solution to implement the phase jump detection is to use two PLLs in parallel, one with high bandwidth and other with low bandwidth (that filters out the phase jump). The phase shift between PLLs will be used for islanding detection purposes.

The NDZ of this technique is reduced, compared with grid voltage magnitude and frequency tracking methods, if the inverter is not working in unit power factor, but this is not advisable.

As a drawback, the threshold selection to prevent from erroneous islanding detection is not easy, specially if certain loads as motors are used, which can cause transient phase jumps that could lead to fake islanding detection.

#### 4.2.2.3 Harmonic identification

This method is based on monitoring e.g. the magnitude of a specific harmonic or the total harmonic distortion (THD) (4.5). Variation of such variables can be indicative of islanding.

$$THD_V = \frac{\sqrt{\sum_{h=2}^n V_h^2}}{V_1}$$
(4.5)

Ideally, a DPG unit, i.e. inverter, works as a current source injecting only a 50 Hz fundamental positive sequence component. However, the inverter also injects harmonic components due to the switching of the power modules (see subsection 2.2.2). Also, other harmonic sources, like non-linear loads, are connected to the PCC.

The PCC voltage harmonics depends on the grid impedance and the current harmonics injected by the inverter. In grid connected mode, the grid impedance is relatively small, the PCC voltage being therefore mainly composed by the fundamental component, with a small harmonic content, i.e. small THD. When the inverter is islanded, the inverter current harmonics will produce higher PCC voltage harmonics than in grid connected mode. Thus, the inverter can detect the islanding condition by monitoring the PCC voltage THD.

Strong points of this method are that it requires low computational requirement, it does not pollute the grid and theoretically its NDZ is zero since it does not depend on the power mismatch between the DPG and the grid. However, it also has some drawbacks. Connection or disconnection of nonlinear loads may change the THD, erroneous islanding situation could be detected if the threshold is not properly set. Also if a RLC load connected to the PCC shows an important low-pass behavior, the viability of the method will be compromised.

## 4.2.3 Active islanding detection methods

Active islanding detection methods inject a small perturbation, the grid response being used to decide if the inverter/microgrid is connected to the grid or not. Three main perturbations have been traditionally used: output frequency/phase perturbation, magnitude perturbation and harmonic (or harmonics) injection.

#### 4.2.3.1 Frequency perturbation methods

This islanding detection technique is based on the change of the grid frequency. Among the are various frequency perturbations that have been proposed, the active frequency drift (AFD), the slip mode frequency shift (SMS) and the sandia frequency shift (SFS) are discussed following.

## 4.2.3.1.1 Active frequency drift (AFD) method

The AFD method is based on introducing a zero current segment, changing the grid frequency to be 0.5-1.5 Hz higher than the main grid frequency. Being  $T_{grid}$  the period of the grid voltage and  $T_{AFD}$  the period of the AFD signal (i.e. some Hz lower than the grid frequency), during a time  $T_{grid} - T_{AFD}$ the inverter injects zero amps, until the grid voltage crosses zero. This is shown in Fig. 4.2.

When the AFD method is applied to an islanded passive load, its voltage will reach the zero crossing before expected, increasing the voltage frequency. The AFD method is easy to implement, but its NDZ is relatively large compared to other active methods. It is found that the method is not particularly effective in a real scenario [72]. Also there must be an agreement between the manufacturers in order to make a positive or a negative frequency drift in case of a multi-inverter scenario.

## 4.2.3.1.2 Slip mode frequency shift (SMS) method



Figure 4.2: AFD waveform example

SMS method shift the phase of the output inverter voltage (and thus the short term frequency). When the DPG is in grid connected mode, this has no effect as the frequency (and phase) will be fixed by the utility grid. On the contrary, when the DPG is islanded, the perturbation will produce a measurable frequency change. A typical SMS phase has the form of (4.6), where  $\theta_m$  is the maximum phase shift that occurs at the  $f_m$  frequency,  $f_n$  is the nominal frequency and  $f^{(k-1)}$  is the frequency in the previous cycle of the fundamental component.

$$\theta_{SMS} = \theta_m \sin\left(\frac{\pi}{2} \frac{f^{(k-1)} - f_n}{f_m - f_n}\right) \tag{4.6}$$

One of the main advantages of SMS is that it has a very small NDZ. In addition, SMS is simple to implement, since only small modifications in the DPG control are required, its use being feasible in a multi-inverter scenario. The drawback of the SMS method is that it cannot detect the islanding condition when loads with a high quality factor and a resonant frequency close to the line frequency are connected to the PCC.

## 4.2.3.1.3 Sandia frequency shift (SFS) method

SFS is an extension of the AFD method. The SFS method aims to vary the grid frequency in order to detect the islanding situation.
The SFS method changes the grid frequency by a term that that follows 4.7, where f is the inverter terminal voltage,  $f_n$  is the nominal frequency (50 Hz), K is the positive feedback gain, and  $cf_n$  is the initial chopping fraction [72].

$$\theta_f = \frac{\pi}{2} \left( cf_n + K \left( f - f_n \right) \right) \tag{4.7}$$

When the inverter is disconnected from the main grid, as f increases, the frequency error increases. At the same time, the chopping fraction increases which will make the inverter to increases its frequency. The inverter therefore acts to reinforce the frequency deviation. This process continues until the frequency reaches the threshold of the over frequency protection.

This method is easy to implement, showing one of the smallest NDZs of all the active islanding detection methods. Also, as SFS and SMS, provides a good compromise between islanding detection capabilities, output power quality and transient response. This method was found to work properly with current control inverters, but was found to be inappropriate for constant power inverters [72].

#### 4.2.3.2 Sandia voltage shift (SVS) magnitude perturbation method

The sandia voltage shift (SVS) method is a magnitude perturbation islanding detection technique that uses feedback to increase or decrease the PCC voltage magnitude. When the inverter is grid connected, the inverter cannot change the PCC voltage magnitude, while if it is disconnected from the utility grid, the inverter can decrease (also increase) the PCC voltage magnitude (Fig. 4.1).

The SVS method is easy to implement and works well in a multi-inverter scenario; it is believed to be one of the most effective methods, being commonly implemented together with a frequency perturbation method, e.g. the SFS method.

A drawbacks of the method is the adverse impact on the PCC voltage distortion.

#### 4.2.3.3 Harmonic injection methods

Harmonic injection methods are based on the injection of a harmonic component at an specific frequency to estimate the grid/microgrid impedance. When the inverter is connected to the utility grid, the estimated high frequency impedance magnitude is very low and typically inductive. On the contrary, when it is disconnected from the utility grid, the estimated high frequency impedance is typically increased. Islanding condition is detected therefore from the impedance variation, either magnitude or phase.

Strengths of this method is that it does not depend on the power mismatch between the DPG and the grid, showing therefore a negligible NDZ. Also, the high frequency impedance is relatively easy to estimate.

Harmonic injection method shows some drawbacks. Connection or disconnection of nonlinear loads may produce transient harmonics, interfering with the measurement of the high frequency impedance, eventually producing erroneous islanding detection. Thus, non-characteristic harmonics may be injected in order to deal with this issue. In addition, implementation of the method can be difficult in a multi-inverter scenario. Multiple inverters injecting the same harmonics may interfere with each other, resulting in erroneous islanding detection.

# 4.2.4 Communication-based islanding detection methods

Communication based islanding detection methods are based on some type of data-sharing between the main grid and the inverter, they are briefly discussed following.

#### 4.2.4.1 Power Line Communication (PLC) methods

PLC methods are based on the propagation of a carrier signal through the transmission lines. A dedicated equipment, called modulator, is placed into the grid-side and is used to superimpose a specific type of signaling to the grid voltage. This signal is therefore broadcasted to all DPGs into a specific area or microgrid. Each DPG is equipped with a demodulator that track the signal. If the inverter does not receive the signal, it means that it is operating in islanded mode.

This method is simple and reliable. In a radial system, only one transmitting generator would be needed. However, PLC methods need extra communication equipment. Also its applicability is reduced in non-radial systems, where more than one modulator might be required. Finally, the method requires the collaboration of grid operators to be implemented. To overcome these limitations, a dedicated communication line can be used. Typical communication channels as microwave links, telephone lines or mobile communications can be used for that purpose. They provide high efficiency, but increases the cost.

#### 4.2.4.2 Supervisory control and data acquisition (SCADA)

The basic idea of this scheme is to monitor the status of all the circuit breakers that could isolate a part of the distribution system. When a circuit breaker is open, a centralized control system determines which areas are islanded and sends the appropriate signal to the DPGs, to either remain in operation, or to turn off. SCADA based methods have theoretically no NDZ. Its weaknesses are the increased complexity and cost in large microgrids.

# 4.2.5 Summary

Table 4.2 summarizes the main characteristics of the islanding detection techniques that have been reviewed.

Generally speaking, passive detection methods are easy and cheap to implement, but show a noticeable NDZ. They can accurately detect the islanding situation in the event of large mismatches between power generation and power demand. PCC voltage magnitude, frequency and phase, also harmonic components or THD, can be used to detect islanding.

Active islanding detection methods show negligible NDZ, but introduce some type of disturbance in the PCC voltage. The use of active islanding methods must be carefully used in a multi-inverter scenario, since the THD must be controlled, also interference between inverters could occur. Magnitude and frequency perturbations, as well as harmonic injection, are commonly used to detect the islanding condition.

Communication based methods show zero NDZ and do not introduce any disturbance in the grid if a dedicated communication channel is used. If power line communications are used, the PCC voltage is distorted. With the introduction of communication between DPGs, the drawback of the costs associated to due to this equipment is overcomed, since communications are nowadays used for dispatchability issues, activation or deactivation of DPG units...

In the following sections, a group of islanding detection methods are proposed that overcome many of the limitations of existing methods, regarding the reduction of the NDZ, reduction of the adverse impact on the power quality, and viability in multi-inverter scenarios.

Name	Type	Strengths	Weakesses
Mag. & Freq. Tracking	Passive	-Easy to implement -Grid friendly	-Large NDZ
Phase Jump	Passive	-Easy to implement	-Large NDZ
Detection		-Grid friendly	-Threshold selection
Harmonic	Passive	-Grid Friendly	-Use with
Identification		-Zero NDZ	nonlinear loads
			-Threshold selection
Frequency	Active	-Easy to implement	-Threshold selection
perturbation		-Multi-inverter	-Pollutes PCC
Magnitude perturbation	Active	-Easy to implement -Zero NDZ	-Reduces inverter
			efficiency
			-Pollutes PCC
			-Use with
Harmonic	Active	-Easy to implement	nonlinear loads
injection		-Zero NDZ	-Conflicts in
			Multi-inverter
Power Line	Communic.	-Easy to implement	-Costs
Communic.		-Zero NDZ	-Pollutes PCC
SCADA	Communic.	-Easy to implement	-Costs
		-Zero NDZ	-Complexity

Table 4.2: Islanding detection techniques summary

# 4.3 Islanding detection in three-phase systems rotating using high-frequency signal injection

Active islanding detection based on the injection of a rotating high frequency signal voltage is proposed in this section. Advantages of the method include almost negligible adverse effects due to the injected high frequency voltage, as well as accurate and fast islanding detection.

# 4.3.1 Islanding detection using high frequency signal injection.

The high frequency impedance has been shown to be a reliable metric for islanding detection purposes [72]. Voltage source inverters (VSI) can easily inject a low-magnitude and high-frequency voltage, from which the high frequency impedance can be estimated. While a large variety of high frequency excitation waveforms can be used, the rotating and pulsating voltage signals results in simple implementations, both options are discussed following.

#### 4.3.1.1 Rotating high frequency signal injection

When a three-phase, linear system, is exited with a high frequency voltage of the form (4.8), the induced high frequency current is (4.9). An estimation of the high frequency impedance can be obtained as (4.10), with its phase angle being (4.11).

$$u_{dqhf} = U_{hf} e^{j\omega_{hf}t} \tag{4.8}$$

$$i_{dqhf} = \frac{U_{hf}}{Z_{dqhf}} e^{j(\omega_{hf}t - \phi_Z)}$$

$$\tag{4.9}$$

$$Z_{dqhf} = R_{hf} + j\omega_{hf}L_{hf} = \frac{u_{dqhf}}{i_{dqhf}}$$
(4.10)

4.3 Islanding detection in three-phase systems rotating using high-frequency signal injection 127



Figure 4.3: Classical architecture connecting a microsource to a grid/microgrid

$$\phi_Z = a \tan\left(\frac{\omega_{hf} L_{hf}}{R_{hf}}\right) \tag{4.11}$$

where  $\omega_{hf}$  is the frequency of the injected signal,  $U_{hf}$  is the voltage magnitude of the injected high frequency signal,  $i_{dqhf}$  is the induced high frequency current,  $Z_{dqhf}$  is the high frequency impedance,  $\phi_Z$  is the phase angle of the high frequency impedance  $R_{hf}$  and  $L_{hf}$  are the high frequency resistance and inductance respectively.

One important issue that needs to be considered is the effect of the output filter of the VSI on the estimated high frequency impedance. Fig. 4.3 shows the classical architecture for connecting a DPG unit to a grid/microgrid. As previously said, the current sensors necessary to implement the VSI current control are place at the inverter side. The output filter current can be either measured or estimated, knowledge of the LCL filter parameters being needed in the second case.

If the inverter output current is measured, the high frequency impedance estimated from the measurement is the combined impedance of the microgrid and/or grid impedance and the output filter. If the current is measured at the inverter-side (see Fig. 4.3) and an LCL filter is used, the output current of the LCL filter can be estimated from (4.12), the microgrid and/or the grid impedance being obtained as (4.13). This avoids therefore the use of additional current sensors at the filter output.

$$i_{dq\mu ghf} = \frac{u_{dqhf1} - u_{dq\mu ghf} - j\omega_{hf}L_1 i_{dqhf}}{j\omega_{hf}L_2}$$
(4.12)

$$Z_{dq\mu ghf} = \frac{u_{dq\mu ghf}}{i_{dq\mu ghf}} \tag{4.13}$$



Figure 4.4: d (blue) and q (red) axis complex vector components of the measured voltage  $u_{dq\mu q}$ 

where  $u_{dqhf1}$  is the commanded high frequency voltage,  $u_{dq\mu ghf}$  is the measured high frequency voltage at the filter output,  $L_1$  is the inverter side inductance filter and  $L_2$  is he microgrid side inductance filter.

To illustrate the principle of operation of the proposed method, a simulation of a transition from grid connected mode to island condition of a VSI (see Fig. 4.3) is shown in Fig. 4.4. A high frequency voltage of magnitude 5 V and frequency 333 Hz is superposed to the fundamental voltage, Fig. 4.4(a) and 4.4(b) showing the q and d-axis components of the voltage and current vectors (the high frequency portion being practically imperceptible due to its reduced magnitude). Fig. 4.4(c) and 4.4(d) show the q and d-axis components of the high frequency voltage and current vectors, obtained by digital filtering of the measured variables shown if Fig. 4.4(a) and 4.4(b). Islanding occurs at t = 1s, the differences in the high frequency voltages and currents, and consequently in the high frequency impedance, between island and grid modes are evident. This supports therefore the validity of the proposed method.

#### 4.3.1.2 Pulsating high frequency signal injection

An alternative form of high frequency excitation is the pulsating voltage vector (4.14). The high frequency current induced for this case is (4.15), the high frequency impedance being (4.16). As for the rotating high frequency signal injection, the effect of the output LCL filter can be decoupled using (4.12) and the microgrid and/or grid impedance being obtained from (4.13).

$$u_{dqhf} = U_{hf} \cos(\omega_{hf} t) = \frac{U_{hf}}{2} e^{j(\omega_{hf} t)} + \frac{U_{hf}}{2} e^{j(-\omega_{hf} t)}$$
(4.14)

$$i_{dqhf} = \frac{U_{hf}}{Z_{dqhf}} \cos(\omega_{hf}t - \phi_Z) = \frac{U_{hf}}{2Z_{dqhf}} e^{j(\omega_{hf}t - \phi_Z)} + \frac{U_{hf}}{2Z_{dqhf}} e^{j(-\omega_{hf}t + \phi_Z)}$$

$$(4.15)$$

$$Z_{dqhf} = \frac{e^{j(\omega_{hf}t)}U_{hf}/2}{e^{j(\omega_{hf}t-\phi_Z)}U_{hf}/2Z_{dqhf}} = \frac{e^{j(-\omega_{hf}t)}U_{hf}/2}{e^{j(-\omega_{hf}t+\phi_Z)}U_{hf}/2Z_{dqhf}}$$
(4.16)

Both rotating and pulsating high frequency injection methods respond to the same physical principles and are expected therefore to provide similar overall performance. Only rotating high frequency injection is discussed in this section. A following section includes the analysis of pulsating high frequency injection.

### 4.3.2 Multi-inverter operation

In a general multi-inverter setup, two different scenarios can be followed in order to inject the high frequency signal: all of the participants in a microgrid can inject it or only one inverter, usually referred as master inverter, injects the high frequency signal and gives advice to the rest of inverters when the islanding situation is detected. In a the first case the risk of interference among inverters exists and it is undesirable to provide an accurate islanding detection technique.

Generally speaking, it is attractive that only the master generator injects (See Fig. 4.5) the high frequency signal to detect the islanding situation. In the case that more than one DPG unit has the capability of injecting the high



Figure 4.5: Generic microgrid architecture and sequencing of the high frequency signal injection.

frequency signal, strategies to avoid interferences between the micro-sources need to be implemented [16].

To avoid interference, the injection of a second high frequency signal for communication purposes is proposed. The islanding situation is only detected by the master inverter of the microgrid (See Fig. 4.5) by means of the primary high frequency signal  $(u_{dqhf1})$ . When the master inverter detects islanding situation, it injects a secondary high frequency signal  $u_{dqhf2}$  (see Fig. 4.5). This secondary high frequency signal is detected by other inverters in the microgrid that need to adapt their working mode to the new situation (power sharing, power demand, power generation capabilities, ...) of the grid.

## 4.3.3 Simulation results.

To validate the proposed method, the simulation scenario is shown in Fig. 4.5 will be used. The main parameters are shown in Table 4.3.

Fig. 4.6(a) and 4.6(b) show the magnitude and phase of the estimated high frequency impedance by the master inverter, during a transition from

Parameter	Value
Grid	380V, 50Hz, Scc=15MVA
Master inverter, inverter 1, 2 and 3	380V, 5kHz.
Load $1,2,3$ and $4$	10kW
Line impedance	11.7mOhm, 8.68e-4H
Simulation step	1e-5s
udqhf1	0.03pu, -333Hz
udqhf2	0.03pu, 275Hz
PI Current regulator gains:	Kp=0. 8, Ki=200
LPF bandwidth	25 Hz
HPF bandwidth	25 Hz
LCL filter resonance frequency	575 Hz

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grid connected to island (t=1s) and from island to grid connected (t=2s). Fig. 4.6(c) shows the commanded high frequency voltage  $(u_{dqhf2})$  and the measured high frequency voltages by inverters 1, 2 and 3. Fig. 4.6(d) shows the magnitude of the second high frequency current measured by inverters 1, 2 and 3 due to the injection by the master inverter of the high frequency voltage  $u_{dqhf2}$ .

 Table 4.3: Simulation setup parameters

It is noted from Fig. 4.6(c) and 4.6(d) that the magnitude of both the measured high frequency current and voltage decreases as the distance to the master inverter increases. This behavior could compromise the reliability of the proposed method if the magnitude of the high frequency current/voltage becomes to small to be reliable detected by one or more microgrid inverters placed in critical points of the microgrid. One potential solution to this problem is that inverters detecting the secondary high voltage inject current in order to restore the magnitude of the high frequency signal.

### 4.3.4 High frequency signal selection.

Several issues need to be considered for the selection of the magnitude  $U_{hf}$  and the frequency  $\omega_{hf}$  of the high frequency voltage.

The magnitude of the high frequency voltages  $u_{dqhf1}$  is limited in first



(a) Estimated high frequency impedance magnitude



(c) measured high frequency voltages



(b) Estimated high frequency impedance phase



(d) Measured high frequency current magnitudes. Uhf1=5V,  $\omega hf1=-333$ Hz, Uhf2=5V,  $\omega hf2=303$ Hz.

Figure 4.6: Simulation results.

instance by connection standards [11], [14], [12], [13], [5], [7], [10], [6], [3], [8], [1], [2], [9], [4] and [68], since the injected high frequency signal increases the THD and might create power quality concerns. The magnitude of  $u_{dqhf2}$  is determined by the microgrid structure, to ensure that the resulting signal magnitude (voltage or current) available on each inverter is higher enough to be detected.

For the frequency selection, several aspects need to be taken into consideration:

- 1. The high frequency signal could interact with the filter resonant frequency, which for the case of LCL filters (see Fig. 4.3 and 4.7) is typically in a range of one tenth of the switching frequency and ten times the fundamental frequency [85]. For the experimental results presented in the next section, the switching frequency is 10 kHz. Therefore, the resonant frequency of the LCL filter should be in a range of 500 Hz to 1 kHz. A value of 575 Hz was chosen.
- 2. Current regulated VSI could react (and partially compensate) to the induced high frequency current injected either for island detection or for communication. The effects of this reaction will depend both on the frequency of the injected signal and the bandwidth of the current regulators, as well as on the grid characteristics. A mean to prevent from this to happen is by means of a band-stop filter in the current feedback, tuned for to reject the frequency of the injected signals (333 Hz for the results presented in this paper, see Fig. 4.7). Fig. 4.7 shows the master inverter control block diagram. It is observed from the figure that the high frequency signal injection is superimposed to the fundamental excitation.

It is not possible therefore to obtain a general model able to predict the impact of a current regulated VSI on the high frequency signal. However, simulations performed using the configuration shown in Fig. 4.5 showed that the method worked adequately even in the presence of current regulated VSI.

As for the high frequency signal used for communications purposes, the use of a band-stop filter in the current feedback of the master inverter is recommended, but is not required in the remaining inverters connected to the grid.

3. Both high frequency signals  $u_{dqhf1}$  and  $u_{dqhf2}$ , can have positive or negative frequencies, as they are complex vectors. In general, these



Figure 4.7: Master inverter control block diagram.



Figure 4.8: Estimated high frequency impedance magnitude (a)) and phase (b)). Positive sequence impedance in island ( $\diamond$ ) and grid connected condition ( $\Box$ ), negative sequence impedance in island ( $\lhd$ ) and grid connected conditions ( $\times$ ). Uhf =1.5V.

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signals should be chosen to be spectrally separated from harmonics of the fundamental frequency (e.g.  $-5^{th}$ ,  $7^{th}$ ...) typically occurring e.g. due to non linear loads. Fig. 4.8 shows the estimated high frequency impedance magnitude and phase for island and grid connected conditions for positive and negative sequence signals in a frequency range from 300 to 420 Hz. It can be observed that the island/grid-connected situation could be detected using either positive or negative sequence signals for this case.

- 4. Special care should be taken if active power filters (APFs) are present in the microgrid, since the APF control could react to the injected high frequency signal. Typically APFs compensate specific harmonics which are integer multiples of the fundamental frequency [39], [88] and [135]. To avoid possible interaction between the injected high frequency signal and the APFs, a high frequency signals used for islanding detection and communications should be chose not to coincide with those characteristics frequencies.
- 5. The high frequency signal could interact with the grid resonance frequency that can vary in a large range depending on the grid topology, transmission lines... [129], it is therefore difficult to reach general conclusions in this regard.
- 6. The use of capacitor banks that might exist in microgrids for reactive power compensation purposes could potentially decrease the reliability of the method, as they would affect to both the magnitude and phase of the microgrid high frequency impedance. Generally speaking, the capacitor banks will decrease the overall magnitude of the microgrid high frequency impedance while they increase the microgrid power factor. If only the magnitude is used, the effects of a capacitor bank could compromise the reliability of the method (if the microgrid high frequency impedance magnitude becomes close to the grid high frequency impedance magnitude), however, if the phase is also used, the increase of the power factor would allow to distinguish the effect of the capacitor banks from the effects of the low grid impedance.

# 4.3.5 Experimental results.

Fig. 4.9 shows the experimental setup that will be used to validate the proposed method. A 100kVa, 380V diesel generator was used as the primary



Figure 4.9: Experimental setup.

power source. The short circuit power of the grid is 2MVA. The rated parameters of the inverters are 30kVA and 380V, with a switching frequency of 10 kHz. A DSP (*TMS320F28335*) has been used for its control. Voltage sensors in the grid side were used for synchronization between the microgrid and the main grid and for power control purposes. Three different loads were connected to the microgrid: 2.5kW (pure resistive), 11kVA with a power factor of 0.9 and 14kVA with a power factor of 0.96.

Fig. 4.10 and 4.11 show the magnitude and phase of the estimated high frequency impedance (4.13) for different frequencies of the injected high frequency voltage  $(u_{dqhf1})$  (4.8), both in island and grid connected operation. The high frequency voltage magnitude of  $u_{dqhf1}$  was set to 1.5V (peak), which corresponds to  $\approx 0.3\%$  of the line-to-line voltage. It can be observed from Fig. 4.10 that, as expected, the magnitude of the estimated high frequency impedance decreases for grid connected operation compared to island operation. Fig. 4.11 shows the phase-angle of the estimated high frequency impedance, which is seen to be larger (more inductive) for grid operation than for island operation, the reason being that the short-circuit high-frequency impedance of the grid is near purely inductive.

Fig. 4.12 shows the transient behavior of the high frequency impedance estimation using the block diagram shown in Fig. 4.7. Islanding detection standards require the detection of a variation of the impedance within a period of time, e.g. 1 Ohm increase in 5 seconds, 0.5 Ohms in 5 seconds 0.5 Ohms in 2 seconds. It is observed that the estimated high frequency impedance is available after  $\approx 18$  ms. It is concluded from the experimental results that both requirements are widely met by the proposed method.

One important issue for the implementation of the method is whether the injection of the high frequency signal is continuous or intermittent. Continuous injection allows almost instantaneous detection of the island or grid



Figure 4.10: Experimentally measured magnitude of the high frequency impedance, in island (top-surface, black) and grid connected (bottom–surface, red) operation for different frequencies of the injected high frequency signal and different load levels. Uhf1 = 1.5V.



Figure 4.11: Experimentally measured phase of the high frequency impedance, in island (bottom-surface, black) and grid connected (top-surface, red) operation for different frequencies of the injected high frequency signal and different load levels. Vhf1=1.5V.



Figure 4.12: Transient for the estimation of the high frequency impedance from grid connected (t<5.8s) to island operation (t>5.8s). Uhf1 = 1.5V,  $\omega_{hf1} = 333Hz$ .

condition, but at the price of a slight increase of the THD, which might need to be taken into consideration to meet the connection requirements. Fig. 4.13 shows the current complex vector spectrum when both the fundamental and the high frequency signals are present. The total harmonic distortion when the high frequency signal is not injected is  $\text{THD}\approx 2.72\%$  while an increase of  $\approx 0.11\%$  (THD $\approx 2.83\%$ ) is observed when the high frequency signal is injected. Alternatively, intermittent injection can be used [83][70] and [16], for this case changes between island and grid modes can only be detected when the high frequency signal is injected. Another issue for intermittent injection is the time that is needed for the transient response of the resulting high frequency current to fade away (due both to systems time constant as well as to digital signal processing time constant) before the measurement can be made. Fig. 4.14(b) shows the transient response of the high frequency current when a high frequency voltage step is applied (Fig. 4.14(a) shows the commanded voltage), the high frequency current reaches its steady state value in 6 ms approximately (2 cycles of high frequency signal). This means that if intermittent signal injection is used, only a few ms are needed to estimate the high frequency impedance (see Fig. 4.12).

An estimation of the benefits of intermittent vs. continuous high frequency signal injection in terms of THD decrease can be made by considering how often and how long the high frequency signal should be injected for the case of intermittent signal injection. E.g., VDE-0126, requires detection of islanding in 2 seconds. Assumed that the high frequency signal is injected for  $\approx 0.025$ s, which includes time needed for the signals to reach steady state 4.3 Islanding detection in three-phase systems rotating using high-frequency signal injection 139



Figure 4.13: Microgrid current complex vector spectrum. The fundamental component is out of range to better show the high frequency signals, having a value of 10.6A, Load= 5kVA, Uhf1 = 1.5V,  $\omega_{hf1} = 333Hz$ .



(a) High frequency voltage: Vhf1=1.5V,  $\omega hf1=333Hz$ 

(b) Induced high frequency current

Figure 4.14: High frequency current transient response.

and the further signal processing, the high frequency signal would then be injected in the range of 1.25% of the time. Since the increase of the THD due to continuous injection is 0.11%, the average THD increase with intermittent injection would be as low as 0.0014%, but with an instantaneous value of 0.11% when the high frequency voltage is being injected.

Fig. 4.15(a) and 4.15(b) show the estimated high frequency impedance magnitude and phase in a transition form grid connected (t=8s) to island situation and from island situation (t=12s) to grid connected. Fig. 4.15(c) shows the commanded magnitude of  $u_{dqhf1}$  when it is continuously injected for island detection purposes, as well as the magnitude of the high frequency voltage  $u_{dghf2}$ , which is injected only by the master inverter when island situation is detected, to forward the island condition to other inverters connected to the microgrid (See Fig. 4.9). It is noted by comparing Figs. 4.15(a)-4.15(c) that there is a slight delay between the transition either from grid connected to island or from island to grid connected, and the injection of  $u_{dqhf2}$ . This is due to the use of a threshold for the detection of islanding or grid connected condition. The magnitude of the high frequency impedance has been used for the experimental results shown at Fig. 4.15. The threshold could be set to be in the middle of the high frequency impedance for island operation and for grid connected operation. However, this option might not accomplish in practice with the islanding detection standards, which require the detection of grid impedance magnitude changes within a certain period of time. Instead, the threshold is selected based on the magnitude changes established by the standards, a hysteresis is included to make the method robust against false alarms (see Fig. 4.15(a)).

In addition to the use of a threshold, only when the signal used for islanding detection surpasses the threshold for a time longer the established minimum time, detection of island/grid condition is fully effective. The selection of an adequate minimum time will depend on several factors as noise or transient behavior of the microgrid loads. The minimum time for the experiments carrier out for this paper has been established in 200 ms (Fig. 4.15). However, this choice was made ad-hoc, deeper analysis of this issue being a potential subject for future research.

Fig. 4.15(c) and 4.15(d) shows the magnitude of  $u_{dqhf2}$  and  $i_{dqhf2}$  that are measured by inverter2. Both signals can be used by inverter2 to detect the island condition.

Finally, the computational requirements of the proposed method are of  $8.2\mu$ s in the signal processor used in the experimental setup. This computational burden makes feasible to implement the proposed algorithms in





(a)Estimated high frequency impedance magnitude



vdqhf2 (green) magnitude by inverter2

1 € 0.5 0

impedance phase



Figure 4.15: Experimental results.

 $\omega hf 2 = 303 \text{Hz}.$ 

already existing digital signal processors.

# 4.4 Islanding detection using high frequency signal injection, current cancellation and dynamic master role assignment

It has been shown in the previous section that interference between converters can occur if multiple inverters in a microgrid or in a grid have the capability of injecting a high frequency signal for islanding detection purposes.

This section proposes a method for islanding detection using high frequency signal injection in grids with multiple parallel-connected inverters. In the proposed method, inverters dynamically respond to changes in the grid (e.g. failure of the master inverter, change from island to grid-connected or from grid-connected to island, ...) automatically reassigning the masterslave roles, without the need of communications. To coordinate the actions of the inverters present in the grid, the proposed method implements two distinguishing features:

- Slave inverters work in a high frequency current cancellation mode. This mode of operation prevents the reaction of the slave inverters against the high frequency signal voltage injected by the master, still keeping full capability of fast and accurate islanding detection.
- In the case of master failure, or significant changes in the grid, the remaining inverters will dynamically reassign roles, the new master inverter being self-selected based on a deterministic performance criteria and without the need of communication.

# 4.4.1 Islanding detection using high frequency voltage injection and high frequency current cancellation

It has already been shown that islanding detection in inverter-based DG can be done by measuring the grid response to a high frequency signal voltage injection. While the implementation of this method is relatively simple when there is a master inverter that injects the high frequency signal (see Fig. 4.16), interferences can occur if multiple inverters connected in parallel do the same, strategies to prevent from this to happen being needed in this case

In the method described in this section, the master inverter continuously injects the high frequency signal voltage udqhf1 used for islanding detection



Figure 4.16: Generic microgrid architecture.



Figure 4.17: Control block diagram of the master inverter.

(4.8) (see Figs. 4.17 and 4.18), the master inverter using a high frequency impedance variation criteria (4.10) to detect islanding. The high frequency impedance is estimated using the measured LCL filter high frequency output voltage  $u_{dq\mu ghf}$  and the estimated LCL filter high frequency output current (4.12).

To prevent the reaction of slave inverters against the high frequency current, they include a PI current regulator in a reference frame synchronous with the injected high frequency voltage  $\omega_{hf}$  (4.17). This current regulator sees the high frequency current at the inverter LCL filter output as a DC signal. By making its command equal to zero, it is guaranteed that no high



Figure 4.18: Master-role assignment transient

frequency current exists at the inverter output (see Fig. 4.19).

$$G_{HFCR} = k_p \left( 1 + \frac{k_i}{s} \right) \tag{4.17}$$

This mode of operation for the slave inverters is called *infinite impedance* mode. In this mode of operation, slave inverters detect islanding/grid connected condition from the changes in the high frequency current regulator output voltage. It is noted that both the output current of the inverter and the output voltage of the LCL filter are normally available in inverter-based DG, no additional sensors are therefore needed to implement this method. It is also important to notice that since no high frequency current exists at the slave inverters output, it will be the high frequency voltage command (i.e. the output of the high frequency current regulator in Fig. 4.19) the variable reflecting the grid connected/islanding condition.

This strategy has several appealing properties. The high frequency signal voltage injected by the master inverter is not corrupted due to the reaction of other inverters in the grid, as no high frequency current flows through them. This also prevents interference between inverters since only the master inverter injects the high frequency signal. It is finally noted that though the proposed strategy is described for current regulated VSI inverters using an LCL filter, it can also be implemented on inverters using other filter designs like inductive filters.

To evaluate the proposed method, a scenario with three parallel-connected converters -a master and two slave inverters-, has been built as an example (Fig. 4.20). The simulation parameters are summarized in Table 4.4. Fig. 4.21 shows the simulation results. The master inverter continuously injects the high frequency voltage (udqhf1, see Table 4.4), the estimated magnitude and phase of the high frequency impedance being shown in Fig. 4.21(a) and



Figure 4.19: Slave inverter control block



Figure 4.20: Simulation scenario

4.21(b) respectively. Transition from island to grid-connected and from gridconnected to island occur at t=3.5 s and t=5.5 s respectively. It is observed from Fig. 4.21(a) and 4.21(b) that the changes in the magnitude and phase of the high frequency impedance allow reliable island/grid-connected detection

Fig. 4.21(c) shows the magnitude of the high frequency current regulator output voltage ( $|u_{dqhf}^*|$ , see Fig. 4.19) for the two slave inverters (inverters 1 and 2 in Fig. 4.20). It can be observed that the high frequency voltage dramatically decreases when the microgrid becomes connected to the main grid. This is due to the variation of the high frequency impedance between island and grid connected condition. While in island condition the overall microgrid high frequency impedance corresponds to the local loads, and can be relatively large, in grid connected condition the overall high frequency impedance is dominated by the grid impedance, which is normally significantly smaller.

This high frequency impedance change produces a variation of the high

Parameter	Value
Grid	380 V, 50 Hz, Scc=15 MVA
Master inverter, inverter 1, and 2	380 V, 10 kHz.
Load $1,2,3$ and $4$	10 kW
Line	11.7 mOhm, 8.68e-4 H
Simulation step	1e-5 s
udqhf1	0.05 pu, -333 Hz
udqhf2	0.05 pu, 275 Hz

Table 4.4: Simulation scenario



(a) Estimated high frequency impedance (b magnitude im





(c) High frequency current regulator output voltage magnitude.

Figure 4.21: Simulation results

frequency current regulator output voltage, which is used by the slave inverters to detect the islanding/grid-connected condition. This is done without the need of a secondary high frequency signal for communication purposes and without interfering with the master inverter operation.

It is noted that a threshold for the high frequency current regulator output voltage magnitude needs to be set to detect the transition between islanding and grid-connected operation. This threshold might depend on the microgrid/grid architectures, microgrid/grid high frequency impedances or grid pollution. As for the islanding detection THD based methods [72] or the voltage harmonic monitoring based methods [56], the selection of the threshold is not always easy and might require a previous knowledge of the microgrid/grid characteristic.

# 4.4.2 Dynamic master role assignment

One concern for methods in which a master inverter is responsible on injecting the high frequency voltage, is the risk of a master inverter failure. This will leave the grid/microgrid without the high frequency signal, the slave inverters therefore loosing their islanding detection capability. Furthermore, even in the event that the master inverter does not fail, changes in the grid/microgrid topology, e.g. switching between islanding and grid connected operation, connection/disconnection of other inverters, generation units, loads, etc, might have a significant impact in the high frequency signal seen by the inverters connected to the microgrid, eventually affecting to the performance of the method. E.g. during grid-connected operation several inverters might be working like masters, due to the low grid impedance, while during islanding, it is likely that one single master inverter might be enough to supply a high frequency signal voltage visible to all the inverters connected to the microgrid. Hence, in the event of switching from grid connected to islanding, all the master inverters but one could likely safely switch to the slave mode. It is concluded that some mechanism for the dynamic reassignment of the master/slave roles is convenient. Using communications or some type or pre-configuration of the master/slave inverters for this purpose is considered unappealing. A strategy for the dynamic reassignment of the master role is described following. It is accomplished in three steps.

1. Detection by the inverters of changes in the microgrid. Such changes can be of three types. a) the master inverter detects a sudden variation of the high frequency impedance; b) the slave inverters detect that no high frequency voltage is present in the grid. This can be due either



(a) high frequency voltage magnitude measured at the LCL filter output, for the master inverter (blue), inverter 1 (red) and inverter 2 (black)

(b) Commanded high frequency voltage magnitude of inverter 1 (red) and 2 (black) after detecting the high frequency voltage lost

0.8



(c) Magnitude of the secondary high frequency voltage injected by inverter 1 (red) after assuming the master role, and measured by inverter 2 (black)

Figure 4.22: Master-role assignment simulation results

to the failure of the master inverter, or to a significant decrease of the grid impedance (e.g. due to a change from island to grid connected operation); and c) the slave inverters detect a sudden increase of the high frequency voltage in the microgrid. This can be due to a change from grid connected to islanding. An example of failure of the master inverter is shown in Fig. 4.22 (the grid topology is shown in Fig. 4.20). Fig. 4.22(a) shows the high frequency voltage magnitude, measured at the LCL filter output, for the master power converter (blue) and two slave power converters, master failure occurring at t=0.5s.

2. Reassignment of the master inverter role. Once any of the events described above occurs, all the inverters start injecting the high frequency voltage immediately. However, the slave inverters do not inject a constant magnitude high frequency voltage, it increases with time instead (4.18)-(4.19), where  $U_{HF0}$  is the magnitude of the high frequency voltage for each slave inverter right before the master inverter failure, and  $U_{HF_{-}\max}$  is the limit established for the high frequency voltage.

$$u_{HF} = \left(U_{HF0} + k_2 t e^{k_1 U_{HF0}}\right) e^{j\omega_{hf}t} \quad \text{if} \quad |u_{HF}| < U_{HF\_\max} \quad (4.18)$$

$$u_{HF} = U_{HF\_\max} e^{j\omega_{hf}t} \quad \text{if} \quad |u_{HF}| = U_{HF\_\max} \tag{4.19}$$

It is observed from (4.18) that the high frequency voltage magnitude increases linearly with time, but both the starting value as well as the rate of increase being function of  $U_{HF0}$ . According to (4.18), the inverter with a larger initial voltage  $U_{HF0}$  starts with a larger initial value and increases the magnitude faster (see Fig. 4.22(b)), therefore reaching  $U_{HF-max}$  first. The philosophy behind this strategy is that, in general, inverters closer to the PCC before the failure are considered better candidates to assume the master role. The strategy established by (4.18)-(4.19) will produce that the inverters placed closer to the PCC will win the race to become master.

Fig. 4.23 shows the time needed by an inverter to reach  $U_{HF_{\rm max}}$ , as a function of  $U_{HF0}$  and the gain  $k_1$ . It is observed from the figure that small differences in  $U_{HF0}$  produce large variations in the time needed to reach  $U_{HF_{\rm max}}$ , therefore reducing the risk of more than one inverter becoming master at the same time. Once one inverter reaches  $U_{HF_{\rm max}}$ , i.e. the rated high frequency voltage magnitude, automatically changes its role to master (Figs. 4.17 and 4.18) and continues injecting the high frequency signal hereafter (see Fig. 4.22(b)).

It is noted that other reassignment strategies different from (4.18)-(4.19) could be used, the key issue for the design of new strategies being their ability to discriminate the most suitable inverters to assume the master role during the master reassignment process. It is also interesting to note that although in the strategy used in this work the high frequency signals are injected during the reassignment process (see Fig. 4.22), it is feasible for the inverters to produce the high frequency signal *internally*, i.e. without physically injecting them intro the grid, in such a way that only when a inverter reaches  $U_{HF-max}$  it becomes the master inverter, and injection of the actual high frequency voltage into the grid occurs.



Figure 4.23: Elapsed time to reach the rated high frequency voltage magnitude as a function of the initial condition  $U_{HF0}$  and of gain  $k_1$ , with gain  $k_2=1$ .

3. Notification of the role change to the rest of microgrid inverters. Once one inverter assumes the master role, it injects a secondary high frequency signal (udqhf2) during a short period (80ms, see Fig. 4.22(c)). This signal informs to the rest of inverters that the master role has already been reassigned. The rest of inverters automatically will stop injecting the high frequency signal and change their mode of operation to slave mode (Fig. 4.19). Fig. 4.22(c) shows the commanded voltage magnitude of the secondary high frequency signal by inverter 1 and the measured secondary high frequency voltage magnitude by inverter 2, which is used to stop its high frequency signal injection (see Fig. 4.22(b)) and to switch to the slave mode.

# 4.4.3 Experimental results

To verify the viability of the proposed islanding detection and dynamic master assignment methods, the experimental setup shown at Fig. 4.24 was used. Though not shown in the figure, inverters 2 and 3 have the same topology as the master inverter, each including a DSP TMS320F28335 for their control. The parameters of the experimental setup are summarized in Table 4.5. All the inverters include voltage sensors in the line side, which are needed for synchronization. The computational requirements for the implementation of the method are of  $8.2\mu$ s for the master inverter operation mode and  $12.8\mu$ s for the slave inverter operation mode.

Fig.4.25 shows the magnitude of the output voltage of the high frequency current regulator (4.17) of inverters 2 and 3 during transitions from island to grid connected (t=0.5s) and back to island (t=1.5s). The master inverter was injecting the high frequency voltage continuously. The magnitude

Parameter	Value
Grid	380  V, 50  Hz, Scc=2  MVA
Generator (G)	100 kVA, 380 V, 152 A
Master inverter, inverter 2 and 3 $$	380 V, 30 kVA, 10 kHz.
Load	15 kW
udqhf1	0.05 pu, -333 Hz
udqhf2	0.05 pu, 275 Hz
LPF bandwidth	25 Hz
HPF bandwidth	25 Hz
LCL filter resonance frequency	575 Hz

 Table 4.5: Experimental setup parameters



Figure 4.24: Experimental setup



Figure 4.25: Experimentally measured magnitude of the high frequency current regulator output voltage of inverters 2 and 3 for island/grid connected operation. The master inverter injected a high frequency voltage of Vhf1=0.03 pu,  $\omega hf1=-333$  Hz.

of the high frequency current regulator output voltage reliably reflects the transitions between island and grid connected, the changes in the operating condition being detected in tens of *ms*, which is in compliance with international standards requirements [11], [14], [12], [13], [5], [7], [10], [6], [3], [8], [1], [2], [9], [4] and [68].

Fig. 4.26 shows the transient response of the master inverter and inverter 2 during a transition from island to grid-connected. Fig. 4.26(a) shows the d and q-axis components of the measured output current of the master inverter LCL filter. Fig. 4.26(c) shows the injected high frequency voltage, while Fig. 4.26(e) shows the resulting high frequency current. It is observed that the master inverter is continuously injecting a high frequency signal, the resulting current strongly changing from island to line connected, which is used by the master inverter to detect the islanding/grid connected situations. Fig 4.26(b) shows the d and q-axis components of the current measured at the slave inverter LCL filter, while Fig. 4.26(d) and 4.26(f) shows the high frequency voltage injected by the slave inverter as well as the high frequency current at the slave inverter output. The *infinite impedance* mode of operation described causes the high frequency current to be zero in steady state.

Fig 4.27 shows the same results as Fig. 4.26 during a transition for grid connected to island situation, a similar behavior of the measured LCL filter output current is observed.

Fig 4.28(a) shows the dynamic reassignment of the master role after the failure of the master inverter (occurs at t=7s in Fig. 4.16). It is observed from Fig. 4.28(a) that after the master inverter failure detection, inverter 2 and



(a) Master inverter measured output LCL filter current



(c) Master inverter injected high frequency voltage



(e) Master inverter measured output LCL filter high frequency current



(b) Slave inverter measured output LCL filter current



(d) Slave inverter injected high frequency voltage



(f) Slave inverter measured output LCL filter current

Figure 4.26: Experimental results showing the transition from island to grid-connected situation



 $\underbrace{\underbrace{\underbrace{\underbrace{\underbrace{s}}}_{i=1}^{10} \\ -10 \\ 1.3 \\ 1.4 \\ 1.5 \\ t(s)} \underbrace{\underbrace{1.5}_{i=1}^{10} \\ 1.7 \\ t(s)} \underbrace{\underbrace{1.5}_{i=1}^{10} \\ 1.7 \\ t(s)} \underbrace{\underbrace{1.5}_{i=1}^{10} \\ 1.7 \\ t(s)} \underbrace{1.5}_{i=1}^{10} \\ t(s) \\ t($ 

(a) Master inverter measured output LCL filter current



(b) Slave inverter measured output LCL filter current



(c) Master inverter injected high frequency voltage



(e) Master inverter measured output LCL filter high frequency current

(d) Slave inverter injected high frequency voltage



(f) Slave inverter measured output LCL filter current

Figure 4.27: Experimental results showing the transition from grid-connected to island situation



(a) Magnitude of the high frequency voltage injected by the master inverter (blue), inverters 2 (red) and 3 (black). High frequency PCC voltage (green).

(b) Magnitude of the secondary high frequency voltage injected by inverter 2 and measured by inverter 3 after inverter 2 assumes the master role

Figure 4.28: Master-role assignment experimental results

3 start injecting the high frequency signal as described by (4.18) and (4.19). Once inverter 2 reaches the rated high frequency voltage (see Fig. 4.28(a)), automatically changes its role to master (see Figs. 4.17 and 4.18), continues injecting the high frequency signal, and injects a burst with the secondary high frequency signal to indicate to the rest of the inverters that the master role has already been reassigned (see Fig. 4.28(b)). Fig. 4.28(b) shows the magnitude of the injected secondary high frequency voltage by inverter 2 (new master) and measured by inverter 3. It is observed in Fig. 4.28(b) that inverter 3, stops injecting the high frequency signal (red) immediately once it detects the presence of the secondary high frequency signal (udqhf2). It is also noted that although udqhf2 is injected during 2 seconds, inverter 1 detected the presence of the secondary signal in less than 100ms, thus the injection time could be reduced.

It is finally noted that the THD at the PCC is only slightly affected by the injection of the different high frequency voltages, increasing from 2.13% for the case when no high frequency signal voltage is injected, to 2.87% when the high frequency signals for both islanding detection and communications are injected.
## 4.5 Islanding Detection using the effects due to the inverter dead-time

Distributed energy resources are usually connected to the main grid/microgrid by means of a three-phase PWM-VSI (see Fig. 4.29). VSIs produce a distortion of the output voltage with respect to the commanded voltage, mainly due to the blanking time (dead-time) needed for safe commutation within each inverter leg. Though other effects due to the non-ideal behavior of the switches (turn-on/turn-off time and voltage drop on the diodes and power switches,...) also affect to the output voltage, they are less important. The distortion of the output voltage due to the inverter dead-time is known to be a function of the inverter current sign [53], [78], producing harmonics of the fundamental frequency of well defined orders.

The distortion of the output voltage produces an increase in the THD of the voltages/currents, having therefore an adverse impact on the power quality [58]-[117]. However, the induced harmonics can also be used as a form of high frequency excitation for active islanding detection purposes.

In this section, islanding detection using the higher order components of the inverter output voltage due to the non-ideal behavior of the inverter is analyzed. By using this harmonics, the injection of additional high frequency signals is avoided, which is beneficial in terms of power quality.

## 4.5.1 Dead-time effects in PWM inverters.

Fig. 4.29 schematically shows a three-phase PWM-VSI used to connect distributed energy resources to the three-phase utility grid/microgrid. Fig. 4.30 shows the gate signals for one leg without (subplots a) to c)) and with (subplots d) to g)) considering the dead-time in the gate signals. Fig. 4.30(a) and 4.30(b) show the ideal gate signals for switches 1 and 4, while Fig. 4.30(c) shows the ideal output voltage, i.e. with no voltage drop across the switches and on-off transitions of the upper and lower switches occurring simultaneously. In practice, due to the non-zero turn-on and turn-off times, a dead-time has to be inserted in every commutation to guarantee that the two switches in a branch (e.g. S1 and S4) do not conduct simultaneously. Fig. 4.30(d) and 4.30(e) show the real gate signals, after inserting the dead-time, when switches S1 and S4 are turned-on and off respectively. When both transistors are turned-off, one of the freewheeling diodes will conduct, depending on the sign of the output current. If the current is positive (see Fig. 4.29), D4 will be conducting (see Fig. 4.30(f)), while D1 will conduct



Figure 4.29: Generic microgrid architecture.

if the current is negative (see Fig. 4.30(g)). In addition, it is observed from Fig. 4.30(f) and 4.30(g) that the voltage drop across the switches and diodes and the turn-on/off times are considered.

The average voltage errors caused by the non-ideal behavior of the inverter (turn-on and turn-off times, voltage drops and dead-time) during each switching period can be calculated using (4.20) and (4.21) for the case of positive and negative currents respectively (see Fig. 4.30(f) and 4.30(g)).

$$\Delta V = \frac{T_d + t_{on}}{2T_s} \left( -U_{DC} - U_d \right) + \frac{t_{off}}{2T_s} \left( U_{DC} - U_{sat} \right)$$

$$= \frac{-T_d - t_{on} + t_{off}}{2T_s} U_{DC} + \frac{-T_d - t_{on}}{2T_s} U_d + \frac{-t_{off}}{2T_s} U_{sat}$$
(4.20)

$$\Delta V = \frac{T_d + t_{on}}{2T_s} \left( U_{DC} + U_d \right) + \frac{t_{off}}{2T_s} \left( -U_{DC} + U_{sat} \right)$$

$$= \frac{T_d + t_{on} - t_{off}}{2T_s} U_{DC} + \frac{T_d + t_{on}}{2T_s} U_d + \frac{t_{off}}{2T_s} U_{sat}$$
(4.21)

where  $T_d$  is the dead-time,  $t_{on}$  is the turn-on time,  $t_{off}$  is the turn-off time,  $T_s$  is the sampling period,  $U_{DC}$  is the dc bus voltage,  $U_d$  is forward voltage drop of the diode and  $U_{sat}$  is the on-state voltage drop across the power switch.

Assumed that  $Ud \approx Usat$ , (4.20) and (4.21) can be safely simplified to (4.22) and (4.23) [53].

$$\Delta V = \frac{-T_d - t_{on} + t_{off}}{2T_s} U_{DC} - \frac{T_d + t_{on} + t_{off}}{2T_s} U_{sat}$$
(4.22)



Figure 4.30: a) to c): gate signals for switches S1, a), and S4, c), and output voltage when no dead time is considered. d) to g): gate signals for switches S1, d), and S4, e), when the dead-time is inserted. Output voltage when the output current is positive, f) and negative g).

$$\Delta V = \frac{T_d + t_{on} - t_{off}}{2T_s} U_{DC} + \frac{T_d + t_{on} + t_{off}}{2T_s} U_{sat}$$
(4.23)

Fig. 4.31(b) shows the voltage error for phase a averaged for each switching cycle, which is seen to depend on the sign of the output current (see Fig. 4.31(a)). It is observed from Fig. 4.31(b) that the average voltage error is a square wave, which can therefore be expressed using Fourier series as (4.24). Taking into account the  $2\pi/3$  phase shift between phases in a balanced threephase system, the average voltage errors for phases b and c can be expressed as (4.25) and (4.26), with n being the harmonic order.

$$U_{an} = \frac{4\Delta V}{\pi} \sum_{n=1,5,7...} \frac{1}{n} \sin(n\omega_0 t)$$
(4.24)

$$U_{bn} = \frac{4\Delta V}{\pi} \sum_{n=1,5,7\dots} \frac{1}{n} \sin\left[n\left(\omega_0 t - \frac{2\pi}{3}\right)\right]$$
(4.25)

$$U_{cn} = \frac{4\Delta V}{\pi} \sum_{n=1,5,7\dots} \frac{1}{n} \sin\left[n\left(\omega_0 t - \frac{4\pi}{3}\right)\right]$$
(4.26)

The resulting voltage vector due to the the non-ideal behavior of the inverter can be expressed as (4.27) (see Fig. 4.31(c) and 4.31(d)), with the transformation from phase quantities to dq quantities being defined by (4.28).

$$v_{dq} = \sum_{n=1,-5,7...} U_n e^{j(n\omega_0 t + \theta)}$$
(4.27)

$$f_{dq}^{s} = f_{d} + jf_{q} = \frac{2}{3} \left( f_{a} + f_{b} e^{j2\pi/3} + f_{c} e^{j4\pi/3} \right)$$
(4.28)

where  $\theta = \pi$  when n<0 and  $\theta = -\pi$  when n>0,  $\omega_0$  is the grid/microgrid frequency and  $U_n$  is given by (4.29)

$$U_n = \frac{2 * \Delta V}{n\pi} \left[ -2\cos(n\pi) - \cos(n2\pi/3) + \cos(n\pi/3) \right]$$
(4.29)



Figure 4.31: Phase current, a), average voltage error, b), d and q components of the average voltage complex vector, c) and d).



Figure 4.32: Complex vector spectrum of the voltage error.



Figure 4.33: Complex vector spectrums in island mode. The fundamental frequency is 50 Hz, with a dead-time of  $3\mu$ s and switching frequency of 10kHz.

It is concluded from (4.24)-(4.27) that the inverter non-ideal behavior produces harmonics having orders of -5, 7,..., with the corresponding harmonic magnitude being inversely proportional to the harmonic order, (4.29)[35] (see Fig. 4.32).

Figs. 4.33 and 4.34 show the frequency spectrum of the voltage and current complex vectors (experimental) for a VSI, measured at the output of the LCL filter, in island and grid connected conditions respectively. The details of the inverter can be found in Table 4.8. Logarithmic scales are used for the magnitudes. Harmonics of order  $-5^{th}$  and  $7^{th}$  are readily observable in both the voltage and current spectrums, their magnitudes being inversely proportional to the harmonic order. It is observed that in the grid connected case, the harmonics induced in the resulting current vector due to the non-ideal behavior of the inverter increase are higher compared to the island case. This is explained by the lower impedance during this operating condition. It is also noted that the resulting higher order harmonics at the output of the LCL filter decrease in grid-connected mode. This is due to the increased voltage drop across the filter because of the lager circulating currents.

## 4.5.2 Islanding detection using harmonics due to the dead-time

The harmonics due to the non-linear behavior of the inverter, (4.27), can be modeled as (4.8). Every harmonic in the voltage will produce the corresponding harmonic at the same frequency in the inverter current  $(i_{dqhf},$ 



Figure 4.34: Complex vector spectrums in grid connected mode. The fundamental frequency is 50 Hz, with a dead-time of  $3\mu$ s and switching frequency of 10kHz.

(4.9) ). The resulting harmonic component at the output of the LCL filter being (4.12) (see Fig. 4.35).

The high frequency impedance (4.13), calculated from the voltage and current harmonics due to the non-ideal behavior of the inverter, can be used to detect islanding [83].

In principle, any of the high order harmonics due to the non-ideal behavior of the inverter could be potentially used for islanding detection purposes. However, due to the decrease of their magnitude as the harmonic order increases (4.29), higher order harmonics will have a lower signal-to-noise ratio, adversely affecting to the accuracy of the method. Furthermore, the maximum harmonic order might also be limited by the interaction between the injected harmonics, the LCL filter resonance frequency and the grid resonance frequency. It is concluded that the  $-5^{th}$  and the  $7^{th}$  harmonics would be the preferred candidates for the implementation of the method.

Two different alternatives for the implementation of the strategy, namely, *Open-loop* mode and *Current Cancellation* mode, are discussed following.

• Open-loop mode: In this mode of operation, the voltage harmonic due to the dead time is used directly as a high frequency voltage excitation. Fig. 4.35 shows the block diagram of the signal processing used for islanding detection using this mode, including the current control of the inverter as well as the necessary filtering. Two band-pass filters, tuned at the frequency of the harmonic used for islanding detection, are used to isolate the corresponding voltage and current harmonic components. A band-stop filter in the fundamental current control loop is used to



Figure 4.35: Signal processing for islanding detection using the high frequency impedance variation for islanding detection

prevent the fundamental current regulator from reacting against the induced current harmonics.

• Current cancellation mode: An alternative implementation to that shown in Fig. 4.35 would be using a PI regulator in a reference frame synchronous with the harmonic used for islanding detection,  $n\omega_0$  (see Fig. 4.36), with the purpose of cancelling the current induced due to the non-ideal behavior of the inverter. The output of the high frequency current regulator ( $u^*_{dqhf}$ , see Fig. 4.36) would contain the harmonic voltage needed to compensate for the non-ideal behavior of the inverter, which can be used for islanding detection purposes [83]. This strategy has the advantage of partially cancelling the effects on the current due the non-ideal behavior of the inverter, therefore reducing the THD of the output voltage and current.

## 4.5.3 Simulation results

Fig. 4.37 shows the scenario used to simulate the proposed method, the simulation parameters being shown in Table 4.6. Fig. 4.38(a) and 4.38(b) show the magnitude and phase of the estimated high frequency impedance in a transition from island to grid connected (t=0.5s) and from grid connected to island (t=1.5s), when the high frequency impedance is used for islanding detection (see Fig. 4.35). The  $-5^{th}$  harmonic is used for the impedance



Figure 4.36: Signal processing for islanding detection when using the output of the high frequency current regulator for islanding detection

Parameter	Value
Grid	380 V, 50 Hz, Scc=15 MVA
Inverter	380 V, 10 kHz.
Load	10 kW
Line	R=11.7mOhm. L=8.68e-4H
Simulation step	1e-7 s
Dead-time	$5\mu s$

Table 4.6: Simulation parameters: single inverter operation

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estimation, though other higher order harmonics could also be used. The islanding detection standards require the detection of the impedance variation within a period of time, e.g. 1 Ohm in 2 seconds for the German standard [8] and 0.5 Ohms in 5 seconds for the Swiss [4] and Australian [2] standards. It is observed that both the magnitude and phase could be potentially used for islanding detection purpose, the change of the high frequency impedance being detected if a few ms. It is concluded from Fig. 4.38 that the islanding detection requirements are widely met by the proposed method.

It is noted that the dead-time can vary in a relatively large range, depending on the rated voltage and current of the power switches. In general, a shorter dead-time would be preferred, since it implies lower distortion (THD)



Figure 4.37: Proposed simulation setup



Figure 4.38: Estimated high frequency impedance



Figure 4.39: Estimated high frequency impedance

of the output inverter voltage. Increasing the dead-time, increases the magnitude of the voltage error and current harmonics, which increases the signal to noise ratio for the islanding detection signal processing, however it also increases the THD, which is limited by connection standards [11], [14], [12], [13], [5], [7], [10], [6], [3], [8], [1], [2], [9], [4] and [68]. The selection of the dead-time results therefore from a compromise between the signal-to-noise ratio and meeting the connection standards in terms of THD. The simulated dead-time is  $5\mu$ s, resulting in a THD of 0.87%, not compromising therefore the connection standards.

Fig. 4.39 shows the high frequency current regulator output voltage when the block diagram shown in Fig 4.36 is used and the same transition as in Fig. 4.38 occurs. It is observed that the change on the current regulator output occurs in a few ms., therefore meeting the islanding detection standards. Fig. 4.40 shows the magnitude of the -5, 7, -11 and 13 harmonics of the current vector, without and with compensation of the  $-5^{th}$  harmonic. It is observed that when the compensation is implemented, the  $-5^{th}$  fades away. Despite of the slight increase of the  $7^{th}$  harmonic, a reduction of the overall harmonic content, and therefore of the THD, is observed.

The proposed strategy has been evaluated so far for a single inverter connected to the utility grid. However in a general case, several micro-sources connected to the utility grid throughout a PCC will exist in the microgrid. To evaluate the proposed method, a scenario with three parallel-connected converters, has been built as an example (Fig. 4.41). The simulation parameters are shows in Table 4.7.

Fig. 4.42(a) and 4.42(b) show the magnitude and phase of the estimated high frequency impedance in a transition from island to grid-connected



Figure 4.40: Harmonics of the current vector with and without compensation of the 5th harmonic implemented

Parameter	Value
Grid	380V, 50Hz, Scc=15MVA
Inverter 1, 2 and 3	380V, 10kHz.
Load $1, 2, 3$ and $4$	10kW
Line	11.7mOhm, 8.68e-4H
Simulation step	1e-7 s
Dead-time	$5\mu s$

Table 4.7: Simulation parameters: parallel inverter operation



Figure 4.41: Proposed simulation setup for parallel scenario



Figure 4.42: Open-loop mode. Estimated high frequency impedance

(t=0.5s) and from grid-connected to island (t=1.5s) in the Open-loop mode, the high frequency impedance being used for islanding detection (see Fig. 4.35). It is observed that almost the same high frequency impedance (magnitude and phase), is estimated by inverter 1 and inverter 2, as they are connected to the PCC throughout lines of similar characteristics (see Table 4.7); on the contrary, the magnitude of the high frequency impedance estimated by inverter 3 is larger, as it is further from the PCC (there are two series-connected lines between inverter 3 and the PCC, see Fig. 4.41).

Fig 4.43(a) and 4.43(b) shows the response of the method in the *Cur*rent cancellation mode. The high frequency current regulator output voltage (current regulator reaction, see Fig 4.36) when the same transition shown in Fig. 4.42 occurs is shown in Fig. 4.43(a). It is observed that inverter 1 and 2 current regulator reactions is very similar, both magnitude and phase, but inverter 3 current regulator reaction magnitude is lower since inverter 3 it is far from the PCC. As in the single inverter case, the change of the current regulator output occurs in a few ms., therefore meeting the islanding detection standards.

## 4.5.4 Experimental results

Experimental results showing the validity of the proposed method are presented in this subsection. Fig. 4.44 shows the experimental setup, the main parameters being shown in Table 4.8. The inverter is a three-phase IGBT-based inverter, with the dead-time set to  $3\mu$ s, which is the minimum value allowed by the power module.

Fig. 4.45 shows the estimated high frequency impedance magnitude and



Figure 4.43: Current cancellation mode. Estimated high frequency impedance



Figure 4.44: Experimental setup for parallel scenario

Table 4.8: Experimental setup parameters: single inverter operation

Parameter	Value
Grid	380  V, 50  Hz, Scc=2  MVA
Inverter	380 V, 10 kHz, 30kVA.
Load	30 kW
Generator	380V, 10kHz, 100kVA.
Dead-time	$3\mu s$



Figure 4.45: Open-loop mode. Estimated high frequency impedance

phase using the implementation shown in Fig. 4.35 (*Open-loop mode*), during a transition from island to grid-connected (t=0.5s) and from grid connected to island (t=2s). The estimated high frequency impedance is available in 100ms, which is much faster than required by islanding detection standards.

Fig. 4.46 shows the high frequency current regulator reaction when the *Current cancellation mode* (see Fig. 4.36) is used, for the same transition shown in Fig. 4.45. Fig. 4.46(a) shows the d and q-axis components, Fig. 4.46(b) shows the magnitude, while Fig. 4.46(c) shows the phase of the high frequency current regulator output voltage. It is observed that the change on the current regulator output occurs in a few ms, again much faster than required by the islanding detection standards. It also observed that both the magnitude and phase could be potentially used for islanding detection purpose.

Fig. 4.47 shows the magnitude of the most relevant harmonics due to the non-ideal behavior of the inverter for the *Open-loop* and *Current cancellation* modes respectively. It is noted that the THD at the PCC is 2.13% in the *Open-loop mode*, reducing to 1.6% in the *Current cancellation mode*, i.e. when the  $-5^{th}$  harmonic is compensated by the high frequency current regulator (see Fig. 4.36).

Fig. 4.49 and 4.50 shows the experimental results when two inverters are connected in parallel (see Fig. 4.48). The parameters of the experimental setup for this case are summarized in Table 4.9.

Fig. 4.49 shows the estimated high frequency impedance (magnitude and phase) of inverter 1 and 2 during a transition from island to grid-connected (t=1s) and from grid-connected to island (t=4s) in the *Open-loop mode* (Fig. 4.35), while Fig. 4.50 shows the high frequency current regulator reaction



(a) Current reaction components. d component(red), q component (blue)



Figure 4.46: Current cancellation mode. Experimental results.



Figure 4.47: Experimentally measured harmonics of the current vector with and without compensation of the 5th harmonic implemented at the PCC. Dead-time= $3\mu$ s



Figure 4.48: Experimental setup with two parallel-connected inverters

Parameter	Value
Grid	380  V, 50  Hz, Scc=2  MVA
Inverter1 and 2	380 V, 10 kHz, 30kVA.
Inverter1 filter	L=2.4mH, C=30uF
Inverter2 filter	L=1.56mH, C=30uF
Load1 and 2	30 kW
Generator	380V, 10kHz, 100kVA.
Dead-time	$3\mu s$

Table 4.9: Experimental setup parameters: parallel inverter operation



Figure 4.49: Open-loop mode. Estimated high frequency impedance



Figure 4.50: Current cancelation mode. Estimated high frequency impedance

magnitude and phase in the *Current cancelation mode*, for same transition as in Fig. 4.49. It is observed from these figures that grid-island conditions are readily detectable by these two modes of operation.

## 4.6 Islanding detection in three-phase and singlephase systems using Pulsating high frequency signal injection

Most of impedance estimation based active islanding detection methods that have been proposed are intended for three-phase systems. Nevertheless, single-phase DPGs (e.g. single-phase micro-wind generation, small-scale solar panel,...) for low-power home applications are becoming of great interest. The reduced implementation cost of the active islanding detection based methods therefore makes them an appealing option for these kind of applications.

In this section, islanding detection using a pulsating high frequency signal is proposed. The main advantage of the pulsating excitation compared to other forms of high frequency excitations that have already been proposed is that it can be used indistinctly with single and three-phase systems.

# 4.6.1 Islanding detection using pulsating high frequency signal injection

DPG units are usually connected to the main grid/microgrid by means of a three-phase (see Fig. 4.29) or single-phase (see Fig. 4.51) PWM-VSI (subsection 2.2). The H-bridge inverter (Fig. 4.51) is the most common topology in single-phase systems (subsection 2.2.1.2). The use of a rotating high frequency signal has been proposed for islanding detection in three-phase systems in subsection 4.3; however this type of high frequency excitation cannot be applied to single-phase systems.

The principles and implementation of islanding detection using a pulsating high frequency signal, both for the case of three-phase and single-phase systems, are analyzed following. In the first place, the case of three-phase system is considered, the single-phase case being analyzed later.

### 4.6.1.1 Three-phase systems

When a pulsating high frequency signal voltage (4.30) is injected into a three-phase system with an angle of injection  $\phi_i$ , the resulting high frequency current at the output of the LCL filter (see Fig. 4.51) is given by (4.31), the grid high frequency impedance being (4.32), where  $u_{dqhf}$  is the injected high frequency voltage complex vector,  $U_{hf}$  is the magnitude of the injected high



Figure 4.51: Single-phase simplified distributed energy resource connection to the utility grid/microgrid.

frequency signal,  $\omega_{hf}$  is the frequency of the high frequency signal,  $u_{dq\mu ghf}$  is the output LCL filter high frequency voltage complex vector,  $i_{dq\mu ghf}$  is the output LCL filter high frequency current complex vector,  $i_{dqhf}$  is the output inverter high frequency current complex vector,  $L_1$  is the inverter side LCL filter inductance,  $L_2$  is the grid side LCL filter inductance,  $Z_{dq\mu ghf}$  is the microgrid high frequency impedance and  $\phi_Z$  is the phase of the microgrid high frequency impedance. The angle of injection  $\phi_i$  can be selected to be constant, or can change with an angular frequency of  $\omega_i$ . In the first case, the pulsating signal will be injected in a stationary reference frame, while in the second case, the pulsating signal is in injected in a reference frame that rotates at  $\omega_i$ .

It is observed from (4.30)-(4.31) that the pulsating high frequency voltage and current can be decomposed into two rotating signals  $(u_{dqhf}^{pc}, u_{dqhf}^{nc}, i_{dqhf}^{pc}, i_{dqhf}^{nc})$  which rotate in opposite direction, each of half the amplitude of the injected signal. Both components can potentially be used for high frequency impedance estimation (4.32).

$$u_{dqhf} = U_{hf} \cos(\omega_{hf}t) e^{j\phi_i} = U_{hf} \cos(\omega_{hf}t) e^{j\omega_i t} = = \frac{U_{hf}}{2} e^{j(\omega_{hf} + \omega_i)t} + \frac{U_{hf}}{2} e^{j(-\omega_{hf} + \omega_i)t} = u_{dqhf}^{pc} + u_{dqhf}^{nc}$$
(4.30)

$$i_{dq\mu ghf} = \frac{u_{dqhf} - u_{dq\mu ghf} - j\omega_{hf}L_{1}i_{dqhf}}{j\omega_{hf}L_{2}} =$$

$$= \frac{U_{hf}}{2 * |Z_{dq\mu ghf}|} e^{j\left(\left(\omega_{hf} + \omega_{i}\right)t - \phi_{Z}\right)} + \frac{U_{hf}}{2 * |Z_{dq\mu ghf}|} e^{j\left(\left(-\omega_{hf} + \omega_{i}\right)t + \phi_{Z}\right)} =$$

$$= i_{dq\mu ghf}^{pc} + i_{dq\mu ghf}^{nc}$$

(4.31)

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$$Z_{dqhf\mu g} = \frac{u_{dq\mu ghf}^{pc}}{i_{dq\mu ghf}^{pc}} = \frac{u_{dq\mu ghf}^{nc}}{i_{dq\mu ghf}^{nc}}$$
(4.32)

In the discussion following, it is assumed that the neutral of the loads are connected to ground, which is the case for low voltage public distribution systems [116]. However, the neutral wire is not typically available in the connection of three-phase distributed energy resources to the utility grid/microgrid through three-phase VSI (see Fig. 4.29). Therefore the zero sequence component of the current is always zero in the inverter side.

The pulsating high frequency signal can be injected either in a stationary reference frame ( $\omega i=0$  in (4.30), see dqs in Fig. 4.52) or in a rotating reference frame,  $\omega_i \neq 0$  in (4.30), (see dqe in Fig. 4.52). When the high frequency signal is injected in a reference frame that rotates e.g. aligned with the de or qe axis (see Fig. 4.52), all the phases are excited sequentially, meaning that the high frequency impedance of all the three phases can be measured. On the contrary, if the high frequency signal is injected in a stationary reference frame, one, two or all the three phases can be excited, depending on the angle of injection selected. As an example, only phase a is excited if the signal is injected in the ds axis, (see Fig. 4.52), in this case the high frequency signal will be sensitive only to phase a condition. It is also noted that since the connection/disconnection between the microgrid and the grid occurs simultaneously in all the three phases, the number of phases being excited would be irrelevant for islanding detection, i.e. all the three phases reflect the island-grid transitions. However, sequential excitation of all phases opens interesting possibilities for detecting asymmetric faults in three phase systems. This issue will be discussed in detail in the following subsections.

Fig. 4.53 shows the signal processing needed for islanding detection using a pulsating high frequency signal for the case of a three-phase system. In the implementation shown in Fig. 4.53 the PWM-VSI is current regulated. In this case, the current regulator can react against the induced high frequency current. To prevent this, band-stop filters are used to reject the positive and negative sequence current components (4.31) from the current feedback (*BSF1* in Fig. 4.53). Band-stop filters *BSF2* and *BSF3* in Fig. 4.53 are used to reject the fundamental component of the voltage and current respectively, while *BSF4* and *BSF5* reject the negative sequence components,



Figure 4.52: *abc* and *dq* reference systems. dqs=stationary reference frame, dqe=rotating reference frame.

4.6 Islanding detection in three-phase and single-phase systems using Pulsating high frequency signal injection



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Figure 4.53: Signal processing for islanding detection using a three-phase inverter.

the positive sequence component of these signals being finally obtained. The high frequency impedance is obtained using (4.31) and (4.32), islanding being detected from the high frequency impedance variation.

## 4.6.1.2 Single-phase system

Though the concept of complex vector is only valid in principle for the case of three-phase systems, it is also possible to use it with single-phase systems. This can be done by defining a complex vector in which one of the components (e.g. *d*-axis in (4.33) and (4.34)) is made equal to the corresponding singlephase voltage/current and the other component (e.g. *q*-axis in (4.33) and (4.34)) is made equal to zero. By doing this, the high frequency impedance (4.32) in a single-phase system can be estimated from (4.33) and (4.34), where  $u_{ahf}$  is the injected high frequency phase voltage,  $u_{a\mu ghf}$  and  $i_{a\mu ghf}$  are the LCL filter high frequency output phase voltage and current respectively and  $i_{ahf}$  is the inverter high frequency output phase current.

$$u_{dqhf} = \begin{bmatrix} u_{dqhf} \\ 0 \end{bmatrix} = \begin{bmatrix} U_{hf} \cos(\omega_{hf}t) \\ 0 \end{bmatrix} =$$

$$= \frac{U_{hf}}{2} e^{j\omega_{hf}t} + \frac{U_{hf}}{2} e^{-j\omega_{hf}t} = u_{dqhf}^{pc} + u_{dqhf}^{nc}$$
(4.33)



Figure 4.54: Signal processing for islanding detection using a single-phase inverter.

$$i_{dq\mu ghf} = \begin{bmatrix} i_{a\mu ghf} \\ 0 \end{bmatrix} = \begin{bmatrix} \frac{u_{ahf} - u_{a\mu ghf} - j\omega_{hf}L_{1}i_{ahf}}{j\omega_{hf}L_{2}} \\ 0 \end{bmatrix} = \\ = \frac{U_{hf}}{2 * |Z_{dq\mu ghf}|} e^{j(\omega_{hf}t - \phi_{Z})} + \frac{U_{hf}}{2 * |Z_{dq\mu ghf}|} e^{j(-\omega_{hf}t + \phi_{Z})} = \\ = i_{dq\mu ghf}^{pc} + i_{dq\mu ghf}^{nc}$$

$$(4.34)$$

Fig. 4.54 shows the signal processing needed for islanding detection in a single-phase system. A single band-stop filter is needed to reject the component at  $\omega_{hf}$  (BSF1, see Fig. 4.54) to prevent the fundamental current regulator reaction. As for the three-phase system case, band-stop filters BSF2 and BSF3 reject the fundamental components and BSF4 and BSF5 reject the negative sequence components. Once the positive sequence component of the voltage and current are isolated, the high frequency impedance is obtained using (4.31) and (4.32), islanding being detected from the high frequency impedance variation.

It is finally noted that the dead-time effect in PWM single-phase inverters produces a distortion that can be expressed as (4.35) 4.5, being therefore possible to use any of the high order harmonics in (4.35) for islanding detection purposes 4.5.

$$u_{an} = \frac{4\Delta V}{\pi} \sum_{n=1,5,7,\dots} \frac{1}{n} \sin(n\omega_f t)$$
(4.35)

## 4.6.2 Phase-to-phase and phase-to-ground fault detection using pulsating high frequency signal injection

It has already been mentioned that since islanding in three-phase system occurs simultaneously in all the three phases, it can be readily detected independent of the high frequency signal injection mode, i.e. stationary or rotating. It is noted in this regard that the implementation of the injection in the stationary reference frame is slightly simpler. However, the injection of the high frequency signal in a rotating reference frame opens interesting possibilities for the detection of phase-to-phase and phase-to-ground faults in three-phase systems.

Fig. 4.55(a) and 4.55(b) show the PCC voltage vector spectrum in a rotating reference frame (dqe in Fig. 4.52) and in a stationary reference frame (idqs in Fig. 4.52), when the pulsating high frequency voltage is been superimposed on top of the fundamental excitation. As shown in Fig. 4.55(a), the pulsating high frequency signal can be decomposed in two rotating signals,  $u_{dqhf}^{pc}$  and  $u_{dqhf}^{nc}$  of frequencies  $\omega_{hf}$  and  $-\omega_{hf}$  respectively. By transforming this voltage vector to the stationary reference frame (see Fig. 4.55(b)), the frequency components  $u_{dqhf}^{pc}$  and  $u_{dqhf}^{nc}$  at  $\omega_{hf} + \omega_i$  and  $-\omega_{hf} + \omega_i$  are obtained respectively.

The most typical asymmetric faults that occur in three-phase systems are the phase-to-ground, phase-to-phase and phase-to-neutral [116]. Typically the neutral wire is not available in the connection of three-phase distributed energy resources to the utility grid/microgrid through three-phase VSI (see Fig. 4.29). Therefore, only the phase-to-ground and phase-to-phase faults will be analyzed in this section.

## 4.6.2.1 Phase-to-ground fault

When a pulsating voltage vector is injected into a three-phase system with a fault to ground in phase a (see Fig. 4.56(a)), the resulting high frequency phase currents are given by (4.36). The pulsating signal is injected in a dqereference frame which rotates at  $\omega_i = 50Hz$  and it is assumed that the fault impedance is much lower than the system (load) impedance (ZL).



(a) PCC voltage vector spectrum in a rotating reference frame



(b) PCC voltage vector spectrum in a stationary reference frame



(c) Output inverter current vector spectrum when feeding a non-symmetrical load.

Figure 4.55: Spectrum signals

## 4.6 Islanding detection in three-phase and single-phase systems using Pulsating high frequency signal injection



Figure 4.56: Different grid faults

$$\begin{bmatrix} i_{a} \\ i_{b} \\ i_{c} \end{bmatrix} = \begin{bmatrix} \frac{V_{a3}}{Z_{L}} e^{j\left(\left(\omega_{hf}+\omega_{i}\right)t-\phi_{Z_{L}}\right)} \\ \frac{V_{b}\sqrt{3}}{Z_{L}} e^{j\left(\left(\omega_{hf}+\omega_{i}\right)t-5*\pi/6-\phi_{Z_{L}}\right)} \\ \frac{V_{c}\sqrt{3}}{Z_{L}} e^{j\left(\left(\omega_{hf}+\omega_{i}\right)t+5*\pi/6-\phi_{Z_{L}}\right)} \end{bmatrix} + \\ &+ \begin{bmatrix} \frac{V_{a3}}{Z_{L}} e^{j\left(\left(-\omega_{hf}+\omega_{i}\right)t+\phi_{Z_{L}}\right)} \\ \frac{V_{b}\sqrt{3}}{Z_{L}} e^{j\left(\left(-\omega_{hf}+\omega_{i}\right)t+5*\pi/6+\phi_{Z_{L}}\right)} \\ \frac{V_{c}\sqrt{3}c}{Z_{L}} e^{j\left(\left(-\omega_{hf}+\omega_{i}\right)t-5*\pi/6+\phi_{Z_{L}}\right)} \end{bmatrix} \end{bmatrix}$$

$$(4.36)$$

Applying Fortescue's theorem, (4.37), to the components in (4.36) at  $\omega_{hf} + \omega_i$ , a set of symmetrical components is obtained (4.38), with  $i^0_{dqhfpc}$ ,  $i^{pc}_{dqhfpc}$  and  $i^{nc}_{dqhfpc}$  being the zero, positive and negative sequence components respectively. It is noted that though the same transformation could be used with the components in (4.37) at  $-\omega_{hf} + \omega_i$ , the discussion following focuses only for the frequency components at  $\omega_{hf} + \omega_i$ .

$$\begin{bmatrix} i^0\\i^+\\i^- \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1\\1 & a & a^2\\1 & a^2 & a \end{bmatrix} \begin{bmatrix} i_a\\i_b\\i_c \end{bmatrix}$$
(4.37)

$$\begin{bmatrix} i_{dqhfpc}^{0} \\ i_{dqhfpc}^{pc} \\ i_{dqhfpc}^{nc} \\ i_{dqhfpc}^{nc} \end{bmatrix} = \begin{bmatrix} 0 \\ \frac{2\sqrt{3}}{3} I_{cc} e^{j\left(\left(\omega_{hf}+\omega_{i}\right)t-\phi_{Z_{L}}\right)} \\ \frac{\sqrt{3}}{3} I_{cc} e^{j\left(\left(-\omega_{hf}-\omega_{i}\right)t-\phi_{Z_{L}}\right)} \end{bmatrix}$$
(4.38)

where  $I_{cc} = U_b \sqrt{3} / Z_L$ .

If the fault occurs in phase b, the resulting symmetrical components using (4.37) are given by (4.39), while if the fault occurs in phase c it is expressed by (4.40). It is observed from (4.38)-(4.40) that the faulty phase can be detected from the phase angle between the positive sequence component  $(i_{dqhfpc}^{pc})$  and the negative sequence component  $(i_{dqhfpc}^{nc})$ , which is  $\theta$  when the faulty phase is phase a,  $2\pi/3$  when the faulty phase is phase b and  $4\pi/3$  when the faulty phase is phase c.

$$\begin{bmatrix} i_{dqhfpc}^{0} \\ i_{dqhfpc}^{pc} \\ i_{dqhfpc}^{nc} \end{bmatrix} = \begin{bmatrix} 0 \\ \frac{2\sqrt{3}}{3} I_{cc} e^{j\left(\left(\omega_{hf} + \omega_{i}\right)t - \phi_{Z_{L}}\right)} \\ \frac{\sqrt{3}}{3} I_{cc} e^{j\left(\left(-\omega_{hf} - \omega_{i}\right)t + 2\pi/3 - \phi_{Z_{L}}\right)} \end{bmatrix}$$
(4.39)

$$\begin{bmatrix} i_{dqhfpc}^{0} \\ i_{dqhfpc}^{pc} \\ i_{dqhfpc}^{nc} \end{bmatrix} = \begin{bmatrix} 0 \\ \frac{2\sqrt{3}}{3} I_{cc} e^{j\left(\left(\omega_{hf}+\omega_{i}\right)t-\phi_{Z_{L}}\right)} \\ \frac{\sqrt{3}}{3} I_{cc} e^{j\left(\left(-\omega_{hf}-\omega_{i}\right)t+4\pi/3-\phi_{Z_{L}}\right)} \end{bmatrix}$$
(4.40)

#### 4.6.2.2 Phase-to-phase fault

When a pulsating voltage vector which rotates at  $\omega_i$ , is injected into a three-phase system in which a phase-to-phase fault between phases *a-b* occurs (see Fig. 4.58(b)), the resulting phase currents are expressed by (4.41) and the resulting symmetrical components are given by (4.42) (only the phasors for the frequency components at  $\omega_{hf} + \omega_i$  are shown). It is assumed that the fault impedance (ZF) is much lower than the load impedance (ZL).

$$\begin{bmatrix} i_{a} \\ i_{b} \\ i_{c} \end{bmatrix} = \begin{bmatrix} \frac{U_{ab}}{Z_{F}} e^{j\left((\omega_{hf} + \omega_{i})t - \pi/6 - \phi_{Z_{F}}\right)} \\ -\frac{U_{ab}}{Z_{F}} e^{j\left((\omega_{hf} + \omega_{i})t - \pi/6 - \phi_{Z_{F}}\right)} \\ 0 \end{bmatrix} + \\ + \begin{bmatrix} \frac{U_{ab}}{Z_{F}} e^{j\left((-\omega_{hf} + \omega_{i})t + \pi/6 + \phi_{Z_{F}}\right)} \\ \frac{U_{ab}}{Z_{F}} e^{j\left((-\omega_{hf} + \omega_{i})t + \pi/6 + \phi_{Z_{F}}\right)} \\ 0 \end{bmatrix}$$

$$(4.41)$$

The resulting symmetrical components when the fault occurs between phases b-c or c-a are given by (4.43)-(4.44). It is observed by comparing (4.42)-(4.44) that the faulty phases can be detected from the phase angle



Figure 4.57: Simulation scenario for both three and single-phase systems

between  $i_{dqhfpc}^{pc}$  and  $i_{dqhfpc}^{nc}$ . I.e.  $\pi/3$  when the fault occurs between phases a and b,  $\pi$  when the fault occurs between phases b and c and  $-\pi/3$  when the fault occurs between phases a and c.

$$\begin{bmatrix} i_{dqhfpc}^{0} \\ i_{pc}^{pc} \\ i_{dqhfpc}^{nc} \\ i_{dqhfpc}^{nc} \end{bmatrix} = \begin{bmatrix} 0 \\ \frac{\sqrt{3}}{3} I_{cc} e^{j\left(\left(\omega_{hf} + \omega_{i}\right) - \phi_{Z_{F}}\right)} \\ \frac{\sqrt{3}}{3} I_{cc} e^{j\left(\left(-\omega_{hf} - \omega_{i}\right) + \pi/3 - \phi_{Z_{F}}\right)} \end{bmatrix}$$
(4.42)

$$\begin{bmatrix} i_{dqhfpc}^{0} \\ i_{dqhfpc}^{pc} \\ i_{dqhfpc}^{nc} \\ i_{dqhfpc}^{nc} \end{bmatrix} = \begin{bmatrix} 0 \\ \frac{\sqrt{3}}{3} I_{cc} e^{j\left(\left(\omega_{hf}+\omega_{i}\right)t-\phi_{Z_{F}}\right)} \\ \frac{\sqrt{3}}{3} I_{cc} e^{j\left(\left(\omega_{hf}+\omega_{i}\right)t+\pi-\phi_{Z_{F}}\right)} \end{bmatrix}$$
(4.43)

$$\begin{bmatrix} i_{dqhfpc}^{0} \\ i_{dqhfpc}^{pc} \\ i_{dqhfpc}^{nc} \\ i_{dqhfpc}^{nc} \end{bmatrix} = \begin{bmatrix} 0 \\ \frac{\sqrt{3}}{3} I_{cc} e^{j\left(\left(\omega_{hf}+\omega_{i}\right)t-\phi_{Z_{F}}\right)} \\ \frac{\sqrt{3}}{3} I_{cc} e^{j\left(\left(\omega_{hf}+\omega_{i}\right)t-\pi/3-\phi_{Z_{F}}\right)} \end{bmatrix}$$
(4.44)

where  $I_{cc} = U_{ab}/Z_F$ .

## 4.6.3 Simulation results

Fig. 4.57 shows the scenario used to simulate the proposed islanding and fault detection methods. The same scenario was used for both single-phase and three-phase cases, the corresponding inverter topologies being shown in Fig. 4.51. The simulation parameters are shown in Table 4.10.

Three-phase						
Grid	Inverter	Load	Line			
380V, 50 Hz, rg/Xg=0.1	380	3 kW	$R=11.7m\Omega$			
Scc=15MVA	10 kHz	JKW	L=8.68e-4H			
Single-phase						
Grid	Inverter	Load	Line			
220V, 50 Hz, rg/Xg=0.1	220V	1 I-W	$R=11.7m\Omega$			
Scc=15MVA	10 kHz	IKW	L = 8.68e-4H			

Table 4.10: Simulation scenario

#### 4.6.3.1 Islanding detection

Fig. 4.58 shows a transition from island to grid connected for the case of a three-phase system, when the pulsating high frequency signal is injected in a stationary reference frame (dqs, see Fig. 4.53). Fig. 4.58(a) shows the dqs components of the filter output voltage and Fig. 4.58(b) shows the dqscomponents of the inverter output current; both the voltages and currents shown in Fig. 4.58(a) and 4.58(b) consist of the fundamental component and the high frequency component, the latest being practically imperceptible due to its reduced amplitude. Fig. 4.58(c) shows the dqs components of the injected inverter high frequency voltage after removing the fundamental voltage. Similarly, Fig. 4.58(d) shows the high frequency components of the inverter output current once the fundamental current has been removed. An increase of the high frequency current magnitude is readily observed after the transition from island to grid connected condition, due to the reduction of the overall high frequency impedance.

Fig. 4.59 shows the same simulation results as in Fig. 4.58 for the case of a single-phase system. Fig. 4.59(a) and 4.59(b) show the inverter output voltage and current respectively (fundamental and high frequency components), while Fig. 4.59(c) and 4.59(d) shows the corresponding high frequency components. A similar behavior of the inverter output high frequency current is observed, the transition between grid and island modes being readily observed.

Fig. 4.60 and 4.61 show the estimated high frequency impedance for three-phase and single-phase systems respectively, when transitions from island to grid and from grid to island occur at t=1s and t=2s. It is observed

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(a) dqs components of the filter output voltage



(c) dqs components of the injected high frequency voltage



(b) dqs components of the inverter output current



(d) *dqs* components of the inverter high frequency current

Figure 4.58: Simulation results. Transition from island to grid connected (t=1 s) for the case of three-phase system.  $\omega hf$ =300 Hz, Vhf=0.01 pu.



(a) dqs components of the filter output voltage



(c) dqs components of the injected high frequency voltage



(b) dqs components of the inverter output current



(d) dqs components of the inverter high frequency current

Figure 4.59: Simulation results. Transition from island to grid connected (t=1 s) for the case of single-phase system.  $\omega hf$ =300 Hz, Vhf=0.01 pu.



(a) Estimated high frequency impedance (b) Estimated high frequency impedance magnitude phase

Figure 4.60: Simulation results. Transition from island to grid connected (t=1 s) for the case of three-phase system.  $\omega hf$ =300 Hz, Vhf=0.01 pu.

that the estimated high frequency impedance is available in a few ms., meeting therefore the islanding detection standards.

As already mentioned, the pulsating high frequency signal can be injected either in a stationary or a rotating reference frame in three phase systems. This is confirmed by the results shown in Fig. 4.62 where grid-island and grid-island transitions are readily observed in the high frequency impedance when the high frequency signal is injected in a rotating reference frame.

## 4.6.3.2 Fault detection

Fig. 4.63(a) and Fig. 4.63(b) show the magnitude of  $i^{nc}_{dqhfpc}$  and the phase angle between  $i^{pc}_{dqhfpc}$  and  $i^{nc}_{dqhfpc}$ , for the following faults: phase-to-ground faults in phase a (0.5<t<1 s), b (1<t<1.5 s) and c (1.5<t<2 s), and phase-to-phase faults between phases a-b (2<t<2.5 s) and b-c (2.5<t<3 s). It is observed that the magnitude of  $i^{nc}_{dqhfpc}$  is zero when there is no fault, the type (phase-to-ground or phase-to-phase) and location or the fault being detected from the phase angle between  $i^{pc}_{dqhfpc}$  and  $i^{nc}_{dqhfpc}$ .

Finally, Fig. 4.64 shows the dynamic behavior of the angle between positive and negative components of the high frequency current,  $i_{dqhfpc}^{pc}$  and  $i_{dqhfpc}^{nc}$  (blue), as well as between the positive and negative components of the fundamental current,  $i_{dqf}$  and  $i_{dqf}^{nc}$  (red), when a phase-to-ground fault occurs in phase b (t=1 s). It is observed that the phase angle between high frequency signals (i.e.  $i_{dqhfpc}^{pc}$  and  $i_{dqhfpc}^{nc}$ ) has a faster transient response than that of the fundamental components (i.e.  $i_{dqf}$  and  $i_{dqf}^{nc}$ ), therefore enabling faster



(a) Estimated high frequency impedance (b) Estimated high frequency impedance magnitude phase

Figure 4.61: Simulation results. Transition from island to grid connected (t=1 s) for the case of single-phase system.  $\omega hf$ =300 Hz, Vhf=0.01 pu.



Figure 4.62: Simulation results for a three-phase system when the pulsating high frequency signal is injected in a rotating reference frame Transition from island to grid connected (t=1 s) for the case of single-phase system.  $\omega hf$ =300 Hz, Vhf=0.01 pu.

## 4.6 Islanding detection in three-phase and single-phase systems using Pulsating high frequency signal injection



Figure 4.63: Simulation results.  $i_{dqhfpc}^{nc}$  magnitude and b) phase angle between  $i_{dqhfpc}^{pc}$  and  $i_{dqhfpc}^{nc}$  for the case of a phase-to-ground fault in phase a (0.5<t<1 s), b (1<t<1.5 s) and c (1.5<t<2 s), and for the case of a phase-to-phase fault between phases a-b (2<t<2.5 s) and b-c (2.5<t<3 s).  $\omega i$ =50 Hz,  $\omega_{hf}$ =300 Hz, Vhf=0.01 pu.



Figure 4.64: Phase angle between  $i_{dqhfpc}^{pc}$  and  $i_{dqhfpc}^{nc}$  and between  $i_{dqf}$  and  $i_{dqf}^{nc}$ .  $\omega i=50$  Hz,  $\omega_{hf}=300$  Hz, Vhf=0.01 pu.

fault detection.

## 4.6.4 Experimental results

Fig. 4.65 shows the experimental setup used both for the case of a threephase and a single-phase systems. The parameters are shown in Table 4.10I.

Fig. 4.66, 4.67 and 4.68 show the magnitude and phase of the estimated high frequency impedance during a transition for island to grid-connected (t=1 s) and from grid-connected to island (t=3 s). The high frequency signal was injected in the stationary reference frame in Fig. 4.66 and in a rotating reference frame in Fig. 4.67. It is observed that the high frequency impedance



Figure 4.65: Experimental Setup

change is detected after a few ms both for the case of three-phase and singlephase systems, therefore meeting the islanding detection standards.

Fig. 4.69(a) and Fig. 4.69(b) show the magnitude of  $i_{dqhfpc}^{nc}$  and the phase angle between  $i_{dqhfpc}^{pc}$  and  $i_{dqhfpc}^{nc}$ , for the following faults: phase-to-ground faults in phase a (2<t<4 s), b (4<t<6 s) and c (6<t<8 s), and phaseto-phase faults between phases a-b (8<t<10 s) and b-c (10<t<12 s). It is observed that the magnitude of  $i_{dqhfpc}^{nc}$  is zero when there is no fault, the type of fault being readily detected from the phase angle between  $i_{dqhfpc}^{pc}$  and  $i_{dqhfpc}^{nc}$ . Finally Fig. 4.70 shows the transient behavior of the phase angle between  $i_{dqhfpc}^{pc}$  and  $i_{dqhfpc}^{nc}$  (blue) and between  $i_{dqf}$  and  $i_{dqf}^{nc}$  (red), when a phase-toground fault occurs in phase b (t=4 s) (see description for Fig. 4.64). In all the cases, it is observed a remarkable agreement with the simulation results shown in Section IV.


Figure 4.66: Experimental results. Transition from island to grid connected (t=1 s) for the case of three-phase system.  $\omega hf$ =300 Hz, Vhf=0.01 pu. The pulsating high frequency signal is injected in the stationary reference frame.



Figure 4.67: Experimental results. Transition from island to grid connected (t=1 s) for the case of three-phase system.  $\omega hf$ =300 Hz, Vhf=0.01 pu. The pulsating high frequency signal is injected in a rotating reference frame.



Figure 4.68: Experimental results. Transition from island to grid connected (t=1 s) for the case of single-phase system.  $\omega hf$ =300 Hz, Vhf=0.01 pu.



Figure 4.69: Experimental results.  $i_{dqhfpc}^{nc}$  magnitude and b) phase angle between  $i_{dqhfpc}^{pc}$  and  $i_{dqhfpc}^{nc}$  for the case of a phase-to-ground fault in phase a (2<t<4 s), b (4<t<6 s) and c (6<t<8 s), and for the case of a phase-to-phase fault between phases a-b (8<t<10 s) and b-c (10<t<12 s).  $\omega i$ =50 Hz,  $\omega_{hf}$ =300 Hz, Vhf=0.01 pu.

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Figure 4.70: Experimental results. Phase angle between  $i_{dqhfpc}^{pc}$  and  $i_{dqhfpc}^{nc}$  and between  $i_{dqf}$  and  $i_{dqf}^{nc}$ .  $\omega i = 50$  Hz,  $\omega_{hf} = 300$  Hz, Vhf = 0.01 pu.

### 4.7 Coordinated Operation of Parallel-Connected Inverters for Active Islanding Detection Using High-Frequency Signal Injection

This section presents a method in which, all the inverters participating in the strategy, inject a synchronized high frequency signal. In order to minimize the impact of the high frequency signal on the grid, the inverters can behave either as voltage sources or as current sources. In addition, they have the ability to self-reconfigure their mode of operation depending on the microgrid/grid condition and without the need of communications or preestablished master/slave roles.

# 4.7.1 Islanding detection using high frequency voltage injection

Voltage-source inverters (VSI) present in a microgrid (e.g. in controlled rectifiers used in APFs, back-to-back power converters, etc.) can easily inject a low-magnitude, high-frequency voltage from which the high frequency impedance is estimated. As an example, both rotating and pulsating high frequency signals can be injected, the analysis being collected in sections 4.3 and 4.6 respectively.

Fig. 4.71 shows the schematic implementation of the proposed method. It follows the same principles as the previous methods, where a rotating high frequency signal (4.8) is injected,  $\omega_{hf}$  and  $U_{hf}$  being the frequency and magnitude respectively. The induced high frequency current  $i_{hf}$  is given by (4.9). The high frequency impedance at the excitation frequency is  $Z_{hf}$  (4.10) with its phase angle being  $\angle Z_{hf}$ . Fig. 4.72a and Fig. 4.72b show the magnitude and phase of the high frequency impedance  $Z_{hf}$  during a transition from island to grid and from grid to island. The change in both metrics between islanding and grid condition are readily observable. Islanding detection is based on the rate of variation of  $Z_{hf}$  with time, i.e.  $\Delta Z_{hf} / \Delta t$ . Comparison of  $Z_{hf}$  with a threshold might also potentially be used 4.3.

# 4.7.2 Islanding detection using high frequency voltage injection for the case of multiple inverters

While simple for the case of a single inverter, the extension of the method described in subsection 4.7.1 to the case of multiple inverters is not trivial.



Figure 4.71: Block diagram of the master inverter.



Figure 4.72: Experimentally measured high frequency impedance during islandgrid transitions  $U_{hf}$ =1.5V,  $\omega hf$ =-333Hz.

Strategies that have been proposed to address this case are presented in this section. In the discussion following *master inverters* refers to inverters which inject a high frequency signal to detect the microgrid condition (grid/island). Slave inverters refers to inverters without such capability, but which still need to know the grid condition for their proper operation. This means that master inverters are responsible of informing the slave inverters on the grid condition. For the evaluation of the strategies, the following issues need to be taken into account:

- 1. All the inverters in the microgrid participating in the strategy should *know* the microgrid condition (island/grid connected) within a time frame compatible with islanding detection standards.
- 2. The adverse impact on the microgrid/grid power quality (THD) due to the injection of high frequency signals should be kept as small as possible and below the limits established by the connection standards.
- 3. Use of separate communication channels is not allowed.
- 4. The injection of an additional high frequency signal for communication purposes is acceptable as this does not have the problems/concerns intrinsic to communications, like cost and the risk of communication breakdown. Details on the use of the secondary high frequency signal can be found in 4.3,4.4.

### 4.7.2.1 Static, single master inverter

In subsection 4.3, the use of a master inverter, responsible of injecting a high frequency rotating voltage vector (4.8) was proposed. The rest of inverters in the microgrid were configured to be slaves. Two high frequency signals were injected by the master inverter: the first one for islanding detection as described in subsection 4.7.1; the second one to communicate the islanding condition to the rest of (slave) inverters present in the microgrid. Fig. 4.73a schematically shows the high frequency model for this case. The inverter closer to the PCC injects the high frequency voltage, therefore behaving like a voltage source. Contrary to this, the rest of inverters as well as the grid voltage do not contain a high frequency voltage component, being modeled therefore as an impedance connected to ground.

The implementation of this strategy is simple as no interference among inverters can occur –only the master inverter injects high frequency signals–. However, it has several limitations:



Figure 4.73: a) Static, single master inverter; b) Dynamic, multiple master inverter

- 1. Failure of the master inverter would leave the grid without the high frequency signal voltage, the rest of inverters in the grid hence losing their capability to detect islanding.
- 2. The location of the master inverter has to be carefully chosen in large microgids. For inverters located far from the PCC, the variation of the high frequency impedance between grid and island condition might be small, reducing the reliability of the method.
- 3. Inverters including high bandwidth current regulators, e.g. active filters, might *see* the high frequency signal as a disturbance and partially compensate for it.

### 4.7.2.2 Dynamic (multiple) master inverter

In subsection 4.4, a dynamic master assignment strategy was proposed. The signal injection by the master inverter is as in the previous case and islanding is detected from the high frequency impedance, as described in subsection 4.7.1. Slave inverters include a high frequency PI current regulator to prevent their reaction against the high frequency current (see Fig. 4.74). By making its command equal to zero, it is guaranteed that no high frequency current circulates through the slave inverters output. This mode of operation was named *infinite impedance*. Slave inverters detect islanding/grid connected condition from the changes in their high frequency current regulator of the master inverter; i.e. if u = 0 means that there is no master inverter injecting



Figure 4.74: Schematic representation of the *master* and *slave* inverters implementing the infinite impedance mode. Current regulators needed for the control of the fundamental current are not shown (see Fig. 4.71 for details)

the high frequency voltage. This master-slave strategy has several appealing properties.

- 1. The high frequency voltage injected by the master inverter is not corrupted by the reaction of other inverters.
- 2. Slave inverters automatically detect failure of the master inverter. A competitive strategy for the reassignment of the master inverter role in the event of master inverter failure was defined in 4.4.
- 3. The master-inverter reassignment strategy naturally allows multiple master inverters. Slave inverters being too far from the master inverter might be unable to detect master's high frequency signal voltage. This will automatically trigger a competitive process to become master. As a result, several master inverters distributed all over the microgrid can operate simultaneously.

Fig. 4.73b schematically shows the high frequency model for this case. Master inverters behave like voltage sources. Slave inverters, due to their *infinite impedance* configuration, behave as an open circuit. As for the case in Fig. 4.73a, the grid is modeled as a ground connected impedance.

Regardless of its appealing characteristics this strategy also has some limitations:

1. The modes of operation of operation of master and slave inverters differ substantially (see Fig. 4.74, 4.3,4.4). Switching between both modes

is triggered by the presence/absence of the high frequency voltage in the microgrid. Though the filtering to detect the presence of the high frequency voltage is relatively simple 4.3, its implementation can be problematic in practice. The signals can be corrupted by noise in the acquisition system, harmonics in the voltages due to non-linear loads, transients, etc. Spurious detection of the high frequency voltage might result in repeated master/slave transitions, with unpredictable results.

2. For a given magnitude of the injected high frequency voltage at the filter output, the resulting high frequency component of the filter current  $i_{hf}$  (4.45) will be function of the high frequency voltage  $u_{hf}$ , the output filter impedance ZF and the equivalent high frequency impedance at the point of connection of the inverter to the microgrid  $Z_{hf}$ .

$$i_{hf} = \frac{u_{hf}}{Z_F + Z_{hf}} \tag{4.45}$$

While  $u_{hf}$  and ZF are known in advance, significant uncertainty exists regarding  $Z_{hf}$ . For inverters close to the PCC in grid operation, this impedance can be very small and the circulating high frequency current  $i_{hf}$  large, adversely impacting the power quality (THD).

To overcome aforementioned limitations, a strategy for the coordinated operation of multiple parallel connected inverters in a microgrid is proposed in the following subsection.

$$[U] = [Z][I] (4.46)$$

$$[I] = \begin{bmatrix} i_{Fhf1} \\ u_{Lhf1} \\ i_{Lhf12} \\ i_{Ihf12} \\ i_{Fhf12} \\ u_{Lhf2} \\ i_{Lhf23} \\ i_{Ihf3} \\ \dots \\ i_{Fhf(N-1)} \\ u_{Lhf(N-1)} \\ i_{Lhf(N-1)N} \\ i_{IhfN} \\ u_{LhfN} \\ i_{IhfN} \\ u_{LhfN} \\ i_{LhfN1} \\ i_{IhfN} \end{bmatrix}$$

$$(4.49)$$

### 4.7.3 Islanding detection in microgrids with multiple inverters using combined current/voltage injection

Most of signal injection based islanding detection methods that have been proposed inject a high frequency voltage. The island/grid condition is estimated from the resulting high frequency impedance. However, it is also possible to inject a high frequency current. Deciding between voltage and current injection can be based on the high frequency impedance seen by the inverter. Voltage injection would be advantageous during island operation or for inverters located far from the PCC. In these cases, the equivalent impedance seen by the inverter will be large, limiting the resulting high frequency current. On the contrary, for inverters operating near the PCC during grid operation, the equivalent impedance will be small. Current injection would be advantageous in this case, since voltage injection would result in a relatively large high frequency current. Combining high frequency voltage injection and high frequency current injection would therefore be advisable for inverters experiencing large variations in the high frequency impedance seen at their terminals, as would be the case of inverters located near the PCC.



Figure 4.75: Generic microgrid architecture.

Islanding detection using combined voltage/current injection is analyzed in this subsection. In the proposed strategy all the inverters synchronously inject a high frequency signal. The inverters dynamically readapt their mode of operation between voltage and current injection, according to their location and to the grid condition. The model used for the analysis is first presented. Combined voltage/current injection, synchronization of the high frequency signals and parallel operation of inverters are analyzed in further subsections.

### 4.7.3.1 Grid model

The microgrid model shown in Fig. 4.75 will be used for analysis and simulation purposes. It is observed that the microgrid has a ring configuration, with node k being the point of common coupling (PCC). The mathematical model of the grid is given by (4.46), where ZFk is the filter impedance between each inverter participating in the strategy (i.e. injecting a high frequency voltage/current) and the microgrid, ZLk-1k is the line impedance between nodes k-1 and k, Zlk is the load impedance in node k, Zg is the grid impedance and vhfk is the high frequency voltage injected by the inverter at node k.

### 4.7 Coordinated Operation of Parallel-Connected Inverters for Active Islanding Detection Using High-Frequency Signal Injection

The model in Fig. 4.75 and (4.46) can be used to analyze the system response to the high frequency signals by just replacing the impedances and voltage sources by their corresponding high frequency values. As discussed for the models shown in Fig. 4.73, the grid voltage as well as the voltage for any generating unit or load not injecting the high frequency voltage/current can be made equal to zero, as they do not contain a high frequency component. Therefore, the grid as well as passive loads or generators are replaced by an equivalent impedance connected to ground. As consequence of this, the grid impedance Zq is connected to ground in the grid side and is measurable (see Fig. 4.75). This is true even in the event that no net power flows through the PCC in grid operation (the microgrid voltage at the PCC) in island condition exactly matches the grid voltage). It is also noted that the model presented in Fig. 4.75 assumes that there is a load connected at each node. This corresponds to the *microgrid* case discussed in subsection 4.7. The model in Fig. 4.75 and (4.46) can be easily adapted to the *multiinverter* case discussed in section 4.7.2 by making the load impedances equal to infinity. This is the case when most or all of the power is evacuated to the grid at the PCC (e.g. distributed photovoltaic generation systems [141]).

It is finally noted that (4.46) assumes that the inverters operate as a *voltage source*. For inverters operating in the *current source* mode, (4.46) can be algebraically rearranged by moving the corresponding current *iFk* to the left term (inputs vector) and the inverter voltage *vhfk* to the right side (outputs vector) of the equation respectively.

#### 4.7.3.2 Combined high frequency voltage/current signal injection

A means to combine current and voltage injection is to use a realizable references anti-windup strategy [38]. This is schematically shown in Fig. 4.76. The high frequency current magnitude  $i_{hf_{max}}$  is commanded to a synchronous PI current regulator rotating at  $\omega_{hf}$  (see (1) and Fig. 4.76). If the voltage required to supply the commanded current is lower than the established voltage limit, i.e.  $u < u_{hf_{max}}$ , the current injection mode works normally. This will occur when  $Z_{hf}$  is small. On the contrary, if the  $u > u_{hf_{max}}$ , the voltage is limited to  $u_{hf_{max}}$ . This will occur when  $Z_{hf}$  is large. The realizable references block in Fig. 4.76 guarantees a smooth transition between both modes of operation [38].

Fig. 4.77 schematically shows the injected high frequency voltage at the inverter terminals (commanded), the high frequency voltage at the filter output and the resulting high frequency current, as a function of the filter impedance vs. equivalent high frequency impedance ratio. When the



Figure 4.76: Power converter, including high frequency current regulator, *realizable references* block, and PLL for the synchronization of the high frequency signal with the grid fundamental voltage.



Figure 4.77: Combined voltage source and current source modes of operation.

impedance  $Z_{hf}$  is large the inverter output voltage is limited, i.e. it operates as a *voltage source*. As  $Z_{hf}$  decreases ( $ZF/Z_{hf}$  increases), once the high frequency current reaches its rated value the inverter works as a *current* source.

For the implementation of the strategy,  $i_{hf_{max}}$  is selected first. The relationship between  $i_{hf_{max}}$  and  $u_{hf_{max}}$  is set to be (4.50), where ZF is the (known) filter impedance and  $\hat{Z}_{hf}$  is the preset value of the high frequency impedance at which the change between voltage source and current source occurs. For the simulation and experiments carried out in this section,  $i_{hf_{max}}$ was set to 1.5% of the rated current and  $hf = 0.35 \cdot ZF$ ,  $u_{hf_{max}}$  being obtained



Figure 4.78: Schematic representation of the transition between island and grid conditions. a) Magnitude of the high frequency voltage and b) current injected for islanding detection; c) high frequency impedance; d) secondary high frequency voltage.

from (4.50).

$$u_{hf_{max}} = i_{hf_{max}} \left( Z_F + \hat{Z}_{hf} \right) \tag{4.50}$$

Fig. 4.78 shows the simulated response of the method. For island mode, the voltage is limited (Fig. 4.78a). For grid operation, the impedance seen by the inverter is small and current injection works normally. The high frequency current command is equal to the nominal value  $i_{hf_{max}}$ . It is remarked that the transition between *voltage* and *current source* modes occurs smoothly, no reconfiguration of the high frequency signal injection mechanism being needed (Fig. 4.78c). Experimental results showing the operation of this method are provided in subsection 4.7.4.

#### 4.7.3.3 Synchronization of the high frequency signal injection

If multiple inverters inject simultaneously, synchronization of the high frequency signal for each inverter is highly advisable. This will reduce the *differential* high frequency voltage among inverters. Otherwise, the resulting differential high frequency voltage will cause high frequency currents circulating among the inverters. This will adversely affect to the power quality (THD), also making more challenging the detection of grid/island condition.

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Phase-synchronization of the inverters can be done by selecting the high frequency voltage to be an integer multiple of the grid frequency. A cascade complex coefficient filter with complex *PLL* (CCCF-CPLL) 3.6 was used for this purpose (see Fig. 4.76).

Errors in the synchronization of the high frequency signals are likely to occur in practice due to several reasons. Differences in the voltage angle in different parts of the network and/or harmonics/unbalances in the grid voltage can affect to the PLL angle estimation and produce an unsynchronized injection of the high frequency voltages. Adverse effects of this would include errors in the estimated high frequency impedance and an increase of the THD due to high frequency currents circulating among the inverters.

Errors due to differences in the voltage angle are expected to be of little importance in practice. The angle difference will be small for inverters operating near to each other. For inverters located farther away from each other, the angle difference and the impedance between the inverters will increase nearly proportionally, roughly cancelling to each other. It is also noted in this regard that in networks spread over a smaller area, the impedances are still inductive but have a significant resistive component [64].

A similar argumentation can be used to analyze the effects of harmonics/unbalances. Neighboring inverters should experience similar disturbances and react in a similar manner, thus limiting the risk of differential high frequency voltages among inverters. However, the behavior in this case will strongly depend on the PLLs response (bandwidth, harmonic rejection capability, etc). Inverters with different PLL designs might respond differently to harmonics, transients, etc., increasing the risk of interference. A thorough analysis of this issue has not been carried out yet.

### 4.7.3.4 Parallel operation of the inverters

Inverters using the combined voltage source/current source modes can be directly connected in parallel. The result is a microgrid in which all the inverters participating in the islanding detection strategy inject the high frequency signal. Each inverter automatically selects the mode of operation as a function of the high frequency impedance  $Z_{hf}$  present at its terminals. Fig. 4.79 show an example obtained using the model in Fig. 4.75, (4.46) for the case of grid (left) and island operation (right). In the example shown in Fig. 4.79, the microgrid consists of seven nodes radially connected with the PCC connected to node #1. Each inverter uses the configuration shown in Fig. 4.76. The system parameters are the same as for the experimental

Grid	380 V, 50 Hz, Scc=2 MVA
Inverters	380 V, 30 kVA, 10 kHz.
Load	15 kW
$u_{hf_{max}}$	13 V (0.0325 pu), 250 Hz (5w $e$ )
$i_{hf_{max}}$	1 A (0.0155 pu)
Line impedance $ZL$	2Ω
LCL filter	2.4/2.3 mH (inverter/grid side), C=30uF

Table 4.11: Experimental setup parameters

results (see Table 4.11). The bars in Fig. 4.79(a) show the inverter output voltage uhf and line voltage uLhf (filter output voltage) for each node. Fig. 4.79(c) shows the filter, line and load high frequency current. The limits for the high frequency voltage  $u_{hf_{max}}$  and current  $i_{hf_{max}}$  are indicated in Fig. 4.79(a) and 4.79(c) (see Fig. 4.77 and (4.51)). Node #1 corresponds to the PCC, the load current in this node coinciding therefore with the high frequency current circulating into the grid.

It is observed from Fig. 4.79(a)-left and 4.79(c)-left that for grid-connected case inverters in nodes #1, #2, and #7 operate in the *current source* mode. Due to their closeness to the PCC the impedance seen by these inverters is small, their high frequency current being limited to  $i_{hf_{max}}$ . On the contrary, nodes #3 to #6 operate in the *voltage source* mode as they are further from the PCC. It is remarked again that the transition between *voltage source* and *current source* occurs smoothly, no reconfiguration of the injection mechanism being needed.

#### 4.7.3.5 Islanding detection and islanding notification

Islanding is detected from the measured high frequency impedance. Fig. 4.79(e) shows the high frequency impedance seen at the inverters terminal (4.51) and filters output (4.52).

$$Z_F + Z_{hf} = \frac{u_{hf}}{i_{F_{hf}}} \approx \frac{u_{hf}^*}{i_{F_{hf}}} \tag{4.51}$$

$$Z_F + Z_{hf} = \frac{u_{L_{hf}}}{i_{F_{hf}}}$$
(4.52)



Figure 4.79: Schematic representation of the microgrid, operating in gridconnected (left) and islanding (right) modes. a) high frequency voltages, b) high frequency currents and c) high frequency impedances. The load current in node #1 corresponds to the high frequency current circulating into the grid. The bars in subplots a) to b) are referred to the maximum high frequency voltage  $u_{hf_{max}}$ , current  $i_{hf_{max}}$  and output filter impedance ZF, respectively.

Since  $Z_{hf}$  is the variable reflecting the changes between grid and islanding modes, (4.52) would be used in principle for islanding detection. However, using (4.51) has the advantage that the commanded high frequency voltage can be used instead of the high frequency component of the measured line voltage needed in (4.52). This slightly simplifies the required signal processing. Still both options are expected to give similar results.

Some expected facts are observed in Fig. 4.79. For the case of gridconnected operation, the high frequency impedances for each node (both  $Z_{hf}$  and ZF + Zhf in Fig. 4.79(e)) depend on the node location relative to the PCC. The impedances for nodes closer to the PCC are significantly smaller. The largest variations of the high frequency impedance between grid (Fig. 4.79(e)-left) and island connection (Fig. 4.79(e)-right) occur at nodes closer to the PCC.

Islanding detection is currently based on the rate of variation of  $Z_{hf}$  with time, i.e.  $\Delta Z_{hf} / \Delta t$ . Comparison of  $Z_{hf}$  with a threshold might also potentially be used 4.3. Islanding detection will be easier and more reliable for nodes closer to the PCC. On the contrary, islanding detection might be difficult for nodes far from the PCC in large microgrids. Thus, inverters working in the *current source* mode would be in principle better candidates to detect islanding than inverters working in the *voltage source* mode.

A possible strategy would be to enable only inverters working in the *cur*rent source to inform on the grid condition to the rest of inverters present in the microgrid. A secondary high frequency signal would be for this purpose. Inverters working in the *current source* mode would detect islanding by measuring a positive  $\Delta Z_{hf}$  over a predefined time window. Once islanding is detected, they would inject the secondary high frequency signal uhf2. On the contrary, if inverters injecting the secondary high frequency voltage detect the change between islanding and grid-mode from the measured  $\Delta Z_{hf}$ , they would discontinue injecting the secondary high frequency voltage. Injection of the secondary high frequency voltage is schematically shown in Fig. 4.78d. Details on the use of the method can be found in 4.3,4.4. This strategy has not been studied in detail, further analysis would be needed to verify its viability and performance.

### 4.7.4 Experimental results

The proposed islanding detection strategy has been tested using the experimental setup shown in Fig. 4.80. The parameters are summarized in



Figure 4.80: Experimental setup, consisting of two inverters. Current regulators needed for the control of the fundamental current are not shown.

Table 4.11. Both inverters are identical and use IGBTs. All the control (current regulators, synchronization, etc.) is implemented on a TMS320F28335 DSP.

Fig. 4.81 shows the transition between island and grid modes. Fig. 4.81(a) and Fig. 4.81(c) show the commanded and filter output voltages for both inverters. Fig. 4.81(b) and Fig. 4.81(d) show the corresponding high frequency currents. The magnitude of the high frequency current  $i_{hf_{max}}$  is set to 1 A (1.5% rated current). It is observed from Fig. 4.81(b) that during islanding both inverters operate in the *voltage source* mode, with  $u_{hf_{max}} = 13$  V. During island operation Inverter #1 changes its mode of operation to the current source mode, the high frequency current magnitude being limited to  $i_{hf_{max}}$ . Inverter #2 keeps operating in the *voltage source* mode. This is due to the line impedance between Inverter #2 and the PCC.

Fig. 4.81(e) show the magnitude of the corresponding high frequency impedances. It is observed that for this particular case the change between grid and island modes is readily detected by both inverters. This is due to the fact that the line impedance ZL is small compared to the impact that the change between grid and island operation has on the equivalent impedance  $Z_{hf}$ . It is noted however that, for the case of large microgrids, inverters far from the PCC might experience significantly smaller variations of the equivalent impedance. This will make them less reliable for islanding detection.



Figure 4.81: Experimental results showing the response of the proposed method during island-grid transitions.

### 4.8 Conclusions

This chapter provides a full review and analysis of the state-of-the art of islanding detection techniques, both for single and three phase systems. It has been shown the importance to detect the islanding situation as soon as possible to increase the customer availability, reliability and power quality.

Four islanding detection techniques have been proposed: three for threephase systems and one both for single and three-phase systems. All of them are based on the injection of a high frequency signal. The islanding condition being detected based on the high frequency impedance.

The first method, proposed in section 4.3, uses two high frequency signals: one for high frequency impedance detection and other to notify to the remaining inverters in the microgrid when it is isolated from the main grid. It works efficiently but it does not include mechanism to reassign the master-slave roles if the master fails.

To overcome this limitation, the method proposed in section 4.4 proposes a technique to reassign a new master unit if the actual master unit fails, without dedicated communication. It is also proposed a high impedance mode of operation, in which each the inverters does not consume high frequency current.

The non-linear behavior of the inverter was also proposed as a reliable mechanism to detect the islanding condition in section 4.5. The advantage of this method is that it does not require the high frequency voltage injection, the distortion induced by the inverter dead-time being used for this purpose.

The use of a pulsating voltage high frequency signal has been proposed in section 4.6. The advantage of this method is that it can be used indistinctly in three phase and single phase systems. Additionally, this excitation waveform has been shown to be useful for fault detection in three-phase systems.

Finally, a islanding detection technique for multi-inverter operation has been presented in section 4.7. In the proposed method all inverters inject the high frequency signal in phase. Each inverter can inject the high frequency signal both in voltage or current control mode. The method provides soft switching capability from voltage to current control mode and vice-versa, showing excellent islanding detection performance in a multi-inverter scenario.

### Chapter 5

### Power quality in microgrids

### 5.1 Introduction

Microgrid/grid power quality is an important aspect that needs to be considered, as it affects to generators, distributors, and end-users of the electric power. The increasing use of electronic switching equipment is contributing to voltage and/or current waveform distortion increase (power quality decrease), i.e. harmonic increase [55], also the use single-phase loads increases the waveform distortion.

Several approaches have been suggested for harmonic compensation (voltage and/or current), i.e. power quality improvement, in microgrids. The use of passive filters or dedicated equipment like active power filters [84] have been traditionally used. Instead of using a dedicated equipment, the DG units can be alternatively used to improve the microgrid power quality, both centralized and distributed control strategies have been proposed for this purpose [121], [120].

In addition to the typical power quality approach, i.e. voltage and/or current harmonics compensation, another critical power quality issue occurs when the physical connection between a DPG unit and the microgrid/grid is performed; having the same voltage in both sides of the breaker that joins the microgrid and the main grid is required to avoid overcurrents that may damage the DPG or tripping the protections. This is not guaranteed in distorted grids when the synchronization is realized using only the positive sequence voltage, which is the most common synchronization technique.

This chapter provides a brief summary of the existing power quality techniques for harmonic compensation issue. At the same time, it proposes a



Figure 5.1: Location

collaborative technique for power quality improvement and a synchronization and smooth connection technique to highly distorted grids/microgrids

### 5.2 Harmonic compensation techniques for DPG units

The presence of power converters, non-linear and single-phase loads increases the microgrid PCC voltage and current harmonics. The most common harmonic compensation techniques are reviewed and discussed in this section.

### 5.2.1 Passive filters

Passive filters have been extensively used due to their easy of implementation and tuning. The passive filtering stages typically can be series connected (Fig. 5.1(a)) if voltage harmonics need to be removed, or parallel connected (shunt, Fig. 5.1(b)) if current harmonics need to be removed. Other hybrid series-parallel configurations can be used, usually referred as hybrid passive filters (see subsection 2.3).

The use of passive filtering stages present some drawbacks due to the filter resonances which may interfere with other elements present in the microgrid, finding a good location to place them not being a trivial issue.

### 5.2.2 Active filters

An active power filter is a dedicated power converter that is used to compensate current and/or voltage harmonics by injecting harmonic components. The same topologies as the passive filters case can be found, i.e. parallel, series or hybrid; parallel active power filter compensates current harmonics while series active power filters compensate voltage harmonics.

The use of active power filters presents some appealing properties, as they can operate in microgrids with grid frequency variations. In addition they are able to control a large number of harmonics at the same time. On the other hand, its costs is typically higher than passive filters.

### 5.2.3 Use of parallel DPG units

A novel technique developed in the last decade makes use of the DPG units to improve the power quality. All of the DPG units connected in parallel to the PCC can inject harmonic currents (as an active power filter does), compensating NLLs current harmonics.

The key point of this strategy is how to balance the harmonic current between DPG units, both centralized and distributed (local) control strategies have being already proposed [121], [120]. Different metrics can be used to select the harmonic current magnitude injected by each DPG units, e.g. based on its rated power, its available current or the distance to the PCC.

In addition to those metrics, the virtual impedance concept has been recently proposed as a cooperative mechanism to share unbalance and/or harmonic compensation without the need of a centralized control [127], [62] among parallel connected DPG units. The main drawback of the virtual impedance concept is that it can only be applied to voltage source inverters operating in voltage control mode (VSI-VCM, subsection 2.5, Fig. 2.15), its use with voltage source inverters working in current control mode (VSI-CCM, subsection 2.5, Fig. 2.15) and also in current source inverters (CSIs) not being feasible.

### 5.3 Connection and disconnection of DPG units to the main grid

A DPG unit or a whole microgrid can operate connected or isolated from the main grid. Transition from grid-connected to island operation, i.e. disconnection, has been the focus of significant research efforts [115], [54], [77], [48], [140]. However, less attention has been paid to the transition from island to grid-connected operation. Connection between a DPG unit or a whole microgrid to the main grid will require an accurate synchronization between both of them.

Synchronization, i.e. the measurement of the grid/microgrid voltage magnitude, frequency and phase angle, by all DPG units will be therefore key to guarantee a robust and stable operation of the system and adequate power quality. Synchronization methods typically try to isolate the positive sequence component of the fundamental voltage, often implementing mechanisms for the compensation of disturbances like harmonics and voltage unbalances for this purpose. Having the same voltage in both sides of the breaker is needed to avoid overcurrents at the connection instant. This is not guaranteed in distorted grids when the synchronization is realized using the positive sequence voltage only, which can be of especial importance in weak grids, e.g. those located at the end of long distance transmission lines for centralized power distribution scenarios or near low-power DPG units in distributed power generation scenarios.

# 5.4 Virtual admittance for voltage harmonic compensation in microgrids

This section presents a method that uses the virtual admittance concept for harmonic and/or unbalance compensation sharing among parallel connected DPG units. This strategy responds to the same physical principles as virtual impedance concept, however contrary to the virtual impedance concept it can be used in VSIs-VCM, VSIs-CCM and CSIs.

### 5.4.1 Virtual admittance concept

Fig. 5.2 shows the inverter Norton equivalent circuit, including the parallel connection of a virtual admittance at the inverter output. In principle, the virtual admittance could be connected either at the inverter output or at the filter output. Since the proposed method is used for unbalance and harmonic compensation, the virtual admittance cannot be connected at the filter output. This is due to the fact that when the harmonic/unbalance are fully compensated (i.e. no harmonic content at the PCC exists), the virtual admittance will not consume any virtual current, and will not contribute therefore to the harmonic sharing issue. Consequently, the virtual admittance needs to be connected at the inverter output.

Fig. 5.3 shows the schematic representation of a three-phase VSI feeding an LCL filter, the proposed control strategy is marked in red. The method shown in Fig. 5.3 can be applied both to VSI-CCM and VSI-VCM. A PI resonant controller PI-RES (2.13), Fig. 2.19), is used to control the inverter output current, including fundamental and harmonic components.



(a) Detailed block diagram



(b) Simplified block diagram

Figure 5.2: Inverter Norton equivalent circuit with parallel virtual admittance



Since the virtual admittance Yv is connected at the inverter output and in parallel with the filter and the load, it will affect in principle to the current phase of the overall output current, and consequently to the inverter output power factor, as shown by (5.1).

$$i_{inv_{dqh}} = i^*_{dqh} - Y_v u_{inv_{dqh}} \tag{5.1}$$

$$|i_{y_v}| = |Y_v| \cdot |u_{inv_{dqh}}| \tag{5.2}$$

$$i_{inv_{dqh}} = i_{dqh}^* - |i_{y_v}| \cdot e^{j \cdot \phi_{i_{dqh}^*}}$$
(5.3)

To prevent from this to happen, the magnitude of the current consumed by virtual admittance (5.2) is forced to be in phase with the overall current command  $i_{dqh}^*$  and the actual inverter current command  $i_{inv_{dqh}}$ . This is called a *non-phase-disturbing* virtual admittance. To do this, the phase angle of the current command  $\phi_{i_{dqh}^*}$  (see Fig. 5.3) is obtained and a unit vector  $e^{j\phi_{i_{dqh}^*}}$ is built. This unit vector is then multiplied by the magnitude of the current consumed by the virtual admittance  $|i_{Y_v}|$ , therefore guaranteeing that the consumption of the virtual current does not change the inverter output power factor.

Finally, the value of  $|i_{Y_v}|$  must not change the sign of the current reference (e.g. causing a phase shift between  $i_{dqh}^*$  and  $i_{inv_{dqh}}$  of  $180^{\circ}$ ). To prevent from this to happen  $|i_{Y_v}|$  is limited to  $|i_{dqh}^*|$ .

It is finally noted that the same current control can be used with VSI-CCM and VSI-VCM, the only difference being how the current command  $i_{i_{dq1}}^*$  is obtained.

For the case of a VSI-VCM,  $i_{i_{dq1}}^*$  comes from an outer voltage controller (see subsection 2.5), while for the case of a VSI-CCM, it can be directly commanded, (see subsection 2.5) or can come from an outer controller (e.g. power controller). In all cases, the mode of operation of the inverter does not affect to the proposed method.

## 5.4.2 Harmonic compensation using virtual admittance loop

The main objective of the proposed method is to eliminate harmonic content and unbalances of the voltage PCC, sharing the required actions among several inverters. The virtual impedance allows in this regard to adjust the contribution of each inverter to the overall current needed to clean up the voltage at the PCC. Fig. 5.4 shows the scenario that will be used both for simulation and experimental verification. It consists of two LCL-based VSIs working in parallel and a central controller. One of the converters will act as a VSI-VCM (e.g. master inverter which sets the voltage magnitude and frequency), meanwhile the second inverter operates as a VSI-CCM (e.g. slave inverter). The master inverter feeds a local resistive linear load and a non-linear-load (NLL), while the slave inverter feeds a local resistive linear load. The proposed virtual admittance control technique (see Fig. 5.3) is implemented in the local controller while the central controller will implement the voltage control, transmitting both the resulting current command as well as the virtual admittance set for each converter (see Figs. 5.4 and 5.5).

The voltage harmonics to be compensated for are measured at the PCC, transformed to a frame synchronous with the frequency of each harmonic (dqh, see Fig. 5.3) and transmitted to the central controller using a communication interface, i.e. a *WiFi* link. Transforming the voltage harmonics to the synchronous reference frame has the advantage that the signals to transmit are DC quantities, relatively low transmission bandwidths being acceptable. On the contrary, transmitting the measured voltages in the stationary reference frame would require significantly higher transmission bandwidths, what might be a concern for the practical implementation of the method.

Fig. 5.5 shows a simplified scheme of the proposed centralized sharing control. The central controller transmits to each inverter (local control) the harmonic current command and the virtual admittance value. Discussion on the criteria for the selection of the virtual admittances is presented later.

Fig. 5.6 shows the proposed control diagram of the central controller. The reference  $(u_{out_{dq_h}}^*)$ , see Fig. 5.6) for each harmonic included in the control is typically set to 0, to cancel that harmonic at the PCC. A synchronous PI regulator is used for this purpose.

The output of the PI controller  $i_{dqh}^*$  is transmitted to each local controller (see Fig. 5.6), where it is fed to the virtual admittance controller, as shown in Fig. 5.3. The output current command in the dqh reference frame,  $i_{inv_{dqh}}$ , is then rotated to the fundamental synchronous reference frame  $(i_{inv_{dqh}})$ . This



Figure 5.4: Microgrid setup used for simulation and experimental verification.

current reference feeds an LCL-decoupling block that is used to decouple the output LCL filter effect using (5.4), such that all the inverters inject in phase at the PCC.

It is noted in this regard that the LCL filter decoupling is often not required for the compensation low-order harmonics, since the LCL filter effect is almost negligible at low frequencies. In case of low cutoff frequency LCL filters or when high-order harmonics are compensated, the LCL filter effect is not negligible, decoupling being then necessary.

$$i_{inv_{dq1h}}^{*} = \frac{CL_{inv}s^{2} + CR_{L_{g}}s + CR_{c}s + 1}{CR_{c}s + 1}i_{inv_{dq1h}} + \frac{Cs}{CR_{c}s + 1}u_{out_{dq1h}}$$
(5.4)

### 5.4.3 Simulation results

Table 5.1 and Fig. 5.4 shows the simulation setup. It consists of two VSIs working in parallel (VSI-CCM and VSI-VCM). The VSI-CCM feeds a local resistive three-phase load meanwhile the VSI-VCM feeds also a local resistive three-phase load and a nonlinear load (NLL, Fig. 5.4 and 5.7).

The MCCF-PLL (subsection 3.4.1.3) method has been used for the synchronization of the power converters and to extract the voltage harmonic magnitude to be compensated, i.e. the  $-5^{th}$  and the  $7^{th}$  harmonics in this work. The centralized PI regulator and the local PI-RES parameters are shown in Table 5.1.



Figure 5.5: Proposed centralized sharing control.



Figure 5.6: Block diagram of the proposed centralized harmonic compensation strategy. Note that this scheme is repeated for each harmonic being canceled.



Figure 5.7: Nonlinear Load (NLL) block diagram.

Table 5.1: Setup parameters

VSI-VCM Inverter		VSI-CCM Inverter	
50kW	Rated power	50kW	
$0.052 \ \Omega$	Capacitor ESR	0.052 Ω	
0.05 Ω	Inductor ESR	0.05 Ω	
2.4 mH	Inverter-side inductor	2.196 mH	
$10 \ \mu F$	Capacitor filter	$10 \ \mu F$	
1.6 mF	Grid-side inductor	2.196 mF	
Centralized controller			
0.07	Ki <sub>-5</sub>	0.9	
0.07	Ki <sub>7</sub>	0.9	
Local PI-RES			
8	Ki	3000	
1	С	300	
6			
	$\begin{tabular}{ c c c c c } ter & & & \\ \hline 50kW & & \\ 0.052 \ \Omega & \\ 0.05 \ \Omega & \\ 2.4 \ mH & \\ 10 \ \mu F & \\ 1.6 \ mF & \\ \hline 1.6 \ mF & \\ Centralize & \\ \hline 0.07 & & \\ 0.07 & \\ Local & \\ \hline 8 & \\ 1 & \\ 6 & \\ \hline \end{tabular}$	terVSI-CCM Inver $50kW$ Rated power $0.052 \Omega$ Capacitor ESR $0.05 \Omega$ Inductor ESR $2.4 \text{ mH}$ Inverter-side inductor $10 \mu$ FCapacitor filter $1.6 \text{ mF}$ Grid-side inductorCentralized controller $0.07$ $Ki_{-5}$ $0.07$ $Ki_7$ Local PI-RES $8$ $Ki$ $1$ $C$ $6$ $Ki$	



Figure 5.8: Simulation results. Harmonic compensation for different values of the virtual admittance.

Fig. 5.8 shows the simulation results using the proposed strategy, for different values of the virtual admittance. At t=0.3s switch S is closed (Fig. 5.4) and at t=0.6s compensation of  $-5^{th}$  and  $7^{th}$  harmonics is enabled. Fig. 5.8(a) shows the commanded virtual admittances.

Figs. 5.8(b) and 5.8(c) show the magnitude of the  $-5^{th}$  ( $|i_{i-5}|$ ) and  $7^{th}$  ( $|i_{i7}|$ ) harmonics of the current injected by each inverter. Fig. 5.8(d) shows the total harmonic distortion (THD) and the harmonic distortion of each harmonic (until  $11^{th}$  order), both in negative and positive sequence. The voltage harmonic distortion is defined as the ratio between the  $n^{th}$  harmonic and the positive sequence voltage components.

It is observed from Figs. 5.8(b) and 5.8(c) that from t=0.6s to t=1.5s the magnitude of the current harmonics injected by both inverters is the same. This is due to the fact that both virtual admittances are equal to each other and equal to zero. From t=1.5s to t=2.5s, the VSC-VCM decreases the magnitude of the injected current harmonics due to its virtual admittance being bigger than that of the VSC-CCM. This situation is reversed from t=2.5s to 3.5s. As expected the inverter with the lower virtual admittance value injects more current while the inverter with the highest virtual admittance injects lower current. At t=3.5s, the injected harmonic currents return to the same values as from t=0.6s to 1.5s (i.e. virtual admittances set to zero).

For t>5.5s, the virtual admittances of the VSI-CCM and VSI-VCM are set to 0.01  $\Omega^{-1}$  and 1000  $\Omega^{-1}$  respectively (Fig. 5.8(a)). As can be seen in Figs. 5.8(b) and 5.8(c), when the virtual admittance of an inverter is set to infinite (i.e. 1000  $\Omega^{-1}$ ), that inverter (VSI-VCM) does not inject any harmonic current, since its virtual admittance is *consuming* all the inverter current. Thus, the rest of the inverters (VSI-CCM) are required to support the harmonic compensation task, supplying all of the necessary current to compensate the voltage harmonics.

It is observed from Fig. 5.8(d) that once the compensation is enable (t=0.6s), the  $-5^{th}$  and  $7^{th}$  voltage harmonics are fully cancelled, the THD decreasing from 7.9% to 2%. It is also noted from Fig. 5.8 that changes in the virtual admittance result in a transient, which lasts around 500 ms. after that time, the controls are readapted to the new configuration and the voltage harmonics are fully cancelled again. It is noted in this regard that the centralized controller has been intentionally set to a relatively low bandwidth (10 Hz), in order to emulate a low-bandwidth communication channel.

Finally, Figs. 5.9(a) and 5.9(b) show the phase voltages at the PCC before and after the compensation is enabled respectively. It is observed that the proposed method definitely removes the high order harmonics of the PCC


Figure 5.9: Simulation results. Detail of the PCC voltages.

voltage.

It can be readily observed that the higher the virtual admittance and the higher the output LCL filter impedance of the inverter are, the lower the current injected by the inverter is (see Figs. 5.8(b) and 5.8(c)). This is due to the fact that the inverter needs more voltage to supply the same amount of current, and therefore the virtual admittance consumes also more virtual current. If all the virtual admittances are set to the same value and all the output impedances (e.g. LCL filter impedance) are equal, all the inverters will injected the same harmonic current.

However, different results would be expected if the parameters of the lines connecting each inverter and the PCC are different. To verify this issue a transmission line (TL) which parameters are  $R_{TL} = 6 \ \Omega$  and  $L_{TL} = 5 \ mH$ has been placed between the VSI-VCM inverter and the PCC. As it can be observed from Fig. 5.10(a), until t=2s both virtual admittances are set to zero, and both inverters inject almost the same current (Figs. 5.10(b) and 5.10(c)). Once the virtual admittances are changed (t=2s), it is observed that the VSI-VCM injects less harmonic current than the VSI-VCM, due to the VSI-VCM highest virtual admittance value ( $Yv=0.05 \ \Omega^{-1}$ ). However in



Figure 5.10: Harmonic compensation simulation results.

this case the VSI-VCM inverter injects less current (0.43A of  $-5^{th}$  harmonic, Fig. 5.10(b)) than in the previous simulation (0.58A of  $-5^{th}$  harmonic, Fig. 5.8(b)). This is due to the VSI-VCM higher output impedance (LCL+TL), which results in a lower current for the same harmonic voltage. It is important to note that the same current as the previous experiment could be obtained using a different virtual admittance value. This behavior is clearly observed when both inverters have the same virtual admittance value (t>3s): the VSI-VCM inverter always injects less current than the VSI-CCM inverter. It is also observed from Fig. 5.10(b) (t>4s) that the higher the value of the virtual admittance of both inverters is, the lower the current injected by the inverter with the highest output impedance is.

### 5.4.4 Experimental results

Laboratory-scaled experimental results are given in this subsection, details of the experimental setup can be found in Fig. 5.4 and Table 5.1. The central controller (Figs. 5.2 and 5.4) has been programmed in a computer using *Matlab-Guide*. The PCC voltage, current references and virtual admittance values are shared between the central controller and the DSP controlling each inverter using a WiFi link. The sampling frequency of the centralized controller is 5 Hz.

Fig. 5.11 shows the response of the proposed method. Fig. 5.11(a) shows the virtual admittance values used in this test, they are the same as for the simulation results in Fig. 5.8. On the other hand, Fig. 5.11(b) shows the magnitude of the current injected by each inverter to compensate for the  $-5^{th}$  harmonic( $|i_{i-5}|$ ).

At t=1s the harmonic compensation strategy is enabled,  $-5^{th}$  and  $7^{th}$  harmonics being compensated. It is observed from Fig. 5.11(b) that, as expected, both inverters inject a similar amount of harmonic current when the virtual admittances are set to zero. Conversely, the inverter with the larger virtual admittance injects less harmonic current to the NLL. The harmonic distortion of the  $-5^{th}$  and  $7^{th}$  harmonics are reduced to zero once the compensation is enabled, reducing the THD from 8.2% to 2% (see Fig. 5.11(c)).

For t>30s the virtual admittance of the VSI-CCM is set to 0.01  $\Omega^{-1}$ and to 1000  $\Omega^{-1}$  for the VSI-VCM (see Fig. 5.11(a)). It is observed from Fig. 5.11(b) that when the virtual admittance of an inverter is set to infinite (VSI-VCM, see Fig. 5.11(a)), that inverter does not participate into the compensation task. Thus, the rest of the inverters (i.e. VSI-CCM) are required to



Figure 5.11: Harmonic compensation experimental results.



Figure 5.12: Harmonic compensation experimental results.

support the harmonic compensation task, supplying all the necessary current to compensate the voltage harmonics.

It is observed that the experimental results are in good agreement with simulation results (Fig. 5.8). One reason for the differences between simulation and experimental results comes from the fact that the required compensation current for each harmonic (Fig. 5.11(b)) is close to the sensitivity limit of the current sensors, decreasing the signal-to-noise ratio and reducing therefore the accuracy of the PI-RES current control loop in the real implementation. This effect does not occur in simulation.

Finally, Fig. 5.12 shows the experimental results when different line impedances exist between each inverter and the PCC. The transmission line was emulated using a series connection of a resistance ( $R_{TL} = 2 \ \Omega$ ) and an inductance ( $L_{TL} = 2 \ mH$ ), placed between the output LCL filter of the VSCI-CCM and the PCC.

Fig. 5.12(a) shows the virtual admittances used in this experiment. Until t=7.5s both virtual admittances are set to zero, the experimental results follow the same tendencies as the simulation ones (see Fig. 5.10(b)): both inverters inject the same current. For 7.5<t<15s the virtual admittances are changed, the VSI-VCM has the highest virtual admittance value (Yv=0.05  $\Omega^{-1}$ ), therefore it injects less harmonic current than the VSI-VCM.

For t>15s, both inverters have the same virtual admittance value, therefore the VSI-VCM injects more current than the VSI-CCM inverter. As in simulation results happens, the higher the value of the virtual admittance of both inverters is, the lower the current injected by the inverter with the highest output impedance is (VSI-CCM), see Fig. 5.12(b). This is a very interesting result, since it implies that the nearer the inverter to the PCC is, the more current it injects, hence minimizing the transmission losses.

Simulation and experimental results demonstrate the viability of the proposed methodology for cooperative harmonic compensation and power sharing. At the same time, the proposed method shows a good applicability for transmission losses reduction, forcing the inverters located far away to the PCC to inject less current than the inverters located near the PCC.

## 5.5 Connection of DPG units to distorted networks

This section proposes a method for synchronization and smooth connection of DPG units to highly distorted grids.

The proposed method will be shown to reduce the induced overcurrents due to the instantaneous voltage mismatch, improving therefore the power quality. In the proposed method, both the positive sequence as well as unbalanced and harmonic components of the grid voltage are considered for the synchronization with the goal of reducing the voltage mismatch at the instant that the breaker closes.

Once the connection process is finished, the harmonic components are gradually removed from the reference used for the synchronization, the positive sequence component of the voltage being eventually used to guarantee precise control the active and reactive power flows.

### 5.5.1 Connection of DPGs to a distorted utility grid using the fundamental voltage

Fig. 2.15 (Chapter 2) shows a generic control block diagram of a voltage source converter working in voltage control mode (VSC-VCM). It consists of an inner current loop (block in red) that controls the inverter output current  $(Reg_i)$  and an outer voltage loop (block in green) that controls the output filter voltage  $(Reg_u)$ .

The voltage reference,  $u_{dq}^*$  (see Fig. 2.15), comes from a synchronization algorithm, typically based on a phase-locked-loop (PLL). As widely discussed in Chapter 3, PLL algorithms implement mechanisms to compensate or eliminate unbalances or harmonics that typically exists in the grid voltage.

Fig. 5.13 shows the  $i_{dqg}$  current when a connection to a distorted grid is performed using a clean estimation of the fundamental component of the PCC. It is observed that the voltage mismatch between the breaker terminals produces an overcurrent after the breaker is closed, its magnitude being a function of the voltage difference between the DPG and the grid, the DPG output filter and the grid impedance. LC and LCL filters are the most common choice for the DPG output filter, the transient current after the connection for both filter designs is analyzed following.



Figure 5.13: Connection of a DPG to a distorted grid



Figure 5.14: Equivalent circuit of a VSC connected to a grid using an LC filter.

#### 5.5.1.1 Connection of VSCs to distorted grids through LC filters

Fig. 5.14 shows the equivalent circuit of a three-phase VSC connected to the utility grid through an LC filter. The transmission line and inductance filter are modeled by an inductance  $(L_{TL} \text{ and } L_i)$  and a resistance  $(R_{TL} \text{ and } R_i)$  respectively. The capacitor filter is modeled by a capacitance C with a series resistance,  $R_c$ .

During the synchronization process and before the breaker is closed, the microgrid voltage  $u_{dq \mu g}$  is normally made equal to the positive sequence component of the grid fundamental voltage. This means that if the grid voltage contains only a fundamental positive sequence component, no current will flow once the breaker is closed, as no differential voltage between the VSC and grid voltage exists. On the contrary, a voltage mismatch between the grid and the VSC output voltages (i.e. at the breaker S terminals, see Fig. 2.15) will exist if the grid voltage is distorted, which will result in an overcurrent once the breaker is closed.

In the following discussion, it is assumed that the grid voltage consists

of the fundamental voltage component and a single harmonic component voltage of order h and magnitude  $|u_{dq gh}|$ . It can also be realistically assumed that the capacitor harmonic current equals the grid harmonic current  $i_{dq gh} = i_{dq ch}$ , since the reference of the VSC current regulator only contains the fundamental component and the inverter inductance removes the produced high frequency overcurrent.

$$\frac{i_{dq\ gh}}{u_{dq\ gh}} = \frac{\frac{s}{L}}{s^2 + s\frac{R}{L} + \frac{1}{LC}}$$
(5.5)

$$p_1 = -\alpha + j \cdot \omega_r; p_2 = -\alpha - j \cdot \omega_r; \tag{5.6}$$

$$\alpha = \frac{R}{2L} \tag{5.7}$$

$$\omega_r = \sqrt{\frac{1}{CL} - \frac{R^2}{4L^2}} \tag{5.8}$$

$$u_{dq\ gh} = |u_{dq\ gh}| e^{j \cdot \left(\omega_{gh} - \omega_0\right) \cdot t} \tag{5.9}$$

$$i_{dq\ gh} = i_{steady} + i_{trans} = |i_{steady}| e^{j\left(\left(\omega_{gh} - \omega_0\right)t + \Theta\right)} + \frac{|u_{dq\ gh}|}{L\omega_r} e^{\alpha t} e^{j\omega_r t}$$
(5.10)

$$|i_{steady}| = \frac{|u_{dq\ gh}|}{\sqrt{R^2 + \left(\omega_{gh}L - \frac{1}{\omega_{gh}C}\right)^2}}$$
(5.11)

$$\Theta = \tan^{-1} \left( \frac{\omega_{gh} L - \frac{1}{\omega_{gh} C}}{R} \right)$$
(5.12)



Figure 5.15: Equivalent circuit of a VSC connected to a grid using an LCL filter.

The transfer function between the grid harmonic current,  $i_{dq\ gh}$ , and the grid harmonic voltage,  $u_{dq\ gh}$ , is given by (5.5), where L is the transmission line inductance  $(L = L_{TL})$ , R is the equivalent resistance of the grid and the filter capacitor  $(R = R_{TL} + R_c)$  and C is the filter capacitor. It can be safely assumed that  $\frac{R^2}{L^2} << \frac{4}{LC}$ , therefore (5.5) corresponds to underdamped system, whose poles are (5.6). The differential voltage across the breaker terminals in a reference frame synchronous with the grid frequency is (5.9), the induced current being (5.10). Note that a harmonic component at a frequency  $\omega_{gh} = h\omega_0$  in a stationary reference frame (i.e.  $\alpha\beta$ ) transforms into a harmonic component at a frequency ( $\omega_{gh} - \omega_0$ ) in a dq reference frame synchronous with the fundamental excitation. The induced current is seen to consist of a transient term and a steady state term. The time constant of the transient term is (5.7) and its resonance frequency (5.8).

The steady state term has the same frequency as the input signal and its magnitude depends on the filter and transmission line parameters (5.11) and (5.12).

#### 5.5.1.2 Connection of VSCs to distorted grids through LCL filters

Fig. 5.15 shows the equivalent circuit of a VSC using an LCL filter. The transmission line is connected between the LCL filter output and the breaker S, being modeled as in the previous subsection. The inverter is synchronized with the positive sequence component of the fundamental voltage at the PCC,  $i_{dq\,i}$  and  $u_{dq\,\mu g}$  only consisting therefore of the fundamental component.

When the breaker closes, the current to voltage transfer function is also modeled by (5.5), the equivalent inductance resulting from the series connection of the line inductance and the LCL filter grid-side inductance ( $L = L_{TL} + L_g$ ) and the equivalent resistance R being the result of the series connection of the transmission line, LCL filter grid-side inductance resistance and filter capacitor resistance, i.e.  $R = R_{TL} + R_g + R_c$ .



Figure 5.16: Proposed technique block diagram.

The time response for this case can also be described by (5.10), and is seem to consist of a transient term with a time constant (5.7) and resonance frequency (5.8), and a steady state term with the same frequency as the PCC harmonic voltage ( $\omega_{gh} - \omega_0$ ), of magnitude and phase (5.11) and (5.12) respectively.

### 5.5.2 Connection of DPGs to a distorted utility grid using fundamental and harmonic voltages

To limit the transient overcurrents following the connection between the DGs and the grid, both the fundamental and the harmonic voltage components can be considered for the synchronization strategy.

Fig. 5.16 shows control block diagram of the proposed strategy. A combination of proportional-integral (PI), (2.11) and resonant (RES) regulators, (2.14), in dq reference frame synchronous with the grid fundamental frequency are used (2.13), both for the current and voltage. The PI synchronous regulators (2.11) are used to control the fundamental voltage and current components, while each RES controller (2.14) is used to control a specific harmonic component of the voltage and current, with n being the harmonic order. It is noted that in a harmonic of order h in the stationary reference frame results in a harmonic of order n = (h - 1) in a reference frame synchronous with the fundamental component of the grid voltage.

It is also noted that as an alternative to the RES regulators, the harmonics components could be also controlled in a dq reference frame synchronous with the harmonic frequency by using PI synchronous regulators [102]. Both implementations, i.e. using PI synchronous regulators or using RES regulators, are independent of the proposed method.

The voltage reference  $u_{dq}^*$  and both the measured voltage and current



Figure 5.17: Equivalent circuit of a VSC connected to a grid using an LCL filter.

 $(u_{dq \ \mu g} \text{ and } i_{dq \ i})$  (see Fig. 5.16) are not filtered (i.e. harmonics are not removed). The NFoL-CPLL (subsection 3.7) method was used for the synchronization, as it provides disturbance rejection capability. The strategy to synchronize and connect the VSC to a distorted grid is as follows:

1. <u> $SW_1^*=ON$ ,  $SW_2^*=ON$ , Breaker S=open.</u> The PI-RES voltage controller provides the required current command  $i_{dq}^*$  (Fig. 5.16) to the PI-RES current controller to force the same voltage at both sides of the breaker terminals (fundamental and harmonics).

2.  $\underline{SW_1^*=\text{OFF}}$ ,  $\underline{SW_2^*=\text{ON}}$ , Breaker  $\underline{S=\text{closed.}}$  Once the voltage error is smaller than a certain threshold, the breaker is closed. Following this, the input of the voltage controller is made equal to zero using  $SW_1^*$  (see Fig. 5.16). By doing this, the voltage loop is disabled, the PI-RES output being locked to the instantaneous value that it has before the breaker closed.

At the same time that  $SW_1^*$  deactivates the voltage control loop, the resonant voltage controller output is gradually eliminated by multiplying the RES output (2.14) by a weighting factor (5.13) of the form shown in Fig. 5.18. By doing this, the VSC gradually decreases the amount of harmonics injected, eventually only the fundamental current being injected. The weighting factor has been selected to follow an exponential waveform, (5.13), where  $\tau$  is the time constant. Although an exponential waveform has been selected for the weighting factor, other waveforms could be potentially used. The requirement for the design of the weighting factor function is that it should meet the grid connection requirements in terms of THD.

$$h(t) = 1 \qquad t < 0s$$
  

$$h(t) = e^{-\frac{t}{\tau}} \qquad t \ge 0s$$
(5.13)

3. <u> $SW_1^*$ =OFF</u>, <u> $SW_2^*$ =OFF</u>, <u>Breaker=closed</u>: Once the current harmonics are removed, the input to the current regulator is made equal to the current



Figure 5.18: Harmonic current adaptive gain.



Figure 5.19: Proposed simulation setup.

command  $i_{dq p}^*$  coming e.g. a power control loop, Switch  $SW_2^*$  being used for this purpose.

### 5.5.3 Simulation results

The proposed method has been tested by simulation, the scenario and the configuration parameters being shown in Fig. 5.19 and Table 5.2 respectively. A programmable AC source was used to emulate the grid voltage, the grid voltage distortion consisting of a  $-5^{th}$  harmonic with a magnitude of 2.6%, which is below the limit of 4% allowed by the grid codes [11], [14], [12], [13], [5], [7], [10], [6], [3], [8], [1], [2], [9], [4] and [68]. A short transmission line (TL, see Fig. 5.19) has been used to emulate the DPG connection to the PCC. Fig. 5.20 shows the frequency response of (5.5), using LC (blue) and LCL (red) filters.

The resulting resonance frequencies (5.8) are 12.5 kHz for the LC filter and 2.25 kHz for the LCL filter respectively. It is noted that the LCL resonance frequency is typically lower than that of the LC filter since the resonance frequency decreases as the inductance that connects the capacitor filter and the PCC increases.

Symbol	Description	Value
$L_i$	Inverter side filter inductance	2.196 mH
$R_i$	Inverter side filter resistance	0.05 Ω
C	Capacitor filter	$10 \ \mu F$
$R_c$	Capacitor ESR	$0.0536 \ \Omega$
$L_g$	Grid side filter inductance	0.5 mH
$R_g$	Grid side filter resistance	0.05 Ω
$L_{TL}$	Transmission line inductance	0.02 mH
$R_{TL}$	Transmission line impedance	0.1 Ω
	Positive sequence voltage magnitude (rms)	380 V
	$-5^{th}$ harmonic voltage magnitude (rms)	10 V
Kp V	PI proportional constant	0.1
Ki V	Voltage PI integral constant	0.5
Kp RESV	Voltage RES proportional constant	1
C V	Voltage RES constant	100
Kp C	Current PI proportional constant	8.4
Ki C	Current PI integral constant	60
Kp RESC	Current RES proportional constant	1
C C	Current RES constant	300

Table 5.2: Simulation and experimental parameters



Figure 5.20: Magnitude and phase of the frequency response function of  $i_{gh}/u_{gh}$  for the LC and LCL filters.

#### 5.5.3.1 Connection to a distorted utility grid using an LC filter

Fig. 5.21 shows the simulation results when the positive sequence component of the fundamental voltage is used for synchronization for the case of an LC filter. Fig. 5.21(a) shows breaker state (Fig. 5.19), it is observed in the figure that it closes t=1s. The dq components of the differential voltage between both sides of the breaker terminals (voltage error) are shown in Fig. 5.21(b), while the dq components of the current circulating through the inverter ( $i_{dq\,i}$  in Fig. 5.19) are shown in Fig. 5.21(c). Fig. 5.21(d) show the current that circulates between the filter output and the grid, Fig. 5.21(e) shows the detail of this current at the instant the breaker closes.

It is observed from Fig. 5.21(d) that the differential voltage shown in Fig. 5.21(b) produces a transient grid current, of peak value of  $\approx 14$  A, which is several times bigger than the steady state current, its dynamics being given by (5.10)-(5.12). The dumped resonance frequency (see Fig. 5.21(e)) is  $\approx 12.5$  kHz, which is in accordance with (5.8). A current harmonic at 300 Hz ( $-5^{th}$  harmonic) exists in steady state (see Fig. 5.21(d)), its magnitude being given by (5.11).

Fig. 5.22 shows the same simulation results as in Fig. 5.21 for the pro-



(e) zoom of  $i_{dq g}$  at the instant that t breaker closes

Figure 5.21: Simulation results. DPG with LC filter synchronization using the positive sequence component of the fundamental voltage.



Figure 5.22: Simulation results. DPG with LC filter synchronization using the proposed soft connection technique.

posed method. It is observed from Fig. 5.22(b) that the differential voltage at the breaker terminals is zero, as both fundamental and harmonic components are considered during the synchronization process. It is observed that with the proposed method, the grid overcurrent in Fig. 5.21(d) ( $i_{dq g}$  in Fig. 5.19) is almost completely cancelled (see Fig. 5.22(d)).

#### 5.5.3.2 Connection to a distorted utility grid using an LCL filter

Fig. 5.23 shows the same simulation test as Fig. 5.21 but using an LCL filter. It is observed that the overcurrent at the instant that the breaker closes (see Fig. 5.23(e)) is smaller than for the LC case, since it is limited by the LCL filter grid-side inductance.

The resonance frequency of the dumped transient response agrees with the predicted one of  $\approx 2.25$  kHz (see Fig. 5.20 and (5.8)), being lower than for the LC filter case (see Fig. 5.20). The higher the inductance between the filter capacitor and the PCC is, the smaller resonance frequency is. Similarly, the higher the inductance between the filter capacitor and the PCC is, the smaller is the transient time constant (5.7). It can be concluded that smaller connection inductances (transmission line plus filter inductances) results in larger transient overcurrents, but more damped.

Fig. 5.24 shows the same simulation results as Fig. 5.22 but for the case of the LCL filter. The same behavior for the inverter output current and the grid current (see Fig. 5.24(c) and 5.23(d)) as for the LC simulation test is observed.

It is concluded that the proposed method eliminates the transient overcurrent after the connection, for both LC and LCL filters.

### 5.5.4 Experimental results

Fig. 5.25 shows the experimental setup. It consists of two VSCs (Master and Slave in Fig. 5.25). The master inverter is used to emulate the programmable AC source (see Fig. 5.19). It is a 50 kW inverter that feeds a local resistive load (53  $\Omega$ ), it uses the same LC filter as in simulation (Table 5.2). The slave inverter configuration is the same as in simulation (see Table 5.2), and feeds a local resistive load (see Table 5.2). The same tests used in simulation were repeated for the experimental verification.

#### 5.5.4.1 Connection to a distorted utility grid using an LC filter

Fig. 5.26 shows the experimental results when the synchronization is realized using the positive sequence component of the fundamental voltage, for the case of an LC filter.

For t<1s the slave inverter is synchronized to the fundamental component of the PCC voltage. The differential voltage at the breaker terminals is equal therefore to the PCC harmonic voltage components (see Fig. 5.26(b)), while the inverter current (see Fig. 5.26(c)) contains only the fundamental component.

At t=1s, the breaker is closed (Fig. 5.26(a)). A transient increase of the grid current is observed (Fig. 5.26(d)). In addition, high-order harmonics appear at the inverter current (Fig. 5.26(c),  $i_{dq\,i}$  in Fig. 5.19) at the instant the breaker closes, which are compensated by the current regulator. The transient current is seen to have a resonance frequency of  $\approx 14$  kHz, with a peak current of  $\approx 16$  A. It is noted that the current spikes observed in the dq components of the grid current ( $i_{dq\,g}$  in Fig. 5.19) are caused by three-phase breaker rebounds (see Fig. 5.26(d)). The differences between the



Figure 5.23: Simulation results. DPG with LCL filter synchronization using the positive sequence component of the fundamental voltage.



Figure 5.24: Simulation results. DPG with LCL filter synchronization using the proposed soft connection technique.



Figure 5.25: Experimental setup.



breaker closes

Figure 5.26: Experimental results. DPG with LC filter synchronization using the positive sequence component of the fundamental voltage.



Figure 5.27: Experimental results. DPG with LC filter synchronization using the proposed soft connection technique.

simulation and the experimental results would be due to differences in the line inductance (the cable mutual inductances have not been included in the simulations), which affect to the transient time constant (5.7), the resonance frequency (5.8) and peak current.

Fig. 5.27 shows the response of the proposed method. The slave VSC uses both the fundamental and the harmonic components of the voltage to feed the synchronization control loop, ideally providing zero differential voltage at the breaker terminals when it closes, (Fig. 5.27(b)). As for the simulation results, no overcurrent is observed when the breaker closes (t=1s, Fig. 5.27(d)). The injected current harmonics later reduce following the pattern shown in Fig. 5.18 (Fig. 5.27(c)), the grid current harmonics therefore increasing (see Fig. 5.27(c) and 5.26(d)). It is noted that once the high-order current harmonics are removed (t>1.35s), the inverter only injects the fundamental component of the current.

#### 5.5.4.2 Connection to a distorted utility grid using an LCL filter

Fig. 5.28 shows the experimental results when the synchronization is realized using the positive sequence component of the fundamental voltage, for the case of an LCL filter. As for the LC filter case, the high-order harmonics in the inverter current that appears at the instant the breaker closes, are compensated by the current regulator (see Fig. 5.28(c)). As for the simulation results (Fig. 5.23(c)), the peak current is smaller than for the case of the LC filter. The resonance frequency (Fig. 5.28(d)) is also smaller as for the LC filter case (2 kHz).

Good agreement among the simulation (see Fig. 5.23) and the experimental results (see Fig. 5.28) is observed, differences being due to the line inductances, which have not been considered for the simulation analysis.

Finally, Fig. 5.29 shows the experimental results using the proposed method for the case of an LCL filter. It is observed from Fig. 5.29(b) that the differential voltage at the breaker terminals at the instant it closes (t<1) is negligible (it mainly consist of noise). It is observed in Fig. 5.29(c) that to match the grid voltage (fundamental+harmonic components), the inverter current contains both fundamental and harmonic components. No overcurrent is observed at the instant the breaker closes (Fig. 5.29(d), t=1), the inverter progressively decreasing later the amount of current harmonics being injected according to the pattern shown in Fig. 5.18.

It is concluded that the proposed method provides a smooth connection as well as smooth transition to steady state, even for the case of highly distorted voltages at the PCC.



(e) zoom of  $i_{dq \ g}$  at the instant that the breaker closes

Figure 5.28: Experimental results. DPG with LCL filter synchronization using the positive sequence component of the fundamental voltage.



Figure 5.29: Experimental results. DPG with LCL filter synchronization using the proposed soft connection technique.

### 5.6 Conclusions

This chapter provides a review of power quality algorithms for islanded and grid connected DPG units. The use of passive filters, active power filters and the virtual impedance methodology for power quality enhance has been introduced.

A method for unbalance and/or harmonic current sharing between parallelconnected DPG units based on the use of the virtual admittance concept has been presented. This concept shares some common characteristics with virtual impedance concept based methods, showing the advantage of being applicable to any DPG unit in any control mode: VSI-VCM, VSI-CCM or CSI. A centralized harmonic compensation strategy has been presented to test the feasibility of the proposed virtual admittance concept. The design of the virtual admittance control loop includes a *non-phase-disturbing* control loop and an LCL decoupling technique, what guarantees that all the inverters synchronously inject the required harmonic current. In addition, as demonstrated, the proposed method also shows a good applicability for transmission losses reduction, forcing the inverters located far away to the PCC to inject less current than the inverters located near the PCC.

This chapter also presents a method for the synchronization and smooth connection of DPG units to highly polluted grids, where traditional methods fail due to the overcurrents that are induced at the instant of the physical connection between the main grid and the microgrid/DPG unit due to a voltage mismatch between the breaker terminals. The proposed method uses both the positive sequence component of the fundamental voltage as well as the grid voltage harmonics for the synchronization, avoiding transient overcurrents at the instant of connection of the DPG unit, which might cause unwanted protection tripping, bad aging of the passive elements or power electronics damage.

# Chapter 6

# **Conclusions and future work**

## 6.1 Conclusions (Spanish)

La presente tesis analiza la sincronización, detección de islanding y la mejora de calidad de red en microrredes.

En el capítulo 2 se han analizado las estrategias básicas de control para convertidores de potencia, incluyendo control de corriente, tensión, potencia e inyección de armónicos. Del mismo modo, se han incluído las definiciones de los diferentes sitemas de referencia y controladores utilizados a lo largo el presente documento.

El capítulo 3 analiza la sincronización de convertidores de potencia monofásicos y trifásicos.

En este capítulo se han presentando tres métodos de sincronización, todos ellos adaptativos en frecuencia, uno para sistemas monofásicos y dos para sistemas trifásicos. Las características principales de los mismos son las siguientes:

- Sincronización en sistemas monofásicos. Se ha propuesto un método basado en un generador en cuadratura (QSG) para poder aplicar técnicas de sincronización trifásicos a sistemas monofásicos. El método incluye una etapa de prefiltrado basada en filtros de rechazo de banda, que elimina los armónicos presentes en la red principal. Además, el retraso de fase introducido por dichos filtros es eliminado en tiempo real por un compensador de retraso de fase.
- Sincronización en sistemas trifásicos. Los dos métodos trifásicos propuestos utilizan etapas de pre-filtrado o de filtrado en el bucle para

eliminar las componentes armónicas de la tensión de red. Ambos algoritmos proveen una respuesta transitoria rápida, una buena capacidad de rechazo de armónicos y una estimación de fase independiente de la magnitud de la tensión de red.

El capítulo 4 recoge el uso de algoritmos para la detección de islanding. Se han propuesto y analizado estrategias de detección de islanding basadas en la estimación de la impedancia de alta frecuencia a la salida del convertidor. Para ello, se ha inyectado una señal de alta frecuencia, o se han aprovechado las componentes armónicas generadas por la conmutación del convertidores de potencia. Todos los métodos propuestos tienen la capacidad de ser implementados en sistemas multi-convertidor, ya que se han analizado y propuesto estrategias para prevenir la interferencia entre convertidores conectados en paralelo.

Algoritmos para la mejora de la calidad de red han sido discutidos en el capítulo 5. Se han analizado y propuesto dos métodos para mejora de la calidad de red: un dedicado a la reducción de tasa de distorsión armónica (THD) y otro dedicado la conexión de convertidores de potencia a redes distorsionadas. Las características principales de los métodos que se han propuesto son las siguientes:

- Método para la reducción del THD. Se ha propuesto el uso de la admitancia virtual como mecanismo para equilibrar la potencia requerida para la compensación de armónicos entre un conjunto de convertidores conectados en paralelo. La principal ventaja del método propuesto es que puede ser aplicado a cualquier tipo de topologías de convertidor y esquema de control.
- Método de sincronización para la conexión suave de convertidores de potencia a redes altamente distorsionadas. El método propuesto utiliza tanto la componente fundamental como las componentes armónicas para realizar la sincronización, lo que contribuye a la reducción de la sobrecorriente inducida en el momento de la conexión debido a la diferencia de tensiones entre los terminales de contactor. Una vez que el convertidor de potencia se ha conectado a la red principal, las componentes armónicas que se estaban inyectando para la sincronización son eliminadas eliminan gradualmente.

## 6.2 Conclusions

This thesis analyzes synchronization, islanding detection and power quality issues of DPG units in microgrids.

A review of the basic strategies for current, voltage, power and harmonic control algorithms have been addressed in Chapter 2, including a basic discussion on the reference frames an designs used along this document.

Chapter 3 analyzes the synchronization of single and three-phase DPG units. Obtain an accurate phase and magnitude estimation of the grid voltage is a key point to guarantee stability and accurately control the generated active/reactive power. An essential feature is the frequency-adaptive capability, in order to deal with grid frequency deviations. This chapter proposes three frequency-adaptive synchronization methods that can work in highly polluted conditions, one for single-phase system and two for three-phase systems.

- A quadrature signal generator (QSG) based on the use of all-pass filters, combined with a three-phase PLL, has been proposed for single-phase synchronization. This method also includes a pre-filter stage based on notch filters to remove harmonics present in the grid voltage. The phase delay introduced by the notch filters is compensated in real time by a phase delay compensator.
- The two proposed three-phase synchronization methods use pre-filter and filter in the loop stages respectively, to remove the disturbances produced by the grid harmonic and unbalances. These algorithms provide fast dynamic response, good harmonic rejection capability, also the phase detection being independent of the input magnitude.

Chapter 4 is devoted to islanding detection. Several islanding detection techniques are proposed and discussed in this Chapter 4. All of them are based on the microgrid/grid high frequency impedance estimation. This is doe either injecting a high frequency signal for this purpose, or making use of the high frequency components produced during the normal operation of the electronic power converters. All the methods have the capability to operate in an multi-inverter scenario, i.e. provide mechanisms to prevent interference among inverters.

Power quality issues are discussed in Chapter 5, including power quality improvement and (THD reduction) and smooth connection of DPG units to distorted grids.

- A centralized harmonic compensation technique based on the use of the virtual admittance concept has been proposed to remove the harmonics induced by non-linear loads in islanded microgrids. Contrary to the virtual impedance loop, the virtual admittance technique can be implemented in VSIs-VCM, VSIs-CCM and CSIs.
- The proposed synchronization method for smooth connection of DPG units to distorted grids is based on the combined use of the positive sequence component as well as unbalanced and harmonic components of the grid voltage, with the goal of reducing the voltage mismatch at the instant of closure of the breaker. Once the connection process is finished, the harmonic components are gradually removed from the reference used for the synchronization.

## 6.3 Future work

In alignment with the synchronization, islanding detection and power quality improvement methods discussed in this paper, the are several lines which are considered suitable for future work:

- The phase detector used in all *PLLs* is non linear (3.12), a linear approximation being commonly used 3.13. Novel linear phase detectors should be investigated to avoid errors due to the linear phase assumption.
- Improve the active islanding detection techniques using harmonics due to the non-ideal behavior of the power converter, as they have no adverse impact on the power quality.
- Deepen the development of islanding detection techniques based on communications, specially those that implements power line techniques.
- Investigate novel decentralized algorithms for harmonic compensation and power quality improvement. Most of the methods found in the literature rely on a master devices which set the harmonic commands to the slave agents. By using a collaborative algorithm, disadvantages associated to the centralized topologies like failure of the master devices, communication delays, etc., can be overcome.
- Development of algorithms for smooth disconnection of DPG units in distorted grids, and adaptive control strategies in the event of unintentional islanding, specially when the DPG units operate close to their

rated power. The virtual admittance concept can thus be applied to smoothly reduce the power injected by the DPG unit when it is disconnected by force from the utility grid.

• The use of communications for microgrids will be a key aspect in the future for power dispatching, harmonic compensation, magnitude and frequency restoration, etc. The use of industry and standard communication buses can be investigated, taking advantage of the equipment and experience in their use.

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# Appendix A

# Publications

# A.1 Peer-reviewed conference publications

A.1.1 Active Islanding Detection Using High Frequency Signal Injection



Connections of the microgrids to the utility grid are required to meet standards normally regulated either by the country (local) authorities or by standardizing institutions as IEEE and IEC [2-7, 24, 25]. In all the cases the system is  Communication based methods [2].- These methods can be divided in three groups: SCADA based methods, methods that use the power line as a carrier for communications and the methods that monitor the device used to connect/disconnect from the grid. These methods are not very popular due to the need of a communication system between the DG and the utility grid.
 A new active method for islanding detection based on the

A new active method for islanding detection based on the injection of high frequency signal voltage is proposed in this paper. Advantages of the method are almost negligible adverse effects due to the injected high frequency voltage, as well as accurate and fast islanding detection. The paper is

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disturbance will be corrected by the grid, while if it is islanding operation, the disturbance will remain. The variables commonly selected for islanding detection are the islanding detection methods, the physical principles and the analytical formulation of the proposed method being presented in Section III and IV. Simulation results are presented in Section V. Discussion of implementation issues are presented in Section VI, experimental results demonstrating the viability of the proposed method being frequency [2, 15] and voltage [2, 15] at the PCC. While active methods are appealing due to their reduced NDZ, the disturbance introduced in the grid can be a concern, presented in Section VII. especially when a large number of inverters are connected to the same PCC and interferences can occur. To prevent these II. Islanding detection using active methods. adverse effects, the use of a high frequency, small magnitude This section reviews active islanding detection methods periodic signal is proposed. The principles of the method are found in the literature. discussed following a) Impedance Estimation Methods III. Islanding detection using high frequency signal The motivation for these methods are the requirements established by the standards for islanding detection [13, 14, injection. 24, 25]. Active methods can be divided in two groups It has already been shown that the high frequency transient active methods and steady-state active methods. pedance is a reliable metric to detect an islanding situation In transient active methods, an impedance measuring device [9] produces a short disturbing signal (normally a [9-12]. Voltage-source inverters (VSI) present in the microgrid (e.g. in controlled rectifiers used in APF, back-tovoltage), e.g. impulse like, and analyzes the grid response back power converters, ...) can easily inject a low-magnitude, (normally in the current) The advantage of these techniques high-frequency voltage from which the high frequency impedance is measured. While a variety of different forms of is that the grid can be excited over a large frequency range, significantly improving the accuracy and reliability of the high frequency excitation can be used, especially simple and reliable implantations are obtained by injecting either a measurements Steady state active methods inject a harmonic (periodic) rotating or a pulsating voltage vector, both options are component [9-11]. In the method proposed in [10], a high frequency signal (400-600 Hz) is injected at the instant of discussed following. Α. Rotating high frequency signal injection zero crossing of the fundamental excitation voltage at the When a three-phase, linear system, is exited with (1), the point of common coupling (PCC); the impedance being induced high frequency current is given by (3), the high frequency impedance at the excitation frequency being (4), estimated from the measured voltages and currents using the Discrete Fourier Transform [10]. A limitation of this method with its phase angle being (5). is that since the signal is injected at the instant of zero  $v_{dqhf} = V_{hf} e^{j}$ (1)crossing of the grid voltage, islanding condition can only be detected at that point. Also, additional current sensors are  $v_{dqhf} = v_{dhf} + jv_{qhf} = \frac{2}{3} \left( v_a + v_b e^{j2pi/3} + v_c e^{j4pi/3} \right)$ (2)  $i_{dqhf} = \frac{V_{hf}}{Z_{dqhf}} e^{j(\omega_{hf}t - \varphi_Z)}$ needed at the PCC to measure the high frequency current. An extension of the method in [10] was presented in [12], for the (3) case of multiple inverters working in parallel for PV applications. The extended method proposes the coordinated  $Z_{dqhf} = R_{hf} + j\omega_{hf}L_{hf} = \frac{v_{dqhf}}{i_{dqhf}}$ (4) injection of a non-characteristic (i.e. non present during normal operation of the grid) harmonic (75 Hz). Previous to  $\varphi_z = \operatorname{a} \operatorname{tan}\left(\frac{\omega_{hf}L_{hf}}{R_{hf}}\right)$ the injection of this harmonic each PV inverter checks if it is already present in the grid; and for this case will wait a few (5) cycles of the fundamental voltage wave before checking again to prevent interference with other PV inverters [12]. where  $\omega_{i_N}$  is the frequency of the injected signal,  $V_{i_N}$  is the voltage magnitude of the injected high frequency signal,  $i_{dyk}$  is the induced high frequency current,  $Z_{dyk}$  is the high frequency impedance,  $\varphi_Z$  is the phase of the high frequency impedance of the three-phase system, and  $R_{i_N}$  and  $L_{i_N}$  are One limitation of this technique is that two or more inverters could simultaneously start the check-and-inject procedure, interference and consequently incorrect islanding detection could occur. The probability of interference increases with the high frequency resistance and inductance respectively. One important issue that needs to be considered is the the number of PV inverters connected to the grid. addition, the interharmonic signal (75 Hz) could interact with effect of the output filter of the VSI on the estimated high the fundamental current/voltage controls (50 Hz) due to the frequency impedance. It can be observed form a classical small spectral separation. architecture for connecting a microsource to a grid/microgrid, b) Grid Variable Variation Methods Fig. 1, that it is straightforward to estimate the microgrid In these methods, the DG produces a small disturbance in and/or grid impedance when currents and voltages are a grid variable. If the DG is connected to the grid, the

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measured at the output of the filter [9-12]. On the other hand, if the inverter output current is measured, the high frequency impedance estimated from the measurement is the equivalent impedance that results form the combined effect of the microgrid and/or grid impedance and the output filter impedance. If the current is measured at the filter input (see Fig. 1) and an LCL filter is used, the output current of the LCL filter can be estimated from (6), the microgrid and/or the grid impedance being obtained from (7), avoiding therefore the use of additional sensors at the filter output.

$$i_{dq\mu ghf} = \frac{v_{dqhf1} - v_{dq\mu ghf} - j\omega_{hf}L_1 i_{dqhf}}{j\omega_{hf}L_2}$$
(6)

$$Z_{dqughf} = \frac{v_{dqughf}}{i_{dqughf}} \tag{7}$$

where  $v_{dept_1}$  is the commanded high frequency voltage,  $v_{dguty_1}$  the measured high frequency voltage at the filter output,  $L_1$  the inverter side inductance filter and  $L_2$  the microgrid side inductance filter.



Fig. 1 Classical architecture for connecting a microsource to a grid/microgrid. To illustrate the principle of operation of the proposed

To finistate the principle of operation of the proposed method, a simulation of a transition (in *t*=1s) from grid connected mode to island condition of a micro-source (See Fig. 1) is shown in Fig. 2. A high frequency voltage of magnitude 5V and frequency 3314*z* is superposed to the fundamental voltage, Fig. 2a and 2b showing the q- and d-axis components of the voltage and current vectors (the high frequency portion being practically imperceptible due to its reduced magnitude). Fig. 2c and 2e show the q- and d-axis components of the high frequency voltage and current vectors, obtained by digital filtering of the measured variables shown if Fig. 2a and 2b. The differences in the high frequency voltages and currents (and consequently in the high frequency impedance) between island and grid modes are evident, supporting therefore the validity of the proposed method.

B. Pulsating high frequency signal injection Although the paper is focused on a rotating voltage vector

Although the paper is focused on a rotating voltage vector excitation, as already mentioned, another simple type of high frequency excitation is the pulsating voltage vector (8). The high frequency current induced for this case is given by (9) and the high frequency impedance by (10). As for the rotating high frequency signal injection the effect of the output LCL filter can be decoupled using (6) and the microgrid and/or grid impedance being obtained from (7).



(10) Both rotating and pulsating high frequency injection methods respond to the same physical principles and are expected therefore to provide similar overall performance. Only rotating high frequency injection is analyzed in detail in this paper.



d) to the second test of the second test of the measured big the second test of the measured high frequency voltage  $v_{day}$ , measured high frequency current  $i_{a,b}$ , measured high frequency voltage  $v_{aby}$ , d).

## IV. Use of multiple high frequency signals to prevent interference

It has been shown in the previous section that the injection on a high frequency signal voltage allows to detect islanding condition. However, in a general case, a large number of VSI that could potentially inject the high frequency signal exist in a microgrid, a strategy to prevent interference that might occur if more than one inverter injects the high frequency signal, is needed.

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potential solution to this problem is that inverters detecting the secondary high voltage boost the signal at a certain, predetermined magnitude, acting therefore as voltage amplifier.

## VI. High frequency signal selection.

Several issues need to be considered for the selection of the magnitude  $V_{bj}$  and the frequency  $\omega_{bj}$  of the high frequency voltage.

The magnitude of the high frequency voltage  $v_{dol/1}$  is limited in first instance by connection standards [3-7], since the injected high frequency signal increases the THD and might create power quality problems, while the magnitude of  $v_{dol/2}$  is determined by the microgrid structure, to ensure that the resulting signal magnitude (voltage or current) available on each inverter is higher enough to be detected.

- For the frequency selection, several aspects need to be taken into consideration:
- The high frequency signal could interact with the filter resonant frequency, which for the case of LCL filter (See Fig. 1 and 6) is typically in a range between a tenth of the switching frequency and ten times the fundamental frequency [19]. For the experimental results that are presented in the next section, the switching frequency is 10kHz, therefore the resonant frequency of the LCL filter should be in a range from 500Hz to 1kHz; a value of 575Hz was chosen for the LCL filter resonance frequency of the experimental setup. Current regulated VSI could react to the induced high
- Current regulated VSI could react to the induced high frequency current injected either for island detection or communication. A mean to prevent from this to happen is by means of a band-stop filter in the current feedback tuned for to reject the frequency of the injected signals (300Hz for the experimental results shown in this paper, see Fig. 6).

If this filter is not implemented, the current regulator of the VSI will detect, and partially compensate for the high frequency current. The effects of this reaction will depend both on the frequency of the injected signal and the bandwidth of the current regulators, as well as on the grid characteristics. It is not possible therefore to obtain a general model able to predict the impact of a current regulated VSI on the high frequency signal. However, simulations performed using the configuration shown in Fig. 4 showed that the method worked adequately even in the presence of current regulated VSI.

As for the high frequency signal used for communications purposes, the used of a band-stop filter in the current feedback of the inverter injecting it is recommended, (master inverter, See Fig. 6), but it is not require in the other inverters connected to the grid that have to detect the signal.

• The high frequency signals that are injected (both  $v_{dqh/1}$ and  $v_{dqh/2}$ ) can have positive or negative frequencies, as they are complex vectors. In general, the spectral separation of the injected high frequency signal form the fundamental dependence harmonics (e.g.  $-5^{th}$ ,  $7^{th}$ ...) should be made as high as possible to avoid interactions and to make the high frequency signal processing (filtering...) easier. From this point of view, if the signal frequency is close to the  $-5^{th}$  harmonic frequency, the signal should be injected as a positive sequence component (avoid interaction with  $-5^{th}$  harmonic), while if the signal frequency is close to the  $7^{th}$  harmonic, frequency, the signal should be injected as a negative sequence signal (avoid interaction with  $7^{th}$  harmonic). Fig. 7 shows the estimated high frequency impedance magnitude and phase for island and grid connected conditions for positive and negative sequence signals in a frequency range from 300 to 420 Hz. It can be observed that the island/grid-connected situation could be detected using either positive or negative sequence signals for this case.



 $(f(H_Z))$ Fig. 7 Estimated high frequency impedance magnitude (a)) and phase (b)). Positive sequence impedance in island (o) and grid connected condition ( $\triangleright$ ), negative sequence impedance in island ( $\Box$ ) and grid connected conditions (x).  $H_g$ =1.5V.

- Special care should be taken if active power filters (APFs) are present in the microgrid, since the APF control could react to the injected high frequency signal. However, as the proposed method uses the measured output voltage of the LCL filter (see (6)-(7)), the method would be in general applicable even when APF's are present. Typically APF's compensate harmonics that are multiple of the fundamental frequency [20-22], thus to avoid possible interaction between the injected high frequency signal and APF's, a frequency that is not an integer multiple of the fundamental frequency should be used.
- The high frequency signal could interact with the grid resonance frequency that can vary in a large range depending on the grid topology, transmission lines... [23], it is therefore difficult to reach general conclusions in this regard.



Islanding threshold

Grid connected

threshold

14

Grid

connected

10

t(s)

Island

10





## A.1.2 Grid Synchronization of Three-Phase Converters Using Cascaded Complex Vector Filter PLL





ω<sub>bw</sub>-jnω<sub>o</sub>

ATO

(3)

(4)

nal value of

S-CCF (n)

φ

deg)

× × PI





$$\frac{w^*(s)}{\theta(s)} = \frac{s \cdot G_{PI}(s)}{s + G_{PI}(s)}$$

#### III. SIMULATION RESULTS

The proposed synchronization technique has been tested using the simulation scheme shown in Fig 8. Four different scenarios have been considered: 1) change of the grid frequency, 2) change of the grid voltage magnitude, 3) grid unbalance and 4) polluted grid conditions (harmonics). The simulation was performed using Matlab. Tustin was used for the discretization of the continuous transfer functions. For each case, the performance of the proposed method is compared with the results provided by the synchronization methods described in section 1: *DSRF-PLL* (Fig. 1a), *DSOGI-PLL* (Fig. 1b), *MCCF-PLL* (Fig. 1c), *BP-CCF-CPLL* (Fig. 1d), and *CCCF-CPLL* (Fig. 6).

a) Gains selection

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Several gains need to be chosen for each method; a tuning methodology has been established, with the goal optimizing the tuning for each method, thus making the comparative analysis fair. The mean squared error (*MSE*) (6), between the real phase ( $\theta$ ) and the estimated phase ( $\theta$ ), was chosen as a reliable figure of merit, its minimization using numerical

optimization has been used for the gain selection for each method. The *MSE* will be function of the proportional and integral gains of the controller,  $k_p$  and  $k_i$ , color maps were found to be adequate to show this dependence. Similarly to (6), the *MSE* can also be calculated using the error in the estimation of the fundamental voltage magnitude (7) and of the fundamental voltage frequency (8), where subscripts *dist* refers to type the disturbance applied, *f* standing for a mubalance in the grid voltage and *h* for the grid voltage containing harmonics.

$$MSE_{phase,dist}(t) = \frac{1}{T} \int \left(\theta - \theta^*\right)^2(t) dt$$
(6)

$$MSE_{amp,dist}(t) = \frac{1}{T} \int \left( V - V^* \right)^2(t) dt$$
(7)

$$MSE_{freq,dist}(t) = \frac{1}{T} \int (\omega - \omega^*)^2(t) dt$$
(8)

Fig. 9 shows the CCCF-CPLL error color maps obtained for the different types of distortions and transient conditions of the line voltage already described in this section. It is observed from the figure that the cases in b), c) and d) have similar color maps, meaning that the same set of gains provides near optimal results (i.e. minimum MSE) for those type of disturbances. It is noted however that the regions with lowest error in Fig. 9a occurs at different gains values. Choosing a set of  $k_p$  and  $k_p$  gains able to provide adequate response under any kind of distortion or varying condition in the line voltage can be done by combining the MSEs in Fig. 9a to 9d into a global  $MSE_{phare,global}$  (9), the purpose of the weights  $w_x$  being to select the type of disturbance that should be better rejected.

 $MSE_{phase,global} = w_f MSE_{phase,f} + w_m MSE_{phase,m} + w_u MSE_{phase,u} + w_h MSE_{phase,h}$ (9)

While the same value could be used for all the four weights in (6), they can also be chosen to be different. For example, sudden step-like changes of the frequency are less likely to occur than other kind of distortions, due to the large inertia of the generators [10, 11]. Then, a smaller value for  $w_i$ , compared to the rest of weights in (6), could be used. Fig. 9e shows the  $MSE_{phase,global}$  when  $w_h = w_a = w_m = 0.33$  and  $w_j = 0.01$ . According to Fig. 9e, values of the gains  $k_p=0.3$  and  $k_r = 38$  would be adeuate choices, as  $MSE_{phase,global}$  is small and has low sensitivity to changes of  $k_p$  and  $k_r$ . It is also observed from Fig. 9e that other regions with low values of  $MSE_{phase,global}$  exist, but have larger sensitivity to variations of  $k_p$  and  $k_r$ .

Fig.10 shows the  $MSE_{phase,global}$  color maps obtained using the tuning methodology described for all synchronization methods considered. The same weights as for the CCCF-CPLL were used. The  $MSE_{phase,global}$  color maps are shown as a function of the PLL PI regulator gains,  $k_p$  and  $k_i$ respectively, for the scenarios described in Table I. It is observed from Fig. 10a and c that for the case of the DSOGI-PLL and BP-CCF-CPLL, there is a region of low values of  $MSE_{phase,global}$ , and with a relatively smooth transition MSE to

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(5)

the regions with larger values. This means that these methods have a good disturbance rejection capability, and the MSE selection of the gains is not critical, i.e. slight changes in the gains do not have a critical impact on the performance of the method. Opposite to this, significantly larger variations of the MSE<sub>phaseglobal</sub> are observed in Fig. 10b for the case of the DSRF-PLL, meaning that this method is more sensitive to the tuning process. The results of optimization stage for each method are summarized in Table II.

method are summarized in Table II. While DSRF-PLL and DSOGI-PLL methods do not need to configure any extra block (see Fig. 1a and 1b), BP-CCF-CPLL, MCCF-PLL and CCCF-CPLL methods use a firstorder CCF (see Fig. 5) for each component being removed/isolated (Figs 1d, 1c and 6). BP-CCF-CPLL method uses three band-pass complex-coefficient-filters: one for fundamental component, one for -1<sup>th</sup> harmonic (to isolate the negative sequence component due to unbalance) and another to isolate the 5<sup>th</sup> fundamental dependence harmonic. For the MCCF-PLL method, three band-pass complex-coefficientfilters tuned at the frequencies to be rejected need to be set while for the CCCF-CPLL, one band-pass complexcoefficient-filter is used for the fundamental component and two band-stop complex-coefficient-filters to reject -1<sup>st</sup> and -5<sup>th</sup> harmonics. The bandwidth ω<sub>bw</sub> for all methods is defined in Table II.



Fig. 10 – Color maps showing the  $MSE_{phase,global}$  as a function of the controller gains for the different methods. Same logarithmic scale as in Fig. 9 was used.

Table I - Simulation Scenario						
Sim. Step	Grid paramete	rs Harmonic	s Frequency jump	Unbalance	Amplitude Jump	
10 <sup>-4</sup> s	380V, 501	Hz 10% pu (-5 <sup>th</sup> )	50Hz to 48Hz	0.7 pu in phase C	50%	
Table II - Optimization stage results						
DSOGI-PLL		$k_p =$	$k_p = 3.72$		$k_i = 28.72$	
DSRF-PLL		$k_p = 1.06$		$k_i = 0.71$		
MCCF-PLL		$k_p = 2.21$	$k_i = 44.13$	W <sub>bw mccf</sub> = 300 rad/s		
CCCF-CPLL		k <sub>p</sub> =0.3	k <sub>i</sub> =38.48			
BP-CCF-PLL k		$k_p = 1.98$	$k_i = 104.2$	w <sub>bw bp-ccf</sub> = 300 rad/s		



c) to the second sec



Fig. 12 –Simulation Results: amplitude (7), frequency (8) and phase (6) MSE for all the methods and for different types of disturbances: a) step-like change of line voltage frequency, b) step-like change of the line voltage magnitude, c) phase voltage unbalance and d) line voltage with harmonics

#### b) Simulation results

Fig. 11 shows the estimated frequencies (Hz) and amplitudes (p.u) for different types of disturbances in the line voltage, including changes in the fundamental voltage frequency and magnitude, unbalances and harmonics; the results for each event disturbance are discussed following.

• Fundamental voltage frequency step-like change: Fig. 11a shows the simulation results when the frequency changes from 50 to 48 Hz occurs (t=1s). It is observed that CCCF-CPLL shows the slowest response, while MCCF-PLL, DSOGI-PLL, and BP-CCF-CPLL and DSRF-PLL show similar, faster response, being the DSOGI-PLL the method with shortest settling time. Fig. 12 shows the mean squared error (MSE) for the estimated fundamental voltage phase.

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diesel generator "G" rated 100kVa, 380V and 152A, was used (6), magnitude (7) and frequency (8). The bars for each s the primary power source for the master and slave inverters. case were normalized by dividing by the worst case, the LCL filters, with a resonance frequency of 575Hz are used to connect the inverters to the grid. The master inverter was maximum value for each case being therefore one. Fig. 12a summarizes the MSE for the case of a step-like change in the programmed to produce the same type of disturbances discussed in the previous sections. A *TMS320F28335 DSP* has been used for the implementation of the algorithms. A frequency, confirming the results observed in Fig. 11a. Fundamental voltage amplitude step-like change A 50% amplitude jump has been introduced in Fig. 11b in t=1s. It sampling frequency of 10 kHz was used, which is equal to the switching frequency. Tustin transformation was used for the is observed from Fig. 11b and 12b that the BP-CCF-CPLL shows an overall better behavior, followed by the CCCFdiscretization of the continuous transfer functions. The gains for the different methods have been tuned to the values CPLL. On the other hand, an amplitude change produces oscillations in the estimated frequency DSRF-PLL showing obtained through the optimization methods described in the previous section (see Table II). the worst behavior in this regard. Regarding the error in the estimation of the frequency and phase terms, the behavior of DSRF-PLL, DSOGI-PLL and MCCF-PLL are the worst, showing a fast but oscillating response. It is finally noted DSP DSP abg that either for amplitude, frequency or phase MSE, the best methods to deal with changes in the amplitude are the BP-∐र् Ţ Filter CCF-CPLL and the CCCF-CPLL. Conversely, DSRF-PLL shows the worst frequency and phase MSE, while MCCF-. imental Setup PLL exhibits the biggest amplitude MSE. Phase voltage unbalance: Fig 11c shows the simulation Frequency (Hz Magnitude (pu results of a 30% unbalance in phase C. It can be observed that the DSOGI-PLL shows the most appealing behavior, followed by the CCCF-CPLL, being the BP-CCF-CPLL the method with the lowest unbalance rejection capability. It is also noted that although the DSOGI-PLL shows good unbalance rejection, it has poor harmonic rejection capability (Fig. 11d). This is explained because the DSOGI-PLL has two SOGI-QSG (see Fig. 1a) that extract the positive sequence component, removing the negative sequence, however it does not have any extra block to remove high order fundamental dependence harmonics The different MSEs during the unbalance for each method are summarized in Fig 12c. The CCCF-CPLL and the DSOGI-PLL are the methods with lowest MSE in all cases (amplitude, frequency and phase), while the BP-CCF-CPLL is the method with the poorest performance, as it does not reject the negative sequence component as it only uses a band-pass-filter for the positive sequence. Harmonic voltage injection. The impact of the harmonics on the estimated fundamental frequency and the Fig. 14— Experimental Results. Frequency (left) and magnitude (right) of the fundamental voltage estimated by different methods for the case of a) step-like change of line voltage frequency, b) step-like change of the line voltage magnitude, c) phase voltage unbalance and d) frequency line voltage with harmonics. fundamental voltage component are shown in Fig. 11d. It is observed that MCCF-PLL and CCCF-CPLL almost totally reject all the harmonics. On the other hand BP-CCF-CPLL, DSOGI-PLL and DSRF-PLL show lower harmonic rejection capability; significant oscillations in the Fig. 14 shows the frequency and amplitude experimentally estimated frequency being observed for both methods. Fig. measured for the same disturbances and transient conditions 12d summarizes the simulation results when harmonics in discussed in section III, Fig. 15 shows the different MSEs, the grid voltage are present. these results are discussed following. Fundamental voltage frequency step-like change: Fig. 14a shows the results when a step-like frequency variation from IV. EXPERIMENTAL RESULTS Experimental verification of the behavior of the 50 to 48Hz (t=0.5) occurs. It is observed that all methods synchronization methods discussed in this paper is presented in this section. The experimental setup is shown in Fig. 13. A show a similar response, except the proposed method that is slower updating the grid frequency, so it causes an 201

BP-CCF CPLL

MEDIUN

YES

YES

LOW

7.42

XCELLE

LOW

MEDIUM

additional phase shift. The experimental results mostly agree with the simulation results. It is noted that this is not considered a critical issues as such kind of transient is not expected to occur in practice. • Fundamental voltage amplitude step-like change Fig. 14b shows the response of the different methods when a step-like variation of 50% is applied to the fundamental voltage magnitude. The dynamic response of all methods is very similar, which is also confirmed by Fig. 15b. Some disagreement is observed among the experimental results in Fig. 15 and the simulation results in Fig. 12. This discrepancy would be explained by the fact that, contrary to the simulation (see Fig. 8 and 11b), the output voltage Fig. 15 -Experimental Results: amplitude (7), frequency (8) and phase (6) MSE for all the methods and for different types of disturbances: a) step-like change of line voltage frequency, b) step-like change of the line voltage magnitude, c) phase voltage unbalance and d) line voltage with harmonics amplitude of the master inverter cannot be changed instantaneously (see Fig. 14b), · Phase voltage unbalance: An unbalance of 30% in phase C was and Fig. 14c shows the frequency and amplitude Table III. obtained by each synchronization method. As for the CCF-CPLL DSOGI-PLL DSRF-PLL MCCF-PLL simulation results, the BP-CCF-CPLL method exhibits a slightly worse unbalance rejection capability, with a negative sequence component showing up both in mplicity lexibility XCELLEN CELLE LOW req. adapt YES YES YES YES amplitude and frequency. The other methods perform very pplication APF NO NO NO YES similar. · Harmonic voltage injection: Fig. 14d shows the output MEDIUM LOW HIGH LOW mplexity amplitude and frequency of all synchronization methods when a -5th harmonic of magnitude 0.1p.u. is present in 7.22 xecution ime (us) 4.98 8.32 6.94 the grid voltage. The *DSRF-PLL* exhibits the poorest performance, with the rest of synchronization methods showing a similar behavior. Still, according to Fig. 15d, the *CCCF-CPLL* shows the lowest overall error MEDIUM MEDIUM MEDIUM XCELLE nbalanc spons XCELLEN XCELLE GOOD XCELLE XCELLEN MEDIUM LOW EXCELLE (amplitude, frequency and phase), which is in accordance with the simulation results presented in section III. The differences in terms of harmonic rejection are related, as in flexibility, as only one BS-CCF is needed for each component the case of the unbalance experiment, to the low-pass be rejected. Methods like DSOGI-PLL and DSRF-PLL do not provide a mechanism to decouple harmonics. All methods are frequency-adaptive so they can move the behavior of the synchronization control strategy of the slave inverter, whose current PI regulators are set to  $k_p$  = central frequency of their filters in case of changes in the fundamental frequency. The frequency estimation of the 8.4 and  $k_i = 60$ . proposed method has slower dynamics compared to the others methods, although it is noted that the rate of frequency variation of a grid is small [10, 11] (e.g. the UNE-EN 5016 limits the maximum frequency shifts: for interconnected Table III summarizes the results obtained for each method according to several criteria: · Simplicity: conceptual complexity of the methods. Flexibility: possibility of adapting the system, e.g. rejected/isolated harmonics, depending on the grid systems the mean frequency value, calculated each 10s, should characteristics. not exceed  $\pm 1\%$  during the 99.5% of a week, though exceptionally deviations between  $\pm 4\%$  and -6% are · Application on APF: possibility to measure high order permitted). harmonics to be further compensated by an APF. • Tune complexity: properties of optimization stage process If the synchronization method is to be used in an APF, the (e.g. smoothness of the MSE color map, ...).Dynamic response: refers to the settling time when MCCF-PLL and the BP-CCF-CPLL would be in principle better options, as they provide the amplitude and phase of the frequency changes occur. Conceptually, the proposed method is relatively simple, as harmonics to be compensated. Regarding their tuning, the CCCF-CPLL shows a smooth it consists of a BP-CCF, several BS-CCFs (depending on the harmonics that want to be rejected) and a CPLL series and wide tuning area so it is easy to tune. Contrary to this, DSRF-PLL method is rather sensitive to variations of the connected, not being necessary decoupling networks (e.g. DSOGI-PLL or MCCF-PLL), which would increase the complexity of the method. CCCF-CPLL method also has parameters As for the computational requirements, DSOGI-PLL has the lower burden, though it is at the price of lower good performance

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## A.1.3 Grid Synchronization of Three-Phase Converters Using Cascaded Complex Vector Filter PLL







that no high frequency current exists at the inverter output (see Fig. 3) and totally cancels it.  $G_{HFCR} = k_p (1 + K_i/s) \tag{4}$ 

This mode of operation for the slave inverter is called infinite impedance mode. It is noted that both the output current of the inverter and the output voltage of the LCL filter are normally available in inverter-based DG, no additional sensors are therefore needed to implement this method [19]. It is also important to notice that since no high frequency current exists at the slave inverters output, it will be the high frequency voltage command (i.e. the output of the high frequency current regulator in Fig. 3) the variable reflecting the grid connected/islanding condition.





This strategy has several appealing properties. The high frequency signal voltage injected by the master inverter is not corrupted due to the reaction of other inverters in the grid, as no high frequency current flows through them. This also prevents interference between inverters since only the master inverter injects the high frequency signal. It is finally noted that though the proposed strategy is described for current regulated VSI inverters using an LCL filter, it can also be

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implemented on inverters using other filter designs like inductive filters.

To evaluate the proposed method, a scenario with three parallel-connected converters –a master and two slave inverters–, has been built as an example (Fig. 4). The simulation parameters are summarized in Table I. Fig. 5 shows the simulation results. The master inverter continuously injects the high frequency voltage ( $v_{dept}$ , see table 1), the estimated magnitude and phase of the high frequency impedance being shown in Fig. 5a and 5b respectively. Transition from island to grid-connected and form grid-connected to island occur at t=3.5 s and  $\pm 5.5$  s respectively. It is observed from Fig. 5a and 5b that the changes in the magnitude and phase of the high frequency impedance allow reliable island/grid-connected detection [19].

Fig. 5c shows the magnitude of the high frequency current regulator output voltage  $(1v_{depl}^{*})$ , see Fig. 3) for the two slave inverters (inverters i and 2 in Fig. 4). It can be observed that the high frequency voltage dramatically decreases when the microgrid becomes connected to the main grid. This is due to the variation of the high frequency impedance between island and grid connected condition. While in island condition the overall microgrid high frequency impedance corresponds to the locals loads, and can be relatively large, in grid connected condition the overall microgrid high frequency impedance corresponds to the locals loads, and can be relatively large, in grid connected condition the overall high frequency impedance is dominated by the grid impedance, which is normally significantly smaller [13]. This high frequency urrent regulator output voltage, which is used by the slave inverters to detect the islanding/grid-connected condition. This is done without the need of a secondary high frequency signal for communication purposes [19] and without interfering with the master inverter operation.

It is noted that a threshold for the high frequency current regulator output voltage magnitude needs to be set to detect the transition between islanding and grid-connected operation. This threshold might depend on the microgrid/grid architectures, microgrid/grid high frequency impedances or grid pollution. As for the islanding detection THD based methods [13, 19, 20] or the voltage harmonic monitoring based methods [21], the selection of the threshold is not always easy and might require a previous knowledge of the microgrid/grid characteristic.

#### IV. Dynamic master role assignment

One concern of methods in which a master inverter is responsible on injecting the high frequency voltage, is the risk of a master inverter failure [19]. This will leave the grid/microgrid without the high frequency signal, the slave inverters therefore loosing their islanding detection capability. Further more, even in the event that the master inverter does not fail, changes in the grid/microgrid topology, e.g. switching between islanding and grid connected



slave inverters detect that no high frequency voltage is present in the grid. This can be due either to the failure of the master inverter, or to a significant decrease of the grid impedance (e.g. due to a change from island to grid connected operation). b) The slave inverters detect a sudden increase of the high frequency voltage in the microgrid. This can be due to a change from grid connected to islanding. An example of failure of the master inverter is shown in Fig. 6 (the grid topology is shown in Fig. 4). Fig. 6a shows the high frequency voltage magnitude, measured at the LCL filter output, for the master power converter (blue) and two slave power converters, master failure occurring at t=0.5s

2. Reassignment of the master inverter role. Once any of the events described above occurs, all the former slave inverters start injecting the high frequency voltage immediately. However, the slave inverters do not inject a constant magnitude high frequency voltage, it increases with time instead (5)-(6), where  $V_{CR0}$  is the magnitude of the high frequency voltage for each slave inverter right before the master inverter failure, and  $V_{CR_{max}}$  is the limit established for the high frequency voltage.

$$\begin{aligned} v_{CR} &= \left( V_{CR0} + k_2 t e^{k_1 V_{CR0}} \right) e^{j \Theta_{bb'} t} & \text{if } |v_{CR}| < V_{CR\_max} \quad (5) \\ v_{CR} &= V_{CR\_max} e^{j \Theta_{bb'} t} & \text{if } |v_{CR}| \ge V_{CR\_max} \quad (6) \end{aligned}$$

It is observed from (5) that the high frequency voltage magnitude increases linearly with time, but both the starting value as well as the rate of increase being function of  $V_{CR0}$ . According to (5), the inverter with a larger initial voltage  $V_{CR0}$  starts with a larger initial value and increases the magnitude faster (see Fig. 6b), therefore reaching  $V_{CR\_max}$  first. The philosophy behind this strategy is that, in general, inverters closer to the PCC before the failure are considered better candidates to assume the master role. The strategy established by (5)-(6) will produce that the inverters placed closer to the PCC will win the race to become master.

Fig. 7 shows the time needed by an inverter to reach  $V_{CR\_\max}$  , as a function of  $V_{CR0}$  and the gain  $k_1$  . It is observed from the figure that small differences in  $V_{CR0}$ produce large variations in the time needed to reach  $V_{CR}$  max, therefore reducing the risk of more than one

 $V_{CR_{max}}$ , interfore reaching the first of more than one inverter becoming master at the same time. Once one inverter reaches  $V_{CR_{max}}$ , i.e. the rated high frequency voltage magnitude, automatically changes its role to master (Fig. 2) and continues injecting the high frequency signal hereafter (see Fig. 6b).

It is noted that other reassignment strategies different from (5)-(6) could be used, the key issue for the design of new strategies being their ability to discriminate the most suitable inverters to assume the master role during the master reassignment process. It is also interesting to note that although in the strategy used in this work the high frequency signals are injected during the reassignment

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process (see Fig. 6), it is feasible for the inverters to produce the high frequency signal internally, i.e. without physically injecting them intro the grid, in such a way that only when a inverter reaches  $V_{CR_{max}}$  it becomes the master inverter, and injection of the actual high frequency voltage into the grid occurs.

3. Notification of the role change to the rest of microgrid inverters. Once one inverter assumes the master role, it injects a secondary high frequency signal  $(v_{dqh/2})$  during a short period (80ms, see Fig. 6c). This signal informs to the rest of inverters that the master role has already been reassigned. The rest of inverters automatically will stop injecting the high frequency signal and change their mode of operation to slave mode (Fig. 3). Fig. 6c shows the commanded voltage magnitude of the secondary high frequency signal by inverter 1 and the measured secondary high frequency voltage magnitude by inverter 2, which is used to stop its high frequency signal injection (see Fig. 6b) and to switch to the slave mode.

## V. High frequency signal selection

Both the magnitude (  $V_{\scriptscriptstyle M}$  ) and the frequency (  $\omega_{\scriptscriptstyle M}$  ) of the high frequency voltage injected by the master inverter need to be set. Generally speaking, low-magnitude, high frequency signals will decreases the adverse impact on the THD, what eds to be considered to meet the connection standards [1-111.

A relatively large frequency range could be used, the limits coming from the interaction with the output LCL filter resonant frequency (see Fig. 2 and 3), the grid resonant frequency and the need of having spectral separation with fundamental frequency dependent harmonics (e.g.  $-5^{th}$ ,  $7^{th}$ ...) that often exist [19]. It is noted in this regard that the injected high frequency signal can have a positive or negative frequency, as it is complex vector. The high frequency signal can be chosen to be synchronous (i.e. an integer multiple like  $\pm 6^{\text{th}}$ , +5 th, -7 th ...) or asynchronous with the fundamental  $\pm 6^{th}, \pm 5^{th}, -7^{th}$  ...) or asynchronous with the fundamental frequency. Being in synchronism might provide some advantages, e.g. during the reassignment of the master role, all the inverters could inject the high frequency signal in phase with each other, the process being then more repetitive However, synchronizing the high frequency signal with the fundamental voltage requires the estimation of the fundamental voltage phase angle, which might be problematic in the case of distorted grids. An asynchronous high frequency signal with  $\omega_{hf} = -333$  Hz was used for the simulation and experimental results shown in this paper (see Table I).

The magnitude of the injected high frequency signal in the simulation results shown in this paper was set to 0.05 pu of the line-to-line voltage. The THD when the high frequency signal is not injected is =1.15% while it increases to =1.38% when the high frequency signal was injected, not compromising therefore the connection standards [1-11].

For the secondary high frequency signal  $(v_{dahf2})$ , which is injected only for communication purpose, the magnitude should be high enough to enable reliable detection by the remaining microgrid inverters, while the same considerations as for  $v_{dqhf1}$  could be made for its frequency. A magnitude of 0.05 pu was found enough for reliable reception by the remaining microgrid inverters

## VI. Experimental results



1.5

0.5

To verify the viability of the proposed islanding detection and dynamic master assignment methods, the experimental setup shown at Fig. 8 was used. Though not shown in the figure, inverters 2 and 3 have the same topology as the master inverter, each including a DSP TMS320F28335 for their control. The parameters of the experimental setup are summarized in Table II. All the inverters include voltage sensors in the line side, which are needed for synchronization. The computational requirements for the implementation of the method are of 8.2µs for the master inverter operation mode and 12.8µs for the slave inverter operation mode

Fig. 9 shows the magnitude of the output voltage of the high frequency current regulator (4) of inverters 2 and 3 during transitions from island to grid connected (t=0.5s) and back to island (t=1.5s). The master inverter was injecting the

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the measured output current of the master inverter LCL filter. Fig. 10b shows the injected high frequency voltage, while Fig. 10c shows the resulting high frequency current. It is observed that the master inverter is continuously injecting a

high frequency signal, the resulting current strongly changing from island to line connected, which is used by the master inverter to detect the islanding/grid connected situations as described in [19]. Fig 10d shows the d and q-axis components of the current measured at the slave inverter LCL filter, while Fig. 10e and 10f shows the high frequency voltage injected by the slave inverter as well as the high frequency current at the slave inverter output. The *infinite impedance* mode of operation describe previously causes the high frequency current to be equal to zero in steady state.



<sup>&#</sup>x27; 1.3 1.4 1.5 1.6 1.7 Fig. 11 Transition from grid-connected to island situation (t=1.5s), a) to c) Master inverter a) current vector d (blue) and q-axis (red) components, of the measured output LCL filter current,  $i_{maxis}$ , b) injected high frequency voltage by the master inverter, c) measured output LCL filter (urrent),  $i_{maxis}$ , (d) to h slave inverter (meter 2), c) Current vector, d (blue) and q-axis (red) of the measured output LCL filter (urrent),  $i_{maxis}$ , (d) to f) slave inverter (inverter 2), c) Current vector, d (blue) and q-axis (red), of the measured output LCL filter current,  $i_{maxis}$ , c) injected high frequency voltage by the master (urrent regulator reaction) and f) measured output LCL high frequency currents  $i_{maxis}$ ,  $i_{maxis}$ 

Fig 11 shows the same results as Fig. 10 during a transition for grid connected to island situation, a similar

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## A.1.4 Synchronization in highly distorted three-phase grids using selective notch filters



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Abstract— Robust methods able to extract the magnitude and frequency of the positive sequence voltage in highly distorted grids is of paramount importance in distributed power generation (DPG) systems. Phase locked loop (PLL) synchronization methods are commonly used for this purpose. PLLs can be grouped into pre-filter stage methods and filter in the loop methods. Both provide similar performance and can be designed to reject one or more disturbing hormonic component. Hawayer compared to provide similar performance and can be designed to reject one or more disturbing harmonic components. However, compared to pre-filter stage methods, filter in the loop methods are conceptually simpler and easier to tune. Conversely, filter in the loop methods can show an unstable behavior if they are not properly designed and do not include disturbance rejection strategies when the magnitude is distorted, their use not being therefore advisable e.g. when power calculation, droop control or magnitude sucheronization are needed magnitude synchronization are needed

This paper proposes a filter in the loop synchronization technique, able to isolate the magnitude and phase of the positive sequence voltage of the microgrid/grid even under high distorted conditions. The method combines an angle-tracking observer, to obtain the positive sequence phase angle, and a scalar product to obtain the positive sequence magnitude, enhancing the disturbance rejection capability for both phase and magnitude estimation

*Index Terms* — three-phase grid synchronization, complex *PLL*, notch filters, filter on the loop, harmonic rejection.<sup>1</sup>

#### I. INTRODUCTION

Historically, centralized power plants have been considered the most effective and reliable way to generate electricity, the use of Distributed Power Generation (DPG) being traditionally use of Distributed Power Generation (DPG) being traditionally restricted to regions lacking adequate infrastructure. However, in recent years, due to the unstoppable increased electricity demand, natural resources decrease and environmental concerns, DPG is growing steadily. Actually only 1% of worldwide energy is generated by DPG, which includes both renewable (wind, solar, etc...) as well as non-renewable (fuel cells, micro gas turbines, etc...) energy resources, meaning that, globally speaking, the new paradigm is at an early stage. Although DPG is usually related to small or medium size power plants, it is expected that in the medium term each home-user can become an autonomous entity, with the capability not only of demanding but also of injecting power into the grid, which is commonly known as *micro-generation* into the grid, which is commonly known as micro-gen

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A very extended and suitable way to insert the DPGs into the electrical system is throughout microgrids. This concept was first defined in [2] as a system with renewable and no-renewable energy resources, including loads, energy storage and heat, being a controllable system providing power generation, power storage and heat to a local area. Generally speaking, a microgrid can operate in two different modes: island and grid-connected [3]. In island

mode, it works as an autonomous system, the magnitude and mode, it works as an autonomous system, the magnitude and frequency of the fundamental voltage being set by a master source or by a central controller [4]. In grid-connected mode, the magnitude and frequency of the fundamental voltage are established by the grid [3]. Estimation of the magnitude and phase of the positive sequence voltage at the point of common coupling (PCC) is of paramount importance to guarantee stable operation and precise control of the active/reactive novar drows in this case. power flows in this case

During grid-connected operation, strict regulations regarding power quality (harmonics and unbalances), islanding detection, frequency shifts and maximum magnitude deviations detection, frequency shifts and maximum magnitude deviations must be fulfilled [7], precise measurement of the fundamental voltage phase angle and magnitude being needed for this purpose. However, harmonics typically due to high power transients, non-linear loads or unbalances [9], often appear in the PCC voltage, development of synchronization methods able to work efficiently under high-distorted conditions is needed, to prevent the converter to re-inject the disturbances into the micropriderial into the microgrid/grid.

Synchronization methods can be roughly classified into methods that extract the grid frequency and methods that extract the grid phase, referred as frequency locked loop (FLL) extract the grid phase, referred as frequency locked loop (FLL) methods, and phase locked loop (PLL) methods respectively. The main drawback of the FLL methods is that they normally have a poor disturbance rejection capability against harmonic distortion [10], strategies to overcome these limitations have already been proposed [11]. On the other hand, PLL methods typically provide disturbance rejection capabilities against harmonic and unbalanced conditions [14], what makes them an appealing option. The PLL methods can be classified as follows: follows

- a) Methods that use a PLL in the synchronous reference frame (SRF-PLL) [15] or an angle tracking observer (ATO) [16]. This methods lock the grid phase and are (ATO) [16]. This methods lock the grid phase and are generally limited to undistorted networks, since do not implement any specific disturbance rejection mechanism, such capability being achieved if needed by using a reduced bandwidth in their PLL/ATO PI controller.
  b) Pre-filter stage methods. They use a previous filtering stage that feeds the SRF-PLL or ATO with the goal of removing specific harmonic components. The pre-filter stage can be composed by a decoupling network [12] or a

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#### b)

Magnitude estimation To estimate the magnitude of the fundamental voltage component,  $U_L$  the scalar product between the grid voltage,  $u_{a\beta}$ , and the unit vector  $e^{i\beta_{ac}}$  is performed, with the phase angle of the unit vector being estimated by the ATO (see Fig. 1). A filtering stage is placed after the scalar product to  $\begin{aligned} & f_{\mu\nu}(t) = 0 \\ & \text{provide a disturbance rejection mechanism for the magnitude estimation, this is discussed in Section III. \\ & \varepsilon_{u} = U_{uq}(t) \cdot e^{i \omega_{u} \cdot t} = \text{Re} \left\{ U_{uq}(t) \right\} \cdot \cos(\omega_{b} \cdot t) + \text{Im} \left\{ U_{uq}(t) \right\} \cdot \sin(\omega_{b} \cdot t) \quad (6.1) \end{aligned}$ 

 $\varepsilon_{M} = U_{1} + \sum U_{n} \cos(6 \cdot m \cdot \omega_{0} \cdot t)$ (6.2)

$$\mathcal{E}_{M} = U_{1} + \sum_{n=0}^{n=010} U_{n} \cos\left(2 \cdot m \cdot \omega_{0} \cdot t\right)$$
(6.3)

$$U_{1} = -Balanced = -Unbalanced$$
  
 $U_{1}+U_{1} = U_{2}+U_{1} = U_{1}+U_{1}$   
 $U_{1}+U_{2} = U_{2}+U_{1} = U_{2}+U_{1}$   
 $U_{2}+U_{2} = U_{2}+U_{1} = U_{2}+U_{2}$   
 $U_{2}+U_{2} = U_{2}+U_{2}$ 

Fig. 3- Harmonics of  $\epsilon_M$  using the proposed magnitude estimation method, for case of balanced and unbalanced voltages.

for case of balanced and unbalanced voltages. Similarly to the phase extraction procedure discussed previously, if the input complex voltage vector is balanced (2), the scalar product will be of the form shown by (6.2). For the case of  $\theta = \gamma = 0$ , the spectrum of  $\varepsilon_{\rm M}$  consist of a DC component, whose amplitude is the grid fundamental voltage component ( $\underline{U}_2$ ), and a set of harmonic components located at  $h^* \delta^* \omega_0$  ( $h=1,2,3,\ldots$ ), the corresponding frequency spectrum is shown in Fig. 3. Conversely, if the input complex vector of the magnitude estimation block is the same as an unbalanced-fed nonlinear load defined in (5), the spectrum of  $\varepsilon_{\rm M}$  (6.3) is composed by a DC component, ( $U_1$ ), and harmonic component solution and harmonic components located at  $h^*2*\omega_0$  ( $h=1,2,3,\ldots$ ).

## III. FILTERING STAGE, TUNING PROCESS AND STABILITY CRITERIA

As already mentioned, the frequency spectrum of the PI regulator input (4) and amplitude errors (6) will be of the form regulation input (\*) and amplitude cross (5) will be of the folding  $h^*\delta_{\omega_0}$  if the grid voltage is balanced and  $h^*2^*\omega_0$  if the grid voltage is unbalanced, with  $h=1,2,3,\dots$  Cascaded second order notch filters, (13), are used to remove specific harmonic components. The notch filter design requirements, [20], indicate that its transfer function when the nortex learned learned is the second s indicates that its transfer function must have the ceros located on top of the unit circle at the notch frequency ( $e^{i\pi s}$ ), and the poles located within the unit circle and near to the zeros, to assure unitary gain for the non-notch band, the nearer the poles assure unitary gain for the non-hotch band, the nearer the poles are to the unit circle, the smaller being the bandwidth of the notch filter [20]. To reject the disturbances modeled in the previous section, a filtering stage consisting on "n" cascaded notch filters is proposed (see Fig. 4), their design, tuning and digital implementation, as well as their stability analysis, is addressed in this section. *a) Filtering stage design* The transfer function of a generic second order analog

a) Filtering stage design The transfer function of a generic second order analog notch filter can be expressed as (7), where  $\xi$  sets the depth and the width of the filter and  $\Omega_n$  is the notch frequency. Since the proposed NFOL-CPLL method is intended to be implemented digitally, the system design and stability analysis will be performed in the discrete time domain. Tustin discretization will be used (8) to transform from the

continuous domain to the discrete domain, (9) being obtained by discretization of (7).

$$NF\left(s\right) = \frac{s^{2} + \Omega_{n}^{2}}{s^{2} + \xi \cdot s + \Omega_{n}^{2}}; \ \Omega_{n} = n \cdot \Omega_{o}$$
(7)

$$s = \frac{2}{T_s} \frac{z - 1}{z + 1}$$
(8)  $NF_{\omega_s}(z) = b \frac{1 - 2 \cdot \cos(\omega_s) z^{-1} + z^{-2}}{1 - 2 \cdot b \cdot \cos(\omega_s) z^{-1} + (2 \cdot b - 1) z}$ (9)

$$\omega_n = \frac{n \cdot \omega_0}{f_s/2} \quad (10) \quad b = \frac{1}{1+\beta} \tag{11}$$

$$\beta = \frac{\sqrt{1 - A^{-}_{-\Delta B}}}{A_{-\Delta B}} \tan\left(\frac{BW}{2}\right); BW = \frac{\Delta w}{f_s/2}$$
(12)

$$FS\left(z\right) = \prod_{n=1}^{N} NF_{\sigma_{n}}\left(z\right) = \frac{\prod_{i=1}^{l} (z-c_{i})}{\prod_{k=1}^{p} (z-p_{k})}$$
(13)

where  $\omega_s$  is the notch frequency (10),  $\omega_0$  stands for the rated grid frequency,  $T_s$  and  $f_s$  are the sampling time and the sampling frequency respectively, BW is the notch filter bandwidth and  $\Lambda_{3dB}$  is the notch filter magnitude at half squared magnitude ( $_{10} \aleph_{-} \sqrt{L}/2$ ) (See Fig. 5).



Fig. 4- Filtering stage block diagram Fig. 5- Digital notch filter design The international standards for grid-connected converters, [6], limit the maximum overall voltage harmonic distortion (THD) to 5%, with each individual harmonic magnitude being smaller than 4% for harmonic orders lower than 11<sup>th</sup>, 2% for the harmonic orders between 11<sup>th</sup> and 17<sup>th</sup>, 1.5% for harmonic orders between 17<sup>th</sup> and 23<sup>rd</sup>, 0.6% for harmonic orders between 23<sup>rd</sup> and 35<sup>th</sup> and 0.3% for orders higher than 35<sup>th</sup>. Since each notch filter adds an additional phase shift in the estimated phase angle of the fundamental voltage, it is convenient to limit the number of notch filters being cascaded. Therefore, only harmonics whose order is lower than 11<sup>th</sup> will be considered for the filtering process. The proposed filtering stage consists of three notch filters, (9), located at ω<sub>2</sub>=2<sup>\*</sup>w<sub>0</sub> (100 Hz), ω<sub>2</sub>=4<sup>\*</sup>w<sub>0</sub> (200 Hz) and ω<sub>2</sub>=6<sup>\*</sup>w<sub>0</sub> (300Hz), which corresponds to 1<sup>th</sup>, 3<sup>\*'d</sup>, 3<sup>\*'d</sup>, 5<sup>th</sup>, -5<sup>th</sup> and 7<sup>th</sup> harmonics of the grid voltage (see section 2), Adding new harmonic components would be straightforward.

components would be straightforward. Finally, a low-pass filter could be added to the filtering stage in order to deal with noise coming from the sensors and electronics. It is not necessary to include it within the ATO, as the PI regulator effectively acts as a low-pass filter. However, it can be placed after the scalar product used for magnitude estimation. In this case, a 300 Hz low-pass filter has been used.

Fig. 6 shows the zero-pole map when (9) is used for the selected notch frequencies, with bandwidth of 7.95 Hz (50 rad/s), shown at is obtained. It is observed that all zeros are

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d). Simulation results are shown in ltage and frequency being 220 rely. The magnitude, frequency vill be shown as these signals are rel s, including synchronization, mr on, droop control, power calculation	per unit, the rated V and 50 Hz and phase error evant for different ignitude/frequency , etc	normative unbalance factor was used during $1 \le t \le 2_s$ , ther 10% upper-normative unbalance factor was used during $1 \ge$ The unbalance rejection capability of all of the tested methe is high, both in estimated magnitude (Fig. 12c), frequer (Fig. 12d) and phase (Fig. 12e).
fable I - Grid parameter boundaries by nor	native[23-25]	
Maximum value	Clearance time (s)	
$47 \le 10^{-1}$	0.2	b) 2 1.2
ueviation 0.8≤ vpu≤1.2	0.2	MCCF-PL
in distortion 4% individual harmonia		
n-like and sten-like frequency char	ges were used for	
juency deviation test (Fig. 10),	with the voltage	<u><u><u></u></u> -0.02</u>
de being kept constant. The corre	sponding profiles	d) 0.01
In In Fig. 10a and 10b. they include	a frequency ramp-	Ē 0
), which are intended to emula	te the inertia of	~_0.01
nous generators and/or the connectio	n/disconnection of	e) 0
ads in weak grids or islanded and	droop-controlled	(B) -5
us [26].	·····	s <sup>°</sup> -10 <u>i i i i i i</u> 1 1.2 1.4 1.6 1.8 2 2.2 2.4
		t(s) Fig. 11- Simulation results showing the response to changes in the magni
		Same variables as in Fig. 10 are shown.
F		
	MCCF-PLL	a) <sup>1.1</sup>
þ	CCCF-CPLL	al 1
		b) g 0.1
- · · · · ·		P 0 MCCF-PL
		c) 0.02
		≦ -0.02
		d) _ 0.01
1 12 14 16 18	2 22 24	
t(s)	fraguancy deviations: a)	
juency, b) magnitude, c) magnitude error, d	) frequency error, e) and	
r.		
e I shows the maximum deviation	s allowed for the	6 10 1 1.2 1.4 1.6 1.8 2 2.2 2.4
ut the performance of the method	is in the event of	Fig. 12- Simulation results showing the response to an unbalance in the p
in the magnitude is shown in F	ig. 11b, with the	<ul> <li>voltages: a) target frequency, b) voltage unbalance factor, c) magnitude</li> <li>d) frequency error and e) phase error.</li> </ul>
y kept constant (Fig. 11a).		Historically electric machines (mainly transformers to
e all the transient response three ed is correct for the case of ramp-li	e methods being	lesser extent, electric machines) were the main sources
y oscillation shows up in the tra	cked frequencies,	harmonics in power systems, however, the power electron
des and phases for the case of step-l	ike variations, that	equipment that is commonly used nowadays, has become of of the primary sources for harmonic distortion. Section II
ly in a few ms.	hy by unbalanced	and Table I describe the maximum harmonic distortion
id single phase loads, which creat	e unbalanced load	allowed for grid-connected equipment.
eventually resulting in non-symmet	rical voltage drops	Fig. 13 shows the simulation results when a 5 <sup>th</sup> harmonic
, eventually resulting in non symmet	e factor (VUE) is	fundamental frequency remaining constant (see Fig 13a)
hase voltage. The voltage unbaland		
hase voltage. The voltage unbaland lefined as the ratio between the neg- ive sequence voltage components [	itive sequence and	It is observed from Fig. 13 that MCCF-PLL and CCC
hase voltage. The voltage unbaland lefined as the ratio between the neg- tive sequence voltage components [2 ting shown in Table I (4%). Two	27], the acceptable voltage unbalance	It is observed from Fig. 13 that MCCF-PLL and CCC PLL methods do not completely reject the injected harmoni
hase voltage. The voltage unbalan- defined as the ratio between the negg- tive sequence voltage components [2 ing shown in Table I (4%). Two alues were tested (see Fig. 12b), v	ative sequence and 27], the acceptable voltage unbalance /ith the frequency	It is observed from Fig. 13 that MCCF-PLL and CCC PLL methods do not completely reject the injected harmoni oscillations being observed both in magnitude and frequer (Figs. 13e, d) in steady state. These oscillations do not both





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presented in this paper. The method is based on a notch-filter in the loop stage to eliminate disturbances and a complex PLL to extract the frequency/phase of the fundamental voltage component. A magnitude extraction block based on a scalar product to obtain the positive sequence amplitude of the grid voltage has also been proposed. The design of the filtering stage, tuning of the controller and stability of the method has been discussed. Six different types disturbances have been tested to verify the validity of the proposed method. It is concluded from these tests that the method shows an exceellent overall performance complying

method shows an excellent overall performance, complying with international detection standards.

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### A.1.5Islanding detection in grid-connected power converters using harmonics due to the non-ideal behavior of the inverter



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The distortion of the output voltage produces an increase in the THD of the voltages/currents, having therefore an adverse impact on the power quality [20, 22]. However, the induced harmonics can also be used as a form of high frequency excitation for active islanding detection purposes. In this paper, islanding detection using the higher order

In this paper, islanding detection using the higher order components of the inverter output voltage due to the nonideal behavior of the inverter is proposed. By using this harmonics, the injection of additional high frequency signals is avoided, which is beneficial in terms of power quality.

The paper is organized as follows: the analysis of the effects due to the dead-time in PWM inverters is presented in section II; the principles of the proposed islanding detection method are presented in section III, while simulation and experimental results to confirm the viability of the proposed method are finally provided in sections IV, V and VI.

### II. Dead-time effects in PWM inverters.

Fig. 1 schematically shows a three-phase PWM-VSI used to connect distributed energy resources to the three-phase utility grid/microgrid. Fig. 2 shows the gate signals for one leg without (subplots a) to c)) and with (subplots d) to g)) considering the dead-time in the gate signals. Fig. 2a and b show the ideal gate signals for switches 1 and 4, while Fig. 2c shows the ideal output voltage, i.e. with no voltage drop across the switches and on-off transitions of the upper and lower switches occurring simultaneously. In practice, due to the non-zero turm-on and turm-off times, a dead-time has to be inserted in every commutation to guarantee that the two switches in a branch (e.g. S1 and S4) do not conduct simultaneously. Fig. 2d and e show the real gate signals, after inserting the dead-time, when switches S1 and S4 are turned-on and off respectively. When both transistors are turned-off, one of the freewheeling diodes will conduct, depending on the sign of the output current. If the current is positive (see Fig. 1), D4 will be conducting (see Fig. 2g). In addition, it is observed from Fig. 2f and g that the voltage drop across the switches and diodes and the turn-on/off times are considered.

The average voltage errors caused by the non-ideal behavior of the inverter (turn-on, turn-off, voltage drops and dead-time) during each switching period can be calculated using (1) and (2) for the case of the current being positive and negative respectively (see Fig. 2f and g).

$$\begin{split} \Delta V &= \frac{T_d + t_{os}}{2T_s} \left( -V_{dc} - V_d \right) + \frac{t_{off}}{2T_s} \left( V_{dc} - V_{ost} \right) \\ &= \frac{-T_d - t_{ost} + t_{off}}{2T_s} V_{dc} + \frac{-T_d - t_{ost}}{2T_s} V_d + \frac{-t_{off}}{2T_s} V_{sot} \end{split}$$
(1)

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Fig. 3.- Phase current, a), average voltage error, b), d and q components of the average voltage complex vector, c) and d).



$$\Delta V = \frac{T_d + T_{out}}{2T_s} \left( V_{dc} + V_d \right) + \frac{\tau_{eff}}{2T_s} \left( -V_{dc} + V_{sat} \right)$$

$$= \frac{T_d + t_{out} - t_{off}}{2T_s} V_{dc} + \frac{T_d + t_{out}}{2T_s} V_d + \frac{t_{off}}{2T_s} V_{sat}$$
(2)

where  $T_d$  is the dead-time,  $t_{on}$  is the turn-on time of the power switch,  $t_{off}$  is the turn-off time of the power switch,  $T_s$  is the sampling period,  $V_{dc}$  is the dc bus voltage,  $V_d$  is

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forward voltage drop of the diode and  $V_{sat}$  is the on-state voltage drop across the power switch.

Assumed that  $V_d \approx V_{sab}$  (1) and (2) can be safely simplified to (3) and (4) [22].

$$\Delta V = \frac{-T_d - t_{on} + t_{off}}{2T_s} V_{dc} - \frac{T_d + t_{on} + t_{off}}{2T_s} V_{sar}$$
(3)  
$$\Delta V = \frac{T_d + t_{on} - t_{off}}{2T_s} V_{dc} + \frac{T_d + t_{on} + t_{off}}{2T_s} V_{sar}$$
(4)

Fig. 3b shows the voltage error for phase *a* averaged for each switching cycle, which is seen to depend on the sign of the output current (see Fig. 3a). It is observed from Fig. 3b that the average voltage error is a square wave, which can therefore be expressed using Fourier series as (5). Taking into account the  $2\pi/3$  phase shift between phases in a balanced three-phase system, the average voltage errors for phases *b* and *c* can be expressed as (6) and (7), with *n* being the harmonic order.

$$V_{an} = \frac{4\Delta V}{\pi} \sum_{n=1,5,7\dots} \frac{1}{n} \sin(n\omega t)$$
(5)

$$V_{bn} = \frac{4\Delta V}{\pi} \sum_{n=1.5,7\dots} \frac{1}{n} \sin\left[n\left(\omega t - \frac{2\pi}{3}\right)\right]$$
(6)

$$V_{cn} = \frac{4\Delta V}{\pi} \sum_{n=1,5,1,...,n} \frac{1}{n} \sin\left[n\left(\omega t - \frac{4\pi}{3}\right)\right]$$
(7)  
The resulting voltage vector due to the the ponsid

The resulting voltage vector due to the the non-ideal behavior of the inverter can be expressed as (8) (see Fig. 3c and d), with the transformation from phase quantities to dq quantities being defined by (9).

$$v_{dq} = \sum_{n=1,-5,7,..} V_n e^{j(n\omega_0 t + \theta)}$$

$$f_{-s,-}^s = f_s + i f_s = \frac{2}{2} \left( f_s + f_s e^{j2\pi/3} + f_s e^{j4\pi/3} \right)$$
(8)
(9)

$$y_{dq} - y_d + y_q - y_3(y_a + y_b e^{-1} + y_c e^{-1})$$
 (7)  
where  $\theta = \pi$  when n<0 and  $\theta = -\pi$  when n>0,  $\omega_0$  is the  
grid/microgrid frequency and  $V_n$  is given by (10)

$$V_n = \frac{2 * \Delta V}{n\pi} \Big[ -2\cos(n\pi) - \cos(n\,2\pi/3) + \cos(n\,\pi/3) \Big]$$
(10)

It is concluded from (5)-(8) that the inverter non-ideal behavior produces harmonics having orders of -5, 7,..., with the corresponding harmonic magnitude being inversely proportional to the harmonic order, (10) [27] (see Fig. 4). Fig. 5 and 6 show the frequency spectrum of the voltage

Fig. 5 and 6 show the frequency spectrum of the voltage and current complex vectors (experimental) for a VSI, measured at the output of the LCL filter, in island and grid connected conditions respectively. The details of the inverter can be found in Table III. Logarithmic scales are used for the magnitudes. Harmonics of order -5<sup>th</sup> and 7<sup>th</sup> are readily observable in both the voltage and current spectrums, their magnitudes being inversely proportional to the harmonic order. It is observed that in the grid connected case, the harmonics induced in the resulting current vector due to the non-ideal behavior of the inverter increase, compared to the island case. This is explained by the lower impedance during this operating condition. It is also noted that the resulting higher order harmonics at the output of the LCL filter decrease in grid-connected mode. This is due to the increased voltage drop across the filter because of the lager circulating currents.



 $_{\rm UJ}$   $^{-10}$   $^{-5}$  0 5  $^{-5}$  harmonic order  $^{-5}$  Fig. 5.- a) Voltage complex vector ( $v_{\rm days}$ ) spectrum and b) current complex vector ( $l_{\rm days}$ ) spectrums in island condition. The fundamental frequency is 50 Hz, with a dead-time of 3µs and switching frequency of 10kHz.



b)  $^{-10}$   $^{-5}$  0  $^{5}$ harmonic order Fig. 6.- a) Voltage complex vector ( $v_{\rm dugs}$ ) spectrum and b) current complex vector ( $v_{\rm dugs}$ ) spectrum, in grid connected condition. The fundamental frequency is 50 Hz, with a dead-time of 3µs and switching frequency of 10kHz.

#### III. Islanding detection using harmonics due to the deadtime

The harmonics due to the non-linear behavior of the inverter, (8), can be modeled as (11). Every harmonic in the voltage will produce the corresponding harmonic at the same frequency in the inverter current ( $i_{doly}$ ). The resulting harmonic component at the output of the LCL filter being (12) (see Fig. 7).

$$i_{dq\mu ghf} = \frac{v_{a}e^{e^{-y_{a}}}}{jn\omega_{0}L_{2}}$$
(11)  
$$i_{dq\mu ghf} = \frac{v_{dq\mu} - v_{dq\mu ghf} - jn\omega_{0}L_{1}i_{dqhf}}{jn\omega_{0}L_{2}}$$
(12)

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German standard [7] and 0.5 Ohms in 5 seconds for the Swiss and Australian standards [8, 9]. It is observed that both the magnitude and phase could be potentially used for islanding detection purpose, the change of the high frequency impedance being detected if a few ms.. It is concluded from Fig. 10 that the islanding detection requirements are widely met by the proposed method.

It is noted that the dead-time can vary in a relatively large range, depending on the rated voltage and current of the power switches [32]. In general, a shorter dead-time would be preferred, since it implies lower distortion (THD) of the output inverter voltage. Increasing the dead-time, increases the magnitude of the voltage error and current harmonics, which increases the signal to noise ratio for the islanding detection signal processing, however it also increases the THD, which is limited by connection standards [2, 28-31]. The selection of the dead-time results therefore from a compromise between the signal-to-noise ratio and meeting the connection standards in terms of THD. The simulated dead-time is 5 $\mu$ s, resulting in a THD of  $\approx$ 0.87%, not compromising therefore the connection standards [2, 28-31].

Fig. 11 shows the high frequency current regulator output voltage when the block diagram shown in Fig 8 is used and the same transition as in Fig. 10 occurs. It is observed that the change on the current regulator output occurs in a few ms., therefore meeting the islanding detection standards [2-9]. Fig. 12 shows the magnitude of the -5, 7, -11 and 13 harmonics of the current vector, without and with compensation of the -5th harmonic. It is observed that when the compensation is implemented, the -5th fades away. Despite of the slight increase of the 7th harmonic, a reduction of the overall harmonic content, and therefore of the THD, is observed.



Fig. 12.- Harmonics of the current vector with and without compensation of the 5<sup>th</sup> harmonic implemented.

#### V. Islanding detection for parallel inverter operation

The proposed strategy has been evaluated so far for a single inverter connected to the utility grid. However in a general case, several micro-sources connected to the utility grid throughout a PCC will exist in the microgrid. To evaluate the proposed method, a scenario with three parallel-connected converters, has been built as an example (Fig. 13). The simulation parameters are shows in Table II.

Fig. 14a and b show the magnitude and phase of the estimated high frequency impedance in a transition from







# A.1.6 Coordinated Operation of Parallel-Connected Inverters for Active Islanding Detection Using High Frequency Signal Injection





Recently published works have shown that the high frequency impedance is a reliable metric to detect an islanding situation [17-22]. Voltage-source inverters (VSI) present in a microgrid (e.g. in controlled rectifiers used in APFs, back-to-back power converters, ...) can easily inject a low-magnitude, high-frequency voltage, from which the high frequency impedance is estimated. As an example, a rotating high frequency signal (1) can be injected, the induced high frequency current iFhf being (2), Zhf (3) being the high frequency impedance at the excitation frequency, with its phase angle being  $\varphi_z$ , where  $\omega_{hf}$  and  $V_{hf}$  are the frequency and magnitude of the injected high frequency voltage.

$$v_{hf} = V_{hf} e^{j\omega_{hf}t}$$
(1)  
$$i_{Fhf} = \frac{V_{hf}}{Z_{hf}} e^{j(\omega_{hf}t - \phi_{z})}$$
(2)

$$Z_{hf} = R_{hf} + j\omega_{hf}L_{hf}; \varphi_z = \operatorname{atan}\left(\frac{\omega_{hf}L_{hf}}{R_{hf}}\right)$$
(3)

Fig. 1 shows the schematic implementation of the method. Fig. 2a and 2b show the magnitude and phase of the high frequency impedance  $Z_{hf}$ , during a transition from island to grid, and from grid to island. The change in both metrics between islanding and grid condition are readily observable. Islanding detection is based on the rate of variation of  $Z_{hj}$ with time, i.e.  $\Delta Z_{hf} / \Delta t$ . Comparison of  $Z_{hf}$  with a threshold might also potentially be used [21]. Further discussion on other forms of high frequency excitation as well as on the implementation of this method can be found in [21,22].

#### III.- Islanding detection using high frequency voltage injection for the case of multiple inverters

While simple for the case of a single inverter, the extension of the method described in Section II to the case of multiple inverters is not trivial, strategies that have been proposes to address this case are discussed in this section. In the discussion following, master inverters refers to inverters which inject a high frequency signal to detect the microgrid

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inverters are responsible of informing the slave inverters of the grid condition. For the evaluation of the strategies, the following issues need to be taken into account: • All the inverters in the microgrid participating in the

- strategy should *know* the microgrid condition (island/grid connected) within a time frame compatible with islanding detection standards.
- The adverse impact on the microgrid/grid power quality (THD), due to the injection of high frequency s should be kept as small as possible, and below the limits established by the connection standards [4-7]. • Use of separate communication channels is not allowed.
- The injection of an additional high frequency signal for communication purposes is acceptable, as this does not have the problems/concerns intrinsic to communications, like cost and the risk of communication breakdown. Details on the use of the secondary high frequency signal can be found in [21,22].

a) Static, single master inverter

In [21], the use of a master inverter, responsible of injecting a high frequency rotating voltage vector (1), was proposed, the rest of inverters in the microgrid being configure to be slaves. Two high frequency signals were injected by the master inverter: the first one for islanding detection, as described in Section II: the second one to communicate the islanding condition to the rest of (slave) inverters present in the microgrid. While no interference between inverters can occur -only the master inverter injects high frequency signals-, this method has several limitations: • Failure of the master inverter would leave the grid without

- the high frequency signal voltage, the rest of inverters in the grid hence losing their capability to detect islanding.
- . In large microgrids, the location of the master inverter has In large microgrids, the location of the master inverter has to be carefully chosen. For inverters located far from the PCC, the variation of the high frequency impedance between grid and island condition might be small, reducing the reliability of the method.

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the high frequency voltage is simple in principle [21], this may be difficult in practice, as the signals can be corrupted by noise in the acquisition system, harmonics in the voltages due to non-linear loads, transients, etc. Spurious detection of the high frequency voltage might result in frequent, unwanted transitions between For a given magnitude of the injected high frequency

voltage at the filter output, the resulting high frequency component of the filter current  $i_{Fhf}$  (4), will be function of the high frequency voltage  $v_{Fhf}$ , the output filter impedance  $Z_{F}$ , and the equivalent high frequency impedance  $Z_{hf}$ , seen at the point of connection of the inverter to the microgrid.

 $i_{Fhf} = \frac{v_{Fhf}}{Z_F + Z_{hf}}$ 

While  $v_{Fhf}$ , and  $Z_F$  are known in advance, significant While  $v_{Fhf}$  and  $Z_F$  are known in advance, significant uncertainty exists regarding  $Z_{hf}$ . For inverters close to the PCC in grid operation, this impedance can be very small, the circulating high frequency current  $i_{Fhf}$  being therefore large, adversely impacting the power quality (THD). To overcome aforementioned limitations, a strategy for

the coordinated operation of multiple parallel connected inverters in a microgrid is proposed in the following section.

#### IV.- Islanding detection in microgrids with multiple inverters using combined current/voltage injection

Most of signal injection based, islanding detection methods proposed so far, inject a high frequency voltage, the island/grid condition being estimated either from the resulting high frequency current or from the high frequency impedance. However, it is also possible to inject a high frequency current, a high frequency current regulator being used for this purpose. Current injection can be advantageous in certain cases. For

inverters operating near the PCC during grid operation, the equivalent impedance will be small, what might result in a relatively large high frequency current if a constant voltage is injected. Using high frequency current injection automatically limits the resulting high frequency current. On the contrary, high frequency voltage injection would be advantageous during island operation or for inverters located far from the PCC, where injection of the rated high frequency current would require too much voltage. Combining high frequency voltage injection and high frequency current injection would therefore be beneficial for inverters experiencing large variations in the high frequency impedance seen at their terminals, as would be the case of inverters working near the PCC.

Islanding detection using combined voltage/current injection is analyzed in this section. In the proposed strategy, all the inverters synchronously inject a high frequency signal, dynamically readapting their mode of operation between voltage and current injection, depending on their location and on the grid condition. The model used for the analysis is first presented, combined voltage/current injection, synchronization of the high frequency signals, as well as the parallel operation of inverters, being analyzed in further subsections.





as a Voltage source. For inverters operating in the Current source mode, (5) can be algebraically rearranged by moving the corresponding current iFk to the left term (inputs vector) and the inverter voltage  $v_{lf}k$  to the right side (outputs vector) of the equation respectively.

b) Combined high frequency Voltage/Current signal injection A means to combine current and voltage injection providing automatic, smooth transition between both modes of operation, is to add a saturation mechanism as a part of the high frequency current regulator [25]. This mechanism, named realizable references, is schematically shown in Fig. 5. A PI current regulator implemented in a reference frame synchronous with the high frequency signal is used, the current command being  $t_{pf}^*$  (see Fig. 5). If the voltage  $v_{hf}$  required to supply the commanded current is lower than the established voltage limit (*limiter* in Fig. 5), the current injection mode works normally. This will occur if  $Z_{hf}$  is small. On the contrary, if the voltage  $v_{hf}$  goes beyond the established voltage limit  $v_{hfmax}$ , the voltage effectively injected is limited to this value. This will be the case when  $Z_{hf}$  is large. If this occurs, the current command is recalculated to make it consistent with the high frequency voltage commanded to the inverter  $v_{hfmax}$ . In each sampling period, the regulator equation is computed digitally in the regular way (6) to (8), (Euler's approach was used in (8)), assuming that the actual current command is *realizable*, i.e. will not saturate the output voltage.

$\hat{i}^*_{Fhf(k)} = i_{hfmax}$	(6)
$e_{Fhf(k)} = \hat{i}_{Fhf(k)}^* - i_{Fhf(k)}$	(7)
$v_{hf(k)}^* = v_{hf(k-1)}^* + (K_p + K_i T) e_{Fhf(k)} - K_p e_{Fhf(k-1)}$	(8)

If the obtained voltage does not need to be limited, no further action is required. On the contrary, if the output voltage has to be limited (9), a new, *realizable reference*, is computed by using the regulator equations backwards, (10) and (11). The equations are written trying to clarify the technique rather than with an optimal implementation.

$$\begin{aligned} & lf \quad v_{hf(k)} > v_{hfmax} \to v_{hf(k)} = v_{hfmax} & (9) \\ & e_{hf(k)}^{e} = \frac{v_{hf(k)}^{e^{*}} - v_{hf(k-1)}^{e^{*}} + K_{p} e_{hf(k-1)}^{e}}{K_{p} + K_{i}T} & (10) \end{aligned}$$

$$i_{hf(k)}^{e^*} = e_{hf(k)}^e + i_{hf(k)}^e$$
(11)

After computing equations (10) and (11), the current error and the output voltage will be consistent. The realizable reference reflects therefore a current command consistent with the controller voltage limit. Because of its design basis, the realizable reference does not depend on any load parameter.

Fig. 6 schematically shows the injected high frequency voltage at the inverter terminals (commanded), the high frequency voltage at the filter output, and the resulting high frequency current, as a function of the relationship between the filter impedance  $Z_{F}$  and the equivalent high frequency impedance  $Z_{hf}$ . When the impedance  $Z_{hf}$  is large, the inverter output voltage is limited, i.e. operates as a *Voltage source*. As  $Z_{hf}$  decreases ( $Z_F/Z_{hf}$  increases), once the high frequency current reaches its rated value, the inverter works in the current control mode, behaving therefore as a *Current source*.

For the implementation of the strategy,  $i_{hfmax}$  is selected first. The relationship between  $i_{hfmax}$  and  $v_{hfmax}$  is set to be (12), where  $Z_F$  is the (known) filter impedance, and  $\hat{Z}_{hf}$  is the preset value of the high frequency impedance at which the change between *Voltage source* and *Current source* occurs. For the simulation and experiments carried out in this paper,  $i_{hfmax}$  was set to 1.5% of the rated current and  $\hat{Z}_{hf}$  to 0.35- $Z_F$ ,  $v_{hfmax}$  for the limiter block in Fig. 5 being obtained from (12).

(12)

$$v_{hfmax} = i_{hfmax} (Z_F + \hat{Z}_{hf})$$

Fig. 7 shows the simulated response of the method. During island mode, the voltage is limited (Fig. 7a), the high frequency current command being recalculated using (9)-(11) to be consistent with the voltage. During grid operation, due to the reduction of the impedance seen by the inverter, current injection works normally, the high frequency current command being equal to the nominal value *lifimax*.

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Frequency current, The limits for the high frequency voltage, vhfmax, and current, ihfmax, (see Fig. 6 and 7), are indicated in Fig. 8a and 8b. It is noted that node #1 corresponds to the PCC, the load current in this node coinciding therefore with the high frequency current circulating into the grid. It is observed from Fig. 8 a-left and b-left that in grid-

connected mode, inverters in nodes #1, #2, and #7 operate in the *Current source* mode. Due to their closeness to the PCC, the impedance seen by these inverters is small, their high frequency current being limited to *ihfmax*. On the contrary, nodes #3 to #6 operate in the *Voltage source* mode, as they are further from the PCC. It is remarked again that the transition between *Voltage source* and *Current source* occurs smoothly, no reconfiguration of the injection mechanism being needed. *e) Islanding detection and islanding notification* 

Islanding is detected from the measured high frequency impedance. Fig. 8c shows the high frequency impedance seen at the inverters terminal (13) and filters output (14).

$$Z_{F} + Z_{hf} = \frac{v_{hf}}{i_{Fhf}} \approx \frac{v_{hf}^*}{i_{Fhf}} \tag{13}$$
$$Z_{hf} = \frac{v_{Lhf}}{i_{Ener}} \tag{14}$$

Since  $Z_{hf}$  is the variable reflecting the changes between grid and islanding modes, (14) would be used in principle for islanding detection. However, using (13) has the advantage that the commanded high frequency voltage can be used,

instead of the high frequency component of the measured line voltage needed in (14), slightly simplifying the required signal processing. Still both options are expected to give similar results.

processing. Still both options are expected to give similar results. Some expected facts are observed in Fig. 8. For the case of grid-connected operation, the high frequency impedances for each node (both  $Z_{hf}$  and  $Z_F + Z_{hf}$  in Fig. 8c) depend on the node location, relative to the PCC, the impedance for nodes closer to the PCC being significantly smaller. Comparing the nodes impedances for the case of grid (Fig. 8c-left) and island (Fig. 8c-right), the nodes closer to the PCC experience the largest variations of the high frequency impedance between grid and island connection.

Currently, islanding detection is based on the rate of variation of  $Z_{hf}$  with time, i.e.  $\Delta Z_{hf} / \Delta t$  [4-13]. Comparison of  $D_{hf}$  with a threshold might also potentially be used [21]. Islanding detection for nodes closer to the PCC will be easier and more reliable. On the contrary, islanding detection might be difficult for nodes far from the PCC in large microgrids. Thus, inverters working in the *Current source* mode would be in principle better candidates to detect islanding than inverters working in the *Voltage source* mode.

inverters working in the *Voltage source* mode. A possible strategy would be to enable only inverters working in the *Current source* to *inform* of the grid condition to the rest of inverters present in the microgrid, using a secondary high frequency signal for this purpose. Inverters working in the *Current source* mode would detect islanding by measuring a positive  $\Delta Z_{hf}$  over a predefined time window. Once islanding is detected, they would inject the secondary high frequency signal  $v_{hf2}$ . On the contrary, if inverters injecting the secondary high frequency voltage detect the change between islanding and grid-mode from the measured  $\Delta Z_{hf7}$  they would discontinue injecting the secondary high frequency voltage. Injection of the secondary high frequency voltage is schematically shown in Fig. 7d, details on the use of the method can be found in [21,22].

This strategy has not been studied in detail, further analysis would be needed to verify its viability and performance.

### V.- Experimental results

The proposed islanding detection strategy has been tested using the experimental setup shown in Fig. 9, the parameters being summarized in Table I. Both inverters are identical, they use IGBTs, all the control (current regulators, synchronization, etc.) being implemented on a TMS320F28335 DSP. Fig. 10 shows the transition between island and grid

Fig. 10 shows the transition between island and grid modes. Fig. 10a and 10c show the commanded and filter output voltages for both inverters, while Fig. 10b and 10d show the corresponding high frequency currents. The magnitude of the high frequency current  $ih_{fimax}$  is set to 1 A (1.5% rated current). It is observed from Fig. 10b that during islanding, both inverters operate in the *Voltage source* mode, with  $v_{hfimax} = 13$  V. During island operation, Inverter #1 changes its mode of operation to the *Current source* mode, its high frequency current being limited to  $ih_{fimax}$ , while Inverter #2 keeps operating in the *Voltage source* mode. This is due to the line impedance between Inverter #2 and the PCC.

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# A.1.7 Strategies for the Connection of Distributed Power Generation Units to Distorted Networks





The steady state term has the same frequency as the input signal and its magnitude depends on the filter and transmission line parameters (9) and (10)

$$\frac{d_{agh}}{d_{agh}} = \frac{\frac{s}{L}}{s^2 + s\frac{R}{L} + \frac{1}{LC}}$$
(3)

$$p_1 = -\alpha + j \cdot \omega_r; p_2 = -\alpha - j \cdot \omega_r;$$

$$R$$

$$\alpha = \frac{\kappa}{2L}$$
(5)
$$\omega_r = \sqrt{\frac{1}{CL} - \frac{R^2}{4L^2}}$$
(6)
$$v_{a(gh)} = |v_{a(gh)}| e^{j(\omega_{\mu} - \omega_{h})r}$$
(7)

 $i_{dqgh} = i_{steady} + i_{trans} = \left| i_{steady} \right| e^{j\left((\omega_{gh} - \omega_0)t + \Theta\right)} + \frac{\left| v_{dqgh} \right|}{L\omega_r} e^{\alpha t} e^{j\omega_r t}$ 

$$\begin{vmatrix} i_{steady} \end{vmatrix} = \frac{|v_{stagk}|}{\sqrt{R^2 + \left(\omega_{gh}L - \frac{1}{\omega_{gh}C}\right)^2}}$$
(9)  
$$\Theta = \tan^{-1} \left(\frac{\omega_{gh}L - \frac{1}{\omega_{gh}C}}{R}\right)$$
(10)

B. Connection of VSCs to distorted grids through LCL filters Fig. 4 shows the equivalent circuit of a VSC using an LCL The transmission line is connected between the LCL filter. filter output and the breaker S, being modeled as in the previous subsection. The inverter is synchronized with the positive sequence component of the fundamental voltage at the PCC,  $i_{dql}$  and  $v_{dqug}$  only consisting therefore of the

fundamental component. When the breaker closes, the current to voltage transfer function is also modeled by (3), the equivalent inductance resulting from the series connection of the line inductance and the LCL filter grid-side inductance  $(\rm L=L_{TL}+L_g)$  and the equivalent resistance R being the result of the series connection of the transmission line, LCL filter grid-side inductance resistance and filter capacitor resistance, i.e.  $R = R_{TL} + R_g + R_c.$ 

The time response for this case can also be described by (8), and is seem to consist of a transient term with a time constant (5) and resonance frequency (6), and a steady state term with the same frequency as the PCC harmonic voltage ( $\omega_{gh}$ - $\omega_o$ ), of magnitude and phase (9) and (10) respectively.



harmonic voltage components can be considered for the synchronization strategy. Fig. 5 shows control block diagram of the proposed strategy. A combination of proportional-integral (PI), (11) and resonant (RES) regulators, (12), in *dq* reference frame synchronous with the grid fundamental frequency are used (13), both for the current and voltage. The PI synchronous regulators (11) are used to control the fundamental voltage and current components, while each RES controller (12) is used to control a specific harmonic component of the voltage and current, with *n* being the harmonic order. It is noted that in a harmonic of order *n*=*h*-*l* in a reference frame synchronous with the fundamental request. with the fundamental component of the grid voltage,

$$PI(s) = K_r + \frac{\kappa_i}{s}$$
(11)  
$$RES_n(s) = \frac{K_{p_{RES_n}} \cdot s^2 + K_{p_{RES_n}} \cdot 2 \cdot C \cdot s + (n \cdot \omega_0)^2 + C^2}{(12)}$$
(12)

$$RES_n(s) = \frac{p_{BS_n}}{s^2 + (n \cdot \omega_0)^2}$$
(12)  
PLRES(c) =  $PU(c) + PES(c)$  (13)

 $PI-RES(s) = PI(s) + RES_n(s)$ 

The voltage reference  $v_{dq}$  and both the measured voltage and current ( $v_{dquee}$  and  $i_{dql}$ ) (see Fig. 5) are not filtered (i.e. harmonics are not removed). The PLL described in [2] was used for the synchronization, as it provides disturbance rejection capability. The strategy to synchronize and connect the VSC to a distorted grid is as follows:

1. <u>SW<sup>\*</sup>1=ON</u>, <u>SW<sup>\*</sup>2=ON</u>, <u>Breaker S=open</u>. The PI-RES voltage controller provides the required current command  $i_{dq}^{*}$ (Fig. 5) to the PI-RES current controller to force the same voltage at both sides of the breaker terminals (fundamental and harmonics).

2. <u>SW\*1=OFF, SW2=ON, Breaker S=closed.</u> Once the voltage error is smaller than a certain threshold, the breaker is closed. Following this, the input of the voltage controller is made equal to zero using  $SW_1^*$  (see Fig. 5). By doing this, the voltage loop is disabled, the PI-RES output being locked to the instantaneous value that it has before the breaker closed



(4)

(8)





decreases as the inductance that connects the capacitor filter and the PCC increases. Following, synchronization using the positive sequence component of the fundamental voltage described in Section III are compared, both for the case of a LC filter and an LCL filter.

A. Connection to a distorted utility grid using an LC filter

Fig. 9 shows the simulation results when the positive sequence component of the fundamental voltage is used for synchronization for the case of an LC filter. Fig. 9a shows breaker state (Fig. 7), it is observed in the figure that it closes t=1s. The dq components of the differential voltage between both sides of the breaker terminals (voltage error) are shown in Fig. 9b, while the dq components of the current circulating through the inverter ( $i_{dw}$  in Fig. 7) are shown in Fig. 9c. Fig. 9d show the current that circulates between the filter output and the grid, Fig. 9e shows the detail of this current at the instant the breaker closes. It is observed from Fig. 9d that the differential voltage

It is observed from Fig. 9d that the differential voltage shown in Fig. 9b produces a transient grid current, of peak value of  $\approx$ 14 A, which is several times bigger than the steady state current, its dynamics being given by (8)-(10). The dumped resonance frequency (see Fig. 9e) is  $\approx$ 12.5 kHz, which is in accordance with (6). A current harmonic at 300 Hz (-5th harmonic) exists in steady state (see Fig. 9d), its magnitude being given by (9).



5.996 0.998 1 1002 1.004 1006 (s) Fig. 11.- Simulation results. Same variables, operating conditions and synchronization strategy as in Fig. 9, using an LCL filter. Fig. 10 shows the same simulation results as in Fig. 9 for the proposed method described in Section III. It is observed from Fig. 10b that the differential voltage at the breaker terminals is zero, as both fundamental and harmonic components are considered during the synchronization process. It is observed that with the proposed method, the grid overcurrent in Fig. 9d ( $idq_g$  in Fig. 7) is almost completely cancelled (see Fig. 10d).

B. Connection to a distorted utility grid using an LCL filter

Fig. 11 shows the same simulation test as Fig. 9 but using an LCL filter. It is observed that the overcurrent at the instant that the breaker closes (see Fig. 11e) is smaller than for the LC case, since it is limited by the LCL filter grid-side inductance.

The resonance frequency of the dumped transient response agrees with the predicted one of  $\approx 2.25$  kHz (see Fig. 8 and (6)), being lower than for the LC filter case (see Fig. 8). The higher the inductance between the filter capacitor and the PCC is, the smaller resonance frequency is. Similarly, the higher the inductance between the filter capacitor and the PCC is, the smaller is the transient time constant (5). It can be concluded that smaller connection inductances (transmission line plus filter inductances) results in larger transient overcurrents, but more damped.

3382



3383



Fig. 15 shows the response of the proposed method. The slave VSC uses both the fundamental and the harmonic components of the voltage to feed the synchronization control loop, ideally providing zero differential voltage at the breaker terminals when it closes, (Fig. 15b). As for the simulation results, no overcurrent is observed when the breaker closes (t=1s, Fig. 15d). The injected current harmonics later reduce following the pattern shown in Fig. 6 (Fig. 15c), the grid current harmonics therefore increasing (see Fig. 15c and 14d). It is noted that once the high-order current harmonics are removed (t>1.35s), the inverter only injects the fundamental component of the current.

B. Connection to a distorted utility grid using an LCL filter

Fig. 16 shows the experimental results when the synchronization is realized using the positive sequence component of the fundamental voltage, for the case of an LCL filter. As for the LC filter case, the high-order harmonics in the inverter current that appears at the instant the breaker closes, are compensated by the current regulator (see Fig. 16c). As for the simulation results (Fig. 11c), the peak current is smaller than for the case of the LC filter. The resonance frequency (Fig. 16d) is also smaller as for the LC filter case ( $\approx 2 \text{ Hz}$ ).

Good agreement among the simulation results (see Fig. 13) and the experimental results (see Fig. 16) is observed, differences being due to the line inductances, which have not been considered for the simulation analysis.

Finally, Fig. 17 shows the experimental results using the proposed method for the case of an LCL filter.

b)  $Vd_g$ - $Vd_{\mu g}$  $Vq_g$ - $Vq_{\mu g}$ S c) ldi Iqi Æ d) - Idg - Iqg 3 1.05 1.2 1.25 1.3 1.15 t(s) 1.3 e) - Idg - Iqg Ð 0.994 0.996 1.002

- Breaker



It is observed from Fig. 17b that the differential voltage at the breaker terminals at the instant it closes (t<1) is negligible (it mainly consist of noise). It is observed in Fig. 17c that to match the grid voltage (fundamental+harmonic components), the inverter current contains both fundamental and harmonic components. No overcurrent is observed at the instant the breaker closes (Fig. 17d, t=1), the inverter progressively decreasing later the amount of current harmonics being injected according to the pattern shown in Fig. 6.

It is concluded that the proposed method provides a smooth connection as well as smooth transition to steady state, even for the case of highly distorted voltages at the PCC.

#### VI. CONCLUSIONS

A method for the synchronization and smooth connection of DPGs to distorted networks has been proposed in this paper. The proposed method uses both the positive sequence component of the fundamental voltage as well as the grid voltage harmonics for the synchronization, avoiding transient overcurrents at the instant of connection of the DPG to the utility grid, which might cause unwanted protection tripping, bad aging of the passive elements or power electronics damage.

3384

a)

ON



# A.1.8 Islanding detection in three-phase and singlephase systems using pulsating high frequency signal injection







corresponding single-phase voltage/current and the other component (e.g. *q*-axis in (5) and (6)) is made equal to zero. By doing this, the high frequency impedance (3) in a single-phase system can be estimated from (5) and (6), where  $v_{ady}$  is phase system of the commuter hole (*J*) and (*J*), where  $v_{adf}$  is the injected high frequency phase voltage,  $v_{augebf}$  and  $i_{augeff}$  are the LCL filter high frequency output phase voltage and current respectively and  $i_{adf}$  is the inverter high frequency output the second se output phase current.  $\begin{bmatrix} v_{rec} \end{bmatrix} \begin{bmatrix} v_{rec} \cos(\omega_{rec} t) \end{bmatrix}$ 

$$\begin{split} \mathbf{v}_{abdy} &= \begin{bmatrix} \mathbf{v}_{abg} \\ \mathbf{v}_{abgr} \end{bmatrix} = \begin{bmatrix} \mathbf{v}_{bg} & \mathbf{c}_{b} \mathbf{c}_{bg} \end{bmatrix} = \\ &= \frac{V_{bf}}{2} e^{i \mathbf{m}_{bf}} + \frac{V_{bf}}{2} e^{-i \mathbf{m}_{af}} = \mathbf{v}_{abgf}^{K} + \mathbf{v}_{abgf}^{K} \\ &i_{aggraph} = \begin{bmatrix} i_{aggraph} \\ \mathbf{0} \end{bmatrix} = \begin{bmatrix} \frac{v_{abg}}{2} - i \mathbf{m}_{afg} \\ \mathbf{0} \end{bmatrix} = \begin{bmatrix} \frac{v_{abg}}{2} - i \mathbf{m}_{afg} \\ \mathbf{0} \end{bmatrix} = \\ &= \frac{V_{bf}}{2^{a} [Z_{aggraph}]} e^{(\mathbf{m}_{af} - \mathbf{v}_{afg})} + \frac{V_{bf}}{2^{a} [Z_{aggraph}]} e^{(-\mathbf{m}_{af} - \mathbf{v}_{afg})} = \quad (6) \\ &= i \sum_{aggraph}^{K} + i \sum_{aggraph}^{K} \end{bmatrix}$$

Fig. 4 shows the signal processing needed for islanding Fig. 4 shows the signal processing needed for islanding detection in a single-phase system. A single band-stop filter is needed to reject the component at  $\omega_{M}(BSF1, see Fig. 4)$  to prevent the fundamental current regulator reaction. As for the three-phase system case, band-stop filters *BSF2* and *BSF3* reject the fundamental components and *BSF4* and *BSF3* reject the negative sequence components. Once the positive sequence component of the voltage and current are isolated, the high frequency impedance is obtained using (2) and (3), islanding being detected from the high frequency impedance variation. impedance variation.

impedance variation. It is finally noted that though in all the discussion presented in this paper it is assumed that a high frequency voltage is injected, it is possible to combine high frequency voltage injection and high frequency current injection as described in [9]. These can be advantageous when multiple parallel-connected inverters implement the method [9]. It is also noted that the dead-time effect in PWM single-phase inverters produces a distortion that can be expressed as (7) [19], being therefore possible to use any of the high order harmonics in (7) for islanding detection purposes [19].

$$v_{on} = \frac{4\Delta V}{\pi} \sum_{m=1.5.7} \frac{1}{n} \sin(n\omega_f t)$$

# III. Phase-to-phase and phase-to-ground fault detection using pulsating high frequency signal injection

It has already been mentioned that since islanding in three-phase system occurs simultaneously in all the three phases, it can be readily detected independent of the high frequency signal injection mode, i.e. stationary or rotating. It is noted in this regard that the implementation of the injection in the stationary reference frame is slightly simpler. However, the injection of the high frequency signal in a rotating reference frame opens interesting possibilities for the detection of phase-to-phase and phase-to-ground faults in three-phase systems.

4.pdf

Fig. 5a and 5b show the PCC voltage vector spectrum in Fig. 5a and 5b show the PCC voltage vector spectrum in a rotating reference frame ( $dq_e$  in Fig. 2) and in a stationary reference frame ( $idq_e$  in Fig. 2), when the pulsating high frequency voltage is been superimposed on top of the fundamental excitation. As shown in Fig. 5a, the pulsating high frequency signal can be decomposed in two rotating signals,  $v_{def}^{eq}$  and  $v_{def}^{eq}$  of frequencies  $\omega_{q_e}$  and  $-\omega_{q_e}$  respectively. By transforming this voltage vector to the stationary reference frame (see Fig. 5b), the frequency contained respectively. The most typical asymmetric faults that occur in three-phase systems are the phase-to-ground, phase-to-phase and

phase systems are the phase-to-ground, phase-to-neutral [21]. Typically the neutral wire is not available in the connection of three-phase distributed energy resources to the utility grid/microgrid through three-phase VSI (see Fig. 1a). Therefore, only the phase-to-ground and phase-to-phase faults will be analyzed in this section.

 a) Phase-to-ground fault When a pulsating voltage vector is injected into a three-phase system with a fault to ground in phase a (see Fig. 6a), phase system is phase currents are given by (8). The pulsating signal is injected in a  $dq_e$  reference frame which rotates at  $o_q = 50H_2$  and it is assumed that the fault impedance is much lower than the system (load) impedance  $(Z_L)$ .



a) PCC voltage vector spectrum in a rotating reference framationary reference frame. c) Output inverter current vector sp feeding a non symmetrical lo



5662

a)

(7)

(16)

- \ \ p\_{Z\_{f}} )  $\phi_{ij} + \omega_i (t + \phi_{Z_L})$  $V_b\sqrt{3}$ +5°π/6+ø-.)  $\frac{T_{b} \sqrt{3}}{Z_{L}}$   $\frac{V_{c} \sqrt{3}}{\sqrt{3}}$  $\dot{i}_a \\ \dot{i}_b \\ \dot{i}_c$  $Z_F$  $V_a$ Z (8) (8) Applying Fortescue's theorem, (9), to the components in (8) at  $\omega_{i,i} + \omega_{i,j}$ , a set of symmetrical components is obtained (10), with  $\hat{\mu}_{abox}$ ,  $\hat{\mu}_{abox}^{m}$ , and  $\hat{\mu}_{abox}$ , being the zero, positive and negative sequence components respectively. It is noted that though the same transformation could be used with the components in (9) at  $-\omega_{i,i} + \omega_{i,j}$ , the discussion following formers only for the formation ensure around each of the 10 set.  $i_{daht}^{pc}$ focuses only for the frequency components at  $\omega_{bj} + \omega_i$ .  $\begin{bmatrix} i_a \end{bmatrix}$  $i_b$  $i_c$ (9) (10) $\sqrt{3}{\sqrt{3}}$  $i_{da}^{nc}$ where  $I = V \sqrt{3}/Z$ . where  $T_{cc} = v_{\beta} \otimes j_{\ell - L_{cc}}$ . If the fault occurs in phase *b*, the resulting symmetrical components using (9) are given by (11), while if the fault occurs in phase *c* it is expressed by (12). It is observed from where occurs in phase c it is expressed by (12). It is observed from (10)-(12) that the faulty phase can be detected from the phase angle between the positive sequence component ( $i_{holpe}^{rec}$ ), which is 0 when the faulty phase is phase  $a, 2\pi/3$  when the faulty phase is phase b and  $4\pi/3$  when the faulty phase is phase c. 0  $2\sqrt{3}$  $(\phi_i)t - \phi_{ZL}$ i<sup>pc</sup> idqhfpc (11)  $\sqrt{3}$ 2√3  $i^0_{dqhfpc}$  $i^{pc}_{dqhfpc}$  $i^{nc}_{dqhfpc}$ (12)  $\sqrt{3}$ b) Phase-to-phase fault When a pulsating voltage vector which rotates at  $\omega_i$ , is When a puisating voitage vector which rotates at  $\omega_r$ , is injected into a three-phase system in which a phase-to-phase fault between phases *a*-*b* occurs (see Fig. 6b), the resulting phase currents are expressed by (13) and the resulting symmetrical components are given by (14) (only the phasors for the frequency components at  $\omega_{uf} + \omega_r$  are shown). It is assumed that the fault impedance ( $Z_F$ ) is much lower than the local immediate ( $Z_F$ ). the load impedance  $(Z_L)$ . The resulting symmetrical components when the fault occurs between phases b-c or c-a are given by (15)-(16). It is observed by comparing (14)-(16) that the faulty phases 5663

can be detected from the phase angle between  $l^{\mu\nu}_{abg}$  and  $l^{\nu\nu}_{abg}$ . Le.  $\pi/3$  when the fault occurs between phases *a* and *b*,  $\pi$  when the fault occurs between phases *b* and *c* and  $-\pi/3$  when the fault occurs between phases *a* and *c*.  $\frac{V_{ab}}{2}e^{j\left(\left(\omega_{kf}+\omega_{i}\right)t-\pi/6-\varphi_{Z_{F}}\right)}$  $\frac{V_{ab}}{Z_F} e^{j\left((-\omega_{kf}+\omega_i)t+\pi/6+\varphi_{Z_F}\right)}$  $\frac{V_a}{Z_a}$ 0..) 5+0-.) 0 (13) √3 (14) (15)

 $|Z_{\varepsilon}|$ 



Inverter Load1

Fig. 5. Simulation scenario for both three and single-phase system Fig. 5. simulation scenario for both three and single-phase systems Fig. 5 shows the scenario used to simulate the proposed islanding and fault detection methods. The same scenario was used for both single-phase and three-phase cases, the corresponding inverter topologies being shown in Fig. 1. The simulation parameters are shown in Table I.

	Table I		
	Three phase		
Grid	Inverter	Load	Line
380V, 50 Hz, rg/Xg	=0.1,380V,	3 kW	R=11.7mOhm
S <sub>cc</sub> =15MVA	10kHz		L=8.68e-4H
	Single phase		
Grid	Inverter	Load	Line
220V, 50 Hz, rg/Xg	=0.1,220V,	1 kW	R=11.7mOhm
S = 5MVA	10kHz		I = 8.68e - 4H

Figure 30 VA [10472]






### A.1.9 Quadrature Signal Generator based on All-Pass Filter for Single-Phase Synchronization





(11)

filter is shown in (1). Its main feature is that it provides unit gain for all frequencies (2) and the phase response is given by (3). At the  $\omega_q$  frequency, often referred as the corner frequency, the all-pass filter shifts 90 degrees the input signal.

$$APF_{q}(s) = \frac{s - \omega_{q}}{s + \omega_{q}} \tag{1}$$

$$APF_{q}(\omega) = 1 \tag{2}$$

$$\angle APF_{q}(\omega) = \phi_{\underline{OSG}} = 180 - 2\arctan\left(\frac{\omega}{\omega_{q}}\right)$$
(3)

Fig. 3 shows the APF frequency response function when  $\omega_a$  equals the fundamental component (e.g. 50 Hz), it is observed that there is a 90 degrees phase shift at the fundamental frequency. The phase angle for the higher order harmonics is given by (3). It is clear from (3) that errors in the phase angle of the quadrature component will occur if the actual grid frequency is different from the  $\omega_q$  in (1). A real time estimation of the corner frequency is therefore required. The frequency estimated by the PLL  $\hat{\omega}_v$  (see Fig. 2) will be used for this purpose.



b) Frequency (112) Fig. 3- a) Magnitude and b) phase of the frequency response function of an APF

### B. Three-phase ATO

This subsection presents the three-phase ATO used in this paper. For discussion purposes, it will be first assumed that the QSG input signal (4) (v' in Fig. 2), consists of the fundamental component and a harmonic component of order n, where  $\theta_l$  and  $\theta_n$  are the phases of the fundamental component and the  $n^{th}$  harmonic respectively. It is also assumed that the QSG corner frequency matches the fundamental frequency. Thus the QSG output and the fundamental frequency. Thus the QSG output and the fundamental frequency. Thus the APF-QSG output is shifted  $\Phi_{QSG}$  degrees (3) respect to the input.  $u_{\alpha\beta}$  complex voltage vector is given by (5).  $v' = U_1 \cos(\omega_0 t - \theta_1) + U_n \cos(m\omega_0 t - \theta_n)$  (4)

$$v'_{q} = U_{1}\cos(\omega_{0}t - \theta_{1} - \frac{\pi}{2}) + U_{n}\cos(n\omega_{0}t - \theta_{n} - \phi_{QSG})$$
 (5)

$$u_{\alpha\beta} = \alpha + j\beta = v' + jv'_{q}$$
(6)

$$u_{\alpha\beta} = U_1 \cdot e^{j\omega_0 t} + U'_{-n} \cdot e^{jn\cdot\omega_0 t} + U'_n \cdot e^{-jn\cdot\omega_0 t}$$
(7)

Assuming  $\theta_I = \theta_n = \theta$ , the resulting  $u_{\alpha\beta}$  voltage complex vector consist of three components (7): a component rotating at the fundamental frequency of magnitude of  $U_I$  and two

3.pdf

components rotating at  $-n\omega_{\theta}$  and  $n\omega_{\theta}$  respectively, their magnitudes depending on  $\Phi_{0SG}$  since the QSG creates a harmonic component that is not in quadrature with the harmonic input (3) (see Fig. 2b).

An ATO is used to estimate the frequency and phase of the fundamental component  $(U_I)$  [13]. The error signal (8) (see Fig. 3) is obtained as the vector cross-product between the input signal  $(u_{ad})$  and the estimated unitary vector  $(e^{t\hat{\psi}_i})$ , whose phase is the estimated phase of the input signal. The error signal  $(\varepsilon_a)$  is normalized by using the estimated fundamental voltage magnitude  $(\hat{U}_I)$ , therefore making the phase error independent of the input magnitude. Assuming perfect tracking of the fundamental component, i.e.  $\hat{\phi}'_i = \omega_d I$ , the phase error consists of two harmonic components of orders  $n \pm I$ . It is noted that if the QSG input signal, v', contains more than one harmonic component, each input harmonic of order n will produce two harmonics of order  $n \pm I$  in the phase error signal.

$$\begin{split} \varepsilon_{\phi} &= \frac{u_{\alpha\beta} \otimes e^{i\phi_{v}^{i}}}{\dot{U}_{1}} = \frac{\operatorname{Re}\left\{u_{\alpha\beta}\right\} \cdot \sin\left(\hat{\phi}_{v}^{i}\right) - \operatorname{Im}\left\{u_{\alpha\beta}\right\} \cdot \cos\left(\hat{\phi}_{v}^{i}\right)}{\dot{U}_{1}} = \\ &= \frac{\sin(\hat{\phi}_{v}^{i})}{\dot{U}_{1}} \left[U_{1}\cos(\omega_{0}\cdot t) + U_{n}\cos\left(n\cdot\omega_{0}\cdot t\right)\right] - \\ &- \frac{\cos(\hat{\phi}_{v}^{i})}{\dot{U}_{1}} \left[U_{1}\sin(\omega_{0}\cdot t) + U_{n}\cos\left(n\cdot\omega_{0}\cdot t - \phi_{\cos\beta}\right)\right] \\ &\varepsilon_{\phi} &= \frac{U_{n}}{\dot{U}_{1}\cdot 2} \left[\sin\left((n+1)\cdot\omega_{0}\cdot t\right) - \sin\left((n-1)\cdot\omega_{0}\cdot t\right) - \\ \end{split}$$
(8)

$$-\cos((n+1) \cdot \omega_0 \cdot t - \phi_{QSG}) - \cos((n-1) \cdot \omega_0 \cdot t - \phi_{QSG})] \qquad (9)$$

$$\hat{U} = u_{\alpha\beta} \cdot e^{j\phi'_{\epsilon}} = \operatorname{Re} \{u_{\alpha\beta}\} \cdot \cos(\hat{\phi}'_{\epsilon}) + \operatorname{Im} \{u_{\alpha\beta}\} \cdot \sin(\hat{\phi}'_{\epsilon}) \qquad (10)$$

$$\hat{U} = U_1 + \frac{U_n}{2} \Big[ \cos\left((\mathbf{n}+1) \cdot \boldsymbol{\omega}_0 \cdot t\right) + \cos\left((\mathbf{n}-1) \cdot \boldsymbol{\omega}_0 \cdot t\right) + \frac{U_n}{2} \Big]$$

$$+\sin\left((n+1)\cdot\boldsymbol{\omega}_{0}\cdot\boldsymbol{t}-\boldsymbol{\phi}_{QSG}\right)-\sin\left((n-1)\cdot\boldsymbol{\omega}_{0}\cdot\boldsymbol{t}-\boldsymbol{\phi}_{QSG}\right)\right]$$

To estimate the magnitude of the fundamental voltage component ( $\hat{U}$  in Fig. 2), a scalar product between the grid voltage  $u_{a\beta}$  and the unit vector  $e^{j\vec{n}_{i}}$  is used (10) (see Fig. 2). The estimated magnitude,  $\hat{U}$ , consists of a DC component, whose magnitude is equal to the magnitude of the fundamental component of the grid voltage ( $U_{I}$ ) and two harmonic components of orders  $n\pm 1$ . If the input voltage consists of more than one frequency component, each harmonic of order n will produce two harmonics of order  $n\pm 1$  in the estimated magnitude. Since the harmonic components will be removed by the PFS discussed following, low-pass filters (LPF) would only be required to remove noise coming from the sensors and electronics

### C. Pre-Filter Stage (PFS)

A potential mechanism for harmonic rejection in the proposed method is to reduce the ATO PI controller bandwidth. However, this solution is unsatisfactory as the microgenerator stability relies on the ATO dynamic response.

In addition, the output APF-QSG quadrature signal depends on the estimated ATO frequency. Therefore, the implementation of a specific mechanism to remove the harmonic content from the input voltage is advisable. Two different approaches are typically used for harmonic

rejection: a pre-filter stage [14] or a filter within the PLL loop [13]. Being N the number of harmonics to be removed, a prefilter stage configuration requires N notch filters while the filter in the PLL loop configuration requires 2(N+1) filters. Therefore, a pre-filter configuration will be used as it is advantageous in this regards and.

Selection of the number of notch filters to be used can be made based on power quality standards. The international standards for grid-connected power converters [5]-[6] limit the maximum overall voltage harmonic distortion (THD) to 5%, maximum overall voltage namionic distortion (11D) to 5%, with each individual harmonic magnitude being smaller than 4% for harmonic orders lower than 11<sup>th</sup>, 2% for harmonic orders between 11<sup>th</sup> and 17<sup>th</sup>, 1.5% for harmonic orders between 17<sup>th</sup> and 23<sup>rd</sup>, 0.6% for harmonic orders between 23<sup>rd</sup> and 35<sup>th</sup> and 0.3% for orders higher than 35<sup>th</sup>. Three notch for (120 Min 2017) for 0.2% of the form of the form (120 Min 2017). filters (12), corresponding to  $\omega_3 = 3 \omega_{\theta} (150 \text{ Hz}), \omega_5 = 5 \omega_{\theta} (250 \text{ Hz})$  and  $\omega_7 = 7 \omega_{\theta} (350 \text{ Hz})$ , will be implemented in this work [13]

$$NF_{\omega_n}(z) = b \frac{1 - 2 \cdot \cos(\omega_n) z^{-1} + z^{-2}}{1 - 2 \cdot b \cdot \cos(\omega_n) z^{-1} + (2 \cdot b - 1) z^{-2}}$$
(12)

$$\omega_{n}^{\prime} = \frac{2}{T_{s}} \cdot \tan\left(\omega_{n} \cdot \frac{T_{s}}{2}\right); \omega_{n} = \frac{n \cdot \omega_{0}}{f_{s}/2}$$

$$b = \frac{1}{1 + 1}$$
(13)

(15)

(18)

$$\beta = \frac{\sqrt{1 - A^2}}{A} \tan\left(\frac{BW}{2}\right); BW = \frac{\Delta\omega}{f/2}$$

D. Phase Delay Compensator (PDC)

The delay introduced by the filtering stage discussed previously can adversely impact the performance of the method, implementation of a phase delay compensation strategy being therefore advisable. The phase delay is estimated from the filter transfer function (12) in real time and later compensated (see Fig. 2). Substituting (16) into the notch filter transfer function, (12) is obtained. By separating the numerator and denominator of the filter transfer function into their real and imaginary components, (17), the notch filter phase delay D at the grid frequency is obtained using (18).  $z = e^{j\hat{\omega}_{i}T_{s}} = \cos(\hat{\omega}_{i}T_{s}) + j \cdot \sin(\hat{\omega}_{i}T_{s})$ (16)

$$NF_{\omega_s} = \frac{real(num) + j \cdot imag(num)}{real(den) + j \cdot imag(den)}$$
(17)

$$D = \tan^{-1} \left( \frac{imag(num)}{real(num)} \right) - \tan^{-1} \left( \frac{imag(den)}{real(den)} \right)$$

4.pdf

III. SIMULATION ANALYSIS UNDER GRID DISTORTED CONDITIONS

Fig. 4 and Table I show the configuration used for the

simulation of the proposed method. A programmable AC source is used to produce different disturbances in the grid voltage, including 1) grid voltage magnitude deviations, 2) grid frequency deviations and 3) harmonics. As already mentioned, the pre-filter stage was designed to reject the 3<sup>rd</sup>, 5th and 7th harmonics, the magnitude of the disturbances have been selected to comply with the grid codes [5]-[6]. In the simulation and experimental results following,

magnitudes and frequencies are shown in per unit relative to the rated grid voltage and frequency (i.e. 220 V and 50 Hz).

Fig. 5 shows the simulation results when the AC source produces a step-like change in the output voltage magnitude. Fig. 5a shows both the grid voltage ( $v_g$  in Fig. 4) (black) and the voltage estimated by the proposed method ( $v_{\mu g}$  in Fig. 4) (red). Figs. 6b-6d show the magnitude, frequency and phase error. It is observed form Fig. 5b that the maximum magnitude error is 0.055 p.u., being below 0.03 p.u. in around 5 ms. Also, a maximum error in the estimated frequency of  $\approx$ 0.05 p.u. is observed (see Fig. 5c), which is compensated by the ATO PI controller after 5 ms. Finally, the maximum transient phase error is  $\approx 2$  degrees (Fig. 5d) which is also compensated by the ATO in less than 5 ms



Symbol	Description	Value
Li	Inverter side filter inductance	2.196 mH
$R_i$	Inverter side filter resistance	0.05 Ω
С	Capacitor Filter	10 µF
$R_c$	Capacitor ESR	0.0536 Ω
Lg	Grid side filter inductance	1.3 mH
$R_{q}$	Grid side filter resistance	0.05 Ω
	Positive sequence voltage magnitude (rms)	230 V
$\Delta \omega$	Notch Filter bandwidth	10 Hz
	Magnitude low-pass filter bandwidth	1000 Hz
$K_p$	ATO proportional gain	100
Ki	ATO integral gain	5000

Figs. 7 and 8 show the simulation results for the case of a

step-like frequency change. Fig. 6 shows the performance of the proposed QSG and PDC blocks. Fig. 6a shows the input and output signals to the QSG block, a 90 degrees phase shift between  $v'_q$  and v' is observed, independently of the input

signal frequency Fig. 6b shows the phase shifts obtained by the PDC block for each notch filter and the total phase delay. The phase

shifts agree with the theoretical ones given by (18). observed that the resulting phase delay is frequency-dependent





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Fig. 9a shows the estimated grid voltage, the effects due to the harmonics injected by the AC source being totally eliminated. Fig. 9b shows the amplitude of the error between the fundamental component of the grid voltage  $v_g$  and the estimated voltage  $v_{gg}$ . The error is due to the transient response of the PFS used to remove the grid disturbances. It has a maximum value of 0.18 pu, and is removed by the PFS after 50 ms. A similar behavior is observed for the frequency error (Fig. 9c), the maximum frequency error being 0.05 pu. Finally, the maximum transient phase error is smaller than 1 deg. (see Fig. 9d), being completely removed after 50 ms.

### IV. EXPERIMENTAL RESULTS

Fig. 10 and Table I show the experimental setup configuration and parameters. It consists of two single-phase voltage source converters (Master and Slave in Fig. 10). The master inverter is used to emulate a programmable AC source (see Fig. 4) meanwhile the slave inverter implements the proposed single-phase synchronization method. Both master and slave inverters are 50 kW inverters feeding each one a local resistive load of  $30 \,\Omega$ . The same tests used in simulation were performed experimentally.

Fig. 11 shows the experimental results when the grid voltage magnitude changes. The PCC voltages are shown in Fig. 11a, the magnitude, frequency and phase errors between the  $v_g$  and  $v_{qg}$  being shown in Fig. 9b, 10c and 10d respectively.



It is observed in Fig. 11a that the proposed method shows an excellent performance tracking the magnitude change. The magnitude error (Fig. 11b) has a peak value of  $\approx 0.08$  pu, being compensated after  $\approx 20$  ms. Frequency (Fig. 11c) and phase (Fig. 11d) errors are negligible. The differences between simulation (Fig. 5) and experimental (Fig. 11) results are due to the fact that the inverter used to produce the disturbances in the experimental set up implements voltage and current control loops, what limits the bandwidth producing the disturbances.

Fig. 12 shows the experimental results when a frequency step-like change of the grid voltage occurs. Fig. 12a shows the actual and estimated voltage. A small peak magnitude error (i.e. <<0.01 pu) is observed (Fig. 12b) at the instant the grid frequency changes, the peak grid frequency error being <<0.05 pu. Both errors are corrected after  $\approx10$  ms by the PLL-ATO.

A negligible phase error is observed in Fig. 12d. Again the differences between the simulation and experimental results are due to the control bandwidth of the master inverter. It is noted in this regards that in a real scenario the grid frequency does not change instantly due to the inertia of the power generators.





# A.2 Peer-reviewed journal publications

### A.2.1 Active Islanding Detection Using High Frequency Signal Injection



#### DÍAZ REIGOSA et al.: ACTIVE ISLANDING DETECTION USING HIGH-FREQUENCY SIGNAL INJECTION

need of a communication system between the DG and the utility grid.

A new active method for islanding detection based on the injection of high-frequency signal voltage is proposed in this paper. Advantages of the method are almost negligible adverse effects due to the injected high-frequency voltage, as well as accurate and fast islanding detection. The proposed method is suitable for the case when the inverter operates alone and for the case when several inverters are connected in parallel. It is however required that the switching frequency is high enough to enable the injection of a voltage signal in a range of a few hundred of hertz. This paper is organized as follows: Section II briefly discusses active islanding-detection methods; Section II briefly discusses active islanding-detection methods; the physical principles and the analytical formulation of the proposed method are presented in Sections III and IV, respectively. Simulation results are presented in Section V. The discussion of implementation issues is presented in Section VI; experimental results demonstrating the viability of the proposed method are presented in Section VII.

II. ISLANDING DETECTION USING ACTIVE METHODS

This section reviews active islanding-detection methods found in the literature.

 Impedance Estimation Methods: The motivation for these methods is the requirements established by the standards for islanding detection [13], [14], [24], [25]. Active methods can be divided into two groups, i.e., transient active methods and steady-state active methods.

In transient active methods, an impedance measuring device [9] produces a short disturbing signal (normally a voltage), e.g., impulse-like, and analyzes the grid response (normally in the current) The advantage of these techniques is that the grid can be excited over a large frequency range, significantly improving the accuracy and the reliability of the measurements.

Steady-state active methods inject a harmonic (periodic) component [9]-[11], [27]. In the method proposed in [10], a high-frequency signal (400-600 Hz) is injected at the instant of zero crossing of the fundamental excitation voltage at the point of common coupling (PCC); the impedance being estimated from the measured voltages and currents using the discrete Fourier transform [10]. A limitation of this method is that, since the signal is injected at the instant of zero crossing of the grid voltage, the islanding condition can be only detected at that point. Also, additional current sensors are needed at the PCC to measure the high-frequency current. An extension of the method in [10] was presented in [12], for the case of multiple inverters working in parallel for PV applications. The extended method proposes the coordinated injection of a noncharacteristic (i.e., not present during normal operation of the grid) harmonic (75 Hz). Previous to the injection of this harmonic, each PV inverter checks if it is already present in the grid and, for this case, will wait a few cycles of the fundamental voltage wave before checking again to prevent interference with other PV inverters [12]. One limitation of this technique is that two or more inverters could simultaneously start the check-and-inject procedure; interference and consequently incorrect islanding detection could occur. The probability of interference

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increases with the number of PV inverters connected to the grid. In addition, the interharmonic signal (75 Hz) could interact with the fundamental current/voltage controls (50 Hz) due to the small spectral separation.

2) Grid Variable Variation Methods: In these methods, the DG produces a small disturbance in a grid variable. If the DG is connected to the grid, the disturbance will be corrected by the grid, whereas if it is in islanding operation, the disturbance will remain. The variables commonly selected for islanding detection are the frequency [2], [15] and the voltage [2], [15] at the PCC.

While active methods are appealing due to their reduced NDZ, the disturbance introduced in the grid can be a concern, particularly when a large number of inverters are connected to the same PCC and interferences can occur. To prevent these adverse effects, the use of a high-frequency small-magnitude periodic signal is proposed. The principles of the method are discussed in the following.

### III. ISLANDING DETECTION USING HIGH-FREQUENCY SIGNAL INJECTION

It has been already shown that the high-frequency impedance is a reliable metric to detect an islanding situation [9]-[12]. Voltage-source inverters (VSIs) present in the microgrid [e.g., in controlled rectifiers used in active power filters (APFs), back-to-back power converters, etc.] can easily inject a low-magnitude high-frequency voltage from which the highfrequency impedance is measured. While a variety of forms of high-frequency excitation can be used, particularly simple and reliable implantations obtained by injecting either a rotating or pulsating voltage vector, both options are discussed in the followine.

### A. Rotating High-Frequency Signal Injection

When a three-phase linear system is exited with (1), the induced high-frequency current is given by (3), the high-frequency impedance at the excitation frequency being (4), with its phase angle being (5), i.e.,

$v_{dqhf} = V_{hf}e^{j\omega_{hf}t}$	(1)
$v_{dqhf} = v_{dhf} + jv_{qhf} = 2/3(v_a + v_b e^{j2pi/3} + v_c e^{j4pi/3})$	(2)
$i_{dqhf} = V_{hf}/Z_{dqhf}e^{j(\omega_{hf}t-\varphi_Z)}$	(3)
$Z_{dqhf} = R_{hf} + j\omega_{hf}L_{hf} = \frac{v_{dqhf}}{i_{dqhf}}$	(4)
$\omega_{Z} = a \tan \left( \omega_{h,\ell} L_{h,\ell} / R_{h,\ell} \right)^{-1}$	(5)

where  $\omega_{hf}$  is the frequency of the injected signal,  $V_{hf}$  is the voltage magnitude of the injected high-frequency signal,  $i_{dqhf}$  is the induced high-frequency current,  $Z_{dqhf}$  is the highfrequency impedance,  $\varphi_Z$  is the phase of the high-frequency impedance of the three-phase system, and  $R_{hf}$  and  $L_{hf}$  are the high-frequency resistance and inductance, respectively.

One important issue that needs to be considered is the effect of the output filter of the VSI on the estimated high-frequency impedance. Fig. 1 shows the classical architecture













Fig. 14. Estimated (a) magnitude and (b) phase of the high-frequency impedance. (c) Commanded magnitude of (blue)  $v_{dqh_{f1}}$ , (red)  $v_{dqh_{f2}}$ , and (green) measured  $v_{dqh_{f2}}$  magnitude by inverter 2. (d) (blue) Measured  $i_{dqh_{f2}}$  by inverter 2. When master inverter and (green) measured  $i_{dqh_{f2}}$  by inverter 2.  $V_{hf1} = 1.5$  V,  $\omega_{hf1} = -333$  Hz,  $V_{hf2} = 1.5$  V, and  $\omega_{hf2} = 303$  Hz.

continuous injection is 0.11%, the average THD increase with intermittent injection would be as low as 0.0014% but with an instantaneous value of 0.11% when the high-frequency voltage is being injected.

Fig. 14(a) and (b) shows the estimated high-frequency impedance magnitude and phase in a transition from grid connected (t = 8) to island situation and from island situation (t = 12) to grid connected. Fig. 14(c) shows the commanded magnitude of  $v_{dqhf1}$  when it is continuously injected for islanddetection purposes, as well as the magnitude of the highfrequency voltage  $v_{dqhf2}$ , which is injected only by the master inverter when island situation is detected, to forward the island condition to other inverters connected to the microgrid (see Fig. 8). It is noted by comparing Fig. 14(a)-(c) that there is a slight delay between the transition either from grid connected to island or from island to grid connected and the injection of v<sub>dqh f2</sub>. This is due to the use of a threshold for the detection of islanding or grid connected condition. This threshold needs to be established for the variable being used for islanding detection, i.e., the magnitude or the phase of the high-frequency impedance. The magnitude of the high-frequency impedance has been used for the experimental results shown at Fig. 14. The threshold could be set to be in the middle of the high-frequency

#### impedance for island and grid-connected operations. However, this option might not be accomplished in practice with the islanding-detection standards [13], [24], [25], which require the detection of grid impedance magnitude changes within a certain period of time. Instead, the threshold is selected based on the magnitude changes established by the standards; a hysteresis is included to make the method robust against false alarms [see Fig. 14(a)].

In addition to the use of a threshold, it was found convenient to establish a minimum time, such that, only when the signal used for islanding detection surpasses the threshold for a time longer than the established minimum time, the detection of the island/grid condition is fully effective. The selection of an adequate minimum time will depend on several factors such as noise or transient behavior of the microgrid loads. The minimum time for the experiments carrier out for this paper has been established in 200 ms (see Fig. 14). However, this is an ad hoc selection; a deeper analysis of this issue is the subject of future research.

Fig. 14(c) and (d) shows the magnitude of  $v_{dqhf2}$  and  $i_{dqhf2}$  that are measured by inverter 2. Both signals can be used by inverter 2 to detect the island condition.

Finally, the computational requirements of the proposed method are of 8.2  $\mu$ s in the signal processor used in the experimental setup. This computational burden makes it feasible to implement the proposed algorithms in already existing digital signal processors.

### VIII. CONCLUSION

An active method based on the injection of a high-frequency signal for islanding detection of microgrids has been presented. The islanding detection has been based on the variation of the measured high-frequency impedance, which has been obtained from the estimated output current and the measured output voltage of the LCL filter using complex-vector filters. The injection of the high-frequency signal can be performed by any VSI connected to the microgrid. It has been shown that a high-frequency voltage of 0.3% of the line voltage is enough for reliable islanding detection, which results in a THD increase of as small as  $\approx 0.11\%$ , not therefore compromising the microgrid meeting the standards. The use of a secondary high-frequency signal has been shown to be a feasible solution to prevent interferences when more than one power converter is connected to the microgrid, therefore making the method suitable for parallel connected inverters. Positive and negative sequence high-frequency signals, relative to the fundamental frequency, have been selected for both islanding detection and communication. This increases the spectral separation with the components at the fundamental frequency and its harmonics, making the filtering process easier and improving the accuracy of the method. Experimental results have been provided to demonstrate the viability of the method.

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DÍAZ REIGOSA et al.: ACTIVE ISLANDING DETECTION USING HIGH-FREQUENCY SIGNAL INJECTION



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# A.2.2 Active Islanding Detection for Multiple Parallel-Connected Inverter-Based Distributed Generators Using High-Frequency Signal Injection



### REIGOSA et al.: ACTIVE ISLANDING DETECTION FOR MULTIPLE PARALLEL-CONNECTED INVERTER-BASED

signal voltage, and the rest of (slave) inverters in the grid use this signal to detect islanding. Assignation of the master role can be done statically (a particular inverter is always the master) or dynamically (the master inverter is chosen among the inverters active in the network, based on some criteria, e.g., the proximity to the point of common coupling). However, both solutions present problems. Failure of the master inverter for the case of a static assignment would leave the grid without the high-frequency signal voltage, the rest of inverters in the grid hence losing their capability to detect islanding. On the other hand, dynamic selection of the master inverter might require the use of communications, communication breakdown becoming therefore a concern.

This paper proposes a method for islanding detection using high-frequency signal injection in grids with multiple parallelconnected inverters. In the proposed method, inverters dynamically respond to changes in the grid (e.g., failure of the master inverter, change from island to grid-connected, or from gridconnected to island, and so on) automatically reassigning the master–slave roles, without the need of communications. To coordinate the actions of the inverters present in the grid, the proposed method implements two distinguishing features.

- The slave inverters work in a high-frequency current cancellation mode. This mode of operation prevents the reaction of the slave inverters against the high-frequency signal voltage injected by the master, still keeping full capability of fast and accurate islanding detection.
- 2) In the case of master failure, or significant changes in the grid, the remaining inverters will dynamically reassign roles, the new master inverter being self-selected based on a deterministic performance criteria and without the need of communication.

The paper is organized as follows. Section II presents a review of active islanding detection-based methods. Section III presents the physical principles of the proposed islanding detection method based on high-frequency current cancellation strategy, while Section IV presents the proposed method for dynamic master roll assignment. Discussion of implementation issues is presented in Section V. Finally, experimental results to demonstrate the viability of the proposed method are presented in Section VI.

II. ISLANDING DETECTION USING ACTIVE METHODS

Active islanding detection methods measure the reaction of the grid to a small disturbance or test signal [1]–[12]. Active islanding detection methods can be divided in two groups.

A. Grid Variable Variation Methods

In these methods, the DG produces small disturbance in a grid variable (e.g., voltage or frequency). The disturbance will normally have no measurable impact for the case of grid-connected operation, while it will be measurable for the case of island condition, the grid/islanding condition being therefore obtained from the grid/microgrid response [13].

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### B. Impedance Estimation-Based Methods

These methods can be divided into grid impedance estimation by active and reactive power variation [14] and methods using harmonic signal injection [15]–[19].

Active and reactive power variation-based methods produce periodic variations of the converter output active and reactive power. This produces variations of the output current and voltage, from which the grid impedance is estimated [14].

Harmonic signal injection methods use some form of highfrequency excitation and can be further classified into two groups.

- Intermittent signal injection-based methods [15]–[18]. The signal is injected normally at the instant of zero crossing of the grid voltage, which implies that the islanding situation can only be detected at that instant of time. The frequency of the signal used in [15]–[17] was 75 Hz and in [18] 400–600 Hz.
- 2) Continuous signal injection-based methods [19]. These methods allow almost instantaneous detection of the island/grid-connected condition [19], but this is achieved at the price of an increase of the THD [1]-[11]. In [19], a high-frequency voltage as small as 0.3% of the line voltage, with a frequency of 300-400 Hz, allowed reliable islanding detection, without compromising the THD restrictions.

Generally speaking, potential concerns for active methods are that they could negatively impact the power quality in grids with large penetration of inverter-based DG. In addition, interference problems among converters can occur if several DG's are connected in parallel to the same PCC, what might result eventually in an increase of the NDZ [13].

III. ISLANDING DETECTION USING HIGH-FREQUENCY VOLTAGE INJECTION AND HIGH-FREQUENCY CURRENT CANCELLATION

It has already been shown that islanding detection in inverterbased DG can be done by measuring the grid response to a high-frequency signal voltage [19]. While the implementation of this method is relatively simple when there is a master inverter responsible of injecting the high-frequency signal (see Fig. 1), interferences can occur if multiple inverters connected in parallel do the same, strategies to prevent from this to happen being needed in this case [15], [19]. The coordinated injection of a noncharacteristic harmonic (75 Hz) was proposed in [15], each inverter checking if this harmonic is present in the grid before





proposed strategy is described for current regulated VSI inverters using an LCL filter, it can also be implemented on inverters using other filter designs like inductive filters. To evaluate the proposed method, a scenario with three

parallel-connected converters (a master and two slave inverters), has been built as an example (see Fig. 4). The simula-tion parameters are summarized in Table I. Fig. 5 shows the simulation results. The master inverter continuously injects the high-frequency voltage ( $v_{dqhf1}$ , see Table I), the estimated magnitude and phase of the high-frequency impedance being shown in Fig. 5(a) and (b), respectively. Transition from island to grid-connected and form grid-connected to island occur at t = 3.5 s and t = 5.5 s, respectively. It is observed from Fig. 5(a) and (b) that the changes in the magnitude and phase of the high-frequency impedance allow reliable island/grid-connected detection [19].

Fig. 5(c) shows the magnitude of the high-frequency current regulator output voltage ( $|v_{dqhf}^*|$ , see Fig. 3) for the two slave inverters (inverters 1 and 2 in Fig. 4). It can be observed that the high-frequency voltage dramatically decreases when the mi-crogrid becomes connected to the main grid. This is due to the variation of the high-frequency impedance between island and

grid connected condition. While in island condition the overall microgrid high-frequency impedance corresponds to the local loads, and can be relatively large, in grid connected condition the overall high-frequency impedance is dominated by the grid impedance, which is normally significantly smaller [13].

This high-frequency impedance change produces a variation of the high-frequency current regulator output voltage, which is used by the slave inverters to detect the islanding/grid-connected condition. This is done without the need of a secondary highfrequency signal for communication purposes [19] and without interfering with the master inverter operation.

It is noted that a threshold for the high-frequency current regulator output voltage magnitude needs to be set to detect the transition between islanding and grid-connected operation. This threshold might depend on the microgrid/grid architectures, microgrid/grid high-frequency impedances, or grid pollution. As for the islanding detection THD-based methods [13], [19], [20] or the voltage harmonic monitoring-based methods [21], the

selection of the threshold is not always easy and might require a previous knowledge of the microgrid/grid characteristic.

IV. DYNAMIC MASTER ROLE ASSIGNMENT

One concern of methods in which a master inverter is responsible on injecting the high-frequency voltage is the risk of a master inverter failure [19]. This will leave the grid/microgrid without the high-frequency signal, the slave inverters therefore losing their islanding detection capability. Furthermore, even in the event that the master inverter does not fail, changes in the grid/microgrid topology, e.g., switching between islanding and grid connected operation, connection/disconnection of other inverters, generation units, loads, etc., might have a significant impact in the high-frequency signal *seen* by the inverters con-nected to the microgrid, eventually affecting to the performance of the method. For example, during grid-connected operation several inverters might be working like masters, due to the low grid impedance, while during islanding, it is likely that one single master inverter might be enough to supply a high-frequency signal voltage visible to all the inverters connected to the microgrid. Hence, in the event of switching from grid connected to islanding, all the master inverters but one could likely safely switch to the slave mode. It is concluded that some mechanism for the dynamic reassignment of the master/slave roles is convenient. Using communications or some type or preconfiguration of the master/slave inverters for this purpose is considered unappealing. A strategy for the dynamic reassignment of the master role is proposed in this paper. It is accomplished in three steps. 1) Detection by the inverters of changes in the microgrid.

Detection by the interfers of changes in the interferguscale changes can be of three types: 1) the master inverter detects a sudden variation of the high-frequency impedance; 2) the slave inverters detect that no highfrequency voltage is present in the grid. This can be due to either the failure of the master inverter, or to a significant decrease of the grid impedance (e.g., due to a change from island to grid connected operation); and 3) the slave inverters detect a sudden increase of the high-frequency voltage in the microgrid. This can be due to a change from grid connected to islanding. An example of failure of the master inverter is shown in Fig. 6 (the grid topology is shown in Fig. 4). Fig. 6(a) shows the high-frequency voltage magnitude, measured at the *LCL* filter output, for the master power converter (blue) and two slave power converters, master failure occurring at t = 0.5 s.

2) Reassignment of the master inverter role. Once any of the events described above occurs, all the inverters start injecting the high-frequency voltage immediately. However, the slave inverters do not inject a constant magnitude high-frequency voltage, it increases with time instead (5)– (6), where V<sub>HF</sub><sub>0</sub> is the magnitude of the high-frequency voltage for each slave inverter right before the master inverter failure, and V<sub>HF</sub><sub>max</sub> is the limit established for the high-frequency voltage

 $v_{HF} = \left(V_{HF0} + k_2 t e^{k_1 V_{HF0}}\right) e^{j\omega_h t} \quad \text{if} \\ |v_{HF}| < V_{HF\_\max} \tag{5}$  $v_{HF} = V_{HF\_\max} e^{j\omega_h t} \quad \text{if} \ |v_{HF}| \ge V_{HF\_\max}. \tag{6}$ 



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Fig. 6. Simulation results showing the high-frequency voltage magnitude measured at the *LCL* filter output, for the master inverter, inverters 1 and 2, (a), commanded high-frequency voltage magnitude of inverters 1 and 2 after detecting the high-frequency voltage lost, (b), and magnitude of the secondary high-frequency voltage injected by inverter 1 after assuming the master role, and measured by inverter 2, (c).  $V_{hf1} = 0.05$  pu,  $\omega_{hf1} = -333$  Hz,  $V_{hf2} = 0.05$  pu,  $\omega_{hf2} = 303$  Hz.



Fig. 7. Elapsed time to reach the rated high-frequency voltage magnitude as a function of the initial condition  $V_{HF0}$  and of gain  $k_1$ , with gain  $k_2 = 1$ .

It is observed from (5) that the high-frequency voltage magnitude increases linearly with time, but both the starting value as well as the rate of increase being function of  $V_{HF0}$ . According to (5), the inverter with a larger initial voltage  $V_{HF0}$  starts with a larger initial value and increases the magnitude faster [see Fig. 6(b)], therefore reaching  $V_{HF_max}$  first. The philosophy behind this strategy is that, in general, inverters closer to the PCC before the failure are considered better candidates to assume the master role. The strategy established by (5)–(6) will produce that the inverters placed closer to the PCC will *win* the race to become master.

Fig. 7 shows the time needed by an inverter to reach  $V_{HF,max}$ , as a function of  $V_{HF0}$  and the gain  $k_1$ . It is observed from the figure that small differences in  $V_{HF0}$  produce large variations in the time needed to reach  $V_{HF,max}$ , therefore reducing the risk of more than one inverter becoming master at the same time. Once one inverter reaches  $V_{HF,max}$ , i.e., the rated high-frequency voltage magnitude, automatically changes its role to master (see Fig. 2)

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and continues injecting the high-frequency signal hereafter [see Fig. 6(b)].

It is noted that other reassignment strategies different from (5) and (6) could be used, the key issue for the design of new strategies being their ability to discriminate the most suitable inverters to assume the master role during the master reassignment process. It is also interesting to note that although in the strategy used in this paper the high-frequency signals are injected during the reassignment process (see Fig. 6), it is feasible for the inverters to produce the high-frequency signal *internally*, i.e., without physically injecting them into the grid, in such a way only when a inverter reaches  $V_{HF,max}$  it becomes the master inverter, and the injection of the actual high-frequency voltage into the grid occurs.

3) Notification of the role change to the rest of microgrid inverters. Once one inverter assumes the master role, it injects a secondary high-frequency signal (v<sub>dqhf2</sub>) during a short period [80 ms, see Fig. 6(c)]. This signal informs to the rest of inverters that the master role has already been reassigned. The rest of inverters automatically will stop injecting the high-frequency signal and change their mode of operation to slave mode (see Fig. 3). Fig. 6(c) shows the commanded voltage magnitude of the secondary highfrequency signal by inverter 1 and the measured secondary high-frequency voltage magnitude by inverter 2, which is used to stop its high-frequency signal injection [see Fig. 6(b)] and to switch to the slave mode.

#### V. HIGH-FREQUENCY SIGNAL SELECTION

Both the magnitude  $(V_{hf})$  and the frequency  $(\omega_{hf})$  of the high-frequency voltage injected by the master inverter needs to be set. Generally speaking, low magnitude, high-frequency signals will decrease the adverse impact on the THD, which needs to be considered to meet the connection standards [1]–[11].

A relatively large frequency range could be used, the limits coming from the interaction with the output *LCL* filter resonant frequency (see Figs. 2 and 3), the grid resonant frequency and the need of having spectral separation with fundamental frequency-dependent harmonics (e.g., -5th, 7th, and so on) that often exist [19]. It is noted in this regard that the injected high-frequency signal can have a positive or negative frequency, as it is a complex vector. The high-frequency signal can be chosen to be synchronous (i.e., an integer multiple like  $\pm 6$ th, +5th, -7th, and so on) or asynchronous with the fundamental frequency. Being in synchronism might provide some advantages, e.g., during the reassignment of the master role, all the inverters could inject the high-frequency signal in phase with each other, the process being then more repetitive. However, synchronizing the high-frequency signal with the fundamental voltage requires the estimation of the fundamental voltage phase angle, which might be problematic in the case of distorted grids. An asynchronous high-frequency signal with  $\omega_{h,f} = -333$  Hz was used for the simulation and experimental results shown in this paper (see Table I).

The magnitude of the injected high-frequency signal in the simulation results shown in this paper was set to 0.05 pu of the

# Master DSP i vabg i ab Filter Filter Circle Circl

TABLE II Experimental Setup Parameters

Grid	380 V, 50 Hz, Scc=2 MVA
Generator (G)	100 kVA, 380 V, 152 A
Master inverter, inverter 2 and 3	380 V, 30 kVA, 10 kHz.
Load	15 kW
Vdahfi	0.03 pu, -333 Hz
V <sub>dahf2</sub>	0.03 pu, 303 Hz
LPF bandwidth	25 Hz
HPF bandwidth	25 Hz
LCL filter resonance frequency	575 Hz

line-to-line voltage. The THD when the high-frequency signal is not injected is  $\approx 1.15\%$  while it increases to  $\approx 1.38\%$  when the high-frequency signal was injected, not compromising therefore the connection standards [1]–[11].

For the secondary high-frequency signal ( $v_{dqhf2}$ ), which is injected only for the communication purpose, the magnitude should be high enough to enable reliable detection by the remaining microgrid inverters, while the same considerations as for  $v_{dqhf1}$  could be made for its frequency. A magnitude of 0.05 pu was found enough for reliable reception by the remaining microgrid inverters.

### VI. EXPERIMENTAL RESULTS

To verify the viability of the proposed islanding detection and dynamic master assignment methods, the experimental setup shown at Fig. 8 was used. Though not shown in the figure, inverters 2 and 3 have the same topology as the master inverter, each including a DSP TMS320F28335 for their control. The parameters of the experimental setup are summarized in Tabel II. All the inverters include voltage sensors in the line side, which are needed for synchronization. The computational requirements for the implementation of the method are of 8.2  $\mu s$  for the master inverter operation mode and 12.8  $\mu s$  for the slave inverter operation mode.

Fig. 9 shows the magnitude of the output voltage of the high-frequency current regulator (4) of inverters 2 and 3 during transitions from island to grid connected (t = 0.5 s) and back to island (t = 1.5 s). The master inverter was injecting the high-frequency voltage continuously. The magnitude of the high-frequency current regulator output voltage reliably reflects the transitions between island and grid connected, the changes in the operating condition being detected in tens of milliseconds, which is in compliance with international standards requirements [1]–[11].

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Fig. 12. (a) Magnitude of the high-frequency voltage injected by the master inverter, inverters 2 and 3 and high-frequency voltage magnitude at the PCC, when the failure of the master inverter occurs, and (b) magnitude of the secondary high-frequency voltage injected by inverter 2 and measured by inverter 3 after inverter 2 assumes the master role.  $V_{h\,f\,1} = 0.03$  pu,  $\omega_{h\,f\,1} = -333$  Hz,  $V_{h\,f\,2} = 0.03$  pu,  $\omega_{h\,f\,2} = 303$  Hz. The dotted lines indicate the instant in which inverter 2 assumes the master role (eff) and inverter 3 detects the secondary high-frequency voltage role (fight).

Fig 12(a) shows the dynamic reassignment of the master role after the failure of the master inverter (occurs at t = 7 s in Fig. 12). It is observed from Fig. 12(a) that after the master inverter failure detection, inverters 2 and 3 start injecting the high-frequency signal as described by (5) and (6). Once inverter 2 reaches the rated high-frequency voltage [see Fig. 12(a)], automatically changes its role to master (see Fig. 2), continues injecting the high-frequency signal, and injects a burst with the secondary high-frequency signal to indicate to the rest of the inverters that the master role has already been reassigned [see Fig. 12(b)]. Fig. 12(b) shows the magnitude of the injected secondary high-frequency voltage by inverter 2 (new master) and measured by inverter 3. It is observed in Fig. 12(b) that inverter 3 stops injecting the high-frequency signal (red) immediately once it detects the presence of the secondary high-frequency signal  $(v_{dqhf2})$ . It is also noted that although  $v_{dqhf2}$  is injected during 2 s, inverter 1 detected the presence of the secondary signal in less than 100 ms, thus the injection time could be reduced.

It is finally noted that the THD at the PCC is only slightly affected by the injection of the different high-frequency voltages, increasing from 2.13% for the case when no high-frequency signal voltage is injected, to 2.87% when the high-frequency signals for both islanding detection and communications are injected.

### VII. CONCLUSION

An active method to detect islanding in grids with multiple parallel-connected inverters has been presented in this paper. In the proposed method, one inverter (master) continuously injects a high-frequency signal for islanding detection, while the rest (slave) inverters use a high-frequency current cancellation strategy to detect islanding. By doing this, interference between converters is avoided, as no high-frequency current circulates to/from the slave inverters.

A strategy for dynamic reassignment of the inverters role (master/slave) without the need of communications or preconfigured roles has also been proposed. The reassignment is done in three steps: 1) detection of significant changes in the grid, including master inverter failure and grid/island transitions; 2) reassignment of the master inverter role; and 3) notification to the rest of microgrid inverters.

Simulation and experimental results have been presented to demonstrate the operation of both concepts.

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Authors' photographs and biographies not available at the time of publication.

# A.2.3 Coordinated Operation of Parallel-Connected Inverters for Active Islanding Detection Using High-Frequency Signal Injection





$$v_{hf} = V_{hf} e^{j\theta_{hf}}; \quad \theta_{hf} = \int \omega_{hf} dt \tag{1}$$

$$i_{Fhf} = \frac{V_{hf}}{Z_{hf}} e^{j(\theta_{hf} - \varphi_z)} \tag{2}$$

$$Z_{hf} = R_{hf} + j\omega_{hf}L_{hf} \quad ; \varphi_z = \operatorname{atan}\left(\frac{\omega_{hf}L_{hf}}{R_{hf}}\right). \quad (3)$$

Fig. 1 shows the schematic implementation of the method. Fig. 2(a) and (b) shows the magnitude and phase of the high-frequency impedance  $Z_{hf}$  during a transition from island to grid and from grid to island. The changes in both metrics · All the inverters in the microgrid participating in the strategy should *know* the microgrid condition (island/grid connected) within a time frame compatible with islanding detection standards.

slave inverters on the grid condition. For the evaluation of the

strategies, the following issues need to be taken into account.

The adverse impact on the microgrid/grid power quality [total harmoic distortion (THD)] due to the injection of high-frequency signals should be kept as small as possible



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is analyzed here. In the proposed strategy, all the inverters synchronously inject a high-frequency signal. The inverters dynamically readapt their mode of operation between voltage and current injection, according to their location and to the grid condition. The model used for the analysis is first presented. Combined voltage/current injection, synchronization of the high-frequency signals, and parallel operation of inverters are analyzed in further sections.

Grid Model: The microgrid model shown in Fig. 5 will be used for analysis and simulation purposes. It is observed that the microgrid has a ring configuration, with node k being the PCC. The mathematical model of the grid is given by (5), shown at the

systems [24]). It is finally noted that (5) assumes that the inverters operate as a voltage source. For inverters operating in the current source mode, (5) can be algebraically rearranged by moving the corresponding current  $i_{Fk}$  to the left term (inputs vector) and the inverter voltage  $v_{hfk}$  to the right side (outputs vector) of the equation, respectively.

in Section I by making the load impedances equal to infinity.

This is the case when most or all of the power is evacuated to the grid at the PCC (e.g., distributed photovoltaic generation

Combined High-Frequency Voltage/Current Signal Injection: A means to combine current and voltage injection is





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Fig. 8. Schematic representation of the transition between island and grid conditions. (a) Magnitude of the high-frequency voltage and (b) current injected for islanding detection; (c) high-frequency impedance; and (d) secondary highfrequency voltage.

voltage will cause high-frequency currents circulating among the inverters. This will adversely affect the power quality (THD), also making more challenging the detection of the grid/island condition.

Phase synchronization of the inverters can be done by selecting the high-frequency voltage to be an integer multiple of the grid frequency. A cascade complex coefficient filter with complex phase-locked loop (CCCF-CPLL) [26] was used for this purpose (see Fig. 6).

Errors in the synchronization of the high-frequency signals are likely to occur in practice due to several reasons. Differences in the voltage angle in different parts of the network and/or harmonics/unbalances in the grid voltage can affect the PLL angle estimation and produce an unsynchronized injection of the high-frequency voltages. Adverse effects of this would include errors in the estimated high-frequency impedance and an increase in the THD due to high-frequency currents circulating among the inverters.

Errors due to differences in the voltage angle are expected to be of little importance in practice. The angle difference will be small for inverters operating near each other. For inverters located farther away from each other, the angle difference and the impedance between the inverters will increase nearly proportionally, roughly cancelling each other. It is also noted, in this regard, that in networks spread over a smaller area, the impedances are still inductive but have a significant resistive component [1].

A similar argumentation can be used to analyze the effects of harmonics/unbalances. Neighboring inverters should experience similar disturbances and react in a similar manner, thus limiting the risk of differential high-frequency voltages among inverters. However, the behavior in this case will strongly depend on the PLL's response (bandwidth, harmonic rejection capability, etc). Inverters with different PLL designs might respond differently to harmonics, transients, etc., increasing the risk of interference. A thorough analysis of this issue has not been carried out yet.

Parallel Operation of the Inverters: Inverters using the combined voltage source/current source modes can be directly

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connected in parallel. The result is a microgrid in which all the inverters participating in the islanding detection strategy inject the high-frequency signal. Each inverter automatically selects the mode of operation as a function of the high-frequency impedance  $Z_{hf}$  present at its terminals. Fig. 9 shows an example obtained using the model in Fig. 5, (5) for the case of grid (left) and island operation (right). In the example shown in Fig. 9, the microgrid consists of seven nodes radially connected with the PCC connected to node 1. Each inverter uses the configuration shown in Fig. 6. The system parameters are the same as the experimental results (see Table I). The bars in Fig. 9(a) show the inverter output voltage  $v_{hf}$  and line voltage  $v_{Lhf}$ (filter output voltage) for each node. Fig. 9(b) shows the filter, line, and load high-frequency current. The limits for the highfrequency voltage  $v_{hfmax}$  and current  $i_{hfmax}$  are indicated in Figs. 8(b) and 9(a) (see Fig. 7 and 7). Node 1 corresponds to the PCC, the load current in this node coinciding, therefore, with the high-frequency current circulating into the grid.

It is observed from Fig. 9(a) and (b) that for grid-connected case inverters in nodes 1, 2, and 7 operate in the *current source* mode. Due to their closeness to the PCC, the impedance seen by these inverters is small, and their high-frequency current is limited to  $i_{hfmax}$ . On the contrary, nodes 3 to 6 operate in the *voltage source* mode as they are further from the PCC. It is remarked again that the transition between *voltage source* and *current source* occurs smoothly, no reconfiguration of the injection mechanism was needed.

Islanding Detection and Islanding Notification: Islanding is detected from the measured high-frequency impedance. Fig. 9(c) shows the high-frequency impedance seen at the inverters terminal (7) and filters output (8)

$$Z_F + Z_{hf} = \frac{v_{hf}}{i_{Fhf}} \approx \frac{v_{hf}^*}{i_{Fhf}}$$
(7)  
$$Z_{hf} = \frac{v_{Lhf}}{i_{Fhf}}.$$
(8)

Since  $Z_{hf}$  is the variable reflecting the changes between grid and islanding modes, (8) would be used in principle for islanding detection. However, using (7) has the advantage that the commanded high-frequency voltage can be used instead of the high-frequency component of the measured line voltage needed in (8). This slightly simplifies the required signal processing. Still, both options are expected to give similar results.

Some expected facts are observed in Fig. 9. For the case of grid-connected operation, the high-frequency impedances for each node [both  $Z_{hf}$  and  $Z_F + Z_{hf}$  in Fig. 9(c)] depend on the node location relative to the PCC. The impedances for nodes closer to the PCC are significantly smaller. The largest variations of the high-frequency impedance between grid [see Fig. 9(c)] and island connection [see Fig. 9(c)] occur at nodes closer to the PCC.

Islanding detection is currently based on the rate of variation of  $Z_{hf}$  with time, i.e.,  $\Delta Z_{hf}/\Delta t$  [4]–[13]. Comparison of  $Z_{hf}$ with a threshold might also potentially be used [21]. Islanding detection will be easier and more reliable for nodes closer to the PCC. On the contrary, islanding detection might be difficult for nodes far from the PCC in large microgrids. Thus, inverters


Grid	380 V, 50 Hz, S <sub>cc</sub> =2 MVA
Inverters	380 V, 30 kVA, 10 kHz.
Load	15 kW
vhfmax	13 V (0.0325 pu), 250 Hz (5×ω <sub>e</sub> )
ihfmax	1 A (0.0155 pu)
Line impedance ZL	2Ω
LCL filter	2.4/2.3 mH (inverter/grid side), C=30uF

working in the *current source* mode would be in principle better candidates to detect islanding than inverters working in the *voltage source* mode.

A possible strategy would be to enable only inverters working in the *current source* to *inform* on the grid condition to the rest of inverters present in the microgrid. A secondary high-frequency signal would be for this purpose. Inverters working in the *current source* mode would detect islanding by measuring a positive  $\Delta Z_{hf}$  over a predefined time window.

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Once islanding is detected, they would inject the secondary high-frequency signal  $v_{hf2}$ . On the contrary, if inverters injecting the secondary high-frequency voltage detect the change between islanding and grid-mode from the measured  $\Delta Z_{hf}$ , they would discontinue injecting the secondary high-frequency voltage. Injection of the secondary high-frequency voltage is schematically shown in Fig. 8(d). Details on the use of the method can be found in [21] and [22]. This strategy has not been studied in detail; further analysis would be needed to verify its viability and performance.

### V. EXPERIMENTAL RESULTS

The proposed islanding detection strategy has been tested using the experimental setup shown in Fig. 10. The parameters are summarized in Table I. Both inverters are identical and use IGBTs. All control (current regulators, synchronization, etc.) is implemented on a TMS320F28335 DSP.

 $\dot{F}ig.$  11 shows the transition between island and grid modes. Fig. 11(a) and (c) shows the commanded and filter output

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impedance  $Z_{hf}$ . It is noted however that, for the case of

large microgrids, inverters far from the PCC might experience significantly smaller variations of the equivalent impedance. This will make them less reliable for islanding detection.

#### VL CONCLUSION

A method to detect islanding in grids with multiple parallelconnected inverters has been presented in this paper. In the proposed method, all the inverters participating in the strategy inject the high-frequency signal. The inverters can operate in two different modes of operation, namely, current injection mode and voltage injection. Combined use of these modes has two advantages, i.e., the adverse impact that the injection of the high-frequency signal has on the power quality (THD) is limited and provides a mean to evaluate the suitability of a particular inverter to detect islanding, which can be important in large microgrids. An important feature of the proposed method is that the transition between current injection and voltage injection modes of operation occurs automatically and smoothly, no change in the configuration of the inverters is required. Simulation and experimental results have been presented to demonstrate the viability of the proposed method.

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<ul> <li>[17] A.</li> <li>m</li> <li><i>P</i></li> <li><i>P</i></li> <li>[18] L.</li> <li>[18] L.</li> <li>(19] L.</li> <li>(19] L.</li> <li>(19] M.</li> <li>(20] M.</li> <li>(20] M.</li> <li>(21) D.</li> <li>(31) <i>I</i></li> <li>(31) <i>I</i></li> <li>(32) D.</li> <li>(41) <i>I</i></li> <li>(32) D.</li> <li>(41) <i>I</i></li> <li>(41) <i>I</i></li></ul>	. V. Timbus, R. Teodorescu, and U. Borup, "Online grid impedance easurement suitable for multiple PV inverters running in parallel," in <i>roc. IEEE APEC</i> , Mar. 2006, pp. 907–911 Asiminoaci, R. Teodorescu, F. Blaabjerg, and U. Borup, "A digital con- olled PV-inverter with grid impedance estimation for ENS detection," <i>EEE Trans. Ind. Appl.</i> , vol. 20, no. 4, pp. 1480–1490, Nov./Dec. 2005 Asiminoaci, R. Teodorescu, F. Blaabjerg, and U. Borup, "A new method fon-line grid impedance estimation for PV inverter," in <i>Proc. IEEE</i> <i>PEC</i> , Sep. 2004, pp. 1527–1533. L. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "On-line grid impedance simation based on harmonic injection for grid-connected PV inverter," <i>Proc. IEEE ISIE</i> , Jun. 2007, pp. 2473–2442. D. Reigosa, F. Briz, C. B. Charro, P. Garcia, and J. M. Guerrero, "Active landing detection using high-frequency signal injection," <i>IEEE Trans.</i> <i>d. Appl.</i> , vol. 48, no. 5, pp. 1588–1597, Sep./Oct. 2012. Reigosa, F. Briz, J. Guerero, P. Garcia, and C. Blanco Charro, "Active isibated meterse using high-frequency signal injection," <i>IEEE Trans.</i>	<ul> <li>David Díaz-Reigosa (S'03–M'07) was born in Spain in 1979. He received the M.E. and Ph.D. de- gress in electrical engineering from the Univer- sity of Oxiedo, Gijón, Spain, in 2003 and 2007, security.</li> <li>Was a Visiting Scholar with the Wisconsin fuction Machines and Power Electronics Consor- tion, University of Wisconsin-Madison, Madison, N, USA, in 2007. He is currently an Associate professor with the Department of Electrical Engi- tiones, and digital signal process.</li> <li>Dr. Diaz Reigosa was awarded a fellowship of the Personnel Research fining Program funded by the Regional Ministry of Education and Science of the Principality of Asturias from 2004 to 2008.</li> </ul>
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## A.2.4Islanding detection in three-phase and singlephase systems using pulsating high frequency signal injection

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## Islanding detection in three-phase and single-phase systems using pulsating high frequency signal injection

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Abstract: This paper analyzes the use of pulsating high frequency signal injection for islanding detection purposes. Active islanding detection using high frequency signal injection is an appealing option due to its reduced non-detection zone, reduced cost and ease of implementation. The use of a rotating However, this method can only be applied to three-phase systems. In this paper, the use of a pulsating high frequency signal injection is proposed. While it uses the same principles as rotating signal injection, it can be applied to both three-phase and single-phase systems.<sup>1</sup>

#### I. Introduction

Islanding is defined as the situation where a distributed generator (DG) or DGs continue generating power when they are not connected to the utility grid. Islanding detection has been the focus of significant research efforts during the last years due to the increasing share of the distributed generation in the power system. Distributed generation can be based either on renewable (wind turbines photovoltaic, ) and non-renewable (biomass, fuel cells, micro-gas turbines,...) energy resources. National, regional and local authorities regulate the interconnection of the distributed energy resources to the utility grid, in most of the cases following the standards and recommendation that are published by standardizing institutions [1-8]. In all the cases the standards require that the system has to detect if it is connected or disconnected from the utility grid (islanding detection) within a timeframe, e.g. 2 seconds for the IEEE-1547 [1], UL-1741 [2], IEC-62116 [3], AS-4777 [4], IEEE-929 [5] and DIN-VDE-0126 [6], or 5 seconds for the Swiss [7] and Australian [8] standards. These standards use the impedance variation within the considered timeframe as the metric for islanding detection, e.g. 1  $\Omega$  variation for the German and  $0.5 \Omega$  for the Swiss and Australian

Three different scenarios can be considered for islanding detection: Single-inverter, Multi-inverter and Microgrid [9]. In the Single-inverter scenario only one DG exists and all the power is exported to the grid. In the Multi-inverter scenario most (or all) of the power generated by the DGs is exported to the grid throughout the point of common coupling (PCC). In the *Microgrid* scenario, a major portion (or all) of power generated by the DGs is consumed by the microgrid loads, the remaining power being exported to the grid throughout the PCC. The *Multi-inverter* case could be considered as a particular case of the Microgrid scenario, but with a majo portion of the energy being exported to the utility grid. In all cases, the system is required to have the ability to detect if it is connected or isolated from the utility grid [9, 17-19].

Islanding detection methods can be classified into three groups: passive [10, 11, 22, 25, 29], active [9, 11-19, 23, 24, 26, 27, 28] and communication based [11] methods. Passive

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and active methods are inverter resident [9, 10], while communication based methods are remote [9, 10]. Passive based methods are grid friendly, as they do not introduce any disturbance in the grid [10], but have the disadvantage of a large non-detection-zone (NDZ) [11]. Active methods are based on the injection of some disturbing signal in the grid [9, 11-19], therefore having a negative impact on the power quality. However, they have low NDZ [17, 18], being easy and cheap to implement. Finally, communication based methods have no NDZ, but they need a communication infrastructure, being therefore subjected to communication failures [10, 17, 18].

Active islanding detection based methods can be further divided into two groups:

- Grid variable variation based methods [11]. Islanding is detected from the grid response to a small disturbance, typically in the voltage or frequency, produced by the power converter connecting the DG to the microgrid.
- Impedance estimation based methods [11-19]. In these methods, islanding is detected from variations at the power converter output impedance. These methods can be further divided into methods that estimate the impedance by the variation of the active/reactive power [12] or by the injection of some form of high frequency excitation [13-18]. The high frequency excitation can be injected continuously or intermittently [17, 18]. The use of harmonics due to the non-ideal behavior of PWM inverters has also been recently proposed to estimate the high frequency impedance [19], no high frequency signal being injected in this case. It is noted that the methods reported in [12-19] can only be used in three-phase systems

While the implementation of islanding active method based on the high frequency impedance variation is relatively simple in the case of Single-inverter, interference among converters can occur both in the Multi-inverter and Microgrid ecenarios, which can result in eroneous impedance estimation and therefore incorrect islanding detection [9, 17, 18]. Strategies to prevent from this to happen have already been proposed [9, 18]. Most of the impedance estimation active islanding

detection methods that have been proposed are intended for three-phase systems [11-18]. Nevertheless, single-phase DGs (e.g. single-phase micro-wind generation, small-scale solar panel,...) for low-power home applications are becoming of great interest. The reduced implementation cost of the active islanding detection based methods therefore makes them an appealing option for these kinds of applications.

In this paper, islanding detection using a pulsating high frequency signal is proposed. The main advantage of the pulsating excitation compared to other forms of high frequency excitations that have already been proposed [12-19] is that it can be used indistinctly with single-phase and

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three-phase systems, while methods in [12-19] can only be used in three-phase systems. Compared to intermittent injection methods [12, 13, 15], the proposed method allows almost instantaneous detection of island/grid-connected condition, as it uses continuous injection. Contrary to this, with intermittent injection [12, 13, 15] detection of island/grid-connected condition is only possible when the high frequency signal is injected, further restriction for these methods come from the fact that a time delay in the processing of the signals is needed use to the transient in the resulting high frequency currents whenever the high frequency voltage is injected [17]. Regardless of implementation aspects, the proposed method responds to the same principles as continuous rotating high frequency voltage signal injection based islanding detection methods [17-19], and provides therefore similar performance in terms of accuracy and reliability detecting the island/grid condition in three-phase systems.

An additional advantage of the pulsating high frequency signal injection is that this type of excitation can be used for unbalance fault detection in three-phase systems.

unbalance fault detection in three-phase systems. The paper is organized as follows. A brief review of active islanding detection methods based on high frequency signal injection as well as the analytical formulation of the proposed method is presented in section II. The use of pulsating high frequency signal injection for phase-to-phase and phase-to-ground fault detection in three-phase systems is discussed in Section III. Finally simulation and experimental results confirming the viability of the method are shown in section IV and V respectively.

# II. Islanding detection using pulsating high frequency signal injection

DGs are usually connected to the main grid/microgrid by means of a three-phase (see Fig. 1a) or single-phase (see Fig. 1b) PWM-VSI [17-20]. The H-bridge inverter (Fig. 1b) is the most common topology in single-phase systems [20]. High frequency signal injection active islanding detection based methods inject a high frequency signal superposed on the fundamental voltage through the PWM-VSIs, islanding being detected from the variations of the measured high frequency impedance. The use of a rotating high frequency signal has been proposed for islanding detection [9, 17-19]; however this type of high frequency excitation cannot be applied to single-phase systems. Selection of the frequency for the high frequency

Selection of the frequency for the high frequency excitation involves trading off several issues, including the adverse impact of the injected signal on the power quality, the spectral separation with the fundamental voltage as well as with the output LCL filter and the grid resonance frequencies [17, 18]. Frequencies ranging between 75 and 400 Hz can be found in the literature [9, 11-19].

The principles and implementation of the proposed islanding detection method using a pulsating high frequency signal are analyzed following. In the first place, the case of three-phase system is considered, the single-phase case being analyzed later.

#### a) Three-phase systems

When a pulsating high frequency signal voltage (1) is injected into a three-phase system with an angle of injection

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 $φ_i$ , the resulting high frequency current at the output of the LCL filter (see Fig. 1) is given by (2), the grid high frequency impedance being (3), where  $v_{depl}$  is the injected high frequency signal,  $α_{iq}$  is the magnitude of the injected high frequency signal,  $α_{iq}$  is the magnitude of the injected high frequency signal,  $α_{iq}$  is the frequency of the high frequency signal,  $α_{iq}$  is the trequency of the high frequency current complex vector,  $i_{depl}$  is the output LCL filter high frequency current complex vector,  $i_{depl}$  is the output LCL filter inductance,  $Z_{deplev}$  is the unicode signal size the inverter side LCL filter inductance,  $L_2$  is the grid side LCL filter inductance.  $Z_{deplev}$  is the unicode high frequency impedance. The transformation from three-phase to dqθ quantities is given by (4). The angle of injection  $φ_i$  can be selected to be constant, or can change with an angular frequency of  $α_i$ . In the first case, the pulsating signal will be injected in a stationary reference frame, while in the second case, the pulsating signal is in injected in a reference frame that rotates at  $α_{i}$ .



grid/microgrid using a) a three-phase VSI, and b) a single-phase VSI.



Fig. 2 *abc* and *dq* reference systems.  $dq_s$ =stationary reference frame,  $dq_e$ =rotating reference frame.

It is observed from (1)-(2) that the pulsating high frequency voltage and current can be decomposed into two rotating signals ( $v_{dayf}^{\mu\nu}$ ,  $v_{dayf}^{\mu\nu}$ ,  $i_{dayf}^{\mu\nu}$ ,  $i_{dayf}^{\mu\nu}$ ) which rotate in opposite direction, each of half the amplitude of the injected signal. Both components can potentially be used for high frequency impedance estimation (3).  $v_{dayf}^{\mu\nu} = V_{uf} \cos(\omega_{hf}t) e^{i\omega_{f}} = V_{hf} \cos(\omega_{hf}t) e^{i\omega_{f}} =$ 

$$= \frac{V_{hf}}{2} e^{j(\omega_{hf}+\omega_{h})t} + \frac{V_{hf}}{2} e^{j(-\omega_{hf}+\omega_{h})t} = v_{dqhf}^{\rhoc} + v_{dqhf}^{nc}$$
(1)





Fig. 3 shows the signal processing needed for islanding detection using a pulsating high frequency signal for the case of a three-phase system. In the implementation shown in Fig. 3 the PWM-VSI is current regulated, a synchronous PI current regulator being used for this purpose ("Current reg." block in Fig. 3). In this case, the current regulator can react against the induced high frequency current. To prevent this, band-stop filters are used to reject the positive and negative sequence current components (2) from the current feedback (*BSF1* in Fig. 3). Band-stop filters *BSF2* and *BSF3* in Fig. 3 are used to reject the fundamental component of the voltage and current respectively, while *BSF4* and *BSF5* reject the negative sequence components, the positive sequence component of (3), islanding being detected from the high frequency impedance variation.

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a)

b)

### b) Single-phase system

Though the concept of complex vector defined by (4) is only valid in principle for the case of three-phase systems, it is also possible to use it with single-phase systems. This can be done by defining a complex vector in which one of the corresponding single-phase voltage/current and the other component (e.g. *d*-axis in (5) and (6)) is made equal to the corresponding single-phase voltage/current and the other component (e.g. *q*-axis in (5) and (6)) is made equal to zero. By doing this, the high frequency impedance (3) in a singlephase system can be estimated from (5) and (6), where  $v_{ang}$ is the injected high frequency output phase voltage and current respectively and  $i_{anf}$  is the inverter high frequency output phase current.

$$\begin{aligned} \mathbf{v}_{dphf} &= \begin{bmatrix} v_{ahf} \\ 0 \end{bmatrix} = \begin{bmatrix} V_{hf} \cos(\omega_{hf}t) \\ 0 \end{bmatrix} = \\ &= \frac{V_{hf}}{2} e^{j\omega_{hf}t} + \frac{V_{hf}}{2} e^{-j\omega_{hf}t} = v_{dphf}^{\rho c} + v_{dphf}^{\sigma c} \\ &i_{dqughf} = \begin{bmatrix} i_{aqughf} \\ 0 \end{bmatrix} = \begin{bmatrix} \frac{v_{ahf} - v_{aqughf}}{j\omega_{hf}L_2} \\ 0 \end{bmatrix} = \\ &= \frac{V_{hf}}{2*[Z_{dqughf}]} e^{j(\omega_{hf} - \varphi_2)} + \frac{V_{hf}}{2*[Z_{dqughf}]} e^{j(-\omega_{hf} + \varphi_2)} = \quad (6) \\ &= i_{dqughf}^{\rho c} + i_{dqughf}^{\sigma c} \end{aligned}$$

Fig. 4 shows the signal processing needed for islanding detection in a single-phase system. A single band-stop filter is needed to reject the component at  $\omega_{hf}$  (BSF1, see Fig. 4) to prevent the fundamental current regulator reaction. As for the three-phase system case, band-stop filters *BSF2* and *BSF3* reject the fundamental components and *BSF4* and *BSF5* reject the negative sequence component. Once the positive sequence component of the voltage and current are isolated, the high frequency impedance is obtained using (2) and (3), islanding being detected from the high frequency impedance variation.

It is finally noted that though in all the discussion presented in this paper it is assumed that a high frequency voltage is injected, it is possible to combine high frequency voltage injection and high frequency current injection as







Fig. 6. a) Phase-to-ground fault, and b) phase-to-phase fault.

described in [9]. These can be advantageous when multiple parallel-connected inverters implement the method [9]. It is also noted that the dead-time effect in PWM single-phase inverters produces a distortion that can be expressed as (7) [19], being therefore possible to use any of the high order harmonics in (7) for islanding detection purposes [19].

$$v_{an} = \frac{4\Delta V}{\pi} \sum_{n=1.5,7,...,n} \frac{1}{n} \sin(n\omega_f t)$$
(7)

# III. Phase-to-phase and phase-to-ground fault detection using pulsating high frequency signal injection

It has already been mentioned that since islanding in three-phase systems occurs simultaneously in all the three phases, it can be readily detected independent of the high frequency signal injection mode, i.e. stationary or rotating. It is noted in this regard that the implementation of the injection in the stationary reference frame is slightly simpler. However, the injection of the high frequency signal in a rotating reference frame opens interesting possibilities for the detection of phase-to-phase and phase-to-ground faults in three-phase systems.

Fig. 5a and 5b show the PCC voltage vector spectrum in a rotating reference frame  $(dq_e \text{ in Fig. 2})$  and in a stationary reference frame  $(dq_s \text{ in Fig. 2})$ , when the pulsating high frequency voltage is been superimposed on top of the fundamental excitation. As shown in Fig. 5a, the pulsating high frequency signal can be decomposed in two rotating signals,  $v_{delyl}^{pc}$  and  $v_{delyl}^{ac}$  of frequencies  $\omega_{hf}$  and  $-\omega_{hf}$ 

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respectively. By transforming this voltage vector to the stationary reference frame (see Fig. 5b), the frequency components  $v_{dqbf}^{pc}$  and  $v_{dqbf}^{nc}$  at  $\omega_{bf} + \omega_i$  and  $-\omega_{bf} + \omega_i$  are obtained respectively.

The most typical asymmetric faults that occur in threephase systems are the phase-to-ground, phase-to-phase and phase-to-neutral [21]. Typically the neutral wire is not available in the connection of three-phase distributed energy resources to the utility grid/microgrid through three-phase VSI (see Fig. 1a). Therefore, only the phase-to-ground and phase-to-phase faults will be analyzed in this section.

a) Phase-to-ground fault

When a pulsating voltage vector is injected into a three-phase system with a fault to ground in phase a (see Fig. 6a), the resulting high frequency phase currents are given by (8). The pulsating signal is injected in a  $dq_e$  reference frame which rotates at  $\omega_i = 50 Hz$  and it is assumed that the fault impedance is much lower than the system (load) impedance  $(Z_L)$ .

$$\begin{bmatrix} i_{a} \\ i_{b} \\ i_{c} \end{bmatrix} = \begin{bmatrix} \frac{V_{a} S}{Z_{L}} e^{f((\omega_{a} + \omega_{b}) - \delta^{*} \pi/6 - \phi_{z_{L}})} \\ \frac{V_{b} \sqrt{3}}{Z_{L}} e^{f((\omega_{a} + \omega_{b}) - \delta^{*} \pi/6 - \phi_{z_{L}})} \\ \frac{V_{c} \sqrt{3}}{Z_{L}} e^{f((\omega_{a} + \omega_{b}) + \delta^{*} \pi/6 - \phi_{z_{L}})} \end{bmatrix} + \begin{bmatrix} \frac{V_{a} S}{Z_{L}} e^{f((-\omega_{a} + \omega_{b}) + \delta^{*} \pi/6 + \phi_{z_{L}})} \\ \frac{V_{b} \sqrt{3}}{Z_{L}} e^{f((-\omega_{a} + \omega_{b}) - \delta^{*} \pi/6 + \phi_{z_{L}})} \\ \frac{V_{c} \sqrt{3}}{Z_{L}} e^{f((-\omega_{a} + \omega_{b}) - \delta^{*} \pi/6 + \phi_{z_{L}})} \end{bmatrix}$$
(8)

Applying Fortescue's theorem, (9), to the components in (8) at  $\omega_{ac} + \omega_{i}$ , a set of symmetrical components is obtained (10), with  $l_{addec}^{0}$ ,  $l_{addec}^{addec}$  and  $l_{addec}^{ec}$  being the zero, positive and negative sequence components respectively. It is noted that though the same transformation could be used with the components in (8) at  $-\omega_{hf} + \omega_i$ , the discussion following focuses only for the frequency components at  $\omega_{hf} + \omega_i$ .

$$\begin{bmatrix} i_{i}^{0} \\ i_{i}^{+} \\ i_{i}^{-} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^{-2} & a^{2} \\ 1 & a^{2} & a^{2} \end{bmatrix} * \begin{bmatrix} i_{a} \\ i_{b} \\ i_{c} \end{bmatrix}$$
$$\begin{bmatrix} i_{adylec}^{0} \\ i_{adylec}^{0} \\ i_{adylec}^{0} \end{bmatrix} = \begin{bmatrix} 2\sqrt{3} \\ \sqrt{3} \\ \sqrt{3} \\ r_{c}e^{f((-\omega_{0}-\omega_{0})-\varphi_{2})} \\ \frac{\sqrt{3}}{2} \\ r_{c}e^{f((-\omega_{0}-\omega_{0})-\varphi_{2})} \end{bmatrix}$$

where  $I_{cc} = V_b \sqrt{3}/Z_L$ . If the fault occurs in phase *b*, the resulting symmetrical components using (9) are given by (11), while if the fault occurs in phase c it is expressed by (12). It is observed from (10)-(12) that the faulty phase can be detected from the phase angle between the positive sequence component (  $i_{daylighc}^{pc}$ ) and the negative sequence component ( $i_{daylighc}^{nc}$ ), which is  $\theta$  when the faulty phase is phase a,  $2\pi/3$  when the faulty phase is phase b and  $4\pi/3$  when the faulty phase is phase c



b) Phase-to-phase fault

When a pulsating voltage vector which rotates at  $\omega_i$ , is injected into a three-phase system in which a phase-to-phase fault between phases a-b occurs (see Fig. 6b), the resulting phase currents are expressed by (13) and the resulting symmetrical components are given by (14) (only the phasors for the frequency components at  $\omega_{bf} + \omega_i$  are shown). It is assumed that the fault impedance  $(Z_F)$  is much lower than the load impedance  $(Z_L)$ .

The resulting symmetrical components when the fault occurs between phases b-c or c-a are given by (15)-(16). It is observed by comparing (14)-(16) that the faulty phases can be detected from the phase angle between  $i_{dqhfpc}^{pc}$  and  $l_{dq/dpc}^{nc}$ . I.e.  $\pi/3$  when the fault occurs between phases *a* and *b*,  $\pi$  when the fault occurs between phases *b* and *c* and  $-\pi/3$  when the fault occurs between phases a and c.

$$\begin{bmatrix} \dot{i}_{a} \\ \dot{i}_{b} \\ \dot{i}_{c} \end{bmatrix} = \begin{bmatrix} \frac{V_{ab}}{Z_{F}} e^{J((\omega_{b} + \omega_{b}) - \pi/6 - \varphi_{2F})} \\ -\frac{V_{ab}}{Z_{F}} e^{J((\omega_{b} + \omega_{b}) - \pi/6 - \varphi_{2F})} \\ 0 \end{bmatrix} + \begin{bmatrix} \frac{V_{ab}}{Z_{F}} e^{J((-\omega_{b} + \omega_{b}) + \pi/6 + \varphi_{2F})} \\ \frac{V_{ab}}{Z_{F}} e^{J((-\omega_{b} + \omega_{b}) + \pi/6 + \varphi_{2F})} \\ 0 \end{bmatrix}$$
(13)

$$\begin{bmatrix} i_{d_{ab}f_{f_{c}}}^{0} \\ i_{d_{ab}f_{f_{c}}}^{0} \\ i_{d_{ab}f_{f_{c}}}^{0} \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{3}}{3} I_{cc} e^{j((\omega_{a}+\omega_{b})-\varphi_{c_{f}})} \\ \frac{\sqrt{3}}{3} I_{cc} e^{j((-\omega_{a}-\omega_{b})+\pi/3-\varphi_{c_{f}})} \end{bmatrix}$$
(14)

$$\begin{bmatrix} i_{deffyc}^{0} \\ i_{deffyc}^{R} \\ \vdots_{deffyc}^{R} \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{3}}{3} I_{cc} e^{f((\omega_{f}+\omega_{i})c+\pi_{c}\varphi_{c})} \\ \frac{\sqrt{3}}{3} I_{cc} e^{f((\omega_{f}+\omega_{i})c+\pi_{c}\varphi_{c})} \\ \frac{\sqrt{3}}{3} I_{cc} e^{f((\omega_{f}+\omega_{i})c-\pi_{c}\varphi_{c})} \end{bmatrix}$$
(15)

IV. High frequency signal selection

where  $I_{cc} = V_{ab}/Z_F$  .

Criteria for the selection of the magnitude and frequency of the injected high frequency signal are discussed in this section

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(9)

(10)





Fig. 8 shows a transition from island to grid connected for the case of a three-phase system when the pulsating high frequency signal is injected in a stationary reference frame  $(dq_s, see Fig. 3)$ . Fig. 8a shows the  $dq_s$  components of the filter output voltage and Fig. 8b shows the  $dq_s$  components

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single-phase system case, the THD increases from  $\approx 1.03\%$  to

≈1.1% due to the high frequency signal injection. It is



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in Fig. 15a and 15b). Fig. 15d shows the power converter: rectifier, DC bus, inverter (three-phase and single-phase) and voltage and current measurement. Fig. 15e shows the control board, it uses a DSP TMS320F28335. Fig. 15f

		Tab	le II			
Three phase						
Grid			Inverter	Load	Line	
380V, 50	Hz,	$r_g/X_g=0.1$	,380V,	3 kW	R=0.1 Ω	
S <sub>cc</sub> =15MVA		~ ~	10kHz			
Single phase						
Grid			Inverter	Load	Line	
220V, 50	Hz,	$r_g/X_g=0.1$	,220V,	2 kW	R=0.1 Ω	
		~ ~				

Fig. 16 shows the experimental results for the same grid-island transitions used in Fig. 8 for simulation. As for the simulation results (see Fig. 8), an increase of the high frequency current magnitude is readily observed after the transition from island to grid-connected condition, due to the reduction of the overall high frequency impedance.



corresponding to the simulation results in Fig. 9. Again,

Fig. 18, 19 and 20 show the magnitude and phase of the estimated high frequency impedance during a transition for island to grid-connected (t=1 s) and from grid-connected to island (t=3 s). The high frequency signal was injected in the stationary reference frame in Fig. 18 and in a rotating reference frame in Fig. 19. It is observed that the high frequency impedance change is detected after a few ms. both for the case of three-phase and single-phase systems, therefore meeting the islanding detection standards [1-8]. The total harmonic distortion for the three phase system case



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<ul> <li>between i<sub>w</sub> and i<sub>w</sub> (red), when a phase-to-ground for occurs in phase b (1=4 s) (see description for Fig. 14). In the cases, it is observed a remarkable agreement with simulation results shown in Section IV.</li> <li><b>UL Cardunson</b></li> <li>This paper proposes an islanding detection method has on the injection of a pulsating high frequency signal. The individual of the pulsating high frequency signal is performed by any VSI connected to the microgrid. This an advantage compared to most of already proposed at islanding detection methods based on the estimation of impedance variation using high frequency signal injection. It has been shown that injecting a high frequency with a magnitude of 0.01 pu of the line voltage is enough reliable islanding detection. The island/grid-connect out is therefore connection standards. The island/grid-connect oution is detected in a few ms. both for the three-ph and single-phase systems. This is fast enough to meet islanding detection standards.</li> <li>Thially, it has been shown that injection of a pulsat frequency signal can also be used for unbalance fit detection in three-phase system.</li> <li>This is fast enough to meet viability of the proposed methods both islanding and unbalanced operation detection.</li> <li>UL1741, UL Standard for Isford 2012.</li> <li>UL1741, UL Standard for Isford 2012.</li> <li>UL1741, UL Standard K Stafty for Static Converters and Charlenee May 7, 1999, revised Jandards Conduction Stand.</li> <li>Austalian Standard Stafty, Tiefd Connection Of Energy Static Converters of the information System Statement.</li> <li>West Standard Stafty, Tiefd Connection Of Leng Static Converters and Charlenee May 7, 1999, revised Jandards Conduction Committee 21 on Photovoltatic Power Systems.</li> <li>West Standards Convention Photovoltatic Power System.</li> <li>West Standards Adstafty, Tiefd Connection Of Leng Static Converters of Charlenees Photovoltate Power System.</li> <li>West Standards Adstafty, Tiefd Connection Devise Batverse, State Static State</li></ul>	<ul> <li>116] M. Ciobotaru, R. Teodorescu and F. Blasbjerg, "On-line Grid Impedance Estimation Based on Harmonic Injection, for Grid-Connected PV Invert," IEEE-ISE, pp. 2473–2442, June 2007.</li> <li>118] Dahading Detection Using High Frequency Signal Injection," IEEE Trans. on Ind Appl., 448(5):1588–1597, Sept. 2012.</li> <li>119] Dahading Detection for Multiple Parellal-Connected Inverter-Based Distributed Generators Using High Frequency Signal Injection," IEEE Trans. on Power Elect., 49(5):1411–1420, March 2014.</li> <li>120] P. Reigosa, F. Briz, C. Blanco and J. M. Guerrero, "Islanding detection in prid-connected power converters using Barmonics due to 266, Sept. 2013.</li> <li>120] Y. Xue, L. Chang, S. B. Kiger, J. Bordonau and T. Shimizu, Topologies of Single-Phase Inverters for Small Distributed Power Generation. An Overweik, "IEEE Trans. on Power Elect., 15(5):1305–1314, Sept. 2004.</li> <li>121] Y. Zhou, H. Li, L. Liu, "Integrated Autonomous Voltage Regulation and Banding Detection for High Penetration PM Applications," IEEE Trans. Power Elect., 28(6):2826-2841, Jane 2013.</li> <li>120] Y. Zhou, H. Li, L. Liu, "Integrated Autonomous Voltage Regulation and RFM Resetive Power Paranton). AmEnd Mark Method Based. 2014, 1499–5012. Was 2013.</li> <li>121] Y. Zhou, H. Li, L. Liu, "Integrated Autonomous Voltage Regulation and RFM Resetive Power Terration. Nature Prevation of Phylopherations," IEEE Trans. Power Elect., 28(6):2826-2841, Jane 2013.</li> <li>123] Y. Zhou, H. Li, L. Liu, "Integrated Autonomous Voltage Regulation and RFM Resetive Power Neuration, Neurosci Photovoltaic Systems," IEEE Trans. Power Elect., 20(1):407-408, Sep. 2014.</li> <li>121] Y. Zhou, H. Li, K. Liu, M. J. Zhang, T. Ku, G. Shen, C. Hu, "A model and photovoltaic Systems," IEEE Trans. Power Elect., 20(1):407-408, Sep. 2014.</li> <li>123] Y. Zhou, H. Li, K. Liu, M. J. Zhang, T. Ku, G. Shen, Y. Zhu, N. He and J. Ma, "An Improved Islanding Detection Method for Grid Connected Inverter With Interface InDC Distribution Systems," Power Elect.</li></ul>
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