Challenges of Multi-channel Interleaved Bidirectional Power Converters and their Digital Solutions

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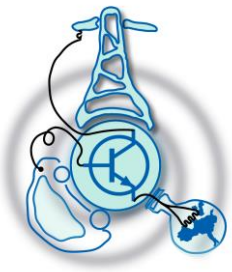

Submitted to the Department of Electrical and Electronic Engineering in partial fulfilment of the requirements for the degree
of

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ABSTRACT

This thesis work presents the challenges of bidirectional interleaved converters and proposes possible solutions which can be easily implemented using commonly available digital controllers. Implementation of interleaved power converters using coupled inductors in opposite direction has the advantage of reducing the magnetization current and hence reduces the volume of inductor required. However, use of coupled inductors has two main challenges. The first is the circulating current through the coupled inductors due to unbalanced pole voltage. The second issue is the sampling problem which causes oscillation in the output. In this thesis, a simple solution is proposed which can be implemented using simple DSP. Independent PI controller for each channel is proposed to ensure balanced channel currents and sampling at higher frequency and averaging it over a switching period is used to minimize the sampling error. Four channel interleaved bidirectional power converters are considered in simulation using both coupled and uncoupled inductors. It has been found that a multi-channel interleaved converter which uses single stage pair coupling gives a better volume reduction as compared to either of uncoupled inductors, circular inter-cell coupling or multi-stage pair coupling. Experimental setup is made to test the proposed solutions. The control algorithm is implemented using Piccolo F28069 DSP from Texas Instruments. The power converter was operated in two modes: as DC/DC buck converter and DC/AC inverter mode both of them at 10 kHz switching frequency. Using sampling instances which are synchronized with PWM carriers resulted oscillation when it is applied to coupled-interleaved power converters. On the other hand, simultaneous sampling of all channels at sampling rate which is a multiple of both the number of channel and the switching frequency gives a better system response. Harmonics analysis is done using Fast Fourier Transform (FFT). All the results reveals that interleaved power converters decrease current ripples and increase ripple frequency which can significantly reduce the size of passive elements in the converter. This increases the power density of the converter, increases system reliability and modularity and improves efficiency. Such

converters suits very well not only for high power high current application, but can also be good candidates for low power applications which may require high power density.

Key Words: Bidirectional Interleaved Power Converters, Coupled Inductors, High Power Density Converters, Piccolo F28069 DSP, Sampling Techniques

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DEDICATION

To

my beloved father ***Mr Tadesse Ayele Belay***

and

the rest of ***my family***

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TABLE OF SYMBOLS

AC	Alternating Current
$\emptyset_m$	phase Margin (degree)
Δ	peak to peak current ripples (A)
Δ_{max}	maximum peak to peak current ripple (A)
A_c	magnetic core cross section area (cm^2)
ADC	Analog to Digital Converter
A_p	area product of inductor (cm^4)
A_w	window area of magnetic core (cm^2)
B_{max}	maximum magnetic flux density (T)
C(t)	carrier signal
CAN	Controller Area Network
Cdc	DC link capacitors (F)
Cf	filter capacitor (F)
d, d(t), d(s)	duty cycle
DC	Direct Current
d-q-0	rotational reference frame
DSP	Digital Signal Processor
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EOC	End of Conversion
ePWM	Enhanced Pulse Width Modulation
F28069	Piccolo micro controller
FET	Field Effect Transistor
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
G1, G2, G3, G4	Switching gate signals for upper legs in their order
G(s)	transfer function of Power Converter
GaN	Gallium Nitride
$G_{open}(s)$	open loop transfer function
GPIO	General Purpose Input Output
HVDC	High Voltage Direct Current
I_er(t)	instantaneous error current (A)
I_ref(t), Iref	instantaneous Reference Current (A)
$I_{a\_average}$	average channel current (A)
I_{a1}, I_{a2}, I_{a3}	instantaneous channel currents of "phase a" (A)
$i_{ch1}, i_{ch2}, i_{ch3}, I_a, I_b, I_c$	instantaneous channel currents (A)
Icir_ab, icir_cd, icir_ab_cd	circulating currents (A)
IGBT	Insulated Gate Bipolar Transistor
$I_{in}, I_{total}, Io(t)$	total current (A)

I_{mag}	magnetizing current (A)
Irms	root mean square current (A)
J	current density (A/cm^2)
K_i	integral gain
K_p	proportional gain
Kvol	constant relating volume and area product of inductors
Kw	core window fill factor
Kwt	constant relating weight to area product of inductors (g/cm^3)
L_1, L_2,L_3,l_{m1}.l_{m2}	inductor parameters (H)
MOSFET	Metallic Oxide Semiconductor Field Effect Transistor
MW	Mega Watt
OFF	position of switch when connected to lower voltage level
ON	position of switch when connected to higher voltage level
PI	proportional-integral controller
PI(s)	transfer function of PI Controller
PWM	Pulse Width Modulation
PWM1A, PWM2A, PWM3A	PWM signals for upper legs
RAM	Random Access Memory
Rload	resistive Load
S1, S2,…,S8	bidirectional switches
SOC	Start of Conversion
t	time (s)
T_a	phase shift between channels (s)
TI 2000	DSP family from Texas Instruments
T_s	Switching period (s)
UPS	Uninterruptable Power Supply
USB JTAG	emulation interfacing DSP with Code composer
V_a, V_b, V_c, V_d	channel pole voltages (V)
Vdc	DC link voltage (V)
V_o	output voltage (V)
Volume	volume of inductor (cm^3)
Vref(t)	reference voltage generated by the controller (V)
ω_b	bandwidth of controller (Hz or rad/s)
ZOH	Zero Order Hold

I. INTRODUCTION

Power converters are main part of today's energy conversion systems. As the concern of environmental pollution is increasing from time to time, renewable energy resources are getting more attention. These renewables include hydro, solar, wind and geothermal which can be used to produce a relatively clean energy. These resources, specifically the wind and solar, are intermittent in nature and needs power converters to monitor and control their output voltage and current. This allows smooth operation and reliable grid integration. Application of power converters is not limited to energy conversion systems. They got wide application in the area of electric vehicle, UPS, switched mode power supply, variable speed drives and HVDC systems.

There are two issues arising from the use of power converters. The first is how to achieve high power density converters by reducing the size of associated filters. The second is how to design power converters for high power application. The conventional power converters are designed with conventional low power electronic devices (such as IGBT and MOSFET). In addition, as the power level increases, the possible maximum switching frequency of electronic devices should decrease so that the switching losses remain within the limit of the switching devices [1]. Low switching frequency, in turn, causes more harmonics which leads to lower efficiency and larger size of filter. This shows that either the conventional power converters needs some design modification or new power electronic devices with higher power rating need to be developed. The latter is not yet developed well and it could be more expensive too. However, different approaches has been proposed in the design of high power converters using conventional power electronic devices. Some of these are, use of power electronic devices in series; use of power electronic devices in parallel and use of power converters units in parallel.

Power electronic devices connected in series can be used for high voltage application. Because of the series connection, each device experiences lower voltage stress while handling higher overall voltage. The devices in series can be switched ON and OFF as a single unit or step by step. If they are operated together, there is no significant contribution in the harmonic reduction. Operating them step by step in the form of multilevel converters, on the other hand, helps to minimize harmonic distortions. However, due to parameter mismatch of the switching devices, it needs advanced control and additional circuit, such as capacitors in parallel, for it to function smoothly [2].

The second method is the use of power electronic devices in parallel which enables to handle higher current. In this case, each device will experience a lower current rate while handling

higher overall total current. The devices connected in parallel are supposed to operate (ON and OFF) together so that they can share the current equally. This also need additional circuit to balance the voltage across the devices. There is no visible contribution from it in the overall harmonic reduction too [2, 3].

Use of power converter units in parallel is yet another option to handle high power at lower voltage rating. They consists of individual power converters sharing the DC bus and output filter circuit. The power electronic devices from parallel legs can be operated either in interleaved way or simultaneously. Operating them simultaneously increases redundancy but doesn't contribute significantly in reducing the filter size. By interleaving the power converters, on the other hand, the switching of power electronic devices on parallel legs are phase shifted from one another which results a phase shift in the current ripples. This causes partial or full cancelation of current ripples leading to a significant reduction in harmonic content in the total output current. Having less harmonics in the output current means less size of filter requirement, and hence, more power density and better efficiency [3]. In addition, literatures shows that use of coupled inductors instead of independent inductors results a more size reduction of inductor sizes as the dc component of magnetization flux cancels out when inductors are coupled in reverse direction [4].

Although interleaved power converters do not need a complex algorithm and any additional balancing circuits as multilevel converters to achieve higher power density, there are some challenges in their implementation. Even if interleaved converters are a better option when it comes the need to handle very high power, their application for lower power level usually requires higher number of components than the equivalent single conventional converter [4]. This needs to be counter balanced by the potential reduction of the filter size to achieve higher power density with a reasonable cost. The second challenge is the implementation of interleaved PWM signals together with appropriate sampling technique which usually needs advanced DSP with FPGA. The controller also needs to balance the current in each channel which may not be equal at equal duties due to the mismatch of inductor parameters in each channel. The third challenge is the issue of circulating currents created by the difference in common mode voltages of each channel while being operated in interleaved mode. This usually can be controlled by taking care of the design of coupled inductors for particular level of circulation current which in turn is related to the magnetization current of coupled inductors [5]. There are also some minor issues related to the electromagnetic compatibility (EMC) as some harmonics from each

channel add up. The magnitude of such harmonics is related to the interleaving angle; and hence, it needs attention from the point of design of EMC filter.

The purpose of this thesis work is to understand the principle behind interleaved converters, study associated challenges and propose an optimal solution which can address most of those challenges and implementing them with commonly available digital platforms such as TI C2000, F28069.

II. OBJECTIVES AND DELIVERABLES

The main objective of this thesis work focuses on investigating, modeling, simulating and implementing a multichannel (3+ channels) converter using digital control platform (TI – C2000). This includes the following specific objectives:

1. Modeling multichannel interleaved converter using both coupled and uncoupled inductors
2. Inductor volume comparison between topologies that use coupled and uncoupled inductors
3. Implementation of PSIM simulation models for the proposed topologies
4. Comparison of sampling techniques by simulation
5. Developing the equivalent digital algorithm and implementing it with commonly available TI-C2000 platforms
6. Build an experimental setup
7. Experimental validation of ripple reduction by interleaved power converters
8. Experimental validation of proposed sampling technique

The deliverables of this thesis work are:

- Working simulation models
- Code composer based C-code for TI-C2000 F28069 microcontroller
- Functional experimental setup
- Project report including simulation results and experimental validation of current ripple reduction and proposed sampling technique

III. STRUCTURE OF THE THESIS

The remaining part of the report is organized into five main parts. Chapter One discusses the state of the art in brief regarding interleaved power converters. Analytical modeling and comparison of proposed models are described in Chapter Two. Chapter Three explains

simulation models and their results. Experimental setup and validation of proposed topologies is presented in Chapter Four. Finally the conclusions and future works are summarized in Chapter Five.

IV. SUMMARY

In the preceding sections, a general overview of power converters and, in particular, interleaved power converters was presented. Advantages and challenges of interleaved power converters were explained in brief. The objectives of this thesis work are defined in mitigating those challenges. The next chapter discusses the state of the art in implementing interleaved power converters.

CHAPTER ONE

1. BACKGROUND AND LITERATURE REVIEW

1.1. Introduction to Power Converter

All power converters use power electronic devices, such as IGBT and MOSFET, being operated in their saturation and cutoff region so that they can act as a switch. This makes the control of current flow through the switches more convenient than operating them in their linear region [6]. Depending on how the power circuit is configured and how the modulation signals are generated, the power converter may act as DC/DC, AC/DC or DC/AC. There are many different strategies of achieving appropriate switching signals for the converters. Pulse width modulation (PWM) is one of the most widely used strategy applicable to any type of power converter. PWM works by comparing a lower frequency reference signal with a high frequency waves of type sawtooth or triangular. As triangular waves have both peaks and valleys, they add more flexibility in their digital implementation. The frequency of the triangular wave (also called carrier signal) is called switching frequency. The main advantage of these PWM modulation techniques is that the resulting harmonics occur at multiples of the switching frequency leading to smaller filter requirements.

In DC/DC converters the reference is usually constant DC value while in DC/AC it is sinusoidal reference. In both cases, whenever the reference is higher than the carrier, the output (switching pulse) becomes high and when the reference signal is lower than the carrier, the switching pulse gets low. The switching pulse is then fed to the switching device's gate driver circuit. Depending on how the reference is updated, PWM techniques can be divided in to naturally sampled, symmetrically sampled and asymmetrically sampled [6, 7]. For naturally sampled PWM techniques, the instantaneous value of the reference signal is compared with the triangular carrier. This needs finding the intersection of the reference and the carrier signal which makes it impossible to implement it digitally for continuously varying reference signal [7]. It may also cause multiple switching per one period of carrier signal if the reference is changing fast which may result damage to switching devices. The symmetrically sampled PWM, on the other hand, samples the reference at the peak of the carrier and holds it over the switching period. In a similar way, asymmetrical sampling samples the reference at each half period of carrier signal; at the peak and valley. As updating of PWM reference is carried out at the peak or valley of the carrier signal, both symmetrical and asymmetrical sampling do not result multiple switching. Most of commonly available DSPs, such as TI F28069, have such

capability. Fig 1.1 (as reprinted from [6]) shows the switching instances in the three types of PWM. More frequent update of PWM reference implies less delay in the system, and as a result, better system performance. This favors asymmetrical sampling as a better option as far as a capable DSP is available [8].

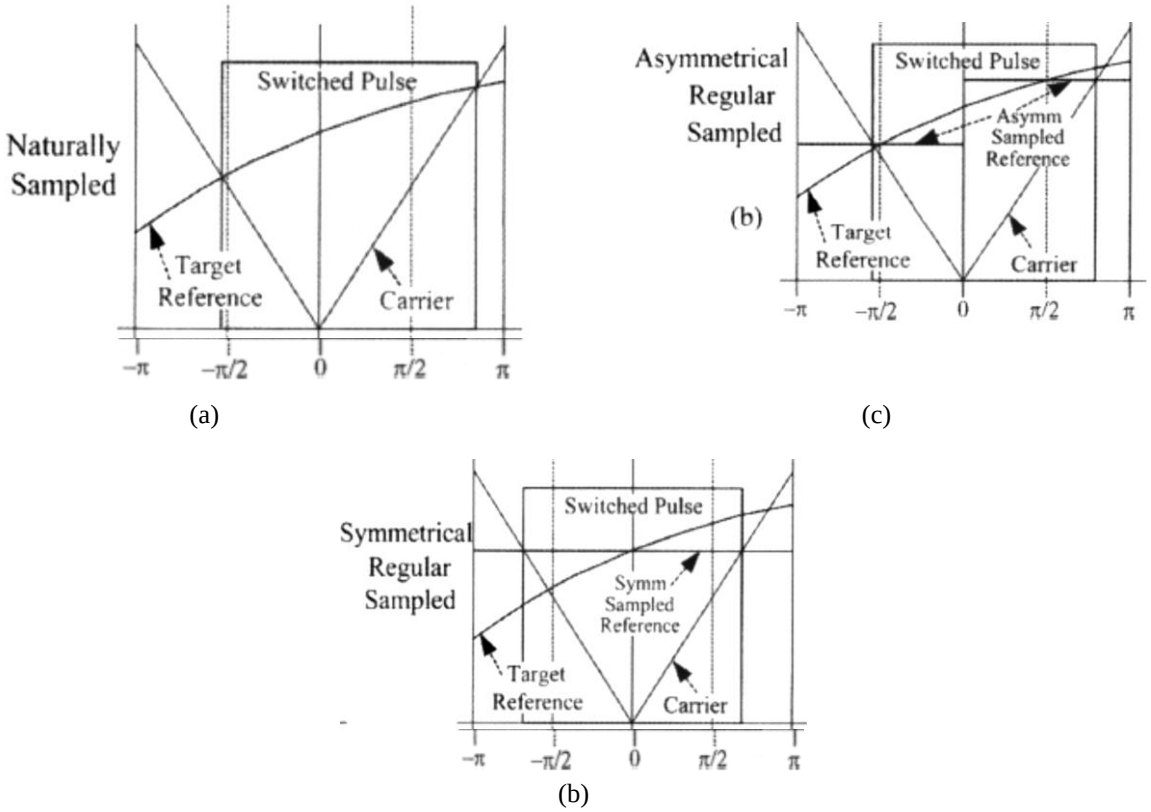


Fig 1.1 Different techniques of sampling applied to triangular carrier PWM: a) naturally sampled; b) symmetrically sampled; c) asymmetrically sampled (reprinted from [6])

1.2. Characteristics of Interleaved Power Converters

Interleaved power converter consists of a number of smaller modules, also called channels, connected in parallel having their switching signals phase shifted from each other over a switching interval [1]. This can be implemented by phase shifting the carrier signals of PWM. Because of the phase shift in the switching signals of each channel, some of the harmonics in the output current will cancel each other and the equivalent ripple frequency will increase proportional to the number of channels [5], [9]. As a result, the size of filter required to handle the resultant harmonics will decrease significantly. This increases the system efficiency and power density [1] [10], [11]. Interleaving has also additional advantages such as better dynamic response (due to higher equivalent frequency), better power quality (due to reduced input/output current/voltage ripples) and better reliability (due to parallel redundancy) [3], [9].

1.3. The Need to Control Circulating Currents

Connecting two or more converters in parallel needs appropriate control to avoid the possible circulation current. Circulation current can be caused by the difference in pole voltage of channels or mismatch of the passive elements between channels [5, 7]. Applying interleaved PWM results a high frequency differential mode voltages between corresponding channels of different converters. The difference in channel currents may not be a problem if uncoupled inductors are used. However, the differential currents become magnetizing currents when coupled inductors are used. Hence, high circulation current means high magnetizing current which may result saturation of coupled inductors. In addition to interleaving, the unbalance in the hardware and control part of the converter may result in unbalanced currents flowing in each channel causing more ripples which leads to more loss and saturation of passive elements [12]. The circulating currents contain both high frequency and low frequency components [13]. The high frequency components could be handled with passive current sharing methods while low frequency components need active methods such as digital controllers [14]. Because of these circulation currents, interleaved converters need a closed loop controller so that each channel can have balanced current and minimized circulation current.

Both linear and non-linear digital controllers can be applied in interleaved power converters. Different literatures presented different controllers, such as proportional integral (PI), hysteresis, resonant, repetitive [5], deadbeat [15], stepping on time[16], backstepping [17] and zero-crossing ripple detection [18], to minimize circulating currents in interleaved power converters. Although hysteresis control is simplest one to implement on digital platforms, it results in variable switching frequency which makes the filter design very complex [6, 7]. Deadbeat control is the fastest control which is based on the discrete modeling of a system. Their drawbacks are their limited capability of compensation for dead band between switches of same leg which is the case in all bidirectional converters. Other controllers such as resonant, repetitive, back stepping needs more computational algorithms. PI controller is a simplest controller which can be applied to any converter. Although they are much slower than deadbeat controllers, they are good in compensating the effect of dead band. Stationary and synchronous frame controllers can also be used while dealing with three phase power converters. The intension of this thesis work is not to investigate optimal control system. It rather focuses on easy and simple implementation of interleaved converters. Simple PI controllers will be considered for implementation of the control system and design of improved control system will be the continuation of this work.

1.4. Interleaving Techniques for DC/DC Converters

Different approaches of interleaving and methods of handling the circulating currents and current mismatches in DC/DC converters are considered in literatures. The advantage of interleaving DC/DC converters can be seen from Fig 1.2. As it can be seen from Fig 1.*2-a*, increasing the number of channels results a total harmonic cancelation at certain duty ratio. A 4-channel converter, for example, will have a total harmonic cancelation at duty ratio of 0.25, 0.5 and 0.75. Fig 1.2-b shows a typical channel current waveforms of a 2-channel converter in comparison with the total input current. These waveforms are based on independent inductors. The phase shift between channel currents is equal to the phase shift between their PWM carrier signals. As it can be seen from the figure, the ripple in the total current (i_{in}) has higher frequency and lower amplitude than each of the channel currents (i_{ch1} and i_{ch2}). It can be easily seen that the channel currents are independent of each other [19]. Fig 1.2-c, on the other hand, shows the channel currents and their total current wave forms for a similar 2-channel interleaved DC/DC converter except highly coupled inductors are used in this case. As it can be seen from the figure, the channel currents are no more independent. Although the channel currents are still phase shifted each other resulting in a higher frequency of current ripple in the output current, they are not contributing much in the reduction of total ripple as independent inductors do. Regardless of this, coupled inductors have better advantage because of the cancelation of dc flux component when they are coupled in opposite direction [4]. This helps in achieving lower volume of inductors while designing them.

Depending on the type of coupling used, the sampling method to be applied in closed loop system also varies. For independent inductors as shown in Fig 1.2-b, sample taken at mid pint of the switching period is equal to the average value of the current wave form. This could be easily achieved by synchronizing PWM and analog to digital converter (ADC) of each channel in the DSP. This is not true for coupled inductors. The sample taken at the midpoint of switching period for each channel doesn't match to the average current.

Different digital controllers, such as repetitive [5], deadbeat [15], stepping on time[16], backstepping [17] and zero-crossing ripple detection [18], are proposed to minimize circulating currents in DC/DC converters. Additional researches are reported on the use of different magnetic coupling techniques such as inter-cell transformer, multiple leg core and multistage coupling together with their associated EMI filter design considerations [5], [19]-[23]. Fig 1.3 shows an example of 8-channel interleaved DC/DC converter using coupled inductors designed in four stages to minimize circulating currents and ripples.

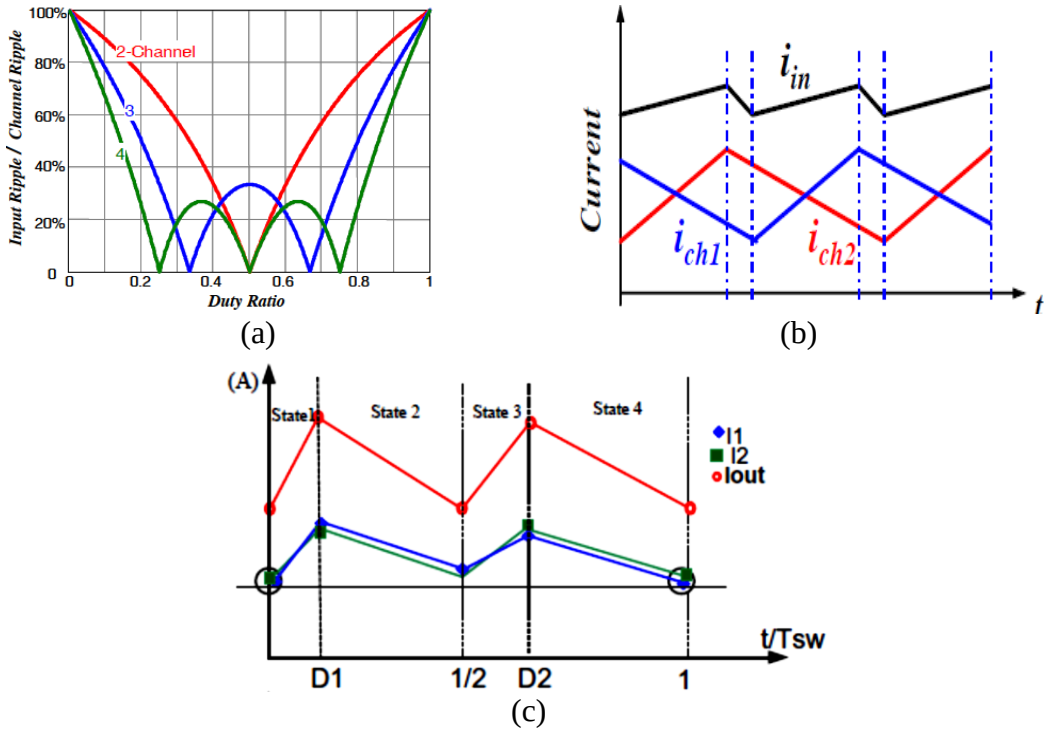


Fig 1.2 Characteristics of interleaved DC/DC converter: a) ripple content as a function of duty ratio and number of channels; b) channel currents and total input current for 2-channel converter with independent inductor (reprinted from [19]); c) channel current and total output current of 2-channel converter with coupled inductors (reprinted from [22])

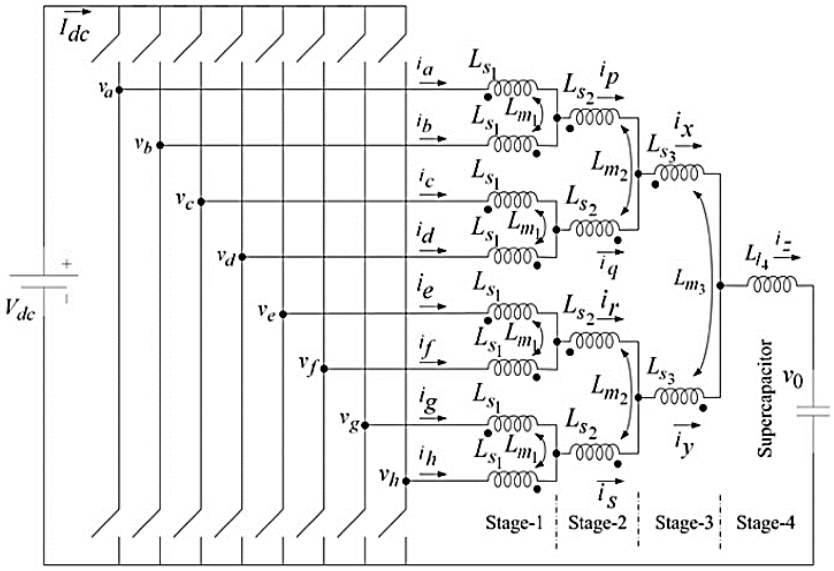


Fig 1.3 Eight channel four-stage interleaved DC/DC converter (reprinted from [5])

1.5. Interleaving Techniques for DC/AC and AC/DC Converters

There are different topologies of DC/AC and AC/DC converters both single phase and three phase. An example of a 6-channel three phase interleaved inverter is shown in Fig 1.4. All

channels share the same DC bus and LC filter (with damping resistor). Independent inductors are used in each channel to limit harmonics and circulating current [1]. The principle of operation is similar to DC/DC converters, except in this case the reference signals are varying at fundamental frequency rather than being constant. A typical waveform showing total phase current and individual channel current for a 3-channel interleaved single phase inverter is shown in Fig 1.5. Channel currents I_{a1}, I_{a2} and I_{a3} are phase shifted each other by 120^0 (i.e. T_a) over the switching period T_s. The total phase current (I_a) which is the sum of the channel currents shows less ripple occurring at higher frequencies than channel currents. As it is discussed for DC/DC converters, the inductors to be used in these topologies can also be either independent or magnetically coupled. The issue of circulation current is also an issue here due to differences in pole voltages and errors in the digital implementations (including sampling techniques) may result more ripples and circulating currents [7].

Different digital control systems are proposed for DC/AC converters, such as resonant control [11], repetitive control with phase-lag compensation and passive damping [3], [24]-[27]. A deadbeat controller with repetitive controller is proposed in [28] to mitigate the effect of quantization and computational delays in multi-phase interleaved inverter. The circulating current can be decomposed into high frequency part (to be controlled through coupling inductors) and low frequency part (to be controlled by *d-q-0* controller for each converter) [2]. A similar technique is used in [28] for MW-level grid connected inverter for wind power generation application.

Different passive methods of balancing channel currents, such as, choke inductors [29], current sharing circuits [13], [14] and magnetically coupled interleaving [30] are reported in literatures. These techniques require additional circuitry and algorithms to control them. Interleaved DC/AC converters made from GaN power FET for battery charging and propulsion of an all-electric boat is presented in [31] where coupling inductors (also called interphase transformers) are used for current sharing. GaN power FET is recent development which could be costly. Influence of continuous and discontinuous PWM schemes on the design of coupled inductors used to suppress circulating current in interleaved inverters is discussed in [32]. Line filter design methodology is presented in [10] where two voltage source converters are interleaved for high power wind energy system using a discontinuous PWM technique. The use discontinuous PWM adds complexity into the digital control implementation.

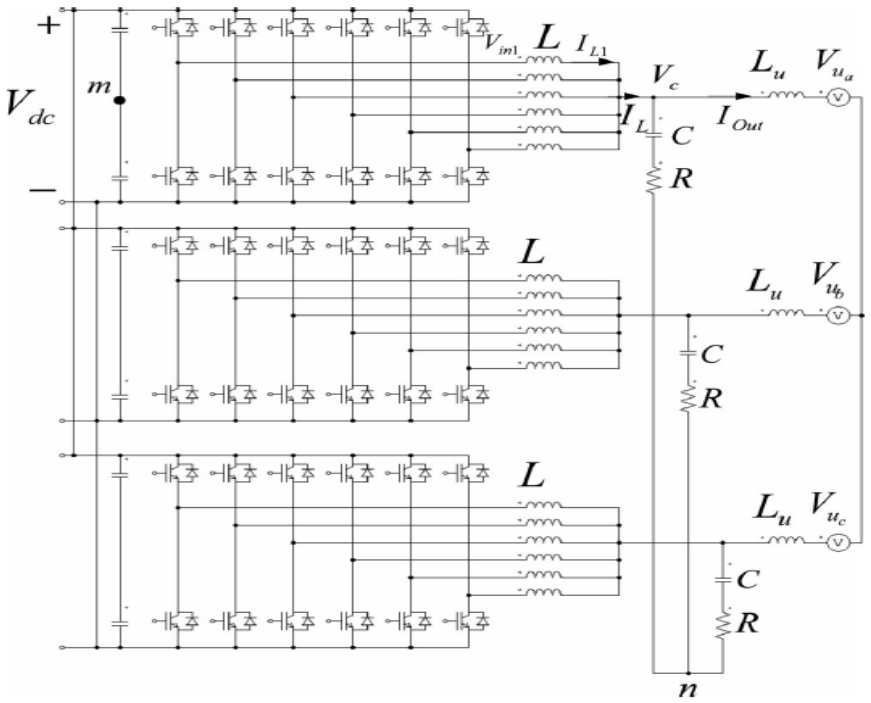


Fig 1.4 Three phase six-channel interleaved inverter (reprinted from [1])

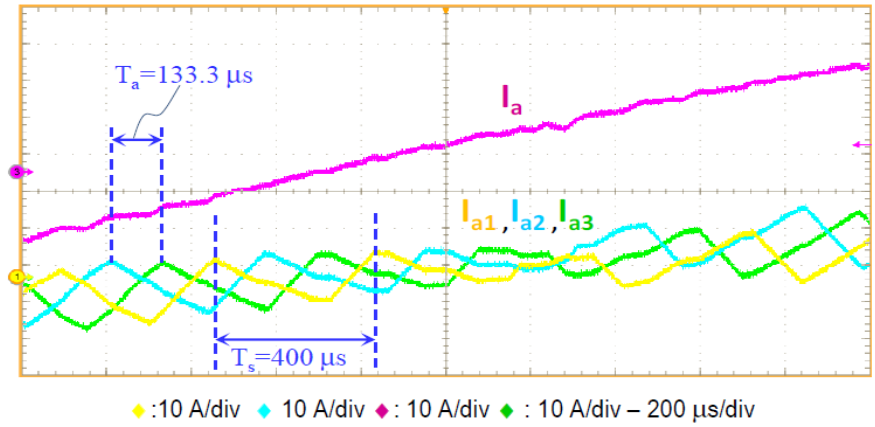


Fig. 1.5 Total and channel currents for a 3-channel interleaved inverter (reprinted from [2])

1.6. Asymetrical Interleaving and Sampling Effects

All the previous discussion is based on symmetrical interleaving in which the carrier signals of each channel are phase shifted by equal angles over a switching period. The effect of asymmetrical interleaving on current ripples and common mode noise is studied for multichannel power factor correction application in [19] and [33]. It shows that by properly selecting the number of channel and switching frequencies with optimal interleaving angle, a better efficiency and reduced size of electromagnetic interference filter can be achieved [19]. The effect of different sampling techniques, such as natural sampling, multi-rate sampling and

high frequency sampling, are analyzed in [34] together with variation of interleaving angle. Accordingly, an optimal interleaving angle is proposed for interleaved inverter depending on the available PWM sampling frequency [34]. However, the optimal interleaving angles lies around the symmetrical interleaving angles, unless selective harmonic elimination is required. In a similar way, natural sampling, symmetrical regular sampling and asymmetrical regular sampling techniques are compared in [35] using carrier based PWM for multi-phase AC machine drive application.

Optimal interleaving angle of parallel grid connected converters as a function of modulation index is discussed in [35] and [36]. In [8], it is indicated that double edge asymmetric regularly sampled carrier based PWM is better as compared to other sampling techniques. Although increasing the sampling frequency as a multiples of carrier frequency has an advantage of improving the systems dynamics by decreasing the PWM updating delay, it is challenging to implement it with ordinary DSP [6] and it may result multiple switching per a single switching period unless the switching device is designed accordingly.

All the above sampling techniques refers to how the PWM updates its reference inside the PWM module. The sampling of current in the feedback loop can also be done in the same way to get average of channel current if independent inductors are used. However, in case of coupled inductors, this doesn't work, and hence, it needs a different strategy. In this thesis, sampling the channel current at higher frequency and averaging them over a switching period is proposed while maintaining asymmetrically sampled PWM.

1.7. Digital Implementation of Interleaved Power Converters

Different methods of implementing current controllers using DSP are reported in literatures. One method of handling this challenge by use of multiple DSP units with communication link through controller area network (CAN) is proposed in [1], [3] and [24] and [26]. Use of advanced field-programmable gate array (FPGA) to handle such high frequency sampling are reported in [2], [13], [20] and [31]. Both of these methods are a bit complex and need additional hardware which increases their cost. In this thesis, a simple TI F28069 DSP will be used to implement the proposed control system.

1.8. Summary

In this chapter, literature review is made regarding different approaches of implementing interleaved power converters. Some of the literatures proposed use of additional circuitry to balance channel currents while others consider advanced controllers together with FPGA to

implement multi-channel interleaved power converters. Only few studies considered the effect of sampling and asymmetrical interleaving. In this thesis inductor size comparison between different topologies is presented and simpler control algorithm is developed and which can balance channel currents and reduce sampling errors. The next chapter describes different models of interleaved power converters both using coupled and uncoupled inductors. Inductor volume comparison for a given output current ripple is also presented.

CHAPTER TWO

2. PROPOSED METHODOLOGY: STEADY STATE MODELING

2.1. Introduction

There are a number of ways in which DC/DC and DC/AC power converters can be realized. Selected topologies will be considered in this thesis and they will be compared from filter size reduction point of view. The analysis for DC/AC follows exactly similar approach as DC/DC except that there is little difference on the circuit configuration and reference inputs. Analyzing a DC/DC power converter for the worst case scenario in terms of harmonics, which is a function of duty cycle, is equivalent to analyzing the worst case scenario of DC/AC which operates for sinusoidal range of duty cycles. Considering this fact, deeper analysis of topologies is done for only interleaved DC/DC converters. Topologies with both coupled and uncoupled inductors are modeled, analyzed and compared each other. Four types of topologies are considered: using uncoupled inductors, using circular inter-cell transformer, using single stage pair coupling and using multi-stage pair coupling. In all these cases, the number of channels considered is four and symmetrical interleaving (equal phase shift between each channel) is assumed. After selecting a better topology, different sampling techniques are studied.

2.2. DC/DC Converter Using Uncoupled Inductors

The first and most straightforward topology is one which uses uncoupled inductors for each channel together with additional common mode inductor. The converter consists of a dc voltage source connected to four parallel legs on which the eight bidirectional switches (S_1 to S_8) are arranged as shown in Fig 2.1.

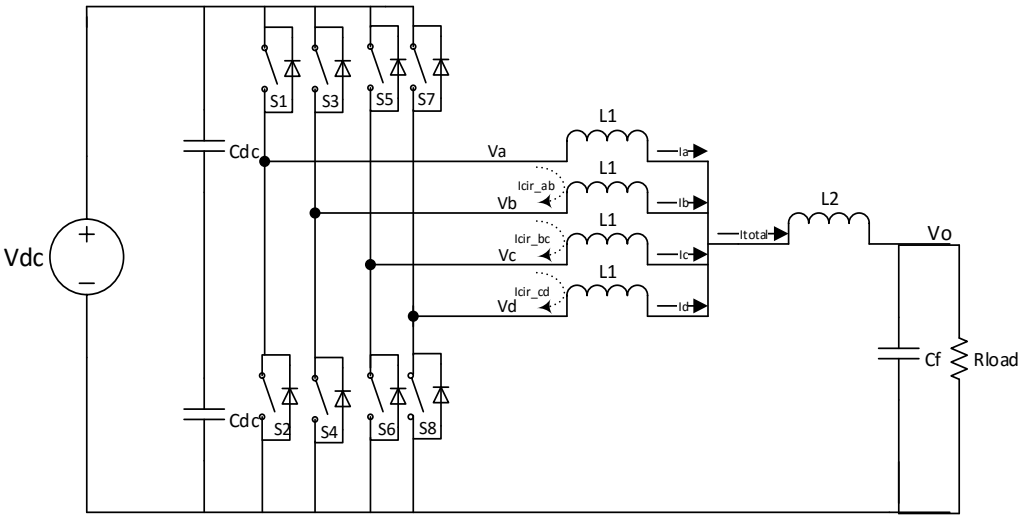


Fig 2.1 Four channel interleaved DC/DC converter using uncoupled inductors

A single or series of capacitors (C_{dc}) are always put in parallel with the dc voltage source to suppress current ripples propagating into the source. The modulation signal for switches S1 and S_2 are generated in such a way that whenever S_1 is ON for a given duty cycle, S_2 is OFF. The same principle applies for S_3&S_4, S_5&S_6 and S_7&S_8. Voltage levels V_a, V_b, V_c and V_d represent the voltage of corresponding channel relative to the negative end of dc voltage source. When the upper switch of any leg is ON, the corresponding channel voltage will be connected to V_{dc} and when it is OFF (lower switch being ON), the channel is connected to 0V. The currents, I_a, I_b, I_c and I_d represent the channel currents while I_{cir_ab}, I_{cir_bc} and I_{cir_cd} represent circulating currents between first and second channel, second and third and third and fourth channels respectively. Although these are the one indicated on Fig 2.1, there are also circulating currents between every pair of channels. Those are omitted for the sake of clarity on the figure. The series inductors for each channel (L_1) are assumed to be similar, which is not the case in reality. Additional series inductor (L_2) is connected to filter out the remaining harmonics. The total current is designated by I_{total}. C_f represents filter capacitor while a resistive load R_{load} is connected at the output. The output voltage is labeled as V_o. Symmetrical interleaving with a 90^0 phase shift ($360^0/4$) between the switching signals of the phases is considered in the forthcoming analysis.

This gives four intervals over one switching period at which different channel combinations will be connected to V_{dc} depending on the duty cycle (d). Fig 2.2 shows the switching pulses (gate signals) of the upper leg switches (*G1* fo channel1, *G*2 for channel2, *G3* for channel3 and *G*4 for channel4). Considering Fig 2.2 (b), for example, it can be seen that the first channel is connected to V_{dc} at time instant ($t/T_s = 0$) and holds in that position until time instant ($t/T_s = d$). T_s represents the switching period. Similarly, second channel is connected to V_{dc} at time instant (t/T_s = 0.25) and continues in that position until time instant ($t/T_s = (0.25+ d)$). The same principle applies for the remaining channels too. Thus, it is always useful to know the status of each channel at a particular instant of time. This is applied later after deriving the expression relating channel current and pole voltages of each channel.

By referring Fig 2.1, the differential equations relating the channel currents and voltages are derived as follows:

$$V_a = L_1 \frac{dI_a}{dt} + L_2 \frac{d(I_{total})}{dt} + V_o \quad (2.1)$$

$$V_b = L_1 \frac{dI_b}{dt} + L_2 \frac{d(I_{total})}{dt} + V_o \quad (2.2)$$

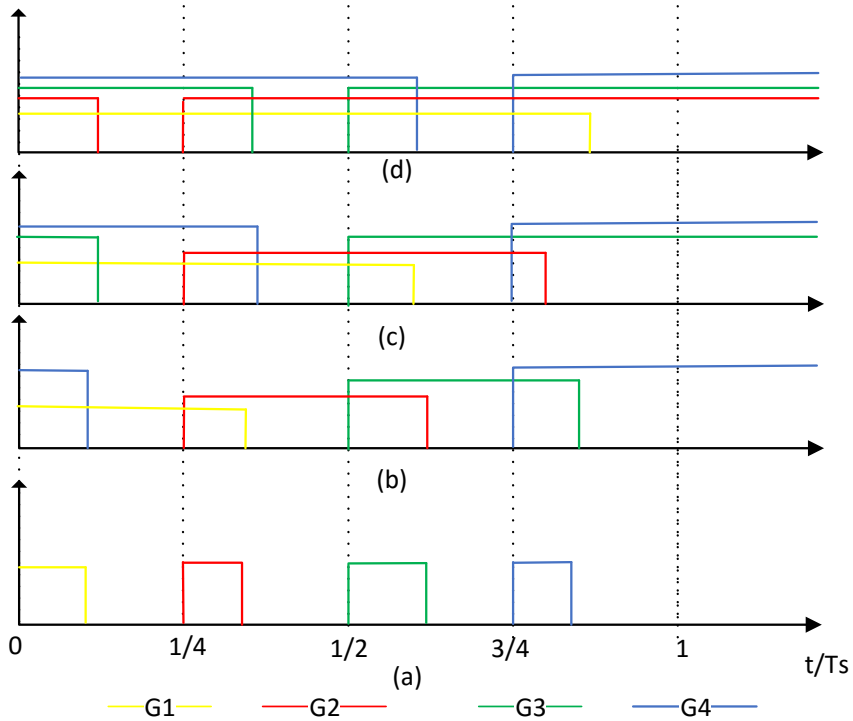


Fig 2.2 Switching instances of symmetrically interleaved four channel interleaved converter for different duty cycle ranges: (a) $0 \leq d \leq 0.25$; (b) $0.25 \leq d \leq 0.5$; (c) $0.5 \leq d \leq 0.75$; (d) $0.75 \leq d \leq 1$

$$V_c = L_1 \frac{dI_c}{dt} + L_2 \frac{d(I_{total})}{dt} + V_o \quad (2.3)$$

$$V_d = L_1 \frac{dI_d}{dt} + L_2 \frac{d(I_{total})}{dt} + V_o \quad (2.4)$$

$$I_{total} = I_a + I_b + I_c + I_d \quad (2.5)$$

Because of the phase shift between the switching signals, any pair of channels experiences a high frequency differential voltages which causes circulation currents from the channel connected to V_{dc} to the other channel connected to 0V. It is relatively direct to analytically represent circulation currents for a two channel converter, rather than a multichannel converter. In a two channel converter, the current flowing through one channels can be assumed to be equal to half of the output current plus the circulating current, while the other channel having current equal to half of the output current minus the circulation current. According to this definition,

$$I_{cir\_ab} = \frac{1}{2}(I_a - I_b) \quad (2.6)$$

This holds true only for ideal conditions in which all passive elements are similar. If there are mismatches between passive elements, it is usual to have differences in the channel currents

even if both channels are switched *ON* or *OFF* simultaneously. But, this doesn't mean that there is circulating current. Increasing the number of channels increases the complexity more as one channel could be connected to V_{dc} (*ON*) at some instants while others are connected to 0V (*OFF)* which technically means that all the circulating current is coming from one channel. In this case, taking the difference between two channel currents may hide the true picture of circulating current.

However, as interleaved power converters are supposed to share currents equally, the average current in each channel is supposed to be equal and the ripples should be optimized so that instantaneous differences between two channel currents always remain within the limit.

By rearranging equations (2.1) to (2.2), the current difference between any two channels can be given by:

$$\frac{d(I_x - I_y)}{dt} = \frac{V_x - V_y}{L_1} \tag{2.7}$$

where *x, y =a, b, c, d, x≠y*.

Similarly the rate of change of output current is found to be:

$$\frac{dI_{total}}{dt} = \frac{V_a + V_b + V_c + V_d - 4V_o}{L_1 + 4L_2} \tag{2.8}$$

Taking further arithmetic manipulation,

$$\begin{bmatrix} \frac{dI_a}{dt} \\ \frac{dI_b}{dt} \\ \frac{dI_c}{dt} \\ \frac{dI_d}{dt} \end{bmatrix} = \begin{bmatrix} N_o & N_1 & N_1 & N_1 & N_2 \\ N_1 & N_o & N_1 & N_1 & N_2 \\ N_1 & N_1 & N_o & N_1 & N_2 \\ N_1 & N_1 & N_1 & N_o & N_2 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \\ V_o \end{bmatrix} \tag{2.9}$$

where $N_o = \frac{3}{4L_1} + \frac{1}{4(L_1+4L_2)}$ $N_1 = \frac{-1}{4L_1} + \frac{1}{4(L_1+4L_2)}$ $N_2 = \frac{-1}{(L_1+4L_2)}$

The change in each channel current, ΔI_x, for a given interval of time, Δt, can be found by referring Fig 2.2 together with equation (2.9).

$$\Delta I_x = \frac{dI_x}{dt}\Delta t \tag{2.10}$$

For example, considering first channel, the current wave form for a duty cycle $0 \leq d \leq 0.25$ looks like as shown in Fig 2.3. *Slope1*, *Slope2* and *So* represents the $\frac{dI_a}{dt}$ values in those

corresponding intervals. Their value are derived by referring equation (2.9). Assuming, $V_o = d * V_{dc}$ at steady state, the slopes can be defined as shown in equation (2.11);

$$slope1 = V_{dc}(N_o + dN_2) \quad (2.11a)$$

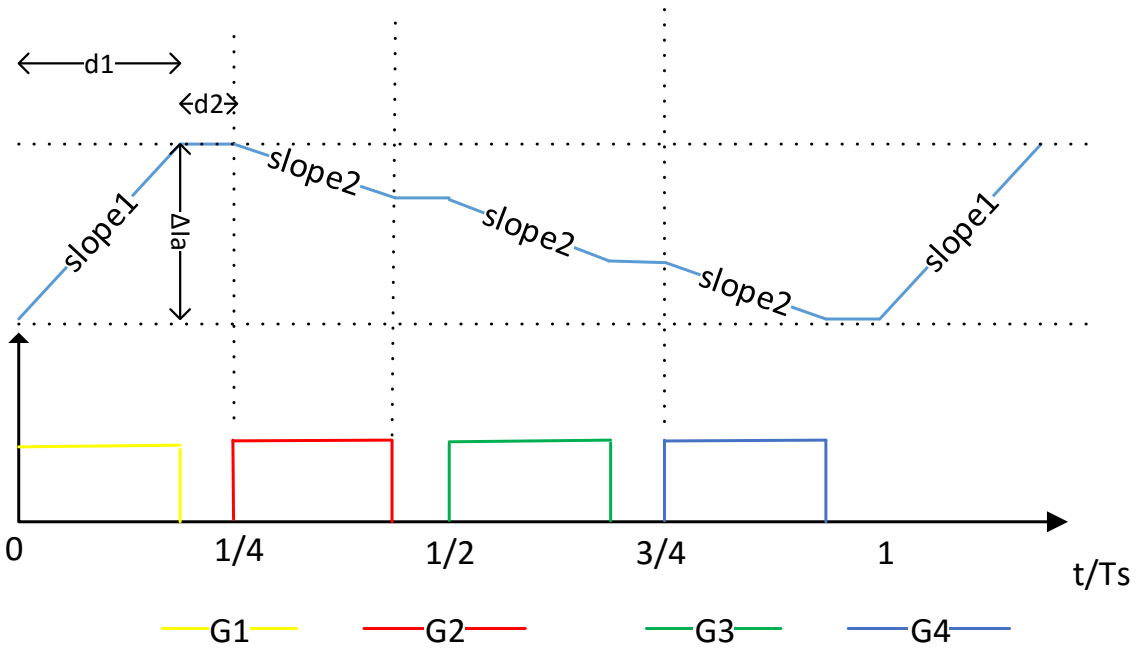


Fig 2.3 Channel current ripples for duty cycle range $0 \leq d \leq 0.25$; d1 = dT_s, $d2$ =

$$slope2 = V_{dc}(N_1 + dN_2) \quad (2.11b)$$

$$So = V_{dc}(N_2) \quad (2.11c)$$

It can be seen from Fig 2.3 that the peak to peak current can be given

$$\Delta I_a = V_{dc}T_s(N_2d^2 + N_0d) \qquad \text{for } 0 \leq d \leq 0.25 \quad (2.12a)$$

Following similar procedure, the ripple currents can be estimated for the remaining duty cycle ranges: $0 \leq d \leq 0.25$, $0.25 \leq d \leq 0.5$, $0.5 \leq d \leq 0.75$ and $0.75 \leq d \leq 1$ as follows:

$$\Delta I_a = V_{dc}T_s(N_2d^2 + (N_0 + 2N_1)d - 0.5N_1) \qquad \text{for } 0.25 \leq d \leq 0.5 \quad (2.12b)$$

$$\Delta I_a = V_{dc}T_s(N_2d^2 + (N_0 + 4N_1)d - 1.5N_1) \qquad \text{for } 0.5 \leq d \leq 0.75 \quad (2.12c)$$

$$\Delta I_a = V_{dc}T_s(N_2d^2 + (N_0 + 6N_1)d - 3N_1) \qquad \text{for } 0.75 \leq d \leq 1 \quad (2.12d)$$

The possible local maximum peak to peak values in each interval can be evaluated by solving each of the quadratic equations in (2.12) over the corresponding interval. The absolute maxima occurs at a duty cycle of d = 0.5 and is given by the following equation.

$$\Delta I_{a\_max} = \frac{V_{dc}T_s}{4L_1} \quad (2.13)$$

Equation (2.13) is used in the selection of inductance for a give maximum peak to peak ripple current in each channel. The total current from equation (2.8) can be solved together with Fig 2.2 to know the maximum ripple in the output current which in turn is used to determine the value of L_2. Equation (2.14) describes the peak to peak ripples in the output current for different duty ranges.

$$\Delta I_{total} = \frac{V_{dc}T_s}{L_1+4L_2}(1-4d)d \quad \text{for } 0 \le d \le 0.25 \quad (2.14a)$$

$$\Delta I_{total} = \frac{V_{dc}T_s}{L_1+4L_2}(2-4d)(d-0.25) \quad \text{for } 0.25 \le d \le 0.5 \quad (2.14b)$$

$$\Delta I_{total} = \frac{V_{dc}T_s}{L_1+4L_2}(3-4d)(d-0.5) \quad \text{for } 0.5 \le d \le 0.75 \quad (2.14c)$$

$$\Delta I_{total} = \frac{V_{dc}T_s}{L_1+4L_2}(4-4d)(d-0.75) \quad \text{for } 0.75 \le d \le 1 \quad (2.14d)$$

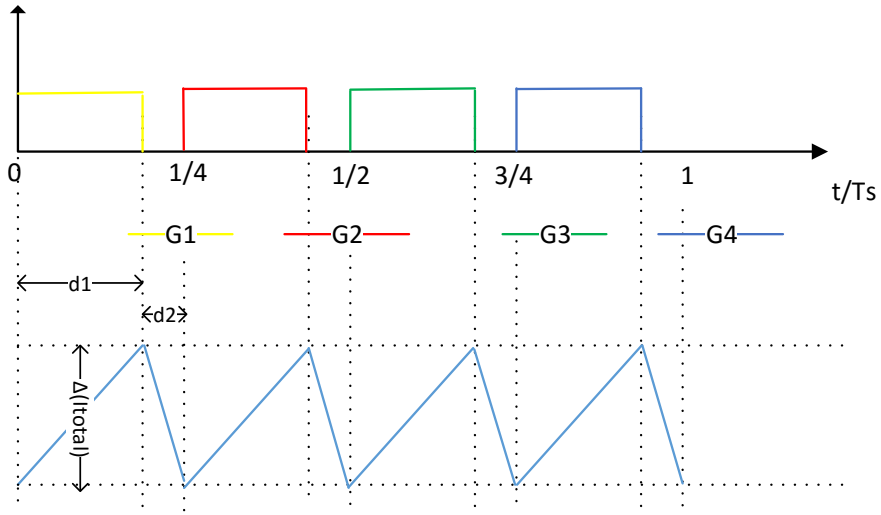


Fig 2.4 Total current ripples for duty cycle range $0 \le d \le 0.25$; d1 = dT_s, *d2 = Ts(0.25 -d)* and ΔI_{total} represents maximum peak to peak ripple (Uncoupled Inductors)

Fig 2.4 shows the ripple waveforms of output current. Its frequency is four times of the switching frequency. The maximum peak to peak ripple is found from equations (2.14) and occurs at a duty cycle equal to midpoint of each interval (i.e. at 1/8, 3/8, 5/8 and 7/8). Equation (2.15) shows the maximum ripple as a function of switching period and inductance values. It clearly shows that the total output current ripple is limited only by leakage inductances of those coupled inductors (L_1) and the inductance of common mode inductor (L_2).

$$\Delta_{max}(I_{total}) = \frac{V_{dc}T_s}{16(L_1+4L_2)} \quad (2.15)$$

As discussed before, the differential current between two channels is mainly caused by differences in the switching instance. The more phase shift between PWM signals of two channels, the more differential current between the two channels. If all passive elements in the converter are exactly similar, the differential current becomes proportional to the circulating current. For the four channel topology, channels with 0^0 and 180^0 or 90^0 and 270^0 have larger phase shift than the remaining combinations. By referring equation (2.7), the differential current between channels with 0^0 and 180^0 can be written as:

$$\frac{d(I_a-I_c)}{dt} = \frac{V_a-V_c}{L_1} \quad (2.17)$$

Again by referring Fig 2.2, the peak to peak value of the differential current obtained as follows:

$$\Delta(I_a - I_c) = \frac{V_{dc}T_s d}{L_1} \quad \text{for } 0 \le d \le 0.25 \quad (2.18a)$$

$$\Delta(I_a - I_c) = \frac{V_{dc}T_s d}{L_1} \quad \text{for } 0.25 \le d \le 0.5 \quad (2.18b)$$

$$\Delta(I_a - I_c) = \frac{V_{dc}T_s(1-d)}{L_1} \text{ for } 0.5 \le d \le 0.75 \quad (2.18c)$$

$$\Delta(I_a - I_c) = \frac{V_{dc}T_s(1-d)}{L_1} \text{ for } 0.75 \le d \le 1 \quad (2.18d)$$

The maximum, differential current occurs at a duty of 0.5, and is given by:

$$\Delta_{max}(I_a - I_c) = \frac{V_{dc}T_s}{2L_1} \quad (2.19)$$

It should be noted that using the above method, the maximum differential current between channels having a phase difference of 90^0 (for example, I_a *and* I_b) is given by

$$\Delta_{max}(I_a - I_b) = \frac{V_{dc}T_s}{4L_1} \quad (2.20)$$

2.3. DC/DC Converter Using Coupled Inductors: Circular Inter-cell transformers

Although uncoupled inductors are simple to analyze and relatively easier to control, they are not optimal solution from inductor size point of view. The size of inductor is roughly proportional to the product of both loading and magnetizing currents, as it will be discussed later. Thus, reducing either of the loading current or magnetizing current for a given value of inductance contributes a lot in reducing the total volume of the inductor. One of such method is to couple the inductors in opposite direction so that the net magnetizing current is reduced.

There are many different ways of using coupled inductors. Use of ladder structure as a core is studied in [20] while coupling each phase with the rest of phases using multiple transformers per channel is described in [30]. In both cases, the current unbalance could be highly reduced and hence lower circulating current could be achieved. However, the equivalent volume of the inductors increases and the modeling becomes more complex as the number of channels increases. In this thesis, coupled inductors in the form of circular inter-cell transformers is discussed here and a multi-stage approach is presented later.

Fig 2.5 shows a 4-channel interleaved DC/DC converter with inter-cell transformers between each pair of channels. A total of four inter-cell transformers are used to form circular coupling. Each inter-cell transformer is associated with a leakage inductance of L_1 on both sides and a magnetizing inductance of l_{m1}. Other parameters are similar to a converter with uncoupled inductors as discussed in the previous section. The analysis starts by defining the differential equations describing the voltages and currents for each channel in relation to the output voltage.

$$V_a = 2L_1 \frac{dI_a}{dt} + l_{m1} \frac{d(2I_a - I_b - I_d)}{dt} + L_2 \frac{dI_{total}}{dt} + V_o \quad (2.21a)$$

$$V_b = 2L_1 \frac{dI_b}{dt} + l_{m1} \frac{d(2I_b - I_c - I_a)}{dt} + L_2 \frac{dI_{total}}{dt} + V_o \quad (2.21b)$$

$$V_c = 2L_1 \frac{dI_c}{dt} + l_{m1} \frac{d(2I_c - I_b - I_d)}{dt} + L_2 \frac{dI_{total}}{dt} + V_o \quad (2.21c)$$

$$V_d = 2L_1 \frac{dI_d}{dt} + l_{m1} \frac{d(2I_d - I_c - I_a)}{dt} + L_2 \frac{dI_{total}}{dt} + V_o \quad (2.21d)$$

$$I_{total} = I_a + I_b + I_c + I_d \quad (2.21e)$$

By rearranging and doing further arithmetic operations on equations (2.21):

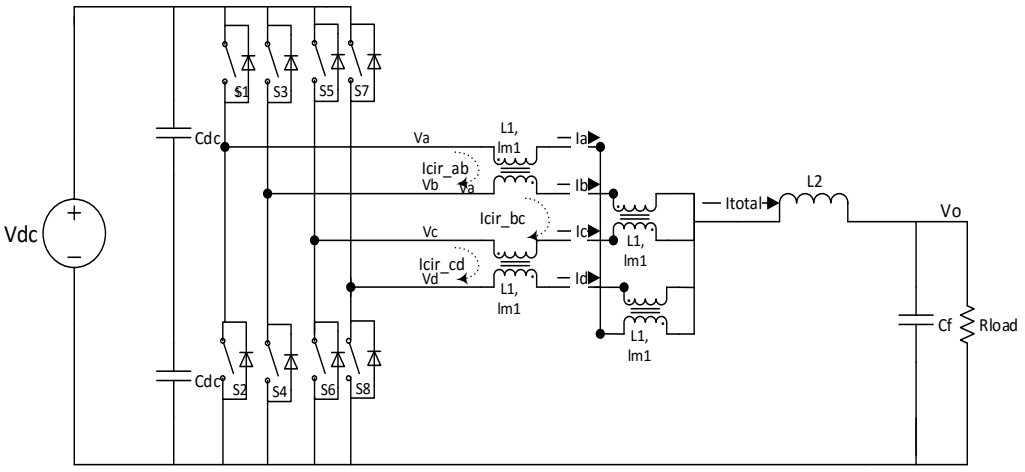


Fig 2.5 Four channel interleaved DC/DC converter using inter-cell transformers

$$\frac{dI_{total}}{dt} = \frac{V_a+V_b+V_c+V_d-4V_o}{2L_1+4L_2} \quad (2.22)$$

$$\frac{d(I_a-I_b)}{dt} = N_o(V_a-V_b) + N_1(V_d-V_c) \quad (2.23)$$

where $N_o = \frac{1}{4}\left(\frac{1}{L_1+l_{m1}} + \frac{1}{L_1+2l_{m1}}\right)$; $N_1 = \frac{1}{4}\left(\frac{1}{L_1+l_{m1}} - \frac{1}{L_1+2l_{m1}}\right)$

As it can be seen from equation (2.23), the differential current between two channels is affected by the status of other channels due to the circular coupling. Following similar procedures for the remaining channels, the following matrix representation for differential currents is found.

$$\begin{bmatrix} \frac{d(I_a-I_b)}{dt} \\ \frac{d(I_b-I_c)}{dt} \\ \frac{d(I_c-I_d)}{dt} \\ \frac{d(I_d-I_a)}{dt} \end{bmatrix} = \begin{bmatrix} N_o & -N_0 & -N_1 & N_1 \\ N_1 & N_o & -N_0 & -N_1 \\ -N_1 & N_1 & N_o & -N_0 \\ -N_0 & -N_1 & N_1 & N_o \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \end{bmatrix} \quad (2.24)$$

The peak to peak differential current between one pair of channels is derived using Fig 2.2 and equation (2.24). Fig 2.6 shows the differential current ripple wave form for $0 \leq d \leq 0.25$ where slope1, and slope2 represent the rate of change of the differential current in each time interval. They are given by: $slope1 = V_{dc}N_o$ *and* $slope2 = V_{dc}N_1$. A similar drawing can also be obtained for all duty ranges. Equation (2.25) summarizes the expression of peak to peak differential currents for different duty cycle ranges.

$$\Delta(I_a - I_b) = V_{dc}T_s d(N_o + N_1) \qquad \text{for } 0 \leq d \leq 0.25 \quad (2.25a)$$

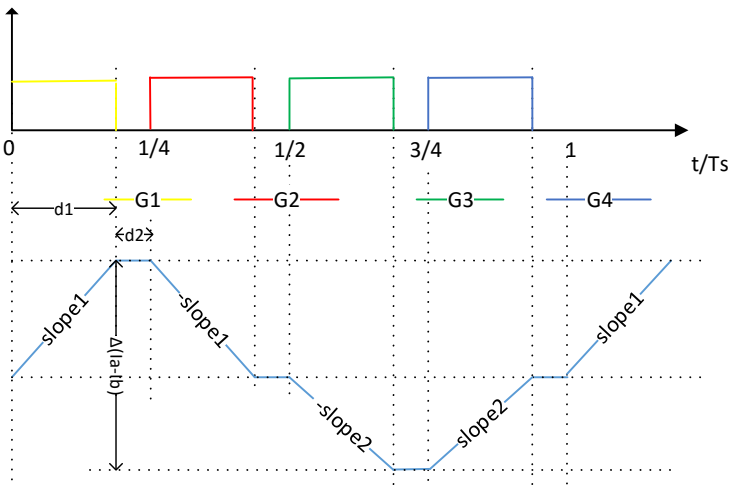


Fig 2.6 Differential current ripples between first and second channels for duty range $0 \leq d \leq 0.25$; d1 = dT_s, *d2* = T_s*(0.25 -d)* and $\Delta(I_a - I_b)$ represents the maximum peak to peak ripple (Inter-cell transformers)

$$\Delta(I_a - I_b) = \frac{V_{dc}T_s(N_o+N_1)}{4} \quad \text{for } 0.25 \le d \le 0.5 \quad (2.25b)$$

$$\Delta(I_a - I_b) = \frac{V_{dc}T_s(N_o+N_1)}{4} \quad \text{for } 0.5 \le d \le 0.75 \quad (2.25c)$$

$$\Delta(I_a - I_b) = V_{dc}T_s(1-d)(N_o+N_1) \quad \text{for } 0.75 \le d \le 1 \quad (2.25d)$$

The maximum ripple in the differential current can be easily derived from equations (2.25) as follows.

$$\Delta_{max}(I_a - I_b) = \frac{V_{dc}T_s}{8(L_1+l_{m1})} \quad (2.26)$$

Again by referring equations (2.21), (2.22) and (2.23), the expression for channel currents and their maximum ripple can be found as shown in equation (2.27).

$$\begin{bmatrix} \frac{dI_a}{dt} \\ \frac{dI_b}{dt} \\ \frac{dI_c}{dt} \\ \frac{dI_d}{dt} \end{bmatrix} = \begin{bmatrix} N_2 & N_3 & N_4 & N_3 & N_5 \\ N_3 & N_2 & N_3 & N_4 & N_5 \\ N_4 & N_3 & N_2 & N_3 & N_5 \\ N_3 & N_4 & N_3 & N_2 & N_5 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \\ V_o \end{bmatrix} \quad (2.27)$$

where $N_2 = \frac{1}{8}\left(\frac{2}{L_1+l_{m1}} + \frac{1}{L_1+2l_{m1}} + \frac{1}{L_1+2L_2}\right)$; $N_3 = \frac{1}{8}\left(\frac{-1}{L_1+2l_{m1}} + \frac{1}{L_1+2L_2}\right)$;

$N_4 = \frac{1}{8}\left(\frac{-2}{L_1+l_{m1}} + \frac{1}{L_1+2l_{m1}} + \frac{1}{L_1+2L_2}\right)$; $N_5 = \frac{1}{8}\left(\frac{-4}{L_1+2L_2}\right)$

The ripple current in first channel for a duty ratio $0.25 \le d \le 0.5$ and its possible maximum value (at $d = 0.5$) is given by equations (2.28a & 2.28b). Similarly, the maximum ripple in the total current can be describe by the equation (2.28c). It occurs at duties $d = 0.125, 0.375, 0.625, and\ 0.875$.

$$\Delta I_a = V_{dc}T_s(N_5 d^2 + (N_2 + 2N_3)d - 0.5N_3) \quad \text{for } 0.25 \le d \le 0.5 \quad (2.28a)$$

$$\Delta I_{a\_max} = \frac{V_{dc}T_s}{16(L_1+l_{m1})} \quad (2.28b)$$

$$\Delta_{max}(I_{total}) = \frac{V_{dc}T_s}{16(2L_1+4L_2)} \quad (2.28c)$$

2.4. DC/DC Converter Using Coupled Inductors: Pair Coupling

Analyzing inter-cell transformers becomes complex as the number of channels increase. This is because of the circular nature of coupling. The main advantage of using coupled inductors is the cancelation of the dc magnetizing currents so that the inductors can be designed for a

possible minimum magnetizing current. Coupled inductors also helps in reducing circulating currents and channel current unbalances. From magnetizing current point of view, using coupled inductors in a multi-stage approach as described in [5] can also achieve the same level of lower magnetizing currents as circular inter-cell transformers do. As it is shown in Fig 2.7, channels are grouped in pair and coupled inductors are used for each pair. Always the number of channels shall be 2^n where n is positive integer so that they can be realized in multi-stages [5]. This approach decreases the number of inductors to be used as compared to circular inter-cell approach. Pair coupling can also be done in a single stage by which the number of channels just need to be even.

The detail approach of analyzing 8_channel four-stage converter is presented in [5]. However, the analytical model used at some of the stages doesn't consider the full number of channels. For example, in analyzing the circulating current in the first stage, only two channels are considered as if they are operating independent of the remaining channels at 180^0 phase shift. This implies one of them can be ON while the other is OFF for a maximum duration of $0.5T_s$ which is true only for a 2-channel converter. In 8-channel this duration is limited to the maximum of $0.125T_s$. This issue is addressed properly in this thesis by considering the actual principle of operation of all channels.

The discussion starts with 4-channel single stage model as shown in Fig 2.7. The first two channels are coupled together and the remaining two are coupled together. Their outputs are connected together in series with common mode inductor. Later on, the effect of adding another stage will be studied. Coupled inductors are assumed to have leakage inductance of L_1 on both sides and a magnetizing inductance of l_{m1}. The inductance of common mode inductor is L_2.

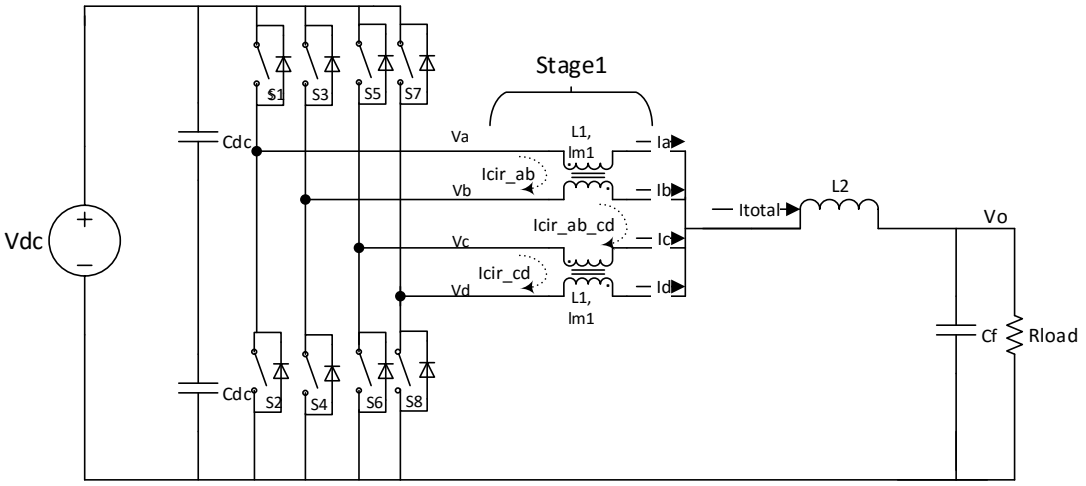


Fig 2.7 Four channel interleaved DC/DC converter using single stage pair-coupling

The differential volt-seconds are higher between channels having higher carrier phase shift. This suggests that the differential current between channels with higher carrier phase shift will be higher than those having smaller phase shift. It is known that a differential current between any two channels is proportional to the magnetizing current flowing through coupling inductors placed in antiparallel direction between the channels.

Thus, it is advantageous to put coupled inductors between adjacent channels (channels with the smallest phase shift between their PWM carriers), so that the magnetizing current can be lower. This leads to design of coupled inductors with reduced size. Equation (2.29) summarizes the differential equations describing the converter shown in Fig 2.7.

$$V_a = L_1 \frac{dI_a}{dt} + l_{m1} \frac{d(I_a - I_b)}{dt} + L_2 \frac{dI_{total}}{dt} + V_o \quad (2.29a)$$

$$V_b = L_1 \frac{dI_b}{dt} + l_{m1} \frac{d(I_b - I_a)}{dt} + L_2 \frac{dI_{total}}{dt} + V_o \quad (2.29b)$$

$$V_c = L_1 \frac{dI_c}{dt} + l_{m1} \frac{d(I_c - I_d)}{dt} + L_2 \frac{dI_{total}}{dt} + V_o \quad (2.29c)$$

$$V_d = L_1 \frac{dI_d}{dt} + l_{m1} \frac{d(I_d - I_c)}{dt} + L_2 \frac{dI_{total}}{dt} + V_o \quad (2.29d)$$

$$I_{total} = I_a + I_b + I_c + I_d \quad (2.29e)$$

Following similar procedures as described in the previous sections, the differential current, total current and channel currents are expressed in equations (2.30), (2.31) and (2.32), respectively.

$$\frac{d(I_a - I_b)}{dt} = \frac{V_a - V_b}{L_1 + 2l_{m1}} ; \frac{d(I_c - I_d)}{dt} = \frac{V_c - V_d}{L_1 + 2l_{m1}} \quad (2.30)$$

$$\frac{dI_{total}}{dt} = \frac{V_a + V_b + V_c + V_d - 4V_o}{L_1 + 4L_2} \quad (2.31)$$

$$\begin{bmatrix} \frac{dI_a}{dt} \\ \frac{dI_b}{dt} \\ \frac{dI_c}{dt} \\ \frac{dI_d}{dt} \end{bmatrix} = \begin{bmatrix} N_o & N_1 & N_2 & N_2 & N_v \\ N_1 & N_o & N_2 & N_2 & N_v \\ N_2 & N_2 & N_o & N_1 & N_v \\ N_2 & N_2 & N_1 & N_o & N_v \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \\ V_o \end{bmatrix} \quad (2.32)$$

where: $N_o = \frac{1}{4L_1} + \frac{1}{2L_1 + 4l_{m1}} + \frac{1}{4L_1 + 16L_2}$; $N_1 = \frac{1}{4L_1} - \frac{1}{2L_1 + 4l_{m1}} + \frac{1}{4L_1 + 16L_2}$; $N_2 = \frac{-1}{4L_1} + \frac{1}{4L_1 + 16L_2}$; $N_v = -\frac{1}{L_1 + 4L_2}$

The maximum current ripples in the differential currents can be found in the same way as the previous cases by referring equation (2.30) and Fig 2.2. The same procedure applies for determining the current ripples in each channel and in the output current. Equations (2.32) to (2.34) gives the maximum peak to peak current ripples which may help in the proper design of the inductors.

$$\Delta_{max}(I_a - I_b) = \frac{V_{dc}T_s}{4(L_1+2l_{m1})} \tag{2.32}$$

$$\Delta_{max}(I_{total}) = \frac{V_{dc}T_s}{16(L_1+4L_2)} \tag{2.33}$$

$$\Delta_{max}(I_a) = \frac{V_{dc}T_s}{8}\left(\frac{1}{L_1} + \frac{1}{L_1+2L_{m1}}\right) \tag{2.34}$$

The other option of pair coupling is to use additional stage as shown in Fig 2.8. The coupled inductors at stage2 has a mutual inductance of l_{m2} and leakage inductance of L_2 on both sides. A common inductor, L_3, is connected after the second stage. The general equation that describes the topology shown in Fig 2.8 can be derived easily as shown in equations (2.35).

$$V_a = L_1\frac{dI_a}{dt} + l_{m1}\frac{d(I_a-I_b)}{dt} + L_2\frac{d(I_a+I_b)}{dt} + l_{m2}\frac{d(I_a+I_b-I_c-I_d)}{dt} + L_3\frac{dI_{total}}{dt} + V_o \tag{2.35a}$$

$$V_b = L_1\frac{dI_b}{dt} - l_{m1}\frac{d(I_a-I_b)}{dt} + L_2\frac{d(I_a+I_b)}{dt} + l_{m2}\frac{d(I_a+I_b-I_c-I_d)}{dt} + L_3\frac{dI_{total}}{dt} + V_o \tag{2.35b}$$

$$V_c = L_1\frac{dI_c}{dt} + l_{m1}\frac{d(I_c-I_d)}{dt} + L_2\frac{d(I_c+I_d)}{dt} - l_{m2}\frac{d(I_a+I_b-I_c-I_d)}{dt} + L_3\frac{dI_{total}}{dt} + V_o \tag{2.35c}$$

$$V_d = L_1\frac{dI_d}{dt} - l_{m1}\frac{d(I_c-I_d)}{dt} + L_2\frac{d(I_c+I_d)}{dt} - l_{m2}\frac{d(I_a+I_b-I_c-I_d)}{dt} + L_3\frac{dI_{total}}{dt} + V_o \tag{2.35d}$$

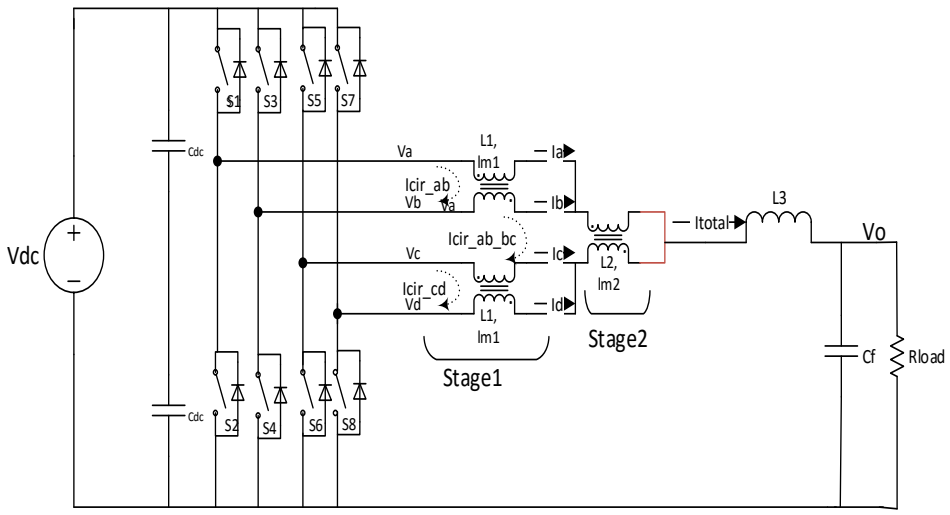


Fig 2.8 Four channel interleaved DC/DC converter using two-stage pair coupling

$$I_{total} = I_a + I_b + I_c + I_d \tag{2.35e}$$

The remaining analysis for ripple currents at different stages follows similar procedures as the previous cases. Equation (2.36) gives the differential current between coupled channels at first stage, while equation (2.37) describes the differential current at second stage. Equations (2.38) and (2.39) describe the total current and channel currents, respectively.

$$\frac{d(I_a - I_b)}{dt} = \frac{V_a - V_b}{L_1 + 2l_{m1}}\ ;\ \frac{d(I_c - I_d)}{dt} = \frac{V_c - V_d}{L_1 + 2l_{m1}} \tag{2.36}$$

$$\frac{d(I_a + I_b - I_c - I_d)}{dt} = \frac{V_a + V_b - V_c - V_d}{L_1 + 2L_2 + 4l_{m2}} \tag{2.37}$$

$$\frac{dI_{total}}{dt} = \frac{V_a + V_b + V_c + V_d - 4V_o}{L_1 + 2L_2 + 4L_3} \tag{2.38}$$

$$\begin{bmatrix} \frac{dI_a}{dt} \\ \frac{dI_b}{dt} \\ \frac{dI_c}{dt} \\ \frac{dI_d}{dt} \end{bmatrix} = \begin{bmatrix} N_o & N_1 & N_2 & N_2 & N_v \\ N_1 & N_o & N_2 & N_2 & N_v \\ N_2 & N_2 & N_o & N_1 & N_v \\ N_2 & N_2 & N_1 & N_o & N_v \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \\ V_o \end{bmatrix} \tag{2.39}$$

where: $N_o = \frac{1}{4(L_1+2L_2+4L_3)} + \frac{1}{4(L_1+2L_2+4l_{m2})} + \frac{1}{2L_1+4L_{m1}}$; $N_v = -\frac{1}{(L_1+2L_2+4L_3)}$

$N_1 = \frac{1}{4(L_1+2L_2+4L_3)} + \frac{1}{4(L_1+2L_2+4l_{m2})} - \frac{1}{2L_1+4l_{m1}}$; $N_2 = \frac{1}{4(L_1+2L_2+4L_3)} - \frac{1}{4(L_1+2L_2+4l_{m2})}$

Following similar procedures as in the previous cases, the maximum ripples at different stages can be summarized as follows.

$$\Delta_{max}(I_a - I_b) = \frac{V_{dc}T_s}{4(L_1+2l_{m1})} \tag{2.40}$$

$$\Delta_{max}(I_{total}) = \frac{V_{dc}T_s}{16(L_1+2L_2+4L_3)} \tag{2.41}$$

$$\Delta_{max}(I_a) = \frac{V_{dc}T_s}{8}\left(\frac{1}{L_1+2l_{m1}} + \frac{1}{L_1+2L_2+4l_{m2}}\right) \tag{2.42}$$

$$\Delta_{max}(I_a + I_b) = \frac{V_{dc}T_s}{8(L_1+2L_2+4l_{m2})} \tag{2.43}$$

$$\Delta_{max}(I_a + I_b - I_c - I_d) = \frac{V_{dc}T_s}{2(L_1+2L_2+4l_{m2})} \tag{2.44}$$

2.5. Inductor Size Comparison

The size of power converters is highly dependent on the size of passive elements used such as capacitors and inductors. The ultimate goal of interleaved power converter is to reduce the current ripples so that output filter size can be minimized. Filter sizes are usually dominated by inductors. Moreover, inductors are the one which determine the behavior of the power converter in terms of channel ripples or total output current harmonics. The total current considered here is the summation of channel currents just before the filtering capacitor. Although the filter capacitor is connected in parallel with resistive load as shown in all previous figures, the analysis in this thesis is limited just to the current ripples in each channel and in the total current before the capacitor. The following section discusses and compares the size of inductors required for a given level of harmonics in the total output current.

Fourier series is the widely used method to analyze harmonic contents of a given periodic signal. This gives the magnitude and phase of every possible harmonic. However, it becomes much cumbersome to apply it in a wave forms which do not have symmetry and different slopes over different segments of a single period as it is the case in the channel currents and differential currents discussed so far. Simulation tools are used instead to determine the harmonic contents of such wave forms as it is discussed in the next chapter.

Peak to peak ripple is yet another expression which indicates the harmonic content indirectly. Values of inductors in power converter, especially in DC/DC, are usually determined in relation to peak to peak ripples. In addition to the inductance value, the size (volume) of an inductor depends on additional parameters such as rated current and magnetizing current as these are key parameters in selecting the right core and copper cross-section. There are different approaches in estimating the volume of an inductor. Both weight and volume estimations based on area product are discussed in [37] and similar approach is used for interleaved converters in [5]. The equations governing the relationship between area product and the volume and weight of an inductor are summarized in equation (2.45) as they are described in [37].

$$Volume = K_{vol} A_p^{(0.75)} \tag{2.45a}$$

$$Weight = K_{wt} A_p^{(0.75)} \tag{2.45b}$$

where A_p area product (cm^4), K_{vol} is a constant (dimensionless) and K_{wt} is a constant (g/cm^3).

A_p is given by the product of core cross-section (A_c) and windows area (A_w). Its general expression is given by equation (2.46).

$$A_p = A_c A_w = \frac{LI_{mag} I_{rms}}{K_w B_{max} J} \tag{2.46a}$$

$$Volume = K\left(LI_{mag} I_{rms}\right)^{0.75} \tag{2.46b}$$

where I_{rms} is the rated rms current flowing in the inductor with inductance of L, while I_{mag} is the peak magnetizing current that is rated at a maximum flux density of B_{max}. K_w is the core window fill factor while J represents the rated current density of copper to be used in the winding. All terms in the denominator of equation (2.46a) can be assumed to be constant for a given type of magnetic core and copper winding and they are represented by a constant in equation (2.46b), i.e. $K = \frac{K_{vol}}{(K_w B_{max} J)^{0.75}}$. Thus, the volume of inductor is solely determined by the numerator terms ($L, I_{mag}\ and\ I_{rms}$). The equations derived in the previous sections to describe maximum peak to peak current ripples at different stages are summarized in Table 2.1.

Table 2.1 Summary of maximum ripple current expressions at different stages of different topologies

	Chanal current $\Delta_{max}(I_a)$	Differential current ripple $\Delta_{max}(I_a - I_b)$	Sub-module current $\Delta_{max}(I_a + I_b)$	Differential current between sub-modules $\Delta_{max}(I_a + I_b - I_c - I_d)$	Total current before capaciter filtering $\Delta_{max}(I_{total})$
Uncoupled	$\frac{V_{dc} T_s}{4L_1}$	$---$	$---$	$---$	$\frac{V_{dc} T_s}{16(L_1 + 4L_2)}$
Inter-cell	$\frac{V_{dc} T_s}{16(L_1 + l_{m1})}$	$\frac{V_{dc} T_s}{8(L_1 + l_{m1})}$	$---$	$---$	$\frac{V_{dc} T_s}{16(2L_1 + 4L_2)}$
Single stage pair coupling	$\frac{V_{dc} T_s}{8}\left(\frac{1}{L_1} + \frac{1}{L_1 + 2l_{m1}}\right)$	$\frac{V_{dc} T_s}{4(L_1 + 2l_{m1})}$	$---$	$---$	$\frac{V_{dc} T_s}{16(L_1 + 4L_2)}$
Multistage pair coupling	$\frac{V_{dc} T_s}{8}\left(\frac{1}{L_1 + 2L_{m1}} + \frac{1}{L_1 + 2L_2 + 4l_{m2}}\right)$	$\frac{V_{dc} T_s}{4(L_1 + 2l_{m1})}$	$\frac{V_{dc} T_s}{8(L_1 + 2L_2 + 4l_{m2})}$	$\frac{V_{dc} T_s}{2(L_1 + 2L_2 + 4l_{m2})}$	$\frac{V_{dc} T_s}{16(L_1 + 2L_2 + 4L_3)}$

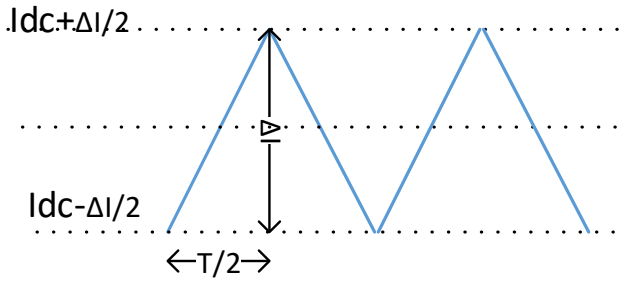


Fig 2.9 A rough approximation of current ripples in finding their rms values

The parameters indicated in the 4th and 5th columns in Table 2.1 are associated with the coupled inductor at stage2. As they are not important in determining the inductor parameters on the other types of topologies, they are omitted. Similarly, the ripples on the differential current in the third column is important only for coupled inductors. To make the analysis simpler, the shape of current ripples are assumed to be symmetrical and triangular as shown in Fig 2.9. A general description of rms current for the wave form shown in Fig 2.9 is given by equation (2.47).

$$I_{rms} = \sqrt{{I_{dc}}^2 + \frac{(\Delta I)^2}{12}} \qquad (2.47)$$

All topologies are assumed to have a dc voltage supply of $V_{dc} = 400V$ and rated dc channel current of $I_{dc} = 10A$. A 10 kHz switching frequency is assumed in all cases. All the elements in the power converter are assumed to be ideal. Let the maximum ripple current at the output be $\Delta_{max} I_{(total)} = 0.25A$. For coupled inductors, the leakage inductance on each side is assumed to be 10% of the magnetizing inductance.

It is easier to start with the common inductor near the load. By referring the Table 2.1, the following results can be derived for better channel current ripples and volume reduction while meeting the constraint of maximum peak to peak ripple in the output current. Putting larger value of inductance near the front end rather than the load will decrease the rated current flowing through inductors, hence lower volume. Accordingly, the common mode inductor near the load is assumed to be zero.

1. *Interleaved using uncoupled inductors:*

$$L_1 = 10mH \text{ and } L_2 = 0H;\ \Delta_{max}(I_a) = 1A;\ I_{a-rms} = 10.004A, I_{a-mag} = 10.5A$$

$$Volume = K(4 * 10mH * 10.004A * 10.5A)^{0.75} = 2.94K$$

2. *Interleaved using Circular Inter-cell Transformers:*

$L_1 = 5mH,\ l_{m1} = 50mH\ and\ L_2 = 0H;\ \Delta_{max}(I_a) = 45.5mA;\ \Delta_{max}(I_a - I_b) = 91mA;$

$I_{a-rms} \approx 10A, I_{a-mag} = 45.5mA$

$$Volume = K(8 * 55mH * 10A * 45.5mA)^{0.75} = 0.3K$$

3. *Interleaved using Single Stage Pair Coupling*

$L_1 = 10mH,\ l_{m1} = 100mH\ and\ L_2 = 0H;\ \Delta_{max}(I_a) = 524mA;\ \Delta_{max}(I_a - I_b) = 47.6mA\ ;\ I_{a-rms} \approx 10.001A, I_{a-mag} = 23.8mA$

$$Volume = K(4 * 110mH * 10.001A * 23.8mA)^{0.75} = 0.183K$$

4. *Interleaved using Multistage Pair Coupling:*

$L_1 = 5mH,\ l_{m1} = 50mH, L_2 = 2.5mH, l_{m2} = 25mH\ and\ L_3 = 0H;\ \Delta_{max}(I_a) = 93mA;\ \Delta_{max}(I_a - I_b) = 95.2mA;\ \Delta_{max}(I_a + I_b) = 43.5mA;\ \Delta_{max}(I_a + I_b - I_c - I_d) = 174mA; I_{a-rms} \approx 10A, I_{a-mag} = 47.6mA;\ I_{a+b-rms} \approx 20A, I_{stage2-mag} = 87mA;$

$$Volume = K(4 * 55mH * 10A * 47.8mA)^{0.75} + K(2 * 27.5mH * 20A * 87mA)^{0.75}$$

$$= 0.357K$$

5. *Non-interleaved using uncoupled Inductors:*

$L_1 = 160mH\ and\ L_2 = 0H;\ \Delta_{max}(I_a) = 62.5mA;\ I_{a-rms} \approx 10A, I_{a-mag} = 10.03A$

$$Volume = K(4 * 160mH * 10A * 10.03A)^{0.75} = 22.68K$$

6. *Non-interleaved with Coupled Inductors:*

Ideally, if coupled inductors are operated in non-interleaved mode, the magnetizing current will be zero. This gives a zero volume of inductor which is not realizable. Due to parameter mismatches, there could be slight difference in the channel currents, let assume it to be of 10mA. This gives $L_1 = 160mH, l_{m1} = 1.6H\ and\ L_2 = 0H;\ \Delta_{max}(I_a) = 62.5mA;\ \Delta_{max}(I_a - I_b) \approx 0A(10mA), I_{a-rms} \approx 10A, I_{a-mag} \approx 5mA$

$$Volume = K(4 * 1.76H * 10A * 5mA)^{0.75} = 0.457K$$

As it can be seen from the above analysis all of the interleaved methods have significant size reduction of inductors as compared to the non-interleaved converter. It should be noted also that

the frequency of output current ripples are four times the frequency of the non-interleaved converters. This makes the size of additional filter requirement (if needed) to be smaller. The volume of the non-interleaved coupled inductors could be minimized more, but needs very precise operation of the controller which is not the case in reality due to transients and parameter variation among different components. Of course, this is true for other topologies too. A proportional change in the magnetization current can be assumed which doesn't affect the ratio of their volumes. However, for coupled non-interleaved case, since the magnetizing current is ideally zero, scaling it by some factor still remains zero. Assuming some minimum magnetizing current could be more appropriate in this case. In addition, a very big value of inductance means very slow dynamics of the controller which is the case in the case of coupled inductors without interleaving. A more detailed analysis and consideration of such factors may be required to make a precise volume estimation which is beyond the scope of this thesis work. The best case of the non-interleaved topology as discussed above is taken as a benchmark to estimate how much volume can be saved for interleaved converters.

Non-interleaved with Coupled Inductors:	*100%*
Non-interleaved using uncoupled Inductors:	*4900%*
Interleaved using uncoupled inductors:	*643%*
Interleaved using circular inter-cell transformers:	*65.6%*
Interleaved using single stage pair coupling:	*40.1%*
Interleaved using multistage pair coupling:	*78.1%*

This shows that interleaved converters with circular inter-cell coupling and those with multistage pair coupling give more or less similar volume reduction. However, the analysis becomes more complex as the number of channels increases. Single stage pair coupling, on the other hand, has resulted a significant volume reduction and is almost equal to half of the other coupling methods.

2.6. Inverters

Inverters operate with the same principle as DC/DC except their topology is connected in such a way that it allows negative current and the reference is sinusoidal. The topologies can be half bridge or full bride. In relation to PI controllers, inverters may have steady error. The maximum ripple and other parameters discussed so far holds true for inverters too. Additional parameters

which describe inverters are amplitude modulation index and frequency modulation ratio. Amplitude modulation index refers to the ratio of the peak value of reference to the peak value of the carrier signal. If this ratio remains below 1, the output voltage always has a fundamental component which is proportional to the dc bus voltage. This region is called linear region. If the peak value of reference signal is greater than the carrier peak, then the output voltage tends to look like more of square wave and the linearity gets lost. This region is called over-modulation and the peak value of the fundamental lies between 1 to $4/\pi$ times of the dc reference voltage. The maximum utilization of the DC bus voltage also depends on the type of inverter implemented, i.e. half bridge or full bridge. Only half of the DC link voltage available for half bridge inverters.

2.7. Summary

In this chapter, four types of interleaved power converters were modeled analytically. Equations relating their voltage and currents were derived. Maximum ripple currents at different stage of the converter were analytically derived for different ranges of duty cycles. Using the equations derived, inductor volume comparison is made between different topologies for a given maximum current ripple in the output. Implementation of simulation models based on the values of inductors already determined in this chapter will be used for simulation in the next chapter. Simulation results will be compared with the analytical findings.

CHAPTER THREE

3. SIMULATIONS: MODELING AND RESULTS

3.1. Introduction

After having the clear picture of the models as discussed in the previous chapter, PSIM® is used to simulate and verify the analysis. Although there are many methods of modeling a system in the process of designing good controller such as steady state, average model, state space modeling and others, the simple and familiar method is used here. As the controller to be designed is proportional-integral type (PI), modeling of the converters is done based on differential equations. The main interest of this thesis is to implement interleaved converters with simple DSP and observe if they have met their goal, i.e. reduction of current ripples in the output. Hence, only current controllers are considered. The current controller should guarantee a balanced channel current as much as possible. Thus, each channel is associated with current sensor and independent controllers are used in closed loop for each channel. Fig 3.1 shows how the system components are interconnected. An *N*-channel power module is connected to a dc voltage source. The power module consists of all the dc link capacitors and inductors (they could be coupled or uncoupled depending on the topology). In case of multi-stage coupling, the coupling in the intermediate stages is to be made just after the current sensors so that each channel current is sensed. All channel currents meet at point of common coupling just before low pass filter which is connected in parallel with the load. The *N* signals sampled from *N* channel currents are fed into the controller which generates two PWM signals per channel: one for upper leg and one for lower leg. These two signals are inverse of one another except for dead time to avoid possibility of short circuit on channel legs. This gives a total of *2N* control signals to be fed into the power module. The low pass filter is used to filter the remaining ripples and it can be just *L* or *LC* filter. The next sections describe how the system is modeled, how the controller is tuned and what results are found.

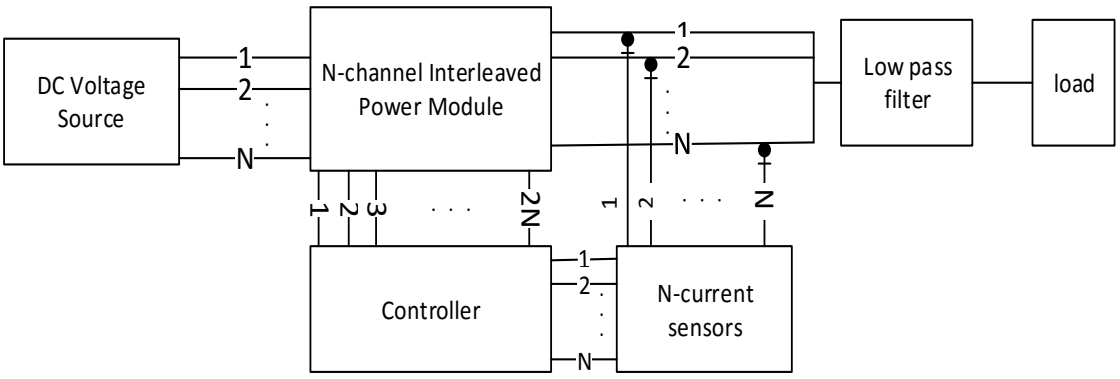


Fig 3.1 Block diagram of the controller structure

3.2. Modeling and Tuning of PI Controller

PI controller is selected for this thesis because of its simplicity and its capability to compensate for dead band [6]. There are two approaches in designing digital controller: either applying direct discretization which needs designing everything in discrete time domain or designing in analog/continuous time domain and converting the controller in to discrete form. The later method is applied in this thesis by which analog PI controller is first designed and then its digital equivalent is derived using the Tustin approximation. Tustin approximation is selected for its better performance outputs regarding frequency wrapping [6].

The general model of a closed loop controller for a power converter, as it is explained in detail in reference [6], is illustrated in Fig 3.2. *I_ref(t), , Io (t), I_sample(t) and I_er(t)* refers to the reference current, output current, sampled current and error current in time domain. *Vref(t)* refers to the output of PI controller which is equivalent to the reference voltage required to generate the PWM. Its maximum value should be less or equal to the peak value of the carrier signal in the PWM, usually normalized to V_{dc}. *ZOH, C(t) and d(t)* represent the zero order holder, carrier signal and output duty cycle of the PWM module in time domain, respectively. *PI(s) and G(s)* refers to the continuous time domain transfer functions of the PI controller and the power converter.

The computational delay for a simple PI controller is almost insignificant as compared to the delay of the PWM update (*ZOH).* This delay of ZOH depends on the type of controller used and the type of carrier signal implemented in the PWM module. Triangular carrier with updating instances of the PWM synchronized with the peak and valleys of the PWM carriers are implemented in this thesis. Thus, a total of delay considered here, represented by T_{delay}, is assumed to be equal to half of the switching period. In addition to the delay, the PWM module has a gain of $\frac{1}{V_{dc}}$.

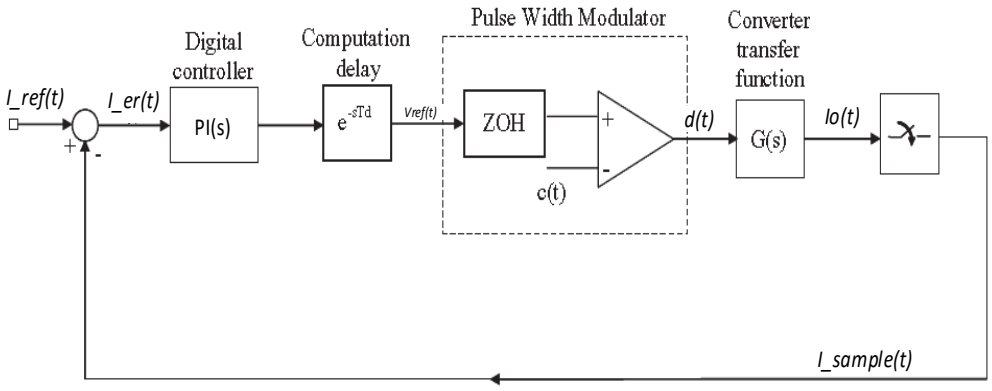


Fig 3.2 General modeling of the closed loop controller for a power converter (modified from [6])

Phase margin and gain margin of the open loop transfer function are used to tune the PI controllers, a method widely used for tuning PI controllers [4], [5], [6]. Equation (3.1) shows the open loop transfer function of the controller shown in Fig 3.2. Parasitic resistance of the inductors are ignored in the analysis as their effect on the parameters of the controller are insignificant [5], [6].

$$G_{open}(s) = PI(s)(\frac{1}{V_{dc}} e^{-s(T_{delay})})G(s) \quad (3.1)$$

$$PI(s) = K_p + \frac{K_i}{s} \quad (3.2)$$

$$G(s) = \frac{V_{dc}}{sL_{eq}} \quad (3.3)$$

where L_{eq} represents the equivalent inductance of the system as seen by the controller.

The controllers considered here monitors each channel independently. Fig 3.3 shows part of one of the topologies discussed in the previous chapters. The mutual and leakage inductances are separated for easier analysis. Equation (3.4a) describes the equation for first channel. The input voltage $V_a(t)$ can be expressed in terms of duty cycle and dc link voltage as $V_a(t) = d(t)V_{dc}$ while $V_x(t)$ depends on the status of other channels, and hence considered as external disturbance for the controller. The simplified s-domain transfer function relating the current and duty cycle can be written as shown in equation (3.4b). This shows that the equivalent inductance of all the controllers will be just L_1, in all of the topologies considered. It should be noted that L_1 represents the leakage inductance for coupled and self-inductance for uncoupled inductors.

$$L_1 \frac{dI_a(t)}{dt} = V_a(t) - V_x(t) \quad (3.4a)$$

$$\frac{I_a(s)}{d(s)} = \frac{V_{dc}}{sL_1} \quad (3.4b)$$

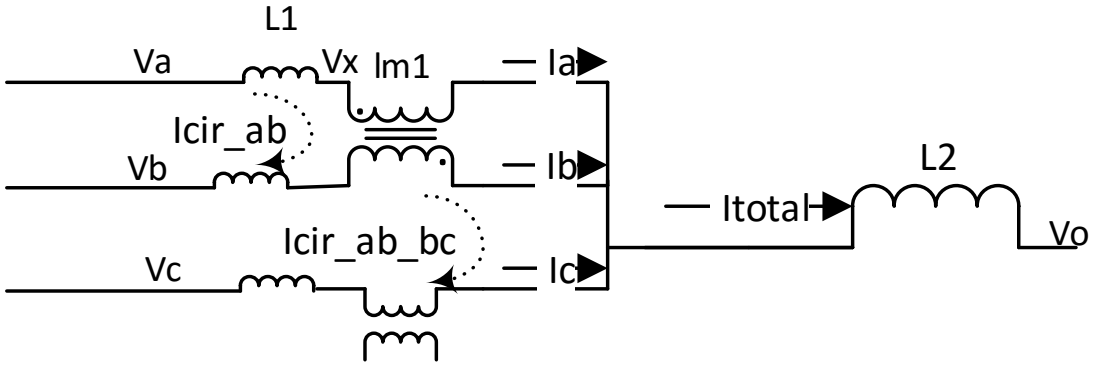


Figure 3.3 Part of single stage pair coupling topology

Furthermore, Pade approximation can be used to approximate the controller delay as shown in equation (3.5).

$$e^{-sT_{delay}} = e^{-s\frac{T_S}{2}} = \frac{1-s\frac{T_S}{4}}{1+s\frac{T_S}{4}} \quad (3.5)$$

where $T_s = 2T_{delay}$ is the switching period of the PWM. Equation (3.1) can be rewritten as shown in equation (3.6a). The gain of PWM module can be transferred to the controller so that the carrier signal will have unity peak to peak, and the controller gets normalized with V_{dc}. Its equivalent frequency domain, after normalization, is described by equation (3.6b).

$$G_{open}(s) = \left(K_p + \frac{K_i}{s}\right)\left(\frac{1}{V_{dc}}\frac{1-s\frac{T_S}{4}}{1+s\frac{T_S}{4}}\right)\left(\frac{V_{dc}}{sL_1}\right) \quad (3.5a)$$

$$G_{open}(j\omega) = \left(K_p + \frac{K_i}{j\omega}\right)\left(\frac{1-j\omega\frac{T_S}{4}}{1+j\omega\frac{T_S}{4}}\right)\left(\frac{1}{j\omega L_1}\right) \quad (3.5b)$$

The parameters of the PI controller (K_p, K_i) can be tuned by selecting a gain margin of unity and a phase margin ($\emptyset_m$) of 45^0 (between 30^0 and 60^0) at frequency equal to the bandwidth of the controller so that the closed loop system remains stable [6]. The bandwidth, ω_b, is chosen to be 10% of the switching frequency. Equation (3.6) gives the equations to be solved for K_p and K_i.

$$\frac{K_i}{K_p} = \frac{\omega_b}{tan^{-1}\left(\emptyset_m + 2tan\left(\omega_b\frac{T_S}{4}\right)\right)} \quad (3.6a)$$

$$K_p = \frac{L_1\omega_b}{tan^{-1}\left(\emptyset_m + 2tan\left(\omega_b\frac{T_S}{4}\right)\right)} \quad (3.6b)$$

3.3. Sampling Techniques

Proper sampling is very critical in closed loop controllers. It should be done in a symmetric way and accurately. Any error in the measurement may lead to oscillations and harmonics at lower frequencies than the switching frequency may appear. Two different sampling techniques are simulated. The first method is sampling at the peak and valleys of each PWM carrier signals. The other technique is sampling simultaneously at a frequency which is a multiple of the switching frequency. In both cases, the PWM will be updated twice per switching period. Samples taken at higher rate are averaged so that the controller is updated with the average value of the current. Circular buffers are used in the simulation to make average of multiple samples taken over a single switching period at.

3.4. Effect of Dead Time

PI controllers are generally immune from dead time effects. The effect of dead time arises because of the stored energy in the inductor while switches are ON needs continuous path. This applies for both DC/DC and DC/AC power converters. During dead time, both IGBTs on the same leg will be OFF and one of the antiparallel diodes on the same leg will conduct to allow the current through the inductor continue its flow. The direction of current determines which diode conducts during dead time. If the current is positive, the lower diode conducts resulting "LOW" pole voltage for the interval equal to the dead time. If the current is negative, instead, the upper diode will conduct resulting "HIGH" pole voltage. The terms HIGH and LOW refers to the relative voltages in which the converter is working (*V_{dc} and 0 for DC/DC, $V_{dc}/2$ and $-V_{dc}/2$ for half bridge inverter, respectively*). This causes pole voltage deviations from the ideal expected shapes, and the difference is usually high frequency square wave pulses at switching frequency with duty equal to the dead time. The PI controller compensates such deviations by itself, which otherwise needs some kind of compensation by adding or subtracting some constant value on the reference depending on the current polarity.

3.5. Simulation Results and Discussions

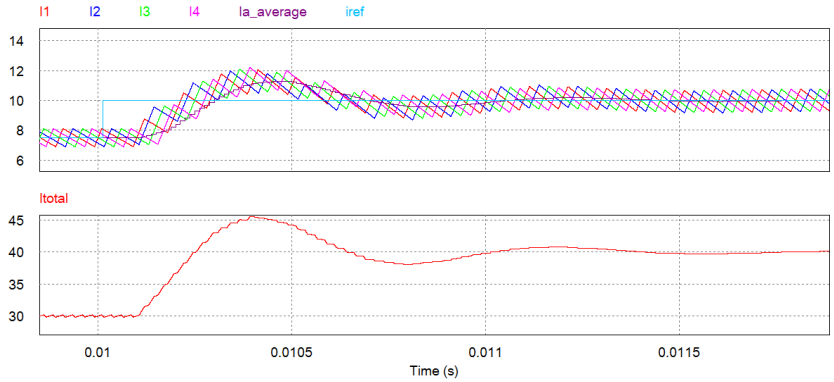
3.5.1. Responses for Step Changes and Peak to Peak ripples

The simulations done in this section are based on the values of inductor parameters determined in the previous chapter. Table 3.1 summarizes the parameters of PI controller considered for simulation.

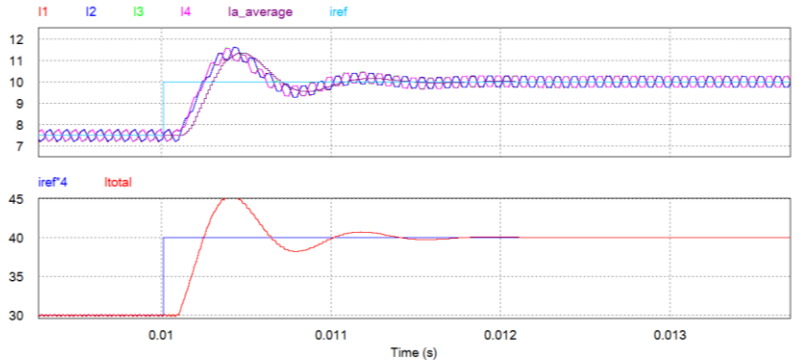
Table 3.1 Continuous time domain parameters of PI controllers for different topologies

Parameter	Uncoupled	Inter-cell	Single stage pair coupling	Multi stage pair coupling
Switching frequency	10 kHz	10 kHz	10 kHz	10 kHz
Bandwidth	1 kHz	1 kHz	1 kHz	1 kHz
L_{eq}	10mH	5mH	10mH	5mH
K_p	56	28	56	28
K_i	180,000	90,000	180,000	90,000

In all of the four topologies mentioned in Fig 3.3, different rate of sampling rate are simulated and it is found that a sampling rate which is a multiple of the channel numbers times the switching frequency gives good results. This could be due to the disturbances due to switching events of different channels.



(a)



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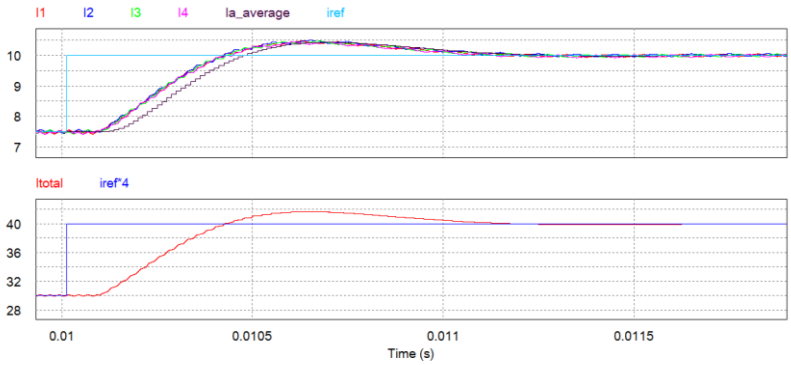

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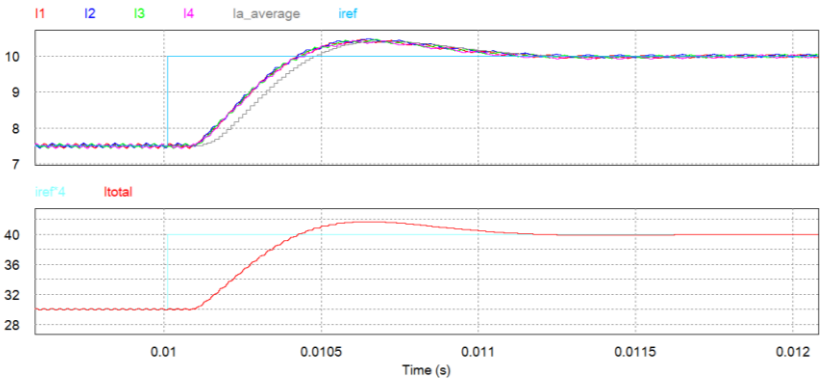


(d)

Fig 3.4. Step response of different coupling techniques for duty step change from o.375 to 0.5 (a) Uncoupled (b) Single stage pair coupling (c) Multi stage pair coupling (d) Circular inter-cell coupling

All the results shown in Fig 3.4 are based on sampling rate of 8 times the switching frequency. The effect of different sampling rate is illustrated later with phase shifted sampling.

Fig 3.4 shows the transient response of different topologies for a step change from a duty cycle of 0.375 to 0.5. *Ia-average* refers to the average current through channel one while *Iref* represents the reference current for each channel. In all cases, channel currents are tracking the reference with settling time of around 1ms. The average current is calculated using circular buffer and has resulted a fractional delay.

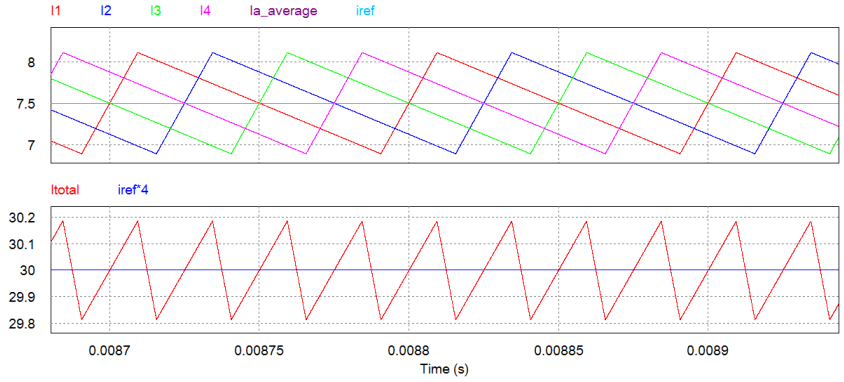
As shown in Fig 3.4 (a) and (b), the responses of interleaved converters with uncoupled inductor and the one with single stage pair coupling have higher overshoot. This is due to higher value of inducatances calculated in the previous chapter which are twice of the values for others. These overshoots can be readjusted by manually tuning the PI controller.

It can be also observed that channel currents have maximum peak to peak ripples at duty ratio of 0.5 while the ripple in the total current is in its minimum. In addition, Fig 3.3 shows that the ripples in the total current is maximum at 0.375. These results matches the theoretical analysis of interleaved converters.

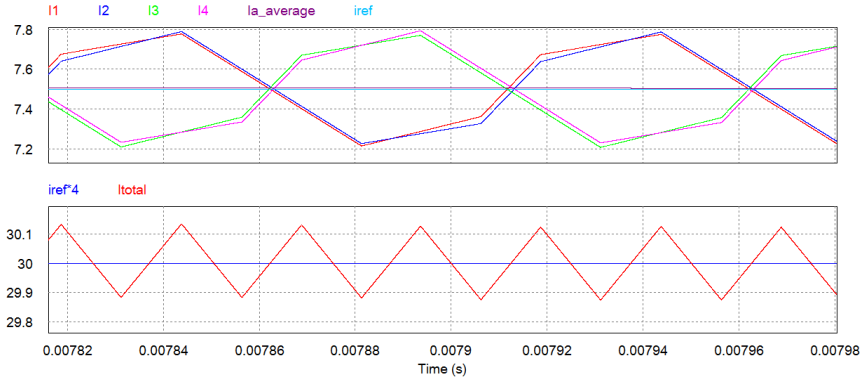
A more detail of the current ripples for a duty cycle of 0.375 is illustrated in Fig 3.5. The peak to peak current ripples in each channel or in the total current matches more or less with the analytical results discussed in the previous chapter. There could be very minor deviations due to very small resistance of coupling inductors considered in simulation.

As it can be seen from Fig 3.5 (a), the channel currents are interleaved by 90^0 and are almost triangular. In Fig 3.5 (b), however, there is almost no phase shift between currents through channel1 and channel2. The same is true for currents through channel3 and channel4. This is due to the pair coupling applied between those channels. As there is no more intermediate coupling stages, the phase shift between pairs looks nearly 180^0. This is not the case for topologies with further coupling as shown in Fig 3.5 (c) and (d).

For multistage and circular coupling cases the current waveforms are unsymmetrical and have multiple slopes. However, the total current ripple is still symmetrical and has frequency of 4times the switching frequency. This interesting point as the objective of interleaving is to get less ripples at higher frequencies in the total output current. It should be noted also that the reference and the average currents are overlapping.



(a)



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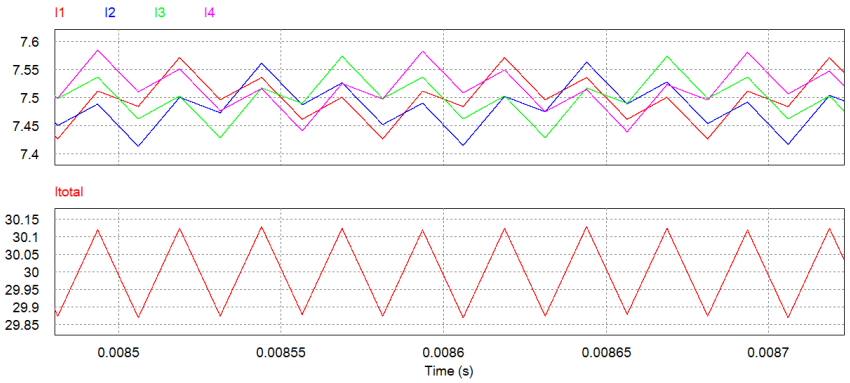

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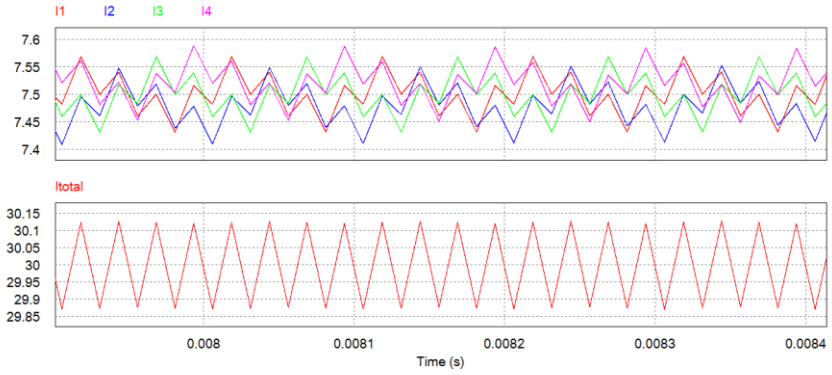
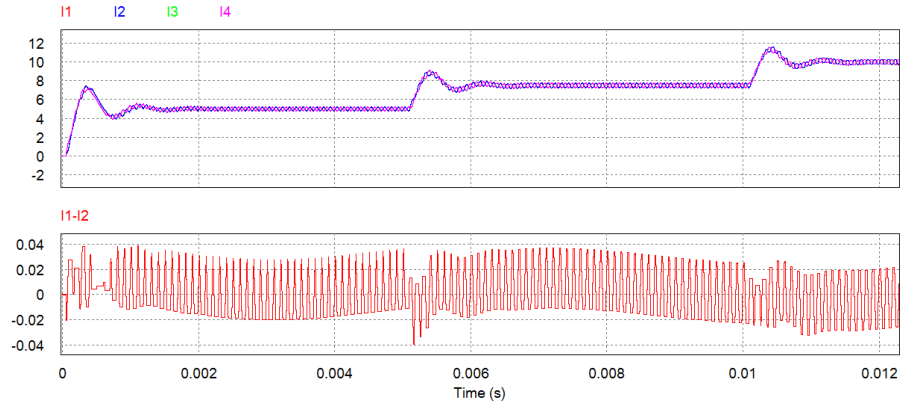
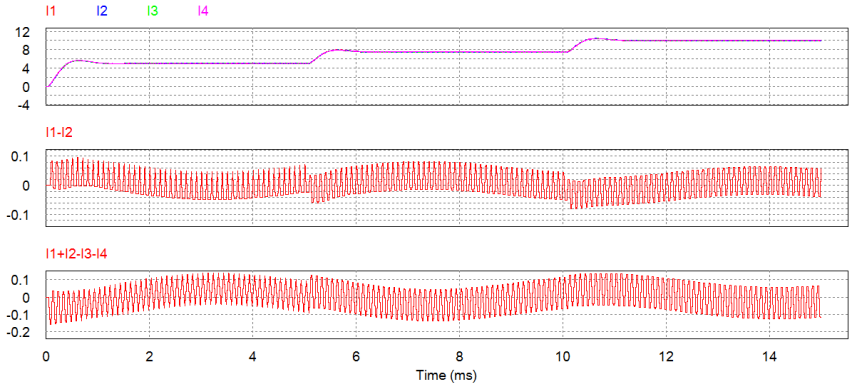


(d)

Fig 3.5. Current ripples for duty ratio of 0.375 for different topology: (a) Uncoupled (b) Single stage pair coupling (c) Multi stage pair coupling (d) Circular inter-cell coupling



(a)



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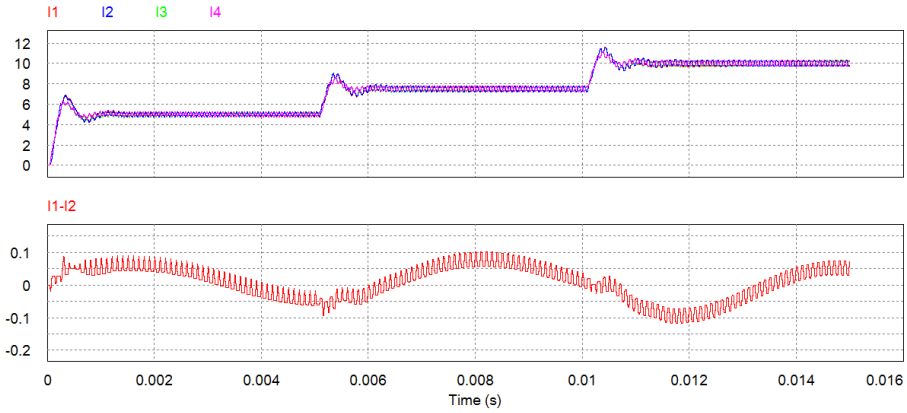


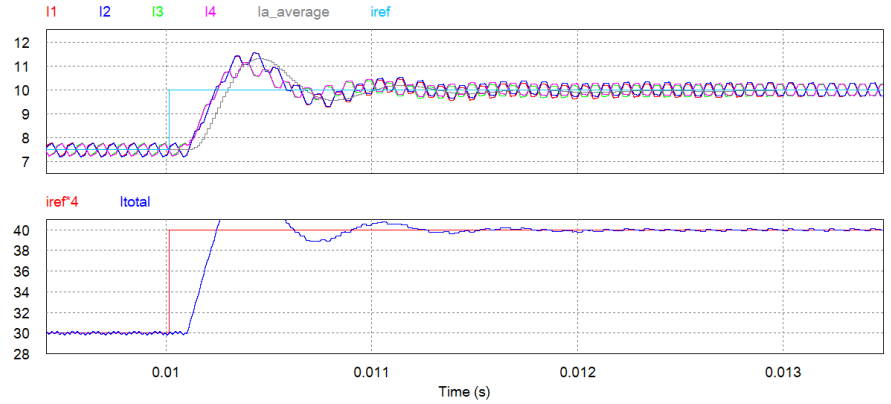
(c)

Fig 3.6. Differential currents in coupled channels in different topologies (a) Single stage pair coupling (b) Multi stage pair coupling (c) Circular inter-cell coupling

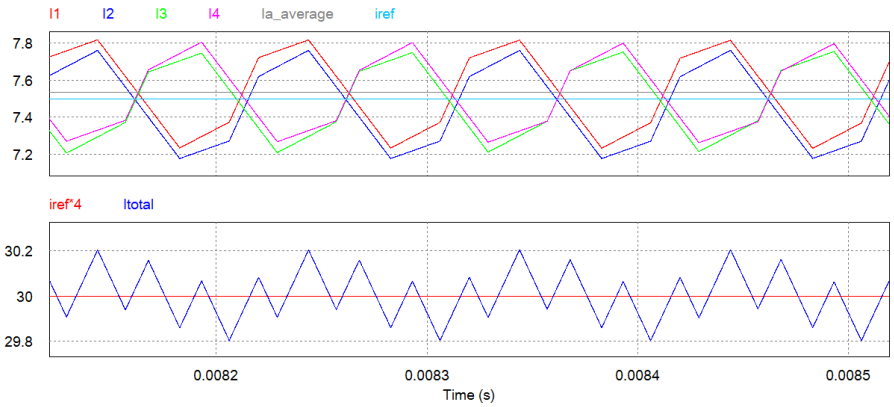
3.5.2. Differential Currents/ Magnetizing Currents/ Circulating Currents

While magnetizing currents are equal to the differential currents, circulating currents are less by half. Fig 3.6 illustrates the differential current through coupled inductors. These currents are the magnetizing currents which determines saturation of the inductive elements. Again due to high inductance assumed for single stage pair coupled topology, the magnetizing currents are relatively smaller than other topologies as shown in Fig 3.6 (a). The differential current in inter-cell transformer coupling looks oscillating although its magnitude is very low. This could be an indication of oscillation in the

corresponding channel currents. One reason for oscillation the controller parameters having larger gain. Another reason is the coupling nature between channels. Being highly coupled in circular mode, any slight sampling error could cause such oscillations. However, as compared to the rated current, these oscillations are very small and their peak is less than the maximum value considered during inductor selection.



(a)



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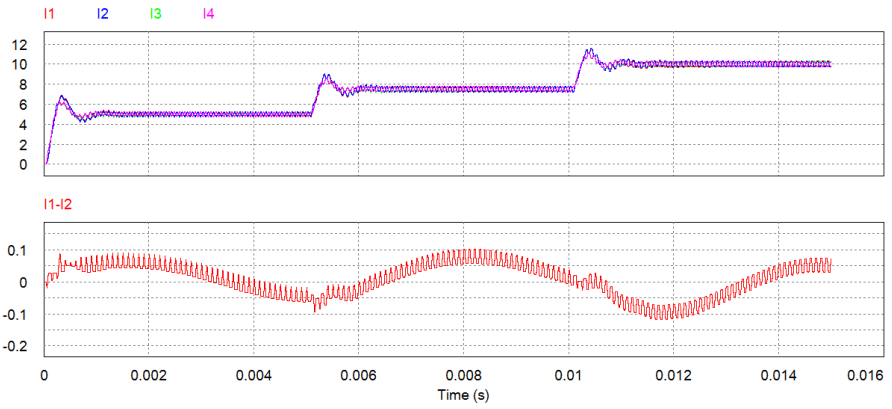


(c)

Fig 3.7 Simulation results for phase shifted sampling (a) Step response for duty change from o.375 to 0.5 (b) Ripple currents for duty ratio of 0.375 (c) differential currents in coupled channels

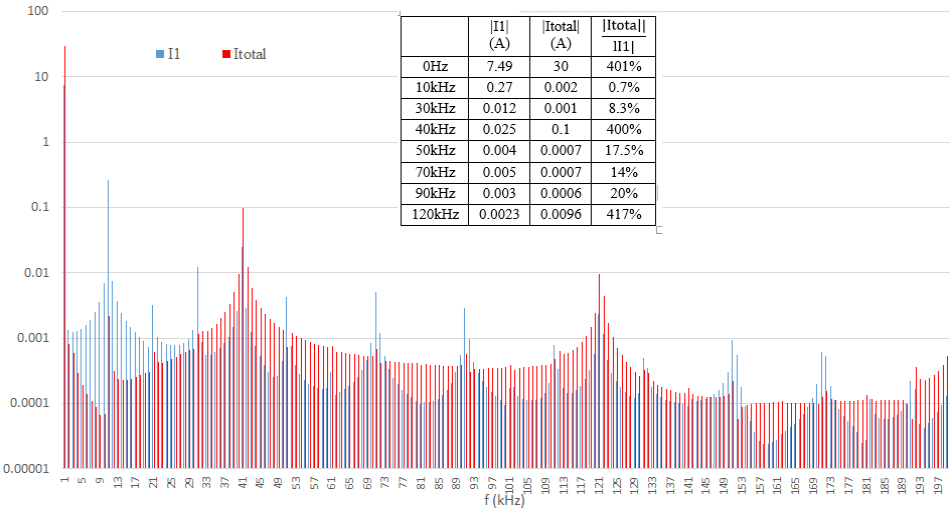
3.5.3. Effect of Sampling

To illustrate effect of sampling, the most commonly used symmetrical sampling method is applied for the converter with single stage pair coupling. This topology is selected as it shows a better inductor volume reduction. However, the technique can be applied to any topology. The sampling instances of each channel are synchronized with their PWM carrier (at peak and valleys). Other parameters are left as they are. The results are shown in Fig 3.7. The overshoot and settling time looks similar to Fig 3.4(b) where simultaneous sampling at 8times the switching frequency is implemented. The differences are more visible in Fig 3.7 (b) where steady state current ripples at duty ratio of 0.375 are zoomed in. There is steady state error between the average value of channel current and the reference. Furthermore, the total current is oscillating at the switching frequency which wasn't the case in the previous discussion. This shows that, sampling is an issue whenever coupled inductors are used in interleaved mode. The issue will be more significant if multiple coupling are to be used such as circular inter-cell or multi-stage pair coupling. The differential currents shown in Fig 3.7 (a) are also higher than what is shown in Fig 3.6 (a). This is due to controllers fighting to meet their own reference based on the sample given to them while the coupling tries to avoid any difference between them.

3.5.4. Harmonic Analysis

To see the harmonic content of the total current and channel currents, the topology based on single stage pair coupling is chosen again. FFT tool from PSIM® is used to analyze steady state signals for a duty cycle of 0.375 at which the total current gives its maximum ripple. The difference in dc component of each channel is in three decimal place (7.501A, 7.497A, 7.498A and 7.50) which shows good current balancing. Fig 3.8 illustrates the remaining harmonics in each channel and in the total output current. The channel current contains harmonics at a multiple of switching frequency and fewer side bands. Although the channel harmonics at 10 kHz is very high, the figure shows that the harmonics in the total current is zero at 10 kHz. If channels were not interleaved the ripple in the total current at 10 kHz would have been four times that of channel ripple at 10 kHz shown in Fig 3.8. But, its first harmonic rather occurred at 40 kHz which shows the effectiveness of interleaving technique in cancelling some harmonics. The higher order harmonics occur at a multiple of 40 kHz (which is equal to number of channel multiplied by the switching frequency).

All harmonics in the total current are too low to violet electromagnetic filter regulations. In a different design, however, it may happen that significant harmonic may appear to violate those regulations. In such situations, adjusting the phase shift between channels slightly will result attenuation of that particular harmonic. Such method helps in minimizing the size of EMC filters required.



	|I1| (A)	|Itotal| (A)	$\frac{\|Itotal\|}{\|I1\|}$
0Hz	7.49	30	401%
10kHz	0.27	0.002	0.7%
30kHz	0.012	0.001	8.3%
40kHz	0.025	0.1	400%
50kHz	0.004	0.0007	17.5%
70kHz	0.005	0.0007	14%
90kHz	0.003	0.0006	20%
120kHz	0.0023	0.0096	417%

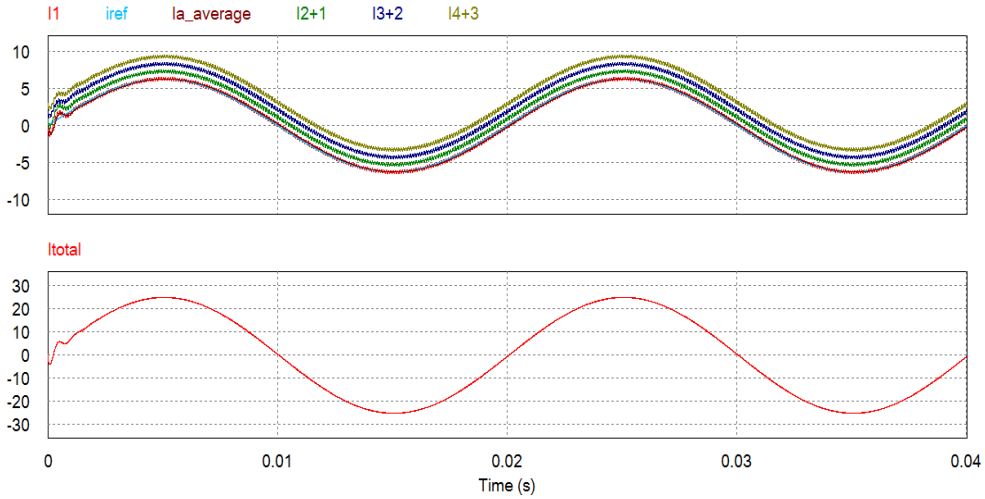
Fig 3.8 Partial current harmonics spectrum of first channel in comparison with the total current for frequency range from 0 to 200 kHz (single stage pair coupling operated as DC/DC)

3.5.5. Half Bridge Inverter

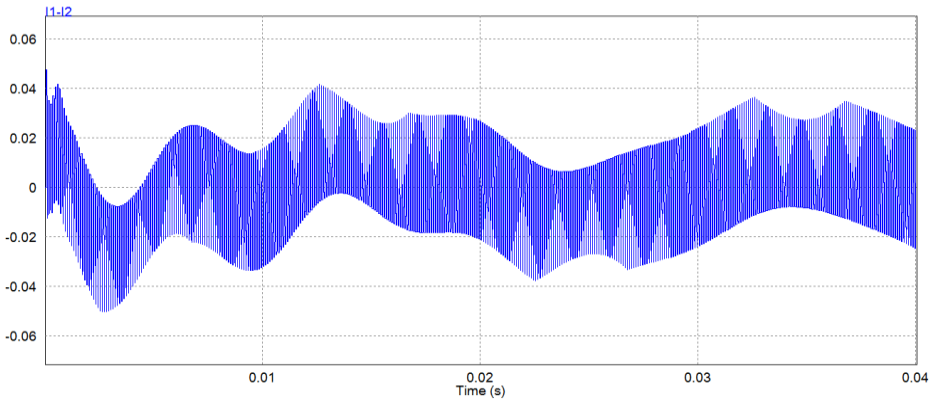
A single stage DC/DC topology with pair coupling is again used to be operated as half bridge inverter. It just needs the negative end of the load to be connected with the midpoint of dc link voltage and changing the reference by sinusoidal. This way, it can be operated as four channel interleaved inverter. Other parameters are left as they are. The peak value of the reference is set at a duty cycle where the total current will have maximum ripple.

Fig 3.8 shows how the ripples look like at the peak value of the reference. The response of the system is shown in Fig 3.9(a) in which each channel currents are shifted up for better view. The response is very smooth and the resultant current is also very smooth. A more detail view is presented in Fig 3.9(c). The coupling effect is similar to what is discussed for DC/DC part. One important thing that Fig 3.9(c) shows is the steady state error due to the delay of PI controller. The reference and the average current looks to have phase delay. This partially the delay of the circular buffers in calculating the average current and partially due to the steady state error of the PI controller. Fig 3.9(b) shows the differential current between coupled channels. Its maximum value is more or less equal to its corresponding value shown in Fig 3.6(a) for DC/DC converters.

FFT result for steady state measurements of the signal is shown in Fig 3.10. The fundamental amplitude for each of the channels is found to be (6.255A, 6.255A, 6.255A and 6.26A) which shows good balancing of channel currents. The remaining harmonics at multiple frequencies of the fundamental (50Hz) are shown in Fig 3.10. Similar to the DC/DC, harmonics at 40 kHz, 80 kHz and 120 kHz are amplified due to overlapping of all channel harmonics.



(a)



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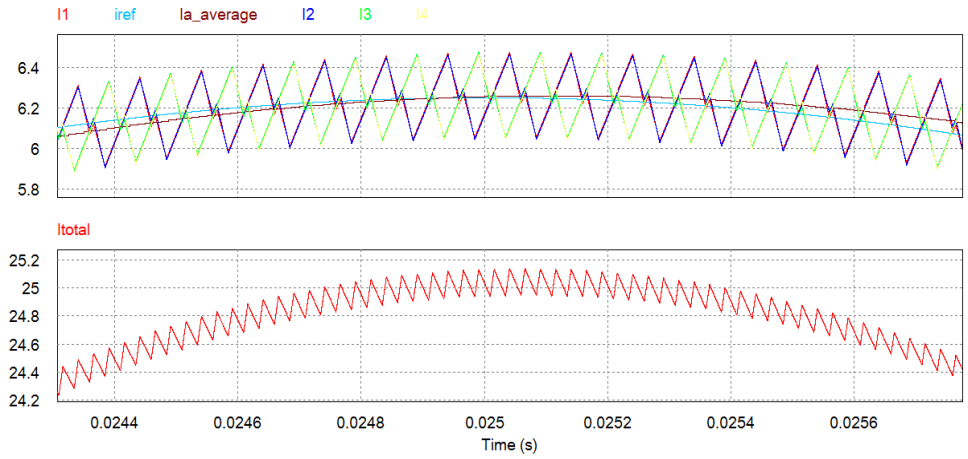
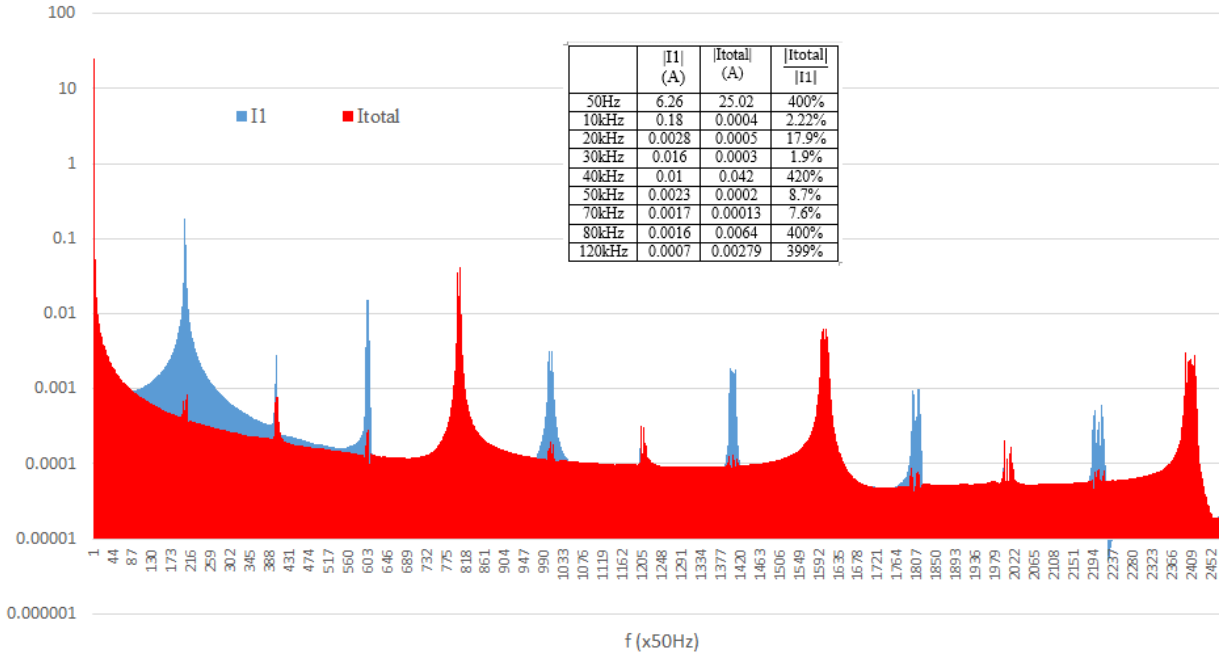


(c)

Fig 3.9 Four channel interleaved inverter using a single stage pair coupling topology (a) response (b) differential current between coupled channels (c) expanded view at the peak

These frequencies are at order of switching frequency multiplied by the number of channels (in this case 4). In additions, the FFT shows lower harmonics at multiples of fundamental frequencies. This is due to fact that the signal length taken is just one period of the fundamental frequency.



	|I1| (A)	|Itotal| (A)	|Itotal| / |I1|
50Hz	6.26	25.02	400%
10kHz	0.18	0.0004	2.22%
20kHz	0.0028	0.0005	17.9%
30kHz	0.016	0.0003	1.9%
40kHz	0.01	0.042	420%
50kHz	0.0023	0.0002	8.7%
70kHz	0.0017	0.00013	7.6%
80kHz	0.0016	0.0064	400%
120kHz	0.0007	0.00279	399%

Fig 3.10 Partial current harmonic spectrum of first channel in comparison with the total current harmonics for frequencies 0 to 120 kHz (single stage pair coupling working as inverter)

3.6. Summary

This chapter covered simulation of different interleaved topologies based on the values of inductance found in Chapter Two. Different sampling techniques were also tasted without changing the controller parameters. Results showed that sampling in synchronization with phase shifted PWM signals resulted poor performance as compared to high rate sampling in which samples taken per switching period are averaged. The FFT analysis was also done both on channel current and the total current. It was shown that the harmonics of the total current occur at the orders of 40 kHz whereas the channel current harmonics are found to add up. On other frequencies than multiples of 40 kHz, the channel harmonics are almost canceled out. The channel current harmonics, on the other hand, occur at the orders of switching frequency (10 kHz). It has also been shown that the level of harmonics in the total current depends on the value of duty cycle.

The next chapter presents how the experimental setup is made to validate the simulation results in terms of total current harmonics versus channel current harmonics. Also, effect of different sampling techniques on the performance of the controller will be tested.

CHAPTER FOUR

4. EXPERIMENTAL SETUPS, MEASURENTS AND DISCUSSIONS

4.1. TMS320F28069 Piccolo Experimenter kit

The DSP used to implement the proposed algorithm is TMS320F28069 from Texas Instruments®. It has F28069 microcontroller card in the form of controlCARD. The experimenter kit is a docking station that features on board USB JTAG emulation, access to all controlCARD signals, breadboard areas and RS-232 and JTAG connectors [38]. The microcontroller can be configured to run up to 90MHz, it has 250KB flash, 100KB RAM, three timers (32bit each), 16 dual sample ADC channels (12 bit each), 8 enhanced ePWM modulator (a total of 16 channel) and many more features [38].

The 8 PWM modulators can be configured independently for different frequency and phase shift. Their compare module gives flexibility in configuring the update interval the type of carrier to be used (saw tooth or triangular). They have also shadow register which enables them to store intermediate duty cycle values before updating instances. A number of events can be generated from each PWM which can be used to synchronize the ADC modules.

The ADC modules operate based on the principle of start of conversion (SOC) and end of conversion (EOC) events. There are 16 SOC which can be configured with events to enable the ADC start conversion of a particular channel on particular events. One ADC input channel can be oversampled by configuring it with two or more SOC. Similarly a single event can be used to configure many SOCs to enable sampling many channels simultaneously. EOC are signals which indicate end of conversion for a particular SOC. The EOC events/signals can be configured to generate interrupts. ADCs can run up to 3.5MSPS (million samples per second) [38].

To implement phase shifted sampling, each ePWM modulator is configured to generate events at the peak and valleys of the corresponding triangular carrier. Those events are used to trigger the corresponding channel in the ADC. At the end of conversion, ADC is configured to generate interrupt so that control algorithm for a particular channel is run and the duty cycles are updated.

To implement sampling at a multiple of switching frequency, one additional ePWM channel is configured to run at the required sampling frequency and generate events on which all channels of the ADC are simultaneously triggered. At the end of each channels conversion, interrupts are again generated so that the corresponding control algorithm is updated. Since no priority is defined, channels will be sampled in their increasing order.

4.2. Digital Controller Implementation

After finding the analog parameters of PI controller, their digital equivalent are found using Tustin approximations. Each control algorithm is run in a separate interrupt service routine where digital to analogue conversions and calibration of sensors take place. To reduce the computational time required for current averaging at high sampling frequency, only updates of old values with new values is done after every sampling. Fig 4.1 shows the flow chart of the code developed. It starts with header file inclusion and is followed by global variable definitions, peripheral initialization, GPIO, ADC and PWM configurations and then waiting for updates. The program runs in infinite loop and watch dog is used to monitor occurrence of program halt at which the program terminates.

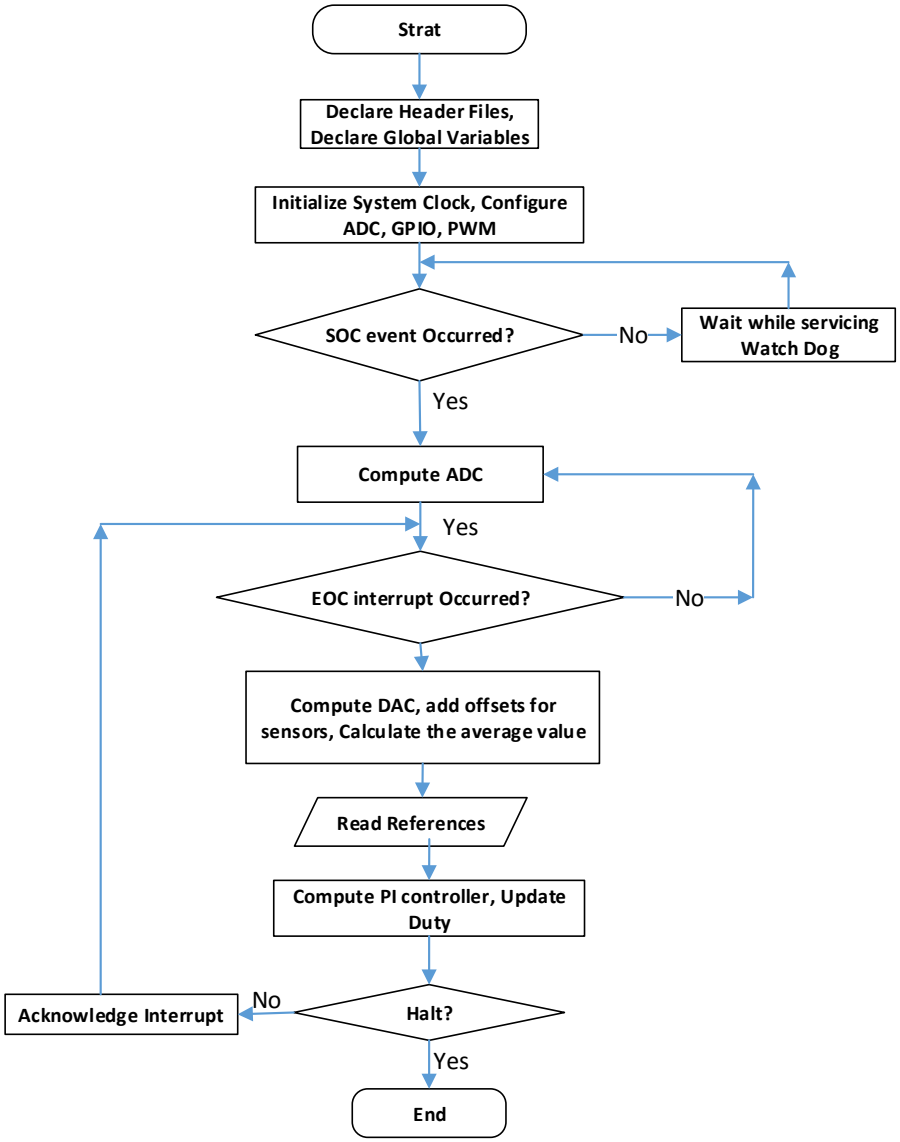


Fig 4.1 Flow chart of the digital controller implemented using Piccolo F28069

4.3. Hardware Setup

Due to time limitation to develop the full four channel topology as proposed in the previous chapters, a prototype is setup with the available power modules and passive elements. Six IGBTs arranged on three legs are used together with three inductor coils (average leakage inductance of 3.8mH and self-inductance of 5.4mH) wound on three limbs. Their inductance varies slightly from one another. The magnetization inductance varies between limbs, but can be assumed equal as they are loosely coupled. In addition, a smaller inductor (about 1.25mH) is used as a common inductor. The dc resistance of inductors is 1.5Ω and 0.5Ω accordingly giving a system time constant of 2.5ms. A 20μF capacitor is connected in parallel with 5.6Ω resistive load. Closed loop hall-effect current sensors are used for three of the channels. Fig 4.2 shows the full hardware setup. A dc voltage source of 60V is used for testing the setup.

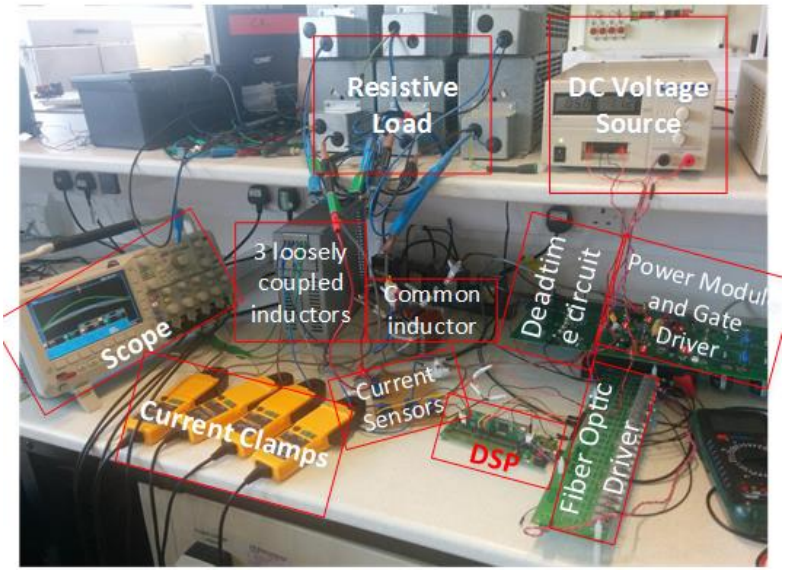


Fig 4.2 Flow chart of the digital controller implemented using Piccolo F28069

Since the sensors have built in antialiasing filter and their outputs match with DSP specification, no additional circuitry is required. However, they need some calibration as they may have offset due to temperature variation. The measured current will be converted into digital value then back to analog inside the DSP. Based on the outputs of PI controller computed inside the DSP, three PWM signals: PWM1A, PWM2A and PWM3A with the required duty cycle and phase shift are generated for upper switches. These signals are fed through the dead time circuit where their complementary signals are generated with dead time for lower switches. This gives six PWM signals: three for the upper switches and three for lower switches with their proper adjustable dead time. The PWM signals are fed to gate driver circuit of the power module. The power module consists of the six IGBTs arranged in half bridge

mode together with dc link capacitors. In addition, the DSP generates one enable signal to enable or disable all the drivers. The overvoltage protection is also included on the board near the power module.

4.4. Measurements and Discussions

As the topology used in the experiment doesn't match with any of the previously discussed topologies, it will be used just to test the algorithms developed and to compare different sampling techniques applied. Both DC/DC and DC/AC measurements are taken. Fig 4.3 shows the open loop response of the system for channel reference current of 1.7A (≈0.5 duty cycle). As it can be seen from mean values of currents in the figure, the channel currents are not balanced and the total current is less than the total reference current. This is partially due to the deadtime which reduces the available pole voltage. The difference between inductor parameters also contributes to this uneven distribution of current. Although the output is not tracking the reference, the ripple cancelation and minimization are still there as shown in the figure. The ripples in the total current have less peak to peak and higher frequency (3times the ripple frequency in each channel). The closed loop implementation is shown in Fig 4.4. Similar results are found for both phase shifted sampling and high frequency simultaneous sampling. Due to the PI controller implemented in closed loop, the deviations observed in open loop are compensated and the reference is well tracked. The currents are not pure triangular waves due to the coupling effect discussed in the previous chapter.

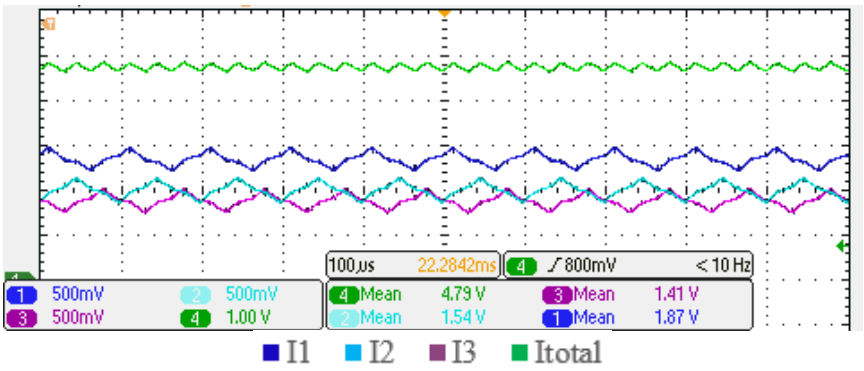


Fig 4.3 Open loop response for DC/DC

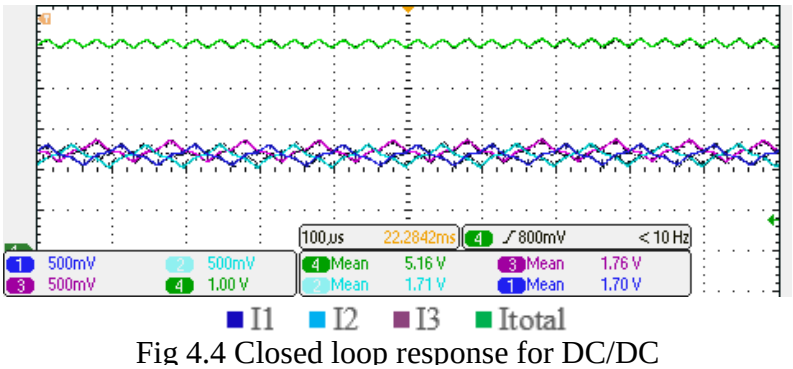


Fig 4.4 Closed loop response for DC/DC

To observe the dynamics of the controller under different sampling techniques, a step change is applied. Fig 4.5 shows output channel and total current wave forms in response to a step change in the reference for phase shifted sampling. The system becomes unstable and oscillating during a step up. This has affected the settling time of the system too. The currents are shifted from each other on vertical axis for better view, otherwise are more or less balanced as shown in Fig 4.5 (b) and (c). The transient looks better on the falling edge as shown in Fig 4.5 (c). Apart from the oscillation, the ripple cancelation is still there and hence, tuning the controller for lower gain could reduce the oscillation.

Different sampling frequencies are tested for simultaneous sampling. Fig 4.6 shows the response of different sampling frequencies for a 10 kHz switching frequency after a step change is applied in the reference. They all have less oscillation as compared with phase shifted sampling. For a better view of steady state oscillations, part of the response which corresponds to a reference input of 1A is magnified as shown in Fig 4.6.

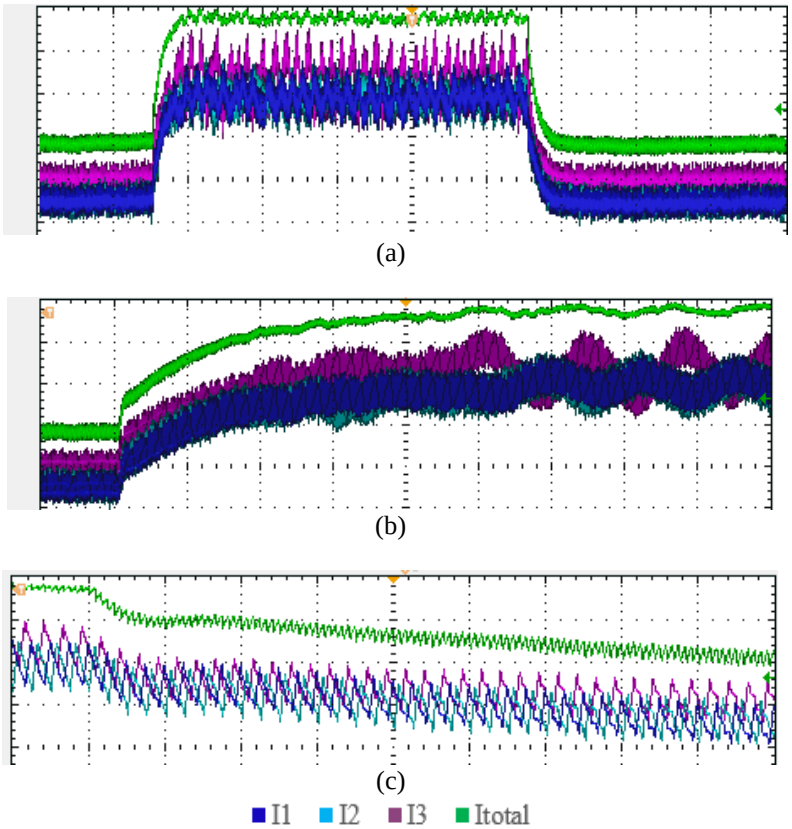


Fig 4.5 System dynamics for a step change in reference from 1A to 1.7A (a) Phase shifted sampling full view (b) expanded view on the rising edge (4ms per division) (c) expanded view of the falling edge (0.4ms per division)

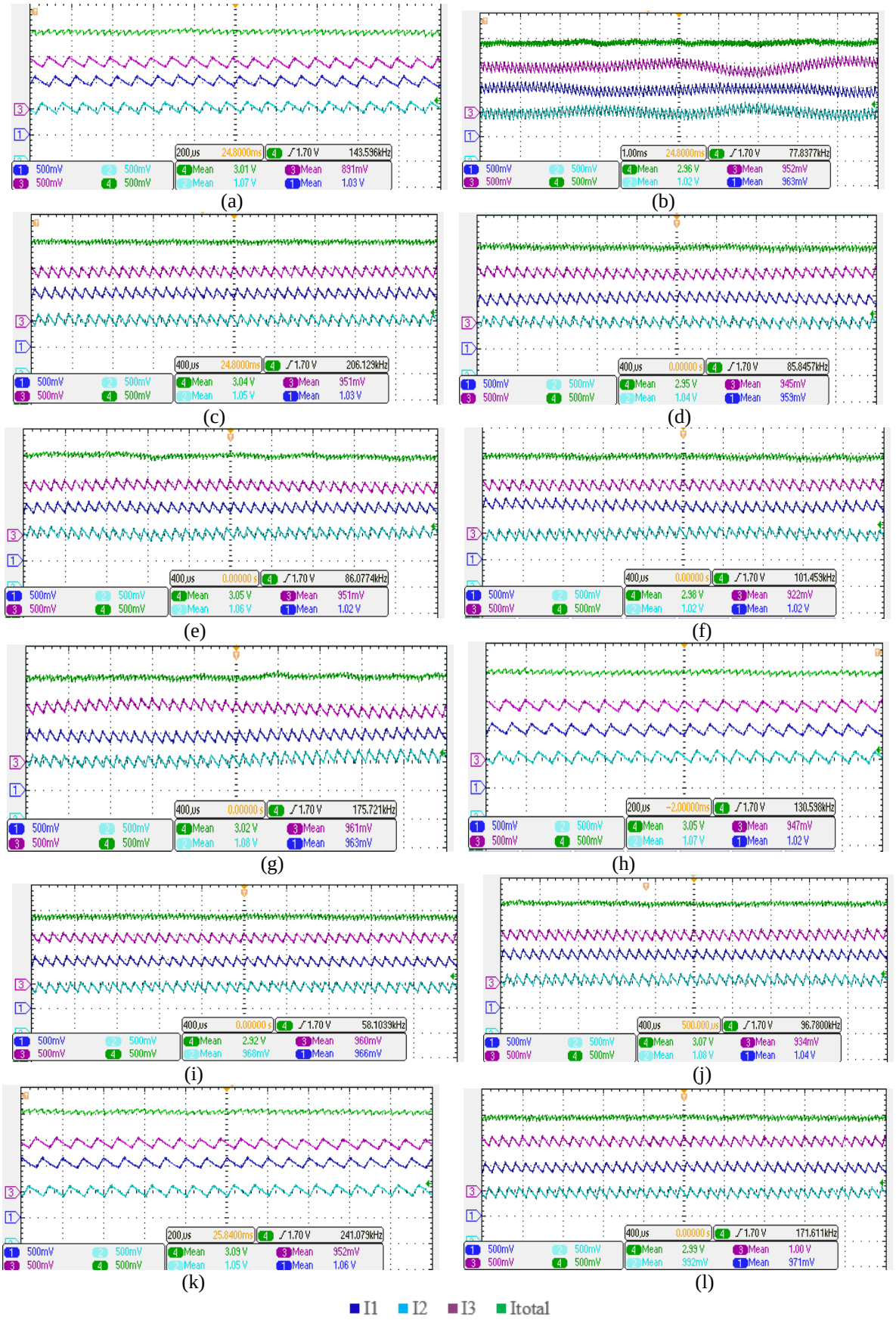


Fig 4.6 Steady state response for a reference input of 1A using simultaneous sampling and averaging over a switching period for different sampling frequencies: (a), (b),…,(l) refres to 10kHz, 20kHz,…,120kHz respectively while switching frequency is maintained at 10kHz

It shows that the worst case is simultaneous sampling at twice of the switching frequency. This could be due to the fact that two of the three inductors are near to each other and hence have higher coupling than the far end. This causes uneven phase shift between phases. Because of this two sampling instances may occur at different levels of channel current (in worst case one at peak current while the other at lower peak).

As the duty cycle is updated twice per switching period, it experiences two different measured currents, hence oscillating trying to meet them. Using the average of the two samples could reduce the difference between the two samples, but the problem still persists. That is why simultaneous sampling at 20 kHz is slightly better than the phase shifted sampling which uses same sampling frequency. These oscillations are very small in steady state. Use of sawtooth carrier signal may reduce this problem which is equivalent to 10 kHz sampling frequency as shown in Fig 4.6 (a). This increases the delay in the PWM module and may result slower response. The other possible solution is to decrease the controller proportional gain so that it acts less for small changes (i.e. decreasing the bandwidth) which again affects the transient response of the system.

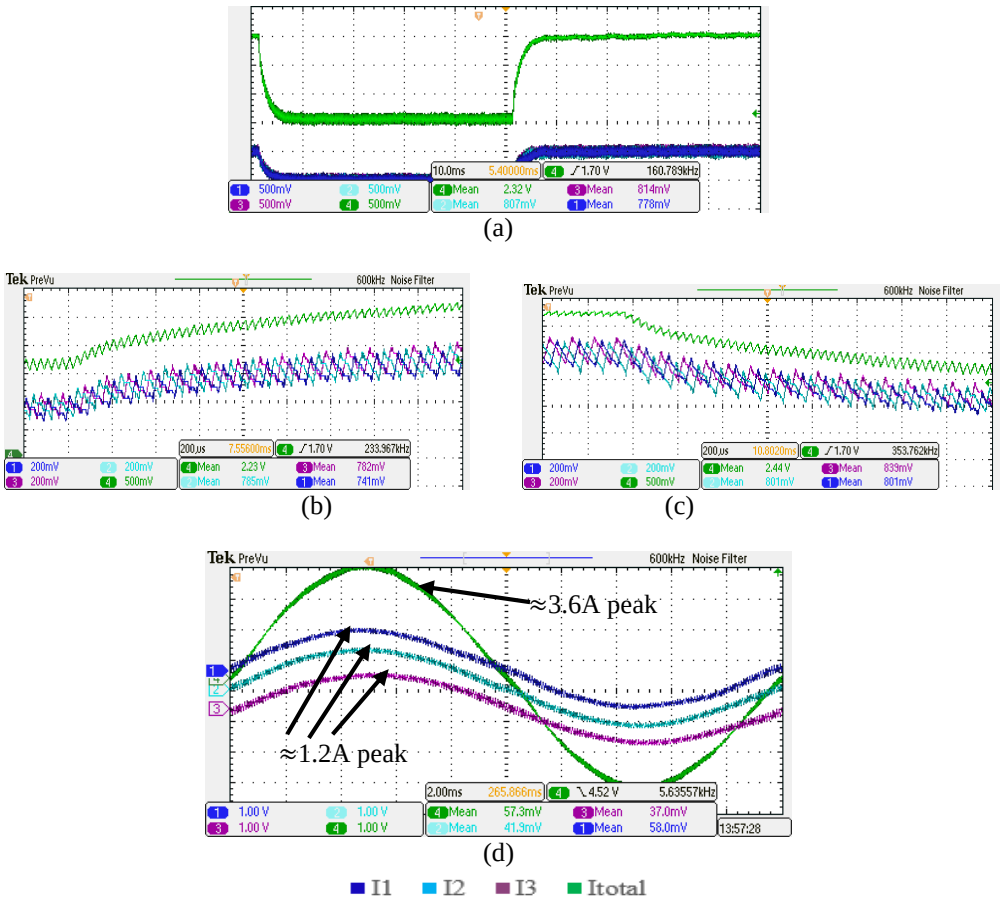
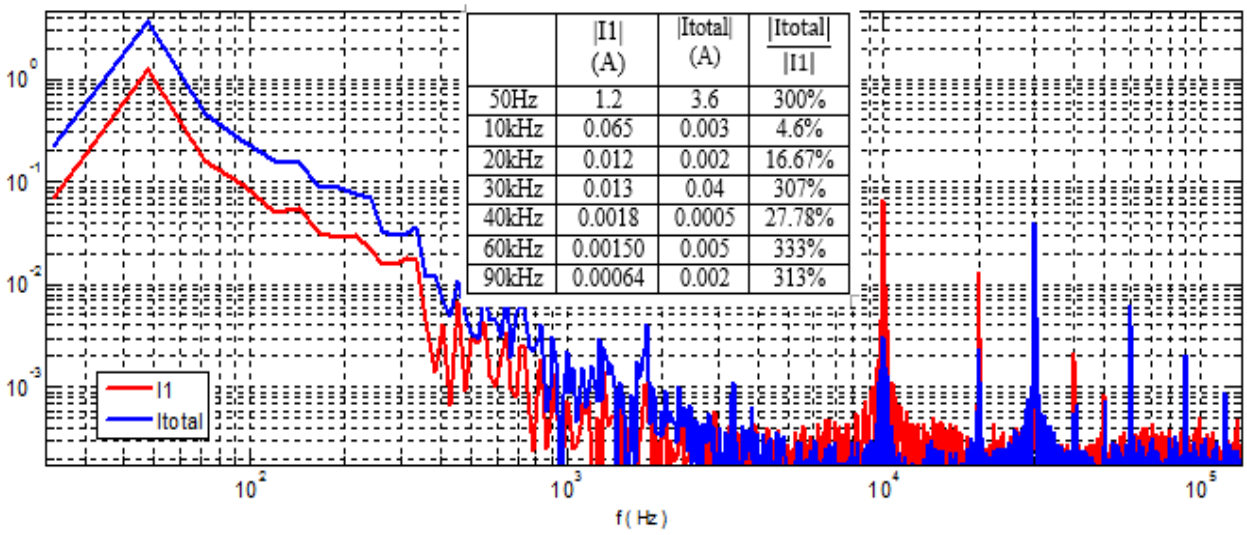


Fig 4.7 System dynamics for a step change in channel reference from 0.5A to 1.0A (a) Sampling at 30 kHz (b) expanded view on the rising edge (c) expanded view of the falling edge (d) operating as three channel interleaved half bridge inverter

Generally, better balance in channel currents and less oscillations are observed for higher sampling frequencies, in particular at those frequencies which are integer multiples of both switching frequency and number of channels (in this case, at 30kHz, 60kHz, 90kHz and so on). At very high frequencies, however, the difference becomes insignificant as shown in Fig 3.15 (h) to (l). The system dynamics at 30 kHz sampling frequency is shown in Fig 4.7. The wave forms shown in Fig 4.7 (a) to (c) are all for DC/DC operation and shows smooth transients with rising and falling time of approximately 2.5ms (nearly equal to the time constant of the system). Fig 4.7(d) shows the results when the converter is operated as half bride inverter.

Harmonics content in the output current is analyzed by feeding the measured data to MATLAB® and applying FFT function. Fig 4.8 shows the results of FFT analysis for the inverter mode operation for which the output currents are shown in Fig 4.7 (d). As it can be seen from Fig 4.8, the harmonic contents are insignificant as compared to the fundamental. It shows that the total current fundamental is three times of the channel current fundamental. Chanel current harmonics which occur at multiple of 30 kHz are add up in the total current while the remaining harmonics get nearly canceled but not totally. The harmonics in the channel current occur at multiples of switching frequency while the total current harmonics occur at multiples of 30 kHz. This matches with the analytical and simulation results. The channel current ripples are added up at high order switching frequencies which are multiples of channel number.



	|I1| (A)	|Itotal| (A)	|Itotal| / |I1|
50Hz	1.2	3.6	300%
10kHz	0.065	0.003	4.6%
20kHz	0.012	0.002	16.67%
30kHz	0.013	0.04	307%
40kHz	0.0018	0.0005	27.78%
60kHz	0.00150	0.005	333%
90kHz	0.00064	0.002	313%

Fig 4.8 Partial harmonic spectrum for channel current and total current from 0 to 100 kHz the converter operating as inverter (measurement shown in Fig 4.7(d))

4.5.Summary

This chapter described how the experimental setup was done with the available materials. It described how the control algorithm and sampling techniques were implemented. The methodologies developed in the previous chapters were implemented, except for different values of inductors. Measurement results are found to match with the simulation results. Harmonics in the total current are found at the order of switching frequency multiplied by the number of channels. At these frequencies, the channel current harmonics were adding up. Sampling at higher rate and averaging over a switching period showed better performance as compared to phase shifted sampling. The next chapter summarizes the main points of the thesis work.

CHAPTER FIVE

5. SUMMARY AND CONCLUSION

In this thesis work, challenges of multi-channel interleaved power converters are investigated and a method of implementing them is proposed which uses commonly available digital platforms, such as Piccolo F38069 from Texas Instruments. Different topologies for implementing interleaved power converters were analyzed and simulated. Bidirectional interleaved power converters using uncoupled inductors, using inter-cell transformers, single stage pair coupling and multistage pair coupling are discussed analytically and using simulation.

Equivalent volume of an inductor is used as a parameter to compare different topologies. Use of coupled inductors is found to have significant volume reduction as compared with uncoupled inductors. Among the coupled topologies themselves, the one with single stage pair coupling is found to be the best in volume reduction. It shows a 60% volume save over its non-interleaved counterpart. Inter-cell transformers and multistage pair coupling topologies resulted 35% and 22% volume save as compared to the non-interleaved coupled inductors, respectively. These results could be further tuned by using a more detail model of volume of an inductor, especially when the magnetizing current is nearly zero.

Independent current controllers per channel are implemented to balance the channel currents, which is otherwise impossible due to the mismatch of inductor parameters. Phase margin and gain margin are used to tune the PI controllers. Their equivalent digital controller is found using Tustin approximations. It has been showed that the inductor parameter that determines the system response of power converter is the leakage inductance (for coupled inductors) or self-inductance (for uncoupled) of the channel inductor connected near the corresponding pole. Thus, increasing the value of such inductances slows the system response. However, designing the system of inductors by putting such higher value of inductance in each channels will be rated at lower rms current, and hence, resulting lower volume. Further optimization may be required to get better combination of system performance and power density.

While the leakage inductance of coupled inductors determines the performance of the system and the current ripples in each channel, the magnetization inductance highly affects the differential currents. Because of this, the current through highly coupled channels are found to be nearly in phase with each other regardless of the phase shift in their PWM carrier signals. This made phase shifted sampling to give sampling errors leading the system into oscillation. Different sampling techniques were simulated and tested experimentally to mitigate these sampling errors. It has been demonstrated that sampling at

higher frequencies and averaging them over the switching period has better system response. Both simulation and experimental setup has proved that using high sampling frequency, equal to an integer multiple of both the number of channel and switching frequency, mitigates the sampling errors. As most of the DSPs run in tens of MHz clock frequency, higher sampling frequencies up to hundreds of kHz can be implemented.

FFT analysis is carried out for both simulation and experimental measurements revealing that the channel current ripples are at switching frequencies while total current ripples frequencies are at channel number multiplied by switching frequency. This makes the required filter size (if any) to be very small.

This thesis work is limited to investigating the general challenge of interleaved power converters from volume reduction and digital implementation points of view. System modeling is based on the assumption of ideal inductors, although the experimental findings validated that assumption true. Due to time limitations, the exact proposed topologies are not implemented. Performance measurements in terms of power loss is not covered.

Further researches could be done on the topic by including non-ideal nature of passive elements, considering different design approaches of inductors and comparing their efficiency. More advanced controllers can be investigated for further improvement of system response while operating as inverter. Voltage controllers can also be added to give it a wider application. Inverter mode operation could also be extended to grid synchronization. Comparison against other candidate topologies for low power applications such as multi-level power converters can also be further investigated.

All in all, interleaved power converters using coupled inductors with simultaneous sampling and averaging over a switching period mitigates the problem of circulating currents and sampling errors associated with interleaved power converters. Use of single stage pair coupling could give potential volume reduction both on the system inductors and filter inductors. Such topologies are better than any other topologies for high power, high current applications. They can also be good candidates for low power applications. Being operated in parallel and having less system inductance, multichannel interleaved power converters gives improved performance, better reliability and higher power density.

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