

Quadrature Signal Generator based on All-Pass Filter for Single-Phase Synchronization

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Abstract—Precise calculation of the grid voltage magnitude and phase is required for the operation of distributed power generation (DPG) systems. While the general concepts involved in the synchronization of single-phase and three-phase systems are the same, the practical implementation can differ substantially, the single-phase case being more challenging. Phase-locked-loop (PLL) based methods have been widely used for the synchronization of single-phase systems. These methods can be roughly grouped into methods that use a quadrature signal generator (QSG) and methods that implement a single-phase PLL. One drawback of single-phase PLL methods is that they usually produce a component at twice the fundamental frequency that needs to be removed. On the contrary, QSG methods do not induce such component, enabling therefore the use of three-phase PLLs. On the other hand, the phase error usually depends on the input magnitude for both methods.

This paper proposes a QSG based single-phase synchronization technique that overcomes the aforementioned limitations of both single-phase PLLs and QSGs. It will be shown that the proposed method accurately estimates the magnitude and phase of the microgrid/grid fundamental voltage with high dynamic response, even under high distorted conditions.

Index Terms—Phase locked loops, single-phase system, filtering algorithms, harmonic filters, delay compensation

I. INTRODUCTION

ELECTRICITY demand has been continuously increasing during last years and is expected to keep rising [1]. One of the environmental priorities for the following decade is shifting to a low CO₂ generation scenario. A wide accepted mechanism to reduce the electrical losses and therefore the emissions is the Distributed Power Generation (DPG) paradigm, where small or medium-size generation spots are located close to the customers. The DPG units can be installed in the customer side, creating a small-scale, single-phase low voltage system, which can combine renewable and non-renewable energy resources, e.g. micro-photovoltaic, micro-wind, biomass, fuel cells, micro-gas turbines... This concept is usually referred as microgeneration [2]. Microgeneration development will boost the customers to become an autonomous entity with the capability not only of demanding but also of generating, storing and/or exporting energy to the grid. Although microgeneration technology is already developed and commercialized, domestic generation is

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still at an early stage. Large costs often combined with a lack of normative and infrastructure for bilateral trading at the customer side are the main limitations for the microgeneration concept spreading [3].

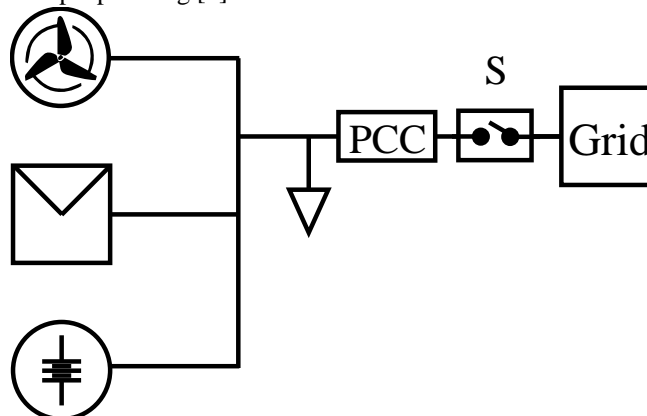


Fig. 1- Generic microgrid.

The coordinated operation of all the participants in a microgeneration (generators, loads, storage...) fits into the microgrid definition [2]. Depending on the physical connection to the utility grid (see Fig. 1), a microgrid can operate isolated or grid-connected [4]. In island mode the magnitude and frequency of the fundamental voltage are set by the microgenerator acting as the master of the microgrid [4], the microgrid operating as an autonomous system. On the contrary, in grid-connected mode the magnitude and frequency of the fundamental voltage are set by the grid [4].

Obtaining a precise and fast estimation of the fundamental voltage magnitude and phase at the PCC, both in island and grid connected modes, is essential for an accurate power flow control. While this is relatively simple for the case of pure sinusoidal grid voltages, harmonics, frequency shifts and magnitude deviations often occur at the point of common coupling (PCC) in practice, e.g. due to non-linear loads or connection/disconnection of big loads, making it a significantly more challenging task.

A large number of single-phase synchronization methods have been proposed [7]-[13], phase-locked-loop (PLL) based techniques being the most popular due to their simplicity and robustness. Both single-phase and three-phase PLLs can be used in single-phase grids.

Single-phase PLLs can have several limitations. A component at twice the fundamental frequency is induced in the estimated frequency/phase. Also, some of them are not frequency-adaptive. Finally, the phase error is affected by the input magnitude, providing therefore poor performance in the event of magnitude and/or frequency deviations.

The use of three-phase PLL based methods for single-phase systems, requires the emulation of a three-phase balanced system. This can be achieved by making the β component of the voltage complex vector equal to zero, or by using a quadrature/orthogonal signal generator (QSG/OSG) [12]. The first solution has the drawback that an unwanted harmonic term is induced in the frequency estimated by the PLL that must be removed. On the other hand, the QSG structures are not typically frequency adaptive, and can be difficult to implement.

In this paper, a new adaptive single-phase synchronization method with disturbance rejection capability is proposed. The method uses a QSG, a modified Angle Tracking Observer (ATO) is included to make the angle error independent of the input magnitude. In addition, a Phase Delay Compensator (PDC) is included to correct the delay introduced by the filtering stage.

The paper is organized as follows. The basics of the method, including the design of the QSG, the filtering process and the PDC are presented in Section II. Simulation and experimental results to validate the proposed method are given in Sections III and IV respectively. Finally, Section V presents the conclusions.

II. SINGLE-PHASE SYNCHRONIZATION USING A THREE-PHASE PLL WITH ANGLE TRACKING OBSERVER AND PHASE DELAY COMPENSATION

Fig. 2 shows the proposed single-phase synchronization method, called “*First-Order All-Pass Phase Locked Loop*” (FOAP-PLL). It consists of four major blocks; a) QSG to emulate a three-phase balanced system; b) modified three-phase ATO [13] to estimate the frequency and phase of the input signal; c) Pre-filter stage (PFS) to remove the voltage harmonics; d) PDC to compensate the phase delay introduced by the PFS. They are discussed following.

A. Quadrature signal generator (QSG)

To use a three-phase PLL in a single-phase system, a

fictitious $\alpha\beta$ stationary reference frame needs to be defined. This can be done by making the α component equal to the phase voltage and the β component equal to zero [9]. However, this produces a mirror-frequency term in the obtained voltage vector, which needs to be removed, a filter or a decoupling network can be used for this purpose. Alternatively, it is possible to avoid the mirror-frequency by making the β component (quadrature signal) equal to the α component shifted 90 degrees. Several approaches have been proposed to achieve this:

- Transport delay block [11]. This method delays the input signal a number of samples corresponding to one fourth of the fundamental component period. Limitations of this method are an increased sensitivity to frequency deviations unless some form of frequency adaptation is implemented, and the need of a relatively large buffer.

- Hilbert transform [10]. It is possible to generate the quadrature component by using the Hilbert transform, which is a non-causal system, being therefore not practically feasible. A discrete realization of the Hilbert transform can be implemented by using causal FIR filters. However, they have high complexity and a substantial computational time.

- Inverse-Park generation [11]. The quadrature component is obtained using the inverse Park transformation of a three-phase balanced system. Its main disadvantage is that it uses two low-pass filters (LPF), making the tuning (LPFs and PI gain selection) difficult due to the presence of two coupled nonlinear loops.

- Second order generalized integrator (SOGI) [12]. The quadrature component is generated by a block which acts as a variable-frequency band-pass filter, whose output is shifted 90 degrees. Its main drawback is that it does not provide a mechanism to compensate harmonics.

To overcome the aforementioned limitations, the use of an All-Pass Filter QSG (APF-QSG) is proposed. The all-pass filter is a powerful tool that has been used in other fields like audio processing, speech coding, and time delay estimation [15]-[16]. The general form of an analog first order all-pass

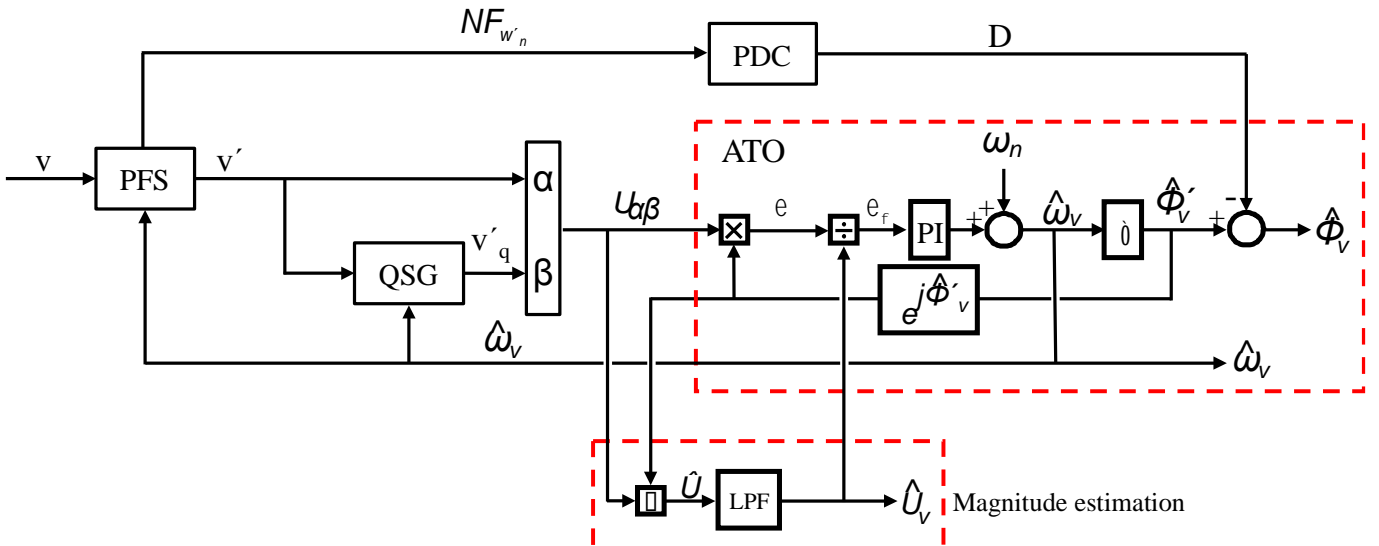


Fig. 2 –FOAP-PLL control structure

filter is shown in (1). Its main feature is that it provides unit gain for all frequencies (2) and the phase response is given by (3). At the ω_q frequency, often referred as the corner frequency, the all-pass filter shifts 90 degrees the input signal.

$$APF_q(s) = \frac{s - \omega_q}{s + \omega_q} \quad (1)$$

$$\left| APF_q(\omega) \right| = 1 \quad (2)$$

$$\angle APF_q(\omega) = \angle_{QSG} = 180 - 2\arctan\left(\frac{\omega}{\omega_q}\right) \quad (3)$$

Fig. 3 shows the APF frequency response function when ω_q equals the fundamental component (e.g. 50 Hz), it is observed that there is a 90 degrees phase shift at the fundamental frequency. The phase angle for the higher order harmonics is given by (3). It is clear from (3) that errors in the phase angle of the quadrature component will occur if the actual grid frequency is different from the ω_q in (1). A real time estimation of the corner frequency is therefore required. The frequency estimated by the PLL $\hat{\omega}_v$ (see Fig. 2) will be used for this purpose.

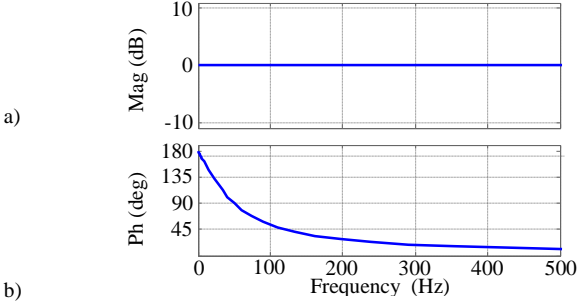


Fig. 3- a) Magnitude and b) phase of the frequency response function of an APF

B. Three-phase ATO

This subsection presents the three-phase ATO used in this paper. For discussion purposes, it will be first assumed that the QSG input signal (4) (v' in Fig. 2), consists of the fundamental component and a harmonic component of order n , where θ_1 and θ_n are the phases of the fundamental component and the n^{th} harmonic respectively. It is also assumed that the QSG corner frequency matches the fundamental frequency. Thus the QSG output and the fundamental component of the voltage, v'_q are 90 degrees phase, while the n^{th} harmonic at the APF-QSG output is shifted Φ_{QSG} degrees (3) respect to the input. $u_{\alpha\beta}$ complex voltage vector is given by (5).

$$v = U_1 \cos(\omega_0 t - q_1) + U_n \cos(n\omega_0 t - q_n) \quad (4)$$

$$v_q = U_1 \cos(\omega_0 t - q_1 - \frac{\rho}{2}) + U_n \cos(n\omega_0 t - q_n - \angle_{QSG}) \quad (5)$$

$$u_{\alpha\beta} = \alpha + j\beta = v' + jv'_q \quad (6)$$

$$u_{ab} = U_1 \times e^{j\omega_0 t} + U'_n \times e^{jn\omega_0 t} + U'_n \times e^{-jn\omega_0 t} \quad (7)$$

Assuming $\theta_1 = \theta_n = 0$, the resulting $u_{\alpha\beta}$ voltage complex vector consist of three components (7): a component rotating at the fundamental frequency of magnitude of U_1 and two

components rotating at $-\omega_0$ and ω_0 respectively, their magnitudes depending on Φ_{QSG} since the QSG creates a harmonic component that is not in quadrature with the harmonic input (3) (see Fig. 2b).

An ATO is used to estimate the frequency and phase of the fundamental component (U_1) [13]. The error signal (8) (see Fig. 3) is obtained as the vector cross-product between the input signal ($u_{\alpha\beta}$) and the estimated unitary vector ($e^{j\hat{\theta}_v}$), whose phase is the estimated phase of the input signal. The error signal (ε_ϕ) is normalized by using the estimated fundamental voltage magnitude (\hat{U}_1), therefore making the phase error independent of the input magnitude. Assuming perfect tracking of the fundamental component, i.e. $\hat{\theta}_v = \omega_0 t$, the error signal (8) can be expressed as (9). It is observed that the phase error consists of two harmonic components of orders $n \pm 1$. It is noted that if the QSG input signal, v' , contains more than one harmonic component, each input harmonic of order n will produce two harmonics of order $n \pm 1$ in the phase error signal.

$$e_\phi = \frac{u_{ab} \cdot \ddot{A} e^{j\hat{\theta}_v}}{\hat{U}_1} = \frac{\text{Re}\{u_{ab}\} \times \sin(\hat{\theta}_v) - \text{Im}\{u_{ab}\} \times \cos(\hat{\theta}_v)}{\hat{U}_1} =$$

$$= \frac{\sin(\hat{\theta}_v)}{\hat{U}_1} [U_1 \cos(\omega_0 \cdot t) + U_n \cos(n \cdot \omega_0 \cdot t)] -$$

$$- \frac{\cos(\hat{\theta}_v)}{\hat{U}_1} [U_1 \sin(\omega_0 \cdot t) + U_n \cos(n \cdot \omega_0 \cdot t - \angle_{QSG})] \quad (8)$$

$$e_\phi = \frac{U_n}{\hat{U}_1} \cdot 2 \left[\sin((n+1) \cdot \omega_0 \cdot t) - \sin((n-1) \cdot \omega_0 \cdot t) - \right.$$

$$\left. - \cos((n+1) \cdot \omega_0 \cdot t - \angle_{QSG}) - \cos((n-1) \cdot \omega_0 \cdot t - \angle_{QSG}) \right] \quad (9)$$

$$\hat{U} = u_{ab} \times e^{j\hat{\theta}_v} = \text{Re}\{u_{ab}\} \times \cos(\hat{\theta}_v) + \text{Im}\{u_{ab}\} \times \sin(\hat{\theta}_v) \quad (10)$$

$$\hat{U} = U_1 + \frac{U_n}{2} \left[\cos((n+1) \cdot \omega_0 \cdot t) + \cos((n-1) \cdot \omega_0 \cdot t) + \right.$$

$$\left. + \sin((n+1) \cdot \omega_0 \cdot t - \angle_{QSG}) - \sin((n-1) \cdot \omega_0 \cdot t - \angle_{QSG}) \right] \quad (11)$$

To estimate the magnitude of the fundamental voltage component (\hat{U} in Fig. 2), a scalar product between the grid voltage $u_{\alpha\beta}$ and the unit vector $e^{j\hat{\theta}_v}$ is used (10) (see Fig. 2). The estimated magnitude, \hat{U} , consists of a DC component, whose magnitude is equal to the magnitude of the fundamental component of the grid voltage (U_1) and two harmonic components of orders $n \pm 1$. If the input voltage consists of more than one frequency component, each harmonic of order n will produce two harmonics of order $n \pm 1$ in the estimated magnitude. Since the harmonic components will be removed by the PFS discussed following, low-pass filters (LPF) would only be required to remove noise coming from the sensors and electronics.

C. Pre-Filter Stage (PFS)

A potential mechanism for harmonic rejection in the proposed method is to reduce the ATO PI controller bandwidth. However, this solution is unsatisfactory as the microgenerator stability relies on the ATO dynamic response.

In addition, the output APF-QSG quadrature signal depends on the estimated ATO frequency. Therefore, the implementation of a specific mechanism to remove the harmonic content from the input voltage is advisable.

Two different approaches are typically used for harmonic rejection: a pre-filter stage [14] or a filter within the PLL loop [13]. Being N the number of harmonics to be removed, a pre-filter stage configuration requires N notch filters while the filter in the PLL loop configuration requires $2(N+1)$ filters. Therefore, a pre-filter configuration will be used as it is advantageous in this regards and.

Selection of the number of notch filters to be used can be made based on power quality standards. The international standards for grid-connected power converters [5]-[6] limit the maximum overall voltage harmonic distortion (THD) to 5%, with each individual harmonic magnitude being smaller than 4% for harmonic orders lower than 11th, 2% for harmonic orders between 11th and 17th, 1.5% for harmonic orders between 17th and 23rd, 0.6% for harmonic orders between 23rd and 35th and 0.3% for orders higher than 35th. Three notch filters (12), corresponding to $\omega_3=3 \omega_0$ (150 Hz), $\omega_5=5 \omega_0$ (250 Hz) and $\omega_7=7 \omega_0$ (350 Hz), will be implemented in this work [13].

$$NF_{\omega_n}(z) = b \frac{1 - 2 \cdot \cos(\omega_n) z^{-1} + z^{-2}}{1 - 2 \cdot b \cdot \cos(\omega_n) z^{-1} + (2 \cdot b - 1) z^{-2}} \quad (12)$$

$$\hat{\omega}_n = \frac{2}{T_s} \cdot \tan\left(\omega_n \cdot \frac{T_s}{2}\right); \omega_n = \frac{n \cdot \omega_0}{f_s/2} \quad (13)$$

$$b = \frac{1}{1 + b} \quad (14)$$

$$b = \frac{\sqrt{1 - A_{-3dB}^2} \tan\left(\frac{BW}{2}\right)}{A_{-3dB}}; BW = \frac{DW}{f_s/2} \quad (15)$$

D. Phase Delay Compensator (PDC)

The delay introduced by the filtering stage discussed previously can adversely impact the performance of the method, implementation of a phase delay compensation strategy being therefore advisable. The phase delay is estimated from the filter transfer function (12) in real time and later compensated (see Fig. 2). Substituting (16) into the notch filter transfer function, (12) is obtained. By separating the numerator and denominator of the filter transfer function into their real and imaginary components, (17), the notch filter phase delay D at the grid frequency is obtained using (18).

$$z = e^{j\hat{\omega}_n T_s} = \cos(\hat{\omega}_n T_s) + j \cdot \sin(\hat{\omega}_n T_s) \quad (16)$$

$$NF_{\omega_n} = \frac{\text{real}(\text{num}) + j \times \text{imag}(\text{num})}{\text{real}(\text{den}) + j \times \text{imag}(\text{den})} \quad (17)$$

$$D = \tan^{-1}\left(\frac{\text{imag}(\text{num})}{\text{real}(\text{num})}\right) - \tan^{-1}\left(\frac{\text{imag}(\text{den})}{\text{real}(\text{den})}\right) \quad (18)$$

III. SIMULATION ANALYSIS UNDER GRID DISTORTED CONDITIONS

Fig. 4 and Table I show the configuration used for the

simulation of the proposed method. A programmable AC source is used to produce different disturbances in the grid voltage, including 1) grid voltage magnitude deviations, 2) grid frequency deviations and 3) harmonics. As already mentioned, the pre-filter stage was designed to reject the 3rd, 5th and 7th harmonics, the magnitude of the disturbances have been selected to comply with the grid codes [5]-[6].

In the simulation and experimental results following, magnitudes and frequencies are shown in per unit relative to the rated grid voltage and frequency (i.e. 220 V and 50 Hz).

Fig. 5 shows the simulation results when the AC source produces a step-like change in the output voltage magnitude. Fig. 5a shows both the grid voltage (v_g in Fig. 4) (black) and the voltage estimated by the proposed method ($v_{\mu g}$ in Fig. 4) (red). Figs. 6b-6d show the magnitude, frequency and phase error. It is observed from Fig. 5b that the maximum magnitude error is 0.055 p.u., being below 0.03 p.u. in around 5 ms. Also, a maximum error in the estimated frequency of ≈ 0.05 p.u. is observed (see Fig. 5c), which is compensated by the ATO PI controller after 5 ms. Finally, the maximum transient phase error is ≈ 2 degrees (Fig. 5d) which is also compensated by the ATO in less than 5 ms.

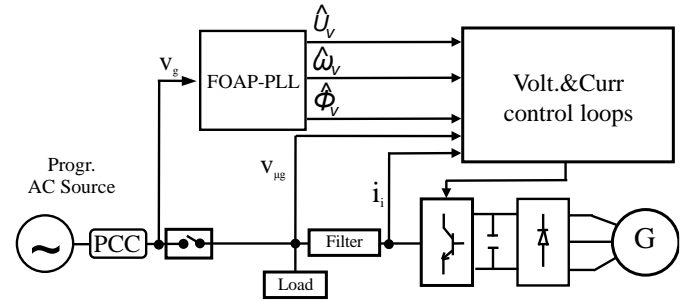


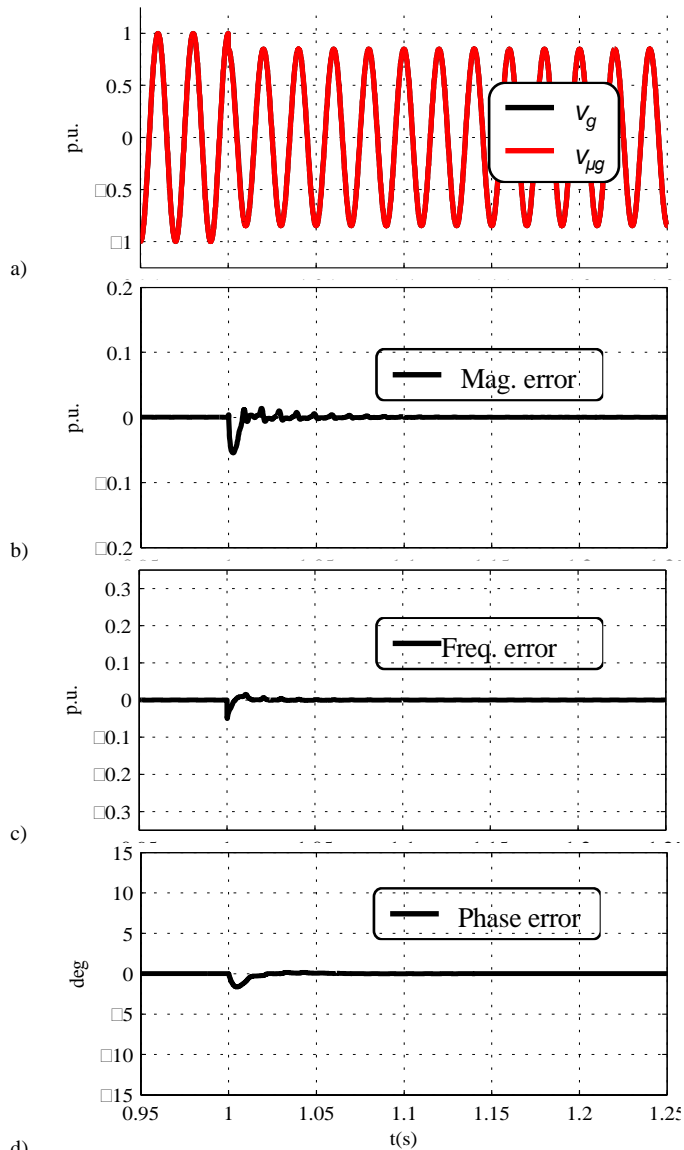
Fig. 4- Simulation setup.

TABLE I
SIMULATION AND EXPERIMENTAL SETUP PARAMETERS

Symbol	Description	Value
L_i	Inverter side filter inductance	2.196 mH
R_i	Inverter side filter resistance	0.05 Ω
C	Capacitor Filter	10 μ F
R_c	Capacitor ESR	0.0536 Ω
L_g	Grid side filter inductance	1.3 mH
R_g	Grid side filter resistance	0.05 Ω
	Positive sequence voltage magnitude (rms)	230 V
DW	Notch Filter bandwidth	10 Hz
	Magnitude low-pass filter bandwidth	1000 Hz
K_p	ATO proportional gain	100
K_i	ATO integral gain	5000

Figs. 7 and 8 show the simulation results for the case of a step-like frequency change. Fig. 6 shows the performance of the proposed QSG and PDC blocks. Fig. 6a shows the input and output signals to the QSG block, a 90 degrees phase shift between v'_q and v' is observed, independently of the input signal frequency

Fig. 6b shows the phase shifts obtained by the PDC block for each notch filter and the total phase delay. The phase shifts agree with the theoretical ones given by (18). It is observed that the resulting phase delay is frequency-dependent

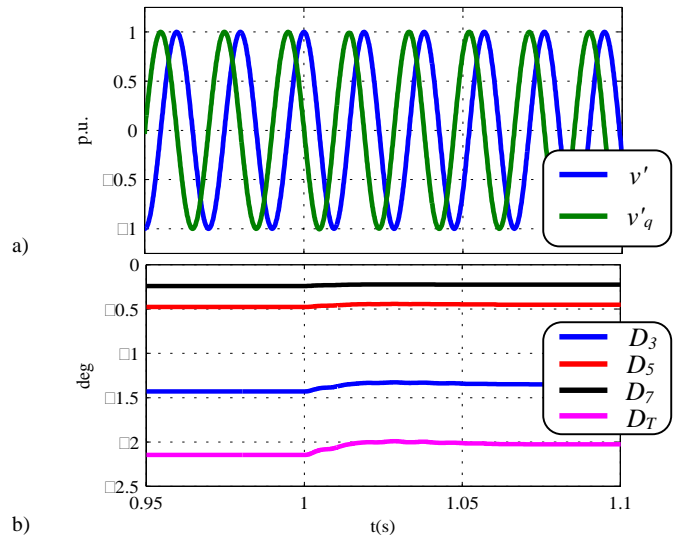


d) Fig. 5- Simulation results showing the response to a step-like change in the output voltage magnitude from 1 p.u. to 0.85 p.u. at $t=1$ s: a) actual v_g and estimated grid voltages $v_{\mu g}$, b) magnitude error, c) frequency error and d) phase error.

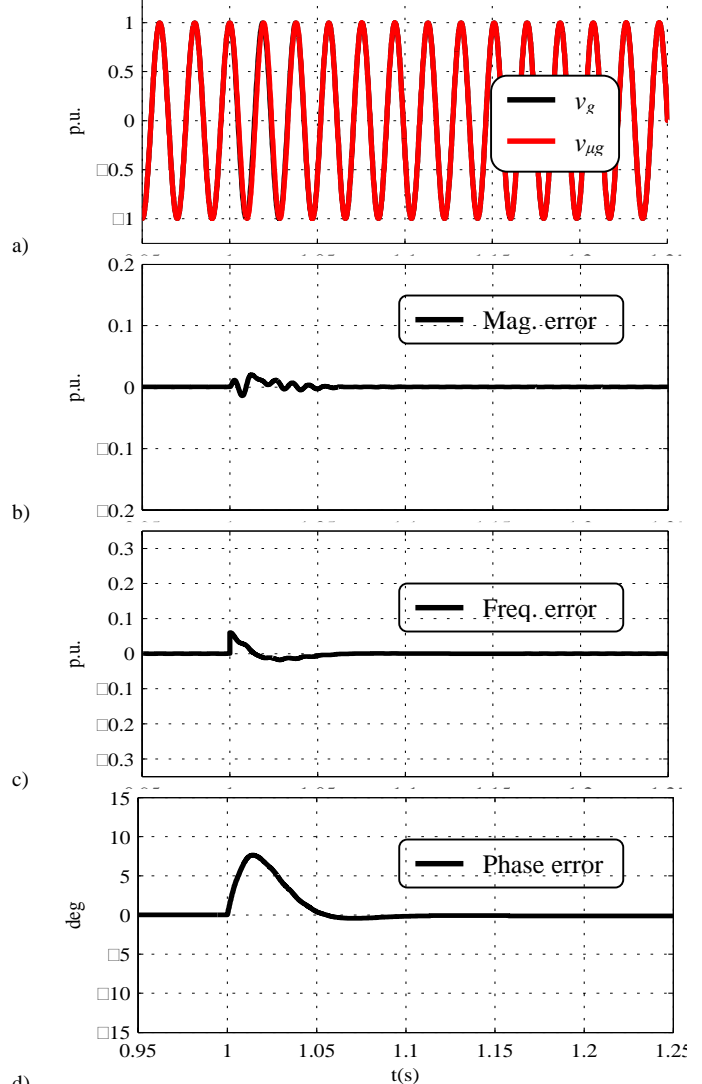
(≈ 2.1 deg. at 50Hz and ≈ 2 deg. at 53 Hz), the nearer the notch frequency to the fundamental component, the bigger the phase delay that it produces.

Fig. 7a shows the actual and estimated grid voltages.. Small transient magnitude and frequency errors (≈ 0.02 p.u. in Fig. 7b, ≈ 0.06 p.u. in Fig. 7c respectively) are observed when the frequency changes, which fade away in less than three cycles of the fundamental voltage. It is finally observed from Fig. 7d that a maximum phase error of ≈ 7.5 deg. is obtained, that is corrected after 60 ms.

Figs. 9 and 10 show the simulation results when 3rd, 5th and 7th harmonics are added to the grid voltage, all harmonics having a magnitude of 5% of the fundamental voltage (Table I). Fig. 8b shows the output of the proposed PFS. It is observed that the disturbance due to the injected harmonics is compensated in less than two cycles of the fundamental component.



b) Fig. 6- Simulation results showing the response of the QSG and PDC blocks to a step-like frequency change from 50 Hz to 53 Hz in $t=1$ s: a) input (v' , Fig. 2) and output (v'_q , Fig. 2) of the QSG, b) phase delays (D , Fig. 2) extracted by the PDC.



d) Fig. 7- Simulation results showing the response to a step-like frequency change from 50 Hz to 53 Hz in $t=1$ s: a) actual v_g and estimated $v_{\mu g}$ grid voltages, b) magnitude error, c) frequency error, d) phase error.

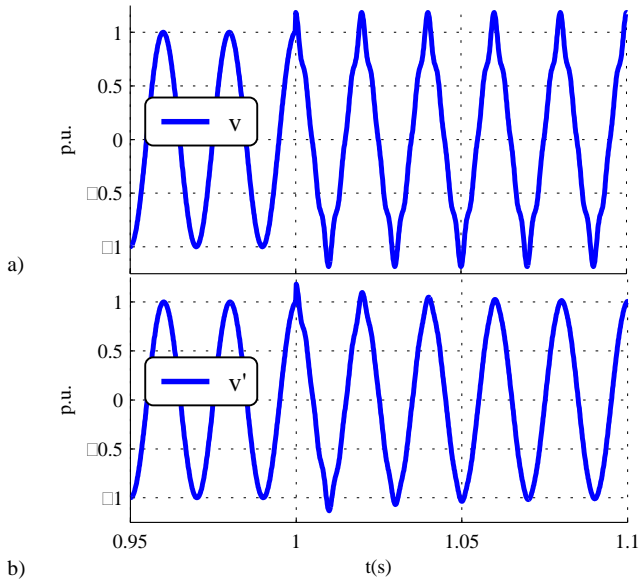


Fig. 8- Simulation results showing the behavior of the PFS when 3rd, 5th and 7th harmonics are added to the grid voltage at $t=1s$: a) input (v , Fig. 2) and b) output (v' , Fig. 2) of the PFS.

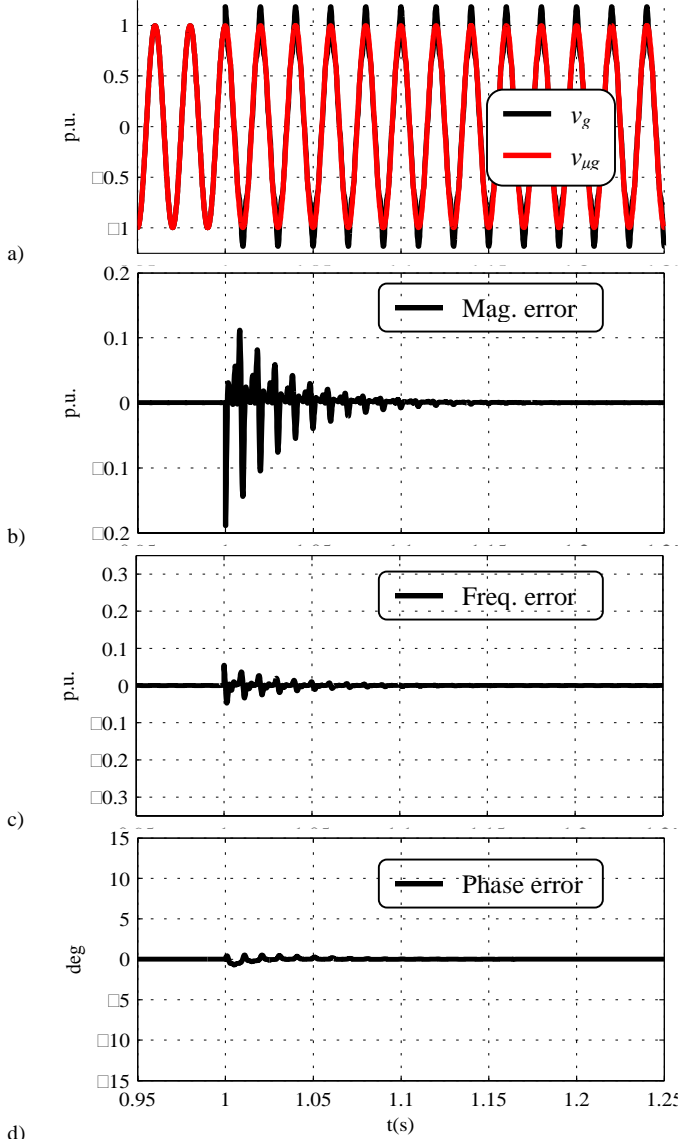


Fig. 9- Simulation results showing the response when 3rd, 5th and 7th harmonics are added to the grid voltage at $t=1s$: a) actual grid voltage v_g and estimated grid voltage $v_{\mu g}$, b) magnitude error, c) frequency error, d) phase error.

Fig. 9a shows the estimated grid voltage, the effects due to the harmonics injected by the AC source being totally eliminated. Fig. 9b shows the amplitude of the error between the fundamental component of the grid voltage v_g and the estimated voltage $v_{\mu g}$. The error is due to the transient response of the PFS used to remove the grid disturbances. It has a maximum value of 0.18 pu, and is removed by the PFS after 50 ms. A similar behavior is observed for the frequency error (Fig. 9c), the maximum frequency error being 0.05 pu. Finally, the maximum transient phase error is smaller than 1 deg. (see Fig. 9d), being completely removed after 50 ms.

IV. EXPERIMENTAL RESULTS

Fig. 10 and Table I show the experimental setup configuration and parameters. It consists of two single-phase voltage source converters (Master and Slave in Fig. 10). The master inverter is used to emulate a programmable AC source (see Fig. 4) meanwhile the slave inverter implements the proposed single-phase synchronization method. Both master and slave inverters are 50 kW inverters feeding each one a local resistive load of 30 Ω . The same tests used in simulation were performed experimentally.

Fig. 11 shows the experimental results when the grid voltage magnitude changes. The PCC voltages are shown in Fig. 11a, the magnitude, frequency and phase errors between the v_g and $v_{\mu g}$ being shown in Fig. 9b, 10c and 10d respectively.

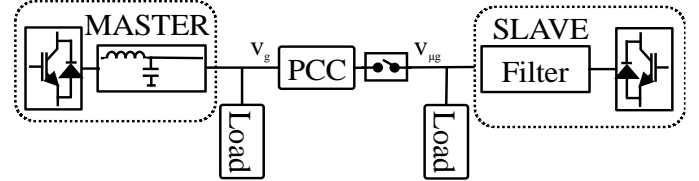


Fig. 10- Experimental setup.

It is observed in Fig. 11a that the proposed method shows an excellent performance tracking the magnitude change. The magnitude error (Fig. 11b) has a peak value of ≈ 0.08 pu, being compensated after ≈ 20 ms. Frequency (Fig. 11c) and phase (Fig. 11d) errors are negligible. The differences between simulation (Fig. 5) and experimental (Fig. 11) results are due to the fact that the inverter used to produce the disturbances in the experimental set up implements voltage and current control loops, what limits the bandwidth producing the disturbances.

Fig. 12 shows the experimental results when a frequency step-like change of the grid voltage occurs. Fig. 12a shows the actual and estimated voltage. A small peak magnitude error (i.e. $< \approx 0.01$ pu) is observed (Fig. 12b) at the instant the grid frequency changes, the peak grid frequency error being < 0.05 pu. Both errors are corrected after ≈ 10 ms by the PLL-ATO.

A negligible phase error is observed in Fig. 12d. Again the differences between the simulation and experimental results are due to the control bandwidth of the master inverter. It is noted in this regards that in a real scenario the grid frequency does not change instantly due to the inertia of the power generators.

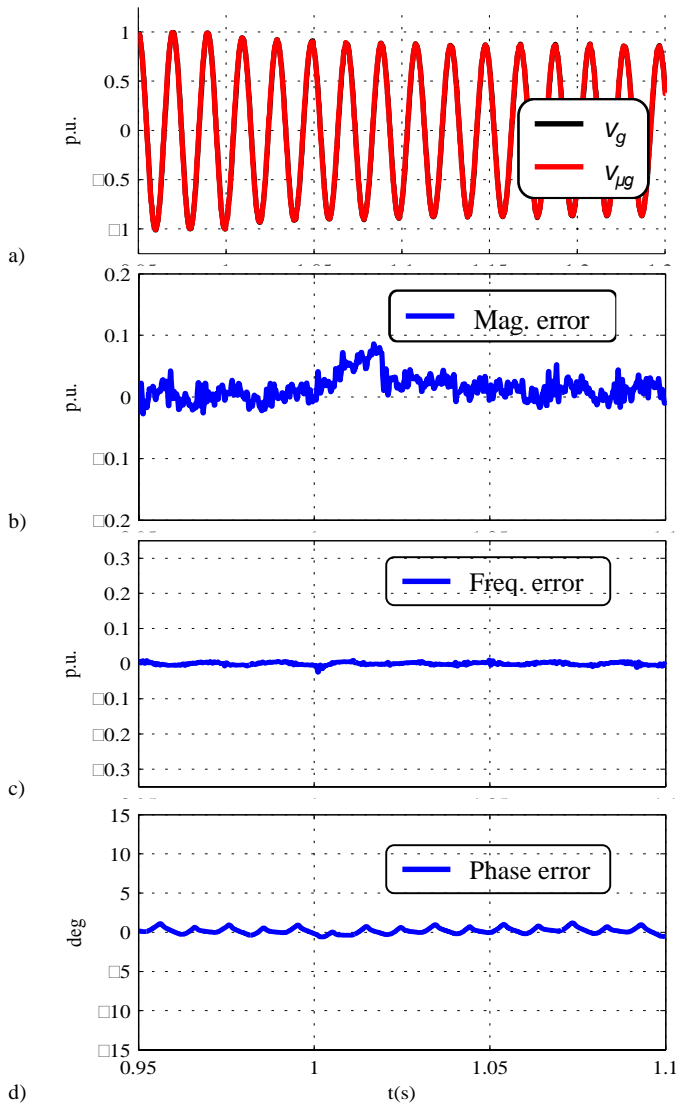


Fig. 11- Experimental results showing the response when the grid voltage magnitude v_g changes from 1 p.u. to 0.85 p.u at $t=1$ s.: a) actual grid voltage v_g and estimated grid voltage $v_{\mu g}$, b) magnitude error, c) frequency error, d) phase error.

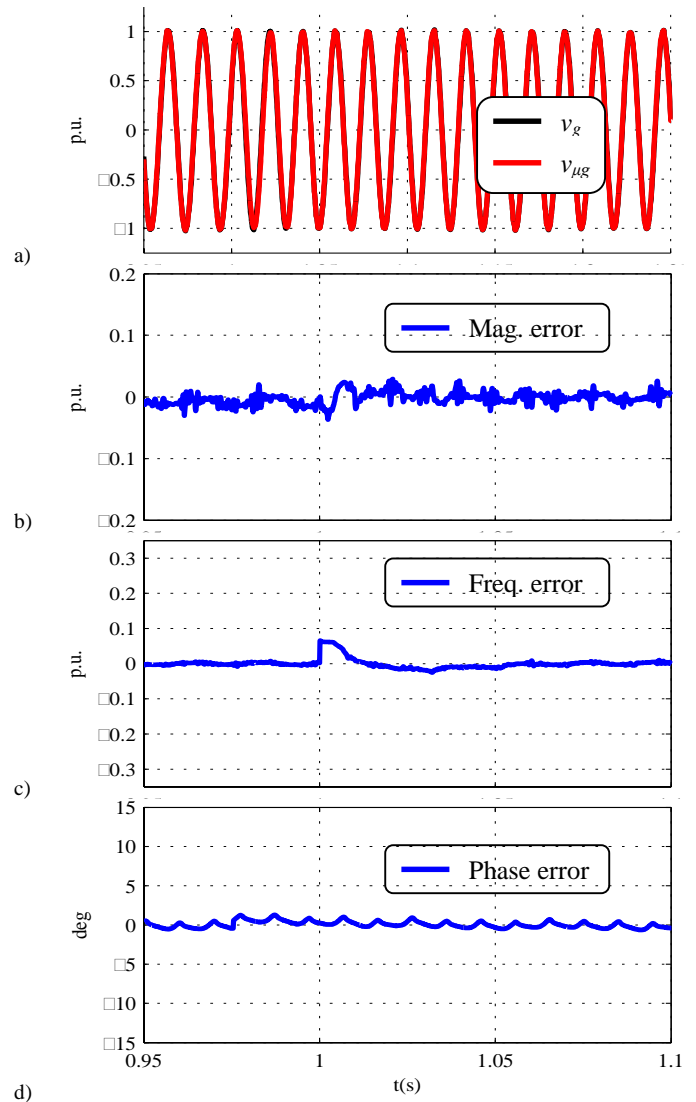


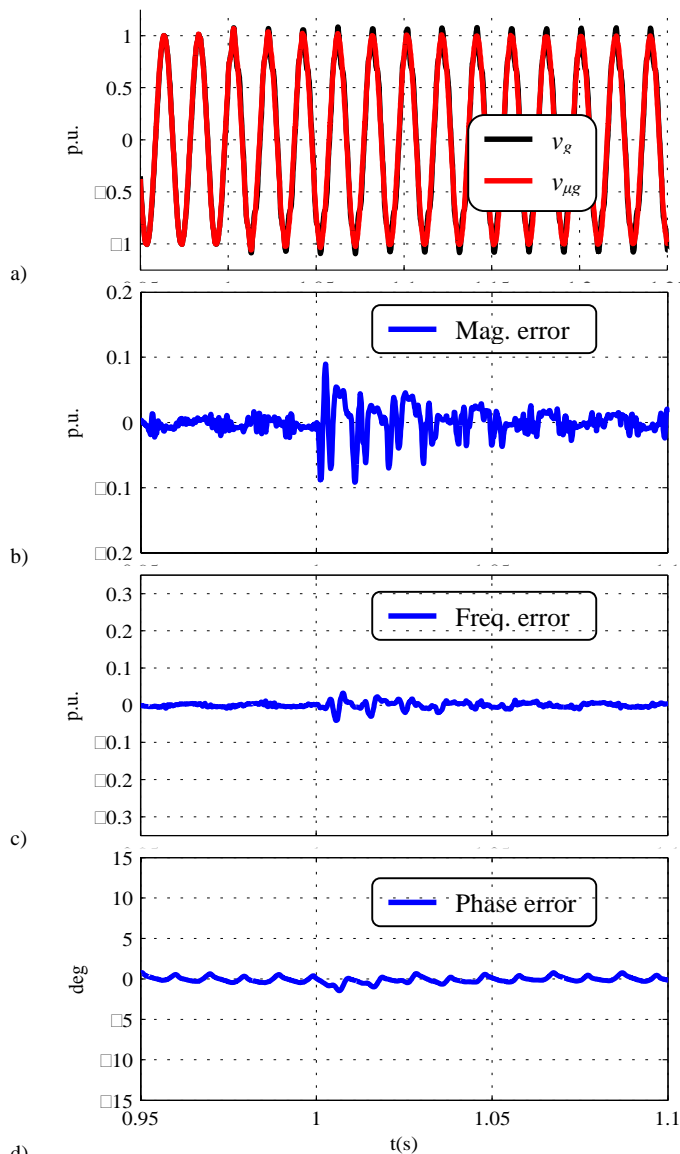
Fig. 12- Experimental results showing the response to a frequency step-like change of the grid voltage v_g from 50 Hz to 53 Hz at $t=1$ s: a) actual grid voltage v_g and estimated grid voltage $v_{\mu g}$, b) magnitude error, c) frequency error, d) phase error.

Finally, Fig. 13 shows the experimental results when 3rd, 5th and 7th harmonics are added to the grid, the magnitude for each harmonic being 0.05 pu. It is observed in Fig 14a that the proposed method cancels the effects due to the harmonics. Similar as for the simulation results (see Fig. 7b), both the magnitude error (Fig. 13b) and the frequency error (Fig. 13c) show an oscillating response produced by the PFS transient response, with a peak value <0.09 pu and <0.04 pu respectively, which fade away in ≈ 50 ms.

It is finally observed that the phase angle error is almost negligible due to the low-pass behavior of the integrator used to extract the grid phase. It can be concluded that there is a good agreement between simulation and experimental results.

V. CONCLUSIONS

A synchronization method for single-phase power converters is presented in this paper. The proposed method uses a pre-filter stage to eliminate the harmonic content of the grid voltage, a QSG to create a fictitious voltage complex vector, and a three-phase ATO to extract the frequency/phase of the fundamental voltage component. In addition, an online phase delay compensator is used to correct the delay due to the filtering stage. Simulations and experimental results showing the performance of the proposed method have been presented. It has been demonstrated that the proposed method shows a good transient response, negligible steady-state error and high harmonic rejection capabilities, fully accomplishing with international standards.



d) Fig. 13- Experimental results showing the response to 3rd, 5th and 7th harmonics injection at $t=1$ s: a) actual grid voltage v_g and estimated grid voltage $v_{\mu g}$, b) magnitude error, c) frequency error, d) phase error.

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