Increasing the Voltage and the Switching Frequency in a Dual Active Bridge Using a Normally-on SiC JFET in a Cascode Configuration

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***Abstract*— Silicon Carbide (SiC) transistors are becoming increasingly available in the market due to the fact that its manufacturing process is more mature. These new semiconductors have several advantages compared with traditional Silicon (Si) devices, such as, for example, higher voltage blocking capability, lower conduction voltage drop and faster transitions, which make them more suitable for high-power and high-frequency converters. The introduction of these new devices in switching power supply systems provides better performance enabling higher frequencies and consequently smaller, lighter and cheaper systems.**

Moreover, the increasing demand of an intermediate storage of electrical energy in battery systems has resulted in the need of bidirectional DC/DC power converters with galvanic isolation, for example due to the use of renewable energy or the incoming traction applications. A Dual Active Bridge (DAB) is a bidirectional DC/DC converter often used in these applications. This topology presents the advantages of soft-switching commutations, low cost, and high efficiency. Therefore, the use of this topology is proposed for applications where power density, cost, weight, and reliability are critical factors.

This paper is focused in the inclusion of commercially available SiC transistors in a DAB converter taking advantage of the characteristic of these devices, as their good switching performance and their high voltage blocking capability. The main goal is to increase the voltage of the input or output voltage in a DAB and also to increase the switching frequency at the same time.

I. INTRODUCTION

SiC devices are growing in relevance in the last few years as a result of their more mature technology and their subsequent appearance in the market. The advantages of these devices with respect to the Si counterpart can be summarized in higher electrical breakdown field (eight times bigger) and thermal conductivity (three times higher) [1]-[3]. These benefits derive in higher voltage blocking capability, faster switching transitions, lower on-state voltage drop and lower thermal resistance, which make SiC devices suitable for high-power and high-frequency converters.

SiC diodes have been commercially available for a long time, and they are commonly used in switching power electronic systems, especially as the output diode of AC/DC Power Factor Corrector (PFC) converters, due to their almost negligible reverse recovery losses [4]-[6]. However, the introduction of SiC transistors in the market is much more recent, and its introduction into power electronics application is not so widespread. Nowadays, there are different commercially available configurations of SiC transistors such as JFETs (normally-on and normally-off), BJTs and MOSFETs. In general, these SiC devices require new drivers (different from the drivers used for Si transistor) to properly turn on and off the device and even negative voltage must be generated [7]-[9]. Moreover, the use of normally-on devices could imply the inclusion of new protections in the converter topology during the start-up process. Nevertheless, with a cascode configuration [10]-[12], it is possible to switch a normally-on device, as a SiC JFET, into a normally-off one by means of adding a low-voltage Si MOSFET. In this case, the global switch can be controlled using a common driver for Si MOSFET (the controlled device is the low-voltage Si MOSFET) keeping the main advantages of the SiC device. The inclusion of the low-voltage Si MOSFET in series with the SiC JFET slightly increases the on-resistance of the global switch, but the change is almost insignificant.

The aim of this paper is to validate the introduction of SiC normally-on JFET, in a cascode configuration, in a DC/DC converter and to verify their good performance at high frequency and high voltage. First, a comparison between a DAB converter using Si MOSFET and a DAB with SiC JFETs in a cascode configuration will be presented.

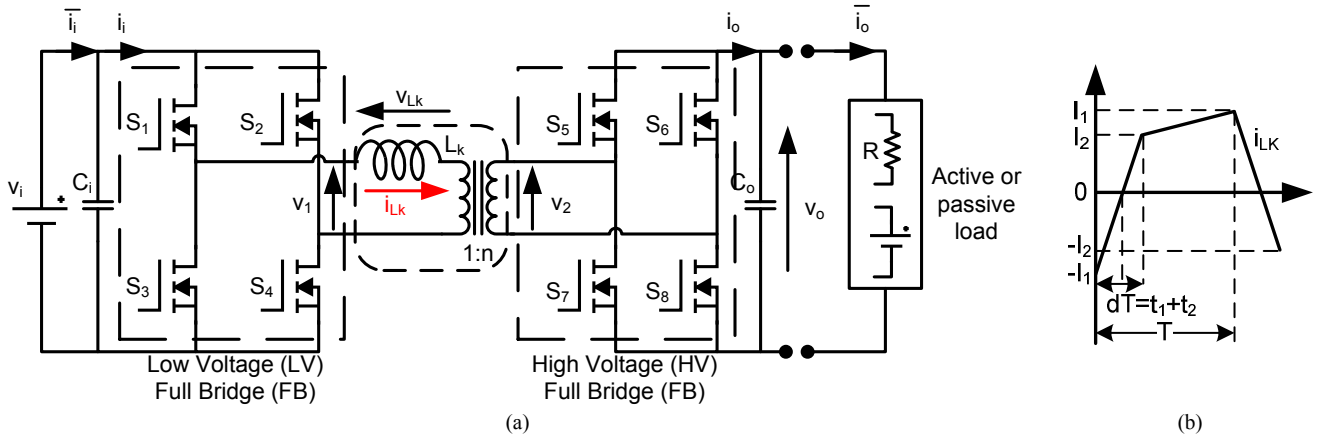


Figure 1. (a) Schematic of the DAB converter. (b) Waveform of the leakage inductance current showhing some interesting values

The inclusion of these SiC devices allows a theoretically increase of the switching frequency and the voltage without a dramatically decrease of the efficiency. For this reason, using the DAB with the SiC devices new tests have been carried out with different specifications (increasing the voltage of the High Voltage (HV) side and increasing the switching frequency). The specifications of a DAB converter are summarized in section II. The use of a SiC JFET cascode configuration in this converter is explained in section III. The experimental results are shown in section IV. Finally, section V ends the paper with some conclusions.

II. Specifications of the DAB converter using silicon transistors

The DAB converter (Figure 1), originally proposed in [13] and [14] and analyzed in more detail in [15]-[18], is a bidirectional DC/DC converter based on two active bridges interfaced through a high-frequency transformer (with a great influence of its leakage inductance), enabling power flow in both directions in case of active load.

The easiest way to control this topology is switching each full bridge with a constant duty cycle of 50% to generate a high-frequency square-wave voltage at its transformer terminals ($\pm v_i$, $\pm v_o$). Considering the presence of the leakage inductance of the transformer (with a controlled and known value), the two square waves can be appropriately phase shifted. These two phase shifted signals (v_1 and v_2) generate a voltage (v_{Lk}) in the leakage inductance (L_k) of the transformer and a certain current (i_{Lk}) flows through it. This current is controlled by the phase-shift between the primary and secondary voltages of the transformer (v_1 and v_2). The sign of the phase-shift controls the power flow from one dc-source to the other, and bidirectional power transfer can be achieved. Power is delivered from the bridge which generates the leading square wave. The main operation waveforms are shown in Figure 2.

The use of a transformer that introduces galvanic isolation also provides the possibility of a high conversion ratio. Generally two quite different full bridges are required. On the one side, a low-voltage (LV) full bridge, where the main problem usually is the high current and special care must be taken about the conduction losses. On the other side, a HV full bridge, where the switching losses are mainly the most important concern. One of the greatest advantages of the DAB is the soft-switching of all the devices at nominal conditions. However, when the power handled by the DAB is reduced, Zero Voltage Switching (ZVS) can be lost, especially in the HV full bridge. The lost of ZVS generates, not only a high decrease in the efficiency, but also on some occasions a lot of noise that can cause problems in the driver circuits connected to the gate of the transistors. For these reasons, maintaining ZVS in a big range of power is an interesting design goal.

In the operation waveforms in Figure 2, the input voltage is the same as the output voltage reflected in the primary,

$$M = \frac{v_o}{v_i \cdot n} = 1 \quad (1)$$

In this operation conditions, ZVS will be theoretically obtained for all the power range. However, this condition is not always fulfilled. The theoretic ZVS limits for each full bridge when M is not equal to 1 are [18]:

$$I_1 > 0 \rightarrow d > \frac{M-1}{2M}, \text{ for M>1. Primary ZVS} \quad (2)$$

$$I_2 > 0 \rightarrow d > \frac{1-M}{2}, \text{ for M<1. Secondary ZVS} \quad (3)$$

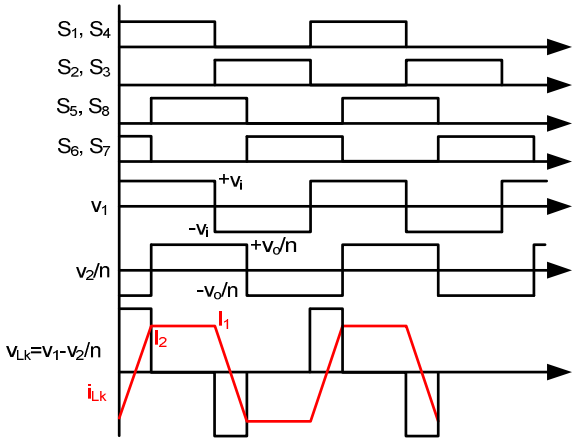


Figure 2. Theoretical waveforms of the DAB

Moreover, the influence of parasitic components can modify the limits to obtain ZVS. Actually, to maintain ZVS, the energy stored in the leakage inductance when the transistors of the full bridge switch, must be enough to charge and discharge its parasitic output capacitances. Equation (4) must be fulfilled, where *v* is the voltage applied to the bridge and C_{eq} is the equivalent value of the parasitic output capacitance of the transistors that compose the bridge when the voltage changes from 0 to *v* V.

$$\frac{1}{2}L_k {i_{Lk}}^2 \geq 4 \cdot \frac{1}{2}C_{eq}v^2. \quad (4)$$

The current through the leakage inductance when the LV full bridge and the HV full bridge are switching are called I_1 and I_2 respectively (Figure 1 and Figure 2).

$$I_1 = \frac{T}{2L_k}\left(2\frac{v_o}{n}d + v_i - \frac{v_o}{n}\right) > 2v_i\sqrt{\frac{C_{eq\_i}}{L_k}}. \quad (5)$$

$$I_2 = \frac{T}{2L_k}\left(2v_i d - v_i + \frac{v_o}{n}\right) > 2v_o\sqrt{\frac{C_{eq\_o}}{L_k}}. \quad (6)$$

Solving equation (5) and (6) more realistic ZVS limits for each bridge are obtain:

$$d > \frac{M-1}{2M} + \frac{2\sqrt{L_k C_{eq\_i}}}{TM}, \text{ for M>1. Primary ZVS.} \quad (7)$$

$$d > \frac{1-M}{2} + \frac{2Mn\sqrt{L_k C_{eq\_o}}}{T}, \text{ for M<1. Secondary ZVS} \quad (8)$$

The stored energy in the leakage inductance is mainly determined by the specifications and the design of the converter. However, the stored energy in the parasitic capacitances of the full bridge depends on the applied voltage and the value of these capacitances. The latter value is highly related with the technology of the selected transistors. In Si MOSFET, the value of C_{eq} is increased for higher voltage blocking capability. The increase is even sharper when the V_{ds_max} is higher than 600 V. When MOSFETs of V_{ds_max} >600 V have to be used, the increase of C_{oss} and R_{dson} (TABLE I) worsen the performance of the DAB. This is an important drawback when HV full bridges are required in a DAB. For voltages higher than approximately 400V, transistors of V_{ds_max}>600V are required (taking into account security margins), and a less performing DAB will be developed if Si MOSFETs are used.

It is important to remark that high voltage buses (for example, 600 V or 800 V) are widely required for electrical traction applications and for motor drives. For this reason, an increase of the voltage applied to the HV full bridge of a DAB could be very interesting regarding this kind of applications in terms of reliability and efficiency. A traditional solution, when HV buses are used, is to design the HV full bridge using IGBTs. However, the use of IGBTs implies an important decrease in the switching frequency in comparison to the use of Si MOSFET and consequently an increase in weight, size and cost of the magnetic components. Another solution that allows high voltage and high frequency is the use of SiC transistors to design the HV full bridge.

TABLE I. CHARACTERISTICS OF SOME OF THE MOST PERFORMING HV SI MOSFET

	V_{ds_max} (V)	R_{dson_max} (mΩ)	I_{d_max} (A)	C_{oss} (pF) @ V_{ds}=100 V, f_{sw}=1 MHz
IPW60R125CP	650	125	25	120
IPX60R125C6	600	125	30	125
SPW55N80C3	800	85	55	305
IPW90R120C3	900	120	36	330

A DAB using silicon MOSFETs has been developed to validate the previously detailed concepts about ZVS limits. The efficiency of this prototype will be also compared with a DAB developed using SiC JFETs in the HV full bridge. The most important specifications of the developed DAB to make the comparison will be presented in the experimental results section.

III. INTRODUCING SIC TRANSISTORS IN THE DAB

As it has been previously detailed there is a certain limit in the maximum voltage withstood by the HV full bridge when Si MOSFETs are used. However, using SiC transistors, thanks to their higher breakdown electric field, the voltage of the HV full bridge can be increased without an important decrease in the performance of the DAB. Most of the commercially available SiC transistors can withstand a V_{ds_max}=1200 V (even few commercial devices can withstand a V_{ds_max}=1700 V).

Moreover, using SiC devices, thanks to their lower parasitic capacitances and their better switching behavior, the switching frequency of the DAB can be increased, allowing the use of smaller magnetic components.

Nowadays, only a few SiC transistors can be purchased and all of them require the use of specific drivers. Some new drivers have been proposed to control these new SiC transistors [19], but they are not as common as the driver used for silicon MOSFET and they are more expensive. However, a cascode configuration, composed by a SiC normally-on JFET and a LV Si MOSFET (Figure 3), has been tested in a simpler converter (i.e. boost converter) and provides a good switching behavior, specially when ZVS is achieved. Additionally, a standard Si-MOSFET driver can be used because the controlled device is the LV Si MOSFET, whilst the SiC JFET will withstand most of the voltage.

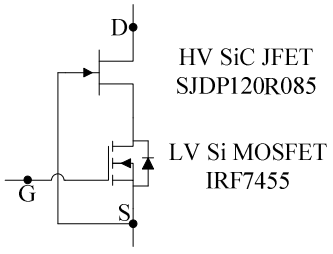


Figure 3. Cascode configuration composed by a LV Si MOSFET and a HV SiC normally-on JFET

The transistors that compose the two full bridges of a DAB operate with ZVS in the turn-on in nominal conditions. For this reason, the use of a cascode configuration is considered appropriate to develop the HV full bridge of a DAB. The operation without ZVS would increase the losses of the cascode in comparison with the use of a single SiC JFET but this kind of operation will be avoided for the HV full bridge due to the high increase of the switching losses. To increase the operation range of the DAB with ZVS, the DAB will be designed with the maximum value of leakage inductance that provides the maximum power using the maximum phase-shift [18].

The main characteristic of the SiC JFET (SJDP120R085 from SemiSouth) and the LV silicon MOSFET used in the cascode are shown in TABLE II. As can be seen, the output capacitance of the HV SiC JFET is lower than the one of all the HV Si MOSFET presented in TABLE I, even when its V_{ds_max} is higher. A new converter has been developed, but in this case replacing the Si MOSFETs of the HV full bridge with the proposed SiC cascode. The specifications of the DAB are presented in TABLE III and the efficiency results will be presented in the experimental results section.

Due to the fact that the LV full bridge presents a good switching performance (because low-voltage Si MOSFETs are used) and thanks to the use of the SiC cascode to develop the HV bridge, an important increase in the switching frequency of the DAB can be performed. Furthermore, the use of the SiC cascode will allow the increase of the output voltage of the DAB. To verify the good performance of the SiC cascode at both higher switching frequency and higher output voltage, a new DAB prototype will be developed with the specifications presented in TABLE IV. Also some tests with different switching frequencies have been carried out. All the experimental results will be presented in the following section.

IV. Experimental Results

To compare the performance of the SiC JFET tested in a cascode configuration with some of the most performing HV Si MOSFETs, efficiency results has been obtained using the previously detailed DAB converter (TABLE III). Although the magnetic components are not optimized, a high efficiency has been obtained using Si MOSFETs. In order to compare Si and SiC devices, a DAB with the HV bridge composed by the SiC cascode has been developed.

TABLE II. CHARACTERISTICS OF THE DEVICES USED IN THE CASCODE

	Si MOSFET (IRF7455)		N-on SiC JFET (SJDP120R085)	
Fabricante	International Rectifier		SemiSouth	
$V_{DS\ max}$ (V)	30		1200	
$I_{D\ max}$ (A)	15		27	
$R_{DSon\ max}$ (mΩ)	7.5		85	
$V_{GS\ max}/V_{GS\ th}$ (V)	+12, -12 / 2		+15, -15 / -5	
C_{iss} (pF)	3480	@	255	@
C_{oss} (pF)	870	V_{DS}=25 V	80	V_{DS}=100 V
C_{rss} (pF)	100	f=1 MHz	80	f=1 MHz

TABLE III. SPECIFICATIONS OF THE DAB TO COMPARE SI AND SIC

Input / Output voltage:	48 V / 400V
Output power:	1 kW
Switching frequency:	100 kHz
LV Si full bridge MOSFETs:	IRFB4310Z
HV Si full bridge MOSFETs:	IPW60R280C6
HV SiC full bridge Cascode:	SJDP120R085+IRF7455
Transformer:	1:8
Leakage inductance:	L_k = 2.6 µH

To perform a fair comparison, only the transistors of the HV full bridge has been changed, substituting the Si MOSFETs for the SiC cascode. All the rest of the components, even the drivers used for the Si DAB have been kept (thanks to the used of the cascode configuration). In Figure 4 the most important waveforms in the SiC DAB are shown. Efficiency results are presented in Figure 5. As can be seen, the efficiency obtained with the SiC HV full bridge is higher for almost all the measured power range. At high power, the efficiency is very similar because the most significant losses are the conduction and core losses of the magnetic components, which are the same in both cases. It is important to remark that, although the comparison is fair because the same specifications and components have been used, these specifications do not take advantage of the properties of the SiC JFET. In order to test these properties, the output voltage and the frequency will be increased.

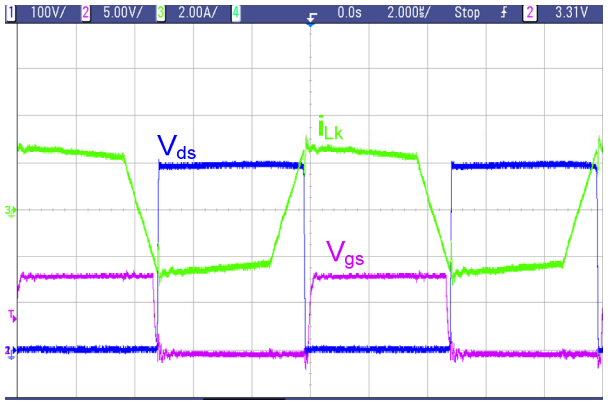


Figure 4. Main waveforms of the DAB Main waveforms of the DAB

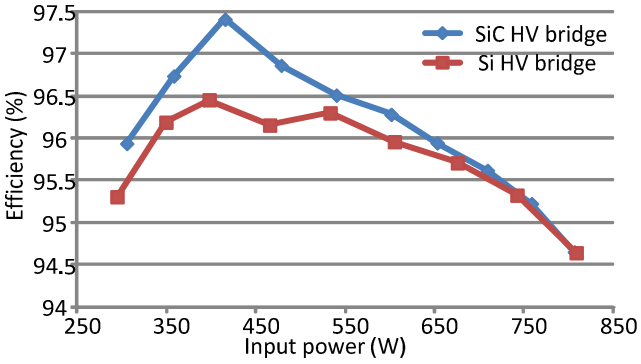


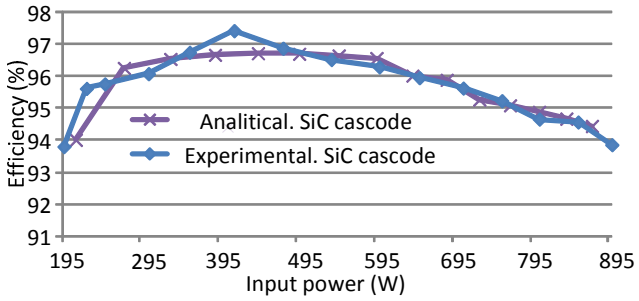
Figure 5. Efficiency comparison of a DAB using Si and SiC transistor

The analytical estimation of the losses in a DAB has been widely reported, for example in [15]. Not many details will be given in this paper, because is not its purpose, but some efficiency graphs comparing the analytical with the experimental results are presented in Figure 6(a) and (b). The analytical results are compared with the experimental results presented in Figure 5 to show how the improvement obtained thanks to the use of SiC devices can be analytically estimated.

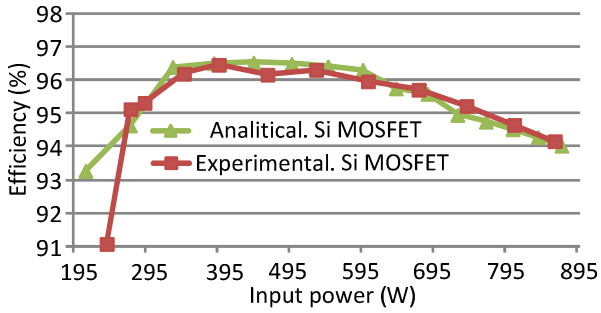
Another DAB with different specifications have been developed to take advantage of the benefits of SiC transistors. New magnetic components (transformer and leakage inductance) have been designed to operate at higher frequency and higher output voltage. The main specifications of the new prototype are presented in TABLE IV.

As has been detailed in [18] and can be seen in equation (9), the use of a higher switching frequency implies the use of a lower value of leakage inductance to manage the maximum value of the power with the maximum phase-shift.

$$P = \frac{(1-d)dTv_i v_o}{nL_k} \rightarrow L_k = \frac{(1-d_{max})d_{max}Tv_i v_o}{nP_{max}} \quad (9)$$



(a)



(b)

Figure 6. Analitical and experimental efficiency results of the DAB with (a) SiC cascode and (b) Si MOSFET in the HV full bridge

TABLE IV. SPECIFICATIONS OF THE DAB WITH SIC

Input / Output voltage:	48 V / 600 V
Output power:	1 kW
Switching frequency:	200 kHz
LV Si full bridge MOSFETs:	IRFB4310Z
HV SiC full bridge Cascode:	SJDP120R085+IRF7455
Transformer:	1:12
Leakage inductance:	L_k = 1.27 µH

In Figure 7(a) the most important waveforms for the DAB with the HV full bridge composed by the SiC cascode operating at a switching frequency of 200 kHz and an output voltage of 600V are shown. Efficiency results for two different frequencies (f_{sw}=166 kHz and f_{sw}=200 kHz) are presented in Figure 7(b). As can be seen, both waveforms and efficiency results show the good performance of the SiC cascode in the HV full bridge of the DAB. The switching losses in a DAB operating with ZVS are very low, but they are not zero. When the switching frequency is increased the efficiency is a bit lower, but in this case, as can be seen in Figure 7(b), the reduction in the efficiency is not very high.

Due to the use of a lower value of the leakage inductance the ZVS operation range can be reduced. The DAB can work without ZVS for higher values of phase-shift and consequently higher values of power. Using (8), the limit of the phase-shift to operate with ZVS can be estimated. For example, for the specifications of the DAB with the HV full bridge composed by SiC cascodes, the analytical values of the power for which ZVS is lost, for two different frequencies and leakage inductances are:

$P_{ZVS} \approx 510\ W$, for f_{sw}=200 kHz and L_k = 1.27 µH (10)

$P_{ZVS} \approx 470\ W$, for f_{sw}=166 kHz and L_k = 1.5 µH (11)

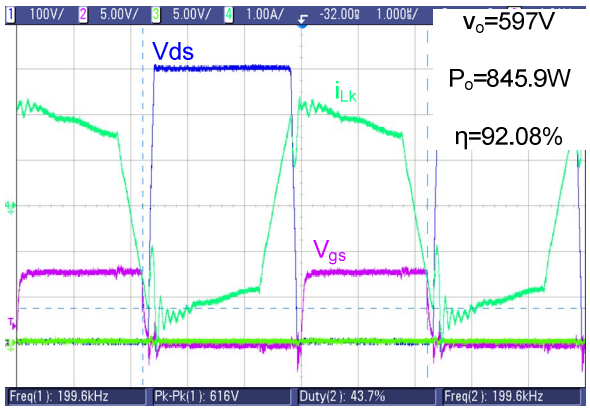
As can be seen in Figure 7(a), these values are a good approximation. However, it is difficult to obtain an exact value of the power because these values depend mostly on the output parasitic capacitance of the transistors that compose the HV full bridge.

Depending on the application, the operation without ZVS in such a narrow range of output power can be acceptable or not (operation without ZVS for high powers can generate problems). However, in applications where the volume is not a big deal, the switching frequency can be reduced, and a wide range of operation with ZVS and a higher efficiency can be achieved with a higher value of leakage inductance.

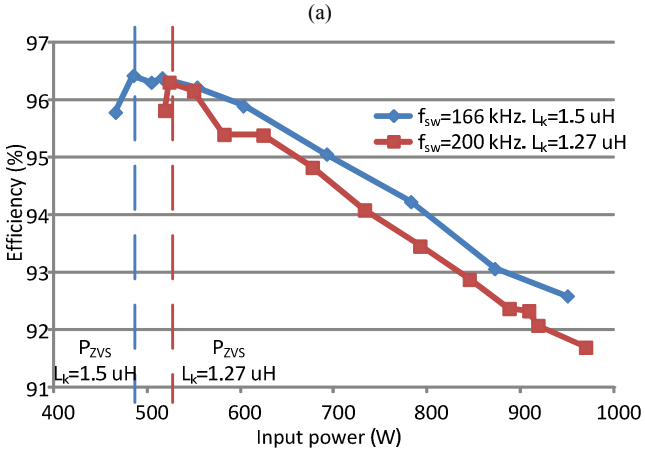
Some efficiency results have been obtained using the specifications presented in TABLE IV but with a different leakage inductance, in this case L_k=2.5 µH, and with a lower switching frequency, in this case f_{sw}=100 kHz. The efficiency results are presented in Figure 8. Obviously the use of a lower switching frequency reduces the switching losses and the use of a higher value of the leakage inductance increases the range of operation with ZVS (using equation (8) with these new specifications the obtained value is P_{ZVS}≈370 W).

In all the efficiency curves shown in this paper, in the range with ZVS operation, the efficiency decreases when the power increases. This effect is due to the need of a higher value of phase-shift to manage higher values of power. The use of a higher phase-shift implies higher values of reactive current processed by the converter [18]. To reduce the value of the phase-shift required to manage high power, a lower value of switching frequency can be used, maintaining the value of the leakage inductance. Obviously, depending on the application, the efficiency for the maximum power can

be more important and changing the switching frequency can be easy or not. However, it is important to consider these techniques to improve the efficiency of the DAB. In Figure 8 the efficiency results for a switching frequency of 100 kHz and 50 kHz are presented using the DAB with the HV full bridge composed by the SiC cascode, validating the good performance of these switches for different frequencies.



(a)



(b)

Figure 7. DAB using SiC cascode in the HV full bridge. (a) Waveforms. (b) Efficiency results for two different frequencies and leakage inductances

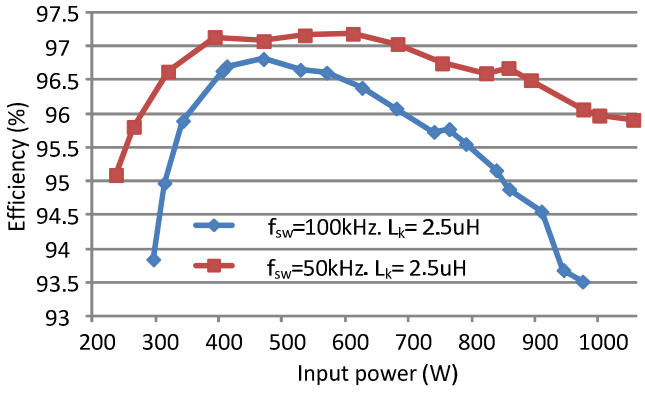


Figure 8. Efficiency results for different frequencies. The efficiency at high power can be increased reducing the frequency keeping the same leakage inductance.

V. Conclusions

In this paper the design and operation of a DAB converter has been roughly presented. When the input or the output voltages used by the DAB are higher than 600 V some restrictions in the use of Si MOSFETs, to develop the full bridges that compose the DAB, are presented. The main restrictions are caused by the worse characteristics of the few commercially available HV Si MOSFETs (with V_{ds_max} higher than 600 V). The use of IGBTs to increase the withstand voltage implies a decrease in the switching frequency and consequently an important increase in the size of the magnetic components. The solution presented in this paper is to replace the HV Si MOSFET by a SiC JFET in a cascode configuration. The use of the SiC JFET allows a higher voltage because its V_{ds_max} is 1200 V, and also an increase in the switching frequency thanks to its low parasitic capacitances. The cascode configuration allows the use of common Si drivers to switch the global cascode (composed by a LV Si MOSFET and a HV SiC normally-on JFET). A better efficiency using the SiC DAB, in comparison with the Si one has been obtained in a DAB prototype with an output voltage of 400 V and a switching frequency of 100 kHz.

Moreover, to take advantage of some of the well-known characteristics of the SiC power devices, as faster transitions and higher blocking voltage capability, a new DAB converter has been developed obtaining a higher voltage (600 V) from the voltage of a common battery (48 V). A higher switching frequency (200 kHz) has been selected thanks to the use of the SiC cascode. New magnetic components have been also developed to fulfil the new specifications. Moreover, a control that can easily change the switching frequency for different loads has been developed and an interesting increase in the ZVS range and in the efficiency at high power has been achieved. Different experimental results of the DAB with the HV full bridge composed by SiC cascode are presented to corroborate the good performance of this SiC transistor.

Acknowledgment

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