Islanding detection in grid-connected power converters using harmonics due to the non-ideal behavior of the inverter

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Abstract: This paper analyzes the use of the voltage distortions in PWM voltage-source-inverters (VSIs) caused by the non-ideal behavior of the inverter for islanding detection purposes. The non-ideal characteristic of the inverters, mainly due to the dead-time needed to have safe commutations, produces fundamental frequency dependent harmonics (-5th, 7th…) in the output voltage. Although these harmonics are in principle an unwanted effect, since they reduce the power quality, they can potentially be used for islanding detection purposes. The physical principles of the method would be the same as for high frequency signal injection methods that have already been proposed but without the need of injecting a high frequency signal.[1]

Index Terms— Active islanding detection, grid impedance measurement, dead-time, power system monitoring, distributed generation.

I. Introduction

The increased expansion of the distributed generation, moving form the classical centralized generation scenario to a high penetration scenario, has increased the grid connection requirements in terms of power generation, power quality and coordination with the electrical network. The distributed generation can use both renewable (wind turbines, photovoltaic,…) and non-renewable (fuel cells, micro gas turbines, biomass,…) resources. A very extended and suitable way to insert the distributed energy resources into the electrical network is through the use of the microgrids [1]. Microgrids could be understood as small-scale versions of the classical, large centralized electric distribution system, having the ability to operate connected or isolated from the utility grid, without affecting to the microgrid's loads (ideally).

The interconnection of microgrids and/or distributed energy resources to the utility grid is regulated by local, regional and national authorities, while standardizing institutions (e. g. IEEE or IEC) publishes standards and recommendations for interconnecting distributed resources with the electric power systems [2-9]. In all cases, the system is required to have the ability to detect if it is connected or disconnected to the utility grid, which is normally referred as islanding detection [10-18]. As an example, the IEEE-1547 [2], UL-1741 [3], IEC-62116 [4], AS-4777 [5] and IEEE-929 [6], requires islanding detection within 2 seconds after the islanding situation occurs. The German (DIN-VDE-0126) [7], Swiss [8] and Australian [9] standards established the grid impedance variation within a period of time as the islanding detection methodology; 1 Ohm in 2 seconds for the German standard and 0.5 Ohms in 5 seconds for the Swiss and Australian standards**.**

Islanding detection methods can be classified into three major groups: passive [10, 11], active [10-18] and communication-based [10] methods. Passive and communication-based methods are grid friendly, as they don't produce any disturbance in the grid. Passive methods usually present large non-detection-zone (NDZ), although are cheap and easy to implement [10, 12]. Communication-based methods need a communication infrastructure, having no NDZ in theory [12]. Active methods are based on the injection of some form of disturbing signal in the grid, having therefore a negative impact on the power quality; the islanding condition being detected by the system response to such signal [10-13]. However active methods are easy and cheap to implement and have low NDZ [10-13].

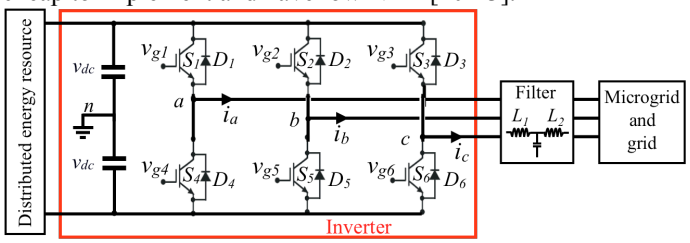

Fig. 1.- Simplified distributed energy resource connection to the utility grid/microgrid using a VSI.

Distributed energy resources are usually connected to the main grid/microgrid by means of a three-phase PWM-VSI [12-13] (see Fig. 1). VSIs produce a distortion of the output voltage with respect to the commanded voltage, mainly due to the blanking time (dead-time) needed for safe commutation within each inverter leg [19-24]. Though other effects due to the non-ideal behavior of the switches (turn-on/turn-off time and voltage drop on the diodes and power switches,…) also influence, they are less important. The distortion due to the inverter dead-time is known to be a function of the inverter current sign [22, 23], -5th, 7th… harmonics of the fundamental frequency being typically produced due to this effect [19, 21].

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The distortion of the output voltage produces an increase in the THD of the voltages/currents, having therefore an adverse impact on the power quality [20, 22]. However, the induced harmonics can also be used as a form of high frequency excitation for active islanding detection purposes.

In this paper, islanding detection using the higher order components of the inverter output voltage due to the non-ideal behavior of the inverter is proposed. By using this harmonics, the injection of additional high frequency signals is avoided, which is beneficial in terms of power quality.

The paper is organized as follows: the analysis of the effects due to the dead-time in PWM inverters is presented in section II; the principles of the proposed islanding detection method are presented in section III, while simulation and experimental results to confirm the viability of the proposed method are finally provided in sections IV, V and VI.

II. Dead-time effects in PWM inverters.

Fig. 1 schematically shows a three-phase PWM-VSI used to connect distributed energy resources to the three-phase utility grid/microgrid. Fig. 2 shows the gate signals for one leg without (subplots a) to c)) and with (subplots d) to g)) considering the dead-time in the gate signals. Fig. 2a and b show the ideal gate signals for switches 1 and 4, while Fig. 2c shows the ideal output voltage, i.e. with no voltage drop across the switches and on-off transitions of the upper and lower switches occurring simultaneously. In practice, due to the non-zero turn-on and turn-off times, a dead-time has to be inserted in every commutation to guarantee that the two switches in a branch (e.g. S1 and S4) do not conduct simultaneously. Fig. 2d and e show the real gate signals, after inserting the dead-time, when switches S1 and S4 are turned-on and off respectively. When both transistors are turned-off, one of the freewheeling diodes will conduct, depending on the sign of the output current. If the current is positive (see Fig. 1), D4 will be conducting (see Fig. 2f), while D1 will conduct if the current is negative (see Fig. 2g). In addition, it is observed from Fig. 2f and g that the voltage drop across the switches and diodes and the turn-on/off times are considered.

The average voltage errors caused by the non-ideal behavior of the inverter (turn-on, turn-off, voltage drops and dead-time) during each switching period can be calculated using (1) and (2) for the case of the current being positive and negative respectively (see Fig. 2f and g).

$$\begin{aligned}\Delta V &= \frac{T_d + t_{on}}{2T_s}\left(-V_{dc} - V_d\right) + \frac{t_{off}}{2T_s}\left(V_{dc} - V_{sat}\right) \\ &= \frac{-T_d - t_{on} + t_{off}}{2T_s}V_{dc} + \frac{-T_d - t_{on}}{2T_s}V_d + \frac{-t_{off}}{2T_s}V_{sat}\end{aligned} \quad (1)$$

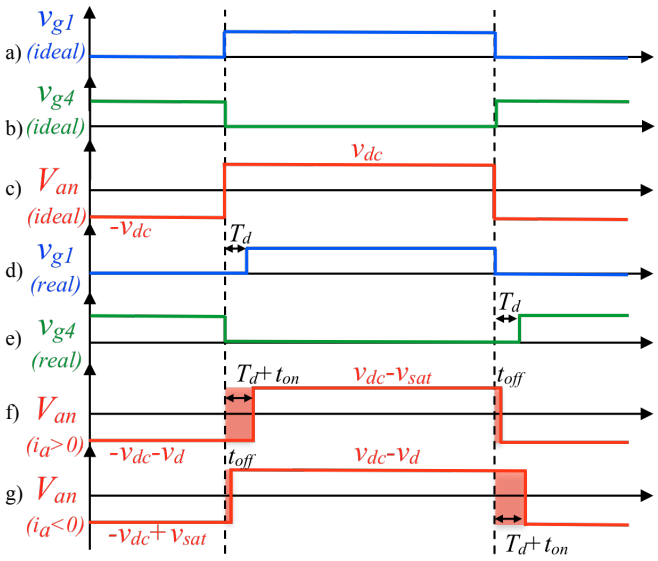

Fig. 2.- a) to c): gate signals for switches S1, a), and S4, c), and output voltage when no dead time is considered. d) to g): gate signals for switches S1, d), and S4, e), when the dead-time is inserted. Output voltage when the output current is positive, f) and negative g).

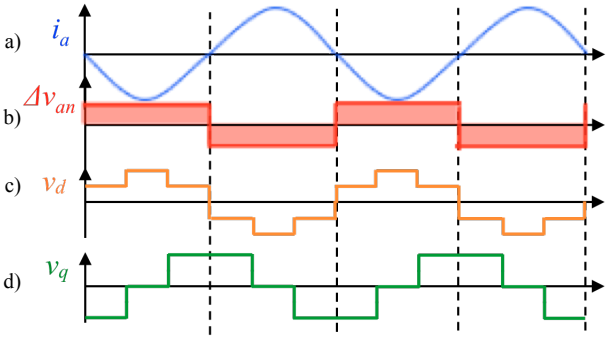

Fig. 3.- Phase current, a), average voltage error, b), *d* and *q* components of the average voltage complex vector, c) and d).

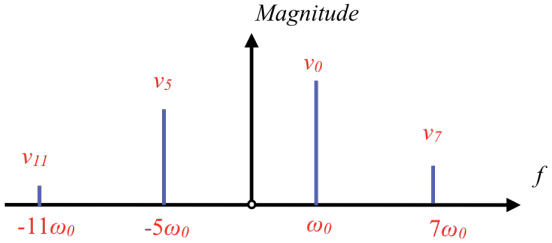

Fig. 4.- Complex vector spectrum of the voltage error.

$$\begin{aligned}\Delta V &= \frac{T_d + t_{on}}{2T_s}\left(V_{dc} + V_d\right) + \frac{t_{off}}{2T_s}\left(-V_{dc} + V_{sat}\right) \\ &= \frac{T_d + t_{on} - t_{off}}{2T_s}V_{dc} + \frac{T_d + t_{on}}{2T_s}V_d + \frac{t_{off}}{2T_s}V_{sat}\end{aligned} \quad (2)$$

where T_d is the dead-time, t_{on} is the turn-on time of the power switch, t_{off} is the turn-off time of the power switch, T_s is the sampling period, V_{dc} is the dc bus voltage, V_d is

forward voltage drop of the diode and V_{sat} is the on-state voltage drop across the power switch.

Assumed that $V_d \approx V_{sat}$, (1) and (2) can be safely simplified to (3) and (4) [22].

$$\Delta V = \frac{-T_d - t_{on} + t_{off}}{2T_s} V_{dc} - \frac{T_d + t_{on} + t_{off}}{2T_s} V_{sat} \quad (3)$$

$$\Delta V = \frac{T_d + t_{on} - t_{off}}{2T_s} V_{dc} + \frac{T_d + t_{on} + t_{off}}{2T_s} V_{sat} \quad (4)$$

Fig. 3b shows the voltage error for phase *a* averaged for each switching cycle, which is seen to depend on the sign of the output current (see Fig. 3a). It is observed from Fig. 3b that the average voltage error is a square wave, which can therefore be expressed using Fourier series as (5). Taking into account the $2\pi/3$ phase shift between phases in a balanced three-phase system, the average voltage errors for phases *b* and *c* can be expressed as (6) and (7), with *n* being the harmonic order.

$$V_{an} = \frac{4\Delta V}{\pi} \sum_{n=1,5,7...} \frac{1}{n} \sin(n\omega t) \quad (5)$$

$$V_{bn} = \frac{4\Delta V}{\pi} \sum_{n=1,5,7...} \frac{1}{n} \sin\left[n\left(\omega t - \frac{2\pi}{3}\right)\right] \quad (6)$$

$$V_{cn} = \frac{4\Delta V}{\pi} \sum_{n=1,5,7...} \frac{1}{n} \sin\left[n\left(\omega t - \frac{4\pi}{3}\right)\right] \quad (7)$$

The resulting voltage vector due to the the non-ideal behavior of the inverter can be expressed as (8) (see Fig. 3c and d), with the transformation from phase quantities to *dq* quantities being defined by (9).

$$v_{dq} = \sum_{n=1,-5,7...} V_n e^{j(n\omega_0 t + \theta)} \quad (8)$$

$$f^s_{dq} = f_d + jf_q = \frac{2}{3}\left(f_a + f_b e^{j2\pi/3} + f_c e^{j4\pi/3}\right) \quad (9)$$

where $\theta = \pi$ when n<0 and $\theta = -\pi$ when n>0, ω_0 is the grid/microgrid frequency and V_n is given by (10)

$$V_n = \frac{2 * \Delta V}{n\pi}\left[-2\cos(n\pi) - \cos(n\,2\pi/3) + \cos(n\,\pi/3)\right] \quad (10)$$

It is concluded from (5)-(8) that the inverter non-ideal behavior produces harmonics having orders of -5, 7,…, with the corresponding harmonic magnitude being inversely proportional to the harmonic order, (10) [27] (see Fig. 4).

Fig. 5 and 6 show the frequency spectrum of the voltage and current complex vectors (experimental) for a VSI, measured at the output of the LCL filter, in island and grid connected conditions respectively. The details of the inverter can be found in Table III. Logarithmic scales are used for the magnitudes. Harmonics of order -5th and 7th are readily observable in both the voltage and current spectrums, their magnitudes being inversely proportional to the harmonic order. It is observed that in the grid connected case, the harmonics induced in the resulting current vector due to the non-ideal behavior of the inverter increase, compared to the island case. This is explained by the lower impedance during this operating condition. It is also noted that the resulting higher order harmonics at the output of the LCL filter decrease in grid-connected mode. This is due to the increased voltage drop across the filter because of the lager circulating currents.

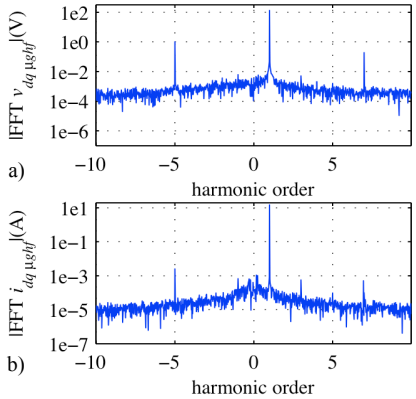

Fig. 5.- a) Voltage complex vector ($v_{dq\mu g}$) spectrum and b) current complex vector ($i_{dq\mu g}$) spectrums in island condition. The fundamental frequency is 50 Hz, with a dead-time of 3µs and switching frequency of 10kHz.

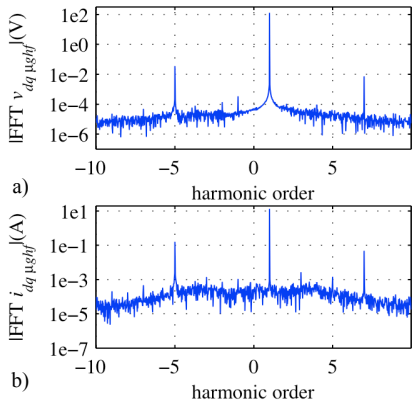

Fig. 6.- a) Voltage complex vector ($v_{dq\mu g}$) spectrum and b) current complex vector ($i_{dq\mu g}$) spectrum, in grid connected condition. The fundamental frequency is 50 Hz, with a dead-time of 3µs and switching frequency of 10kHz.

III. Islanding detection using harmonics due to the dead-time

The harmonics due to the non-linear behavior of the inverter, (8), can be modeled as (11). Every harmonic in the voltage will produce the corresponding harmonic at the same frequency in the inverter current (i_{dqhf}). The resulting harmonic component at the output of the LCL filter being (12) (see Fig. 7).

$$v_{dqhf} = V_n e^{jn\omega_0 t} \quad (11)$$

$$i_{dq\mu ghf} = \frac{v_{dqhf} - v_{dq\mu ghf} - jn\omega_0 L_1 i_{dqhf}}{jn\omega_0 L_2} \quad (12)$$

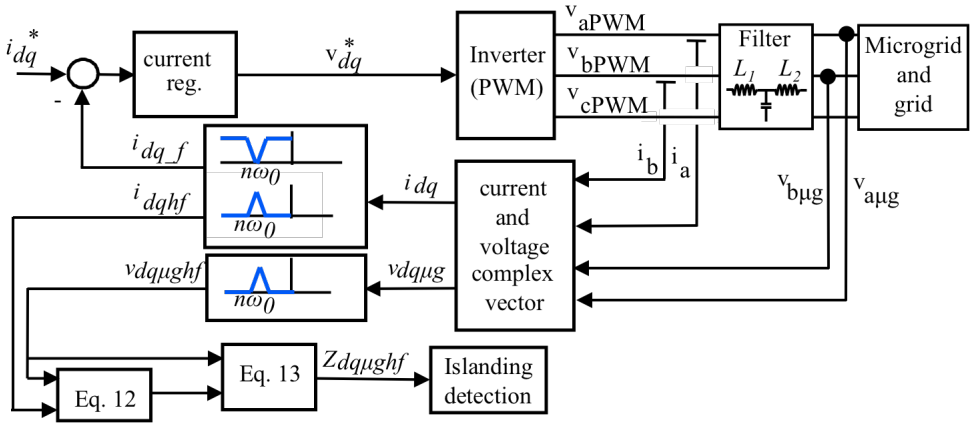

Fig. 7.- Signal processing for islanding detection using the high frequency impedance variation for islanding detection .

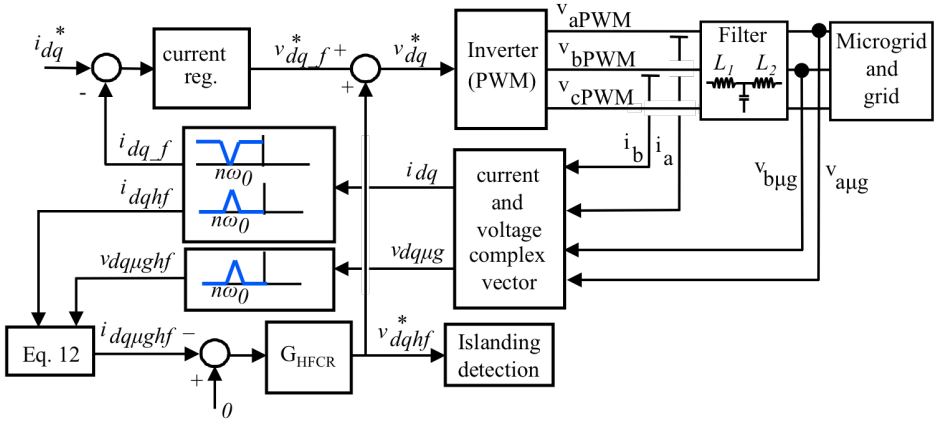

Fig. 8.- Signal processing for islanding detection when using the output of the high frequency current regulator for islanding detection.

$$Z_{dq\mu ghf} = \frac{v_{dq\mu ghf}}{i_{dq\mu ghf}} \qquad (13)$$

where $v_{dq\mu ghf}$ is the measured high frequency voltage at the filter output (see Fig. 7), L_1 is the inverter side inductance and L_2 is the grid/microgrid side inductance. The details on the implementation of islanding detection using high frequency can be found in [12, 13].

The high frequency impedance (13), calculated from the voltage and current harmonics due to the non-ideal behavior of the inverter, can be used to detect islanding [12, 13].

In principle, any of the high order harmonics due to the non-ideal behavior of the inverter could be potentially used for islanding detection purposes. However, due to the decrease of their magnitude as the harmonic order increases (10), higher order harmonics will have a lower signal-to-noise ratio, adversely affecting to the accuracy of the method. Furthermore, the maximum harmonic order might also be limited by the interaction between the injected harmonics, the LCL filter resonance frequency and the grid resonance frequency [12]. It is concluded that the -5th and the 7th harmonics would be the preferred candidates for the implementation of the method.

Two different alternatives for the implementation of the strategy, namely, *Open-loop* mode and *Current Cancellation* mode, are discussed following.

Open-loop mode: In this mode of operation, the voltage harmonic due to the dead time is used directly as a high frequency voltage excitation. Fig. 7 shows the block diagram of the signal processing used for islanding detection using this mode, including the current control of the inverter as well as the necessary filtering. Two band-pass filters, tuned at the frequency of the harmonic used for islanding detection, are used to isolate the corresponding voltage and current harmonic components. A band-stop filter in the fundamental current control loop is used to prevent the fundamental current regulator from reacting against the induced current harmonics.

Current cancellation mode:

An alternative implementation to that shown in Fig. 7 would be using a PI regulator in a reference frame synchronous with the harmonic used for islanding detection, $n\omega_0$ (see Fig. 8), with the purpose of cancelling the current induced due to the non-ideal behavior of the inverter. The output of the high frequency current regulator (v^*_{dqhf} , see Fig. 8) would contain the harmonic voltage needed to compensate for the non-ideal behavior of the inverter, which can be used for islanding detection purposes [13]. This strategy has the advantage of partially cancelling the effects on the current due the non-ideal behavior of the inverter, therefore reducing the THD of the output voltage and current.

Table I. Simulation parameters: single inverter operation.	
Grid	380 V, 50 Hz, S_{cc}=15 MVA
Inverter	380 V, 10 kHz.
Load	10 kW
Line	R=11.7mOhm. L=8.68e-4H
Simulation step	1e-7 s
Dead-time	5μs

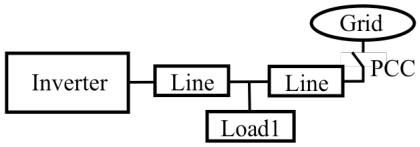

Fig. 9.- Simulation scenario.

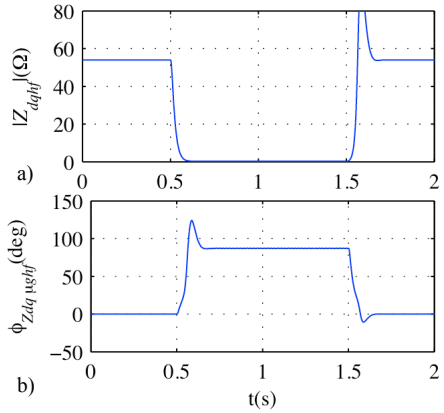

Fig. 10.- Estimated high frequency impedance magnitude, a) and phase, b).

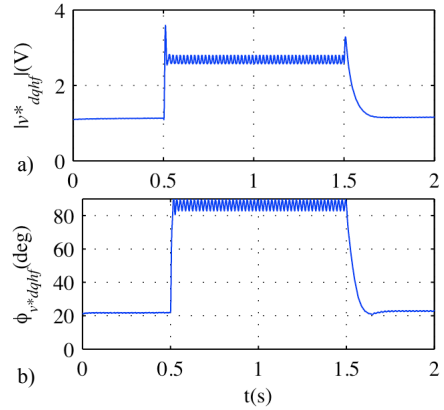

Fig. 11.- High frequency current regulator reaction magnitude, a) and phase b).

IV. Simulation results

Fig. 9 shows the scenario used to simulate the proposed method, the simulation parameters being shown in Table I.

Fig. 10a and b show the magnitude and phase of the estimated high frequency impedance in a transition from island to grid connected (t=0.5s) and from grid connected to island (t=1.5s), when the high frequency impedance is used for islanding detection (see Fig. 7). The -5th harmonic is used for the impedance estimation, though other higher order harmonics could also be used. The islanding detection standards require the detection of the impedance variation within a period of time, e.g. 1 Ohm in 2 seconds for the German standard [7] and 0.5 Ohms in 5 seconds for the Swiss and Australian standards [8, 9]. It is observed that both the magnitude and phase could be potentially used for islanding detection purpose, the change of the high frequency impedance being detected if a few ms.. It is concluded from Fig. 10 that the islanding detection requirements are widely met by the proposed method.

It is noted that the dead-time can vary in a relatively large range, depending on the rated voltage and current of the power switches [32]. In general, a shorter dead-time would be preferred, since it implies lower distortion (THD) of the output inverter voltage. Increasing the dead-time, increases the magnitude of the voltage error and current harmonics, which increases the signal to noise ratio for the islanding detection signal processing, however it also increases the THD, which is limited by connection standards [2, 28-31]. The selection of the dead-time results therefore from a compromise between the signal-to-noise ratio and meeting the connection standards in terms of THD. The simulated dead-time is 5μs, resulting in a THD of ≈0.87%, not compromising therefore the connection standards [2, 28-31].

Fig. 11 shows the high frequency current regulator output voltage when the block diagram shown in Fig 8 is used and the same transition as in Fig. 10 occurs. It is observed that the change on the current regulator output occurs in a few ms., therefore meeting the islanding detection standards [2-9]. Fig. 12 shows the magnitude of the -5, 7, -11 and 13 harmonics of the current vector, without and with compensation of the -5th harmonic. It is observed that when the compensation is implemented, the -5th fades away. Despite of the slight increase of the 7th harmonic, a reduction of the overall harmonic content, and therefore of the THD, is observed.

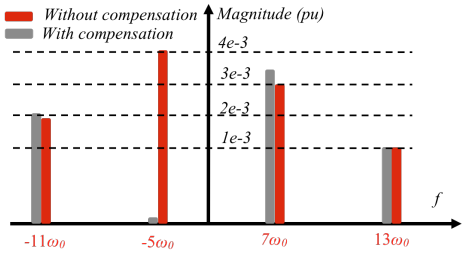

Fig. 12.- Harmonics of the current vector with and without compensation of the 5th harmonic implemented.

V. Islanding detection for parallel inverter operation

The proposed strategy has been evaluated so far for a single inverter connected to the utility grid. However in a general case, several micro-sources connected to the utility grid throughout a PCC will exist in the microgrid. To evaluate the proposed method, a scenario with three parallel-connected converters, has been built as an example (Fig. 13). The simulation parameters are shows in Table II.

Fig. 14a and b show the magnitude and phase of the estimated high frequency impedance in a transition from

Table II. Simulation parameters: parallel inverter operation.	
Grid	380V, 50Hz, Scc=15MVA
Inverter 1, 2 and 3	380V, 10kHz.
Load1,2,3 and 4	10kW
Line	11.7mOhm, 8.68e-4H
Simulation step	1e-7 s
Dead-time	5µs

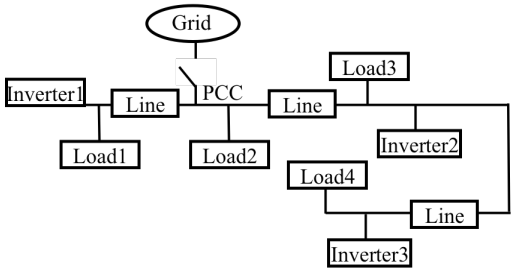

Fig. 13 Simulation scenario.

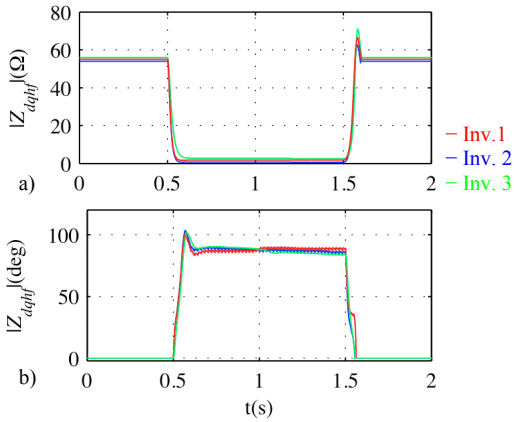

Fig. 14. *Open-loop mode*. Estimated high frequency impedance magnitude, a) and phase, b).

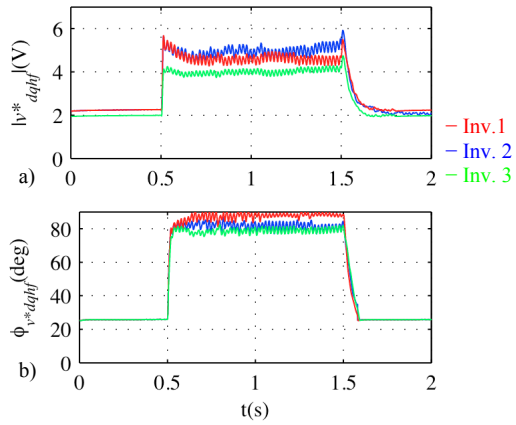

Fig. 15. *Current cancellation mode*. High frequency current regulator reaction magnitude, a) and phase, b).

island to grid-connected (t=0.5s) and from grid-connected to island (t=1.5s) in the *Open-loop mode*, the high frequency impedance being used for islanding detection (see Fig. 7). It is observed that almost the same high frequency impedance (magnitude and phase), is estimated by inverter1 and inverter2, as they are connected to the PCC throughout lines of similar characteristics (see Table II); on the contrary, the magnitude of the high frequency impedance estimated by inverter3 is larger, as it is further from the PCC (there are two series-connected lines between inverter3 and the PCC, see Fig. 13).

Fig 15a and b shows the response of the method in the *Current cancellation mode*. The high frequency current regulator output voltage (current regulator reaction, see Fig 8) when the same transition shown in Fig. 14 occurs is shown in Fig. 15. It is observed that inverter1 and 2 current regulator reactions is very similar, both magnitude and phase, but inverter 3 current regulator reaction magnitude is lower since inverter 3 it is far from the PCC. As in the single inverter case, the change of the current regulator output occurs in a few ms., therefore meeting the islanding detection standards [2-9].

VI. Experimental results

Experimental results showing the validity of the proposed method are presented in this section. Fig. 16 shows the experimental setup, the main parameters being shown in Table III. The inverter is a three-phase IGBT-based inverter, with the dead-time set to 3µs, which is the minimum value allowed by the power module.

Table III. Experimental setup parameters: single inverter operation.	
Grid	380 V, 50 Hz, S_{cc}=2 MVA
Inverter	380 V, 10 kHz, 30kVA.
Load	30 kW
Generator	380V, 10kHz, 100kVA.
Dead-time	3µs

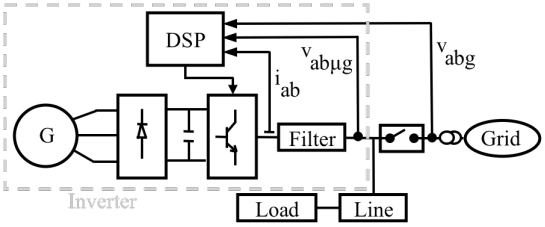

Fig. 16 Experimental setup.

Fig. 17 shows the estimated high frequency impedance magnitude and phase using the implementation shown in Fig. 7 (*Open-loop mode*), during a transition from island to grid-connected (t=0.5s) and from grid connected to island (t=2s). The estimated high frequency impedance is available in ≈100ms, which is much faster than required by islanding detection standards [2-9].

Fig. 18 shows the high frequency current regulator reaction when the *Current cancellation mode* (see Fig. 8) is used, for the same transition shown in Fig. 17. Fig. 18a shows the *d* and *q*-axis components, Fig. 18b shows the magnitude, while Fig. 18c shows the phase of the high frequency current regulator output voltage. It is observed that the change on the current regulator output occurs in a few ms, again much faster than required by the islanding detection standards. It also observed that both the magnitude and phase could be potentially used for islanding detection purpose.

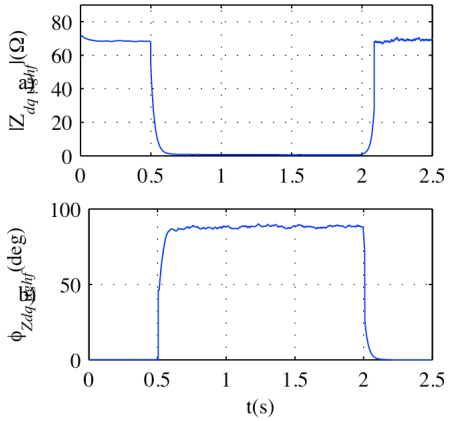

Fig. 17. *Open-loop mode*. Estimated high frequency impedance magnitude, a) and phase b). Dead-time=3µs.

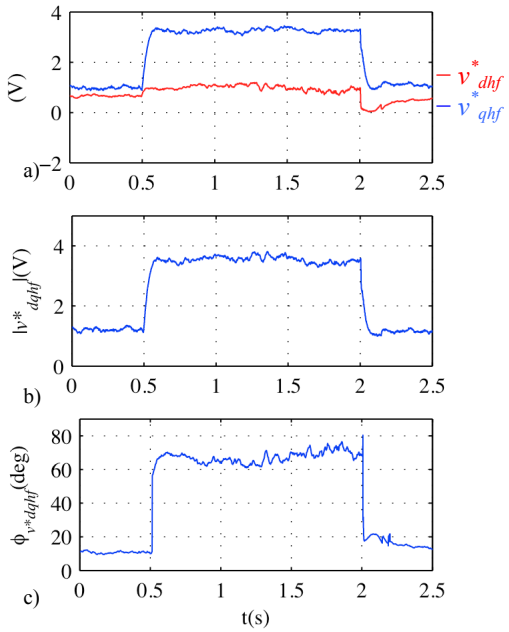

Fig. 18. *Current cancellation mode*. Current regulator reaction components, a), magnitude, b) and phase c). Dead-time=3µs.

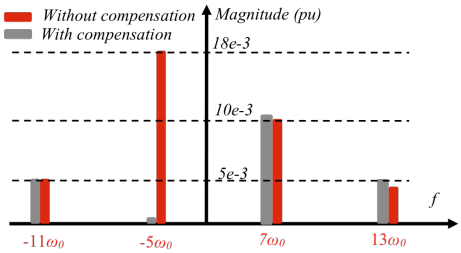

Fig. 19 Experimentally measured harmonics of the current vector with and without compensation of the 5th harmonic implemented at the PCC. Dead-time=3µs.

Fig. 19 shows the magnitude of the most relevant harmonics due to the non-ideal behavior of the inverter for the *Open-loop* and *Current cancellation* modes respectively. It is noted that the THD at the PCC is ≈2.13% in the *Open-loop mode,* reducing to ≈1.6% in the *Current cancellation mode*, i.e. when the -5th harmonic is compensated by the high frequency current regulator (see Fig. 8).

Table IV. Experimental setup parameters: parallel inverter operation.	
Grid	380 V, 50 Hz, S_{cc}=2 MVA
Inverter1 and 2	380 V, 10 kHz, 30kVA.
Inverter1 filter	L=2.4mH, C=30uF
Inverter2 filter	L=1.56mH, C=30uF
Load1 and 2	30 kW
Generator	380V, 10kHz, 100kVA.
Dead-time	3µs

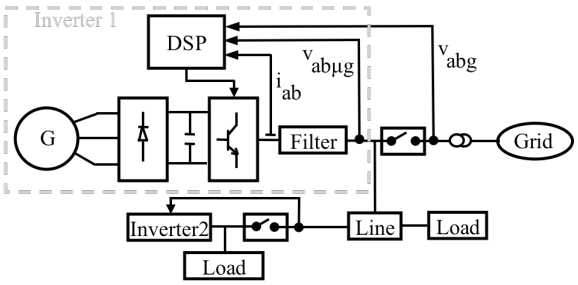

Fig. 20. Experimental setup with two parallel-connected inverters.

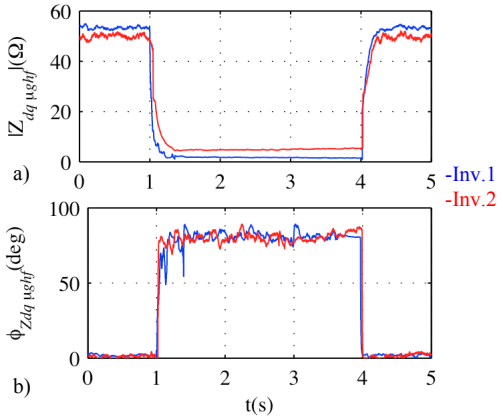

Fig. 21. *Open-loop mode*. Estimated high frequency impedance magnitude, a) and phase b). Dead-time=3µs.

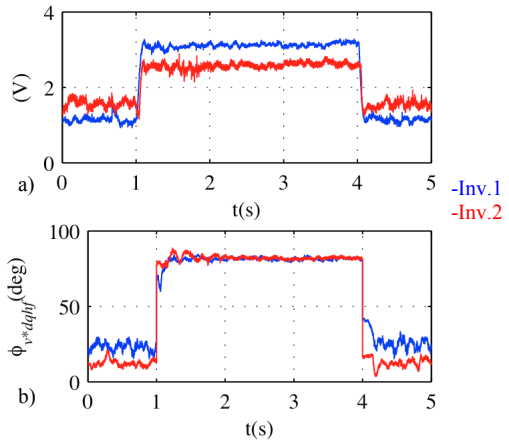

Fig. 22. Current cancellation mode. Current regulator reaction components, a) and phase b). Dead-time=3µs.

Fig. 21 and 22 shows the experimental results when two inverters are connected in parallel (see Fig. 20). The parameters of the experimental setup for this case are summarized in Table IV.

Fig. 21 shows the estimated high frequency impedance (magnitude and phase) of inverter 1 and 2 during a transition from island to grid-connected (t=1s) and from grid-connected to island (t=4s) in the *Open-loop mode* (Fig. 7), while Fig. 22 shows the high frequency current regulator reaction magnitude and phase in the *Current cancelation mode*, for same transition as in Fig. 21. It is observed from these figures that grid-island conditions are readily detectable by these two modes of operation.

VII. Conclusions

A method for islanding detection using higher order harmonics (-5th, 7th…) of the fundamental frequency due to the non-ideal behavior of PWM inverters has been proposed in this paper. Compared to already proposed methods which inject a high frequency signal, the proposed method does not need to inject additional high-frequency/harmonic, meaning that has no adverse impact on the THD of the microgrid voltages and currents.

Two different implementations, namely *Open-loop mode* and *Current injection mode*, have been analyzed. A dead-time as small as 3μs with a switching frequency of 10 kHz has been shown to be enough for reliable detection of islanding condition. With the proposed signal processing, evaluation of the grid condition takes ≈100ms, which is fast enough to meet the islanding detection standards [2-9]. Simulations and experimental results have been provided to confirm the viability of the proposed method. It is finally noted that the computational requirements of the proposed method are reduced, meaning that it can be easily integrated in an already existing digital signal processors.

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