# Synchronization in highly distorted three-phase grids using selective notch filters

Cristian Blanco, David Reigosa, Fernando Briz and Juan M. Guerrero
University of Oviedo. Dept. of Elect., Computer & System Engineering. Gijón, 33204, Spain
blancocristian@uniovi.es, diazdavid@uniovi.es, fernando@isa.uniovi.es, guerrero@isa.uniovi.es

***Abstract*— Robust extraction of the positive sequence voltage magnitude and frequency in highly distorted grids is of paramount importance in distributed power generation (DPG) systems. Phase locked loop (PLL) synchronization methods are commonly used, they can be grouped into pre-filter stage methods and filter in the loop methods. Though both provide similar performance and can be designed to reject one or more disturbing harmonic components although, compared to pre-filter stage methods, filter in the loop methods are conceptually simpler and easier to tune. Conversely, filter in the loop methods can show unstable behavior if they are not properly designed and do not include disturbance rejection strategies when the magnitude is distorted, their use not being therefore advisable when power calculation or magnitude synchronization is needed.**

**This paper proposes a filter in the loop synchronization technique able to isolate the magnitude and phase of the positive sequence voltage of the microgrid/grid even under high distorted conditions. The method is based on an angle-tracking observer, which extracts the positive sequence phase, and a scalar product to extract the positive sequence magnitude, which provides a disturbance rejection mechanism for both phase and magnitude estimation.**

***Index Terms* — Grid synchronization, complex *PLL*, complex coefficients filters, harmonic rejection.[1]**

## I. INTRODUCTION

Historically, centralized power plants have been considered the most effective and reliable way to generate electricity, the use of Distributed Power Generation (DPG) being traditionally restricted to regions lacking adequate infrastructure. However, in recent years, due to the unstoppable increased electricity demand, natural resources management and environmental concerns, DPG is growing little by little. Actually only 1% of worldwide energy is generated by DPG, which includes both renewable (wind, solar, etc…) as well as non-renewable (fuel cells, micro gas turbines, etc…) energy resources, meaning that, globally speaking, the new paradigm is at an early stage. Although DPG is usually related to small or medium size power plants, it is expected that in the medium term each home-user can become an autonomous entity, with the capability not only of demanding but also of injecting power into the grid, which is commonly known as *micro-generation* [1].

A very extended and suitable way to insert the DPGs into the electrical system is throughout microgrids. This concept was first defined in [2] as a system with renewable and no-renewable energy resources, including loads, energy storage and heat, being a controllable system providing power generation, power storage and heat to a local area.

Generally speaking, a microgrid can operate in two different modes: island and grid-connected [3]. In island mode, it works as an autonomous system, the magnitude and frequency of the fundamental voltage being set by a master source or by a central controller [4]. In grid-connected mode, the magnitude and frequency of the fundamental voltage are established by the grid [3]. Estimation of the magnitude and phase of the positive sequence voltage at the point of common coupling (PCC) being of paramount importance to guarantee stable operation and precise control of the active/reactive power flows.

During grid-connected operation, strict regulations regarding power quality (harmonics and unbalances), islanding detection, frequency shifts and maximum magnitude deviations must be fulfilled [7]. Although during island operation mode these regulations are not necessary to be met, some *"good practice"* recommendations are usually given [8]. Both positive and negative sequence harmonics usually appears at the PCC voltage in case of high power transients, non-linear loads or unbalances [9], being therefore an essential issue the development of a synchronization method that efficiently works under high-distorted conditions to prevent the converter to re-inject the disturbances to the microgrid/grid.

Synchronization methods can be roughly classified into methods that extract the grid frequency, referred as frequency locked loop (FLL) methods and methods that extract the grid phase, referred as phase locked loop (PLL) methods. The main drawback of the FLL methods is that they usually have a poor disturbance rejection capability [10] agaist harmonic distortion strategies to overcome these limitations have already been proposed [11]. On the other hand, PLL methods typically provide disturbance rejection capabilities against harmonic and unbalanced conditions [14], what makes them an appealing option. The PLL methods could be organized as follows:

a) Methods that use a PLL in the synchronous reference frame (SRF-PLL) [15] or an angle tracking observer (ATO) [16]. This method locks the grid phase and it is generally limited to undistorted networks since it does not implement any specific disturbance rejection mechanism, being achieved it by using a reduced bandwidth in their PLL/ATO PI controller.

b) Pre-filter stage methods: they use a previous filtering stage that feeds the SRF-PLL or ATO with the goal of removing specific harmonic components. The pre-filter stage can be composed by a decoupling network [12] or a cascade of filters (real or complex coefficients) [14], some

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of them allowing the extraction of high order harmonics [13].

c) Filter in the loop methods: they eliminate harmonic components by inserting a filtering stage within the SRF-PLL/ATO close-locked loop, [18]. The main drawback of these methods is that the disturbance rejection mechanism is only effective for phase extraction, but not for the magnitude. This can have adverse effects for power calculations or during the synchronization process.

In this paper, a new filter in the loop synchronization method with disturbance rejection capability for both phase and magnitude estimation is proposed. The paper is organized as follows: section II shows the basics of the proposed synchronization method. Filtering process, tuning and stability criteria are shown in section III, while a simulation based analysis of the proposed method under different working conditions is given in Section IV. Finally the conclusions are presented in Section V.

## II. GRID SYNCHRONIZATION USING SELECTIVE CASCADE OF NOTCH FILTERS

Any three-phase balanced system (voltages and/or currents) can be expressed as a complex vector into an $\alpha\beta$ reference frame (1). An ideal grid will only exhibit a positive sequence voltage (n=1). However, a negative sequence (n=-1) voltage, due to unbalanced loads, as well as higher order harmonic components (n=-5, 7, -11, 13,…), due to non-linear loads like diode and thyristor rectifiers, can be found in practice.

$$u_{\alpha\beta} = U_1 e^{j(\omega_0 t-\theta_1)} + U_{-1} e^{j(-\omega_0 t-\theta_{-1})} \sum_{\substack{n=-5,7,\\ -11,13...}} U_n e^{j(n\omega_0 t-\theta_n)} \quad (1)$$

where n is the harmonic order.

Fig. 1 shows the block diagram of the proposed method, the signal processing used to estimate the fundamental voltage component magnitude and phase is explained following.

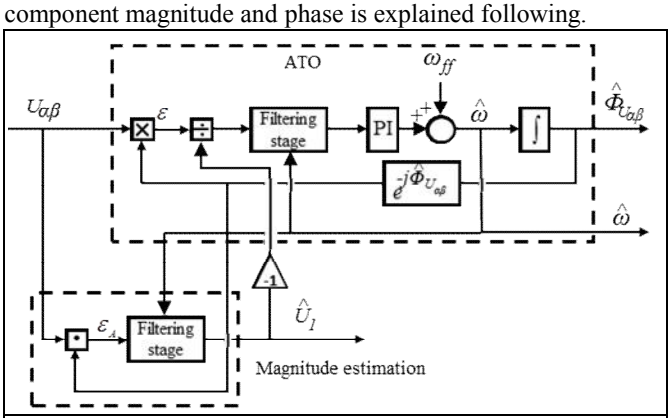



Fig. 1- Block diagram of the proposed method.

### a) Phase extraction procedure

An ATO with a filter in the loop stage is used to estimate the phase of fundamental component (positive sequence). For discussion purposes, it will be first assumed that the input signal, $U_{\alpha\beta}$, (2), consist of the fundamental component, and two harmonics, one being a positive sequence component of order m and the other a negative sequence component of order -*n*. The error signal (3) is obtained as the vector cross-product between the estimated unit vector $e^{j\hat{\phi}_{U\alpha\beta}}$, whose phase is the estimated phase of the input signal, and the input signal ($U_{\alpha\beta}$). The error is divided by the estimated fundamental input magnitude ($U_1$) in order to make it insensitive against SAGs and magnitude changes. Assuming perfect tracking of the fundamental component, $\hat{\phi}_{u_{\alpha\beta}} = \omega_0 t$, the error signal, (3), can be expressed as (4).

$$U_{\alpha\beta} = U_1 \cdot e^{j\cdot\omega_0\cdot t} + U_m \cdot e^{j\cdot m\cdot\omega_0\cdot t+\theta} + U_n \cdot e^{-j\cdot n\cdot\omega_0\cdot t+\gamma} \quad (2)$$

$$\varepsilon_\phi = U_{\alpha\beta} \otimes e^{j\cdot\hat{\phi}_{u_{\alpha\beta}}} = \mathrm{Re}\{U_{\alpha\beta}\}\cdot\sin(\hat{\phi}_{u_{\alpha\beta}}) - \mathrm{Im}\{U_{\alpha\beta}\}\cdot\cos(\hat{\phi}_{u_{\alpha\beta}}) = \sin(\hat{\phi}_{u_{\alpha\beta}})\left[U_1\cos(\omega_0\cdot t) + U_m\cos(m\cdot\omega_0\cdot t+\theta) + U_n\cos(-n\cdot\omega_0\cdot t+\gamma)\right] - \cos(\hat{\phi}_{u_{\alpha\beta}})\left[U_1\sin(\omega_0\cdot t) + U_m\sin(m\cdot\omega_0\cdot t+\theta) + U_n\sin(-n\cdot\omega_0\cdot t+\gamma)\right] \quad (3)$$

$$\varepsilon_\phi = U_m\sin((m+1)\cdot\omega_0\cdot t-\theta) + U_n\sin(-(n+1)\cdot\omega_0\cdot t-\gamma) \quad (4)$$

Assuming $\theta = \gamma = 0$, and for particular the case of n=5 (-5$^{th}$ harmonic) and m=7 (7$^{th}$ harmonic), a 6$^{th}$ harmonic is induced into the error signal (4), which amplitude is a linear combination of the amplitude of the -5$^{th}$ and 7$^{th}$ harmonics. Similarly, the -11$^{th}$ and the 13$^{th}$ harmonics will induce a 12$^{th}$ harmonic in the error signal, i.e. harmonics at frequencies $h*6*\omega_0$ ($h$=1,2,3,…) are induced into the error signal.

When a nonlinear load is fed with a three phase unbalanced voltage system, the voltage complex vector, $u_{\alpha\beta}$, can be expressed as (5), both positive and negative odd harmonics being present into the PCC grid voltage (see Fig. 2a) [19]. As a consequence of this, the error signal (4) (see Fig. 1) contains all even harmonics. Fig. 2a(red) shows the ATO input spectrum under unbalanced conditions while Fig. 2b shows the error signal spectrum, showing the harmonics at frequencies $h*\omega_0$ (h=2,4,6,8,…).

Fig. 2a shows the ATO input spectrum for balanced (blue), negative sequence component, i.e. harmonic -1, is not present, and unbalanced conditions (red), negative sequence component is present, while Fig. 2b shows the error signal spectrum for both balanced (blue) and unbalanced (red) conditions, showing the harmonics at frequencies h*6*$\omega_0$, the differences being readily observable.

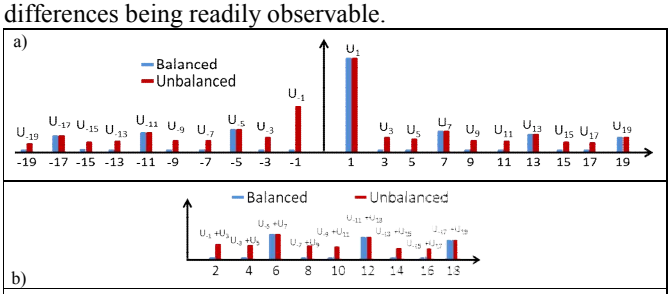



Fig. 2- Distribution of ATO harmonics in case of balanced and unbalanced ATO inputs. a) Input to the ATO and b) error signal (8), for the case of balanced and unbalanced grid voltages.

### b) Magnitude extraction procedure

To estimate the fundamental voltage component magnitude $U_1$, a scalar product is performed between the grid voltage, $u_{\alpha\beta}$, and the unit vector $e^{j\hat{\phi}_{u\alpha\beta}}$, which phase is the estimated phase of the ATO (See Fig. 1). A filtering stage is placed after the scalar product to provide a disturbance rejection mechanism for the magnitude estimation.

$$u_{\alpha\beta} = \sum_{\substack{n=\pm(2k+1) \\ k=0:1:\infty}} V_n e^{j(n\omega_0 t+\theta)} \quad (5)$$

$$\varepsilon_A = U_{\alpha\beta}(t)\cdot e^{j\cdot\omega_0\cdot t} = \mathrm{Re}\{U_{\alpha\beta}(t)\}\cdot\cos(\omega_0\cdot t) - \mathrm{Im}\{U_{\alpha\beta}(t)\}\cdot\sin(\omega_0\cdot t) = \quad (6)$$
$$= U_1 + U_m\cos((m+1)\cdot\omega_0\cdot t-\theta) + U_n\cos(-(n+1)\cdot\omega_0\cdot t-\phi)$$

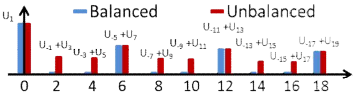



Fig. 3- Harmonics of the error signal in the proposed magnitude extraction block, for case of balanced and unbalanced conditions.

Similarly as discussed for the phase extraction procedure previously, if the input complex voltage vector is balanced (2), the scalar product will be of the form shown by (6). For the case of $\theta=\gamma=0$, the spectrum of $\varepsilon_A$ consist of a DC component, whose amplitude is the grid fundamental voltage component ($\underline{U_1}$), and a set of harmonic components located at $h*6*\omega_0$ ($h$=1,2,3,…), the corresponding frequency spectrum is shown in Fig. 3. Conversely, if the input complex vector of the magnitude estimation block is the same as an unbalanced-fed nonlinear load defined in (5), the spectrum of $\varepsilon_A$ is composed by a DC component, which amplitude is the grid fundamental voltage component ($U_1$), and harmonic components located at $h*2*\omega_0$ ($h$=1,2,3,…).

## III. Filtering Stage, Tuning Process and Stability Criteria

To reject the disturbances discussed in the previous section, a filtering stage consisting on "$n$" cascade notch filters is proposed (see Fig. 4), their design, tuning and digital implementation, as well as their stability analysis, is presented in this section.

### *a) Filtering stage design*

The transfer function of a generic second order analog notch filter can be expressed as (7), where $\xi$ sets the depth and the width of the filter and $\Omega_n$ is the notch frequency. Since the proposed method is intended to be implemented in a DSP based system, the system design and stability analysis will be performed in the discrete time domain. To guarantee precise transformation of the frequencies of interest from the continuous domain to the discrete domain, Tustin discretization will be used (8), (9) being obtained by discretization of (7).

$$NF(s) = \frac{s^2+\Omega_n^2}{s^2+\xi\cdot s+\Omega_n^2};\ \Omega_n = n\cdot\Omega_o \quad (7)$$

$$s = \frac{2}{T_s}\frac{z-1}{z+1} \quad (8)$$

$$NF_{\omega_n}(z) = b\frac{1-2\cdot\cos(\omega_n)z^{-1}+z^{-2}}{1-2\cdot b\cdot\cos(\omega_n)z^{-1}+(2\cdot b-1)z^{-2}} \quad (9)$$

$$\omega_n = \frac{n\cdot\omega_0}{f_s/2} \quad (10)$$

$$b = \frac{1}{1+\beta} \quad (11)$$

$$\beta = \frac{\sqrt{1-A_{-3dB}^2}}{A_{-3dB}}\tan\left(\frac{BW}{2}\right);\ BW = \frac{\Delta w}{f_s/2} \quad (12)$$

$$FS(z) = \prod_{n=1}^{N} NF_{\omega_n}(z) = \frac{\prod_{i=1}^{C}(z-c_i)}{\prod_{k=1}^{P}(z-p_k)} \quad (13)$$

where $\omega_n$ is the notch frequency (10), $\omega_0$ stands for the rated grid frequency, $T_s$ is the sampling time ($f_s$ is the sampling frequency), BW is the notch filter bandwidth and $A_{-3dB}$ is the notch filter magnitude at half squared magnitude ($\sqrt{2}/2$) (See Fig. 5).

As already mentioned, the frequency spectrum of the PI regulator input (4) and amplitude errors (6) consist of harmonic components at $h*6*\omega_0$ ($h$=1,2,3,…) or $h*2*\omega_0$ ($h$=1,2,3,…), depending on whether the grid voltage is balanced of unbalanced. A filtering stage consisting on a cascade of "$n$" second order notch filters, (13), is used to remove these harmonic components. The notch filter design requirements, [20], indicates that this transfer function must have $C$ ceros located on the unit circle at the notch frequencies ($e^{\pm\omega_n}$) to make zero gain at notch frequencies and $P$ poles adjacent to the zeros to assure unitary gain for the non-notch band, with the poles located within the unit circle [20]. The nearer the poles are to the unit circle, the smaller will be the bandwidth of the notch filter [20].

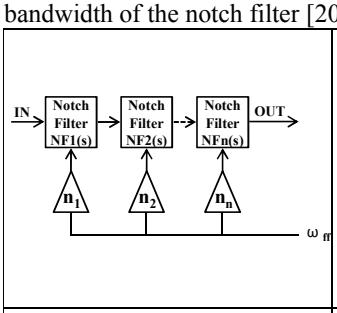



Fig. 4- Filtering stage block diagram

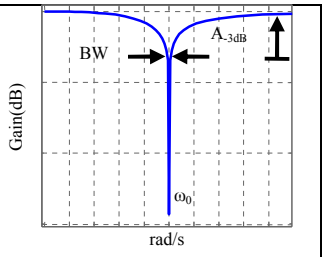



Fig. 5- Digital notch filter design

The international standards for grid-connected converters, [6], limit the maximum total voltage harmonic distortion (THD) to 5%, each individual harmonic magnitude being smaller than 4% for harmonic orders lower than 11$^{th}$, 2% for the harmonic orders between 11$^{th}$ and 17$^{th}$, 1.5% for the harmonic orders between 17$^{th}$ and 23$^{rd}$, 0.6% for harmonic orders between 23$^{rd}$ and 35$^{th}$ and 0.3% for orders higher than 35$^{th}$. Since each notch filter adds an additional phase shift into the estimated phase, only harmonics whose order is lower than 11$^{th}$ will be considered for the filtering process. The proposed filtering stage consists of three notch filters, (9), located at $\omega_2$=100, $\omega_4$=200 and $\omega_6$=300Hz, that corresponds to -1$^{st}$, 3$^{rd}$,-3$^{rd}$, 5$^{th}$, -5$^{th}$ and 7$^{th}$ harmonics (see section 2). Other harmonic components could be taken into account, the method being reconfigurable to reject them.

It is also important to note that a lowpass filter could be placed inside the filtering stage in order to deal with white Gaussian noise coming from the sensors and electronics. It is not necessary to include it inside the ATO since the PI regulator acts as a lowpass filter, but it can be placed inside the

magnitude estimator. In this case, a 300Hz lowpass filter has been used.

If (9) is used for the selected notch frequencies using a bandwidth of 50rad/s, the zero-pole map shown at Fig. 6 is obtained. It is observed that all zeros are placed on the unit circle, the poles being close to the zeros and inside the unit circle, following therefore the design requirements.

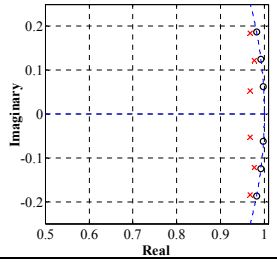



Fig. 6- Filtering stage zero-pole map.

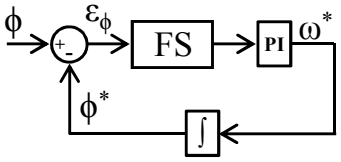



Fig. 7- ATO linear model.

*b) Tuning methodology and stability analysis*

This subsection analyzes the tuning methodology of the PI controller to guarantee the system stability and adequate dynamic response. The linearized model of the proposed ATO is shown in Fig. 7, where the *ATO* error, $\varepsilon_\phi$ (4), is proportional to the *sine* of the difference between the estimated ($\phi^*$) and the real angle ($\phi$); $\sin(\phi-\phi^*)\approx\phi-\phi^*$ can be safely assumed if the angle error is small enough. The *ATO* closed-loop transfer function and the overall transfer function are given by (14) and (15) respectively, $G_{PI}(s)$ being the transfer function of the PI controller, (16), and FS the transfer function of the filter stage.

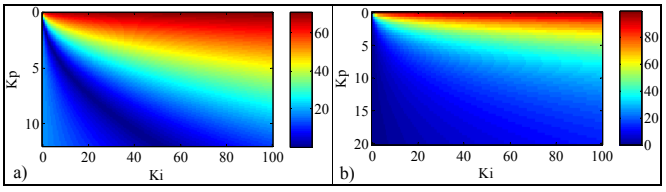
$$\frac{\phi^*(s)}{\phi(s)}=\frac{FS(s)\cdot G_{PI}(s)}{s+FS(s)\cdot G_{PI}(s)} \quad (14)$$

$$\frac{\omega^*(s)}{\phi(s)}=\frac{s\cdot FS(s)\cdot G_{PI}(s)}{s+FS(s)\cdot G_{PI}(s)} \quad (15)$$

$$G_{PI}(s)=K_p+\frac{K_i}{s} \quad (16)$$

Different figures of merit were taken into consideration for the selection of $K_p$ and $K_i$ to guarantee stability and adequate dynamic performance, including frequency based (difference between phase margin, *PhMar*), and time based (maximum overshoot, *Over*, and settling time, *setTime*). A global performance index, *GPI*, of the form shown by (17) can be defined, with the weights $w_{phMar}$, $w_{over}$ and $w_{setTim}$ being set according to the importance given to each one on the tuning criteria. This is discussed later in this subsection.

$$GPI=w_{phMar}\cdot phMar+w_{over}\cdot over+w_{setTim}\cdot setTim \quad (17)$$



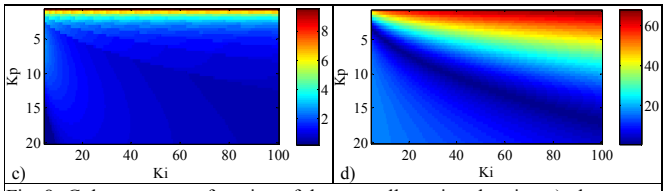




Fig. 8- Color maps as a function of the controller gains showing a) the absolute value of the difference between the system Phase Margin and the optimum value (70 deg), b), overshoot in %, c), settling time in seconds d) and global performance index (GPI) (17).

Color maps were found to be convenient for visualization purposes. The optimum value for the phase margin was selected to be 70º [22], while for the overshoot and time response, the lower is their value, the better is the behavior of the system. Fig. 8a shows *PhMar*, which is defined to be *PhMar*=|*Phase margin*–70º|, i.e. the absolute value of the difference between the actual and the target phase margin, as a function of $K_p$ and $K_i$. Figs. 8b and 8c show the overshoot percent and settling time respectively, as a function of $K_p$ and $K_i$. Fig. 8d shows the global performance index (17). For the selected weights, $w_{phMar}$, $w_{over}$ and $w_{setTim}$, in (17), relatively large values would normally be assigned to $w_{phMar}$, since stability is key, while smaller values would be used for $w_{over}$ and $w_{setTim}$. $w_{phMar}$=0.9, $w_{over}$=0.01 and $w_{setTim}$=0.1 were used for the results shown in this paper. Fig. 8d shows the *GPI* color map. It is observed from the figure that the color map has smooth transitions, meaning that slight changes in the controller gains do not have a sharp impact on the overall stability. The values of the gains providing the minimum in the color map in Fig. 8d are $K_p$=5.77 and $K_i$=17.31.

## IV. Simulation Analysis under Grid Distorted Conditions

Simulation results showing the validity of the theoretical analysis are presented in this section. Fig. 9 shows the proposed simulation setup where a programmable AC source was used to produce six different disturbances in the grid voltage: 1) grid frequency change, 2) grid voltage magnitude change, 3) grid unbalance, 4) harmonic conditions, 5) simultaneous change of the grid frequency and magnitude and 6) simultaneous change of the grid frequency and harmonic distortion.

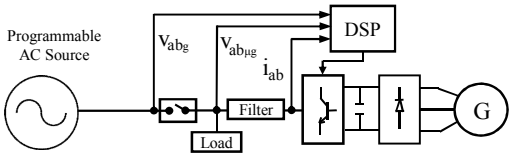



Fig. 9- Block diagram of the proposed method.

For each disturbance, the performance of the proposed method is compared with two well know, widely used synchronization methods: *MCCF-PLL* [12] and *CCCF-CPLL* [14]. Although a large number of synchronization methods could be found in the literature, the *MCCF-PLL* and the *CCCF-CPLL* methods have been selected since they are methods designed to be used under high polluted networks [14].

The *MCCF-PLL* and the *CCCF-CPLL* methods have been configured to reject -1st, -5th and 7th harmonics. The bandwidth

of the stop filters has been set to 50rad/s for all methods, meanwhile the band-pass filter for the fundamental component has been set to 600 rad/s in *MCCF-PLL* and *CCCF-CPLL*. The lowpass filter of the proposed method has a bandwidth of 300 Hz (≈ 1900 rad/s).

Since the *CCCF-CPLL* method uses the same ATO than the proposed method, the same tuning parameters have been used for both methods. The same tuning methodology as describe in the previous section was followed for the *MCCF-PLL*, resulting in a PI regulator gains of $K_p$=4.06 and $K_i$=8.37.

**Table I** – *Grid parameter boundaries by normative[23-25]*

| | Maximum value | Clearance time (s) |
|---|---|---|
| Frequency deviation | $47 \leq f_{Hz} \leq 53$ | 0.2 |
| Voltage deviation | $0.8 \leq V_{pu} \leq 1.2$ | 0.2 |
| Unbalance factor | 4% | - |
| Harmonic distortion | 4% individual harmonic | - |

The applied disturbances have been selected with the aim to reach the limits of the different grid codes [23-25] (see Table I, where the clearance time refers to the detection and disconnection time from the main grid). Simulation results are given per unit for visualization purposes, being the rated grid voltage and frequency are 220V and 50Hz respectively. Magnitude, frequency and phase signals are plotted since they are used commonly for different control strategies like synchronization, magnitude/frequency restoration, droop control, power calculation, etc…

*a) Frequency deviations test*

Fig. 10a and 9b show the frequency and magnitude of the AC source voltage that includes both ramp-like and step-like frequency deviations, intended to emulate the inertia of synchronous generators and/or the connection of disconnection of big loads in weak grids or islanded drooped microgrids [26]. A frequency ramp-like change of 3 Hz in 0.2s and a step-like change of 6 Hz were performed (from the upper to the lower limit of Table I).

Fig. 10c, 9d and 9e show the estimated magnitude, frequency and phase error respectively, the phase error being calculated as the phase difference between the AC source fundamental voltage phase and the estimated phase.

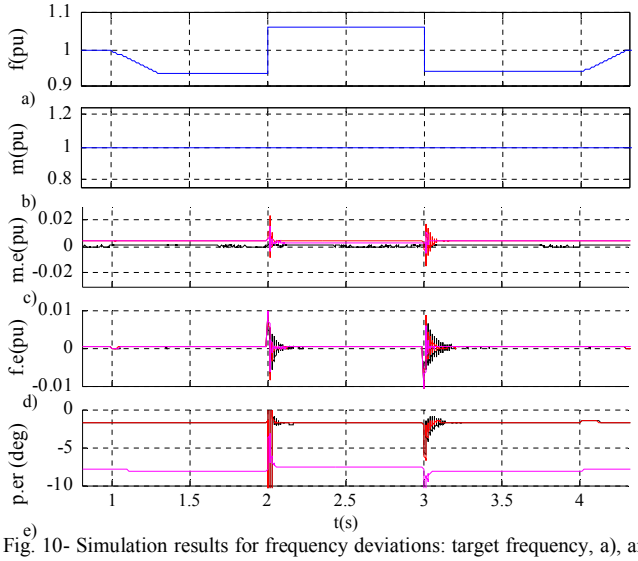



Fig. 10- Simulation results for frequency deviations: target frequency, a), and magnitude, b), magnitude error, c), frequency error, d) and phase error, e).

It is observed from Fig. 10c that the proposed method shows a good magnitude tracking capability with zero steady state error. On the other hand, the remaining methods show a small (1%) steady state magnitude error, showing small transient magnitude oscillations when the frequency step changes are performed (t=2s and t=3s). All the methods show similar frequency tracking capabilities (see Fig. 10d), negligible steady-state frequency errors are observed even when a 6Hz frequency step is performed.

The main performance mismatch between methods is related to the phase delay produced by the filtering stage (see Fig. 10e). The proposed method produces a phase delay of ≈1.7 deg (as *MCCF-PLL* method) meanwhile the delay introduced by the *CCCF-PLL* method is ≈8 deg. However these offsets can be easily compensated by means of the filters transfer functions.

*b) Magnitude deviations test*

Table I shows the maximum allowed magnitude deviations for grid-connected systems. In the present test, the frequency remains constant (see Fig. 11a) as long as the magnitude of the AC source changes from 1pu to 0.8pu in 0.2s, ramp-like, and from 0.8 to 1.2pu, step-like change, from the lower to the upper limit, t=2s, and backwards, t=3s (see Fig. 11b).

While all of the tested methods response under ramp-like deviations is adequate (magnitude (Fig. 11c), frequency (Fig. 11d) and phase (Fig. 11e) errors are negligible), when a step-like change is applied, small transient oscillations appear in the tracked frequencies, magnitudes and phases. The proposed method shows zero steady-state magnitude, frequency and phase errors. The frequency oscillations, whose peak magnitude is ≈0.01 p.u, are damped after 0.25s. The same phase delays were obtained as in subsection IV*a*, where small oscillations appear into the phase error due to the frequency oscillations.

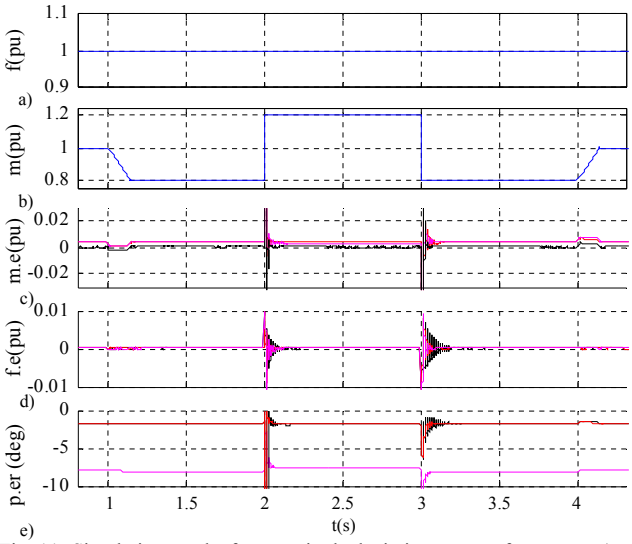



Fig. 11- Simulation results for magnitude deviations: target frequency, a), and magnitude, b), magnitude error, c), frequency error, d) and phase error, e).

*c) Unbalance test*

Unbalanced conditions are caused mainly by unbalanced loads operation. E.g. most low-voltage loads and some medium-voltage ones (e.g. electric traction motors), are single-phase fed. This equipment, when connected to a three-phase

system, causes unbalanced load currents, which creates non-symmetrical voltage dips in individual phases causing voltage unbalances. The voltage unbalance factor (VUF) is usually defined as the ratio between the negative sequence and the positive sequence voltage components [27], the limits being shown in Table I (limited to 4%). Two voltage unbalance factor values were tested (see Fig. 12b) in order to compare the performance of the proposed method, while the frequency remains unchanged (see Fig. 12a). A 4% lower-normative unbalance factor was selected during 1s<t<2s and also a 10% upper-normative unbalance factor was used in 2s<t<3s. The unbalance rejection capability of all of the tested methods is high, both in magnitude (Fig. 12c), frequency (Fig. 12d) and phase (Fig. 12e). The proposed method shows the best global performance, exhibiting negligible steady-state errors (magnitude, frequency and phase). The behavior under step-like unbalance variations is similar than the magnitude deviations test, where small oscillations were obtained that are damped after 0.25s.

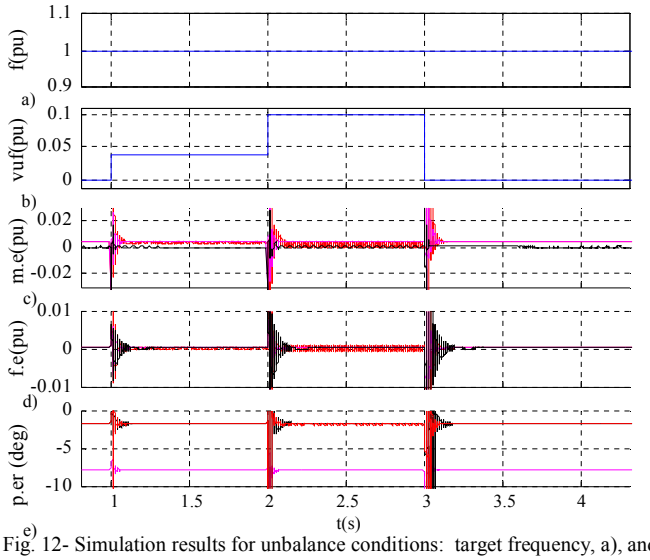



Fig. 12- Simulation results for unbalance conditions: target frequency, a), and voltage unbalance factor, b), magnitude error, c), frequency error, d) and phase error, e).

*d) Harmonic conditions test*

Historically, electric machines were the main sources of harmonics in power systems, however, the power electronic equipment that is commonly used now days, should be included as a source of harmonic distortion. Section III.a and Table I describe the maximum harmonic distortion allowed for grid-connected equipment.

Fig. 13 shows the simulation results of the proposed scenario, where a 5th harmonic with a magnitude modified from 0pu to 0.04pu at t=1s, changed to 0.1pu at t=2s and finally removed at t=3s is injected by the AC source, meanwhile the frequency remains unchanged (Fig.12a and b).

*MCCF-PLL* and *CCCF-PLL* methods do not reject completely the injected harmonics and oscillations were found both in magnitude and frequency (Figs. 12c, d) that disappear in the estimated phase due to the lowpass effect of the integrator (Fig. 13e). The magnitude error is close to 0.005pu for the *MCCF-PLL* and *CCCF-CPLL* methods when a 0.04 p.u. 5th harmonic is injected and 0.01pu when the 5th harmonic magnitude changes to 0.1pu. A similar behavior is observed for the frequency estimation (see Fig. 13c). The proposed method shows the better performance; negligible steady state error in magnitude, frequency and phase estimations and fast transient response when the steps commands are applied (t=1, 2 and 3s).

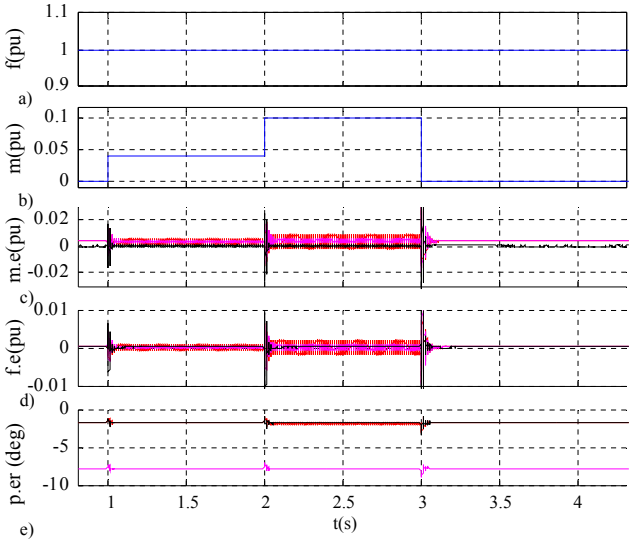



Fig. 13- Simulation results for harmonic conditions: target frequency, a), and harmonic instant magnitude (p.u.), b), magnitude error, c), frequency error, d) and phase error, e)

*e) Simultaneous frequency and magnitude deviation test*

A simultaneous change in magnitude and frequency which can be caused by the connection and disconnection of big loads in weak grids or islanded drooped microgrids is presented in this section. Fig. 14a and b show the frequency and magnitude changes including ramp-like and step-like patterns.

The proposed synchronization method shows an overall acceptable tracking capability, both in magnitude, frequency and phase. In magnitude and frequency terms, it does not show steady state error (*MCCF-PLL* and *CCCF-CPLL* show a small magnitude error) and it exhibit 1.7deg. of phase delay in the estimated phase.

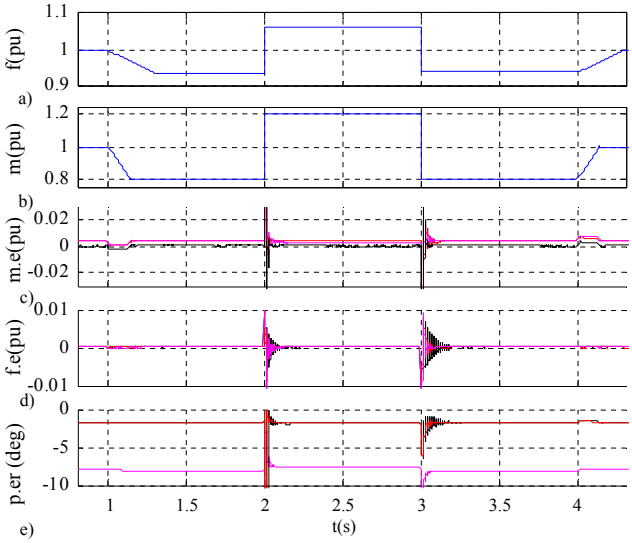


Fig. 14- Simulation results containing simultaneous frequency and magnitude deviations: target frequency, a), and magnitude, b), magnitude error, c), frequency error, d) and phase error, e).

*f) Simultaneous frequency deviations and harmonic conditions test*

This test shows a combination of tests *a)* and *d)* where frequency deviations (Fig. 15a) and a 5th harmonic, whose magnitude follows Fig. 15b, is generated by the AC source. This test is run to confirm the harmonic rejection capability under frequency deviations. It is observed from Fig. 15c and d that the proposed method estimates the magnitude and frequency with negligible steady-state error, while the same phase delays as in the previous test are obtained (see Fig. 15d). It is noted from Fig. 15c, d and e, that the obtained results both for the proposed method, CCCF-PLL and MCCF-PLL methods follows a mixture between tests *a* (Fig. 10) and *d* (Fig. 13).

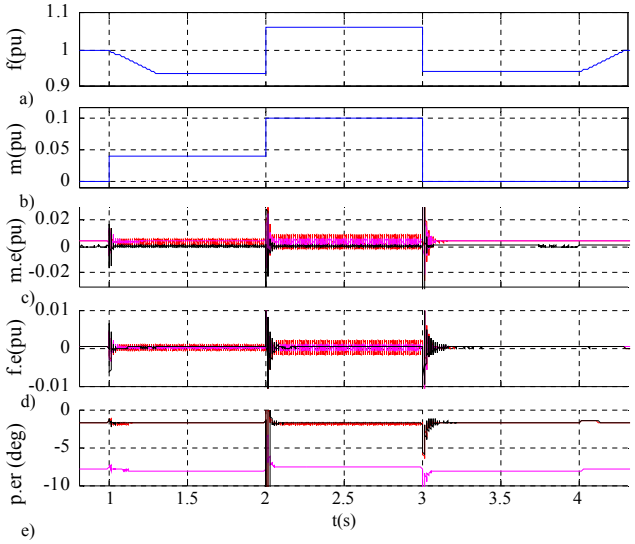



Fig. 15- Simulation results containing simultaneous frequency deviations and harmonic conditions: a) target frequency, b) 5th harmonic instant magnitude (p.u.), c) magnitude error (p.u.) d) frequency error (p.u.), e) phase error (deg).

## V. Experimental Results

In this section the experimental results testing the performance the synchronization methods are presented. The experimental setup is shown in Fig. 16, where LCL filters, with a resonance frequency of 575Hz are used. The master inverter was programmed to produce the same disturbances discussed in the previous section whereas TMS320F28335 DSP has been used for the implementation of the algorithms, using a sampling and switching frequency of 10 kHz. As simulation results, Tustin transformation was used for the discretization of the continuous transfer functions. The different methods have been tuned to the values obtained through the optimization method described in the Section II.

It is also important to note that the execution time of the proposed method is 10 µs meanwhile the *CCCF-CPLL* uses 12.8 µs and the *MCCF-PLL* method consumes 13.8 µs where the proposed method is configured to reject -1st, 3rd,-3rd, 5th, -5th and 7th harmonics (Section III) meanwhile the CCCF-CPLL and the MCCF-PLL only rejects -1st, 5th and 7th harmonics. This denotes the simplicity of the notched filtering on the loop stage designed.

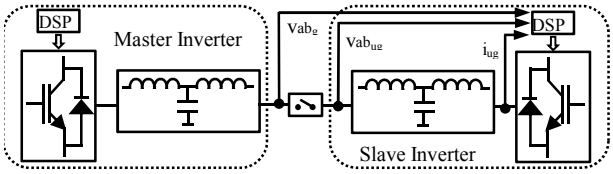



Fig. 16 –Experimental Setup

*a) Frequency deviations test*

Fig. 17 shows the experimental results under frequency deviations implemented into the master inverter output voltage. Ramp-like (t=1, 4s) and step-like (t=2, 3s) deviations have been used. As simulation results, the proposed method shows an excellent magnitude and frequency tracking capability, where negligible steady-state error is observed (excluding white Gaussian noise) both in the magnitude (Fig. 17c) and frequency (Fig. 17d) error signals. It is worth to mention that some spikes are present into the frequency error when a 6Hz (0.12 p.u.) step-like frequency variation is produced that cannot be considered since this type of deviation is less likely to occur in practice due to the large inertia of the generators.

Talking into phase error terms (Fig. 17e), the same phase delays are obtained as simulation results, where the phase error contains less Gaussian noise than the frequency error due to the lowpass behavior of the phase integrator. Small phase deviations appear when a 0.12 p.u. step-like frequency command is applied that are rectified after 50ms.

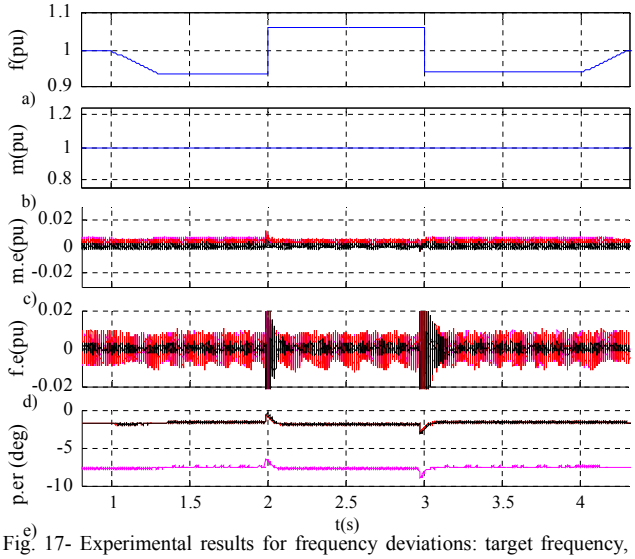



Fig. 17- Experimental results for frequency deviations: target frequency, a), and magnitude, b), magnitude error, c), frequency error, d) and phase error, e).

*b) Magnitude deviations test*

Fig. 18 shows the magnitude deviation experimental results when the master inverter output voltage follows Fig. 18b. The proposed method exhibits good magnitude tracking capability (mean of the magnitude error is close to zero) and it also shows better Gaussian noise cancellation than the remaining methods. This difference is more noticeable into the frequency error (Fig.17d), where the Gaussian noise is higher for the *MCCF-PLL* and the *CCCF-CPLL* methods. Some spikes are

obtained when a step-like deviation is performed that not affect in a great degree the behavior of the slave inverter because of its voltage and current control loops.

As Fig.17e shows, all of the tested methods exhibit undistorted steady-state phase and small phase deviations are present when a step-like magnitude change is performed.

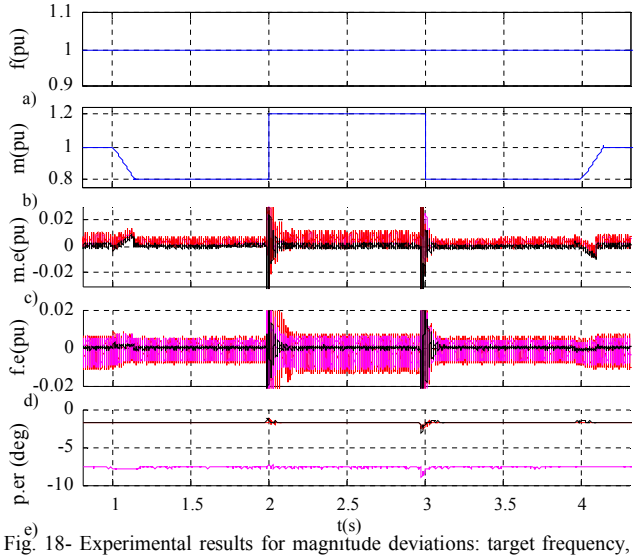



Fig. 18- Experimental results for magnitude deviations: target frequency, a), and magnitude, b), magnitude error, c), frequency error, d) and phase error, e).

*c) Unbalance test*

A negative sequence component whose magnitude follows Fig. 19b has been injected into the master inverter output voltage. The proposed method shows good rejection to the double-fundamental-frequency harmonic created by the unbalance, even when a 0.1 p.u. negative sequence is present (2<t<3s), both in magnitude (Fig. 19c), frequency (Fig. 19d) and phase (Fig. 19e).

The remaining methods show a similar good performance dealing with unbalances, as predicted in simulation results.

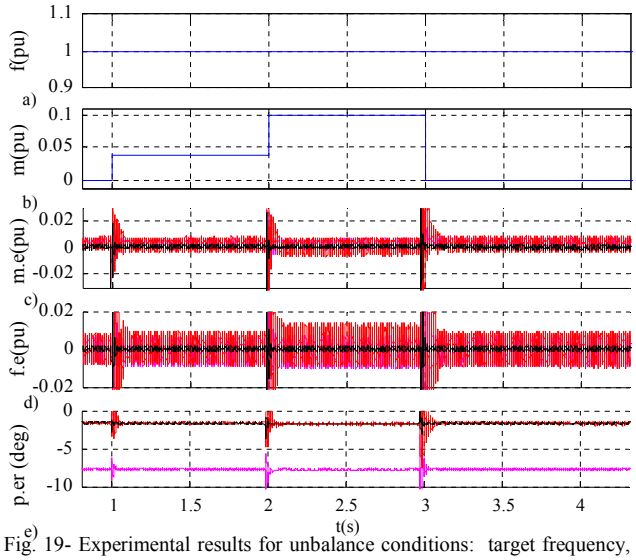



Fig. 19- Experimental results for unbalance conditions: target frequency, a), and unbalance factor, b), magnitude error, c), frequency error, d) and phase error, e).

*d) Harmonic conditions test*

This section contains the experimental results when a 5th harmonic, whose magnitude follows Fig. 20b, was injected into the master inverter output voltage.

*MCCF-PLL* and *CCCF-CPLL* shows equivalent magnitude and frequency harmonic rejection capability meanwhile the proposed method exhibits better harmonic cancellation as Figs. 18c and 18d show.

Fig. 19e shows the phase error for all methods under harmonic distortion. It is important to note that the phase delays obtained match with the simulation ones, where small spikes appear into the phase error when the magnitude of the harmonics change sharply.

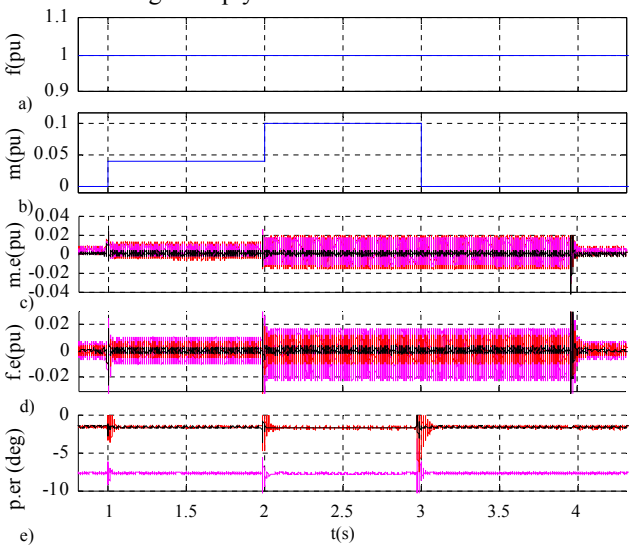
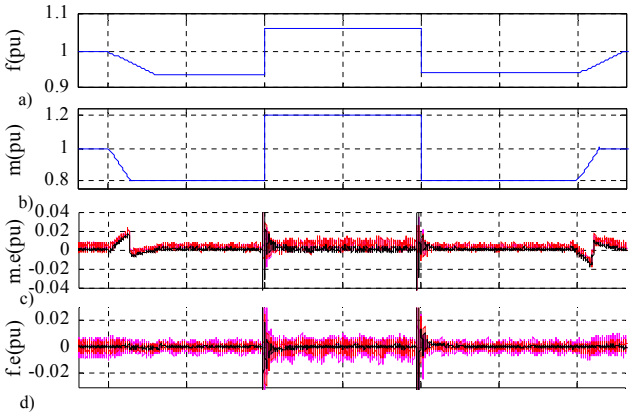



Fig. 20- Experimental results for harmonic conditions: target frequency, a), and harmonic instant magnitude (p.u.), b), magnitude error, c), frequency error, d) and phase error, e)

*e) Simultaneous frequency and magnitude deviation test*

In this test a simultaneous change both in frequency (Fig. 21a) and magnitude (Fig. 21b) is applied. All of the tested methods show a small magnitude error when a simultaneous ramp-like change (t=1, 2s) occurs both in frequency and magnitude that is slightly smaller for the proposed method.

The frequency and angle tracking is good, showing some spikes when ramp-like deviations are performed that confirm simulation results.



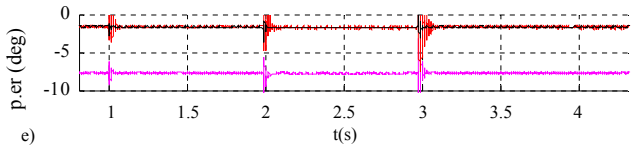



Fig. 21- Experimental results containing simultaneous frequency and magnitude deviations: target frequency, a), and magnitude, b), magnitude error, c), frequency error, d) and phase error, e).

*f) Simultaneous frequency deviations and harmonic conditions test*

This test aims to verify simultaneously the frequency-adaptive and harmonic rejection capabilities. The frequency of the master inverter output voltage follows Fig. 22a meanwhile the magnitude of the injected 5th harmonic is changed using Fig. 22b.

As Fig. 22 shows, there are not substantial differences between the magnitude (Fig. 22c), frequency (Fig. 22d) and phase (Fig. 22e) errors present in this test from the errors obtained in subsection V.d (Fig. 20): "*harmonic conditions test*" that proves the excellent frequency tracking capability of the tested methods. The proposed method shows the same performance working at different frequencies.

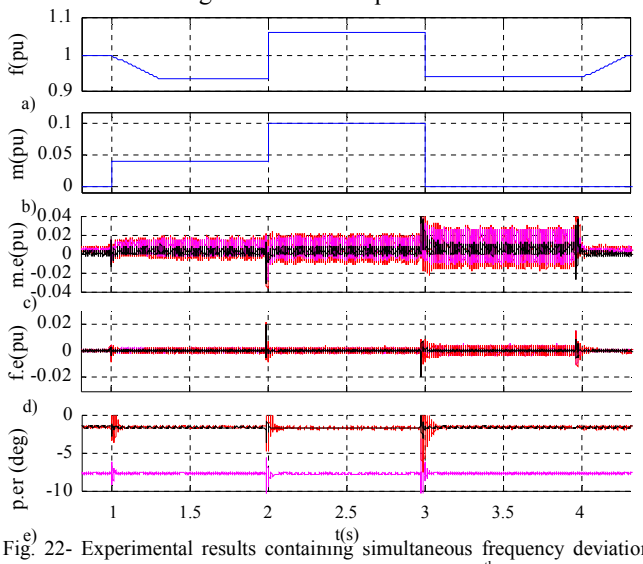



Fig. 22- Experimental results containing simultaneous frequency deviations and harmonic conditions: a) target frequency, b) 5th harmonic instant magnitude (p.u.), c) magnitude error (p.u.) d) frequency error (p.u.), e) phase error (deg).

## VI. Conclusions

A synchronization method for islanded and grid connected power converters is presented in this paper. The method is based on a notch-filter in the loop stage to eliminate disturbances and a complex PLL to extract the frequency/phase of the fundamental voltage component. A magnitude extraction block based on the scalar product to obtain the positive sequence amplitude of the grid voltage has been proposed.

The design of the filtering stage, the tuning of the controller and the stability of the whole method has been discussed. Simulation and experimental results comparing the proposed method with existing synchronization methods have been presented, using six different disturbances. It is concluded from the simulation and experimental results that the proposed method shows an excellent overall performance accomplishing with international detection standards, showing better performance than the existing methods in terms of disturbance rejection, time consumption and simplicity.

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