Different purpose design strategies and techniques to improve the performance of a Dual Active Bridge with phase-shift control

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***Abstract*— This paper addresses the performance of the bidirectional Dual Active Bridge (DAB) converter. One of the advantages of the DAB is the possibility to achieve Zero Voltage Switching (ZVS) operation in all the switches of this converter. However, the ZVS operation range can be lost for light loads, especially if high voltage is required in at least one of the DAB ports and the phase-shift control is used to regulate the power processed by the converter. Theoretically simple averaged and small-signal models are presented for the DAB converter. Using the study presented in this paper, the boundaries of ZVS operation can be easily evaluated. The proposed models and analysis of the ZVS boundaries allow the proposal and evaluation of two different design strategies with different purposes: on the one hand, increasing the ZVS operation range and, on the other, improving efficiency at full load. Moreover, some techniques are presented for increasing the ZVS operation range and improving the efficiency of the DAB at full load (both using phase-shift control) employing the aforementioned analysis to obtain certain design criteria and conclusions. Finally, the proposed models, design strategies and techniques to improve the performance of the DAB are experimentally tested using a 1kW prototype with input and output voltages of 48V and 400V, respectively.**

I. INTRODUCTION

Energy efficiency is one of the challenges of the new millennium. A more intelligent use of electrical energy (greater efficiency, energy recovery, etc.) and the flexible use of clean energy sources are on the leading edge of society concerns. The next generation of power supply systems should be more flexible, more competitive, perform better (greater efficiency, durability, autonomy, etc.) and, in general, be more intelligent. For instance, the inclusion of an intermediate storage system provides a new degree of freedom in applications such as regenerative braking, electrical or hybrid vehicles, renewable energy generators, local energy generation, etc. These examples usually require an energy storage device to store up possible extra energy and supply the network during high demand periods thanks to the stored energy.

The increasing demand for intermediate storage of electrical energy in battery systems has resulted in the need for bidirectional DC/DC power converters, usually involving galvanic isolation. A Dual Active Bridge (DAB) is a bidirectional DC/DC converter often used in these kinds of applications. This topology presents the advantages of soft-switching commutations, automatic bidirectional power flow and high efficiency. The use of this topology is thus proposed for applications where power density, cost, weight, and reliability are critical factors. The topology has been extensively analyzed and different control methods have been proposed. This paper presents a conceptually simple analysis of the converter and new improvements with different purposes, such as increasing the ZVS operation range or improving efficiency.

The paper is organized as follows. Section II describes the behavior of the DAB converter in addition to proposing very simple averaged and small-signal models. Furthermore, the necessary and sufficient conditions to achieve ZVS are presented based on the proposed analysis. Section III presents two design strategies with different goals, increasing the ZVS operation range or improving efficiency at full load, providing an assessment of the main advantages and drawbacks of each strategy. Section IV describes different techniques to increase the ZVS operation range and efficiency of the DAB at full load, maintaining the use of simple phase-shift control. Section V presents the experimental results that verify the good performance of the proposed models, design strategies and techniques to improve the performance of the DAB. Finally, conclusions are drawn in Section VI.

II. SIMPLE AVERAGED AND SMALL-SIGNAL ANALYSIS OF THE DAB

The DAB converter (Figure 1), originally proposed in [1] and [2] and analyzed in more detail in [3]-[6], is a bidirectional DC/DC converter with galvanic isolation based on two active bridges interfaced through a high-frequency transformer (with major influence of its leakage inductance in the operation of the converter), enabling power flow in both directions in the case of active load. The transformer not only provides galvanic isolation, but also allows a high conversion ratio. For these reasons, this converter is usually chosen when the input and output voltages are quite different and hence two different designs are required for the full bridges.

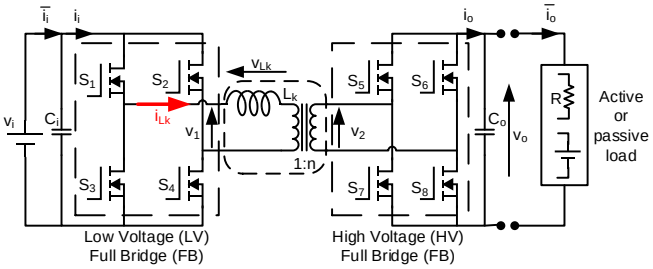


Figure 1. Schematic of the DAB converter.

The easiest way to control this topology is by switching each full bridge using complementary constant pulse-width modulated signals with a 50% duty cycle, as can be seen in Figure 2(a), which shows the main operation waveforms of this control method. Using this modulation, a high-frequency square-wave voltage signal is generated at the transformer terminals ($\pm v_i$, $\pm v_o$). Considering the presence of the leakage inductance of the transformer (with a controlled and known value) and controlling the transistors of both full bridges, the two square waves can be properly phase-shifted to regulate the power flow. These two phase-shifted signals (v_1 and v_2) generate a voltage (v_{Lk}) in the leakage inductance (L_k) of the transformer and a certain current (i_{Lk}) flows through it. This current is controlled by the phase shift between the primary and secondary voltages of the transformer (v_1 and v_2). The sign of the phase shift controls the power flow from one port (i.e. dc-source) to the other, allowing bidirectional power transfer to be achieved. Power is delivered from the bridge which generates the leading square wave. This simple control method is usually called phase-shift control [3], [5]. Figure 2(b) shows a very simplified schematic of the DAB converter considering the phase-shift control that can be used to calculate the current and voltages in the leakage inductance. As can be seen in Figure 2(a), using the phase-shift control both full bridges can be replaced by two square-wave voltage sources that generate a voltage and hence a current in the leakage inductance. Obviously, in order to remove the transformer, both square-wave voltage sources must be referred to the same point. For this reason, v_o is divided by the turn ratio of the transformer (n) in the square-wave voltage source v_2 presented in Figure 2(b).

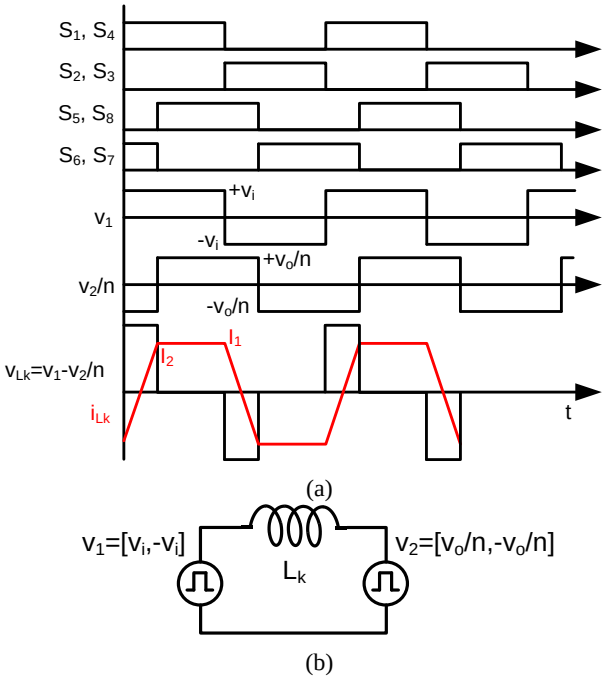


Figure 2. (a) Main operation waveforms of the phase-shift control method. (b) Simplified schematic of the DAB converter considering phase-shift control.

Figure 3(a) shows the leakage inductance current in a general case in which $v_i \neq v_o$, where d is the phase shift between v_1 and v_2, and T is half of the switching period. In Figure 3, all the currents are referred to the primary side of the transformer. Due to the symmetry of the circuit, it is only necessary to deduce the equations of the leakage inductance current for a half cycle. Figure 3(b) shows the input current in a semi-period, while Figure 3(c) shows the output current. Both current waveforms can be easily obtained from Figure 3(a) taking into account the values of v_1 and v_2. For instance, the output current (Figure 3(c)) is the same as the leakage inductance current (Figure 3(a)) when v_2 is positive, while the opposite is true when v_2 is negative. The shadowed areas of the input and output currents constitute the data used to obtain their average values.

Using Faraday's law, the leakage inductance current can be calculated as

$$\frac{di_{L_k}}{dt} = \frac{v_1 - v_2}{L_k}. \quad (1)$$

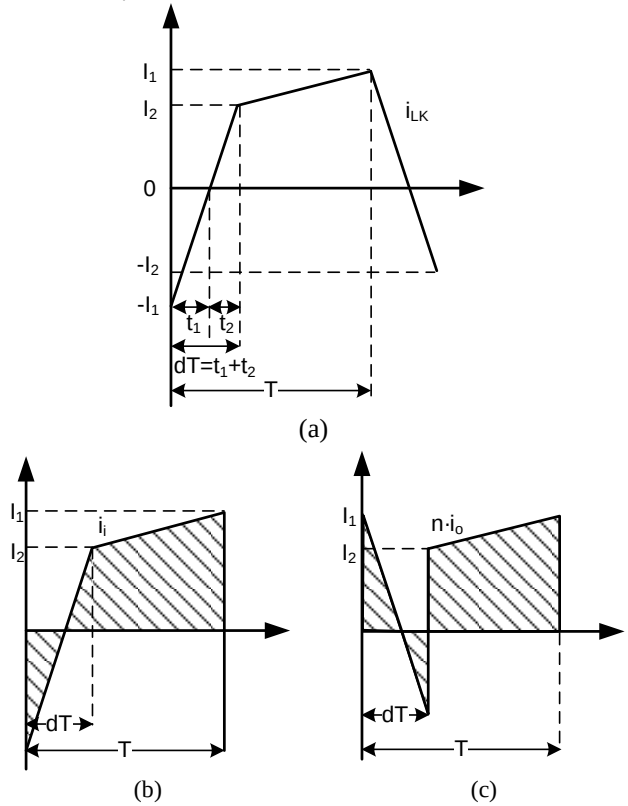


Figure 3. (a) Leakage inductance current with some important parameters. (b) Input current (i_i) and (c) output current on the primary side of the converter ($n \cdot i_o$), both used to calculate the proposed averaged model.

Considering the representation of the leakage inductance current in Figure 3(a), and solving (1) for the two different states of the converter in a semi-period, the following equations are obtained:

$$v_i + \frac{v_o}{n} = L_k \frac{I_1 + I_2}{dT}, \qquad \text{for } 0 < t < dT, \tag{2}$$

$$v_i - \frac{v_o}{n} = L_k \frac{I_1 - I_2}{(1-d)T}, \qquad \text{for dT} < t < \text{T}, \tag{3}$$

I_1 and I_2 being the respective leakage inductance current when the leading and the lagging full bridge are switched. Using the following conditions of i_{Lk}:

$$\frac{I_1}{t_1} = \frac{I_2}{t_2}, \tag{4}$$

$$t_1 + t_2 = dT, \tag{5}$$

the set of equations (2) and (3) can be solved, obtaining:

$$I_1 = \frac{T}{2L_k}\left(2\frac{v_o}{n}d + v_i - \frac{v_o}{n}\right), \tag{6}$$

$$I_2 = \frac{T}{2L_k}\left(2v_i d - v_i + \frac{v_o}{n}\right), \tag{7}$$

$$t_1 = T\left(\frac{2\frac{v_o}{n}d + v_i - \frac{v_o}{n}}{2\left(v_i + \frac{v_o}{n}\right)}\right), \tag{8}$$

$$t_2 = T\left(\frac{2v_i d - v_i + \frac{v_o}{n}}{2\left(v_i + \frac{v_o}{n}\right)}\right). \tag{9}$$

The output average current injected into the output cell, comprising the load and the output capacitor, is calculated using Figure 3(c) as

$$\overline{i_o} = \frac{1}{nT}\left(\frac{1}{2}I_1 t_1 - \frac{1}{2}I_2 t_2 + (1-d)TI_2 + (1-d)T\frac{1}{2}(I_1 - I_2)\right). \tag{10}$$

Using (6), (7), (8) and (9), the expression of the output average current (10) can be simplified as

$$\overline{i_o} = \frac{(1-d)dTv_i}{nL_k}. \tag{11}$$

Using a similar analysis to the one described previously to obtain the average output current, the average input current can be obtained as

$$\overline{i_i} = \frac{1}{T}\left(\frac{1}{2}I_2 t_2 - \frac{1}{2}I_1 t_1 + (1-d)T\frac{1}{2}(I_1 + I_2)\right). \tag{12}$$

Once again, using (6), (7), (8) and (9), the expression of the input average current can be simplified as

$$\overline{i_i} = \frac{(1-d)dTv_o}{nL_k}. \tag{13}$$

Finally, using (11) and (13), the averaged equivalent circuit of the DAB is presented in Figure 4.

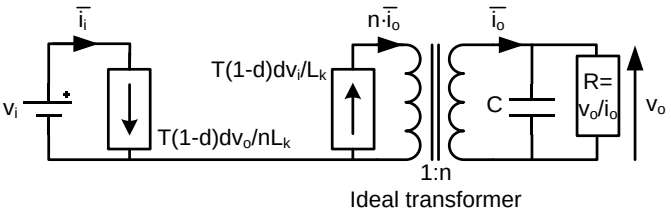


Figure 4. Simple averaged model of the DAB.

To design a feedback loop that ensures stable operation of the DAB, the small-signal dynamic model of the DAB must be analyzed. Different small-signal models have been proposed to define the dynamic properties of the DAB [7]-[10]. However, most of the proposed small-signal models take into account the effect of the parasitic components of the converter and hence are quite complex. The proposed simplified small-signal model of the DAB is obtained using the well-known averaged techniques presented in [11] and [12]. Equations of the average input and output currents, (13) and (11) respectively, are perturbed and particularized at a given operation point, obtaining the following equations:

$$\widehat{i_i} = \frac{\partial \overline{i_i}}{\partial d}|_{\widehat{v_o}=0}\hat{d} + \frac{\partial \overline{i_i}}{\partial v_o}|_{\hat{d}=0}\widehat{v_o} = g_{id}\hat{d} + g_{iv_o}\widehat{v_o}, \tag{14}$$

$$\widehat{i_o} = \frac{\partial \overline{i_o}}{\partial d}|_{\widehat{v_i}=0}\hat{d} + \frac{\partial \overline{i_o}}{\partial v_i}|_{\hat{d}=0}\widehat{v_i} = g_{od}\hat{d} + g_{ov_i}\widehat{v_i}, \tag{15}$$

where the g parameters are easily calculated from the above partial differential equations, resulting in the following values:

$$g_{od} = \frac{V_o(1-2D)}{(1-D)DR}, \tag{16}$$

$$g_{ov_i} = \frac{V_o}{V_i R}, \tag{17}$$

$$g_{id} = \frac{V_o^2(1-2D)}{V_i(1-D)DR} = \frac{V_o}{V_i}g_{od}, \tag{18}$$

$$g_{iv_o} = \frac{V_o}{V_i R}. \tag{19}$$

The small-signal model defined by (14) and (15) is represented in Figure 5 by its small-signal equivalent circuit.

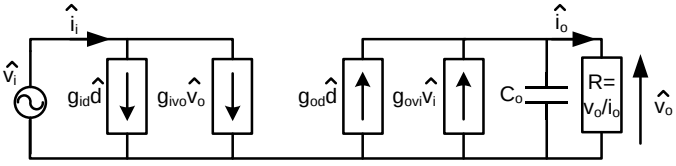


Figure 5. Simplified small-signal model.

As can be easily appreciated, the output voltage variations due to variations in both the phase shift and the input voltage have the same characteristics as a first-order system response. The aforementioned dynamic response of the converter is given by the following equation:

$$\widehat{v_o} = \frac{R}{RCs+1}(g_{od}\hat{d} + g_{ov_i}\widehat{v_i}). \tag{20}$$

A. Necessary and sufficient conditions to achieve ZVS.

One of the major advantages of the DAB is soft-switching operation of all the devices at nominal conditions. However, when the power handled by the DAB is reduced, ZVS can be lost, especially in the High Voltage (HV) full bridge. The loss of ZVS generates not only a high decrease in efficiency, but also, on some occasions, EMI problems. For these reasons, maintaining ZVS over a wide power range is an interesting design goal, especially for HV applications, in which hard-switching operation is usually avoided.

As to the ZVS operation range, which is one of the main topics of this paper, the values of the current through the leakage inductance (L_k) at two important points are especially relevant. These two values are the current through L_k when the leading and lagging full bridges are switched (I_1 and I_2, respectively). These current values, represented in Figure 2(a) and in Figure 3(a) in greater detail, are given by (6) and (7).

The necessary condition to achieve ZVS in both the leading and the lagging full bridge is that I_1 and I_2 must respectively be greater than zero. This constraint ensures that the current can flow through the parasitic body diode of the transistors that must be turned-on, providing a soft-switching turn-on.

Defining the relation between the output voltage on the primary side of the converter and the input voltage as M:

$$M = \frac{v_o}{v_i \cdot n}, \tag{21}$$

I_1 and I_2 can be easily rewritten using (6), (7) and (21) as:

$$I_1 = \frac{T v_i}{2L_k}\,(2Md + 1 - M), \tag{22}$$

$$I_2 = \frac{T v_i}{2L_k}\,(2d - 1 + M). \tag{23}$$

When M=1 (as in the case represented in Figure 2(a)), I_1 and I_2 are:

$$I_1 = \frac{T}{L_k} \cdot v_i d, \qquad if\ M = 1. \tag{24}$$

$$I_2 = \frac{T}{L_k} \cdot v_i d, \qquad if\ M = 1. \tag{25}$$

As can be easily seen, when M=1, I_1 and I_2 are equal and also higher than zero for positive phase-shift values.

However, when M is not equal to 1, the necessary condition to achieve ZVS will be fulfilled only for certain values of M and d. I_2 will always be higher than zero when M is higher than 1, as can be seen using (23), and the necessary condition to achieve ZVS will be always fulfilled. However, when M is lower than 1, the necessary condition to achieve ZVS in the lagging full bridge will be fulfilled only if the following expression is fulfilled:

$$d > \frac{1 - M}{2}. \tag{26}$$

Following a similar procedure, I_1 will be higher than zero when M is lower than 1, as can be seen in (22) (this situation is represented in Figure 3), otherwise the following expression must be fulfilled to ensure ZVS in the leading full bridge:

$$d > \frac{M - 1}{2M}. \tag{27}$$

These two necessary conditions to achieve ZVS [6] are represented in Figure 6. The *x*-axis represents the phase shift between v_1 and v_2 (d), while the *y*-axis represents the relation between the output and input voltages (M). As has been previously detailed and can be seen in Figure 6, for higher phase-shift values, which imply higher current and hence higher power, ZVS is achieved even for values of M quite different from 1. For low values of d, however, ZVS is only achieved when M is close to 1.

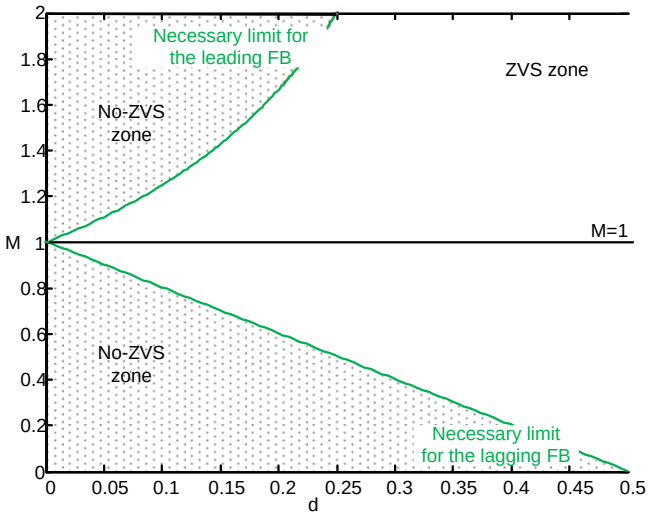


Figure 6. Representation of the necessary condition to achieve ZVS in the leading and lagging FB as a function of M and d.

As previously described, the boundaries presented here have to be fulfilled to achieve ZVS, although this condition does not ensure ZVS. To ensure ZVS, the values of I_1 and I_2 not only have to be higher than zero, but also higher than a certain value of positive current. The sufficient condition to achieve ZVS is that the stored energy in the leakage inductance at the moment when one full bridge is switched (E_{Lk}) must be higher than the stored energy in the output parasitic capacitances of the transistors that comprise the aforementioned full bridge ($E_{Coss,FB}$). This condition is represented via the following equation:

$$E_{Lk} > E_{Coss,FB} \rightarrow \frac{1}{2} L_k {i_{L_k,FBX}}^2 > 4\frac{1}{2} C_{eq} V_{FBX}^2, \tag{28}$$

where $i_{Lk,FBX}$ is the current through the leakage inductance when one full bridge is switched, and C_{eq} is the equivalent value of the output parasitic capacitances of the transistor when they are switching between 0 and V_{FBX} volts. Depending on the full bridge in which the condition is evaluated, V_{FBX} may be the input or the output voltage and $i_{Lk,FBX}$ may be I_1 or I_2.

The value of the leakage inductance current must be calculated from (28), giving:

$$i_{L_k,FBX} > 2V_{FBX}\sqrt{\frac{C_{eq}}{L_k}}. \tag{29}$$

Using (6), (7) and (29), the sufficient condition to achieve ZVS can be estimated using the following equations (where a positive power flow from the input to the output voltage source has been considered):

$$I_1 = \frac{Tv_i}{2L_k}\,(2Md + 1 - M) > 2v_i\sqrt{\frac{C_{eq\_i}}{L_k}}. \tag{30}$$

$$I_2 = \frac{Tv_i}{2L_k}\,(2d - 1 + M) > 2v_o\sqrt{\frac{C_{eq\_o}}{L_k}}. \tag{31}$$

Solving (30) and (31), the boundaries are finally obtained:

$$d > \frac{M-1}{2M} + \frac{2\sqrt{L_k C_{eq\_i}}}{TM}. \tag{32}$$

$$d > \frac{1-M}{2} + \frac{2Mn\sqrt{L_k C_{eq\_o}}}{T}. \tag{33}$$

where C_{eq_i} and C_{eq_o} are the equivalent values of the parasitic capacitances of the transistor of the input (or leading) full bridge and the output (or lagging) full bridge, respectively. The value of the equivalent capacitance can be characterized using different performance metrics depending on the required accuracy (determined by the switching frequency or the resolution required in the calculations). For example, a simple approach to estimate the equivalent capacitance is to use the value of the non-linear and voltage-dependent output parasitic capacitance of the MOSFETs (C_{oss}) at a certain voltage (C_{eq_o}=$C_{oss}(v_o)$). A more complex and precise approach is to calculate an equivalent capacitance using simulation [13]. In this paper, an average value of the nonlinear output capacitance of the transistor is used as the equivalent capacitance.

$$C_{eq\_o} = \int_0^{v_o} C_{oss}(v)dv. \tag{34}$$

Equation (32) must be fulfilled to ensure ZVS in the leading full bridge, while (33) must be fulfilled to ensure ZVS in the lagging full bridge. As can be seen, these sufficient conditions to achieve ZVS not only depend on the value of M and d, but also on some of the design parameters of the DAB, such as the switching frequency, the value of the leakage inductance and the parasitic capacitances of the selected transistors. Hence, the representation of these sufficient ZVS limits will be different for each DAB design. However, it can be easily appreciated that using these conditions, which include the influence of the parasitic capacitances of the transistors, a value of M equal to 1 does not ensure ZVS operation for the entire power range.

III. DESIGN STRATEGIES

A fairly widespread purpose design of a power supply system is to maximize efficiency. The efficiency of the converter is usually only important at full load, and maximizing efficiency at this operation point is generally the main goal of converter design. However, good efficiency over a wide power range can also be a common requirement in the design of a converter. In the particular case of the DAB converter, there is a trade-off between the efficiency of the converter at full load and the efficiency of the converter over a wide power range.

On the one hand, to obtain good efficiency over a wide power operation range, ZVS must be achieved for the entire desired operation range due to the fact that there is a sudden drop in efficiency if the converter operates with hard-switching transitions (because switching losses would be high). To achieve ZVS over a wide operation range, the value of L_k should be chosen as high as possible (to store more energy), as can be deduced from (28). Furthermore, the value of d to obtain maximum power (d_{max}) should be selected high (near the maximum value 0.5), as deduced from Figure 6, to increase the ZVS operation range.

On the other hand, the reactive current and hence the rms current handled by the converter is higher for higher values of d (in Figure 3, it can be seen that the negative part of the current is higher when d is higher). For this reason, a low value of d should be used to achieve good efficiency at full load (where conduction losses are predominant). To achieve a high value of power handled with a low value of d, the value of L_k must also be low (and obviously ZVS will be lost in a smaller operation range), as can be easily deduced from (11). The expression of the output power deduced from (11) may illustrate this concept:

$$P_o = \bar{i_o}v_o = \frac{(1-d)dTv_i v_o}{nL_k}. \tag{35}$$

Generally, the specifications of the DAB converter will be the input and output voltage and the maximum power. The switching frequency will be chosen in line with the maximum volume of the converter. The value of n (the turn ratio of the transformer) should be initially selected to obtain a value of M equal to 1 (although this could change). Taking these assumptions into consideration when designing the DAB converter, only the maximum value of d and the value of L_k need be selected, depending on the application. Two different design strategies will be presented in detail in the following subsections. It should be noted that an additional inductor is generally used in series with the leakage inductance of the transformer. In the literature on the DAB, the sum of the additional inductor in series with the leakage inductance of the transformer and the leakage inductance of the transformer itself is usually called L_k. This paper will use the same definition of L_k.

A. Design 1: aimed at increasing the ZVS operation range.

As was previously established, the highest possible values of L_k and d_{max} should be chosen to increase the ZVS

operation range. The highest value of d is theoretically 0.5; however, for a value of d close to 0.5, the nonlinearity of the output power is more severe than for lower values of d because the evolution of the output power with d is parabolic, as can be seen using (35). This is the main reason why d_{max} is generally limited to 0.4 or even 0.35. To obtain good linearity between the control parameter d and the output current or voltage (in the case of a resistor load), d_{max} is chosen as 0.35 in this study. Once the value of d_{max} has been chosen, the maximum value of L_k that allows the maximum power may be calculated directly rewriting (35) as:

$$L_k = \frac{(1-d_{max})d_{max}Tv_iv_o}{nP_{max}}. \quad (36)$$

B. Design 2: aimed at increasing efficiency at full load.

To increase efficiency at full load, the phase-shift value required to manage the maximum power must be as small as possible. A small value of d provides smaller reactive and rms currents, thus reducing conduction losses. However, the value of d cannot be reduced till zero for different reasons. On the one hand, it is very important to maintain ZVS at full load and a minimum value of d which ensures ZVS at full load is required. On the other hand, the value of d cannot be as small as zero due to certain constructive parameters (e.g. the dead-times between the switching of the transistors in the same leg of the full bridge or the resolution of the PWM modulator). A small value of d that ensures ZVS at full load, called d_{ZVS_Pmax}, is required. Once the value of d_{ZVS_Pmax} is known, probably by empirical means, the value of L_k is easily calculated using:

$$L_k = \frac{(1-d_{ZVS\_Pmax})d_{ZVS\_Pmax}Tv_iv_o}{nP_{max}}. \quad (37)$$

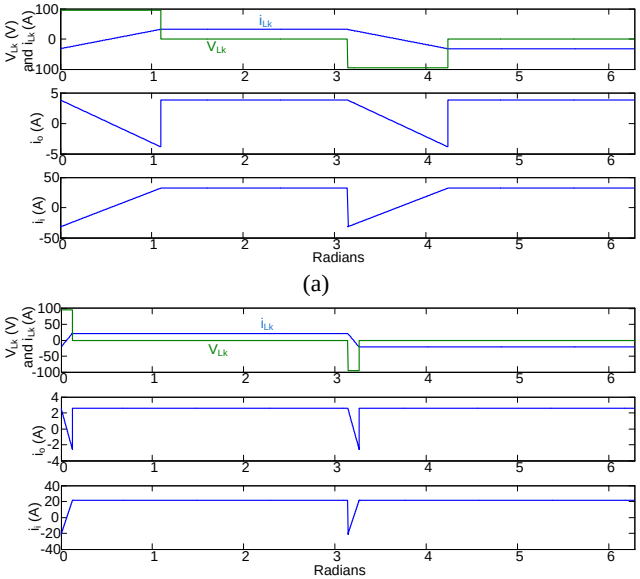
C. Comparison of the two proposed design strategies.

A set of specifications will be used as a conceptual example to compare the two design strategies. Furthermore, a realistic value of the parasitic capacitances of the transistors of both full bridges (considering the use of MOSFETs) will be selected to make the comparison. The specifications are given in Table I.

Table I. Specifications to compare different design strategies

Specifications	Selected values for the comparison
Input voltage (v_i)	48V
Output voltage(v_o)	400V
Maximum power (P_{max})	1kW
Switching frequency (f_{sw})	100kHz
Turn ratio of the transformer (n)	8
Equivalent output parasitic capacitances of the LV FB (C_{eq_i})	1000pF
Equivalent output parasitic capacitances of the HV FB (C_{eq_o})	100pF

Using the specifications in Table I, considering Design 1, a value of d_{max}=0.35 and Equation (36), the value of L_k is equal to 2.62µH. Considering Design 2, a value of d_{ZVS_Pmax}=0.04 and Equation (37), the value of L_k is equal to 0.44µH. The analytical operation waveforms at full load obtained using Design 1 and Design 2 are respectively shown in Figure 7(a) and Figure 7(b). It can be seen that the phase shift to obtain maximum power is much greater in Design 1 than in Design 2.



(a)

(b)

Figure 7. Main operation waveforms at full load for (a) Design 1 and (b) Design 2.

To compare both designs, the value of the phase shift and the power at which ZVS is lost in the HV full bridge can be estimated using the following equations:

$$d_{ZVS} = \frac{1-M}{2} + \frac{2Mn\sqrt{L_kC_{eq\_o}}}{T}. \quad (38)$$

$$P_{ZVS} = \frac{(1-d_{ZVS})d_{ZVS}Tv_iv_o}{nL_k}. \quad (39)$$

The rms current at full load may also be an important parameter to compare both strategies due to its direct relationship with conduction losses (which are dominant when ZVS is achieved). Table II shows the calculated values for the two proposed design strategies. As can be seen, the P_{ZVS} of Design 2 is more than twice the P_{ZVS} of Design 1.

Table II. Comparative parameters between the two proposed design strategies.

	Design 1. Increase the ZVS operation range	Design 2. Increase efficiency at full load
L_k(µH)	2.62	0.44
d_{max}	0.35	0.04
d_{ZVS}	0.054	0.022
P_{ZVS}(W)	234	590
i_{rms_o} (A) @ P_o=1kW	3.37	2.56

Using Equations (32) and (33), the sufficient conditions to achieve ZVS can be calculated considering both strategies and the calculated parameters for each of them. The sufficient boundaries for Design 1 are shown in Figure 8(a). The sufficient boundaries to operate with ZVS are also plotted in Figure 8(a) using the power handled by the converter as the *x*-axis instead of the value of d. As can be seen, using a value of M equal to 1, ZVS operation will be lost at approximately 230W. It can also be easily appreciated that operation with ZVS could be increased somewhat for a value of M slightly higher than 1.

Figure 8(b) shows the sufficient boundaries for Design 2. The sufficient boundaries to operate with ZVS are also plotted in Figure 8(b) using the power handled by the converter as the *x*-axis instead of the value of d. As can be seen, ZVS operation will be lost at approximately 580W using a value of M equal to 1. In this case, the range of operation with ZVS can be considerably increased using a value of M slightly higher than 1.

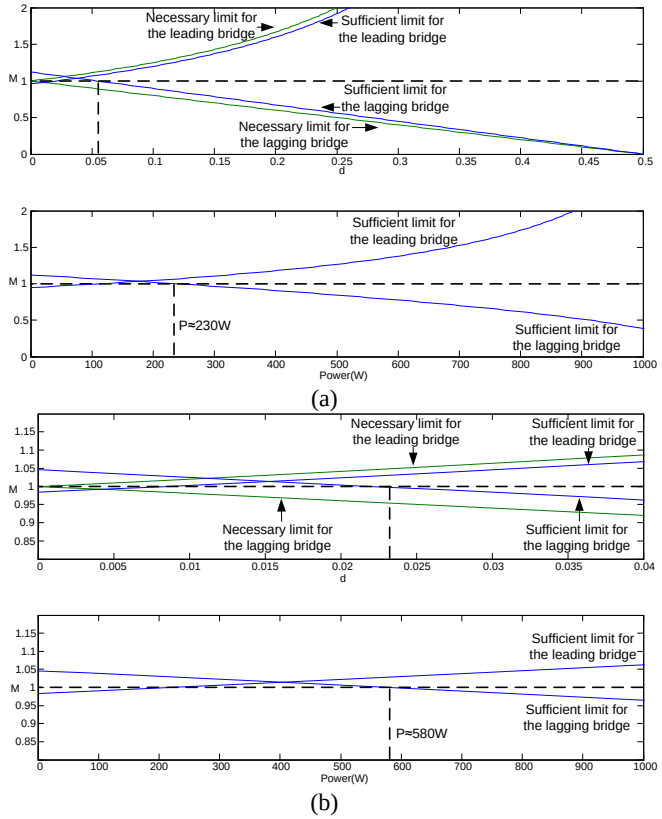


Figure 8. Representation of the necessary and sufficient conditions to achieve ZVS using d and the power as the *x*-axis. (a) Design 1 and (b) Design 2.

IV. TECHNIQUES TO IMPROVE THE PERFORMANCE OF A DAB

The design strategies presented in this paper have different purposes and obviously the specifications of the DAB converter will determine which one is the most suitable option in each application. Once the design strategy has been chosen, there are several techniques to improve the overall performance of DABs; in this case whether to increase the ZVS operation range or efficiency at full load. Some of these techniques have already been reported [13]-[25], although most of them involve changing the control (i.e. changing phase-shift control) for other kinds of controls, such as the use of a PWM signal different from 50% or introducing the phase shift between branches of the full bridges. All these techniques add complexity in comparison to phase-shift control. In this section, some techniques, both to increase the ZVS operation range and to improve efficiency at high power, will be presented without any modification in the phase-shift control. A control using a similar technique in a quite different application is presented in [26]. The idea is to maintain a simple control and to reduce the processing in a microcontroller or an FPGA. The implementation of the proposed techniques is possible thanks to the use of a digital control that allows changes in the feedback loop parameters and operation characteristics of the DAB (e.g. the switching frequency), which will be manipulated to improve its performance.

A. Modification of I_2 when ZVS is close to being lost.

The use of a transformer that introduces galvanic isolation also provides the possibility of a high conversion ratio in DABs. In this case, two quite different full bridges are required (Figure 9). A full bridge which manages a safe voltage is required on the Low Voltage (LV) port, where the main problem is usually the high current and conduction losses. A full bridge which manages unsafe voltage is needed on the High Voltage (HV) port, where switching losses are mainly the most important concern. Employing a DAB with very different input and output voltages are fairly widespread because, otherwise, the use of another bidirectional topology without galvanic isolation could provide better performance than the use of a DAB if no isolation is needed.

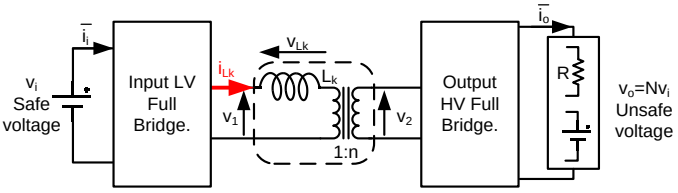


Figure 9. Scheme of the DAB showing the most usual voltage specifications.

Taking into account these assumptions, the increase in the ZVS range must be achieved ensuring ZVS in the HV full bridge, as the effect of losing ZVS in the LV full bridge is not so important. The ZVS operation range in the HV full bridge can be extended by increasing the value of I_2, which defines the energy stored in L_k used to discharge the output parasitic capacitances of the transistors in the HV full bridge (considering the scheme presented in Figure 9, where the power flows from the input to the output voltage). The value of I_2 must only be increased for currents demanded by the load close to the non-ZVS zone, not for all the operation points. For high values of current demanded by the load, where ZVS is

obtained, high values of I_2 entail high values of rms current, leading to an increase in conduction losses.

There are different ways to increase the value of I_2. For example, if the input voltage of the DAB must be maintained at a regulated value, but this value can be slightly modified, the value of the input voltage is easily reduced when the power handled by the converter is close to the power at which ZVS is lost. Unfortunately, the input voltage in DABs is usually provided by a battery; hence the input voltage will be given by the state of charge of the battery. In this case, there is another way to modify the input voltage of the DAB: a pre-regulator stage. The use of a converter between the battery and the DAB converter provides control in the input voltage of the DAB, simplifying its design. Other advantages and drawbacks should be taken into account to consider the overall performance of the electronic power system when using a pre-regulator stage. However, these considerations fall outside the scope of this study, which focuses on the performance of the DAB. This technique is graphically presented in Figure 10.

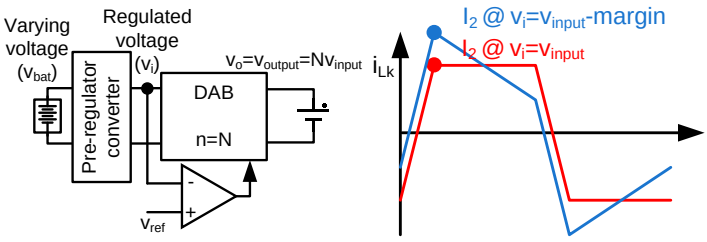


Figure 10. Technique to increase the ZVS operation range, decreasing the input voltage to increase the value of I_2.

When the power handled by the DAB converter is controlled using the phase shift (d), and considering d_{ZVS} as the phase-shift value at which ZVS is lost, the change in the reference value used to regulate the input voltage is given by:

$$v_{ref} = \begin{cases} v_{input} & , \quad d > d_{ZVS} \\ v_{input} - margin, & d \le d_{ZVS} \end{cases} \tag{40}$$

A more realistic operation condition is that the output voltage of the DAB should be regulated (also allowing some range of variation). In this case, the output voltage must be increased in order to increase the value of I_2. However, on increasing the output voltage, the energy stored in the parasitic output capacitance of the transistors is also increased. This technique can only be successfully applied when the increase in the energy stored in L_k due to the increase in I_2 is higher than the increase in the energy stored in the capacitances. This condition can be easily calculated using:

$$\Delta E_{L_k} > \Delta E_{C_{oss,F.B.}} \rightarrow L_k \Delta {I_2}^2 > 4 C_{eq} \Delta {v_o}^2 . \tag{41}$$

The increase in I_2 due to the increase in v_o is given by:

$$\Delta I_2 = \frac{T \Delta v_o}{2 L_k n}. \tag{42}$$

The condition that must be fulfilled to make this technique effective is obtained using (42) in (41), and is given by:

$$L_k \left(\frac{T \Delta v_o}{2 L_k n} \right)^2 > 4 C_{eq} \Delta {v_o}^2 \rightarrow \frac{T^2}{16 C_{eq} L_k n^2} > 1. \tag{43}$$

This technique is represented graphically in Figure 11.

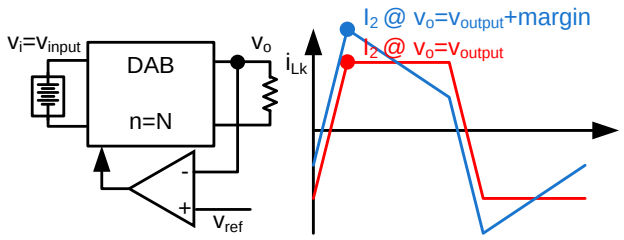


Figure 11. Technique to increase the ZVS operation range, increasing the output voltage to increase the value of I_2.

Considering the previously detailed nomenclature, the change in the reference value to regulate the output voltage is given by:

$$v_{ref} = \begin{cases} v_{output} & , \quad d > d_{ZVS} \\ v_{output} + margin, & d \le d_{ZVS} \end{cases} \tag{44}$$

If the input and output voltages must be regulated without any possibility of variation in a certain voltage range, a possible solution still exists to obtain a slightly higher value of I_2. In this case, the proposed technique entails selecting a turn ratio (n) of the transformer different to the relation between the output and the input voltage (N, being $v_o = N \cdot v_i$). If n is equal to N, the value of M will be equal to 1. With a value of M=1, the necessary condition to achieve ZVS is always fulfilled. However, using a value of M higher than 1, I_2 will be higher than I_1, thus increasing the ZVS operation range of the HV full bridge. Values of M higher than 1 can be obtained with values of n slightly lower than N. The main disadvantage is that, obviously, the value of n cannot be changed in real time for different currents managed by the DAB converter. Hence, the use of this technique entails having a higher rms current than when using a value of n=N.

B. Turn-off of the DAB converter for low power.

A number of techniques to increase the ZVS operation range by increasing the value of I_2 were presented in the previous subsection. For light loads, however, the value of I_2 inevitably falls below the minimum value of current that ensures ZVS (i_{minZVS}), even when using the previously proposed techniques. In some applications, operation under ZVS may be almost necessary, even for very light loads, a possible option being to maintain soft-switching operation by turning off the converter when the value of the current demanded by the load is lower than i_{minZVS}. This operation mode is usually called burst mode. The use of burst mode is quite widespread [27] and its implementation in a DAB is quite easy, especially when digital control is used to generate the PWM signals. Figure 12 shows a simplified scheme of burst mode operation.

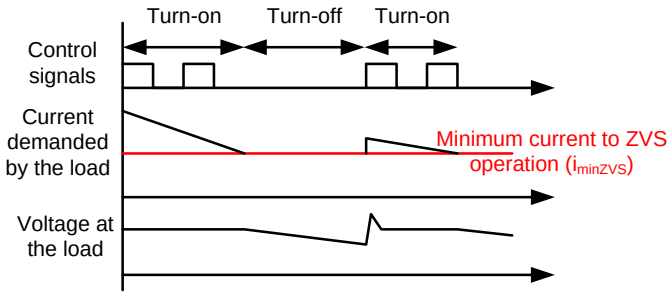


Figure 12. Illustrative explanation of burst mode operation.

The implementation of burst mode in a DAB is even easier than in other converters. In this case, the current demanded by the load can be estimated from the value of the control parameter, the phase shift (d). There is a relationship between the value of d and the value of the current injected to the load (11). As the value of d is generated by the digital control, burst mode can be activated without sensing the current demanded by the load when the value of d determines a current lower than i_{minZVS}. Burst mode can also be easily deactivated (by turning on the converter) without current sensors. When the regulator of the closed-loop control specifies a value of d that determines a current higher than i_{minZVS}, burst mode is deactivated. Using the value of d to determine the current is less precise than using a current sensor. Depending on the application and especially on the required precision, the value of the current may be easily estimated by the phase-shift ($i_o \equiv i_o(d)$), while a current sensor should be used for greater resolution ($i_o \equiv i_{o\_sense}$).

When burst mode is activated and the converter is turned-off, the current to the load is provided by the output capacitor and hence the output voltage decreases. Burst mode should also be deactivated if the specifications of the DAB converter determine a minimum voltage value (v_{omin}), seeing as this limit is reached. Figure 13 shows a scheme of the implementation of burst mode.

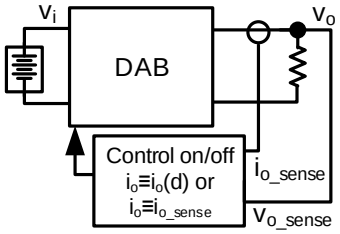


Figure 13. Technique to increase the ZVS operation range by turning off the converter for light loads.

A possible implementation of the control to turn on and turn off the DAB is given by:

$$Control = \begin{cases} turn-on, & i_o > i_{minZVS} \; o \; v_o < v_{o_{min}} \\ turn-off, & i_o < i_{minZVS} \end{cases} \quad (45)$$

C. Modification of L_k or the switching frequency.

When a DAB is designed to increase the ZVS range, the maximum power is processed by the converter with a high phase-shift value. As previously explained, this entails an increase in the rms current, conduction losses and obviously a reduction in efficiency. Some techniques can be implemented to obtain greater efficiency at high power, even using this design strategy.

The amount of power processed by the DAB converter is determined by the input and output voltages, the switching frequency, the phase shift, the value of n and the value of L_k as presented in (35). For a given design, all the aforementioned parameters are usually specified, with the exception of the phase shift, which is the control parameter and therefore must be modified to control the amount of power demanded by the load. However, both the value of L_k and the switching frequency can be appropriately modified to change the phase-shift value of required to process a given power.

The main objective is to process a great amount of power with a small phase shift. This can be achieved using a small value of L_k. However, as previously explained, small values of L_k provide small ranges of ZVS operation. Using different values of L_k for different power ranges could provide an improvement in the overall efficiency of the DAB converter. Some configurations are proposed in Figure 14 to obtain a different value of L_k for different powers processed by the DAB. Other techniques to obtain a variable inductor are presented in [28]-[30] and could be also applied to this case.

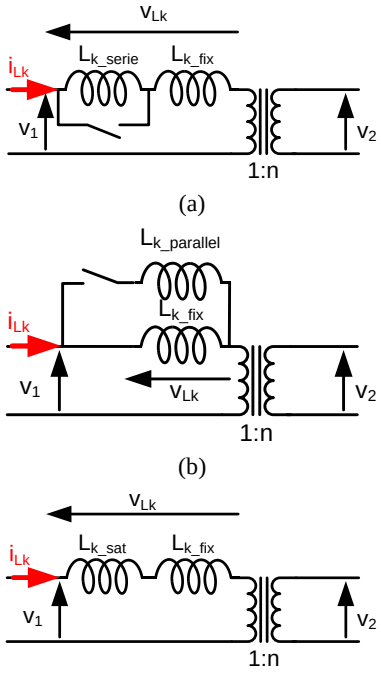


Figure 14. Possible combinations of inductances to obtain different values of L_k for different powers. (a) Series connection, (b) parallel connection, and (c) use of a saturable inductor.

The proper use of the examples shown in Figure 14 requires complex controls (e.g. connection and disconnection of inductors). However, almost the same purpose as using different inductors can be obtained by varying the switching frequency for different power levels. Thanks to the use of a digital control, modifying the frequency is much easier. F_{s1} is selected as a trade-off between switching losses and the size of the magnetic components. F_{s2} (being $F_{s2} < F_{s1}$) can be used for high powers levels (for example higher than P_1), reducing the phase shift to obtain the same power. For example, if a power of P is obtained using F_{s1} and a phase-shift of d_1, the same power P will be obtained using F_{s2} and d_2, being $d_2 = d_1 \cdot \frac{F_{s2}}{F_{s1}}$ (35). Obviously, as previously detailed, increased efficiency is achieved using a smaller phase-shift value thanks to the reduction in the rms current and conduction losses. Once again, the amount of processed power can be easily detected without a current sensor using the phase shift, which practically determines the current value. Figure 15 shows a scheme of the application of this technique in which the evaluated parameter can be an estimated value of power given by the phase shift (d) or by the sensed current if greater precision is required.

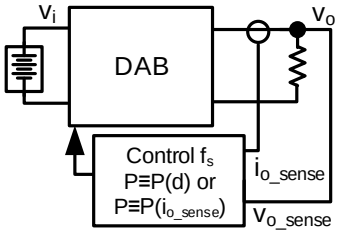


Figure 15. Technique to increase the efficiency of the DAB converter by reducing the frequency for heavy loads.

The switching frequency can be selected using the following equation (where $F_{s1} > F_{s2}$):

$$f_s = \begin{cases} F_{s2}, & P > P_1 \\ F_{s1}, & P \leq P_1 \end{cases}, \quad (46)$$

V. Experimental results.

Some experimental results will now be presented to validate the previously proposed models, design strategies and techniques to improve the performance of the DAB converter. All the experimental results were obtained using a DAB prototype with the specifications given in Table I. Figure 16 shows the experimental setup developed by the authors. The current sensors were implemented to verify the input and output currents, but are not used in the control techniques presented here because these currents can be estimated using the phase shift. Table III specifies the main components used to develop the prototype for the nominal specifications given in Table I.

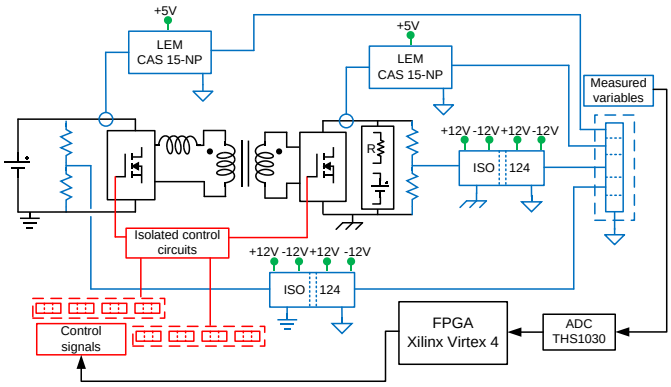


Figure 16. Experimental setup of the DAB converter.

Table III. Components used to develop the DAB prototype and the experimental setup.

Component	Description
Input Low Voltage MOSFETs (S1-S4)	IRFB4310Z
Output High Voltage MOSFETs (S5-S8)	IPW60R280C6
Transformer	ETD59+3F3. n=8. N_1=5 / N_2=40
Leakage inductance (L_k)	Design 1: ETD39+3F3. N=7. L_k=2.6µH Design 2: ETD29+3F3. N=3. L_k=0.4µH
Digital control Platform	FPGA Xilinx Virtex 4
A/D Converter	THS1030

On most occasions, efficiency results will be presented to provide a comparison between different design strategies or improvement techniques, although the implementation of different techniques could also entail further advantages or drawbacks that should be taken into account depending on the particular specifications of each application. These efficiency results should be considered only as comparative results. The efficiency measurements were obtained once the converter had reached the stable temperature point of operation. Small heat sinks were used in all the transistors without any forced cooling device. Input and output voltages (v_i and v_o) and currents ($\overline{i_i}$ and $\overline{i_o}$) were measured using four calibrated digital multimeters (FLUKE 187) to obtain these efficiency results (in which control and driver losses were ignored) by means of the following equation:

$$\eta(\%) = \frac{v_o \overline{i_o}}{v_i \overline{i_i}} \cdot 100\,. \quad (1)$$

There is a substantial scatter on some experimental curves, however the tendency of the efficiency curves follows the previously analyzed theoretical results. The obtained efficiency values are considered good enough to make a comparison between the different proposed designs and techniques because all of them have been obtained following the same procedure and in the same conditions.

A. Proposed averaged and small-signal model.

To validate the proposed averaged model presented in (11), (13) and Figure 4, simulation was carried out and experimental results obtained. Simulation of the complete DAB converter (switching model) provides almost the same results as simulation of the averaged circuit. Furthermore, the experimental and simulation results (both averaged model and complete DAB converter) are very similar, as can be seen in Figure 17.

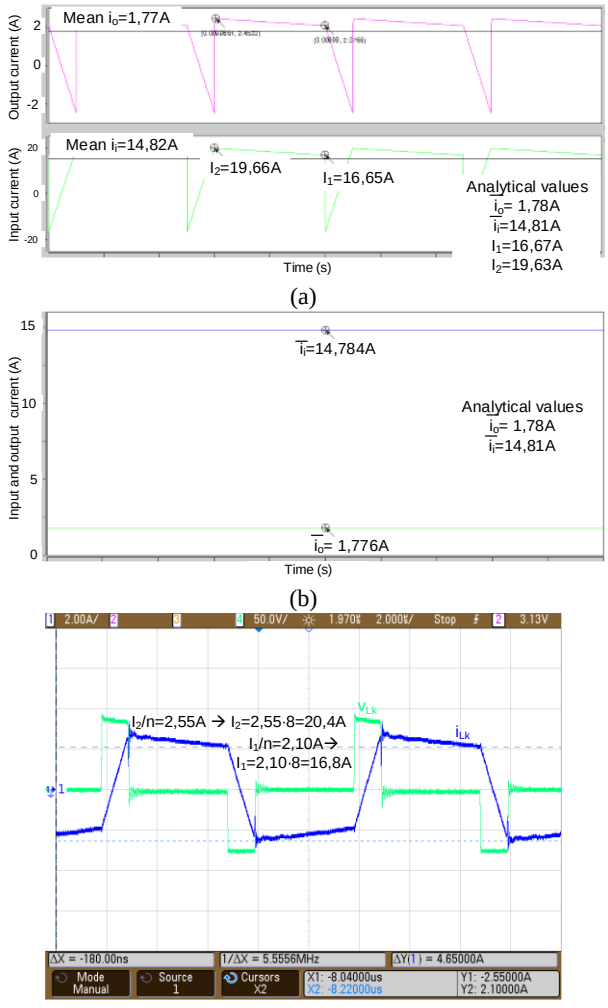


Figure 17. Validation of the proposed averaged model. Interesting current values, such as I_1 and I_2, are highlighted. (a) Simulation of the switching model of the DAB converter, (b) simulation of the proposed averaged model, and (c) experimental results.

Table IV shows a summary of the results. An easy comparison can be carried out. Slight differences can be seen in the experimental results, mainly due to the effect of parasitic components and the efficiency of the converter (≈94%). However, analytical, simulation and also experimental results provide a very accurate match.

To validate the proposed small-signal model presented in Equations (14)-(19) and Figure 5, simulation was carried out and experimental results obtained. As in the case of the averaged model, simulation of the complete DAB converter (switching model) once again provides almost the same results as simulation of the averaged circuit and the analytical results obtained using Equation (20). Simulation, analytical and experimental results are presented in Figure 18, in which a small step in the phase shift is applied (from d=0.15 to d=0.16) and the evolution of the output voltage is presented (using an output capacitance of C_o=0.5µF). As can be seen, a slight difference exists in the experimental results due to the efficiency of the prototype that is not taken into consideration in the simulations.

B. Design strategies.

An experimental comparison of the two proposed design strategies is presented in this section. Two identical prototypes, with the only exception of the additional inductor used to determine the value of L_k, were developed and compared. The values of the leakage inductance for each strategy are given in Table II. Figure 19 shows the efficiency comparison.

As can be seen, when a smaller value of L_k is used, a higher power is processed using a lower phase shift thus achieving greater efficiency. An improvement in efficiency of almost 3 points at full load is achieved with the design that minimizes the phase shift. However, the ZVS operation range is much narrower than in the design with a higher value of L_k. The power value at which ZVS is lost can be clearly appreciated, showing a drastic drop in efficiency. These experimental power values are very similar to the analytical P_{ZVS} values previously shown in Table II.

Table IV. Comparison of analytical (MatLab), simulation (Saber) and experimental results

	Analytical results	**Switching model simulation results**	**Averaged model simulation results**	**Experimental results**
Average input current ($\overline{i_i}$)	14.81A	14.82A	14.81A	15.8A
Average output current ($\overline{i_o}$)	1.78A	1.77A	1.78A	1.79A
L_k current when the leading bridge switches (I_1)	16.67A	16.65A	X	16.8A
L_k current when the lagging bridge switches (I_2)	19.63A	19.66A	X	20.4A

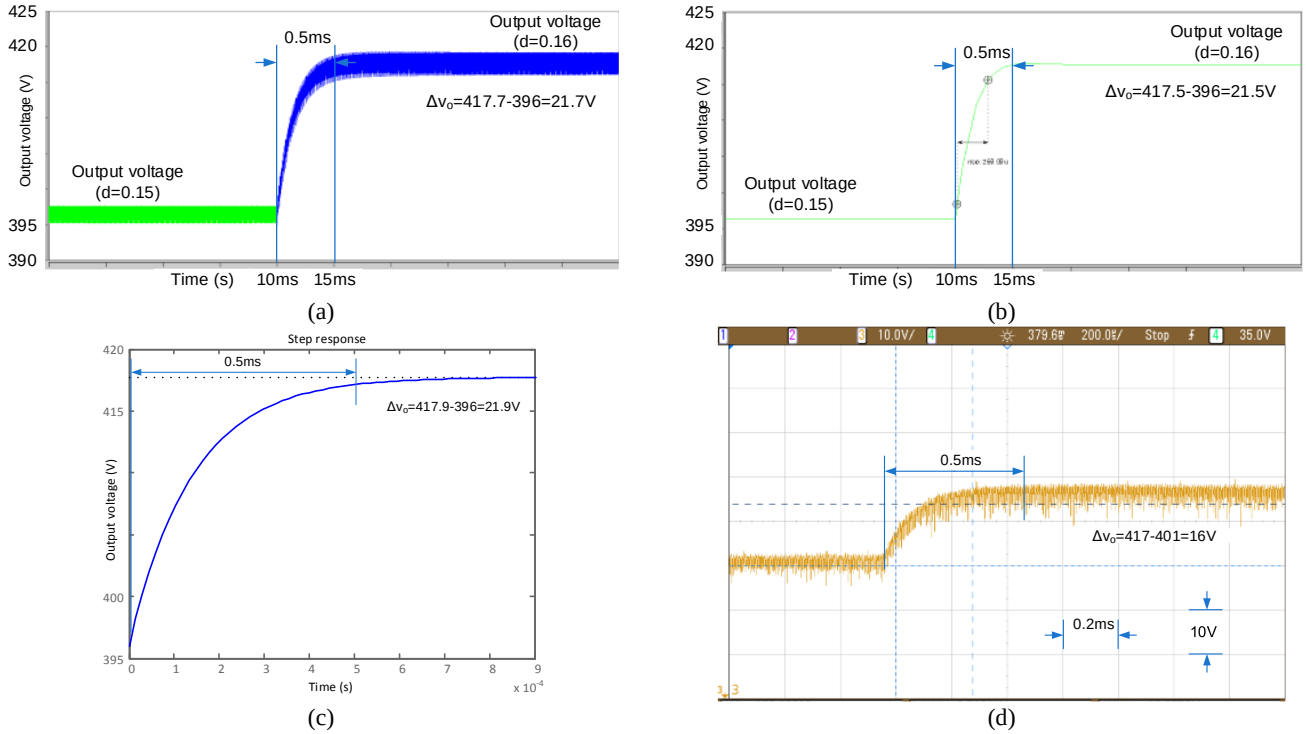


Figure 18. Validation of the proposed small-signal model for changes in the phase shift. Evolution of the output voltage of (a) the switching model simulation of the DAB, (b) the proposed averaged model, (c) the proposed analytical small-signal model (20), and (d) the prototype.

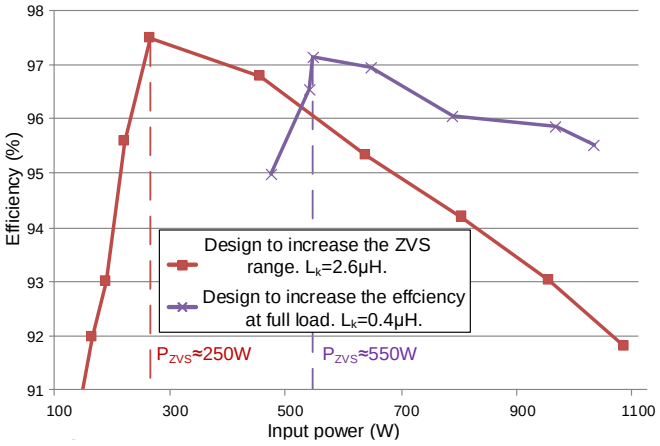


Figure 19. Efficiency results for the two different design strategies.

The main operation waveforms at full load are shown in Figure 20 for the two design strategies. As can be seen, both converters are processing a similar power with very different phase-shift values and hence different levels of efficiency.

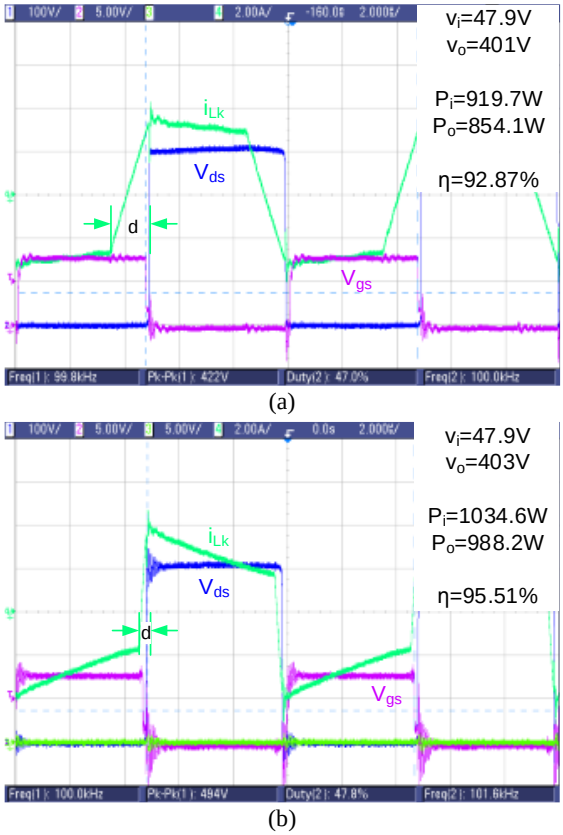


Figure 20. Representative operation waveforms for the two design strategies. (a) Design to increase the ZVS operation range with L_k=2.6μH, and (b) design to increase efficiency at full load with L_k=0.4μH.

C. Techniques to improve the performance of a DAB.

To experimentally verify the interest of the techniques presented in this paper to improve the performance of a DAB (ZVS operation range or efficiency for high power), a number of different tests were carried out mainly using the previously presented prototype. Slight modifications to the main specifications are mandatory to validate some techniques and these will be clearly highlighted. It should be noted that the success of each of these techniques will be mainly given by the specifications of the application. The comparison between the different techniques will be given in terms of the overall efficiency of the DAB converter, although further advantages or drawbacks should be taken into account between the different techniques (e.g. the effect of modifying the frequency or the variation in the input or output voltages).

First, an efficiency comparison between the same DAB prototype modifying the input or output voltage is presented in Figure 21. The main objective is to change the input or output voltage for low power in order to increase the ZVS operation range. For the previously mentioned specifications, the value of I_2 must be increased in order to increase the ZVS operation range. This can be achieved by decreasing the input voltage or increasing the output voltage. In Figure 21, the input voltage has been decreased almost 10% from its nominal value, while the output voltage has been increased 5%. As can be seen, the ZVS operation range has increased slightly in both cases.

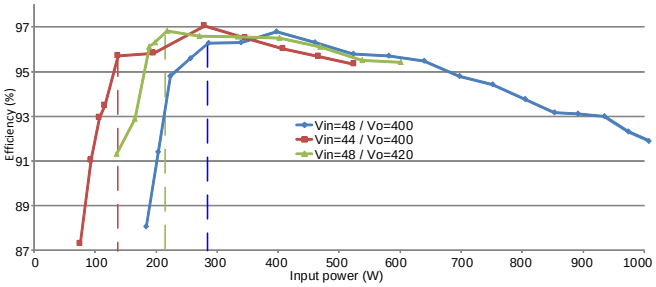


Figure 21. Efficiency comparison of the same DAB with slight variations of the input or output voltage to increase the ZVS operation range.

A comparison of the sufficient conditions to achieve ZVS as a function of the power handled by the converter between the same DAB specifications presented in Figure 21 can likewise be obtained using (33). Figure 22 shows the comparison, in which a good match between analytical and experimental results is obtained. As can be seen, the power at which ZVS is lost for different specifications (which may be an important parameter for the design of the DAB) can be easily estimated using the analytical results. The main difference is given by the change in the value of M provided as a result of the change in the input or output voltage.

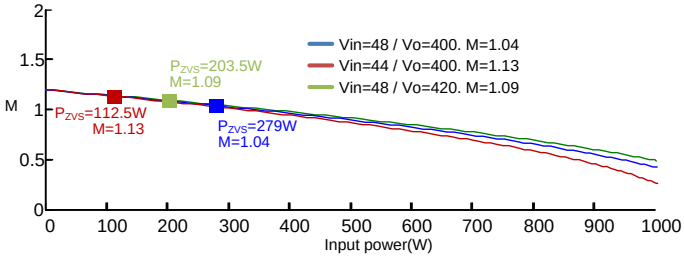


Figure 22. Necessary boundary conditions to achieve ZVS as a function of the power and M.

To increase the ZVS operation range even more, burst mode can be activated for light loads, turning the DAB on and off to ensure that the converter processes a higher current than the minimum current that ensures ZVS even when its average value defines a low-load operation. Using this technique, ZVS can be achieved even for a very light load. The main drawback is the unavoidable ripple that will appear in the regulated voltage. The efficiency obtained by activating burst mode for light loads is shown in Figure 23. As can be seen, although the efficiency is low for very light loads, the decrease in efficiency is not so drastic, given that ZVS is not lost (the minimum efficiency is higher than 85%). Figure 23 also serves to show the bidirectional power flow that can be automatically achieved in the DAB converter.

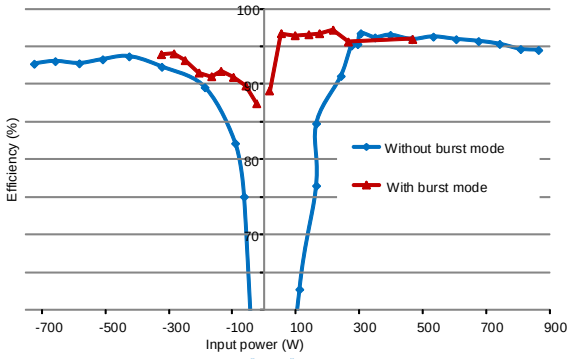
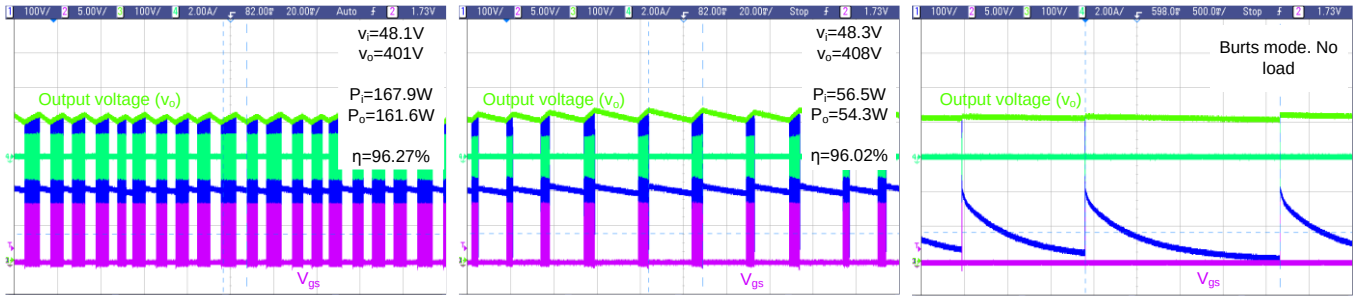


Figure 23. Efficiency comparison using burst mode.



(a) (b) (c)

Figure 24. Main operation waveforms when burst mode is activated for an output power of (a) 161.6W, (b) 54.3W, and (c) without load.

Depending on the load, burst mode can operate by turning off the converter only for a few switching cycles or for longer periods of time. Even at no load, the converter can correctly regulate the voltage in burst mode by only turning on the converter in a few cycles to maintain a good level of efficiency. The ripple due to the use of burst mode depends on the power limit at which this mode is activated and the voltage limits used to activate and deactivate the DAB when it is operating in burst mode. In the example presented here, a simple control loop has been designed using the previously proposed small-signal model to regulate the output voltage (v_{ref}=410V). A higher level control activates burst mode when the phase shift determined by the control loop entails a processed power lower than 250W. When the DAB is operating in burst mode, the high level control turns on the DAB (with a fixed phase shift) when its output voltage is lower than V_{ref} -10 and turns it off when its output voltage is higher than V_{ref} +10. Burst mode is deactivated when the DAB is turned on and the output voltage is lower than V_{ref} -10 during a few cycles (approximately 10ms). Using this setup, the voltage ripple is about 5% the nominal voltage, although it could be reduced by sensing the output voltage with greater precision and using a narrower margin of the variation in the output voltage. Figure 24 shows the main operation waveforms for different loads.

Finally, the efficiency results obtained by decreasing the switching frequency for high loads are presented in Figure 25. As can be seen, using the nominal conditions of Design 1 to increase the ZVS operation range, the efficiency of the DAB is much higher at full load when the switching frequency is decreased. At approximately half the maximum power, the efficiency results are virtually the same for all the tested switching frequencies and hence the switching frequency should be changed back to the nominal value. Using digital control, a change in the switching frequency is much easier than the connection and disconnection of inductors or even the use of variable or saturable inductors. For this reason, the frequency change technique was chosen to verify the improvement in efficiency at high power. As can be seen, the efficiency of the DAB is 3 points higher at full load using half the nominal switching frequency.

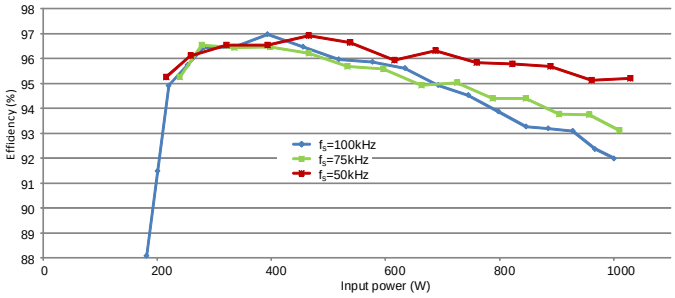


Figure 25. Efficiency comparison for different switching frequencies.

VI. CONCLUSIONS

This paper focuses on the study of a DAB bidirectional converter for battery management and renewable energy applications. Quite simple averaged and small-signal models of this topology are presented. Using the basic averaged model, a dynamic characterization of this converter can be made and subsequently used to calculate and design the control loops for this topology.

One important advantage of the DAB converter is its high efficiency, mainly thanks to operation with ZVS in all its switches. This paper presents an analysis of the trade-off between the ZVS operation range and the amount of reactive current handled by the converter. ZVS operation boundaries, considering not only the necessary, but also the sufficient conditions that must be met by the converter based on the previously proposed averaged model, are evaluated. Furthermore, different design strategies that can provide a broader ZVS operation range or greater efficiency at full load are proposed.

Another important advantage is the easy control that can be used to manage the power handled by the DAB converter. However, using the easiest way of controlling the converter (i.e. phase-shift control), the ZVS operation range may be narrower than when using other more complex controls. A number of techniques to enlarge the ZVS operation range while maintaining phase-shift control are presented in this paper. Some techniques to improve efficiency at high power are likewise presented. A substantial improvement in the overall performance of the DAB converter can be achieved by combining a good choice of design strategy and the use of some of the proposed techniques (considering the particular specifications of each application). Depending on the specifications of a particular application some of these techniques could be implemented. It is important to remark that some of the presented techniques (voltage changes and burst mode) are oriented to increase the ZVS operation range while the modification in the switching frequency is oriented to increase the efficiency at high power.

VII. ACKNOWLEDGMENT

This work has been supported by the Spanish Government under projects CONSOLIDER MICINN-10-CSD2009-00046, MICINN-10-DPI2010-21110-C02-01, FPI grant BES-2011-044114 and FPU grant AP2008-03380.

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